

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner,

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,
Patent Owner.

IPR2024-00789
Patent 10,861,872 B2

Before JO-ANNE M. KOKOSKI, KIMBERLY McGRAW, and
MICHAEL T. CYGAN, *Administrative Patent Judges*.

KOKOSKI, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

Micron Technology, Inc. (“Petitioner”) filed a Petition to institute an *inter partes* review of claims 1–6 and 11–13 of U.S. Patent No. 10,861,872 B2 (“the ’872 patent,” Ex. 1001). Paper 1 (“Pet.”). Yangtze Memory Technologies Company, Ltd. (“Patent Owner”) filed a Preliminary Response. Paper 11 (“Prelim. Resp.”). With Board authorization (Paper 12), Petitioner filed a Reply (“Prelim. Reply,” Paper 13), and Patent Owner filed a Sur-reply (“Prelim. Sur-reply,” Paper 14), to the Preliminary Response.

Institution of an *inter partes* review is authorized by statute when “the information presented in the petition . . . and any response . . . shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” 35 U.S.C. § 314 (2018); *see also* 37 C.F.R. § 42.4 (2023). For the reasons discussed below, we determine that Petitioner establishes a reasonable likelihood of prevailing with respect to the unpatentability of at least one claim of the ’872 patent. Accordingly, we institute an *inter partes* review of claims 1–6 and 6–13 of the ’872 patent.

A. *Real Parties in Interest*

Petitioner identifies “Micron Technology Inc. and its subsidiaries, including Micron Consumer Products Group LLC” as the real parties in interest. Pet. 7. Patent Owner identifies itself as the real party in interest. Paper 5 (Mandatory Notice), 2.

B. *Related Matters*

The parties indicate that the ’872 patent is asserted in *Yangtze Memory Techs. Co., Ltd. v. Micron Tech. Inc.*, Case No. 3:23-cv-05792-RFL (N.D. Cal.). Pet. 7; Paper 5, 2.

C. The '872 Patent

The '872 patent relates “to three-dimensional (3D) memory devices” that include “a substrate, a memory stack including interleaved conductive layers and dielectric layers on the substrate, and a staircase structure on one side of the memory stack” with a plurality of dummy source structures vertically extending through the staircase structure that surround the staircase contact. Ex. 1001, 1:15–17, 1:34–43.

Figure 1A is reproduced below.

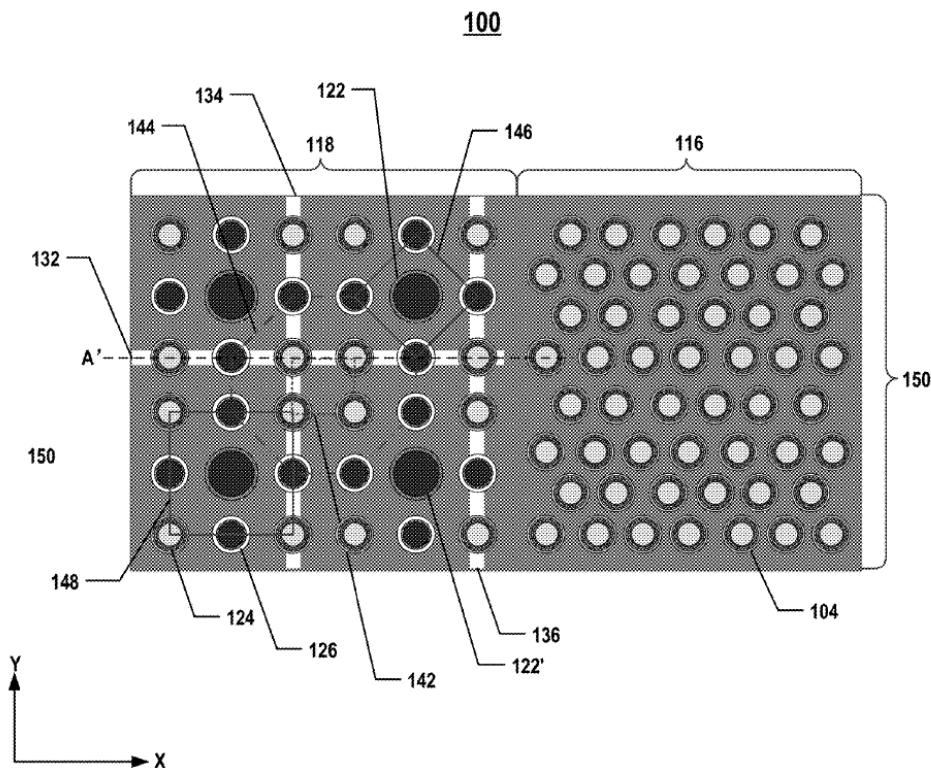


FIG. 1A

Figure 1A illustrates a plan view of a 3D memory device described in the '872 patent. Ex. 1001, 2:38–40. Memory device 100 includes memory region 150, which further includes inner region 116 (the “core region array”) and outer region 118 (the “staircase region”). *Id.* at 6:15–19. Staircase region 118 includes staircase contacts 122, plurality of dummy channel

structures 124, and plurality of dummy source structures 126 distributed among dummy channel structures 124 and staircase contacts 122. *Id.* at 6:31–35. Staircase contacts 122, dummy channel structures 124, and/or dummy source structures 126 may be arranged in any suitable pattern, such as the dummy source structures indicated by diamond shape 146 that surrounds staircase contact 122. *Id.* at 6:35–41. At least two dummy source structures may be arranged in each of first row 132 that extends along a first lateral direction (x direction), second row 134 that extends in a second lateral direction (y direction) perpendicular to the first lateral direction, and third row 136 that extends in a third lateral direction in parallel with the first or the second lateral direction. *Id.* at 6:51–58, 7:1–4.

The '872 patent teaches that the four dummy structures comprising diamond shape 146 “may be located adjacent to staircase contact 122” such that “there is no other components such as dummy channel structures, dummy source structures, and staircase contacts between staircase contact 122 and each of the four dummy source structures.” Ex. 1001, 6:41–46. Also, the four dummy source structures “may be spaced with nominally equal lateral distances to staircase contact 122.” *Id.* at 6:46–48.

D. Illustrative Claim

Petitioner challenges claims 1–6 and 11–13 of the '872 patent. Claim 1, the only independent claim challenged, is illustrative of the claimed subject matter and is reproduced below.

1. [1.PRE] A three-dimensional (3D) memory device, comprising:
 - [1.A] a substrate;
 - [1.B] a memory stack comprising interleaved conductive layers and dielectric layers on the substrate;

- [1.C] a staircase structure on one side of the memory stack;
- [1.D] a staircase contact in the staircase structure; and
- [1.E] a plurality of dummy source structures each extending vertically through the staircase structure, the plurality of dummy source structures surrounding the staircase contact,
- [1.F] wherein each of the dummy source structures comprises a conductive contact.

Ex. 1001, 20:5–16 (bracketed material added).

E. Asserted Grounds

Petitioner asserts that claims 1–6 and 11–13 would have been unpatentable on the following grounds:

Claim(s) Challenged	35 U.S.C. §	Reference(s)/Basis
1–6, 11, 13	103 ¹	Park ²
1–6, 11–13	103	Tessariol ³

Pet. 8. Petitioner relies on the Declaration of Sanjay Banerjee, Ph. D. (“Banerjee Dec.,” Ex. 1003) in support of its contentions. Patent Owner submits the Declaration of Kelin Kuhn, Ph.D. (“Kuhn Dec.,” Ex. 2001) in support of its Preliminary Response.

II. ANALYSIS

A. Level of Ordinary Skill in the Art

Petitioner contends that a person of ordinary skill in the art (“POSITA”) would have had “a bachelor of science degree in electrical

¹ The Leahy-Smith America Invents Act (“AIA”), Pub. L. No. 112–29, 125 Stat. 284 (2011), revised 35 U.S.C. §§ 102 and 103 effective March 16, 2013. Because the ’872 patent has an effective filing date after March 16, 2013 (Ex. 1001, codes (22), (63)), we refer to the AIA version of Sections 102 and 103.

² Park, US 9,859,297 B2, issued Jan. 2, 2018 (Ex. 1005).

³ Tessariol, US 2019/0081061 A1, published Mar. 14, 2019 (Ex. 1006).

engineering or a similar discipline” with “2–3 years of professional experience working with (e.g., researching, designing, or teaching) monolithic 3D structures and NAND memory devices,” or “an equivalent level of skill, knowledge, and experience (e.g., an advanced degree may replace some of the professional experience).” Pet. 33. Petitioner further contends that a “POSITA would have been aware of and generally knowledgeable about 3D NAND’s structure, how it is manufactured, and its component parts.” *Id.* (citing Ex. 1003 ¶¶ 40–43). At this stage of the proceeding, Patent Owner neither responds to Petitioner’s proposed definition, nor provides a definition of its own. *See generally*, Prelim. Resp. Petitioner’s undisputed proposed definition appears to be consistent with the cited prior art and the disclosure of the ’872 patent, and we adopt it for purposes of this Decision. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001) (explaining that specific findings regarding ordinary skill level are not required “where the prior art itself reflects an appropriate level and need for testimony is not shown” (quoting *Litton Indus. Prods., Inc. v. Solid State Sys. Corp.*, 755 F.2d 158, 163 (Fed. Cir. 1985))).

B. Claim Construction

We construe each claim “in accordance with the ordinary and customary meaning of such claim as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent.” 37 C.F.R. § 42.100(b). Under this standard, claim terms are generally given their plain and ordinary meaning as would have been understood by a person of ordinary skill in the art at the time of the invention and in the context of the entire patent disclosure. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1313 (Fed. Cir. 2005) (en banc). Only those terms in controversy need to be construed,

and only to the extent necessary to resolve the controversy. *Realtime Data LLC v. Iancu*, 912 F.3d 1368, 1375 (Fed. Cir. 2019).

The parties propose constructions for the terms “dummy source structure” and “surrounding” in claim 1. Pet. 24–32; Prelim. Resp. 15–26.

1. “*dummy source structure*”

Claim 1 recites, in relevant part “a plurality of dummy source structures each extending vertically through the staircase structure, the plurality of dummy source structures surrounding the staircase contact, wherein each of the dummy source structures comprises a conductive contact.” Ex. 1001, 20:11–16. Petitioner argues “that the term ‘dummy source structure’ would have been understood to mean ‘a structure that occupies the void that was used for the gate replacement process.’” Pet. 24.

Petitioner argues that “[t]he ’872 Patent seeks to address 3D memory structural issues that arise during the gate replacement process ‘by replacing the [gate line slits] with dummy source structures.’” *Id.* (citing Ex. 1001, 5:30–34). Petitioner notes the ’872 patent explains that, in the gate replacement process, the gate line slits’ large dimensions create problems such as unevenness and gaps in gate electrodes, and “[t]he large area of gate line slits also ‘limit[s] the usable space on the wafer surface to place other components, such as staircase contacts.’” *Id.* at 24–25 (citing Ex. 1001, 4:44–50, 4:65–67; Ex. 1003 ¶ 74). Petitioner argues that “the ’872 Patent describes solving the[se] alleged problems by using the voids that are later occupied by the ‘dummy source structures,’ namely, ‘dummy source holes.’” *Id.* at 25. Petitioner argues that

the ’872 Patent discloses that because the “gate replacement process can be performed to deposit a conductive material **through the dummy source holes that subsequently form the dummy source structures,**” the “conductive material

travels shorter distances to fill up the lateral recesses for forming the gate electrodes.” Ex. 1001, 5:49–58. Nonetheless, the specification defines the “dummy source structures” as what occupies the “dummy source holes”: “dummy source holes that subsequently form the dummy source structures.” *Id.* Thus, when the ’872 Patent states that it is “replacing the [gate line slits] with dummy source structures” (*Id.*, 5:30–34), what it means is it is “replacing the [gate lines slits] with [dummy source holes in which the dummy source structures are subsequently formed].” *Id.*, 4:65–67; Banerjee ¶¶ 76–77.

Pet. 25–26 (alterations in original).

Petitioner further argues that the ’872 patent “does not impose any meaningful limitation on the actual structure of the dummy source structure (the claims only require that the structures include a conductive contact).”

Pet. 26. According to Petitioner, the ’872 patent teaches that the dummy source structures can have different layouts, patterns and designs based on the size of the staircase region, and “that ‘dummy source structures’ can ‘contact with the substrate and may provide interconnect between the 3D memory device and peripheral devices.’” *Id.* at 26–27 (citing Ex. 1001, 5:41–43, 8:51–53, 16:63–66; Ex. 1003 ¶¶ 79–80).

Patent Owner responds that “[t]he term ‘dummy source structure’ should be construed according to its plain and ordinary meaning as a structure that does not function as a source.” Prelim. Resp. 15. Patent Owner contends that, “as the qualifying term ‘dummy’ suggests,” dummy source structures function “as a mechanical supporting structure.” *Id.* at 16 (citing Ex. 1001, 16:38–44). Patent Owner contends that the ’872 patent explains that

the dummy source hole is filled with “dielectric materials, conductive materials, or any combination thereof” so that a “dummy source structure 246 including spacer 242 and contact 244 is thereby formed in the dummy source hole.”

Ex. 1001, 16:28–31, 16:56–63. “When conductive materials are used to fill dummy source hole 212 (e.g., contact 244), the dummy source structure 246 may function as an interconnect to connect 3D memory device 100 with other peripheral devices,” and “[w]hen dielectric materials are used to fill dummy source hole 212, dummy source structure 246 may function as a mechanical support structure to improve the stability of the staircase region.” Ex. 1001, 16:63–17:3. At no point does the specification suggest that a dummy source structure can function, in contradiction to its name, as a source to the memory cells.

Prelim. Resp. 16.

Patent Owner also contends that Petitioner’s proposed construction “fails to differentiate between dummy source structures and non-dummy source structures (*i.e.*, actual source structures that function as the source for memory cells).” Prelim. Resp. 17. Patent Owner further contends that “Petitioner’s proposed construction impermissibly attempts to limit the language of an apparatus—here, the claimed three-dimensional memory device—in such a way as to dictate the process by which the apparatus is made.” *Id.* at 18. Moreover, according to Patent Owner, Petitioner does not show “that the ‘gate replacement process’ required by its construction is an essential part of the claimed invention such that it should be read into the claims through the construction of ‘dummy source structure.’” *Id.* at 19. In particular, Patent Owner notes that “the specification repeatedly qualifies use of the ‘gate replacement process’ as merely one possible manufacturing method.” *Id.* at 20 (citing Ex. 1001, 4:30–33, 5:52–55, 16:40–49); *see also id.* at 21 (“Petitioner’s construction attempts to impermissibly narrow the scope of the claim by limiting it to one particular disclosed embodiment: gate replacement process.”).

Petitioner replies that Patent Owner’s proposed construction would read out an express embodiment because, “[b]y stating that a ‘dummy source structure’ *may not* function as a source ‘[i]n some embodiments,’ it follows that a ‘dummy source structure’ *may* function as a source in other embodiments.” Prelim. Reply 2 (emphases in original). Petitioner also argues that “the specification states that when the dummy source structure includes a conductive core, it ‘may function as an interconnect,’ **not** a support structure.” *Id.* at 4 (citing Ex. 1001, 16:66–17:3). Petitioner further argues that Patent Owner’s “construction also cannot be correct because it includes a negative limitation which renders the term meaningless: a tree house is ‘a structure that does not function as a source,’ but qualifies as a ‘dummy source structure’ under” the proposed construction. *Id.* at 5.

Patent Owner responds that the ’872 patent “discloses both ‘dummy source structures’ and ‘source structures,” and “uses the qualifier ‘dummy’ to distinguish the two types of structures.” Prelim. Sur-reply 2 (citing Ex. 1001, 16:33–38). Patent Owner contends that although “dummy source structures may function as ‘interconnects,’” the ’872 patent “nowhere describes dummy source structures functioning as a source to the memory cells.” *Id.* (citing Ex. 1001, 5:40–43, 11:46–49, 16:66–17:3). Patent Owner also contends that Petitioner does not identify any intrinsic evidence “where the term ‘source’ means ‘source for deposition materials,’” and that the ’872 patent consistently uses “source” “in reference to source to gates of the memory cells.” *Id.* at 3 (citing Ex. 1001, 16:33–38, 11:8–9). Patent Owner further contends that the ’872 patent “explains that ‘the dummy source structure 246 may function as an interconnect to connect 3D memory device 100 **with other peripheral devices**’—not as an interconnect to a

supply that provides source to the memory cells.” *Id.* at 4 (citing Ex. 1001, 16:66–17:3) (emphases in original).

Having reviewed the claim language, the Specification, and the record currently before us, we determine, for purposes of this Decision, that “dummy source structure” is a structure that does not function as a source to the memory cells.

The Specification teaches that “[e]ach dummy source structure may include an insulating spacer layer in a dummy source hole and a conductive contact within the spacer layer.” Ex. 1001, 5:37–40; *see also id.* at 11:39–43 (“Dummy source structure 178 can further include a spacer 177 made of any suitable dielectric materials (e.g., silicon oxide) between contact 179 and memory stack 160 to electrically separate surrounding conductive layers 106 in memory stack 160 from contact 179.”). The Specification further teaches that “[i]n some embodiments, one or more dummy source structures are in contact with the substrate and may provide interconnect between the 3D memory device and peripheral devices.” *Id.* at 5:40–43; *see also id.* at 11:46–49 (“In some embodiments, dummy source structures 178 may function as interconnects to connect 3D memory device 100 with other peripheral devices.”). The Specification teaches that such peripheral devices include “any suitable digital, analog, and/or mixed-signal peripheral circuits used for facilitating the operation of 3D memory device 100, such as page buffers, decoders, and latches.” *Id.* at 9:34–42. The Specification explains that dummy source structures “can be uniformly distributed in the staircase structure,” and the arrangement of the dummy source structures “may improve the uniformity and stability for etching dummy channel holes in the staircase region” and “may allow the gate electrode/word lines to be formed with improved uniformity and quality, reducing the resistivity of the gate

electrodes/word lines.” *Id.* at 5:43–52; *see also id.* at 8:49–53 (“The symmetrical architecture of dummy channel structures and dummy source structures can improve the performance and efficiency of etching processes. Different layouts, patterns, and designs may be adopted based on the size of the staircase region.”).

In addition, the Specification describes the functions of the dummy source structure:

When conductive materials are used to fill dummy source hole 212 (e.g., contact 244), the dummy source structure 246 may function as an interconnect to connect 3D memory device 100 with other peripheral devices. When dielectric materials are used to fill dummy source hole 212, dummy source structure 246 may function as a mechanical support structure to improve the stability of the staircase region.

Ex. 1001, 16:63–17:3. Notably, the Specification does not describe the dummy source structure as functioning as a source for the memory cells.

Instead, the Specification distinguishes between dummy source structures and source structures. In particular, the Specification teaches that “[s]ource structures formed in the inner region may be connected with surround channel structures . . . via a common source, such as a doped region” in the substrate. Ex. 1001, 16:34–38. Dummy source structures, however, “may not connect to channel structures in the channel region,” and instead “may be formed simultaneously with source structures in the inner region, while functioning as a mechanical supporting structure after gate-replacement process, without connecting to channel structures in the inner region.” *Id.* at 16:38–44.

On this record, we do not adopt Petitioner’s position that “dummy source structure” requires that the structure occupy the void used for the gate replacement process. In particular, we are not persuaded that the gate

replacement process is an essential part of the claimed invention, such that it should be treated as a part of the claimed 3D memory device. *See Andersen Corp. v. Fiber Composites, LLC*, 474 F.3d 1361, 1365 (Fed. Cir. 2007); *see also Vanguard Prods. Corp. v. Parker Hannifin Corp.*, 234 F.3d 1370, 1372–73 (Fed. Cir. 2000) (“A novel product that meets the criteria of patentability is not limited to the process by which it was made.”).

2. “surrounding”

Claim 1 recites, in relevant part, “the plurality of dummy source structures surrounding the staircase contact.” Ex. 1001, 20:12–14. Petitioner argues that the term “surrounding” “does not require that the dummy source structures form a border that fully encloses the staircase contact.” Pet. 27–28. Petitioner argues that “[t]he specification discloses that ‘the number of dummy source structures surrounding one or more dummy channel structure 124 may be more or less than eight, six, or four,’” and therefore “there may be less than four dummy source structures that ‘surround’ a work line contact.” *Id.* at 28 (citing Ex. 1001, 8:8–11). Petitioner also argues that dependent claim 15 (which depends from claim 14) recites “wherein at least one dummy channel structure is surrounded by at least four dummy source structures,” which, under the doctrine of claim differentiation, “implies that ‘surrounded’ in independent claim 14 covers implementations in which fewer than four dummy source structures surround a single dummy channel structure.” *Id.* (citing Ex. 1001, claim 15 (21:9–11)).

Patent Owner responds that “the Board need not resolve the full scope of ‘surrounding’ and need not determine whether it requires ‘fully encircling’” because “Petitioner has alleged that the claimed ‘plurality of dummy source structures surrounding the staircase contact’ of Claim 1 is

satisfied ‘by structures on two sides’ of the object.” Prelim. Resp. 21–22 (citing Pet. 61). Patent Owner contends that “[t]he term ‘surrounding’ does not encompass features that are merely on two sides” because “the claims expressly distinguish the concepts of ‘surrounding’ and ‘between.’” *Id.* at 22. Patent Owner contends that “[t]he term ‘between’ is used when reciting the concept of being located in the middle of two structures and ‘surrounding is used when reciting the concept of being located in the middle of more than two structures.” *Id.* In that regard, Patent Owner notes that claim 15 recites “wherein at least one dummy channel structure is surrounded by at least four dummy source structures,” while claim 11 recites “wherein at least one dummy source structure is located between the first and second staircase structure.” *Id.* (citing Ex. 1001, 20:49–52, 21:15–17). Patent Owner also points to the Specification’s explanation that “multiple dummy source structures, such four dummy source structures indicated by a diamond shape 146, may surround a staircase contact, such as staircase contact 122” and its description of another embodiment wherein “at least one dummy source structure may be located between two staircase contacts.” *Id.* at 23–24 (citing Ex. 1001, 6:32–7:25) (emphases omitted).

Having reviewed the claim language, the Specification, and the record currently before us, and for purposes of this Decision, we agree with Patent Owner that “surrounding” requires more than structures on two sides of the object. The Specification repeatedly uses “between” to describe objects in the middle of two structures. *See, e.g.*, Ex. 1001, 3:65–67 (“a layer can be located between any pair of horizontal planes between, or at, a top surface and a bottom surface of the continuous structure”), 4:56–57 (“dummy channel holes are formed between adjacent GLSs”), 7:12–15 (“one or more dummy channel structures may be located between two dummy source

structures, and vice versa”), 7:16–17 (“at least one dummy source structure may be located between two staircase contacts”), 9:63–64 (“an insulation layer (not shown) is formed between substrate 102 and memory stack 160), 17:42–44 (“at least one dummy source structure is located between the first and second staircase contacts”). In contrast, the Specification uses “surrounding” to indicate an object in the middle of more than two structures. *See, e.g., id.* at 6:38–41 (“multiple dummy source structures, such as the four dummy source structures indicated by a diamond shape 146, may surround a staircase contact, such as staircase contact 122”), 6:60–63 (“A plurality of dummy channel structures, such as the four dummy channel structures indicated by square shape 148, may surround a staircase contact.”), 7:31–34 (“four dummy channel structures indicated by dashed-line square shape 142 are surrounded by eight dummy source structures indicated by an octagon 144”), 7:38–40 (“one dummy channel structure indicated by dashed-line square 147 is surrounded by four dummy source structures indicated by a diamond 149”), 17:61–62 (“at least one dummy channel structure is surrounded by at least four dummy source structures”), 17:63–64 (“at least two dummy channel structures are surrounded by at least six dummy source structures”), 17:65–67 (“at least four dummy channel structures are surrounded by at least eight dummy source structures”).

That claim 15 recites “wherein at least one dummy channel structure is surrounded by at least four dummy source structures” and claim 14, from which claim 15 depends, recites “wherein a subset of the dummy channel structures is surrounded by the plurality of dummy source structures,” does not require a different result. While we agree with Petitioner that the doctrine of claim differentiation may “impl[y] that ‘surrounded’ in independent claim 14 covers implementations in which fewer than four

dummy source structures surround a single dummy channel structure,” that does not require that “surround” encompasses a dummy channel structure between two dummy source structures. Pet. 28 (citing Ex. 1001, claim 15 (21:9–11)). For example, three dummy source structures surrounding one dummy source structure could satisfy claim 14 but not claim 15 (“at least four dummy source structures”).

Accordingly, we determine that “surrounding” in claim 1 of the ’872 patent does not encompass structures on only two sides of an object. We need not provide an explicit construction of “surrounding,” as terms in controversy need to be construed only to the extent necessary to resolve the controversy. *Realtime Data*, 912 F.3d at 1375.

3. Other Terms

We determine that no other term requires express construction to determine whether to institute *inter partes* review. *Realtime Data*, 912 F.3d at 1375 (“The Board is required to construe ‘only those terms . . . that are in controversy, and only to the extent necessary to resolve the controversy.’” (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999))). To the extent further discussion of the meaning of any claim term is necessary to our decision, we provide that discussion below in our analysis of the asserted grounds of unpatentability.

C. Obviousness over Tessariol

Petitioner contends that claims 1–6 and 11–13 would have been obvious over Tessariol. Pet. 74–101.

1. Overview of Tessariol

Tessariol is directed “to devices, to methods used in forming a circuit structure, and to methods used in forming an array of elevationally-extending transistors and a circuit structure adjacent thereto.” Ex. 1006 ¶ 1.

Tessariol teaches construction 10 comprises base substrate 11 and various materials formed elevationally over base substrate 11. *Id.* ¶ 27. Figure 9 is reproduced below.

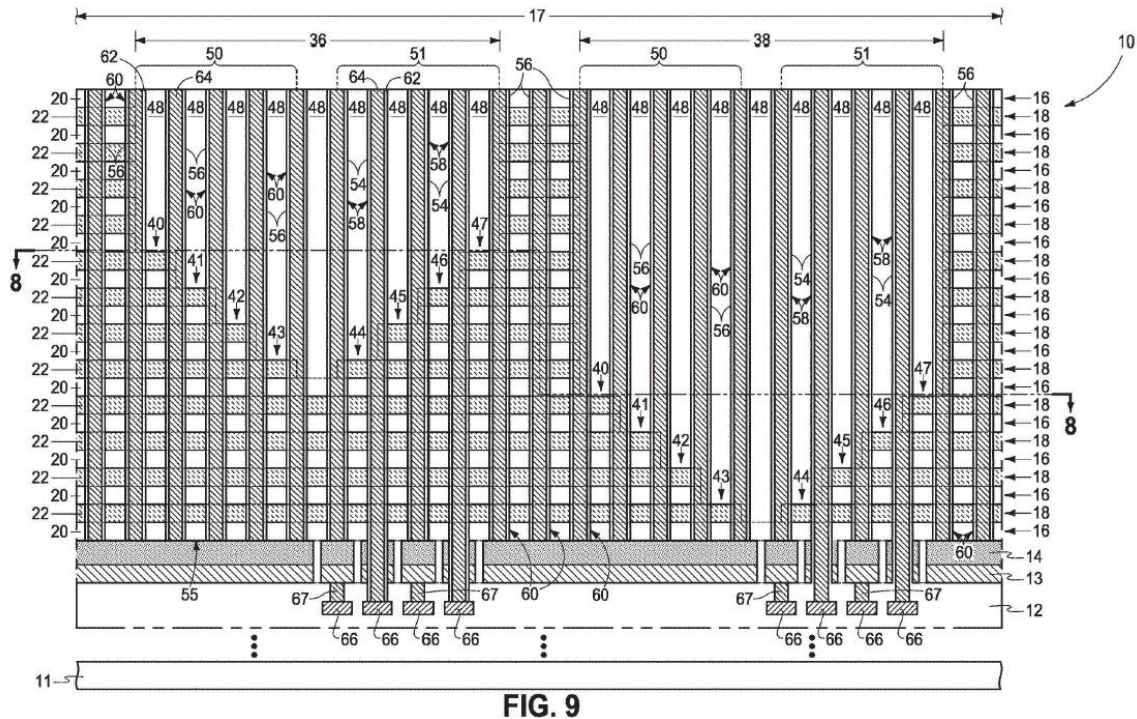


FIG. 9

Figure 9 is a diagrammatic cross-sectional view of a portion of a substrate construction in process as described in Tessariol. *Id.* ¶ 16. Dummy-structure openings 56 and via openings 54 are formed through insulating material 48 and vertically-alternating tiers 16 and 18. *Id.* ¶ 37. Operative conductive vias 58 are formed within via openings 54, and dummy structures 60 are formed within dummy-structure openings 56. *Id.* ¶ 38. Operative conductive vias 58 and dummy structures 60 comprise insulative lining 62 and conductive core 64. *Id.* Some alternate ones of operative conductive vias 58 are directly electrically coupled to individual conductive lines 66 through source material 14, conductive material 13, and conductive vias 67, and other alternate ones of operative conductive vias 58 are directly

electrically coupled to individual conductive lines 66 through materials 14 and 13 to be directly against individual conductive lines 66. *Id.* ¶ 39.

Figure 15 is reproduced below.

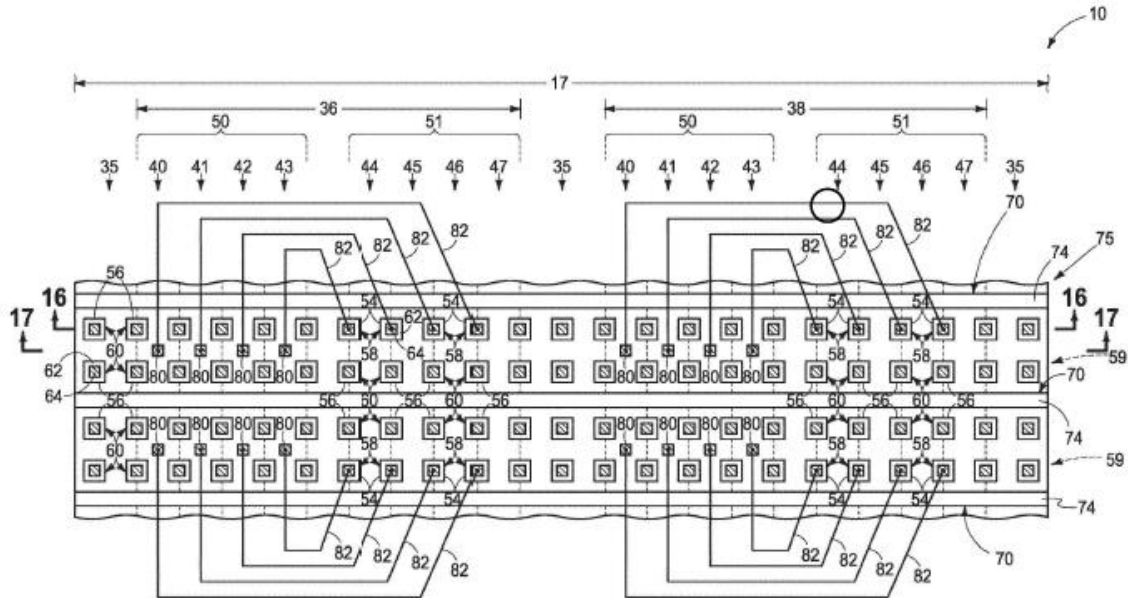


FIG. 15

Figure 15 is a diagrammatic cross-sectional view of a portion of a substrate construction at a later processing step. Ex. 1006 ¶ 22. Operating conducting vias 80 individually extend to and directly electrically couple with conductive material 72. *Id.* ¶ 46. Interconnect lines 82 individually directly electrically couple together different individual operating conducting vias 80 to different individual operating conductive vias 58 through conductive extensions 69 *Id.* Strings 87 of transistors 85 connect with individual conductive lines 84 through conductive extensions 81. *Id.* Insulator material 86 surrounds conductive components 69, interconnect lines 82, conductive extensions 81, and conductive lines 84. *Id.*

Tessariol teaches that “[t]he circuit structures comprises a stair step structure (e.g., any of 34, 36, and 38) comprising vertically alternating tiers (e.g., 16, 18) comprising conductive steps . . . that are at least partially

elevationally separated from one another by an insulative material (e.g., 20).” Ex. 1006 ¶ 48. Tessariol also teaches that “[d]ummy structures (e.g., 60) individually extend elevationally through one of the conductive steps at least to the bottom of the vertically-alternating tiers.” *Id.* ¶ 48. Tessariol defined “dummy structure” as “a structure which is used to mimic a physical property of another structure (e.g., presence, or physical load-carrying/supporting ability of an operative structure) and which may comprise a circuit inoperable dead end (e.g., is not part of a current flow path of a circuit even if conductive.)” *Id.* ¶ 68.

2. Claim 1

Petitioner contends that Tessariol teaches all of the elements of independent claim 1. Pet. 74–91. For example, Petitioner contends Tessariol teaches “a substrate” (base substrate 11), “a memory stack comprising interleave conductive layers and dielectric layers on the substrate” (stacks 24 and 30, which comprise alternating layers 20 and 72 on substrate 11), “a staircase structure on one side of the memory stack” (staircase in adjacent region 17 next to array region 15), and “a staircase contact in the staircase structure” (operating conductive via 80). *Id.* at 75–83 (citing Ex. 1006 ¶¶ 27–29, 31, 34, 41, 46, Figs. 1, 2, 5, 6, 17; Ex. 1003 ¶¶ 183–201).

With respect to limitation [1.E] (“a plurality of dummy source structures each extending vertically through the staircase structure, the plurality of dummy source structures surrounding the staircase contact”), Petitioner contends that Tessariol’s dummy structures 60 and conductive vias 58 are the claimed “plurality of dummy source structures” because they comprise insulative lining 62 and conductive core 64, and “are formed in dummy structure openings 56 and elevationally extending via openings 54

that are formed through a memory stack comprised of insulating and conductive materials.” Pet. 84 (citing Ex. 1006 ¶¶ 37–38). Petitioner provides an annotated partial version of Tessariol’s Figure 15, reproduced below, to illustrate its contentions with respect to the “the plurality of dummy source structures surrounding the staircase contact” element of limitation [1.E].

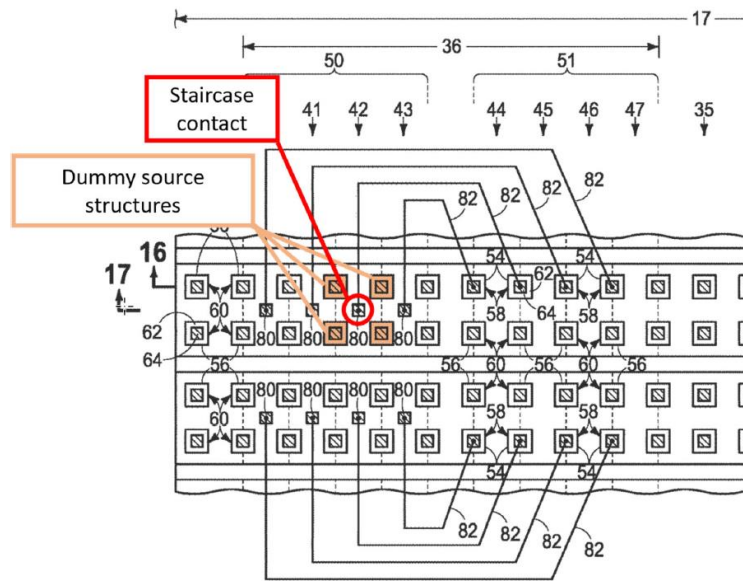


FIG. 15

Annotated partial Figure 15 is a diagrammatic cross-sectional view of a portion of a substrate construction in process as described in Tessariol, with Petitioner’s addition of a red circle labeled “Staircase contact” and peach shading labeled “Dummy source structures.” Pet. 88; Ex. 1006 ¶ 22. Petitioner contends that four dummy source structures (dummy structures 60, shaded peach) surround each staircase contact 80 (circled in red). Pet. 85–88; Ex. 1003 ¶¶ 202–210.

As to limitation [1.F] (“wherein each of the dummy source structures comprises a conductive contact”), Petitioner contends that “Tessariol discloses dummy structures 60 and operative conductive vias 58 that

comprise ‘an insulative lining 62 (e.g., silicon dioxide and/or silicon nitride) and a conductive core 64 (e.g., metal material),’” which “is like an embodiment of the ’872 Patent in which the dummy structures have a conductive core and insulating liner.” Pet. 89 (citing Ex. 1006 ¶ 38; Ex. 1001, 11:34–49) (footnote omitted).

Patent Owner responds that although Petitioner maps Tessariol’s dummy structures 60 and conductive vias 58 to the claimed “dummy source structures,” Tessariol’s Figure 15 shows that Petitioner only alleges that dummy source structures 60 surround operating conducting via 80 (the “staircase contact”). Prelim. Resp. 40–41. Patent Owner argues that dummy structure 60 does not comprise a conductive contact. *Id.* at 41. In particular, Patent Owner argues that Tessariol “explains that while a ‘dummy structure’ may be conductive, they are ‘not part of a current flow path of a circuit’ because they only ‘mimic a physical property’ (not the functional property) of ‘an operative structure.’” *Id.* (citing Ex. 1006 ¶ 68). According to Patent Owner, “dummy structures would not have a ‘conductive contact’ as that is a functional property, not just a physical property, of the operative structure.” *Id.* (citing Ex. 2001 ¶¶ 39–46).

Petitioner replies that “[t]he ’872 Patent describes the ‘conductive contact’ in structural (not functional) terms: conductive material that fills the dummy source hole.” Prelim. Reply 6 (citing Pet. 62–63; Ex. 1001, 2:2–8, 11:37–39, 16:13–25, 16:50–52, 16:63–64, 18:38–41); *see also id.* at 7 (“[D]uring prosecution, Applicant distinguished the prior art’s ‘pillar’ from the ‘conductive contact’ on purely structural grounds, with no mention of it contacting the substrate or current flowing through it.”) (citing Ex. 1002, 514–515). Petitioner contends that if “conductive contact” is “the place where the dummy source contacts the substrate” or “where the current

must flow,” embodiments in the ’872 patent “in which the ‘dummy source structure’ serves as a ‘dummy’ and in which it does not contact the substrate” would be excluded from the scope of the claim. *Id.* at 6–7 (citing Ex. 1001, 18:22–23). Patent Owner responds that “the term ‘conductive contact’ requires not only conductivity but also being a contact—based on the term’s plain meaning,” and “the Petition relies on a ‘conductive core,’ while disregarding the ‘contact requirement.’” Prelim. Sur-reply 4–5 (citing Prelim. Resp. 39–42; Pet. 89–90). According to Patent Owner, “a ‘conductive contact’ serves as a contact between a dummy source structure and another structure (e.g., peripheral devices, etc.) and must be conductive.” *Id.* at 5 (citing Prelim. Resp. 41–42; Ex. 2001 ¶¶ 39–46).

As an initial matter, we are persuaded, on this record, that Petitioner sufficiently establishes that Tessariol’s dummy structures 60 are “dummy source structures,” i.e., structures that do not function as a source for the memory cells. Tessariol teaches that

a “dummy structure” refers to a structure which is used to mimic a physical property of another structure (e.g., presence, or physical load-carrying/supporting ability of an operative structure) and which may comprise a circuit inoperable electrical dead end (e.g., is not part of a current flow path of a circuit even if conductive).

Ex. 1006 ¶ 68. Accordingly, Tessariol teaches that dummy structures 60 are structures that do not function as a source to the memory cells.

We note that although Petitioner also identifies conductive vias 58 as the claimed “dummy source structures,” Petitioner relies only on dummy structures 60 with respect to limitations that set forth other properties of the “dummy source structures” (such as limitation [1.F]). *See* Pet. 89–99.

While we question the sufficiency of Petitioner’s contentions with respect to

whether conductive via 58 is a structure that does not function as a source to the memory cells, Petitioner's showing with regard to dummy structures 60 is sufficient to meet Petitioner's burden at this stage of the proceeding.

We are also persuaded, on this record, that Petitioner sufficiently establishes that Tessariol's dummy structures 60 "comprise[] a conductive contact" as required by limitation [1.F]. The '872 patent teaches that "[e]ach dummy source structure may include an insulating spacer layer in a dummy source hole and a conductive contact within the spacer layer," and, "[i]n some *embodiments*, one or more dummy source structures are in contact with the substrate and may provide interconnect between the 3D memory device and peripheral devices." Ex. 1001, 5:37–43 (emphasis added). Thus, it follows that, in some embodiments, a dummy source structure comprising a conductive contact *does not contact* the substrate or provide interconnect with peripheral devices. *See also id.* at 18:22–23 ("In some embodiments, the plurality of dummy source structures are not in contact with the substrate.").

The '872 patent also teaches that, "[w]hen conductive materials are used to fill dummy source hole 212 (e.g., contact 244), the dummy source structure 246 *may function* as an interconnect to connect 3D memory device 100 with other peripheral devices." *Id.* at 16:63–66. Here, the permissive use of "may function" indicates that dummy source structure 246 might not function as an interconnect, even when it comprises a contact made of conductive materials. If "conductive contact" were defined to require contact between a dummy source structure and another structure (e.g., peripheral devices, etc.), as Patent Owner argues, there would be no need to state that the dummy source structure *may function* as an interconnect. Moreover, the '872 patent does not clearly express an intent to require

dummy structures comprising conductive contacts to physically contact another structure or to act as an interconnect to peripheral devices.

Tessariol’s teaching that dummy structure 60 is “formed to comprise an insulating layer 62 (e.g., silicon dioxide and/or silicon nitride) and a conductive core 64 (e.g., metal material),” and “may comprise a circuit inoperable electrical dead end (e.g., is not part of a current flow path of a circuit, even if conductive)” is consistent with the ’872 patent’s description of a “conductive contact.” Ex. 1006 ¶¶ 38, 68. Accordingly, we are persuaded that Petitioner adequately establishes that Tessariol teaches the “each of the dummy source structures comprises a conductive contact” limitation of claim 1.

Having reviewed the parties’ arguments and the evidence of record, we are persuaded that Petitioner sufficiently establishes, for purposes of institution, that the teachings of Tessariol account for all the recitations of independent claim 1. Pet. 74–91.

3. *Claims 2–6 and 11–13*

Claims 2–6, and 11–13 depend, directly or indirectly, from claim 1. Ex. 1001, 20:17–33, 20:49–61. At this stage of the proceeding, Patent Owner does not address Petitioner’s specific contentions with respect to these claims.

We reviewed the arguments and evidence of record thus far and find that, for purposes of institution, Petitioner adequately shows how Tessariol teaches each limitation of claims 2–6 and 11–13. Pet. 92–101.

4. *Conclusion*

For these reasons, we determine that Petitioner establishes a reasonable likelihood of prevailing in showing that claims 1–6 and 11–13 would have been obvious over Tessariol.

D. Asserted Obviousness over Park

Petitioner contends that claims 1–6, 11, and 13 would have been obvious over Park. Pet. 40–74. Patent Owner argues that Park does not disclose “a plurality of dummy source structures” or “the plurality of dummy source structures surrounding the staircase contact.” Prelim. Resp. 32–38. Having already determined that Petitioner establishes a reasonable likelihood of establishing that claims 1–6, 11, and 13 would have been obvious over Tessariol, we need not address this ground in full. We offer the following comments in response to the parties’ arguments and evidence to provide guidance to the parties.

1. Overview of Park

Park relates “to semiconductor devices including vertical channels and methods of manufacturing the same.” Ex. 1005, 1:22–25. Park teaches that the “semiconductor device includes a substrate, first channel structures, gate lines, cutting lines, dummy patterns and dummy lines” and provides “improved structural and electrical reliability.” *Id.* at 1:36–41.

Figure 2 is reproduced below.

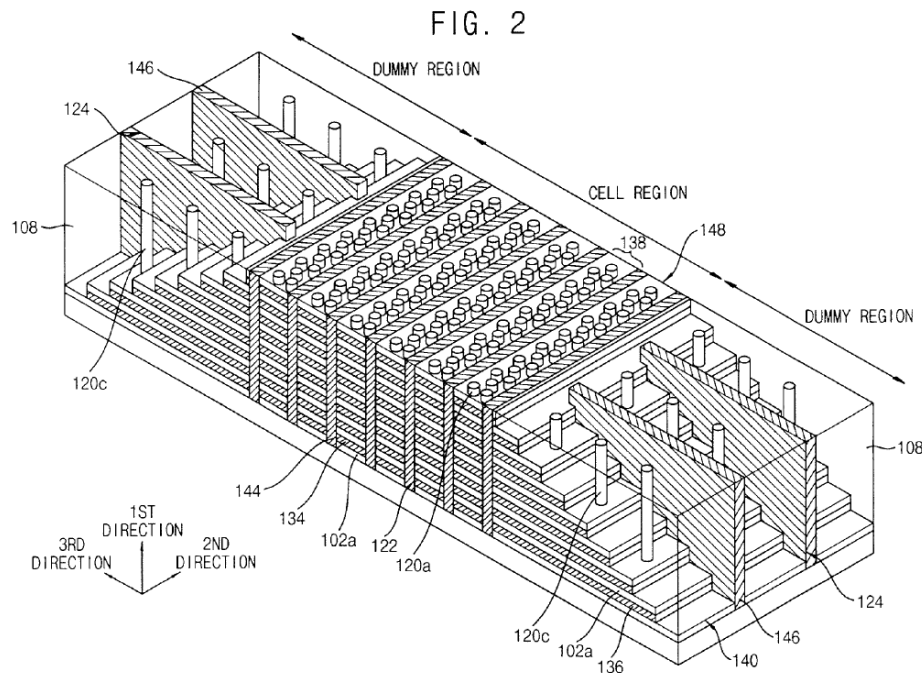


Figure 2 illustrates a perspective view of a semiconductor device described in Park. Ex. 1005, 3:35–37. The semiconductor device includes a memory cell structure disposed on a cell region of substrate 100 and a dummy structure disposed on a dummy region of substrate 100. *Id.* at 6:1–4. The memory cell structure includes first and second channel structures 120a and 120b, gates lines 134, and common source line (CSL) 144. *Id.* at 6:9–11. Gate lines 134 are formed on outer sidewalls of first and second channel structures 120a and 120b, extend in the second direction,⁴ and are spaced apart from each other along the first direction. *Id.* at 6:11–15. Park teaches that the lowermost gate line of gate lines 134 may serve as a ground

⁴ Park explains that “[a] direction substantially vertical to the top surface of the substrate is referred to as a first direction, and two directions substantially parallel to the top surface of the substrate and substantially crossing each other are referred to as a second direction and a third direction.” Ex. 1005, 5:57–61.

selection line (GSL), the uppermost gate line of the gate lines 134 may serve as a string selection line (SSL), and gate lines 134 in between may serve as word lines. *Id.* at 7:11–15.

Insulating interlayer pattern 102a is interposed at each level between gate lines 134, and insulating interlayer pattern 102a and gate lines 134 may be alternately stacked along the first direction to define first structure 138, which may extend in the second direction. Ex. 1005, 7:19–26. “Both lateral portions of the first structure 138 in the second direction may serve as a wiring region and have a stepped shape,” such that “different wirings may be connected to different gate lines 134 included in the first structure 138 so that an electrical signal may be individually applied to each gate line 134.” *Id.* at 7:26–31. First opening 122 may be formed between first structures 138 neighboring each other, and may extend through the alternating stack of insulating interlayer patterns 102a and gate lines 134 to the top of substrate 100. *Id.* at 7:52–56.

The dummy structure includes second structure 140 and dummy source line 146. *Id.* at 8:1–2. A plurality of second structures 140 may be arranged and spaced apart from each other along the second direction, with a plurality of dummy source lines 146 extending between the neighboring second structures 140. *Id.* at 8:3–6. Second structure 140 may include alternately stacked insulating interlayer patterns 102a and dummy patterns 136. *Id.* at 8:7–9. Park teaches that insulating interlayer pattern 102a in second structure 140 may be the same as insulating interlayer pattern 102a in first structure 138, and that dummy patterns 136 may be formed at levels corresponding to gate lines 134 in first structure 138. *Id.* at 8:13–18. Second opening 124 may be formed between neighboring second structures 140, and may extend to the top surface of substrate 100.

Id. at 8:27–31. Dummy source line 146 may be disposed in second opening 124, and may be contact with the top of substrate 100. *Id.* at 8:49–51.

2. *Claim 1*

As to limitation [1.E] (“a plurality of dummy source structures each extending vertically through the staircase structure, the plurality of dummy source structures surrounding the staircase contact”), Petitioner contends that Park’s common source lines 144 and dummy source lines 146 are the claimed “plurality of dummy source structures” because “[d]uring the gate replacement process, first openings 122 and second openings 124 are etched in the insulating/sacrificial layer stack,” and “are the voids that are used for the gate replacement process.” Pet. 50–52 (citing Ex. 1005, 11:66–12:4, Fig. 9). Petitioner further contends that after the gate replacement process, first opening 122 and second opening 124 “are each lined with an insulating layer and then filled with conductive material to form a common source line 144 and a dummy source line 146, respectively.” *Id.* at 53 (citing Ex. 1005, 13:39–41). Petitioner contends that “[t]he ’872 Patent describes almost identical dummy source structures” to “Park’s common source lines 144 and dummy source lines 146” because “the ’872 Patent states that ‘dummy source structures 178 can laterally separate 3D memory device 100 into multiple memory regions, such as memory blocks,’ and “Park’s common source lines 144 and dummy source lines 146 do the same.” *Id.* at 54 (citing Ex. 1001, 11:44–46; Ex. 1005, 12:5–18). Petitioner also contends that Park’s common source lines 144 “are an interconnect for a source connection,” like the ’872 Patent’s dummy source structures that “may provide interconnect between the 3D memory device and peripheral

devices.” *Id.* at 55–56 (citing Ex. 1001, 5:41–43, 16:63–66; Ex. 1005, 7:63–64; Ex. 1003 ¶ 146).

Patent Owner responds that “Park’s common source lines 144 are not dummy source structures because they function as a source to the memory cells and are, therefore, actual—not dummy—source structures.” Prelim. Resp. 36–37. Patent Owner argues that “Park expressly distinguishes between the ‘common source line’ for the memory cell structure, which functions as the source line, and a ‘dummy source line.’” *Id.* at 37 (citing Ex. 1005, 6:1–11, 7:59–60, 13:39–41). Patent Owner also argues that Park’s Figure 1 shows “separate regions where the common source line and dummy source lines are located—the common source line is in the ‘cell region’ and the dummy source line is in the ‘dummy region.’” *Id.* at 37–38 (citing Ex. 1005, Fig. 1). Patent Owner further argues that “the ’872 patent’s disclosure that ‘dummy source structures’ may ‘serve as an interconnect between the 3D memory devices and peripheral devices’ does not suggest that Park’s common source line is also a dummy structure” because “the interconnect referenced in the ’872 patent is not a source line.” *Id.* at 38 (citing Ex. 1001, 5:40–43).

As set forth above, we construed “dummy source structure” as “a structure that does not function as a source to the memory cell.” Section II.C.1, *supra*. Thus, Petitioner must show that Park’s common source lines 144 and dummy source lines 146 do not function as sources to the memory cell. *Harmonic Inc. v. Avid Tech. Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016) (stating that it is Petitioner’s burden to show with particularity why a challenged claim is unpatentable); *see also* 37 C.F.R. § 42.104(b)(4) (A petition “must specify where each element of the claim is found in the prior art patents or printed publications relied upon.”). Based

on the current record, we find that Patent Owner’s arguments regarding common source lines 144 have merit. Petitioner’s reasoning with respect to common source lines 144 is based on Petitioner’s proposed claim construction, which we do not adopt for purposes of this Decision. See Pet. 50–56. Park distinguishes common source lines 144 that are included on the memory cell structure with first and second channel structures 120a and 120b, and gate lines 134 from dummy source lines 146 that are included on the dummy region with second structure 140 and third channel structure 120c that “may not serve as a channel of the memory cell, and may merely serve as a supporting pillar of the second structure 140.” Ex. 1005, 6:9–11, 8:1–2, 8:57–60. That common source lines 144 are disposed on the cell region of the substrate while dummy source lines 146 are disposed on the dummy region alone at least indicates that the common source lines 144 and dummy source lines 146 may not operate in the same way or serve the same purpose. We question, therefore, whether common source lines 144 are “structures that do not function as sources for the memory cell.”

With respect to the “a plurality of dummy source structures surrounding the staircase contact” limitation of claim 1, Petitioner contends that two common source lines 144 surround a staircase contact. Pet. 57–62. Because we determined that, for purposes of this Decision, “surrounding” does not encompass structures on only two sides of an object, Petitioner does not show that Park teaches this limitation. Section II.C.2, *supra*.

We invite the parties to develop these arguments further at trial, to the extent permitted under our rules.

III. CONCLUSION

Based on the arguments in the Petition, the Preliminary Response, the Preliminary Reply, and the Preliminary Sur-reply, we determine that

Petitioner establishes a reasonable likelihood that it will prevail on its challenge to at least one claim of the '872 patent. Accordingly, we institute an *inter partes* review of all the challenged claims on all the challenged grounds.

The factual findings set forth in this Decision are preliminary and provided for the sole purpose of deciding whether to institute a review. Any final findings will be based on the full trial record, including any information presented in a timely filed response to the Petition. *See Trivascular, Inc. v. Samuels*, 812 F.3d 1056, 1068 (Fed. Cir. 2016) (noting that “there is a significant difference between a petitioner’s burden to establish a ‘reasonable likelihood of success’ at institution, and actually proving invalidity by a preponderance of the evidence at trial”) (quoting 35 U.S.C. § 314(a); comparing *id.*, with § 316(e)).

IV. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that an *inter partes* review is instituted with respect to all of the grounds asserted in the Petition; and

FURTHER ORDERED that, pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is hereby given of the institution of a trial, which shall commence on the entry date of this Decision.

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Patent 10,861,872 B2

For PETITIONER:

Jeremy Jason Lang
Jared Bobrow
K. Patrick Herman
ORRICK, HERRINGTON & SUTCLIFFE LLP
jlang@orrick.com
jbobrow@orrick.com
pherman@orrick.com

For PATENT OWNER:

James L. Davis, Jr.
Christopher M. Bonny
Allen S. Cross
ROPES & GRAY LLP
James.L.Davis@ropesgray.com
Christopher.Bonny@ropesgray.com
Allen.Cross@ropesgray.com