

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,

Petitioner,

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,

Patent Owner.

Case IPR2024-00789
Patent 10,861,872

**PATENT OWNER'S RESPONSE
UNDER 37 C.F.R. § 42.120**

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LIST OF EXHIBITS

Exhibit	Description
Ex. 2001	July 29, 2024, Declaration of Dr. Kuhn (“KuhnI”)
Ex. 2002	CV of Dr. Kuhn
Ex. 2003	Shur, “Introduction to Electronic Devices” (1996) (“Shur”)
Ex. 2004	Streetman, “Solid State Electronic Devices” (1995) (“Streetman”)
Ex. 2005	US Patent No. 8,766,336 (“Grupp”)
Ex. 2006	Declaration of Jonathan Bradford
Ex. 2007	January 17, 2025, Declaration of Dr. Kuhn (“KuhnII”)
Ex. 2008	Deposition Transcript of Dr. Banerjee
Ex. 2009	<i>Contact</i> , New Oxford American Dictionary, Third Edition, 2010
Ex. 2010	<i>Contact</i> , Wiley Electrical and Electronics Engineering Dictionary, 2004
Ex. 2011	<i>Electric Contact</i> , McGraw-Hill Dictionary of Scientific and Technical Terms, Sixth Edition, 2002
Ex. 2012	Micron’s Preliminary Claim Constructions
Ex. 2013	Plaintiff’s Proposed Claim Constructions

LIST OF ABBREVIATIONS

Abbreviation	Term
'872 or '872 patent	U.S. Pat. No. 10,861,872
'872FH	File History of U.S. Pat. No. 10,861,872
Challenged Claims	'872, Claims 1-6 and 11-13
Office	U.S. Patent and Trademark Office
Park	U.S. Pat. No. 9,859,297
Petition or Pet.	Petition for <i>Inter Partes</i> Review of U.S. Patent No. 10,861,872 (IPR2024-00789, Paper 1)
Parallel district court litigation	<i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc.</i> , NDCA-3-23-cv-05792 (N.D. Cal.)
Patent Owner or PO	Yangtze Memory Technologies Co. Ltd.
Petitioner	Micron Technology, Inc.
POSITA	Person of ordinary skill in the art
Tessariol	U.S. Patent Pub No. 2019/0081061

I. INTRODUCTION

The references in Petitioner's Grounds fail to disclose or render obvious the Challenged Claims of U.S. Patent No. 10,861,872 ("872," Ex. 1001). For example, the art fails to disclose or render obvious multiple claim elements under the proper construction of those terms, and Petitioner repeatedly fails to consistently map features from the art to all of the claim requirements applicable to the claimed "plurality of dummy source structures."

For Ground 1, Park fails to disclose or renders obvious the Challenged Claims at least because Park fails to disclose or render obvious multiple requirements of the sole challenged independent claim, including "dummy source structures" and dummy source structures "surrounding" the staircase contact. Park's alleged "dummy source structures" are not "surrounding the staircase contact" because Park's alleged staircase contact is merely "between" two alleged dummy source structures. And Park's common source lines are not "dummy source structures" because Park's common source lines function as a source to memory cells.

Similarly, for Ground 2, Tessariol fails to disclose or renders obvious the Challenged Claims at least because Petitioner has not shown that any particular structure satisfies all of the claim requirements applicable to the claimed "plurality of dummy source structures." For example, Petitioner fails to show that Tessariol's "conductive vias 58" do not function as a source to memory cells as required under

the proper construction of “dummy source structures,” and the conductive vias do not “surround” the alleged staircase contact as required by claim 1. Meanwhile, Tessariol’s “dummy structures 60” do not comprise a “conductive contact” because Tessariol does not teach that dummy structure 60 is a conductive structure that permits current flow with an adjoining conductive structure, and Petitioner’s only alleged motivation to modify Tessariol is conclusory and contradicted by the reference.

As set forth herein, the Grounds presented in the Petition fail to make the required showing of obviousness.¹

II. THE ’872 PATENT

The claimed invention of the ’872 is directed to “an improved 3D [three-dimensional] memory structure scheme” that improves device performance by mitigating problems arising from device fabrication processes. Ex. 1001, 4:64-65, 5:22-33. KuhnII, ¶¶40-45. Compared to planar memory structures, 3D memory structures increase storage density by stacking memory cells vertically and are used in a variety of applications such as consumer electronics and storage devices. Ex.

¹ This Patent Owner Response is supported by the declaration of Dr. Kuhn. *See* Ex. 2007 (“KuhnII”). All emphasis and color annotations have been added unless otherwise noted.

1001, 4:64-65, 5:22-33. As the '872 explains, "3D memory architecture[s] can address the density limitation in planar memory cells." '872, 1:5-6; KuhnII, ¶40. The '872 is specifically directed to improving a semiconductor fabrication technique for 3D memory structures. Ex. 1001, 1:15-18, 4:30-33. As 3D memory devices are "scaled to smaller sizes," fabrication becomes more challenging. Ex. 1001, 1:18-22, 4:37-38; KuhnII, ¶41. One such fabrication challenge arises when certain device openings, called gate line slits ("GLS"), are used to deposit conductive material into trenches that extend laterally ("lateral recesses") in the memory array of the device to form gate lines (gate electrodes) for transmitting signals to activate memory cells. Ex. 1001, 4:44-49, 5:17-20; KuhnII, ¶41. The GLS, as depicted in the color-annotated version of the '872's Fig. 5 below, has "a dimension along the extending direction (or the x-direction) much greater than the dimension along the expanding dimension (or the y-direction))." Ex. 1001, 5:22-30. As a result of this shape, formation of the GLS "can contribute to unbalanced variations of wafer flatness (e.g., wafer warpage bias) in different directions," which "can have an adverse impact on the photolithography process to form device patterns, leading to potential die yield loss." *Id.* KuhnII, ¶41.

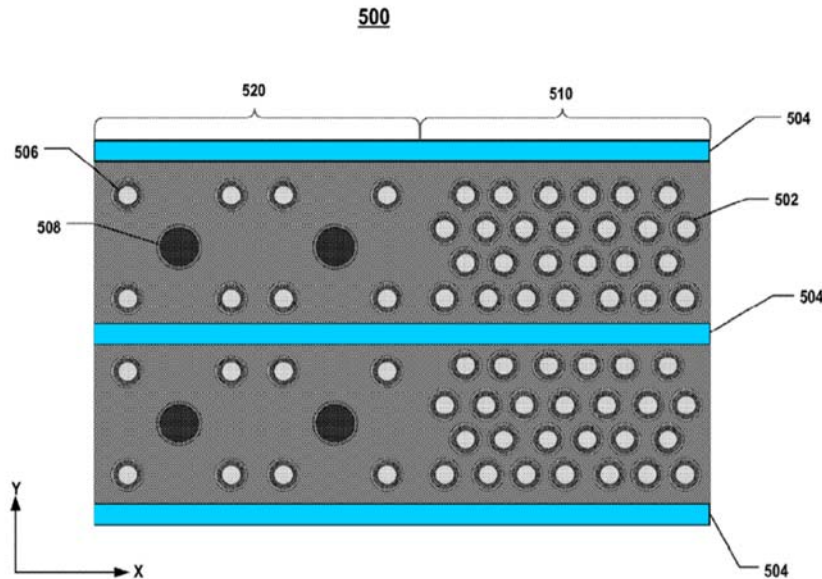


FIG. 5

The '872 solves this issue, for example, by introducing “a plurality of dummy source structures,” each of which “extend[s] vertically” through a staircase structure—a memory stack of multiple stairs where each stair has alternating layers of dielectric and conductor materials—on “one side of the memory stack.” Ex. 1001, 1:39-42, 5:31-36; KuhnII, ¶42. The claimed invention of the '872 also allows for “removing GLSs from the staircase region.” Ex. 1001, 8:22-23; KuhnII, ¶42. The dummy source holes, which later become the dummy source structures, can be used as access points to form gate lines. Ex. 1001, 15:16-48; KuhnII, ¶42. The dummy source structures can be “arranged in a pattern” such that, when used as access points for forming gate lines, the gate lines are formed with “improved uniformity and quality.” Ex. 1001, 4:43-52. This arrangement of the dummy source structures, as

taught by the '872, is advantageous because it allows the deposited conductive material to travel “shorter distances to fill up the lateral recesses,” thus allowing the gate lines to be “less susceptible to voids or density nonuniformity.” Ex. 1001, 4:52-58. KuhnII, ¶42.

An exemplary arrangement of dummy source structures is depicted in the plan view in the color-annotated version of the '872's Fig. 1A, below. The dummy source structures are “arranged in a pattern,” meaning in an arrangement that is “repeated at a regular interval.” Ex. 1001, 7:61-8:1; KuhnII, ¶43. The '872 further teaches that the dummy source structures “surround staircase contacts 122 of nominally same lateral distances to the respective staircase contacts 122” so that, as one example, the depositing “conductive material for forming the gate electrodes may travel nominally same distances to surrounding lateral recesses” to fill the lateral recesses. Ex. 1001, 8:25-34, 8:45-49; KuhnII, ¶43. This “facilitat[es]” the fabrication process such that the gate electrodes are formed “with improved uniformity and quality” and “warping bias” of the memory device is reduced. Ex. 1001, 8:25-34., 8:45-49; KuhnII, ¶43. The '872 emphasizes that the “symmetrical architecture” of dummy source structures is advantageous because it “can improve the performance and efficiency of etching processes,” which are additional processes in fabricating the memory device. Ex. 8:49-51. The '872 further teaches that the dummy source structures are “located adjacent to staircase contact 122,” meaning there are “no

other components such as dummy channel structures, dummy source structures, and staircase contacts” between staircase contact 122 and each of the dummy source structures. Ex. 1001, 6:41-46. KuhnII, ¶43. In the figure below, the red circles 122 are the staircase contacts that are surrounded by orange dummy source structures 126. KuhnII, ¶43.

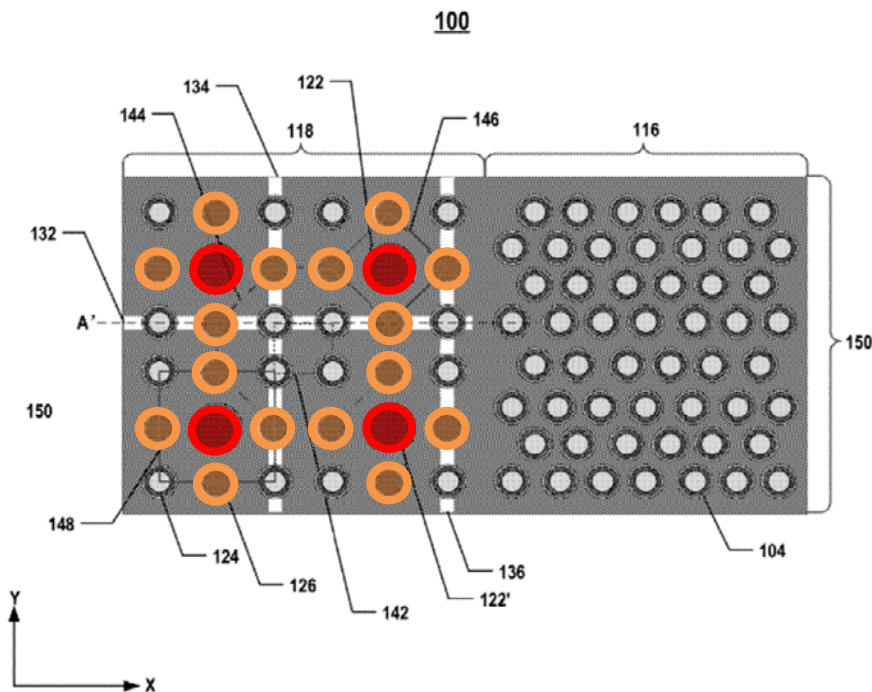


FIG. 1A

Other exemplary images of the dummy source structure arrangement entail arranging the dummy source structures symmetrically around staircase contacts 122, such that each structure is nominally the same lateral distance to the respective staircase contacts 122. Additionally, in each of the embodiments of the '872, each of the dummy source structures is located adjacent to a staircase contact 122, such that there are no other components located between. These arrangements are

depicted in Figs. 1B-1C, below. The '872 does not include any illustrations of the dummy source structure arrangement in plan view other than those depicted in Figs. 1A-1C. KuhnII, ¶44.

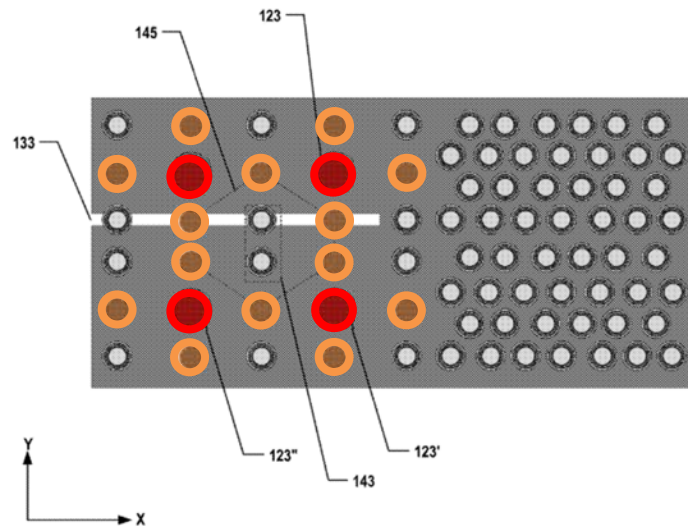


FIG. 1B

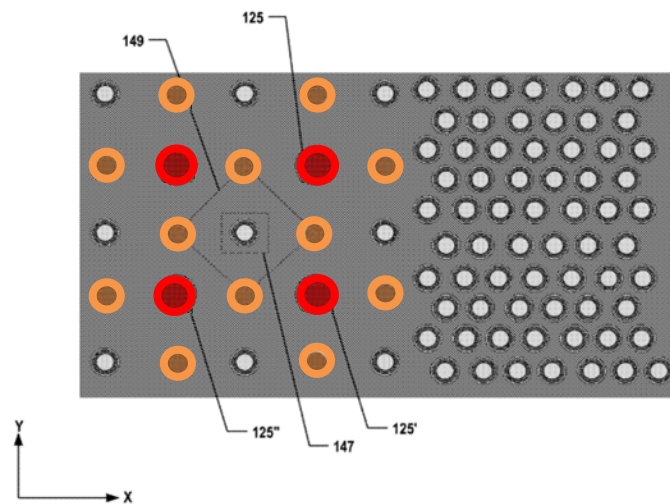


FIG. 1C

The memory device of the '872 includes: (1) substrate with “two lateral

surfaces extending laterally in the x-y plane” (Ex. 1001, 9:3-5); (2) “memory stack 160” that includes “interleaved conductive layers 106 and dielectric layers 108” and “a staircase structure 175” on “[a]t least [] one side in the lateral direction” (Ex. 1001, 9:67-10:3); (3) “dummy source structure 178” that includes “a dummy source hole filled with conductive materials as a contact 179”; and (4) a “spacer 177 made of any suitable dielectric materials (e.g., silicon oxide) between contact 179 and memory stack 160 to electrically separate surrounding conductive layers 106 in memory stack 160 from contact 179” (Ex. 1001, 11:39-43). A cross-section view of the memory device, depicting the dummy source structure, is below. KuhnII, ¶45.

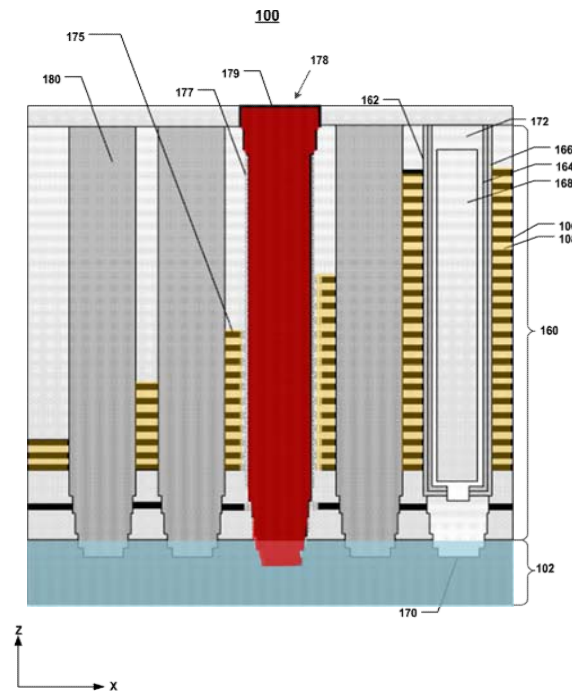


FIG. 1D

The only independent claim of the Challenged Claims, claim 1, is directed to aspects of the above-described invention:

[1.pre] A three-dimensional (3D) memory device, comprising:

[1.a] a substrate;

[1.b] a memory stack comprising interleaved conductive layers and dielectric layers on the substrate;

[1.c] a staircase structure on one side of the memory stack;

[1.d] a staircase contact in the staircase structure; and

[1.e] a plurality of dummy source structures each extending vertically through the staircase structure, the plurality of dummy source structures surrounding the staircase contact,

[1.f] wherein each of the dummy source structures comprises a conductive contact.

III. FILE HISTORY

The claims of the '872 remain patentable over the prior art for at least the same reasons identified during prosecution. KuhnII, ¶¶47-51. As discussed further below in §VI, the prior art does not disclose or render obvious, *inter alia*, the claimed “dummy source structures” that comprise a “conductive contact” of the '872. Claims directed to this limitation were allowed after extensive prosecution and consideration of numerous prior art references.

The '872 was filed on May 2, 2019. During the pendency of the '872 patent application, Applicant was required to restrict the invention to that of a “three-

dimensional (3D) memory device” or “a method for forming” the same. Ex. 1002 (Part 1 of 2), 458 (5/21/2020 Requirement for Restriction/Elections). Applicant elected claims that restricted the invention of the ’872 to that of a “three-dimensional (3D) memory device.” Ex. 1002 (Part 1 of 2), 466 (5/22/2020 Applicant Arguments/Remarks Made in an Amendment). KuhnII, ¶47.

The Examiner then rejected the pending claims under 35 U.S.C. § 102(a)(1) as being allegedly anticipated by and under 35 U.S.C. § 103 as being allegedly obvious over U.S. Pub. No. 2016/0293622 (“Jeong”). Ex. 1002 (Part 1 of 2), 468-78 (6/11/2020 Office Action). In supporting this assertion, the Examiner mapped the ’872’s claimed “plurality of dummy source structures” to Jeong’s “dummy pillars” because “like the dummy source of the instant application, [they] function as a mechanical support for conductive layers” of a memory stack. Ex. 1002 (Part 1 of 2), 470, 474, 476-77 (6/11/2020 Office Action). During a telephonic Applicant-initiated interview, Applicant discussed with the Examiner the distinction between the claimed “dummy source” and the “dummy pillar” of Jeong. Ex. 1002 (Part 1 of 2), 505 (8/14/2020 Applicant-Initiated Interview Summary, Office Action Appendix). KuhnII, ¶48. Based on these discussions, Applicant subsequently filed an amendment to the claims, further limiting the independent claims to recite, “wherein each of the dummy source structures comprises a conductive contact.” Ex. 1002 (Part 2 of 2), 510, 513 (8/18/2020 Request for Reconsideration After Non-Final

Rejection). Applicant stated that the “dummy pillars in Jeong are different from the claimed ‘dummy source structure’ in amended independent claims 1 and 8 at least because the dummy pillars do not include conductive contacts,” explaining:

Nothing in Jeong’s pillar is conductive contact, as the pillar consists of insulating layers, a semiconductor pattern, and a charge storage layer. By contrast, as explained at paragraph [0057] of the present application: ‘In some embodiments, ***dummy source structure 178 includes a dummy source hole filled with conductive materials as a contact 179.*** Dummy source structure 178 can further include a spacer 177 made of any suitable dielectric materials (e.g., silicon oxide) between contact 179 and memory stack 160 to electrically separate surrounding conductive layers 106 in memory stack 160 from contact 179. As a result, dummy source structures 178 can laterally separate 3D memory device 100 into multiple memory regions, such as memory blocks.’

Id., 514-15. The Applicant reiterated that the claimed “dummy source structure” includes “a contact” made of “conductive materials,” and that Jeong’s structure made solely of “insulating layers,” a layer containing a “semiconductor pattern,” and a “charge storage layer” did not meet this criterion. *Id.* In making this argument, the Applicant cited to a section of the specification that additionally states that the claimed “dummy source structure” ***can*** function to “laterally separate” the three-dimensional memory device into “multiple memory regions” ***to the extent that*** the “dummy source structure” includes “a spacer [] made of any suitable dielectric materials,” such as “silicon oxide,” situated “between contact 179 and memory stack

160.” *Id.* Neither the spacer nor the functionality of laterally separating the memory device into regions of memory is recited in any of the independent claims of the ’872. As such, these features were not necessary to overcome the prior art of record. KuhnII, ¶49.

The Examiner subsequently allowed all pending claims and did so after reviewing four additional prior art references identified by the Applicant in a later-submitted Information Disclosure Statement.² Ex. 1002 (Part 2 of 2), 1-6 (10/26/2020 Notice of Allowance), Ex. 1002 (Part 2 of 2) 1-2 (10/30/2020 Information Disclosure Statement), Ex. 1002 (Part 2 of 2), 236-37 (11/9/2020 Notice of Allowance) (“The reasons for allowance have not changed since the previous Office Action (Notice of Allowance, mailed on 10/26/2020).”). The Examiner stated in the Reasons for Allowance that the prior art of record does not teach or render

² Petitioner incorrectly asserts that “Examiner did not consider any prior art references in connection with or following the August 14, 2020 claim amendments.” Pet., 22-23. An Information Disclosure Statement, which identified an additional four foreign patent documents, was submitted by Applicant on October 30, 2020, complied with the provisions of 37 C.F.R. § 1.97, and was considered by the Examiner. Ex. 1002 (Part 2 of 2) 1-2 (10/30/2020 Information Disclosure Statement), Ex. 1002 (Part 2 of 2), 237 (11/9/2020 Notice of Allowance).

obvious the limitation “*wherein each of the dummy source structures comprises a conductive contact.*” Ex. 1002 (Part 2 of 2), 7 (10/26/2020 Notice of Allowance) (emphasis in the original). KuhnII, ¶50. The Examiner further stated, “the individual limitations may be found in a plurality of prior arts but there is no motivation to combine,” and “[b]ecause no reference alone teaches all the limitations, nor is there any motivation to combine the prior arts to construct all the limitations of” independent pending claims 1 and 8, the independent claims are “deemed patentable over the prior arts.” *Id.*, 7-10. The ’872 issued on December 8, 2020 with twenty claims. Ex. 1002 (Part 2 of 2), 272 (Issue Notification). KuhnII, ¶51.

IV. LEVEL OR ORDINARY SKILL IN THE ART

For purposes of this proceeding only, Patent Owner does not object to the definition of a person of ordinary skill in the art (“POSITA”) proffered by Petitioner and adopted by the Board at institution—i.e., a person with “bachelor of science degree in electrical engineering or a similar discipline, along with 2-3 years of professional experience working with (e.g., researching, designing, or teaching) monolithic 3D structures and NAND memory devices, or an equivalent level of skill, knowledge, and experience (e.g., an advanced degree may replace some of the professional experience).” Pet. 33. The Challenged Claims are valid regardless of the precise definition used for a POSITA.

V. CLAIM CONSTRUCTION

Other than the terms identified below, Patent Owner submits that constructions of the claim terms are not necessary to assess whether the prior art reads on the Challenged Claims for the purposes of the *inter partes* review. Patent Owner, however, reserves the right to modify or elaborate on its proposed constructions and to raise further claim construction issues in the parallel district court proceedings.

A. “dummy source structure” (Claims 1-6, 11-13)

The term “dummy source structure” should be construed according to its plain and ordinary meaning as **a structure that does not function as a source to memory cells**. KuhnII, ¶¶58-81. Petitioner proposes construing this term as “structure[s] that occupies the void that was used for the gate replacement process,” but Petitioner’s proposal reads the word “dummy” out of the claims by failing to differentiate between “dummy” source structures and non-dummy source structures and would impermissibly limit the language of an apparatus claim according to the process by which the apparatus is made. KuhnII, ¶58.

1. Patent Owner’s Construction Is Supported by the Intrinsic Evidence

Consistent with the plain and ordinary meaning and the intrinsic record, “dummy source structure” should be construed as a structure that does not function as a source to memory cells. KuhnII, ¶59. The claim term at issue is “dummy source

structure” rather than “source structure,” and Patent Owner’s construction properly gives meaning to the word “dummy.” KuhnII, ¶60.

Moreover, the ’872 patent teaches that the dummy source structures do not function as a source to the memory cells. KuhnII, ¶61. For example, the “dummy source structures”—as the qualifying term “dummy” suggests—“function[] as a mechanical supporting structure.” Ex. 1001, 16:38-44. And while the ’872 patent teaches that the dummy source structures may function as “interconnects to connect 3D memory device 100 with *other* peripheral devices,” the ’872 patent never describes the dummy source structure functioning as a source to the memory cells. *See, e.g.*, ’872, 5:40-43, 11:46-49; KuhnII, ¶61. For example, the specification explains that “[w]hen conductive materials are used to fill dummy source hole 212 (e.g., contact 244), the dummy source structure 246 may function as an interconnect to connect 3D memory device 100 with other peripheral devices,” and “[w]hen dielectric materials are used to fill dummy source hole 212, dummy source structure 246 may function as a mechanical support structure to improve the stability of the staircase region.” Ex. 1001, 16:63-17:3; KuhnII, ¶62. At no point does the specification suggest that a “dummy source structure” can function, oxymoronicly, as a source to the memory cells. As such, “dummy source structure” should be construed as a structure that does not function as a source to the memory cells. KuhnII, ¶63.

Petitioner argues that PO's construction "cannot be correct because it includes a negative limitation" that would read in "a tree house" (Prelim. Reply (Pap. 13) 5), but Petitioner's argument misunderstands the law. The Board is required to construe terms "only to the extent necessary to resolve the controversy." *Realtime Data, LLC v. Iancu*, 912 F.3d 1368, 1375 (Fed. Cir. 2019). To resolve the parties' dispute regarding whether the art teaches dummy source structures, at issue before the Board is whether the term "dummy source structures" includes actual source structures—it does not. KuhnII, ¶¶63-69.

Petitioner's suggestion that "[t]here is no dispute that the 'dummy source structure' may not be a 'dummy,'" is also wrong. Prelim. Reply 5 (citing POPR (Pap. 14), 16). KuhnII, ¶64. While the specification teaches dummy source structures functioning as interconnects (*see* '872, 16:66-17:3), the '872 patent does not teach dummy source structures functioning as actual source structures. *Id.* And Petitioner's strained argument that "source" could mean "source for deposition materials" (as opposed to a source to gates of memory cells) falls flat. KuhnII, ¶65. Petitioner fails to identify any evidence in the intrinsic record where the term "source" means "source for deposition materials"—there is none. Instead, "source" is used consistently with its meaning in relation to semiconductor device operation, namely as the "source" for charge for the transistors forming the memory cells. *See, e.g.,* '872, 16:33-38, 11:8-9; KuhnII, ¶65.

Petitioner premises its arguments on misunderstandings of the specification, which never says that a “dummy” source structure is the same as or includes a “source structure.” The specification states that “[i]n some embodiments, dummy source structure 246 may not connect to channel structures in the inner region.” Prelim. Reply 2 (citing ’872, 16:38-40). While this passage suggests that embodiments of a dummy source structure may or “may not connect to channel structures,” the permissive language there does not suggest that dummy source structures should, can, or may “function as a source to the memory cells.” KuhnII, ¶66.

Petitioner’s argument incorrectly equates the ability of a dummy source structure to “connect to channel structures” to its functioning as a source. But a dummy source structure’s “connect[ion] to channel structures” does not, on its own, establish that the dummy source structure provides a “source to the memory cells” (i.e., connects the memory cells to source power). For example, while one end of the dummy source structure may connect to channel structures via the substrate (or the source plane), the other end of the dummy source structure may be an electrical dead end (e.g., floating) or may connect to peripheral devices instead of a ground source. Accordingly, the cited portion of the specification does not support Petitioner’s interpretation that the dummy source structure provides a “source.” KuhnII, ¶¶67-68.

Petitioner’s counterargument also distorts the ’872’s teaching. *See* Prelim. Reply 4 (citing ’872, Claim 1, 16:66-17:3). KuhnII, ¶68. The ’872 explains that “the dummy source structure 246 may function as an interconnect to connect 3D memory device 100 with other peripheral devices”—not as an interconnect to source the memory cells. ’872, 16:66-17:3. The ’872 does not once disclose or suggest that the dummy source structure provides a source to the memory cells. KuhnII, ¶68.

Petitioner’s argument that Patent Owner never “disclaimed” providing source to the memory cells (Prelim. Reply 4) misapplies the law. Patent Owner’s construction is based on the plain meaning and Patent Owner is not relying on disclaimer, which applies only where “the inventor limited the invention in the course of prosecution, making the claim scope narrower than it would otherwise be.” *Phillips v. AWH Corp.*, 415 F.3d 1303, 1317 (Fed. Cir. 2005) **Error! Bookmark not defined.** Patent Owner’s construction is consistent and commensurate with the plain meaning of “dummy source structure” and simply provides meaning to the term “dummy,” which Petitioner attempts to read out. KuhnII, ¶69.

2. Petitioner’s Proposed Construction Renders the Term “Dummy” Superfluous in Meaning, and Improperly Limits the Term “Dummy Source Structure” to a Process of Manufacture

Petitioner proposed that “dummy source structure” should be construed as a “structure that occupies the void that was used for the gate replacement process.” Petitioner’s proposed construction eviscerates any meaning that the term “dummy”

carries within the context of a “dummy source structure.” Besides, Petitioner’s proposed construction should not be adopted as it improperly limits the term to a process of manufacture. KuhnII, ¶70.

First, Petitioner’s proposed construction is incorrect because it reads out the term “dummy” from “dummy source structure” and conflates dummy source structures with non-dummy source structures that function as the source for memory cells. KuhnII, ¶71. Indeed, structures (e.g., that occupy voids used for gate replacement processes) can be either dummy source structures that do not function as a source for the memory cells, or source structures that function as a source for the memory cells. Petitioner ignores this important distinction between the two types of structures and their functions to improperly force a read on the prior art. While dummy source structures can mimic the physical properties of non-dummy source structures, they do not function as a source, which is the primary function of its non-dummy counterpart. *Id.*, ¶¶72-73. Instead, dummy structures can serve, for example, as load-bearing structures during semiconductor device fabrication, which reduces mechanical stress on non-dummy structures during fabrication. ’872, 5:5:21-48; KuhnII, ¶74. For instance, while dummy source structures may be comprised of conductive material and thus may function as an “interconnect between the 3D memory device and peripheral devices” (’872, 5:37-43), they do not function as the source for memory cells. KuhnII, ¶74. Petitioner’s proposed construction

ignores this key difference and does not properly distinguish between dummy and non-dummy source structures. *Id.*

Second, Petitioner’s proposed construction impermissibly attempts to limit the language of an apparatus—here, the claimed three-dimensional memory device—in such a way as to dictate the process by which the apparatus is made. KuhnII, ¶75. It is well-established that, absent limited exceptions not argued here by Petitioner, the claimed product “is not limited to the process by which it was made,” *Vanguard Prods. Corp. v. Parker Hannifin Corp.*, 234 F.3d 1370, 1372-73 (Fed. Cir. 2000)**Error! Bookmark not defined.** While “process steps can be treated as part of a product claim if the patentee has made clear that the process steps are an essential part of the claimed invention,” *Cont’l Circuits LLC v. Intel Corp.*, 915 F.3d 788, 799 (Fed. Cir. 2019)**Error! Bookmark not defined.**, the term “dummy source structure” on its face is not a process step. KuhnII, ¶75. Indeed, as discussed in connection with §III, during prosecution Applicant expressly elected to restrict the invention to the claimed 3D memory device to the apparatus itself, and not to any process by which the device or its features are made. Ex. 1002 (Part 1 of 2), 458 (5/21/2020 Requirement for Restriction/Elections). In addition, Petitioner has not even attempted to show that “gate replacement process” is an essential part of the claimed invention. KuhnII, ¶¶76-78.

Third, Petitioner has not shown that the “gate replacement process” should

be read into the claims through lexicography or disclaimer that would support such a construction. Petitioner relies on one disclosure, which, in full, reads:

“Also, the arrangement of the dummy source structures may allow the gate electrodes/word lines to be formed with improved uniformity and quality, reducing the resistivity of the gate electrodes/word lines. **For example, the gate-replacement process can be performed to deposit a conductive material through the dummy source holes that subsequently form the dummy source structures.** Because the conductive material travels shorter distances to fill up the lateral recesses for forming the gate electrodes, the gate electrodes are less susceptible to voids or density nonuniformity.”

Pet., 25 (citing '872, 5:49-58). This statement, on its face, is merely an **“example”** of how the claimed dummy source structures **“can”** be formed and does not suggest that “a gate-replacement process” is an essential part of the claimed invention. KuhnII, ¶¶76-78. Indeed, the specification repeatedly qualifies the use of the “gate-replacement process” as merely one possible manufacturing method. *See e.g.*, '872, 4:30-33 (“[A] gate-replacement process is **often** used”), 5:52-55 (“the gate-replacement process **can** be performed to deposit a conductive material through the dummy source holes”), 16:40-49 (“**In some embodiments** ... dummy source structure 246 **may**...function[] as a mechanical supporting structure after gate-replacement process.... **In some embodiments**, ... dummy source structure 246 **may** ... still reach the lower part of the dielectric stack to carry out the gate-

replacement process.”); KuhnII, ¶78.

Moreover, the ’872 discloses that dummy source structures can be formed in several other ways using “one or more thin film deposition processes” such as atomic layer deposition, chemical vapor deposition, and physical vapor deposition. Ex. 1001, 13:55-64; *see also* Ex. 1001, 12:34-36 (defining acronyms), 19:61-20:2 (explaining that “Summary and Abstract sections may set forth one or more but not all exemplary embodiments of the present disclosure as contemplated by the inventor(s)” and that the “breadth and scope of the present disclosure should not be limited by any of the above-described exemplary embodiments, but should be defined only in accordance with the [] claims and their equivalents”). KuhnII, ¶79.

Fourth, Petitioner’s construction impermissibly narrows the claim scope to one particular disclosed embodiment: the gate replacement process. *See In re Am. Acad. of Sci. Tech. Ctr.*, 367 F.3d 1359, 1369 (Fed. Cir. 2004) (“We have cautioned against reading limitations into a claim from the preferred embodiment described in the specification, even if it is the only embodiment described, absent clear disclaimer in the specification.”); *see also Superguide Corp. v. DirecTV Enterprises, Inc.*, 358 F.3d 870, 875 (Fed. Cir. 2004)**Error! Bookmark not defined.**; *Liebel-Flarsheim Co. v. Medrad Inc.*, 358 F.3d 898, 906 (Fed. Cir. 2004)**Error! Bookmark not defined.** (discussing recent cases wherein the court expressly rejected the contention that if a patent describes only a single embodiment, the claims of the patent must be

construed as being limited to that embodiment). KuhnII, ¶80.

In the Decision to Institute (“DI”), the Board refused to adopt Petitioner’s position that “‘dummy source structure’ requires that the structure occupy the void used for the gate replacement process” (DI 12) and correctly construed that “‘dummy source structure’ is a structure that does not function as a source to the memory cells” (*id.*, 11). The Board should maintain this construction for at least the reasons explained above. KuhnII, ¶81.

B. “surrounding” (Claims 1, 13)

The term “surrounding” should be given its plain and ordinary meaning, which, contrary to Petitioner’s arguments, requires features that are more than just on two sides with another structure “between.” KuhnII, ¶¶82-94.

As an initial matter, the Board need not resolve the full scope of “surrounding” and need not determine whether it requires “fully encircling.” KuhnII, ¶83. Petitioner has alleged that the claimed “plurality of dummy source structures surrounding the staircase contact” of Claim 1 is satisfied “by structures on two sides” of the object. Pet., 61; *see generally* Pet., 50-62. Similarly, Patent Owner’s arguments directed to this limitation (§VII.A.2) turn on whether “surrounding” encompasses structures on only two sides. Thus, the Board need only resolve whether “surrounding” encompasses structures on only two sides. KuhnII, ¶83. The Board does not need to reach Petitioner’s purported clarification that “surrounding”

does not “require fully encircling” because the Board is required to construe terms “only to the extent necessary to resolve the controversy.” *Realtime Data, LLC v. Iancu*, 912 F.3d 1368, 1375 (Fed. Cir. 2019)**Error! Bookmark not defined..**

The term “surrounding” does not encompass features that are merely on two sides. *KuhnII*, ¶84. First, the claim term at issue is “surrounding” rather than “between.” Indeed, the claims expressly distinguish the concepts of “surrounding” and “between.” The term “between” is used when reciting the concept of being located somewhere in the middle of two structures and “surrounding” is used when reciting the concept of being located somewhere in the middle of more than two structures. Compare ’872 Claim 17 (“wherein at least *one dummy channel structure is surrounded by at least eight dummy source structures*”) with ’872, Claim 11 (“wherein at least *one dummy source structure is located between the first and second staircase structure*”); see also, e.g., Claim 12, Claim 15, Claim 16.

The ’872 specification likewise repeatedly uses the terms “surrounding” and “between” to describe different concepts. As in the claims, the specification uses “between” when discussing the concept of being located somewhere in the middle of two structures and “surrounding” when discussing the concept of being located somewhere in the middle of more than two structures:

As shown in FIG. 1A, multiple dummy source structures, such as the *four dummy source structures indicated by a diamond shape 146, may surround a staircase contact*, such as staircase contact 122. ... [¶] ...

A plurality of dummy channel structures, such as the *four dummy channel structures indicated by square shape 148, may surround a staircase contact*. The four dummy channel structures may be spaced with nominally equal lateral distances to the staircase contact, as shown in FIG. 1A. In other words, the dummy channel structures surrounding a staircase contact may be evenly distributed around the staircase contact. ... [¶] ... In some embodiments, *at least one dummy source structure may be located between two staircase contacts*. For example, FIG. 1A shows that *two dummy source structures are located between staircase contacts 122 and 122'*. FIG. 1B shows another embodiment in which *two dummy source structures are located between staircase contacts 123 and 123'*, while *one dummy source structure is located between staircase contacts 123' and 123*". FIG. 1C shows yet another embodiment in which *one dummy source structure is located between staircase contacts 125 and 125'*, and *one dummy source structure is located between stair case contacts 125' and 125*". *Other numbers of dummy source structures may also be disposed between two staircase contacts.*"

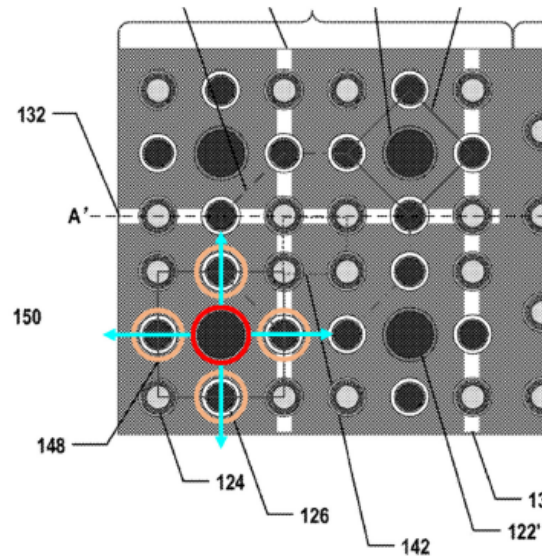
'872, 6:38-7:28. This distinction is used consistently throughout the specification, including when the structures are slits. '872, 4:56-61 ("*[D]ummy channel holes are formed between adjacent GLS*"). KuhnII, ¶85.

Nothing in the '872 teaches that a staircase contact can be "surrounded" by just two dummy source structures. If structures placed on only two sides of an object were within the scope of the plain meaning of "surrounding," then there would have

been no need for the '872 to consistently use different terminology—"located between"—when there are structures on just two sides. KuhnII, ¶¶86-87.

Petitioner's argument that the specification contemplates "less than four dummy source structures that 'surround' a word line contact" (Pet., 28 (citing '872 8:8-11)) is irrelevant. The dispute is not whether less than four (*e.g.*, three) dummy structures can "surround" a word line contact, the dispute is whether exactly two parallel dummy structures can "surround" a word line contact. KuhnII, ¶¶87-89.

Petitioner argues that Figure 1A demonstrates that "'surrounded includes being able to draw four lines outward from the staircase contact with each line being separated from the others by 90 degrees and intersecting a dummy source structure" (Pet., 30), but this argument is convoluted and a far departure from the plain meaning of "surrounding." KuhnII, ¶90. Even if "surrounding" was defined by some minimum angle between structures (as described by Petitioner), Figure 1A illustrates a separation of 90 degrees from the **center** of such structures:



Pet., 31 (Petitioner’s annotations). Thus, this configuration disclosed in the specification with four dummy source structures at 90 degrees is different from—and does not provide support for—a configuration having only two dummy structures, *i.e.* where the angle is 180 degrees. KuhnII, ¶91.

Finally, Petitioner’s extrinsic evidence should be given little weight. KuhnII, ¶92. Petitioner fails to explain the relevance that a lay description of an “isthmus” (provided by the website “<https://www.studycountry-com/wiki/what-is-a-piece-of-land-surrounded-by-water-on-2-sides>” in March of 2024) has to the meaning of “surrounding” as used by the ’872. Pet., 32 (citing Ex. 1018). Similarly, Petitioner’s reliance on U.S. Pat. No. 9,530,492 (the “’492 patent”) is misplaced. Pet., 32 (citing Ex. 1019, 2:14-16). Although the ’492 patent states that “the conventional SBPI operations are strongly affected by the stored V_{ts} of two surrounding NAND cells dispersed in the adjacent left and right BLs” (Ex. 1019, 2:14-16), this passage is

merely referring to the effects of NAND cells in the surroundings (*i.e.*, in the vicinity). KuhnII, ¶93. The '492 patent does not suggest that two NAND cells can surround SBPI operations. And even if Petitioner's interpretation of the '492 patent were correct, it cannot overcome the consistent usage of "surrounding" in the '872, consistent with the plain meaning. *Id.*

In the Institution Decision, the Board correctly noted that "'surrounding' in claim 1 of the '872 patent does not encompass structures on only two sides of an object." DI 16. KuhnII, ¶94.

C. "conductive contact" (Claims 1, 13)

The term "conductive contact" should be construed as **a conductive structure that permits current flow with an adjoining conductive structure**. KuhnII, ¶¶95-111. This construction properly gives meaning to the word "contact" in the claims and is supported by the intrinsic evidence as well as the plain meaning of the word "contact," as evidenced by extrinsic dictionary definitions. *Id.*, ¶96. Petitioner's arguments in its Preliminary Reply either ignore or mischaracterize PO's evidence, while proposing a construction that improperly reads "contact" out of the claim and conflates the term "conductive contact" with a conductive core. Prelim. Rep., 5-7. KuhnII, ¶97. Petitioner's construction should be rejected.

1. Patent Owner's Construction Is Supported by the Intrinsic Evidence

The claims, specification, and drawings of the '872 support construing

“conductive contact” as a conductive structure that permits current flow with an adjoining conductive structure.³ . KuhnII, ¶¶98.

First, the word “contact” in the claims supports PO’s construction. The ’872’s claims expressly require a “conductive **contact**” rather than a conductive material or conductive core: “each dummy source structure comprises a conductive contact.” See Claim 1. PO’s construction, which requires a conductive structure that permits current flow with an adjoining conductive structure, properly gives meaning the term “contact” because the “contact” structure is what permits the conductive material to conduct current with an adjoining conductive structure. KuhnII, ¶¶98-100.

In the Institution Decision, the Board stated that the claims do not “require contact between a dummy source structure and another structure” (DI 23-24), but Patent Owner respectfully submits that this interpretation improperly reads out the express limitation of “contact” from the claimed “conductive contact.” KuhnII, ¶101. While a conductive core may provide a “conductive contact” in some situations, the mere presence of a conductive material or conductive core alone does not necessarily mean that a contact is present, as the Board’s interpretation would suggest. *Id.*

³ Petitioner does not appear to dispute the “conductive” requirement of this claim term. Prelim. Rep., 6; KuhnII, ¶¶95-97.

Moreover, reading out an express claim limitation in this manner is improper. See *Merck & Co. v. Teva Pharms. USA, Inc.*, 395 F.3d 1364, 1372 (Fed. Cir. 2005) **Error! Bookmark not defined.** (“A claim construction that gives meaning to all the terms of the claim is preferred over one that does not do so.”).

Second, the specification supports PO’s construction because it describes, for example, dummy source structures that contact another structure such as a peripheral device, and therefore permit current flow to another conductive structure. KuhnII, ¶102. For example, the ’872 patent shows that in Fig. 2L, each dummy source structure 246 (shown in black)—which is filled with conductive material—extends vertically through a staircase structure and an insulation layer to form an exposed conductive contact 244. Ex. 1001, 11:37-39, 16:21-32, 16:63-66; . KuhnII, ¶102.

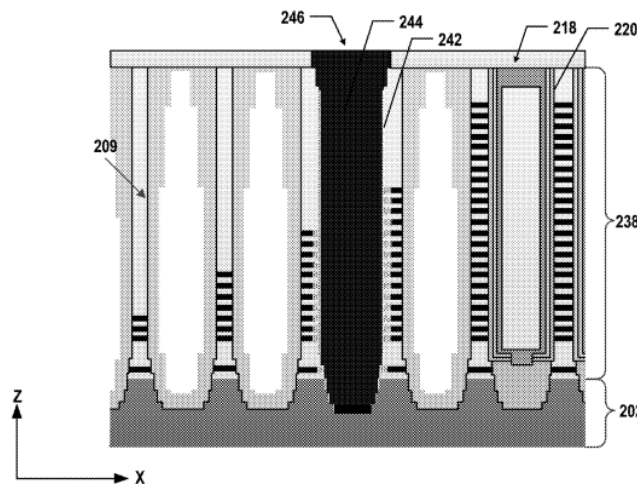


FIG. 2L

This exposed conductive contact enables the dummy source structure to “function as an interconnect to connect 3D memory device 100 with other peripheral devices.”

Id., 16:63-66. KuhnII, ¶103. Thus, the specification and drawings confirm that the structure of the conductive material in the “conductive contact” includes a “contact” with another structure, such that the conductive structure permits current flow with an adjoining conductive structure. KuhnII, ¶104. Conversely—as Petitioner’s expert, Dr. Banerjee, concedes—a structure that is completely enclosed by an insulator does not form such a contact. *See* Ex. 2008, 38:11-15 (“[T]he insulator material is what’s used to create a scenario where you have no direct electrical **contact** with the rest of the device.”); *see also id.* 28:9-11; KuhnII, ¶105. In the Institution Decision, the Board misinterpreted the portion of the specification that states “[w]hen conductive materials are used to fill dummy source hole 212 (e.g., contact 244), the dummy source structure 246 may function as an interconnect to connect 3D memory device 100 with other peripheral devices.” ’872, 16:63-66; KuhnII, ¶106. The Board read this passage as disclosing a “**dummy source structure**” with “**contact 244**” that “may or may not” function as an interconnect (DI 23-24), but the specification instead states that the “**dummy source structure**” with “**conductive material**” may or may not function as an interconnect, and that the “contact 244” is an example (“e.g.”) of using a conductive material to form an interconnect. Logically, if a dummy source structure with conductive material is completely enclosed with insulator, for example, then it would not function as an interconnect (or as a “contact”), even though conductive material is in the dummy

source structure. This passage of the '872 specification is worded to allow for those exceptions. KuhnII, ¶106.

Moreover, the Board's conclusion that the above-cited passage of the '872 allows for a contact that does not "function as an interconnect" (DI 23) is still consistent with PO's construction. PO's construction, which requires a conductive structure that permits current flow with an adjoining conductive structure, limits the **structure**. The conductive **structure** must permit current flow with an adjoining conductive structure, for example by contacting an interconnect or other conductive structure. PO's construction does not require that the conductive contact actually have current passing through it—indeed, the claimed conductive contact is part of the "dummy source structure," which "does not function as a source to memory cells." See §V.A. KuhnII, ¶107. PO's construction also does not limit the location of the "contact" on the dummy source structures (e.g., whether the contact is on top of the dummy source structures or elsewhere). Thus, the '872 specification is consistent with PO's construction. KuhnII, ¶108.

Therefore, the intrinsic record, including the '872 claims and specification, supports the construction that the "conductive contact" is a conductive structure that permits current flow with an adjoining conductive structure. KuhnII, ¶109.

2. Extrinsic Evidence Supports Patent Owner's Construction

The extrinsic evidence further supports PO's construction of "conductive

contact,” which requires a conductive structure that permits current flow with an adjoining conductive structure. For example, “electric contact” is defined as “[a] physical contact that permits current flow between conducting parts.” *See* Ex. 2011 (McGraw-Hill Dictionary of Scientific and Technical Terms, Sixth Edition). As another example, “contact” is defined as “the state or condition of physical touching, a connection for the passage of electric current from one thing to another, or a part or device by which such a connection is made.” *See* Ex. 2009 (New Oxford American Dictionary, Third Edition). Similarly, “contact” is defined in another technical dictionary as “[t]he coming together, touching, union, or junction of surfaces or objects, or the junction of two conductors so that current may flow.” *See* Ex. 2010 (Wiley Electrical and Electronics Engineering Dictionary). PO’s construction is consistent with the plain meaning of “contact” as confirmed by these references. In contrast, Petitioner’s construction—i.e., “conductive material that fills the dummy source hole” (Prelim. Rep., 6)—would read on a metal structure that is completely enclosed by insulator and therefore contradicts and ignores the well-understood meaning of “contact.” KuhnII, ¶110.

Accordingly, the Board should construe the term “conductive contact” as **a conductive structure that permits current flow with an adjoining conductive structure.** *Id.*, ¶111.

VI. THE PRIOR ART REFERENCES RELIED UPON⁴

A. U.S. Patent No. 9,859,297 (“Park”) (Ex. 1005)

Petitioner does not contend that Park anticipates the Challenged Claims, and instead argues only that it renders obvious certain claims, including the sole independent Challenged Claim, Claim 1. Pet., 8, 40-74.

Park discloses aspects of a memory device upon which the '872 improves. Park describes a semiconductor device including: a substrate having a cell region and stepped dummy region; a common source line (“CSL”); gate lines; insulating interlayer patterns; dummy patterns; and dummy source lines. Ex. 1005, 6:1-9:3, Figs. 1-2. Park’s semiconductor device includes both **common source lines**, which function as a common source for the memory cell (and are therefore not dummy source structures), and **dummy source lines** in the dummy region. Ex. 1005, 13:53-58, 23:1-4, Fig. 1, Fig. 13. As illustrated in Figures 1 and 13 below, **common source lines** extend in the “2nd direction,” and are spaced apart from each other along the “3rd direction,” of the cell region; the **dummy source lines**, on the other hand, extend in the “3rd direction,” and are spaced apart from each other along the “1st direction,” of the dummy region:

⁴ For the purposes of the present IPR proceeding only, Patent Owner does not contest that the Park and Tessariol references qualify as prior art to the '872.

FIG. 13

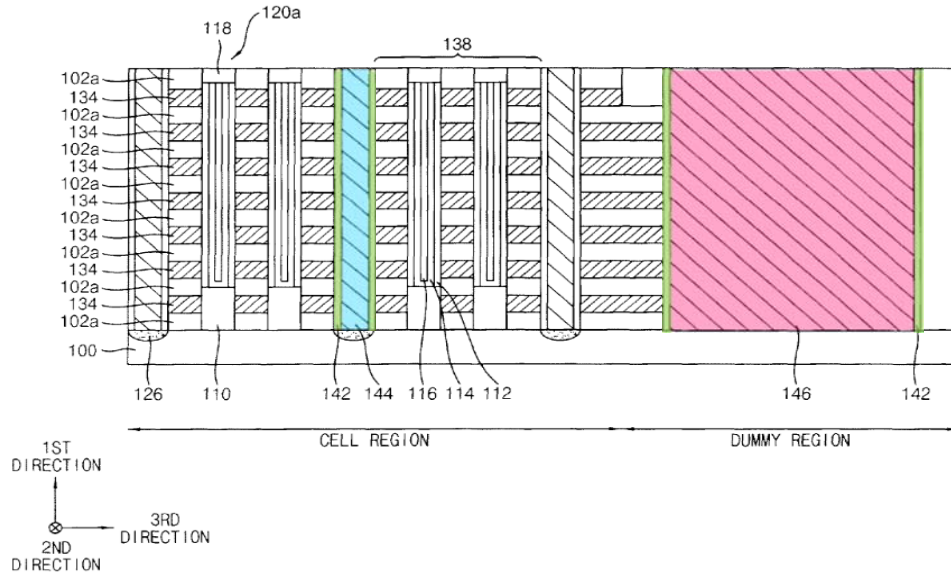
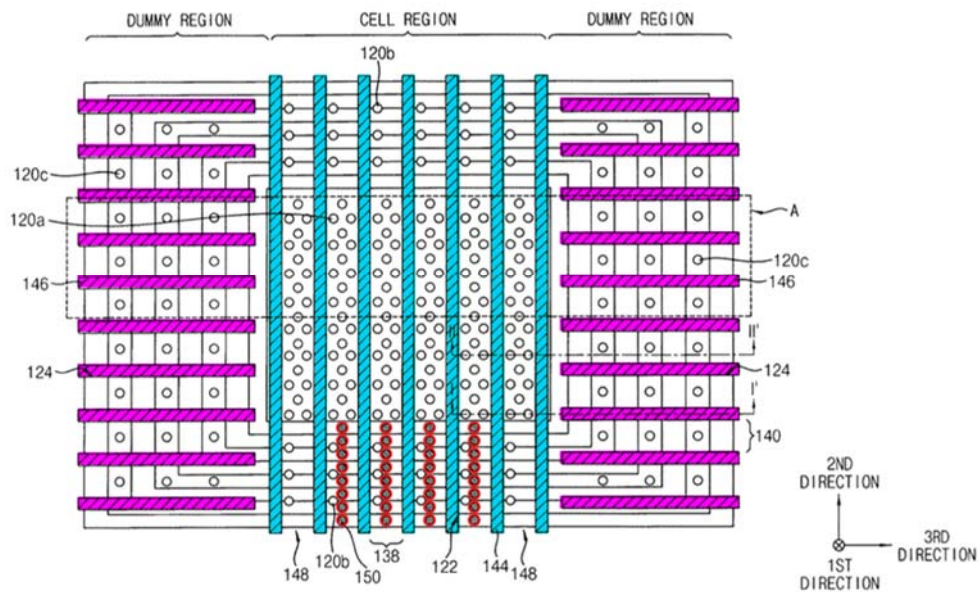


FIG. 1



Ex. 1005, Fig. 13, Fig. 1, 3:6-9.

Park further discloses that between the **common source lines** is a wiring region, where **contact plugs** (annotated in red in Figure 1 above) are formed in

contact holes etched through the upper insulation layers and electrically connect to the gate lines. Ex. 1005, Fig. 1, 7:26-37, 13:60-54. Because Park's contact plugs are just between two **common source lines**, the **common source lines** do not surround the **contact plugs**. See Ex. 1005, Fig. 1. Park's **dummy source lines** also do not surround the **contact plugs** as shown above in Fig. 1.

B. U.S. Patent Pub No. 2019/0081061 (“Tessariol”) (Ex. 1006)

Petitioner does not contend that Tessariol anticipates the Challenged Claims, and instead argues only that it renders obvious the Challenged Claims. Pet., 8, 74-101.

Tessariol discloses aspects of three-dimensional memory devices upon which the '872 claims improve. Ex. 1006, [0006]. Tessariol's circuit structure includes a stair step structure composed of **vertically-stacked alternating layers** (*e.g.*, alternating layers of insulative material and conductive materials). Ex. 1006, [0029], [0031], [0034]. Dummy-structure openings and via openings are formed through the vertically-alternating layers. Ex. 1006, [0037]. Within via openings **operative conductive vias** are formed and within dummy openings **dummy structures** are formed—each extending through the **vertically-alternating layers**, as depicted below. Ex. 1006, [0038].

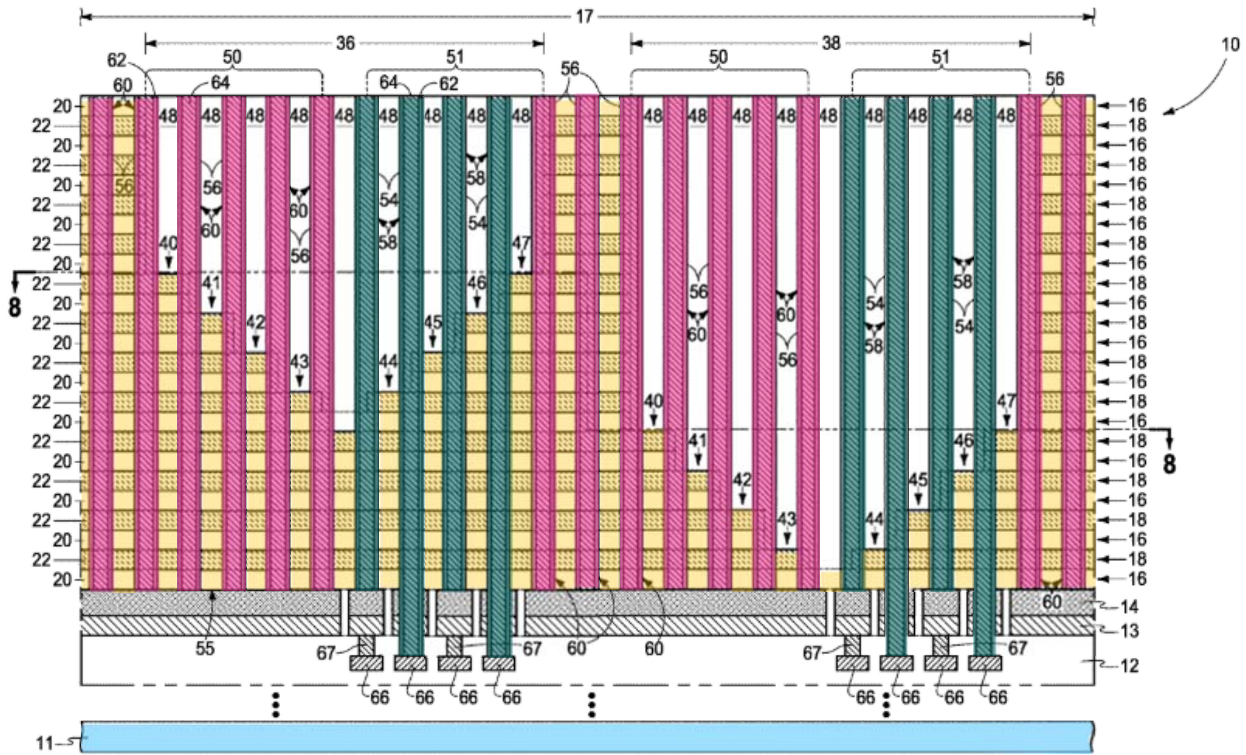


FIG. 9

Tessariol discloses that **operative conductive vias** and **dummy structures** may be composed of an **insulative lining** (e.g., silicon dioxide and/or silicon) and a **conductive core**, as depicted below. Ex. 1006, [0038]. Whereas the **operative conductive vias** may “directly electrically couple to individual conductive lines,” Tessariol does not disclose that the **dummy structures** can comprise a conductive contact. As Tessariol explains, “[i]n this document, *a ‘dummy structure’ refers to a structure which is* used to mimic a physical property of another structure (e.g., presence, or physical load-carrying/supporting ability of *an operative structure*) *and which may comprise a circuit inoperable electrical dead end* (e.g., is not part of a current flow path of a circuit even if conductive).” Ex. 1006, [0068]. In other words,

while dummy structures may be conductive, they are not part of a circuit because they only mimic the physical properties (not the functional properties) of their operative counterparts. Consequently, even as electrical dead ends, dummy structures do not have a conductive contact.

Tessariol additionally discloses **operating conductive vias**, depicted in the color-annotated below:

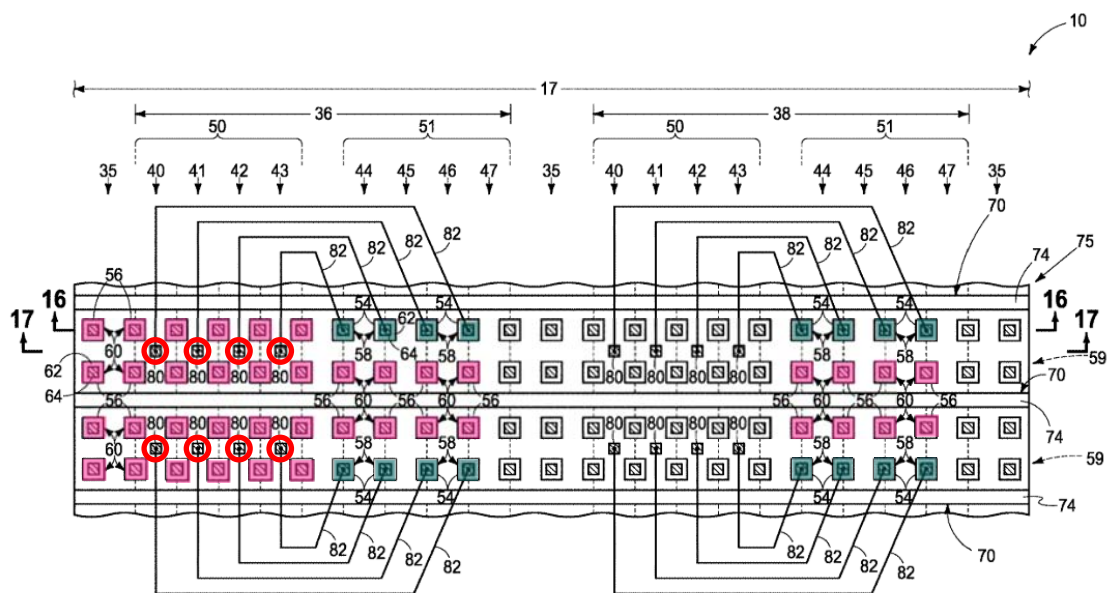


FIG. 15

These **operating conductive vias** each connect to a conductive step of the **vertically-alternating layers**, extend through the layers, and are “directly electrically coupled to one another by an interconnect line” above the alternating layers. Ex. 1006, [0046], [0052].



VII. GROUND 1: PARK DOES NOT DISCLOSE OR RENDER OBVIOUS CLAIMS 1-6, 11-13

Park fails to disclose or render obvious the Challenged Claims at least because Park fails to disclose or render obvious multiple requirements of limitation [1.e] of the sole challenged independent claim, including “dummy source structures” and dummy source structures “surrounding” the staircase contact under the proper construction of those terms (§V.A-B). As for the added limitations of dependent claims 2-6 and 11, Petitioner continues its pattern of inconsistently mapping either Park’s common source lines or dummy source lines to the claimed “dummy source structures,” and additionally fails to show that Park teaches the “distance” and “row” requirements of claims 3-4 and 6. KuhnII, ¶¶120-163.

A. Independent Claim 1: Park Does Not Disclose or Render Obvious Multiple Requirements of Limitation [1.e]

Petitioner fails to show that Park discloses or renders obvious at least two requirements of limitation [1.e]: “a plurality of dummy source structures each extending vertically through the staircase structure, the plurality of dummy source structures surrounding the staircase contact.” Park’s common source lines and dummy source lines, alone or collectively, are not “surrounding” the purported “staircase contact.” KuhnII, ¶121. Instead, Park’s disclosures are nearly identical to the very prior art that the invention of the ’872 improves upon. Second, Ground 1 is reliant on Petitioner’s incorrect construction for “dummy source structure.” Under the proper construction of this term, the structures identified by Petitioner function as a source and are therefore not “dummy source structures.” KuhnII, ¶¶122-123.

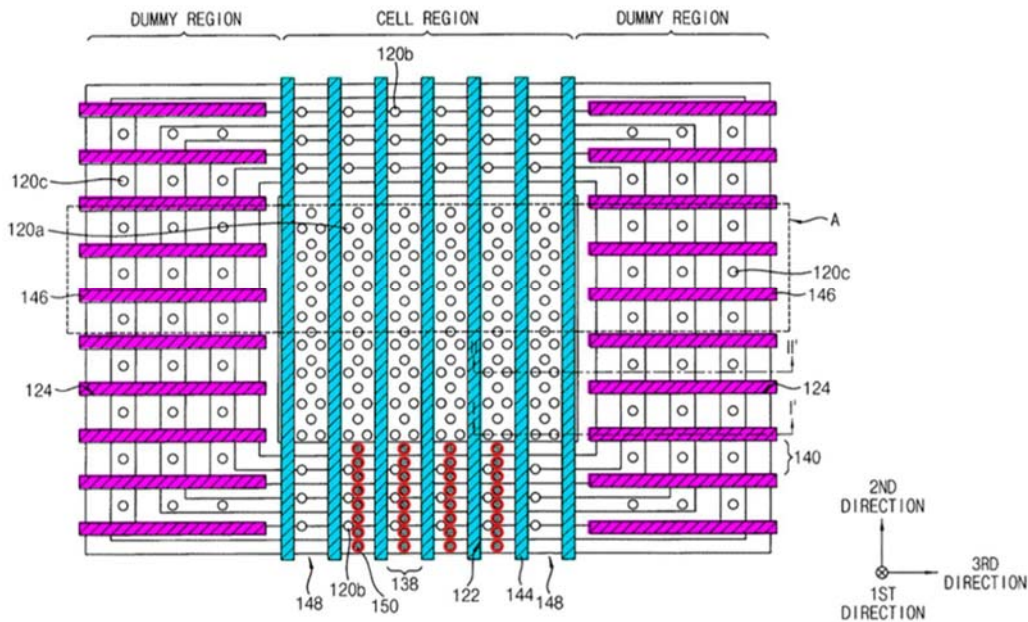
1. Park’s Common Source Lines and Dummy Source Lines, Alone or in Combination, Are Not “Surrounding” the Contact Plugs (Limitation [1.e])

Park’s alleged “dummy source structures” are not “surrounding the staircase contact” under the proper construction of “surrounding”—that the term does not encompass structures on only two sides of an object (§V.B). *See also* DI, 16; KuhnII, ¶¶124-134. The staircase contact of Park is merely “between” two alleged dummy source structures, and therefore the alleged dummy source structures are not surrounding the staircase contact. KuhnII, ¶¶124-125.

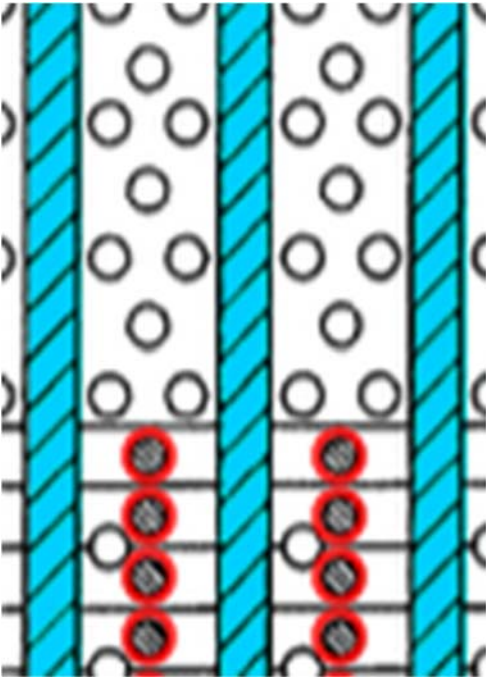
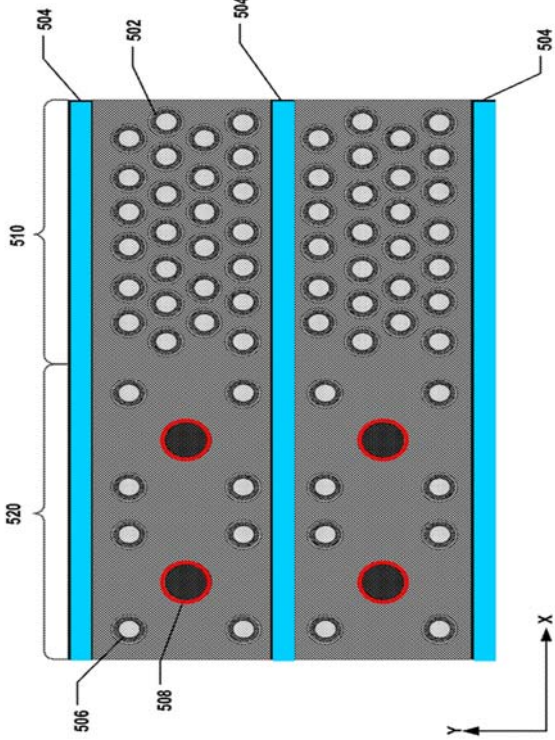
Limitation [1.e] requires “the plurality of dummy source structures” to be “surrounding the staircase contact.” KuhnII, ¶126. As discussed in §V.B, this requires that the dummy source structures are on more than just two sides of the staircase contact, and it is insufficient for a staircase contact to be merely “between” two dummy source structures. *Id.*

Park maps two separate elements—**common source lines 144** and **dummy source lines 146**—to the ’872’s “dummy source structures” (Pet., 2-3, 50-51), but neither structure surrounds the alleged staircase contacts. KuhnII, ¶127. First, Park’s **dummy source lines** do not “surround” the contact plugs (the alleged “staircase contact”) as depicted below, because the **contact plugs** are merely between the two sets of **dummy source lines**. Tellingly, although Petitioner argues that common source lines 144 and dummy source lines 146 collectively surround the contact plugs 150 (Pet., 58), Petitioner’s explanation focuses solely on the common source lines 144 alone. See Pet., 58-62. KuhnII, ¶128.

FIG. 1



Park's **common source lines** also do not surround the **contact plugs** (the alleged “staircase contact”) because the **common source lines** are merely on two sides of the **contact plugs**—there is no dispute that Park's common source lines 144 fail to disclose or render obvious this limitation under the proper construction. KuhnII, ¶129. Moreover, Petitioner overlooks that the configuration of Park's common source line 144 and contact plug 150 is precisely the configuration that the invention distinguished over the admitted prior art. *Id.* Below is a side-by-side comparison of the relevant portions:

	
Excerpt of Petitioner's annotated Park, Fig. 1 (Pet., 59) (highlighting contact plugs 150 in red between parallel common source line 144 in blue). <i>See also</i> Ex. 1005, 2:46-47, 5:27-33, 6:15-17.	'872, Fig. 5 (rotated view of admitted prior art, illustrating staircase contacts 508 in red between parallel gate line slits 504 in blue). <i>See also</i> Ex. 1001, 5:1-14.

The '872 discloses that the prior art GLSs extend through a staircase region that includes staircase contacts 508. Ex. 1001, 5:1-8. Similarly, Park's common source lines 144 cross through the wiring region that contain contact plugs 150. Ex. 1006, 13:62-64. The '872 discloses that characteristics of "the shape of GLS 504" is "a slit shape with a dimension along the extending direction (or the x-direction) much greater than the dimension along the expanding dimension (or the y-direction)." Ex. 1001, 5:23-25. Similarly, Park's common source lines 144 "extend in the second

direction” in “a plan view,” in which the “second direction [is] parallel to the top surface of the substrate,” and much greater than in the third direction. KuhnII, ¶130. Accordingly, Park’s common source lines 144 geometry and arrangement are substantially the same as that of the prior art GLSs that the ’872 improved upon. Notably, the ’872 uses the term “between”—not “surround”—to describe the “dummy channel holes [] between adjacent GLSs” in Figure 5. ’872, 4:56-57, 5:1-2. KuhnII, ¶131. Furthermore, Park discloses, at best, the same configuration of alleged staircase contacts “between” parallel gate line slits, rather than “surround[ed]” by dummy source structures. KuhnII, ¶132.

Thus, under the proper construction of “surrounding” as excluding features that are merely on two sides with another structure between, Park’s alleged “dummy source structures”—common source lines and/or dummy source lines—are not “surrounding the staircase contact” as required by the Challenged Claims. KuhnII, ¶133. The Institution Decision correctly notes that “[b]ecause we determine that ‘surrounding’ does not encompass structures on only two sides of an object, we are not persuaded, on this record, that Park teaches dummy source structures ‘surrounding the staircase contact’ as recited in claim 1.” DI 16, 23; KuhnII, ¶134.

2. Park’s Common Source Lines Are Not “Dummy Source Structures” (Limitation [1.e])

Park’s common source lines—Petitioner’s alleged “dummy source structures”—function as a common source lines and are therefore not “dummy source

structures” as properly construed. KuhnII, ¶¶135-145.

All Challenged Claims require “a plurality of dummy source structures.” As discussed in §V.A (Claim Construction), the claimed “dummy source structure” is a structure that does not function as a source to memory cells. KuhnII, ¶136. As discussed, Park does not disclose “dummy source structures” that meet every requirement of the claims, and so Petitioner attempts to map a combination of two separate elements—common source lines 144 and dummy source lines 146—to the ’872’s “dummy source structure.” Pet., 2-3, 50-51; KuhnII, ¶137.

As an initial matter, Park’s **dummy source lines** cannot be the claimed “dummy source structures” because Petitioner does not map Park’s dummy source lines to every relevant claim requirement. As discussed in §VII.A.1, while Petitioner alleges that Park’s common source lines 144 and dummy source lines 146 are collectively “a plurality of dummy source structures,” Petitioner maps only the common source lines to other limitations of the claims relating to the dummy source structure, such as the requirement of “the plurality of dummy source structures surrounding the staircase contact” as discussed above. Pet. 50-62. Because Petitioner does not map Park’s dummy source lines to the “surrounding” requirement, Park’s dummy source lines cannot be the claimed “dummy source structures” of the Challenged Claims. KuhnII, ¶138.

In addition, Park’s **common source lines** are not dummy source structures

because they function as a source to the memory cells and are, therefore, actual—not dummy—source structures. KuhnII, ¶139. Park expressly distinguishes between the “common source line” for the memory cell structure, which functions as the source line, and a “dummy source line.” See, e.g., Ex. 1005, 6:1-11, 7:59-60, 13:39-41. Similarly, Park’s figures show separate regions where the common source line and dummy source lines are located—the common source line is in the “cell region” and the dummy source line is in the “dummy region.” Ex. 1005, Fig. 1. Thus, Park’s common source lines 144 are not dummy source structures. KuhnII, ¶140.

Petitioner attempts to incorrectly equate Park’s common source line to the ’872’s teaching that “‘dummy source structures’ can [make] ‘contact with the substrate and may provide interconnect between the 3D memory device and peripheral devices.’” Pet., 55-56 (omitting citations); KuhnII, ¶141. Contrary to Petitioner’s suggestion, the ’872’s disclosure that “dummy source structures” may “serve as an interconnect between the 3D memory devices and peripheral devices” (Ex. 1001, 5:40-43) does not suggest that Park’s common source line is also a dummy structure. KuhnII, ¶141. Specifically, the interconnect referenced in the ’872 is not a source line. The ’872 explains that the “peripheral device” that the dummy source structure may connect to includes “peripheral circuits used for facilitating the operation of the 3D memory device 100, such as page buffers,

decoders, and latches.” Ex. 1001, 9:37-40; KuhnII, ¶142. As such, the ’872 “dummy source structure” does not function as a source to a memory cell. Park’s common source lines 144, on the other hand, do function as the source to memory cells, and therefore common source lines 144 are **actual** source structures and not **dummy** source structures. KuhnII, ¶142.

In the Institution Decision, the Board correctly noted that “[b]ased on the current record, we are not persuaded that Petitioner sufficiently shows that Park teaches the claimed ‘dummy source structure.’” DI 21. KuhnII, ¶143. The Board distinguished the common source lines from the dummy source lines and stated that “common source lines 144 are disposed on the cell region of the substrate while dummy source lines 146 are disposed on the dummy region alone,” and therefore the common source lines and the dummy source lines “may not operate in the same way or serve the same purpose.” *Id.*, 22. Tellingly, Petitioner makes no effort to explain why common source lines do not function as designed, i.e., as sources, but instead, as **dummy** source lines. KuhnII, ¶¶143-144.

Accordingly, Park does not disclose “dummy source structures” as claimed. *See also* DI 22 (“[N]either Petitioner nor Dr. Banerjee sufficiently explains why Park’s common source lines 144 are ‘structures that do not function as sources for the memory cell.’”). KuhnII, ¶145.

B. Claim 2: Park’s Dummy Source Structures Are Not Located Adjacent to the Staircase Contact

Petitioner again has not pointed to “dummy source structures” that meet every applicable element of the Challenged Claims. Petitioner does not allege that Park’s dummy source lines are adjacent to the staircase contact as required by Claim 2. Pet. 64-65. For Claim 2, Petitioner instead maps the claimed “plurality of dummy source structures” to Park’s common source lines 144 (Pet. 64-65), but as explained in Claim 1, Park’s common source lines 144 are not “dummy source structures” because they function as a source to memory cells. *See* §VII.A.2; KuhnII, ¶146. Accordingly, Petitioner has failed to show that Park discloses or renders obvious Claim 2. KuhnII, ¶147.

C. Claim 3: At Least Two of Park’s Dummy Structures are Not of Nominally Equal Lateral Distances to the Staircase Contact

Petitioner fails to show that Park discloses “at least two of the plurality of dummy source structures are of nominally equal lateral distances to the staircase contact” as required by Claim 3 because Petitioner’s reliance on Park’s Fig. 1 is insufficient to show that the claimed distance-based requirement is satisfied. KuhnII, ¶148. With respect to Park’s dummy source lines 146, Petitioner points to annotated lines in Park’s Fig. 1 as purporting to show uniform distribution, but Fig. 1 does not include a scale, dimensions, or any other means to measure distances between components. Pet., 65-66; KuhnII, ¶149. When a reference does not disclose that the

drawings are to scale and is silent as to dimensions, arguments based on measurement of the drawing features are of little value. *See Hockerson-Halberstadt, Inc. v. Avia Group Int’l*, 222 F.3d 951, 956 (Fed. Cir. 2000) (“[I]t is well established that patent drawings do not define the precise proportions of the elements and may not be relied on to show particular sizes if the specification is completely silent on the issue.”); *see also* MPEP 2125. With respect to Park’s common source lines 144, Petitioner does not even annotate Figure 1 to attempt to show the relative distances, but even if Petitioner had done so, such arguments would be insufficient for the reasons discussed above for dummy source lines 146. KuhnII, ¶150. Finally, Petitioner does not argue that it would have been obvious to modify Park such that the alleged dummy structures are of nominally equal lateral distances to the alleged staircase contact. KuhnII, ¶151.

Accordingly, Park does not disclose or render obvious Claim 3. KuhnII, ¶152.

D. Claim 4: Park’s Dummy Structures Are Not of Nominally Equal Lateral Distances to the Staircase Contact

For the same reasons explained above for Claim 3, Petitioner’s reliance on figures is insufficient to show that that the plurality of purported dummy source structures are of “nominally equal” lateral distances to the purported staircase contact. *See* §VII.C. Thus, Park does not disclose or render obvious Claim 4. KuhnII, ¶¶153-154.

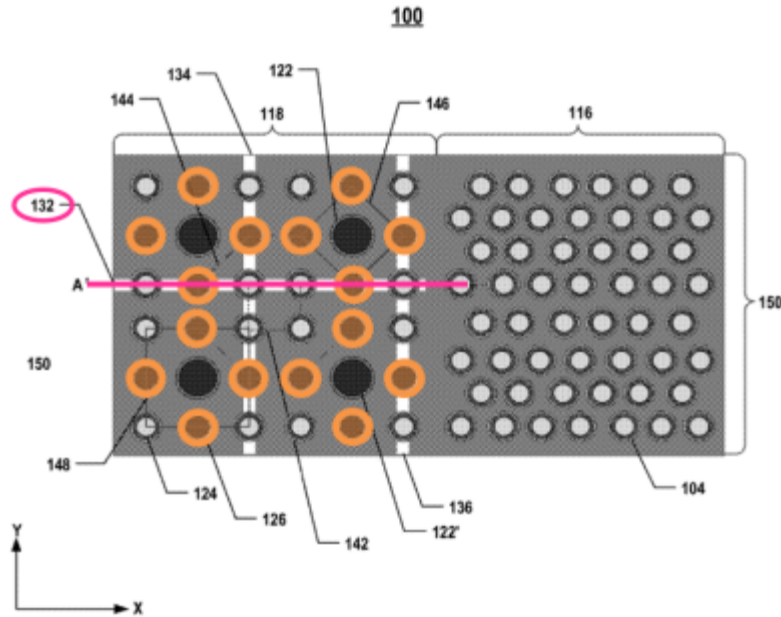
E. Claim 5: Park’s Dummy Source Structures Are Not Arranged in a First Row That Extends Along a First Lateral Direction

Petitioner again has not pointed to “dummy source structures” that meet every applicable element of the Challenged Claims. Petitioner does not allege that Park’s common source lines are arranged in a first row that extends along a first lateral direction as required by Claim 5. Pet. 68-69. For claim 5, Petitioner instead maps the claimed “plurality of dummy source structures” to Park’s dummy source lines (Pet. 68-69), but as explained in Claim 1, Park’s dummy source lines do not surround the alleged staircase contact. See §VII.A.1. KuhnII, ¶155. Accordingly, Petitioner has failed to show that Park discloses or renders obvious Claim 5. KuhnII, ¶156.

F. Claim 6: Park’s Dummy Source Structures Are Not Arranged in a Second Row That Is Perpendicular to the First Lateral Direction

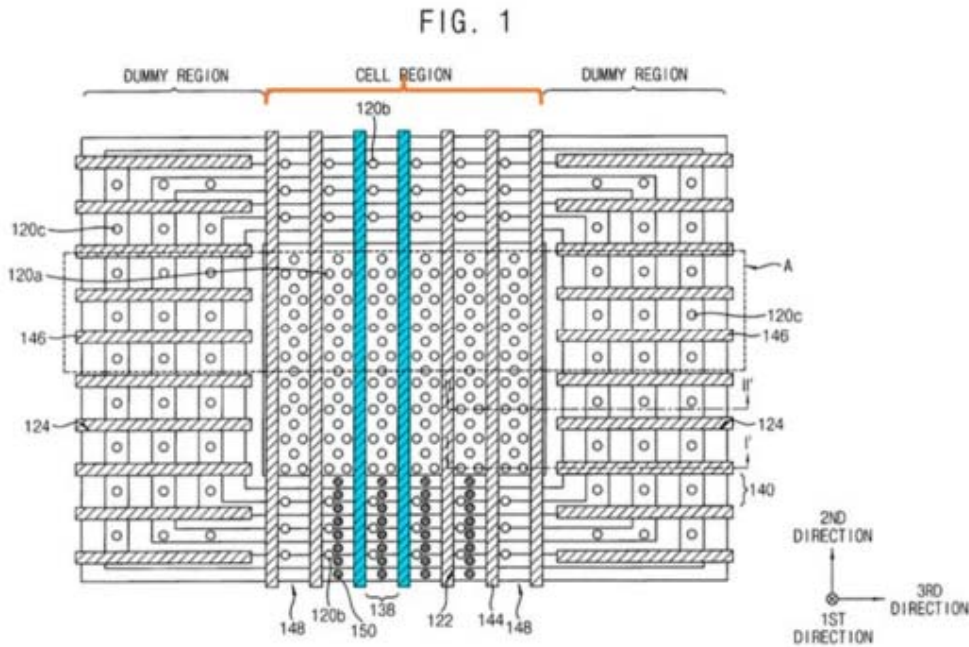
Park’s common source lines, which Petitioner maps to this claim as the alleged “at least two other dummy source structures,” span the entire cell region and, therefore, are not “arranged in a row” as required by Claim 6. KuhnII, ¶¶157-161.

Claim 6 requires “wherein in the plan view, at least two other dummy source structures are arranged in a second row that extends along a second lateral direction perpendicular to the first lateral direction.” *Id.*, ¶158. For example, Figure 1A of the ’872 shows at least two dummy source structures (orange) arranged in row 132:



'872, Fig. 1A (annotated).

Here, Petitioner maps only Park's common source lines to this claim, because it mapped the dummy source lines to claim 5, but fails to show that Park's common source lines are arranged in a row. Pet. 68-71. In Petitioner's mapping, two of Park's common source lines are adjacent to each other in a direction identified as the "3RD DIRECTION" in Park's Figure 1 (KuhnII, ¶159):



Ex. 1005, Fig. 1 (annotated); Pet., 71. Petitioner alleges that the 3RD DIRECTION (“east to west”) is the alleged row of common source lines. Pet., 70-71. However, these common source lines are not “arranged in a second **row**.” While the common source lines are aligned laterally (in the “3RD DIRECTION”), they each extend across the entire cell region in the “2ND DIRECTION” (annotated in orange in Figure 1 above), rather than in a row. This extension means that the common source lines occupy the entire space of the cell region, rather than being organized in row. KuhnII, ¶160. Thus, Park’s alleged dummy source structures are not “arranged in a second row” as required by Claim 6. KuhnII, ¶161.

G. Claim 11: Park’s Dummy Source Structure Is Not Located Between First and Second Staircase Contacts

For Claim 11, Petitioner maps the claimed “at least one dummy source structure” to Park’s common source lines 144 (Pet. 71-72), but as explained in Claim 1, Park’s common source lines 144 are not “dummy source structures” because they function as common source lines for the memory cells. *See* §VII.A.2; KuhnII, ¶162. Accordingly, Petitioner has failed to show that Park discloses or renders obvious Claim 11. KuhnII, ¶163.

VIII. GROUND 2: TESSARIOL DOES NOT DISCLOSE OR RENDER OBVIOUS CLAIMS 1-6, 11-13

Tessariol does not disclose or render obvious the Challenged Claims at least because the alleged “dummy source structures” do not satisfy multiple requirements of the sole independent claim—claim 1. As for the added limitations of dependent claims 3-4, Petitioner fails to show that Tessariol teaches or renders obvious the claimed “distance” and “row” requirements. KuhnII, ¶¶164-211.

A. Independent Claim 1: Tessariol Does Not Disclose or Render Obvious Multiple Limitations

Tessariol does not disclose or render obvious multiple limitations relating to the claimed “dummy source structures.” Petitioner points to Tessariol’s conductive vias 58 and dummy structures 60 as the alleged dummy source structure, but neither structure satisfies all of the claimed requirements. KuhnII, ¶¶165-169.

As a preliminary matter, even under Petitioner’s incorrect construction of

“conductive contact” (“structure that occupies the void that was used for the gate replacement process,” *see* Pet. 24), Petitioner admits that Tessariol fails to meet the claims. Specifically, Petitioner admits that “Tessariol’s dummy structures 60 and operative conductive vias 58 do not fill the voids used for the sacrificial gate replacement process.” Pet., n.6; KuhnII, ¶166. And under the correct construction of “conductive contact” (see §V.C), neither the conductive vias 58 or the dummy structures 60 meet all the requirements of the claimed dummy source structure. KuhnII, ¶166.

First, Petitioner fails to show that Tessariol’s conductive vias 58 do not function as a source to memory cells as required under the proper construction of “dummy source structures,” and furthermore, the conductive vias do not “surround” the alleged staircase contact as expressly required by limitation [1.e]. KuhnII, ¶167. Second, Tessariol’s dummy structures 60 do not include a “conductive contact” as required by limitation [1.f], and Petitioner has failed to show that a POSITA would have been motivated to couple Tessariol’s dummy structures to its upper-level interconnect lines. *Id.*, ¶168.

Neither the dummy structures 60 nor the conductive vias 58 satisfies all of requirement of the claimed “dummy source structures.” It is insufficient to show that dummy structures 60 satisfy some requirements, while conductive vias satisfy other requirements, when the claim recites that each of the claimed requirements

apply to the “plurality of dummy source structures.” As explained below, neither dummy structures 60 nor conductive vias 58 meets all of the various requirements for the claimed plurality of dummy source structures recited in Claim 1. KuhnII, ¶169.

1. Petitioner Has Not Shown That Tessariol’s Conductive Vias Are “Dummy Source Structures” and, Moreover, the Conductive Vias Do Not “Surround” a Staircase Contact (Limitation [1.e])

Tessariol’s conductive vias 58 do not meet two separate requirements of limitation [1.e]. First, Petitioner fails to show that the conductive vias 58 do not function as a source to memory cells as required under the proper construction of the term. See §V.A; KuhnII, ¶170. Second, Tessariol’s conductive vias 58 do not “surround” the alleged staircase contact, and indeed Petitioner does not even allege that this requirement is met by the conductive vias 58. KuhnII, ¶¶171-172.

(a) Petitioner Fails to Show That Tessariol’s Conductive Vias Are “Dummy Source Structures” Under Proper Construction of the Term (Limitation [1.e])

Petitioner fails to show that Tessariol’s conductive vias 58 are “dummy source structures” because, under the proper construction of the term, Petitioner has not shown that conductive vias 58 are structures that do not function as a source to memory cells. See §VIII.A. Indeed, the Petition includes no analysis of this requirement. *Intelligent Bio-Sys., Inc. v. Illumina Cambridge Ltd.*, 821 F.3d 1359, 1369 (Fed. Cir. 2016) (“Unlike district court litigation—where parties have greater

freedom to revise and develop their arguments over time and in response to newly discovered material—the expedited nature of IPRs bring with it an obligation for petitioners to make their case in their petition to institute.”). Accordingly, Petitioner has not shown that Tessariol discloses limitation [1.e]; KuhnII, ¶173.

(b) Tessariol’s Conductive Vias Do Not “Surround” the Alleged Staircase Contacts (Limitation [1.e])

Tessariol’s conductive vias 58 also do not “surround” the alleged staircase contact as required by limitation [1.e]. KuhnII, ¶¶174-182. Indeed, Petitioner does not even allege that conductive vias 58 satisfy this requirement. Pet. 87-88; KuhnII, ¶175.

Limitation [1.e] requires “the plurality of dummy source structures” to be “surrounding the staircase contact.” As discussed in §V.B, this requires that the dummy source structures are on more than just two sides of the staircase contact, and it is insufficient for a staircase contact to be merely “between” two dummy source structures. KuhnII, ¶176.

Tessariol’s conductive vias 58 do not “surround” the alleged staircase contact (conductive vias 80), and indeed are not even in the same region as the alleged staircase contact. As Petitioner admits, “conductive vias 58 are in regions 51” (Pet., 86) and the alleged staircase contact, in contrast, is located in region 50. Thus, as shown in Fig. 15, below, the **alleged staircase contact (conductive vias 80)** are located only in region 50 adjacent to **conductive vias 58** located region 51. KuhnII,

¶177.

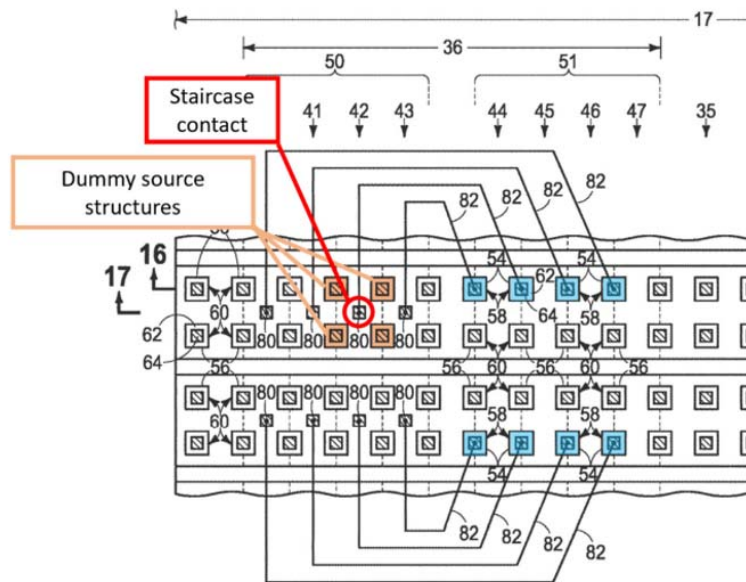


FIG. 15

Tessariol, Fig. 15 (annotated by Petitioner at Pet. 88; conductive via 58 annotations added by PO). Accordingly, the **conductive vias 58** do not surround the **conductive vias 80** in region 50. KuhnII, ¶178.

Petitioner appears to admit that the **conductive vias 58** do not “surround” the alleged staircase contact. Pet., 86; KuhnII, ¶179. As shown in the figure below, Petitioner maps only **dummy structures 60**⁵ to this limitation, not **conductive vias 58**:

⁵ The **dummy structures 60** fail to satisfy other requirements of the claimed “plurality of dummy source structures.” See §VIII.A.2.

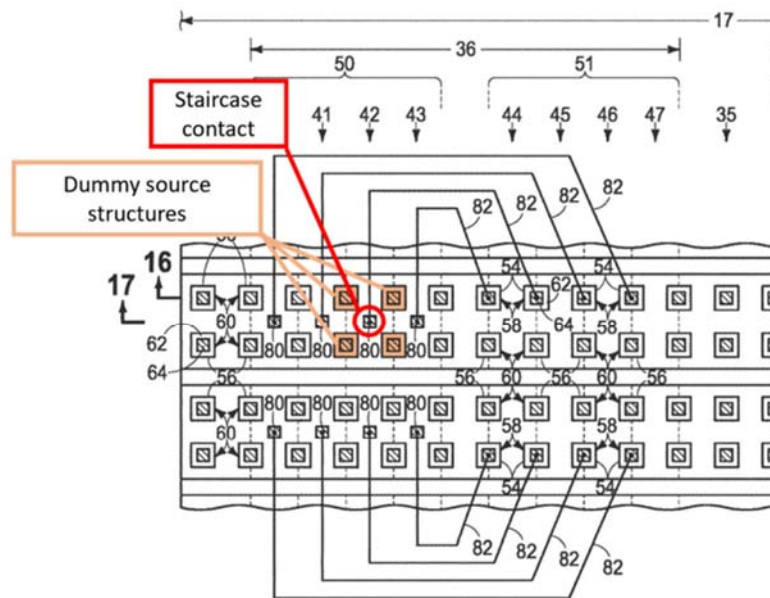


FIG. 15

Tessariol, Fig. 15 (annotated by Petitioner at Pet. 88). Petitioner does even allege that the conductive vias surround the alleged staircase contact (conductive vias 80). Pet. 87-88; KuhnII, ¶¶180-181.

Thus, Tessariol’s conductive vias 58 do not “surround” the alleged staircase contact as required by limitation [1.e]. KuhnII, ¶182.

2. Tessariol’s Dummy Structures Do Not Disclose or Render Obvious Dummy Source Structures Comprising a “Conductive Contact” (Limitation [1.f])

Tessariol’s dummy structures 60 also do not meet all of the requirements for the claimed “plurality of dummy source structures.” KuhnII, ¶¶183-195. Specifically, Tessariol’s dummy structures 60 do not meet at least the requirement of limitation [1.f] that the dummy source structures must comprise a “conductive

contact” because Petitioner has not shown that dummy structure 60 in Tessariol is a conductive structure that permits current flow with an adjoining conductive structure. KuhnII, ¶184. Recognizing this gap, Petitioner argues that POSITA would have modified Tessariol to connect dummy structures 60 to upper-level interconnects, but Petitioner’s only alleged motivation is conclusory and contradicted by Tessariol. KuhnII, ¶185.

(a) Tessariol’s Dummy Structures Do Not Comprise a “Conductive Contact” Under the Proper Construction (Limitation [1.f])

Petitioner has not shown that Tessariol’s dummy structures 60 include a “conductive contact” because Petitioner has not shown that dummy structure 60 has a conductive structure that permits current flow with an adjoining conductive structure as required under the proper construction of “conductive contact” (§V.C). KuhnII, ¶186.

Claim 1 requires that “each of the dummy source structures comprises a conductive contact.” As explained in Section V.C, “conductive contact” means a conductive structure that permits current flow with an adjoining conductive structure. KuhnII, ¶187. For example, the ’872 patent shows dummy source structures 246, which are made with conductive material, extending vertically through a staircase structure and an insulation layer to form an exposed conductive contact 244. Ex. 1001, 11:37-39, 16:21-32, 16:63-66; KuhnII, ¶187. This conductive contact enables

the dummy source structure to “function as an interconnect to connect 3D memory device 100 with other peripheral devices” (*id.*, 16:63-66), and in view of this connection, the conductive contact structure is a conductive structure that permits current flow with an adjoining conductive structure, as required by PO’s construction. KuhnII, ¶188.

In contrast, Petitioner has not shown that dummy structures 60 in Tessariol is a conductive structure that permits current flow with an adjoining conductive structure. KuhnII, ¶189. On the sides, Tessariol’s dummy structures 60 are covered by an insulating lining 62. Tessariol, [0038], Fig. 16. KuhnII, ¶190. Tessariol’s dummy structures 60 do not connect to upper-level interconnects, and instead are covered by insulating material 86. *Id.*, [0046], Fig. 16. KuhnII, ¶191. Finally, the bottoms of dummy structures 60 land on a substrate. KuhnII, ¶192. For all of these sides, Petitioner has not shown that the structure is a conductive structure that permits current flow with an adjoining conductive structure. KuhnII, ¶¶189-195. Indeed, Petitioner has provided no argument in its Petition that there is a conductive contact with the insulating lining 62, insulating material 86, or the substrate. And Dr. Banerjee confirms that conductive material—such as Tessariol’s interconnect lines and conductive vias—that is surrounded by insulation material could not conduct current with other structures like the claimed “conductive contacts.” Ex. 2008, 38:11-15 (“[T]he insulator material is what’s used to create a scenario where

you have no direct electrical contact with the rest of the device.”); *see also id.* 28:9-11 (“[W]hen you apply a voltage across the insulated layer there should not be any significant conduction currents flowing through it.”).

Accordingly, Petitioner has not shown that Tessariol’s dummy structures comprise a “conductive contact,” as required by claim limitation [1.f]. KuhnII, ¶195.

(b) A POSITA Would Not Have Been Motivated to Couple Tessariol’s Dummy Source Structures to Upper-Level Interconnect Lines (Limitation [1.f])

Petitioner fails to show that a POSITA would have been motivated to modify Tessariol’s dummy structures to contact upper-level interconnect lines. KuhnII, ¶¶196-205.

Petitioner appears to recognize that Tessariol does not disclose a “conductive contact” in relation to its dummy structures, and so Petitioner makes a conclusory assertion that because Tessariol’s conductive vias can couple to upper-level interconnects, it would have been obvious that Tessariol’s dummy structures “can” also contact upper-level interconnects. Pet., 90-91. However, whether a POSITA “can” do something is not the proper test for obviousness, and is indicative of improper hindsight. KuhnII, ¶¶197-198; *In re Nuvasive, Inc.*, 842 F.3d 1376, 1384 (Fed. Cir. 2016) (“[T]he question is whether it would have been obvious to [a POSITA] to combine the cited references.”); *Nautilus Hyosung Inc. v. Diebold Self-service Systems division of Diebold*, IPR2016-00633, Pap. 9, *21 **Error! Bookmark**

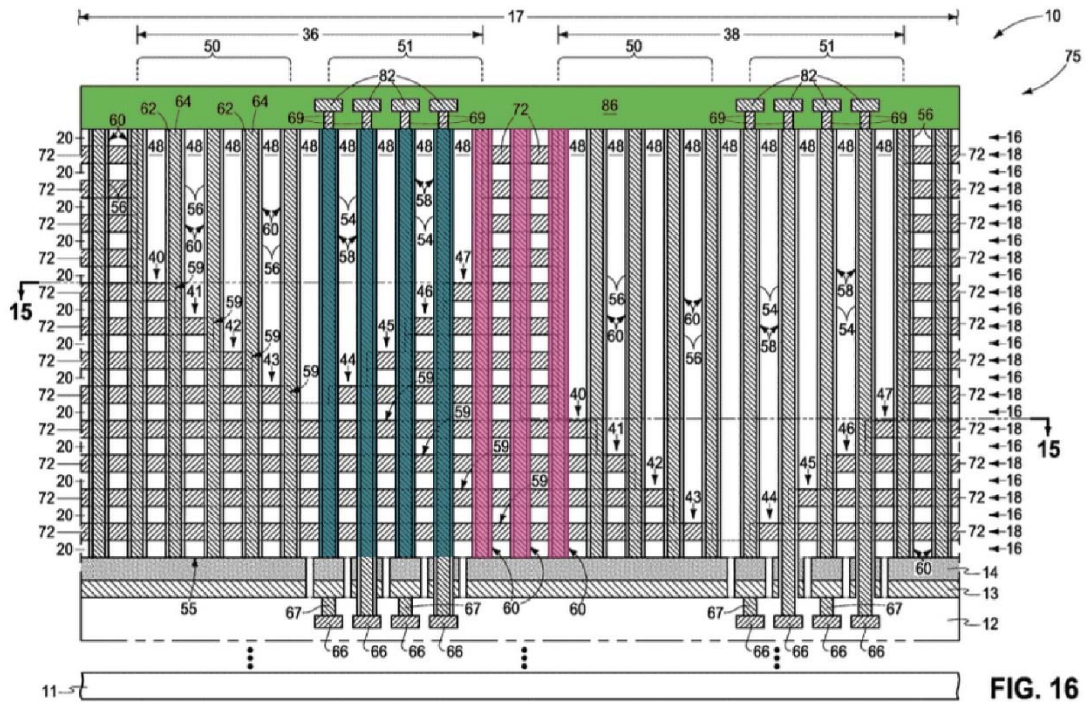
not defined. (“An assertion that something could be done does not articulate a reason why something would be done by one of ordinary skill in the art at the time of the invention and, therefore, raises a specter of impermissible hindsight bias in an obviousness analysis.”).

Regardless, Petitioner has not shown that a POSITA would have been motivated to modify Tessariol’s dummy structures to couple to upper-level interconnects, as alleged. KuhnII, ¶198. Indeed, Petitioner’s own expert concedes that there is no need for such a modification. As Dr. Banerjee explains, unlike the conductive vias, “interconnects 82 are simply not made on the dummy structures, because **there is no need for them to connect to upper-level devices.**” Ex. 1003 ¶216; KuhnII, ¶199. This admission belies his subsequent assertion that “[i]t would therefore have been obvious to a POSITA that dummy source structures 60 can include a contact that could connect to an upper-level interconnect.” Ex. 1003 ¶216. Petitioner has not shown that there would be any functional benefit to adding the proposed connection. KuhnII, ¶¶200-202.

Dr. Banerjee asserts that the proposed modification “reduces time and process steps” (*id.*), but this argument is based on nothing more than conclusory expert testimony. Ex. 1003, ¶¶204, 216; KuhnII, ¶200. Neither Petitioner nor its expert provides any explanation for how this modification would save process steps—because it would not. KuhnII, ¶201.

To the contrary, a POSITA would not have been motivated to modify Tessariol's dummy structures to contact upper-level interconnects because this modification would not eliminate any process steps. Petitioner's only theory is that "dummy structures 60 and operative conductive vias 58 may ... be formed simultaneously" to "save time and process steps," but **Tessariol already discloses that conductive vias 58 and dummy structures 60 are formed "at the same time"** in a process that does **not** include connecting the upper level-interconnects to dummy structures 60. Tessariol, [0038], Fig. 16. KuhnII, ¶201. Thus, this alleged reduction in steps does not result from Petitioner's proposed modification, and would not have motivated the modification. KuhnII, ¶202.

Moreover, as shown below in Figure 16, Petitioner's proposed modification would instead complicate the circuit design, because the additional features would need to be deposited above **dummy source structures 60**, which introduces additional opportunities for manufacturing defects. KuhnII, ¶203.



And the same **insulating material** that covers the **dummy structures 60** without interconnects (see above) would still need to be deposited to fill the areas surrounding any added interconnects. KuhnII, ¶204. So even if it were *possible* to add an interconnect to the dummy structures, Petitioner failed to identify any motivation for a POSITA to add upper-level interconnects to the top of the non-functional dummy structures 60. *Id.*

Thus, Petitioner has not shown that Tessariol discloses or renders obvious that the alleged “dummy source structures” comprise a “conductive contact.” KuhnII, ¶205.

B. Claim 3: Tessariol's Dummy Structures Are Not Nominally Equal Lateral Distance to the Staircase Structure

Petitioner fails to show that Tessariol discloses “at least two of the plurality of dummy source structures are of nominally equal lateral distances to the staircase contact” as required by Claim 3 because Petitioner’s reliance on Tessariol’s Fig. 15 is insufficient to show that the claimed distance-based requirement is satisfied. KuhnII, ¶206. Petitioner points to Tessariol’s Fig. 15 as purporting to show uniform distribution, but Fig. 15 does not include a scale, dimensions, or any other means to measure distances between components. Pet., 93; KuhnII, ¶207. Petitioner does not explain how distances are measured or what (if any) scale is being used to measure the distances in the figure. Pet., 93. KuhnII, ¶208. As discussed for Ground 1 (§VII.C), when the reference does not disclose that the drawings are to scale and is silent as to dimensions, arguments based on measurement of the drawing features are of little value. *See Hockerson-Halberstadt*, 222 F.3d at 956; *see also* MPEP 2125. Therefore, Petitioner cannot rely on Fig. 15 to show distances. KuhnII, ¶208. Petitioner does not even annotate Figure 15 to attempt to show the relative distances, but even if Petitioner had done so, such arguments would be insufficient. Finally, Petitioner does not argue that it would have been obvious to modify Tessariol such that the alleged dummy structures are of nominally equal lateral distances to the alleged staircase contact. KuhnII, ¶209.

Accordingly, Tessariol does not disclose or render obvious Claim 3. KuhnII,

¶210.

C. Claim 4: Tessariol’s Dummy Structures Are Not of Nominally Equal Lateral Distances to the Staircase Contact

For the same reasons explained above for Claim 3, Petitioner’s reliance on Figure 15 is insufficient to show that the plurality of purported dummy source structures are of “nominally equal” lateral distances to the purported staircase contact. *See* §VIII.B. Petitioner merely points to previous sections in the Petition and provides no new illustrations or arguments for this claim. Thus, Tessariol does not disclose or render obvious Claim 4. KuhnII, ¶211.

IX. CONCLUSION

For the reasons above, Petitioner has failed to demonstrate by a preponderance of the evidence that any of the Challenged Claims of the ’872 are anticipated or obvious. Accordingly, the Board should find in favor of Patent Owner and uphold the validity of all Challenged Claims.

Dated: January 17, 2025

Respectfully submitted,

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Memory Technologies Co. Ltd.*

CERTIFICATE OF WORD COUNT

The undersigned certifies that the foregoing PATENT OWNER'S RESPONSE under 37 C.F.R. § 42.120 complies with the type-volume limitation in 37 C.F.R. § 42.24(a)-(c). According to the word-processing system's word count, the brief contains 12,635 words, excluding the parts of the brief exempted by 37 C.F.R. § 42.24(c).

Dated: January 17, 2025

Respectfully submitted,

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CERTIFICATE OF SERVICE

The undersigned certifies that the foregoing PATENT OWNER'S RESPONSE UNDER 37 C.F.R. § 42.120 was served in its entirety by filing through the Patent Trial and Appeal Case Tracking System (P-TACTS), as well as providing a courtesy copy via e-mail to the following attorneys of record for Petitioner listed below:

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