

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,

Petitioner,

v.

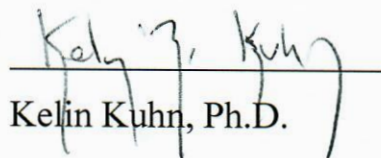
YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,

Patent Owner.

Case IPR2024-00789
Patent 10,861,872

**DECLARATION OF KELIN KUHN, Ph.D. IN SUPPORT OF PATENT
OWNER'S RESPONSE**

Executed this 17th day of January, 2025 in Winthrop, Washington.


Kelin Kuhn, Ph.D.

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I, Kelin Kuhn, Ph.D., hereby declare as follows:

I. INTRODUCTION

1. I have been retained by counsel for Yangtze Memory Technologies Company, LTD (“YMTC”) in the above captioned *inter partes* review of U.S. Patent No. 10,861,872 (Ex. 1001, “’872 patent”). I have been asked to consider the scope and content of the prior art, and respond to certain allegations regarding the prior art, presented by Micron Technology, Inc., (“Petitioner”) in its petition for *inter partes* review of the ’872 patent (“Petition”) and the April 17, 2024 Declaration of Dr. Sanjay Banerjee (Ex. 1003). The arguments raised in Dr. Banerjee’s declaration are similar to those raised in the Petition. Unless otherwise noted, my opinions with respect to the Petition also apply to the corresponding section of Dr. Banerjee’s declaration, and vice-versa. As explained in Sections X-XI (discussing the Grounds raised in the Petition) the invalidity arguments raised in the Petition does not anticipate or render obvious any of the Challenged Claims, and the arguments raised in Dr. Banerjee’s declaration are insufficient for similar reasons.

2. I am being compensated for my time at my usual consulting rate of \$600 per hour, plus reimbursement for any actual expenses. No part of my compensation depends on the content of the opinions that I herein render or on the outcome of this review proceeding. I have no expectation or promise of additional business with

Patent Owner (“PO”) in exchange for the positions explained herein. I do not have any direct financial interest in any of the parties.

3. Unless otherwise noted, the statements made herein are based on my personal knowledge, and if called to testify about this declaration, I could and would do so competently and truthfully.

II. QUALIFICATIONS

4. My qualifications including cases in which I was an expert are stated more fully in my curriculum vitae which has been provided as Appendix A. Here, I provide a brief summary of my qualifications.

5. I received my B.S., magna cum laude, in Electrical Engineering from the University of Washington, Seattle in 1980, and received an M.S. and a Ph.D. in Electrical Engineering from Stanford University in 1985. I undertook post-doctoral work at Stanford from 1985 to 1987.

6. I am presently retired from industry. However, I still periodically engage in engineering projects for select clients and have a small business (Confluence Technology Services) to support that activity.

7. I am also currently an adjunct professor of Materials Science and Engineering at Cornell University, where my research interests are in the areas of quantum materials, post-CMOS technology, and spintronics.

8. For nearly a decade, beginning in 1987, I held faculty positions at the University of Washington, Seattle, beginning as a Research Assistant Professor in Material Science and Engineering, then as Assistant Professor in Electrical and Computer Engineering, and finally as a tenured Associate Professor of Electrical and Computer Engineering. During this period, I worked in III-V molecular beam epitaxy and optoelectronics, and was awarded the University's highest accolade for a faculty member, the Distinguished Teaching Award, in 1995.

9. In 1997, I joined Intel Corporation ("Intel") at the Aloha Campus in Oregon as a Senior Process Engineer. I focused on front-end integration on the Intel 0.35 μ m process technology. In this role, I was responsible for the silicide section of the process flow, interaction with the reliability community, and integration on the CMOS camera chip project.

10. In 1999, I was transferred to Portland Technology Development at Ronler Acres, Oregon, as a Senior Process Engineer. I worked on front-end integration on the 130 nm CMOS generation. In this role, I was responsible for the isolation section of the process flow as well as integration of Optical Proximity Correction technologies into 130 nm.

11. In 2001, I advanced to the title of Principal Engineer. In 2002, I was promoted to the role of Process Program Manager for Intel's 90 nm communications process technology. Over a three-year period, my team developed a derivative

analog/RF technology (including a SiGe bipolar junction transistor (“BJT”)) on top of Intel’s premium 90 nm microprocessor process.

12. In 2004, I advanced to the title of Senior Principal Engineer and was promoted to the role of Device Technology Manager of the pathfinding team at Intel that was responsible for the high-k metal-gate transistor architecture of Intel’s 45 nm microprocessor processor technology. I received an Intel Achievement Award in 2006 for my work on the high-k metal gate.

13. In 2007, I achieved the title of Intel Fellow and became Director of Advanced Device Technology. Fellow is the highest level of technical achievement within Intel, with approximately 50 Fellows among approximately 100,000 total employees. My work evolved to a strategic role in overseeing the transition of advanced device technologies from research into development. In this role, I played an active part in the transfer of transistor technology for the 32 nm node, 22 nm node, and 14 nm node (the last two nodes involving Intel’s FinFET device). I received a second Intel achievement award in 2008 for my work on Intel’s FinFET device.

14. In 2009, my title remained the same, but my role transitioned from development (in Portland Technology Development, at Ronler Acres) to research (in the Components Research Group, still at Ronler Acres). From 2009 until my retirement from Intel in 2014, I researched advanced device architectures for Intel processes in the five-to-ten year time frame.

15. While much of my later work at Intel still remains confidential, certain aspects of my work during this period are featured in my book CMOS And Beyond: Logic Switches for Terascale Integrated Circuits (Co-Editor with Prof. Tsu-Jae King Liu, Cambridge Press, 2015), as well as in my paper “Considerations for Ultimate CMOS Scaling” (IEEE Trans. on Elec. Dev., Vol. 59, No. 7, 2012), winner of the 2013 Paul Rappaport Award.

16. Since my retirement in 2014, my consulting work has included a variety of semiconductor related projects. While the detailed technical content is, of course, protected by client confidentiality, these projects include, FinFETs, vertical power transistors, solar cells, conventional (planar) MOS, and flash.

17. I am the author of more than 100 technical papers in electronics and photonics. I am currently the Associate Editor in Chief (AEiC) of IEEE Electron Device Letters, having served as an editor since 2015, and as AEiC since 2024.

18. A few of my other representative journal publications include: “Understanding the feasibility of scaled III–V TFET for logic by bridging atomistic simulations and experimental results,” (Symposium on VLSI Technology, 2012); “Process Technology Variation,” (IEEE Transactions on Electron Devices, Vol. 58, No. 8, 2011); “A 45 nm logic technology with high-k+metal gate transistors, strained silicon, 9 Cu interconnect layers, 193 nm dry patterning, and 100% Pb-free packaging,” (2007 IEEE International Electron Devices Meeting); and “Comparison

of Junctionless and Conventional Trigate Transistors With Lg Down to 26 nm,” (IEEE Electron Device Letters, Vol. 32, No. 9, 2011).

19. A few representative book chapters include, “The Magic of MOSFET Manufacturing,” Chapter in the 75th Anniversary of the Transistor, Wiley-IEEE Press, July 2023, ISBN: 978-1-394-20247-8. Chapter 1, CMOS and Beyond CMOS: Scaling Challenges” (Book title: “High Mobility Materials for CMOS Applications”, Woodhead Publishing Series in Electronic and Optical Materials, Elsevier, June 2018, ISBN 9780081020616).

20. I am an inventor on approximately 80 granted U.S. patents in the field of semiconductor technology.

21. A few of my other relevant honors include being a Fellow at the Institute of Electrical and Electronics Engineers (“IEEE”), a recipient of the IEEE Frederik Philips Award (2016), a recipient of the IEEE Paul Rappaport Award (2013), the recipient of eleven Intel Divisional Awards, and election to the National Academy of Engineering (2023). Earlier in my career, I received the NSF Presidential Young Investigator Award.

22. As specifically relevant to this project, I want to highlight the 3’D gate-last vertical gate-all-around (GAA) devices and the 3’D vertical GAA arrays that are discussed at some length in “Considerations for Ultimate CMOS Scaling” (see Fig. 15 in particular). I also want to highlight on-going proprietary and confidential

work, in the matter of Silicon Storage Technology, Inc. vs. Taiwan Semiconductor Manufacturing Company involving flash.

23. Attached as Exhibit 1 to this report is a current copy of my curriculum vitae, which outlines my academic, professional and experiential qualifications in the semiconductor and integrated circuit industries, as well as a list of publications I have authored and co-authored and presentations I have given.

III. MY ASSIGNMENT AND BASES OF OPINIONS

24. I have been asked to provide my opinions as to the scope and content of the '872 patent as well as the prior art presented by Petitioner and Dr. Banerjee in the Petition. Specifically, I have been asked to opine on what a person of ordinary skill in the art would have understood the '872 patent to disclose, and I have been asked to provide my opinions concerning whether Park (Ex. 1005) or Tessariol (Ex. 1006) discloses or renders obvious claims 1-6 and 11-13 of the '872 patent.

25. In the course of conducting my analysis and forming my opinions, I have reviewed the references and materials cited in the Petition, the Preliminary Response, Preliminary Reply, Preliminary Sur-Reply, and herein including those listed below:

Exhibit No.	Reference
N/A	Petition for <i>Inter Partes</i> Review of U.S. Patent No. 10,861,872 (IPR2024-00789, Paper 1)
Ex. 1001	U.S. Patent No. 10,861,872 B2 to Liu et al.
Ex. 1002	File History of U.S. Patent No. 10,861,872 B2 to Liu et al.
Ex. 1003	Declaration of Dr. Sanjay Banerjee ("Banerjee")

Ex. 1004	Curriculum Vitae of Dr. Sanjay Banerjee
Ex. 1005	U.S. Patent No. 9,859,297 B2 to Park et al. (“Park”)
Ex. 1006	U.S. Patent Publ. No. 2019/0081061 A1 to Tessariol et al. (“Tessariol”)
Ex. 1007	Aritome, “NAND Flash Memory Technologies” (2016)
Ex. 1008	Silvagni, “3D NAND Flash Based on Planar Cells,” Computers 2017
Ex. 1009	Michelsoni et al., “Inside Solid State Drives (SSDs)” (2nd Ed. 2018)
Ex. 1010	U.S. Patent No. 10,381,369 B2 to Kim et al.
Ex. 1011	U.S. Patent No. 10,475,737 B2 to Tang et al.
Ex. 1012	Certified English Translation of Chinese Patent Application Publ. No. CN108766971 to Liu (“Liu”)
Ex. 1013	Chinese Patent Application Publ. No. CN108766971 to Liu
Ex. 1014	U.S. Patent No. 8,945,996 B2 to Tang et al.
Ex. 1015	YMTC’s Exemplary Infringement Claim Chart for U.S. Patent No. 10,861,872 – (Ex. 49) 128L [PROTECTIVE ORDER MATERIAL – FILED UNDER SEAL]
Ex. 1016	YMTC’s Exemplary Infringement Claim Chart for U.S. Patent No. 10,861,872 – (Ex. 50) 176L [PROTECTIVE ORDER MATERIAL – FILED UNDER SEAL]
Ex. 1017	YMTC’s Exemplary Infringement Claim Chart for U.S. Patent No. 10,861,872 – (Ex. 51) 232L [PROTECTIVE ORDER MATERIAL – FILED UNDER SEAL]
Ex. 1018	Print out from Geographic Wiki, https://www.studycountry.com/wiki/what-is-a-piece-of-landsurrounded-by-water-on-2-side (last visited Mar. 28, 2024)
Ex. 1019	U.S. Patent No. 9,530,492 to Lee
Ex. 1023	Michelsoni, “3D Flash Memories” (2016)
Ex. 1033	Plaintiff and Counterclaim Defendant Yangtze Memory Technologies Company, Ltd.’s Disclosure of Asserted Claims and Infringement Contentions, dated May 6, 2024, in Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC, Case No. 3:23-cv-05792-RFL
N/A	Patent Owner’s Preliminary Response (IPR2024-00789, Paper 11)
N/A	Petitioner’s Preliminary Reply (IPR2024-00789, Paper 13)
N/A	Patent Owner’s Preliminary Sur-Reply (IPR2024-00789, Paper 14)
Ex. 2003	Shur, “Introduction to Electronic Devices” (1996) (“Shur”)

Ex. 2004	Streetman, “Solid State Electronic Devices” (1995) (“Streetman”)
Ex. 2005	US Patent No. 8,766,336 (“Grupp”)
Ex. 2008	Deposition Transcript of Dr. Banerjee
Ex. 2009	<i>Contact</i> , New Oxford American Dictionary, Third Edition, 2010
Ex. 2010	<i>Contact</i> , Wiley Electrical and Electronics Engineering Dictionary, 2004
Ex. 2011	<i>Electric Contact</i> , McGraw-Hill Dictionary of Scientific and Technical Terms, Sixth Edition, 2002
Ex. 2012	Micron’s Preliminary Claim Constructions (District Court)
Ex. 2013	Plaintiff’s Proposed Claim Constructions (District Court)
N/A	Decision Granting Institution of <i>Inter Partes Review</i> of U.S. Patent No. 10,861,872 (IPR2024-00789, Paper 15)

26. My opinions in this declaration are based on my review of these documents, as well as upon my education, training, research, knowledge, and experience.

27. All emphases (such as bolding, underlying, or italics) appearing in quotations and citations cited herein have been added by me, unless otherwise stated.

IV. SUMMARY OF MY OPINIONS

28. It is my opinion that Park does not disclose or render obvious claims 1-6 and 11-13 of the ’872 patent at least because:

- Park does not disclose or render obvious “dummy source structures” that are “surrounding the staircase contact” as required by independent claim 1 (from which the remaining Challenged Claims depend).

- Park does not disclose or render obvious “dummy source structures” that are adjacent to a “staircase contact,” as required by claim 2.
- Park does not disclose or render obvious that the “at least two of the plurality of dummy source structures are of nominally equal lateral distances to the staircase contact,” as required by claim 3.
- Park does not disclose or render obvious a “plurality of dummy source structures” that are of equal lateral distances to the staircase contact, as required by claim 4.
- Park does not disclose or render obvious “dummy source structures” that are “are arranged in a first row that extends along a first lateral direction,” as required by claim 5.
- Park does not disclose or render obvious “dummy source structures” that are arranged “in a second row that extends along a second lateral direction perpendicular to the first lateral direction,” as required by claim 6.
- Park does not disclose or render obvious that a “dummy source structure” is located between “first and second staircase contacts,” as required by claim 11.

- Park does not disclose or render obvious that “at least two dummy source structures are located between the first and second staircase contacts.” as required by claim 12.
- Park does not disclose or render obvious that “the conductive contact comprises a conductor layer, and wherein the at least one dummy source structure further comprises a spacer surrounding the conductor layer along a sidewall of the conductor layer, the spacer comprising a dielectric material,” as required by claim 13.

29. It is my opinion that Tessariol does not disclose or render obvious claims 1-6 and 11-13 of the '872 patent at least because:

- Tessariol does not disclose or render obvious “dummy source structures” that are “surrounding the staircase contact” and comprise a “conductive contact” as required by independent claim 1 (from which the remaining Challenged Claims depend).
- Tessariol does not disclose or render obvious “dummy source structures” that are adjacent to a “staircase contact,” as required by claim 2.

- Tessariol does not disclose or render obvious that “at least two of the plurality of dummy source structures are of nominally equal lateral distances to the staircase contact,” as required by claim 3.
- Tessariol does not disclose or render obvious a “plurality of dummy source structures” that are of equal lateral distances to the staircase contact, as required by claim 4.
- Tessariol does not disclose or render obvious “dummy source structures” that are “are arranged in a first row that extends along a first lateral direction,” as required by claim 5.
- Tessariol does not disclose or render obvious “dummy source structures” that are arranged “in a second row that extends along a second lateral direction perpendicular to the first lateral direction,” as required by claim 6.
- Tessariol does not disclose or render obvious “dummy source structure” that is located between “first and second staircase contacts,” as required by claim 11.
- Tessariol does not disclose or render obvious that “at least two dummy source structures are located between the first and second staircase contacts.” as required by claim 12.

- Tessariol does not disclose or render obvious that “the conductive contact comprises a conductor layer, and wherein the at least one dummy source structure further comprises a spacer surrounding the conductor layer along a sidewall of the conductor layer, the spacer comprising a dielectric material,” as required by claim 13.

V. APPLICABLE LEGAL STANDARDS

30. I am not a legal expert and offer no opinions on the law. However, I have been informed by counsel of the various legal standards that apply, and I have applied those standards in arriving at my conclusions.

A. Claim Construction

31. I was informed, unless otherwise noted, I should give claim terms their ordinary and customary meaning as understood by a person of skill in the art at the time of the invention. I was informed and I understand that the words of the patent’s claims and the context in which the term is used in the claims can be highly instructive in ascertaining the term’s meaning. I further understand that the terms of a claim are to be interpreted in the context of the entire patent, including the patent’s other claims, its specification and its figures.

32. I have been further instructed that a patent’s “prosecution history” may often provide helpful evidence about how the Patent Office and the applicant understood the patent and its claims. Therefore, I have been instructed that claim

terms should also be interpreted in light of the patent's prosecution history. In addition to the claims, the specification, the figures, and the prosecution history, I have been instructed that certain "extrinsic evidence" such as scientific or technical references may also help inform the way in which the person of ordinary skill in the art might understand the claim term. I have been instructed that extrinsic evidence must always be considered in the context of the intrinsic evidence.

B. Anticipation

33. I have been informed by counsel that a patent claim is invalid as anticipated if each element of that claim is present either explicitly or inherently in a single prior art reference. I have also been informed that, to be an inherent disclosure, the prior art reference must necessarily disclose the limitation, and the fact that the reference might possibly practice or possibly contain a claimed limitation is insufficient to establish that the reference inherently teaches the limitation.

C. Obviousness

34. I understand that a claim is unpatentable if it would have been obvious to a person of ordinary skill in the art at the time the invention was made. I understand that a claim could have been obvious from a single prior art reference or from a combination of two or more prior art references. I understand that an obviousness analysis requires an understanding of the scope and content of the prior

art, any differences between the invention and the prior art, and the level of ordinary skill in evaluating the pertinent art.

35. I further understand that a claim would have been obvious if it unites old elements with no change to their respective functions or alters prior art by mere substitution of one element for another known in the field, and that combination yields predictable results. Also, I understand that obviousness does not require physical combination or bodily incorporation, but rather consideration of what the combined teachings would have suggested to persons of ordinary skill in the art at the time of the invention.

36. While it may be helpful to identify a reason for this combination, I understand that there is no rigid requirement of finding an express teaching, suggestion, or motivation to combine within the references. When a product is available, design incentives and other market forces can prompt variations of it, either in the same field or a different one. If a person of ordinary skill in the art can implement a predictable variation, obviousness likely bars its patentability. For the same reason, if a technique has been used to improve one device and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique would have been obvious. I understand that a claim would have been obvious if a person of ordinary skill in the art would have had

reason to combine multiple prior art references or add missing features to reproduce the invention recited in the claims.

37. I further understand that certain factors may support or rebut the obviousness of a claim. I understand that such secondary considerations include, among other things, commercial success of the patented invention, skepticism of those having ordinary skill in the art at the time of invention, unexpected results of the invention, any long-felt but unsolved need in the art that was satisfied by the invention, the failure of others to make the invention, praise of the invention by those having ordinary skill in the art, and copying of the invention by others in the field. I understand that there must be a nexus, that is, a connection, between any such secondary considerations and the invention.

38. I understand that in considering obviousness, it is important not to determine obviousness using the benefit of hindsight derived from the patent being considered.

D. Claim Dependency

39. I understand that a patent may include two types of claims, independent claims and dependent claims. An independent claim stands alone and includes only the limitations it recites. A dependent claim can depend from an independent claim or another dependent claim. I understand that a dependent claim includes all the

limitations that it recites in addition to all of the limitations recited in the claim from which it depends.

VI. THE '872 PATENT

A. Overview of the '872 Patent

40. The claimed invention of the '872 is directed to “an improved 3D [three-dimensional] memory structure scheme” that improves device performance by mitigating problems arising from device fabrication processes. Ex. 1001, 4:64-65, 5:22-33. Compared to planar memory structures, 3D memory structures increase storage density by stacking memory cells vertically and are used in a variety of applications such as consumer electronics and storage devices. As the '872 explains, “3D memory architecture[s] can address the density limitation in planar memory cells.” '872, 1:5-6. The '872 is specifically directed to improving a semiconductor fabrication technique for 3D memory structures. Ex. 1001, 1:15-18, 4:30-33.

41. As 3D memory devices are “scaled to smaller sizes,” fabrication becomes more challenging. Ex. 1001, 1:18-22, 4:37-38. One such fabrication challenge arises when certain device openings, called gate line slits (“GLS”), are used to deposit conductive material into trenches (or “lateral recesses”)—that extend laterally in the memory array of the device—to form gate lines (gate electrodes) for transmitting signals to activate memory cells. Ex. 1001, 4:44-49, 5:17-20. The GLS, as depicted in the color-annotated version of the '872's Fig. 5 below, has “a

dimension along the extending direction (or the x-direction) much greater than the dimension along the expanding dimension (or the y-direction)).” Ex. 1001, 5:22-30. As a result of this shape, formation of the GLS “can contribute to unbalanced variations of wafer flatness (e.g., wafer warpage bias) in different directions,” which “can have an adverse impact on the photolithography process to form device patterns, leading to potential die yield loss.” *Id.*

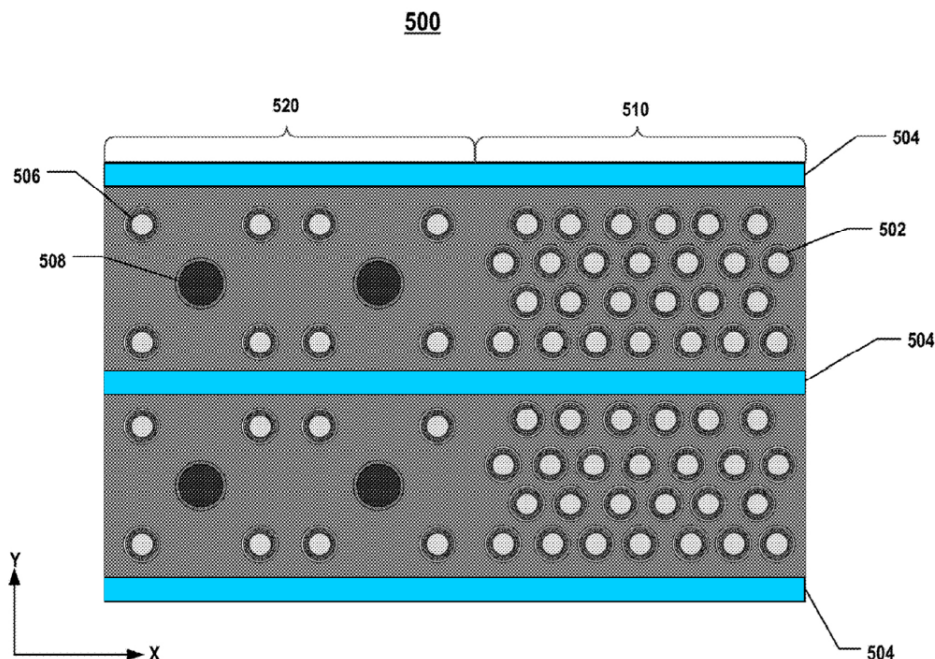


FIG. 5

42. The '872 solves this issue, for example, by introducing “a plurality of dummy source structures,” each of which “extend[s] vertically” through a staircase structure—a memory stack of multiple stairs where each stair has alternating layers of dielectric and conductor materials—on “one side of the memory stack.” Ex. 1001,

1:39-42, 5:31-36. That is, the claimed invention of the '872 allows for “removing GLSs from the staircase region” altogether and replacing them with dummy source structures that mitigate the aforementioned issues. Ex. 1001, 8:22-23. As part of this replacement process, dummy source holes, which later become the dummy source structures, can be used as access points to form gate lines instead of the gate line slits. Ex. 1001, 15:16-48. The dummy source structures can be “arranged in a pattern” such that, when used as access points for forming gate lines, the gate lines are formed with “improved uniformity and quality.” Ex. 1001, 4:43-52. The specific arrangement of the dummy source structures, as taught by the '872, is advantageous because it allows the deposited conductive material to travel “shorter distances to fill up the lateral recesses,” thus allowing the gate lines to be “less susceptible to voids or density nonuniformity.” Ex. 1001, 4:52-58.

43. An exemplary arrangement of dummy source structures is depicted in the plan view in the color-annotated version of the '872's Fig. 1A, below. The dummy source structures are “arranged in a pattern,” meaning in an arrangement that is “repeated at a regular interval.” Ex. 1001, 7:61-8:1. The '872 further teaches that the dummy source structures “surround staircase contacts 122 of nominally same lateral distances to the respective staircase contacts 122” so that, as one example, the depositing “conductive material for forming the gate electrodes may travel nominally same distances to surrounding lateral recesses” to fill the lateral

recesses. Ex. 1001, 8:25-34, 8:45-49. This “facilitat[es]” the fabrication process such that the gate electrodes are formed “with improved uniformity and quality” and “warpage bias” of the memory device is reduced. Ex. 1001, 8:25-34., 8:45-49. The ’872 emphasizes that the “symmetrical architecture” of dummy source structures is advantageous because it “can improve the performance and efficiency of etching processes,” which are additional processes in fabricating the memory device. Ex. 8:49-51. The ’872 further teaches that the dummy source structures are “located adjacent to staircase contact 122,” meaning there are “no other components such as dummy channel structures, dummy source structures, and staircase contacts” between staircase contact 122 and each of the dummy source structures. Ex. 1001, 6:41-46. In the figure below, the red circles 122 are the staircase contacts that are surrounded by orange dummy source structures 126.

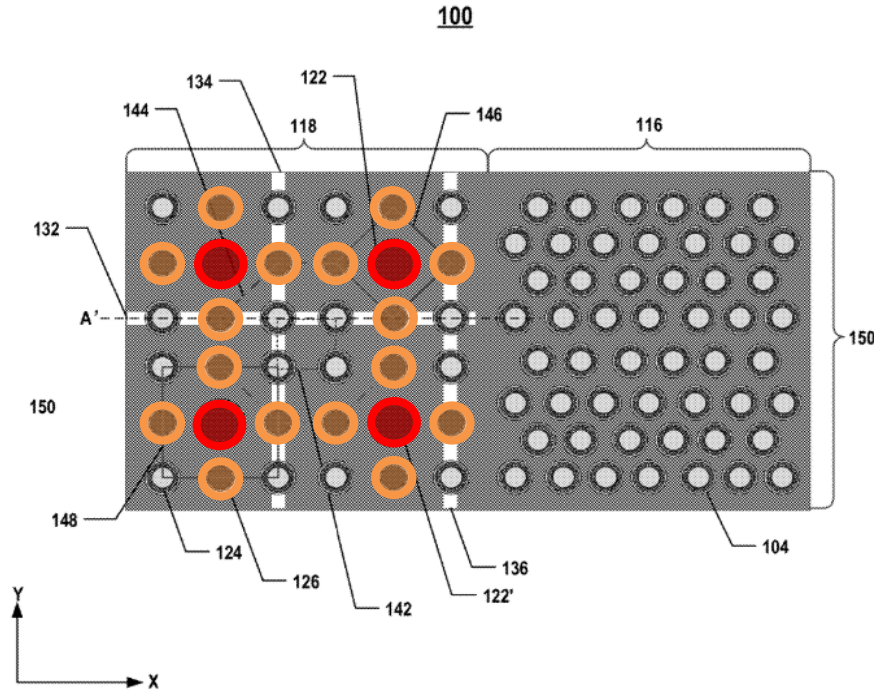


FIG. 1A

44. Other exemplary images of the dummy source structure arrangement entail arranging the dummy source structures symmetrically around staircase contacts 122, such that each structure is nominally the same lateral distance to the respective staircase contacts 122. Additionally, in each of the embodiments of the '872, each of the dummy source structures is located adjacent to a staircase contact 122, such that there are no other components located between. These arrangements are depicted in Figs. 1B-1C, below. The '872 does not include any illustrations of the dummy source structure arrangement in plan view other than those depicted in Figs. 1A-1C.

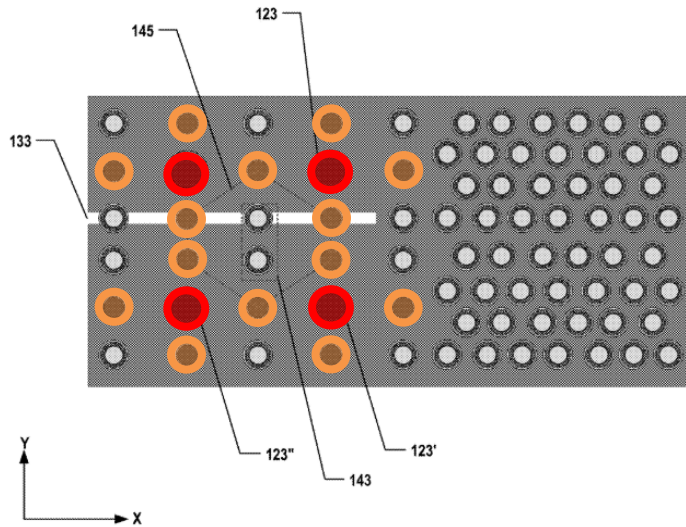


FIG. 1B

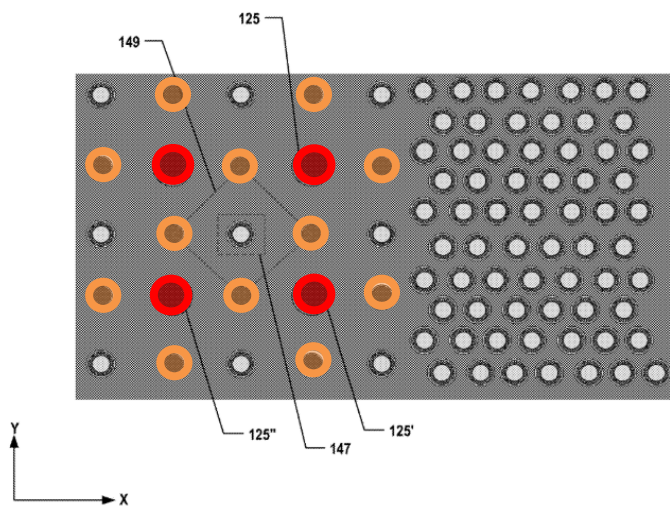


FIG. 1C

45. The memory device of the '872 includes: (1) substrate with “two lateral surfaces extending laterally in the x-y plane” (Ex. 1001, 9:3-5); (2) “memory stack 160” that includes “interleaved conductive layers 106 and dielectric layers 108” and “a staircase structure 175” on “[a]t least [] one side in the lateral direction” (Ex. 1001, 9:67-10:3); (3) “dummy source structure 178” that includes “a dummy source hole

filled with conductive materials as a contact 179”; and (4) a “spacer 177 made of any suitable dielectric materials (e.g., silicon oxide) between contact 179 and memory stack 160 to electrically separate surrounding conductive layers 106 in memory stack 160 from contact 179” (Ex. 1001, 11:39-43). A cross-section view of the memory device, depicting the dummy source structure, is below.

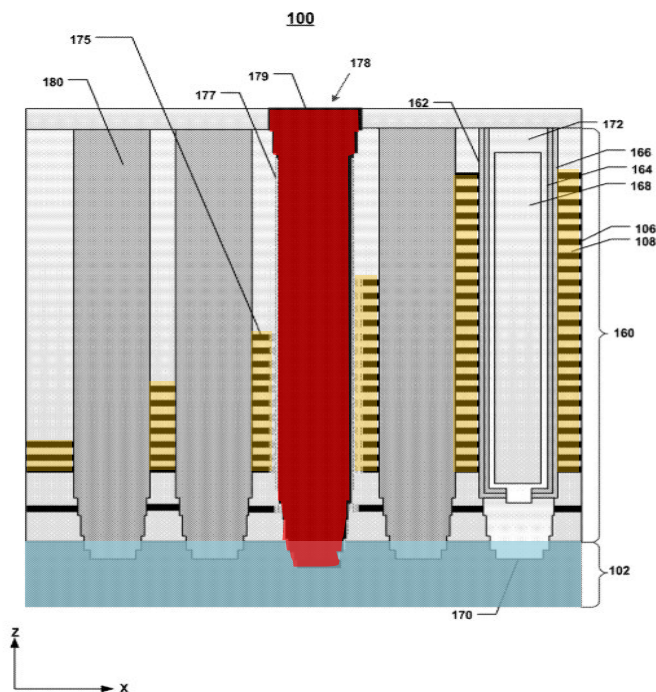


FIG. 1D

B. Listing of the Challenged Claims

46. For reference, claims 1-6 and 11-13 (“Challenged Claims”) of the ’872 Patent are reproduced below:

[1.pre] A three-dimensional (3D) memory device, comprising:

[1.a] a substrate;

[1.b] a memory stack comprising interleaved conductive layers and

dielectric layers on the substrate;

[1.c] a staircase structure on one side of the memory stack;

[1.d] a staircase contact in the staircase structure; and

[1.e] a plurality of dummy source structures each extending vertically through the staircase structure, the plurality of dummy source structures surrounding the staircase contact,

[1.f] wherein each of the dummy source structures comprises a conductive contact.

[2] The 3D memory device of claim 1, wherein the plurality of dummy source structures are located adjacent to the staircase contact.

[3] The 3D memory device of claim 1, wherein at least two of the plurality of dummy source structures are of nominally equal lateral distances to the staircase contact.

[4] The 3D memory device of claim 1, wherein the plurality of dummy source structures are of nominally equal lateral distances to the staircase contact.

[5] The 3D memory device of claim 1, wherein in a plan view, at least two of the plurality of dummy source structures are arranged in a first row that extends along a first lateral direction.

[6] The 3D memory device of claim 5, wherein in the plan view, at least two other dummy source structures are arranged in a second row that extends along a second lateral direction perpendicular to the first lateral direction.

[11] The 3D memory device of claim 1, comprising first and second staircase contacts, wherein at least one dummy source structure is located between the first and second staircase contacts.

[12] The 3D memory device of claim 1, wherein at least two dummy source structures are located between the first and second staircase contacts.

[13] The 3D memory device of claim 1, wherein the conductive contact comprises a conductor layer, and wherein the at least one dummy source

structure further comprises a spacer surrounding the conductor layer along a sidewall of the conductor layer, the spacer comprising a dielectric material.

C. File History

47. The '872 was filed on May 2, 2019. During the pendency of the '872 patent application, Applicant was required to restrict the invention to that of a “three-dimensional (3D) memory device” or “a method for forming” the same. Ex. 1002 (Part 1 of 2), 458 (5/21/2020 Requirement for Restriction/Elections). Applicant elected claims that restricted the invention of the '872 to that of a “three-dimensional (3D) memory device.” Ex. 1002 (Part 1 of 2), 466 (5/22/2020 Applicant Arguments/Remarks Made in an Amendment).

48. The Examiner then rejected the pending claims under 35 U.S.C. § 102(a)(1) as being allegedly anticipated by and under 35 U.S.C. § 103 as being allegedly obvious over U.S. Pub. No. 2016/0293622 (“Jeong”). Ex. 1002 (Part 1 of 2), 468-78 (6/11/2020 Office Action). In supporting this assertion, the Examiner mapped the '872's claimed “plurality of dummy source structures” to Jeong's “dummy pillars” because “like the dummy source of the instant application, [they] function as a mechanical support for conductive layers” of a memory stack. Ex. 1002 (Part 1 of 2), 470, 474, 476-77 (6/11/2020 Office Action). During a telephonic Applicant-initiated interview, Applicant discussed with the Examiner the distinction between the claimed “dummy source” and the “dummy pillar” of Jeong. Ex. 1002 (Part 1 of 2), 505 (8/14/2020 Applicant-Initiated Interview Summary, Office Action

Appendix). Based on these discussions, Applicant subsequently filed an amendment to the claims, further limiting the independent claims to recite, “wherein each of the dummy source structures comprises a conductive contact.” Ex. 1002 (Part 2 of 2), 510, 513 (8/18/2020 Request for Reconsideration After Non-Final Rejection). Applicant stated that the “dummy pillars in Jeong are different from the claimed ‘dummy source structure’ in amended independent claims 1 and 8 at least because the dummy pillars do not include conductive contacts,” explaining:

Nothing in Jeong’s pillar is conductive contact, as the pillar consists of insulating layers, a semiconductor pattern, and a charge storage layer. By contrast, as explained at paragraph [0057] of the present application: ‘In some embodiments, dummy source structure 178 includes a dummy source hole filled with conductive materials as a contact 179. Dummy source structure 178 can further include a spacer 177 made of any suitable dielectric materials (e.g., silicon oxide) between contact 179 and memory stack 160 to electrically separate surrounding conductive layers 106 in memory stack 160 from contact 179. As a result, dummy source structures 178 can laterally separate 3D memory device 100 into multiple memory regions, such as memory blocks.’

Id., 514-15.

49. The Applicant reiterated that the claimed “dummy source structure” includes “a contact” made of “conductive materials,” and that Jeong’s structure

made solely of “insulating layers,” a layer containing a “semiconductor pattern,” and a “charge storage layer” did not meet this criterion. *Id.* In making this argument, the Applicant cited to a section of the specification that additionally states that the claimed “dummy source structure” can function to “laterally separate” the three-dimensional memory device into “multiple memory regions” to the extent that the “dummy source structure” includes “a spacer [] made of any suitable dielectric materials,” such as “silicon oxide,” situated “between contact 179 and memory stack 160.” *Id.* Neither the spacer nor the functionality of laterally separating the memory device into regions of memory is recited in any of the independent claims of the ’872. As such, these features were not necessary to overcome the prior art of record.

50. The Examiner subsequently allowed all pending claims and did so after reviewing four additional prior art references identified by the Applicant in a later-submitted Information Disclosure Statement. Ex. 1002 (Part 2 of 2), 1-6 (10/26/2020 Notice of Allowance), Ex. 1002 (Part 2 of 2) 1-2 (10/30/2020 Information Disclosure Statement), Ex. 1002 (Part 2 of 2), 236-37 (11/9/2020 Notice of Allowance) (“The reasons for allowance have not changed since the previous Office Action (Notice of Allowance, mailed on 10/26/2020).”). The Examiner stated in the Reasons for Allowance that the prior art of record does not teach or render obvious the limitation “wherein each of the dummy source structures comprises a

conductive contact.” Ex. 1002 (Part 2 of 2), 7 (10/26/2020 Notice of Allowance) (emphasis in the original).

51. The Examiner further stated, “the individual limitations may be found in a plurality of prior arts but there is no motivation to combine,” and “[b]ecause no reference alone teaches all the limitations, nor is there any motivation to combine the prior arts to construct all the limitations of” independent pending claims 1 and 8, the independent claims are “deemed patentable over the prior arts.” *Id.*, 7-10. The ’872 issued on December 8, 2020 with twenty claims. Ex. 1002 (Part 2 of 2), 272 (Issue Notification).

VII. LEVEL OF ORDINARY SKILL IN THE ART

52. My opinions in this declaration are based on the understandings of a person of ordinary skill in the art, which I understand is sometimes referred to as an “ordinary artisan” or by the acronyms “POSITA” (person of ordinary skill in the art) or “POSA,” as of the time of the invention.

53. I have been asked to consider the level of ordinary skill that someone in the field of technology of the ’872 patent would have had at the time the claimed invention disclosed in the ’872 patent was made. In determining the level of ordinary skill in the art, I considered the following: (1) the levels of education and experience of persons working in the field; (2) the types of problems encountered in the field; and (3) the sophistication of the technology.

54. In my opinion, a person of ordinary skill in the art capable of reading and understanding the claims of the '872 patent at the time of the invention would have had at least a bachelor's degree in electrical engineering, computer engineering, or a similar discipline, along with at least 2 years of professional experience with semiconductor memory devices, or an equivalent level of knowledge and experience. For example, an advanced degree may replace some of the professional experience, or extensive experience may replace some of the educational requirements.

55. In this case, Dr. Banerjee has asserted in his declaration that a person of ordinary skill in the art at the time of the invention described in the '872 patent would have a:

a bachelor of science degree in electrical engineering or a similar discipline, along with 2-3 years of professional experience working with (*e.g.*, researching, designing, or teaching) monolithic 3D structures and NAND memory devices, or an equivalent level of skill, knowledge, and experience (*e.g.*, an advanced degree may replace some of the professional experience). This POSITA would have been aware of and generally knowledgeable about 3D NAND's structure, its component parts, how it operates, and how it is controlled.

Banerjee, ¶42.

56. In view of my educational background and years of experience, including my many years of experience developing and manufacturing MOS transistors, 3D MOS transistors, monolithic 3D gate-all-around transistors, and memory devices, I both met and exceeded the qualifications of a person of ordinary skill in the art as of the earliest possible priority date of the '872 Patent in February

2019. That is true under both my own definition of a person of ordinary skill in the art, as well as under Dr. Banerjee’s definition, and my opinions as set forth herein are the same regardless of which definition of a person of ordinary skill in the art is applied.

VIII. CLAIM CONSTRUCTION FOR THE ’872 PATENT

57. I have been asked to opine on the scope and content of the ’872 patent and what a person of ordinary skill in the art would have understood the ’872 patent to disclose and teach as it relates to the terms “dummy source structures,” “surrounding,” and “conductive contact.”

A. “Dummy Source Structure” (Claims 1-6, 11-13)

58. The term “dummy source structure” should be construed according to its plain and ordinary meaning as a structure that does not function as a source to memory cells. Petitioner’s proposal that the term be construed as a “structure[s] that occupies the void that was used for the gate replacement process,” disregards the word “dummy” by not differentiating between “dummy” source structures and non-dummy source structures.¹

¹ In my July 29, 2024 declaration submitted with the Patent Owner Preliminary Response, there is a typo that mistakenly refers to Petitioner’s proposed construction of “dummy source structure” as Patent Owner’s proposed construction.

**(a) The Term “Dummy Source Structure” as Used in the
’872 Patent**

59. “Dummy source structure” should be construed as a structure that does not function as a source to memory cells based on the disclosures of the ’872 patent and the plain and ordinary meaning of the term.

60. This construction gives proper meaning to the word “dummy” because the claim term is “dummy source structure” rather than “source structure.”

61. The ’872 patent discloses that the dummy source structures do not function as a source to the memory cells. The ’872 patent discloses that the “dummy source structures” function as “a mechanical supporting structure.” Ex. 1001, 16:38-44. And while the dummy source structures may function as “interconnects to connect 3D memory device 100 with other peripheral devices,” the ’872 patent does not describe the dummy source structure functioning as a source to the memory cells. *See, e.g.,* ’872, 5:40-43, 11:46-49.

62. The ’872 patent discloses that the dummy source hole is filled with “dielectric materials, conductive materials, or any combination thereof” so that a “dummy source structure 246 including spacer 242 and contact 244 is thereby formed in the dummy source hole.” Ex. 1001, 16:28-31, 16:56-63. The specification continues that “when conductive materials are used to fill dummy source hole 212 (e.g., contact 244), the dummy source structure 246 may function as an interconnect to connect 3D memory device 100 with other peripheral devices,” and “[w]hen

dielectric materials are used to fill dummy source hole 212, dummy source structure 246 may function as a mechanical support structure to improve the stability of the staircase region.” Ex. 1001, 16:63-17:3.

63. The specification does not suggest that a dummy source structure can function as a source to the memory cells, as that functionality would contradict the label “dummy source structure.” As such, “dummy source structure” should be construed as a structure that does not function as a source to the memory cells.

64. I disagree with Petitioner’s suggestion that “[t]here is no dispute that the ‘dummy source structure’ may not be a ‘dummy.’” Prelim. Reply 5. The ’872 patent does not teach dummy source structures functioning as actual source structures, just that the dummy source structures can function as interconnects. ’872, 16:66-17:3.

65. Additionally, the term “source” cannot mean “source for deposition materials” (as opposed to a source to gates of memory cells), as suggested by Petitioner. Based on my review, there are no examples in the intrinsic record where the term “source” means “source for deposition materials.” Instead, “source” is used consistently with its meaning in relation to semiconductor device operation, namely as the “source” for charge for the transistors forming the memory cells. See, e.g., ’872, 16:33-38, 11:8-9.

66. Dummy source structures do not function as a source to memory cells.

I understand that Petitioner relies on the following passage to argue otherwise, but the passage never says that a “dummy” source structure is the same as a “source structure”: “In some embodiments, dummy source structure 246 may not connect to channel structures in the inner region.” Prelim. Reply 2 (citing ’872, 16:38-40). Even if the use of the permissive “may” language in the ’872 suggests embodiments of a dummy source structure may or “may not connect to channel structures,” neither disclosure suggests that dummy source structures “function as a source to the memory cells.”

67. It is also incorrect to equate “connect[ion] to channel structures” to functioning as a source. Whether a dummy source structure “connect[s] to channel structures” does not disclose that the dummy source structure provides a “source to the memory cells” (i.e., connects the memory cells to source power). For example, while one end of the dummy source structure may connect to channel structures via the substrate (or the source plane), the other end of the dummy source structure may be an electrical dead end or may connect to peripheral devices. Regardless, the dummy source structure is not the common source line, nor is it an extension of the common source line.

68. There is no teaching in the ’872 patent that the dummy source structure provides a source to the memory cells and thus the construction excluding such

functionality is consistent with all disclosed embodiments. Petitioner misunderstands the '872's teaching that dummy source structures “may function as an interconnect” and “extend into the substrate.” *See* Prelim. Reply 4 (citing '872, Claim 1, 16:66-17:3). The '872 explains that “the dummy source structure 246 may function as an interconnect to connect 3D memory device 100 with other peripheral devices”—not as an interconnect to a supply that provides a source to the memory cells. '872, 16:66-17:3.

69. As explained above, construing “dummy source structure” as a structure that does not function as a source to memory cells is consistent with the plain meaning of “dummy source structure” as well as the disclosure of the '872 patent, and provides meaning to the term “dummy,” while Petitioner’s construction does not.

(b) Petitioner’s Proposed Construction Does Not Give Meaning to “Dummy” Source Structure, and Limits the Term to a Process of Manufacture

70. Petitioner’s proposal that “dummy source structure” should be construed as a “structure that occupies the void that was used for the gate replacement process” does not give meaning to the word “dummy” and wrongly adds in a requirement that this must be made as part of a gate replacement process.

71. Petitioner’s proposed construction disregards the plain meaning of the term and does not differentiate between dummy source structures and non-dummy

source structures (i.e., actual source structures that function as the source for memory cells).

72. Structures that occupy, or are formed from, voids used for gate replacement processes can be either dummy source structures—if they do not function as a source for the memory cells—or source structures if they do function as a source for the memory cells. Petitioner’s construction does not account for the distinction between the two types of structures and their functions.

73. A dummy source structure is a type of dummy structure that is used for the purposes of improving integrated circuit functionality and manufacturing yield. While dummy source structures can mimic the physical properties of non-dummy source structures, they do not function as the source. In contrast the primary function of its non-dummy counterpart is to function as a source.

74. Dummy structures can, instead, serve as load-bearing structures during semiconductor device fabrication, which reduces mechanical stress on non-dummy structures during fabrication. ’872, 5:5:21-48. For instance, while dummy source structures may be comprised of conductive material and thus may function, e.g., as an “interconnect between the 3D memory device and peripheral devices” (’872, 5:37-43), they do not function as the source for memory cells. Petitioner’s proposed construction ignores this difference and does not distinguish between dummy and non-dummy source structures.

75. Petitioner's proposed construction also wrongly adds in a limitation regarding the process by which the apparatus is made.

76. The Petition and other documents that I reviewed also do not show that a "gate replacement process" is an essential part of the claimed invention.

77. Petitioner does not cite to any lexicography or disclaimer that would support its construction. Petitioner relies on one disclosure, which, in full, reads:

"Also, the arrangement of the dummy source structures may allow the gate electrodes/word lines to be formed with improved uniformity and quality, reducing the resistivity of the gate electrodes/word lines. For example, the gate-replacement process can be performed to deposit a conductive material through the dummy source holes that subsequently form the dummy source structures. Because the conductive material travels shorter distances to fill up the lateral recesses for forming the gate electrodes, the gate electrodes are less susceptible to voids or density nonuniformity."

Pet., 25 (citing '872, 5:49-58)

78. The above statement does not support Petitioner's construction, and does not support any argument that a gate replacement process is an essential part of the invention. The statement is merely an "example" of how the claimed dummy source structures "can" be formed and does not suggest that "a gate-replacement process" is an essential part of the claimed invention. Indeed, the specification

repeatedly qualifies the use of the “gate-replacement process” as merely one possible manufacturing method. See e.g., ’872, 4:30-33 (“[A] gate-replacement process is often used”), 5:52-55 (“the gate-replacement process can be performed to deposit a conductive material through the dummy source holes”), 16:40-49 (“In some embodiments ... dummy source structure 246 may...function[] as a mechanical supporting structure after gate-replacement process.... In some embodiments, ... dummy source structure 246 may ... still reach the lower part of the dielectric stack to carry out the gate-replacement process.”).

79. In addition, the ’872 teaches that the dummy source structures can be formed in multiple ways using “one or more thin film deposition processes including ALD [atomic layer deposition], CVD [chemical vapor deposition], PVD [physical vapor deposition], any other suitable processes, or any combination thereof.” Ex. 1001, 13:55-64; see also Ex. 1001, 12:34-36 (defining acronyms), 19:61-20:2 (explaining that “Summary and Abstract sections may set forth one or more but not all exemplary embodiments of the present disclosure as contemplated by the inventor(s)” and that the “breadth and scope of the present disclosure should not be limited by any of the above-described exemplary embodiments, but should be defined only in accordance with the [] claims and their equivalents”).

80. In other words, Petitioner’s construction attempts to improperly narrow the scope of the claim by limiting it a gate replacement process, which is just one disclosed embodiment in the ’623 patent.

81. I understand that in the Institution Decision to Institute (“DI”), the Board refused to adopt Petitioner’s position that “‘dummy source structure’ requires that the structure occupy the void used for the gate replacement process” (DI 12) and construed “‘dummy source structure’ as a structure that does not function as a source to the memory cells” (id., 11). I agree with the Board’s construction for the reasons explained above.

B. “Surrounding” (Claims 1, 13)

82. The term “surrounding” should be given its plain and ordinary meaning, which, contrary to Petitioner’s arguments, requires features that are more than just on two sides with another structure “between.”

83. As an initial matter, my analysis of the validity of the Challenged Claims does not turn on whether “surrounding” requires “fully encircling.” Therefore, it is my understanding that the Board does not need to resolve the full scope of “surrounding” or whether it requires “fully encircling,” and I do not offer an opinion on that issue in this declaration.

84. The term “surrounding” does not encompass features that are merely on two sides. First, the claim term at issue is “surrounding” rather than “between,”

and the claims expressly distinguish the concepts of “surrounding” and “between.” The term “between” is used when reciting the concept of being located somewhere in the middle of two structures and “surrounding” is used when reciting the concept of being located somewhere in the middle of more than two structures. Compare ’872 Claim 17 (“wherein at least one dummy channel structure is surrounded by at least eight dummy source structures”) with ’872, Claim 11 (“wherein at least one dummy source structure is located between the first and second staircase structure”); see also, e.g., Claim 12, Claim 15, Claim 16.

85. The ’872 specification also uses the terms “surrounding” and “between” to describe different concepts. As in the claims, the specification uses “between” when discussing the concept of being located somewhere in the middle of two structures and “surrounding” when discussing the concept of being located somewhere in the middle of more than two structures:

As shown in FIG. 1A, multiple dummy source structures, such as the four dummy source structures indicated by a diamond shape 146, may surround a staircase contact, such as staircase contact 122. ... [¶] ... A plurality of dummy channel structures, such as the four dummy channel structures indicated by square shape 148, may surround a staircase contact. The four dummy channel structures may be spaced with nominally equal lateral distances to the staircase contact, as shown in FIG. 1A. In other words, the

dummy channel structures surrounding a staircase contact may be evenly distributed around the staircase contact. ... [¶] ... In some embodiments, at least one dummy source structure may be located between two staircase contacts. For example, FIG. 1A shows that two dummy source structures are located between staircase contacts 122 and 122'. FIG. 1B shows another embodiment in which two dummy source structures are located between staircase contacts 123 and 123', while one dummy source structure is located between staircase contacts 123' and 123". FIG. 1C shows yet another embodiment in which one dummy source structure is located between staircase contacts 125 and 125', and one dummy source structure is located between staircase contacts 125' and 125". Other numbers of dummy source structures may also be disposed between two staircase contacts."

'872, 6:38-7:28.

86. This distinction is used consistently throughout the specification, including when the structures are slits. For example, the specification states that "dummy channel holes are formed between adjacent GLS".' 872, 4:56-61.

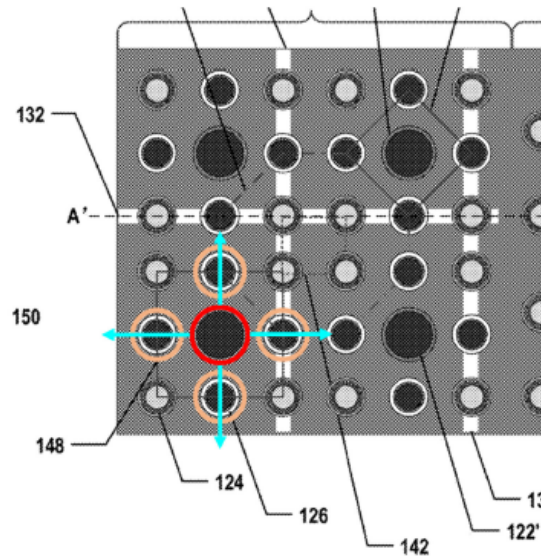
87. Based on my review, there is nothing in the '872 patent that teaches that a staircase contact can be "surrounded" by just two dummy source structures.

88. If structures placed on only two sides of an object were within the scope of the plain meaning of "surrounding," then there would have been no need for

the '872 to consistently use different terminology—"located between"—when there are structures on just two sides.

89. Further, it is irrelevant that the specification contemplates "less than four dummy source structures that 'surround' a word line contact" (Pet., 28 (citing '872 8:8-11)). The validity issues I discuss in my declaration require resolving whether only two parallel dummy structures can "surround" a word line contact, but do not require resolving exactly how much more is required. For example, the validity issues I discuss in my declaration do not require resolving whether less than four (e.g., three) dummy structures can "surround" a contact.

90. The argument that Figure 1A demonstrates that "surrounded includes being able to draw four lines outward from the staircase contact with each line being separated from the others by 90 degrees and intersecting a dummy source structure" (Pet., 30) is not consistent with the plain meaning of "surrounding." Indeed, even if "surrounding" was defined by some minimum angle between structures (as described by Petitioner), Figure 1A illustrates a separation of 90 degrees from the center of such structures:



Pet., 31 (Petitioner’s annotations).

91. Thus, this configuration disclosed in the specification with four dummy source structures at 90 degrees is different from—and does not provide support for—a configuration having only two dummy structures, i.e. where the angle is 180 degrees.

92. Finally, Petitioner’s extrinsic evidence does not change my opinion. Petitioner does not explain the relevance that a lay description of an “isthmus” (provided by the website “<https://www.studycountry-com/wiki/what-is-a-piece-of-land-surrounded-by-water-on-2-sides>” in March of 2024) has to the meaning of “surrounding” as used by the ’872. Pet., 32 (citing Ex. 1018).

93. Petitioner’s reliance on U.S. Pat. No. 9,530,492 (the “’492 patent”) is similarly misplaced. Pet., 32 (citing Ex. 1019, 2:14-16). Although the ’492 patent states that “the conventional SBPI operations are strongly affected by the stored Vts

of two surrounding NAND cells dispersed in the adjacent left and right BLs” (Ex. 1019, 2:14-16), this passage is merely referring to the effects of NAND cells in the surroundings (i.e., in the vicinity). The ’492 patent does not suggest that two NAND cells can surround SBPI operations. And even if Petitioner’s interpretation of the ’492 patent were correct, it does not outweigh the consistent usage of “surrounding” in the ’872, consistent with the plain meaning.

94. I understand that in the Institution Decision, the Board noted that “‘surrounding’ in claim 1 of the ’872 patent does not encompass structures on only two sides of an object.” DI 16. I agree with the Board’s construction for the reasons explained above.

C. “Conductive Contact” (Claims 1 and 13)

95. The term “conductive contact” should be construed as a conductive structure that permits current flow with an adjoining conductive structure.

96. This construction gives proper meaning to the word “contact” in the claims and is supported by the intrinsic evidence as well as the plain meaning of the word “contact” as evidenced by extrinsic dictionary definitions.

97. I understand that Petitioner discussed its views on the meaning of “conductive contact” in its Preliminary Reply. Petitioner’s arguments in its Preliminary Reply either ignore or mischaracterize the evidence discussed below. In addition, Petitioner proposed a construction that disregards the term “contact” and

conflates the term “conductive contact” with a conductive core. Prelim. Rep., 5-7. Therefore, as discussed further below, I disagree with Petitioner’s proposed construction.

(a) The Term “Conductive Contact” as Used in the ’872 Patent

98. The claims, specification, and drawings of the ’872 support construing “conductive contact” as a conductive structure that permits current flow with an adjoining conductive structure.

99. The word “contact” in the claims supports this construction. The ’872’s claims expressly require a “conductive contact” rather than a conductive material or conductive core: “each dummy source structure comprises a conductive contact.” *See* Claim 1.

100. This construction, which requires a conductive structure that permits current flow with an adjoining conductive structure, gives proper meaning the term “contact” because the “contact” structure is what permits the conductive material to conduct current with an adjoining structure.

101. I understand that the Board in its Institution Decision concluded that the claims do not “require contact between a dummy source structure and another structure” (DI 23-24), but this interpretation disregards the term “contact” in the claims. While a conductive material or a conductive core may in some circumstances provide a conductive contact, depending on the particular structure,

the mere presence of a conductive material or conductive core alone does not necessarily mean that a contact is present.

102. The specification also supports construing “conductive contact” as a conductive structure that permits current flow with an adjoining conductive structure because it describes, for example, dummy source structures that contact another structure such as a peripheral device, and therefore permit current flow to another conductive structure. For example, the ’872 patent shows that in Fig. 2L, each dummy source structure 246 (shown in black)—which is filled with conductive material—extends vertically through a staircase structure and an insulation layer to form an exposed conductive contact 244. Ex. 1001, 11:37-39, 16:21-32, 16:63-66.

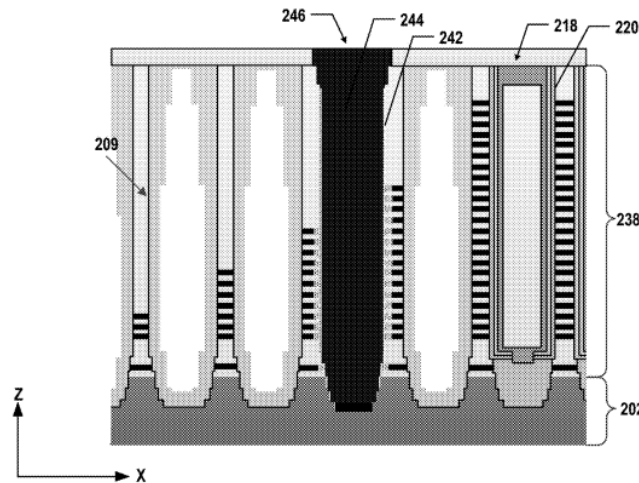


FIG. 2L

103. This exposed conductive contact enables the dummy source structure to “function as an interconnect to connect 3D memory device 100 with other peripheral devices.” Id., 16:63-66.

104. Thus, the specification and drawings confirm that the “conductive contact” is a conductive structure that permits current flow with an adjoining conductive structure

105. Conversely, a structure that is completely enclosed by an insulator does not form such a contact. Dr. Banerjee appears to recognize that this scenario prevents such a contact. See Ex. 2008, 38:11-15 (“[T]he insulator material is what’s used to create a scenario where you have no direct electrical contact with the rest of the device.”); see also id. 28:9-11.

106. I understand that in the Institution Decision, the Board based its decision on its interpretation of the portion of the specification that states “[w]hen conductive materials are used to fill dummy source hole 212 (e.g., contact 244), the dummy source structure 246 may function as an interconnect to connect 3D memory device 100 with other peripheral devices.” ’872, 16:63-66. The Board read this passage as disclosing a “dummy source structure” with “contact 244” that “may or may not” function as an interconnect (DI 23-24), but the specification instead states that the “dummy source structure” with “conductive material” may or may not function as an interconnect, and that the “contact 244” is an example (“e.g.”) of using a conductive material to form an interconnect. Logically, if a dummy source structure with conductive material is completely enclosed with insulator, for example, then it would not function as an interconnect (or as a “contact”), even

though conductive material is in the dummy source structure. This passage of the '872 specification is worded to allow for those exceptions.

107. Moreover, the Board's conclusion that the above-cited passage of the '872 allows for a contact that does not "function as an interconnect" (DI 23) is still consistent with construing "conductive contact" as a conductive structure that permits current flow with an adjoining conductive structure. This construction, which requires a conductive structure that permits current flow with an adjoining conductive structure, limits the structure. The structure must permit current flow with an adjoining conductive structure, for example by contacting an interconnect or other conductive structure. This construction does not require that the conductive contact actually have current passing through it—indeed, the claimed conductive contact is part of the "dummy source structure," which "does not function as a source to memory cells." See §VIII.A.

108. Construing "conductive contact" as a conductive structure that permits current flow with an adjoining conductive structure also does not limit the location of the "contact" on the dummy source structures (e.g., whether the contact is on top of the dummy source structures or elsewhere). Thus, the '872 specification is consistent with this construction.

109. Therefore, the intrinsic record, including the '872 claims and specification, supports the construction that the “conductive contact” is a conductive structure that permits current flow with an adjoining conductive structure.

(b) Extrinsic Evidence Supports the Construction

110. The extrinsic evidence further supports construing “conductive contact” as a conductive structure that permits current flow with an adjoining conductive structure. For example, “electric contact” is defined as “[a] physical contact that permits current flow between conducting parts.” See Ex. 2011 (McGraw-Hill Dictionary of Scientific and Technical Terms, Sixth Edition). As another example, “contact” is defined as “the state or condition of physical touching, a connection for the passage of electric current from one thing to another, or a part or device by which such a connection is made.” See Ex. 2009 (New Oxford American Dictionary, Third Edition). Similarly, “contact” is defined in another technical dictionary as “[t]he coming together, touching, union, or junction of surfaces or objects, or the junction of two conductors so that current may flow.” See Ex. 2010 (Wiley Electrical and Electronics Engineering Dictionary). Construing “conductive contact” as a conductive structure that permits current flow with an adjoining conductive structure is consistent with the plain meaning of “contact” as confirmed by these references. In contrast, Petitioner’s construction—i.e., “conductive material that fills the dummy source hole” (Prelim. Rep., 6)—would read on a metal structure that is completely

enclosed by insulator and therefore contradicts and ignores the well-understood meaning of “contact.”

111. Accordingly, “conductive contact” should be construed as a conductive structure that permits current flow with an adjoining conductive structure.

IX. THE ASSERTED PRIOR ART

A. U.S. Patent No. 9,859,297 (“Park”) (Ex. 1005)

112. I note that Petitioner does not contend that Park anticipates the Challenged Claims, and instead argues only that it renders obvious certain claims, including the sole independent Challenged Claim, Claim 1. Pet., 8, 40-74.

113. Park discloses aspects of a memory device upon which the ’872 improves. Park describes a semiconductor device including: a substrate having a cell region and stepped dummy region; a common source line (“CSL”); gate lines; insulating interlayer patterns; dummy patterns; and dummy source lines. Ex. 1005, 6:1-9:3, Figs. 1-2. Park’s semiconductor device includes both **common source lines**, which function as a common source for the memory cell (and are therefore not dummy source structures), and **dummy source lines** in the dummy region. Ex. 1005, 13:53-58, 23:1-4, Fig. 1, Fig. 13. As illustrated in Figures 1 and 13 below, **common source lines** extend in the “2nd direction,” and are spaced apart from each other along the “3rd direction,” of the cell region; the **dummy source lines**, on the other hand,

extend in the “3rd direction,” and are spaced apart from each other along the “1st direction,” of the dummy region:

FIG. 13

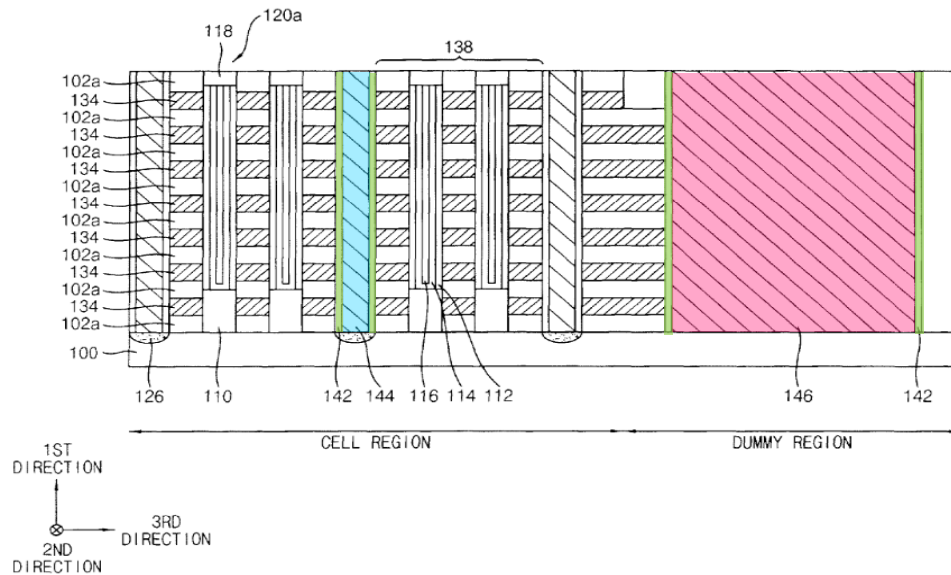
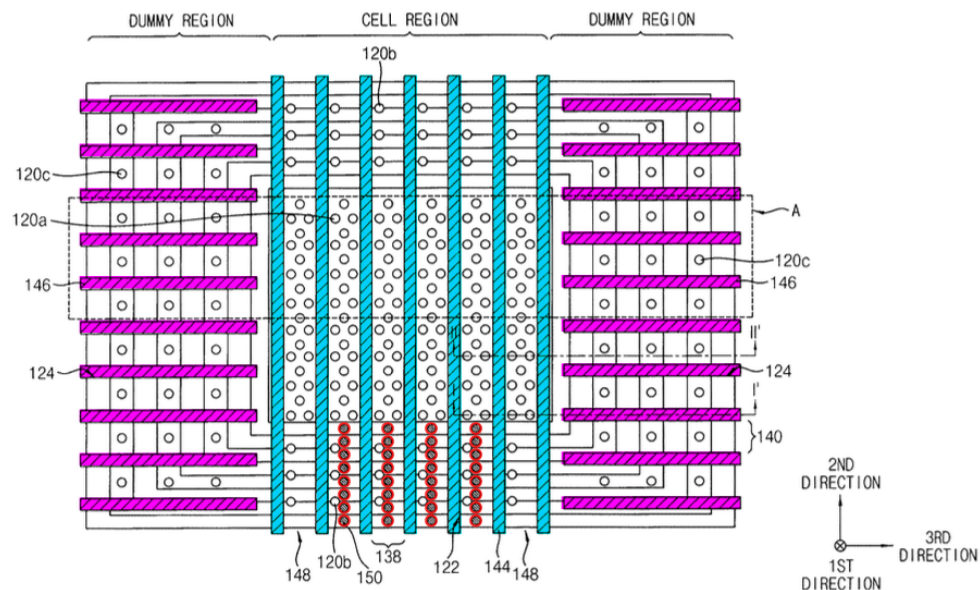


FIG. 1



Ex. 1005, Fig. 13, Fig. 1, 3:6-9.

114. Park further discloses that between the **common source lines** is a wiring region, where **contact plugs** (annotated in red in Figure 1 above) are formed in contact holes etched through the upper insulation layers and electrically connect to the gate lines. Ex. 1005, Fig. 1, 7:26-37, 13:60-54. Because Park's contact plugs are just between two **common source lines**, the **common source lines** do not surround the **contact plugs**. See Ex. 1005, Fig. 1. Park's **dummy source lines** also do not surround the **contact plugs** as shown above in Fig. 1.

B. U.S. Patent Pub No. 2019/0081061 ("Tessariol") (Ex. 1006)

115. I note that Petitioner does not contend that Tessariol anticipates the Challenged Claims, and instead argues only that it renders obvious the Challenged Claims. Pet., 8, 74-101.

116. Tessariol discloses aspects of three-dimensional memory devices upon which the '872 claims improve. Ex. 1006, [0006]. Tessariol's circuit structure includes a stair step structure composed of **vertically-stacked alternating layers** (e.g., alternating layers of insulative material and conductive materials). Ex. 1006, [0029], [0031], [0034]. Dummy-structure openings and via openings are formed through the vertically-alternating layers. Ex. 1006, [0037]. Within via openings **operative conductive vias** are formed and within dummy openings **dummy structures** are formed—each extending through the **vertically-alternating layers**, as depicted below. Ex. 1006, [0038].

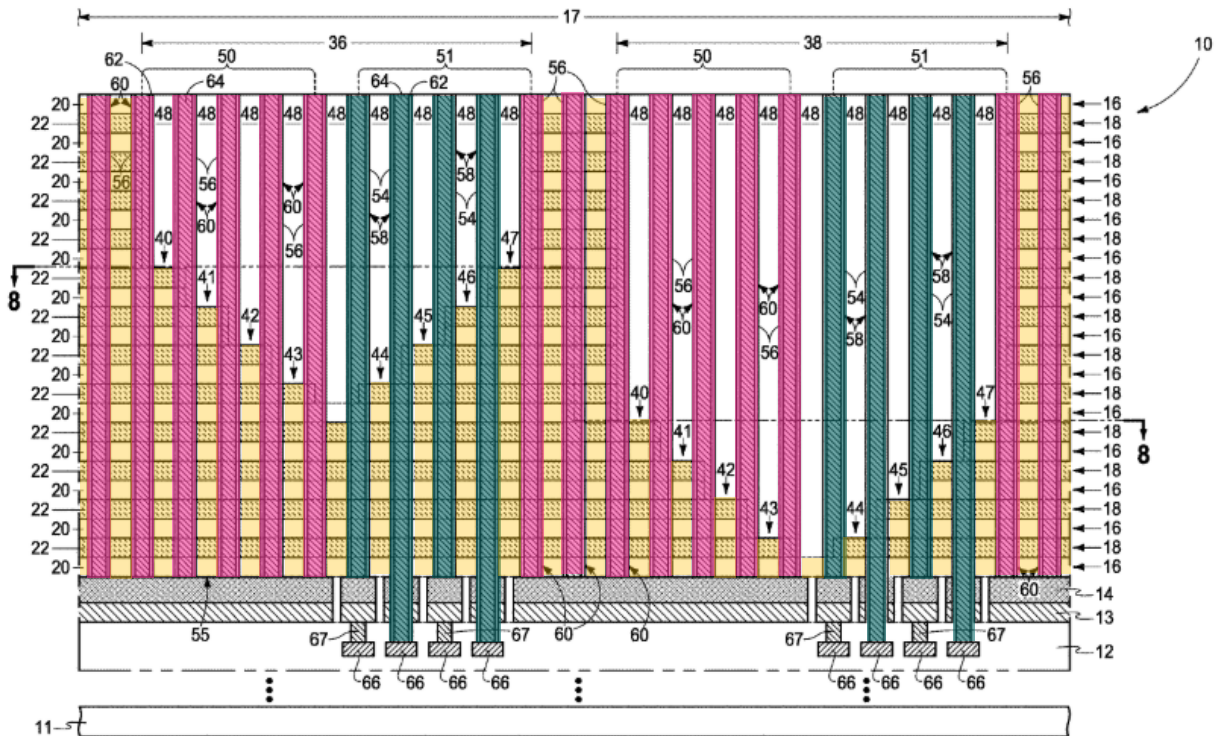


FIG. 9

117. Tessariol discloses that **operative conductive vias** and **dummy structures** may be composed of an **insulative lining** (e.g., silicon dioxide and/or silicon) and a **conductive core**, as depicted below. Ex. 1006, [0038]. Whereas the **operative conductive vias** may “directly electrically couple to individual conductive lines,” Tessariol does not disclose that the **dummy structures** can comprise a conductive contact. As Tessariol explains, “[i]n this document, *a ‘dummy structure’ refers to a structure which is used to mimic a physical property of another structure (e.g., presence, or physical load-carrying/supporting ability of an operative structure) and which may comprise a circuit inoperable electrical dead end* (e.g., is not part of a current flow path of a circuit even if conductive).”

Ex. 1006, [0068]. In other words, while dummy structures may be conductive, they are not part of a circuit because they only mimic the physical properties (not the functional properties) of their operative counterparts. Consequently, even as electrical dead ends, dummy structures do not have a conductive contact.

118. Tessariol additionally discloses **operating conductive vias**, depicted in the color-annotated below:

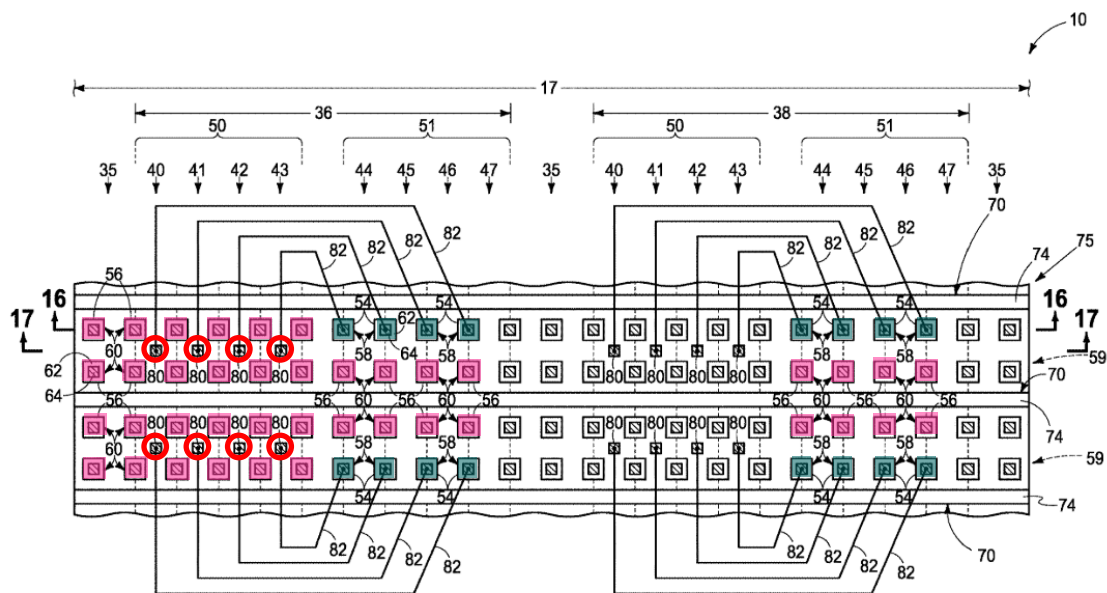
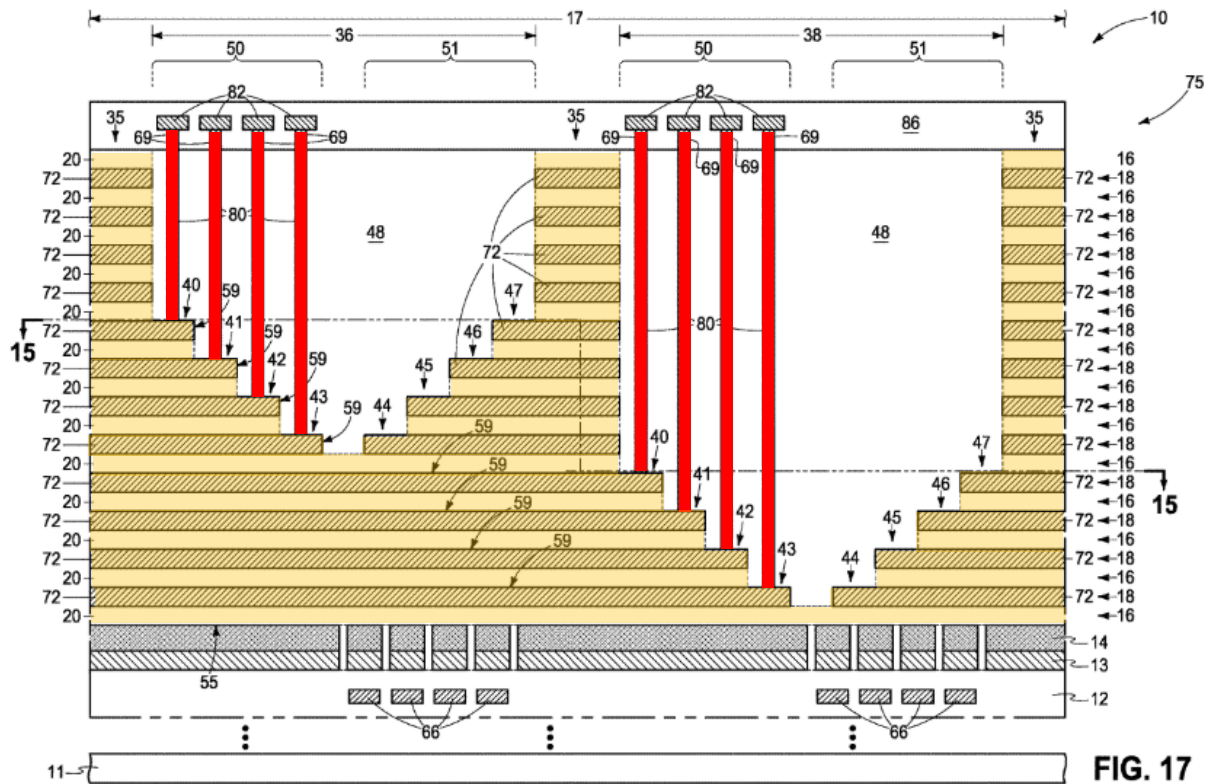


FIG. 15

119. These **operating conductive vias** each connect to a conductive step of the **vertically-alternating layers**, extend through the layers, and are “directly electrically coupled to one another by an interconnect line” above the alternating layers. Ex. 1006, [0046], [0052].



X. PETITIONER’S GROUND 1: PARK DOES NOT DISCLOSE OR RENDER OBVIOUS CLAIMS 1-6, 11-13

120. For the reasons explained below, it is my opinion that Park does not disclose or render the Challenged Claims at least because Park does not disclose or render obvious multiple requirements of limitation [1.e] of the sole challenged independent claim, including “dummy source structures” and dummy source structures “surrounding” the staircase contact under the proper construction of those terms (§VIII.A-B). In addition, Park does not disclose or render obvious the additional limitations of claims 2-6 and 11.

A. Independent Claim 1: Park Does Not Disclose or Render Obvious Claim 1, and Specifically, Limitation [1.e]

121. Petitioner does not show that Park discloses or renders obvious at least two requirements of limitation [1.e]: “a plurality of dummy source structures each extending vertically through the staircase structure, the plurality of dummy source structures surrounding the staircase contact.”

122. Park’s common source lines and dummy source lines, alone or collectively, are not “surrounding” the purported “staircase contact.” Instead, Park’s disclosures are nearly identical to the very prior art that the invention of the ’872 improves upon.

123. Further, Ground 1 is reliant on Petitioner’s incorrect construction for “dummy source structure.” Under the proper construction of this term, the structures identified by Petitioner function as a source and are therefore not “dummy source structures.”

(a) Park’s Common Source Lines and Dummy Source Lines, Alone or in Combination, Are Not “Surrounding” the Contact Plugs (Limitation [1.e])

124. Park’s alleged “dummy source structures” are not “surrounding the staircase contact” under the proper construction of “surrounding”—that the term does not encompass structures on only two sides of an object (§VIII.B). See also DI, 16.

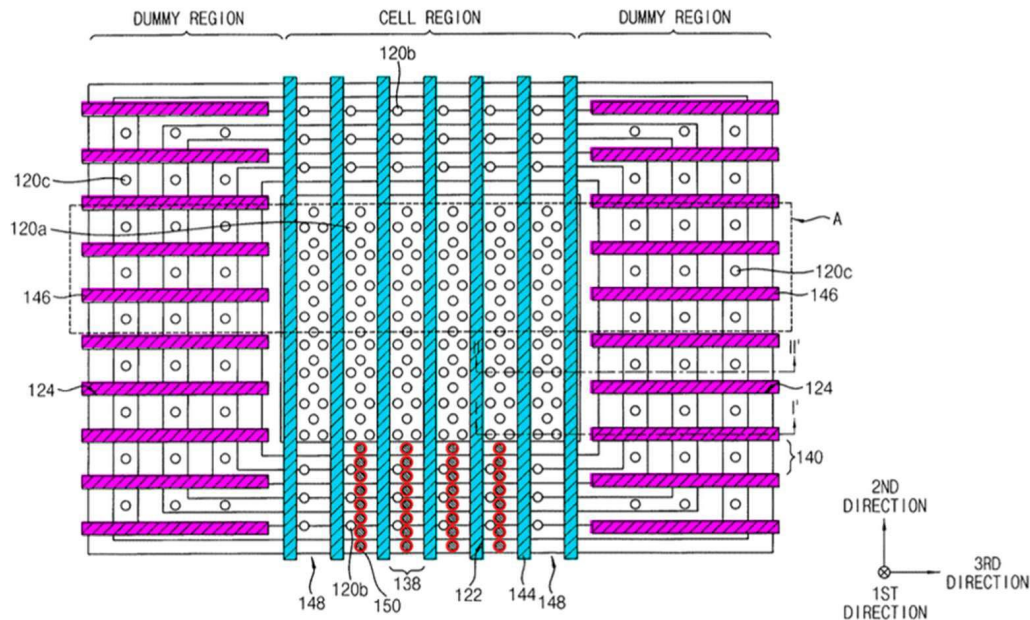
125. Park’s staircase contact is merely “between” two alleged dummy source structures, and therefore the alleged dummy source structures are not surrounding the staircase contact.

126. As I discuss above in §VIII.B, limitation [1.e]—which in part is directed to “the plurality of dummy source structures surrounding the staircase contact”—requires that the dummy source structures are on more than just two sides of the staircase contact, and it is insufficient for a staircase contact to be merely “between” two dummy source structures.

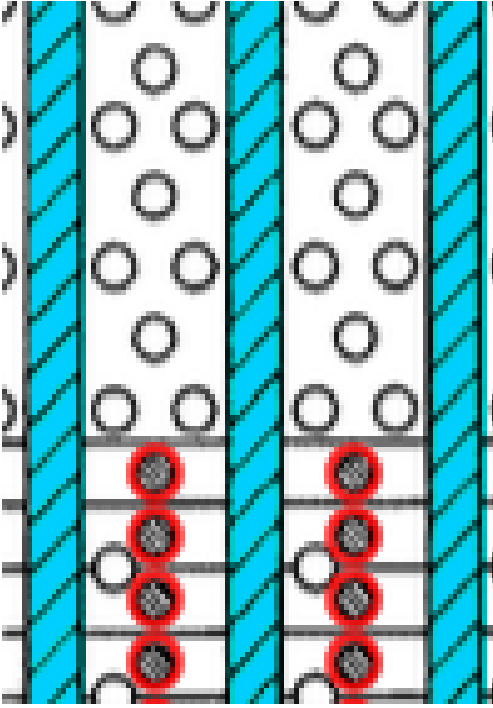
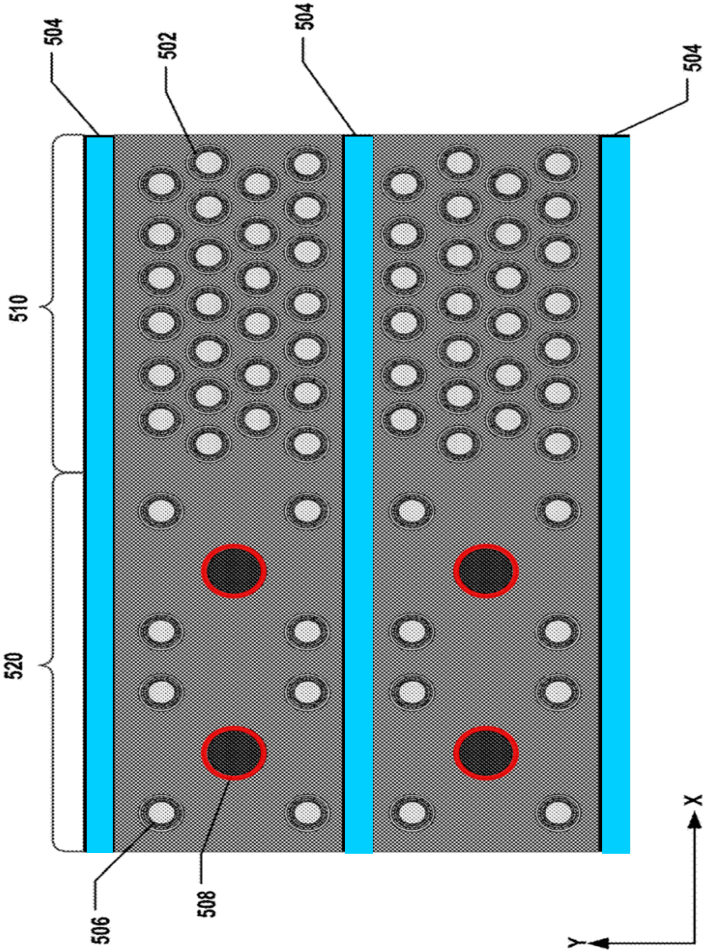
127. Petitioner maps two separate elements of Park—**common source lines 144** and **dummy source lines 146**—to the ’872’s “dummy source structures” (Pet., 2-3, 50-51), but neither structure surrounds the alleged staircase contacts.

128. The **dummy source lines** do not “surround” the contact plugs (the alleged “staircase contact”) as depicted below, because the **contact plugs** are merely between the two sets of **dummy source lines**. Thus, although Petitioner argues that common source lines 144 and dummy source lines 146 collectively surround the contact plugs 150 (Pet., 58), Petitioner’s explanation focuses solely on the common source lines 144 alone. See Pet., 58-62.

FIG. 1



129. Park’s **common source lines** also do not surround the **contact plugs** (the alleged “staircase contact”) because the **common source lines** are merely on two sides of the **contact plugs**—there is no dispute that Park’s common source lines 144 do not disclose or render obvious this limitation under the proper construction. Moreover, Petitioner overlooks that the configuration of Park’s common source line 144 and contact plug 150 is precisely the configuration that the invention distinguished over the admitted prior art. Below is a side-by-side comparison of the relevant portions:

	
Excerpt of Petitioner's annotated Park, Fig. 1 (Pet., 59) (highlighting contact plugs 150 in red between parallel common source line 144 in blue). <i>See also</i> Ex. 1005, 2:46-47, 5:27-33, 6:15-17.	'872, Fig. 5 (rotated view of admitted prior art, illustrating staircase contacts 508 in red between parallel gate line slits 504 in blue). <i>See also</i> Ex. 1001, 5:1-14.

130. The '872 discloses that the prior art GLSs extend through a staircase region that includes staircase contacts 508. Ex. 1001, 5:1-8. Similarly, Park's

common source lines 144 cross through the wiring region that contain contact plugs 150. Ex. 1006, 13:62-64. The '872 discloses that characteristics of “the shape of GLS 504” is “a slit shape with a dimension along the extending direction (or the x-direction) much greater than the dimension along the expanding dimension (or the y-direction).” Ex. 1001, 5:23-25. Similarly, Park’s common source lines 144 “extend in the second direction” in “a plan view,” in which the “second direction [is] parallel to the top surface of the substrate,” and much greater than in the third direction.

131. Accordingly, Park’s common source lines 144 geometry and arrangement are substantially the same as that of the prior art GLSs that the '872 improved upon. Notably, the '872 uses the term “between”—not “surround”—to describe the “dummy channel holes [] between adjacent GLSs” in Figure 5. '872, 4:56-57, 5:1-2.

132. Additionally, Park discloses, at best, the same configuration of alleged staircase contacts “between” parallel gate line slits, rather than “surround[ed]” by dummy source structures.

133. Thus, under the proper construction of “surrounding” as excluding features that are merely on two sides with another structure between, Park’s alleged “dummy source structures”—common source lines and/or dummy source lines—are not “surrounding the staircase contact” as required by the Challenged Claims.

134. The Institution Decision correctly notes that “[b]ecause we determine that ‘surrounding’ does not encompass structures on only two sides of an object, we are not persuaded, on this record, that Park teaches dummy source structures ‘surrounding the staircase contact’ as recited in claim 1.” DI 16, 23.

(b) Park’s Common Source Lines Are Not “Dummy Source Structures” (Limitation [1.e])

135. Park’s common source lines—Petitioner’s alleged “dummy source structures—function as common source lines are therefore not “dummy source structures” as properly construed.

136. All Challenged Claims require “a plurality of dummy source structures.” As I discuss in §VIII.A, the claimed “dummy source structure” is a structure that does not function as a source to memory cells.

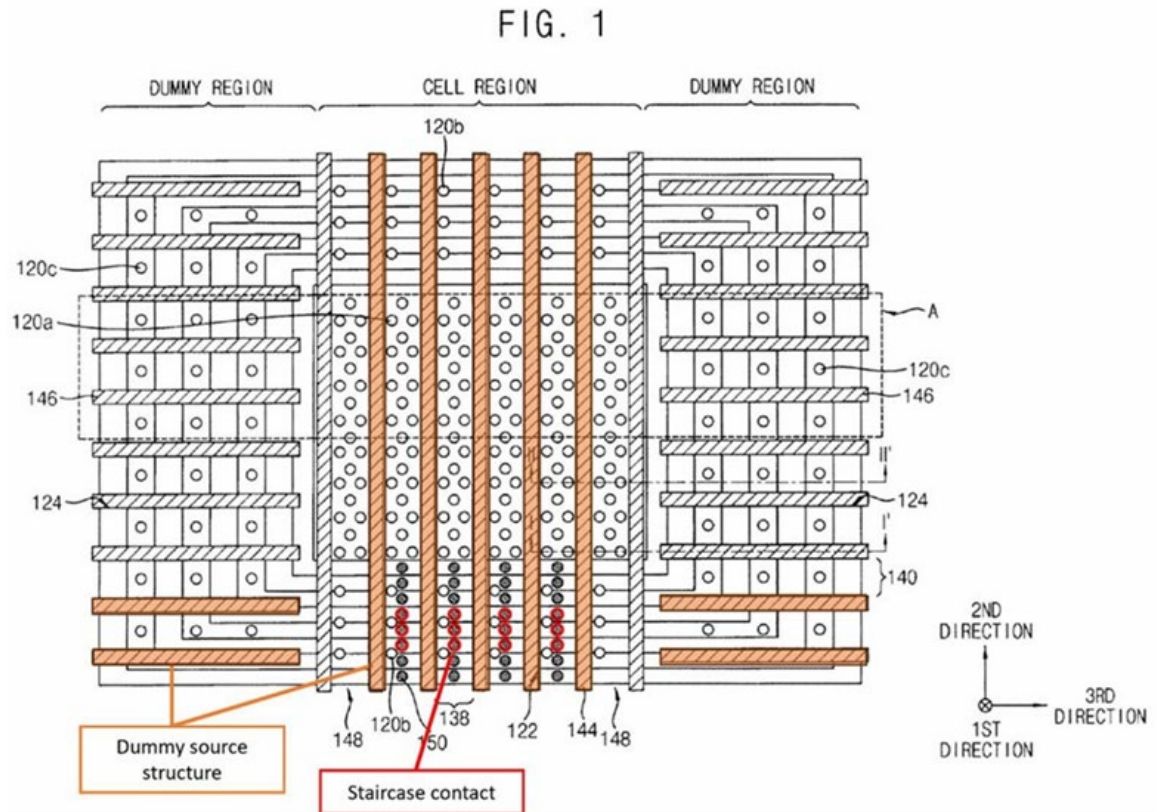
137. Further, as discussed, Park does not disclose “dummy source structures” that meet every requirement of the claims. Petitioner proposes mapping a combination of two separate elements—common source lines 144 and dummy source lines 146—to the ’872’s “dummy source structure.” Pet., 2-3, 50-51.

138. As an initial matter, Park’s **dummy source lines** cannot be the claimed “dummy source structures” because Petitioner does not map Park’s dummy source lines to every relevant claim requirement. As I discuss above in the preceding section, while Petitioner alleges that Park’s common source lines 144 and dummy source lines 146 are collectively “a plurality of dummy source structures,” Petitioner

maps only the common source lines to other limitations of the claims relating to the dummy source structure, such as the requirement of “the plurality of dummy source structures surrounding the staircase contact” as discussed above. Pet. 50-62. Because Petitioner does not map Park’s dummy source lines to the “surrounding” requirement, Park’s dummy source lines cannot be the claimed “dummy source structures” of the Challenged Claims.

139. Further, Park’s **common source lines** are not dummy source structures because they function as a source to the memory cells and are, therefore, actual—not dummy—source structures. As an example, I reproduce below the annotated version of Fig. 1 from pg. 58 of Dr. Banerjee’s declaration. It is immediately clear that the common source lines 144 (which Dr. Banerjee has indicated in orange) extend (in the 2nd direction) across the entirety of the “cell region”. The lines are not in the region marked “dummy region”, they are clearly marked 144 (“common source lines”) and a POSITA would recognize that simply extending the “common source line” (144) to a location adjacent to the staircase contacts does not change its function. It is still the common source line, not a dummy source. In the same way that extending a word line further into the staircase does not turn it into a dummy word line, extending the common source line further into the staircase does not turn into a dummy source structure. Overall, a POSITA would understand that the straightforward dimensional extension into the staircase of the common source line

(whose function is to supply electrical carriers to the sources of the transistors), would not remove its functionality and convert it into a dummy source structure.



Ex. 1005, Fig. 1 (annotated).

140. In fact, Park expressly distinguishes between the “common source line” for the memory cell structure, which functions as the source line, and a “dummy source line.” *See, e.g.,* Ex. 1005, 6:1-11, 7:59-60, 13:39-41. Similarly, Park’s figures show separate regions where the common source line and dummy source lines are located—the common source line is in the “cell region” and the dummy

source line is in the “dummy region.” Ex. 1005, Fig. 1. Thus, Park’s common source lines 144 are not dummy source structures.

141. Petitioner attempts to incorrectly equate Park’s common source line to the ’872’s teaching that “‘dummy source structures’ can [make] ‘contact with the substrate and may provide interconnect between the 3D memory device and peripheral devices.’” Pet., 55-56 (omitting citations). Contrary to Petitioner’s suggestion, the ’872’s disclosure that “dummy source structures” may “serve as an interconnect between the 3D memory devices and peripheral devices” (Ex. 1001, 5:40-43) does not suggest that Park’s common source line is also a dummy structure. As I mentioned above, the function of Park’s common source line (144) does not somehow change if it is simply extended further into that part of Park’s “cell region” that contains the staircase contacts. It is still the common source line. Moreover, it is not serving as an interconnect between “3D memory devices and peripheral devices”, it is serving the same function it does elsewhere in Park’s “cell region”.

142. Specifically, the interconnect referenced in the ’872 is not a common source line. The ’872 explains that the “peripheral device” that the dummy source structure may connect to includes “peripheral circuits used for facilitating the operation of the 3D memory device 100, such as page buffers, decoders, and latches.” Ex. 1001, 9:37-40. As such, the ’872 “dummy source structure” does not function as a source to a memory cell. Park’s common source lines 144, on the other hand,

do function as the source to memory cells, and therefore common source lines 144 are actual source structures and not dummy source structures.

143. I understand that in the Institution Decision, the Board noted that “[b]ased on the current record, we are not persuaded that Petitioner sufficiently shows that Park teaches the claimed ‘dummy source structure.’” DI 21. The Board distinguished the common source lines from the dummy source lines and stated that “common source lines 144 are disposed on the cell region of the substrate while dummy source lines 146 are disposed on the dummy region alone,” and therefore the common source lines and the dummy source lines “may not operate in the same way or serve the same purpose.” Id., 22. I agree with this analysis.

144. Indeed, Petitioner makes no effort to explain why common source lines do not function as designed, i.e., as sources, but instead, as dummy source lines.

145. Accordingly, in my opinion, Park does not disclose “dummy source structures” as claimed. See also DI 22 (“[N]either Petitioner nor Dr. Banerjee sufficiently explains why Park’s common source lines 144 are ‘structures that do not function as sources for the memory cell.’”).

B. Claim 2: Park’s Dummy Source Structures Are Not Located Adjacent to the Staircase Contact

146. Petitioner does not allege that Park’s dummy source lines are adjacent to the staircase contact as required by Claim 2. Pet. 64-65. For Claim 2, Petitioner instead maps the claimed “plurality of dummy source structures” to Park’s common

source lines 144 (Pet. 64-65), but as explained in Claim 1, Park's common source lines 144 are not "dummy source structures" because they function as a source to memory cells. *See* §X.A.

147. Accordingly, Petitioner has not shown that Park discloses or renders obvious Claim 2.

C. Claim 3: At Least Two of Park's Dummy Structures are Not of Nominally Equal Lateral Distances to the Staircase Contact

148. Petitioner does not show that Park discloses "at least two of the plurality of dummy source structures are of nominally equal lateral distances to the staircase contact" as required by Claim 3 because Petitioner's reliance on Park's Fig. 1 is insufficient to show that the claimed distance-based requirement is satisfied.

149. With respect to Park's dummy source lines 146, Petitioner points to annotated lines in Park's Fig. 1 as allegedly showing uniform distribution, but Fig. 1 does not include a scale, dimensions, or any other means to measure distances between components. Pet., 65-66. I understand that patent drawings that do not define the precise proportions of the elements may not be relied on to show particular sizes if the specification is silent on the issue. Moreover, the dummy source lines 146 have no stated relationship in the patent (dimensional, symmetry, or otherwise) to the staircase contacts (150). Furthermore, a POSITA would not assume (particularly given embodiments such as that shown in Fig. 30, where some of the dummy structures have been rotated; and embodiments such as Fig. 31 where some

of the dummy structures are not only rotated, but asymmetrically rotated) that there is any dimensional relationship between the dummy source lines (146) and the staircase contacts (150). Overall, a POSITA would not assume any particular dimensional relationship between the dummy source lines 146 and the staircase contacts (150) based on Fig. 1 or any other figure in Park.

150. With respect to Park's common source lines 144, Petitioner does not annotate Figure 1 to attempt to show the relative distances, but even if Petitioner had done so, such arguments would be insufficient for the reasons discussed above for dummy source lines 146.

151. Finally, Petitioner does not argue that it would have been obvious to modify Park such that the alleged dummy structures are of nominally equal lateral distances to the alleged staircase contact.

152. Accordingly, Park does not disclose or render obvious Claim 3.

D. Claim 4: Park's Dummy Structures Are Not of Nominally Equal Lateral Distances to the Staircase Contact

153. For the same reasons explained above for Claim 3, Petitioner's reliance on figures is insufficient to show that the plurality of purported dummy source structures are of "nominally equal" lateral distances to the purported staircase contact. *See* §X.C.

154. Park therefore does not disclose or render obvious Claim 4.

E. Claim 5: Park’s Dummy Source Structures Are Not Arranged in a First Row That Extends Along a First Lateral Direction

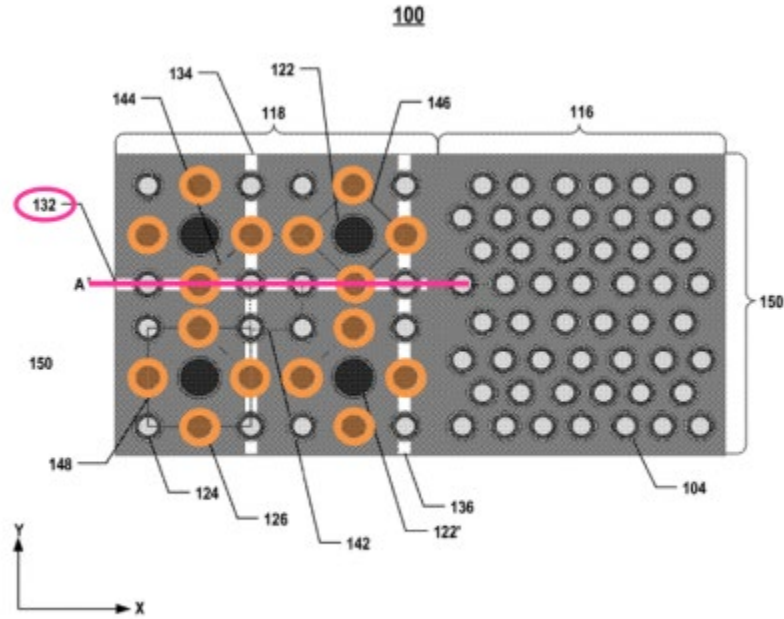
155. Park continues to lack “dummy source structures” that meet every applicable element of the Challenged Claims. Petitioner does not allege that Park’s common source lines are arranged in a first row that extends along a first lateral direction as required by Claim 5. Pet. 68-69. For claim 5, Petitioner instead maps the claimed “plurality of dummy source structures” to Park’s dummy source lines (Pet. 68-69), but as explained in Claim 1, Park’s dummy source lines do not surround the alleged staircase contact. *See* §X.A.

156. Accordingly, Petitioner has not shown that Park discloses or renders obvious Claim 5.

F. Claim 6: Park’s Dummy Source Structures Are Not Arranged in a Second Row That Is Perpendicular to the First Lateral Direction

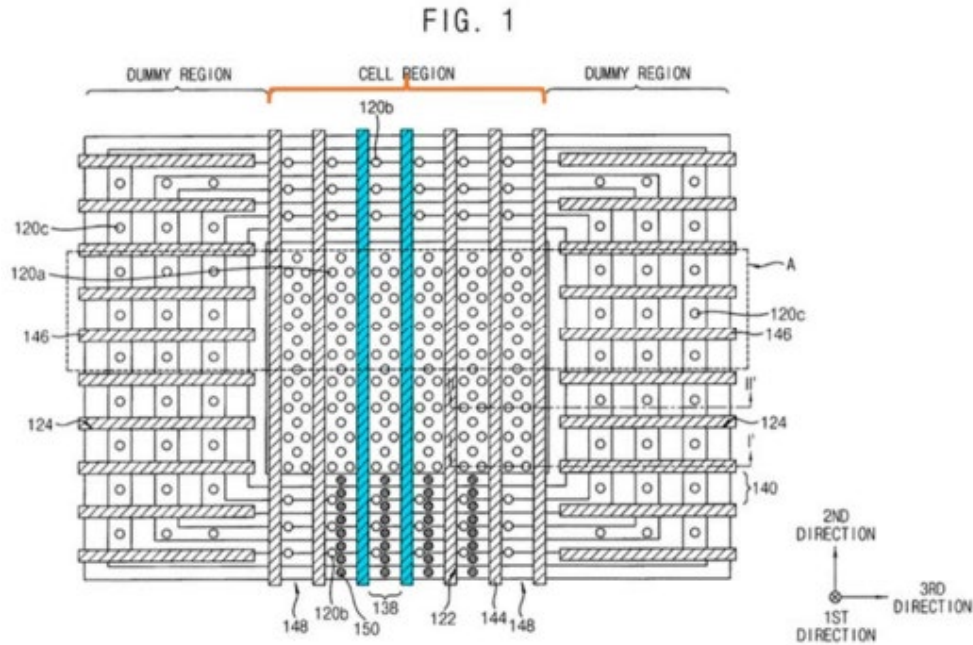
157. Park’s common source lines, which Petitioner maps to this claim as the alleged “at least two other dummy source structures,” span the entire cell region and, therefore, are not “arranged in a row” as required by Claim 6.

158. Claim 6 requires “wherein in the plan view, at least two other dummy source structures are arranged in a second row that extends along a second lateral direction perpendicular to the first lateral direction.” For example, Figure 1A of the ’872 shows at least two dummy source structures (orange) arranged in row 132:



'872, Fig. 1A (annotated).

159. Here, Petitioner maps only Park's common source lines to this claim, because it mapped the dummy source lines to claim 5 but did not show that Park's common source lines are arranged in a row. Pet. 68-71. In Petitioner's mapping, two of Park's common source lines are adjacent to each other in a direction identified as the "3RD DIRECTION" in Park's Figure 1:



Ex. 1005, Fig. 1 (annotated)

160. Petitioner alleges that the 3RD DIRECTION (“east to west”) is the alleged row of common source lines. Pet., 70-71. However, these common source lines are not “arranged in a second **row**.” While the common source lines are aligned laterally (in the “3RD DIRECTION”), they each extend across the entire cell region in the “2ND DIRECTION” (annotated in orange in Figure 1 above), rather than in a row. This extension means that the common source lines occupy the entire space of the cell region, rather than being organized in row.

161. Thus, Park’s alleged dummy source structures are not “arranged in a second row” as required by Claim 6.

G. Claim 11: Park’s Dummy Source Structure Is Not Located Between First and Second Staircase Contacts

162. For Claim 11, Petitioner maps the claimed “at least one dummy source structure” to Park’s common source lines 144 (Pet. 71-72), but as explained in Claim 1, Park’s common source lines 144 are not “dummy source structures” because they function as common source lines for the memory cells. *See* §X.A.

163. Accordingly, Petitioner has not shown that Park discloses or renders obvious Claim 11.

XI. PETITIONER’S GROUND 2: TESSARIOL DOES NOT DISCLOSE OR RENDER OBVIOUS CLAIMS 1-6, 11-13

164. For the reasons explained below, it is my opinion that Tessariol does not disclose or render obvious the Challenged Claims at least because the alleged “dummy source structures” do not satisfy multiple requirements of the sole independent claim—claim 1. In addition, Tessariol does not disclose or render obvious the additional limitations of claims 3-4.

A. Independent Claim 1: Tessariol Does Not Disclose or Render Obvious Multiple Limitations

165. Tessariol does not disclose or render obvious multiple limitations relating to the claimed dummy source structures. Petitioner points to Tessariol’s conductive vias 58 and dummy structures 60 as the alleged dummy source structure, but neither structure satisfies all of the claimed requirements.

166. As a preliminary matter, even under Petitioner’s incorrect construction of “conductive contact” (“structure that occupies the void that was used for the gate replacement process,” see Pet. 24), Petitioner admits that Tessariol does not meet the claims. Specifically, Petitioner admits that “Tessariol’s dummy structures 60 and operative conductive vias 58 do not fill the voids used for the sacrificial gate replacement process.” Pet., n.6. And under the correct construction of “conductive contact” (see §VIII.C), neither the conductive vias 58 or the dummy structures 60 meet all the requirements of the claimed dummy source structure.

167. Tessariol’s conductive vias 58 are not “dummy source structures” as required by limitation [1.e] because Petitioner does not shown that the conductive vias 58 do not function as a source to memory cells as required under the proper construction of the term, and furthermore, Tessariol’s conductive vias do not “surround” the alleged staircase contact as required by limitation [1.e].

168. Tessariol’s dummy structures 60 are not “conductive contact” as required by limitation [1.f], and a POSITA would not have been motivated to couple Tessariol’s dummy structures to its upper-level interconnect lines. Overall, since Tessariol already has a conductive via 58 structure (whose described and illustrated function is to connect to the upper-level interconnects) there is no motivation for a POSITA to repurpose dummy structures 60 to duplicate that existing function.

169. I understand that it is insufficient to show that dummy structures 60 satisfy some requirements, while conductive vias satisfy other requirements, when the claim recites that each of the claimed requirements apply to the “plurality of dummy source structures.” Neither the dummy structures 60 nor the conductive vias 58 satisfies all of requirement of the claimed “dummy source structures.” As explained below, neither dummy structures 60 nor conductive vias 58 meets all of the various requirements for the claimed plurality of dummy source structures recited in Claim 1.

(a) Petitioner Has Not Shown That Tessariol’s Conductive Vias Are “Dummy Source Structures” and, Moreover, the Conductive Vias Do Not “Surround” a Staircase Contact (Limitation [1.e])

170. Petitioner has not shown that Tessariol’s conductive vias 58 are “dummy source structures” under proper construction of the term.

171. Tessariol’s conductive vias 58 are also not “dummy source structures” per the limitation of [1.e] because they do not “surround” the alleged staircase contact.

172. Indeed, Petitioner does not even allege that this requirement is met by the conductive vias 58.

(i) Petitioner Does Not Show That Tessariol's Conductive Vias Are "Dummy Source Structures" Under Proper Construction of the Term (Limitation [1.e])

173. Petitioner does not show that Tessariol's conductive vias 58 are "dummy source structures" because, under the proper construction of the term, Petitioner has not shown that conductive vias 58 are structures that do not function as a source to memory cells. *See* §VIII.A. Accordingly, Petitioner has not shown that Tessariol discloses limitation [1.e].

(ii) Tessariol's Conductive Vias Do Not "Surround" the Alleged Staircase Contacts (Limitation [1.e])

174. Tessariol's conductive vias 58 also do not "surround" the alleged staircase contact as required by limitation [1.e].

175. Indeed, Petitioner does not even allege that conductive vias 58 satisfy this requirement. Pet. 87-88.

176. Limitation [1.e] requires "the plurality of dummy source structures" to be "surrounding the staircase contact." As I discuss in §VIII.B, this requires that the dummy source structures are on more than just two sides of the staircase contact, and it is insufficient for a staircase contact to be merely "between" two dummy source structures.

177. Tessariol's conductive vias 58 do not "surround" the alleged staircase contact (conductive vias 80), and indeed are not even in the same region as the alleged staircase contact. As Petitioner acknowledges, "conductive vias 58 are in

located region 51.



conductive vias 80 in region 50.

“surround” the alleged staircase contact. Pet., 86.

180. As shown in the figure below, Petitioner maps only **dummy structures 60**² to this limitation, not **conductive vias 58**:

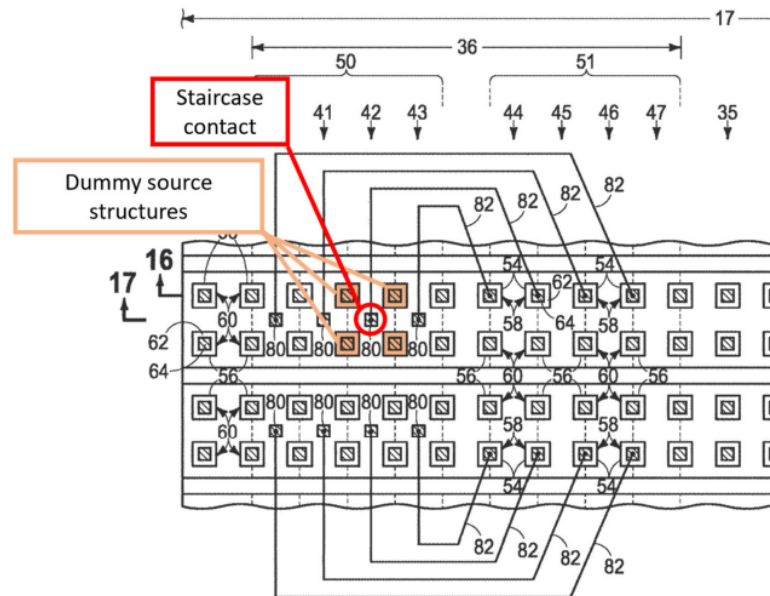


FIG. 15

181. Tessariol, Fig. 15 (annotated by Petitioner at Pet. 88). Petitioner does allege that the conductive vias surround the alleged staircase contact (conductive vias 80). Pet. 87-88.

182. Thus, Tessariol’s conductive vias 58 do not “surround” the alleged staircase contact as required by limitation [1.e].

² The **dummy structures 60** do not satisfy other requirements of the claimed “plurality of dummy source structures.” See §X.A.

(b) Tessariol's Dummy Structures Do Not Disclose or Render Obvious Dummy Source Structures Comprising a "Conductive Contact" (Limitation [1.f])

183. Tessariol's dummy structures 60 also do not meet the requirements for the claimed "plurality of dummy source structures."

184. Specifically, Tessariol's dummy structures 60 do not meet at least the requirement of limitation [1.f] that the dummy source structures must comprise a "conductive contact" because Petitioner has not shown that a dummy structures 60 in Tessariol has a conductive structure that permits current flow with an adjoining conductive structure.

185. Petitioner's argument that a POSITA would have modified Tessariol to connect dummy structures 60 to upper-level interconnects relies on conclusory motivation and is contradicted by Tessariol.

(i) Tessariol's Dummy Structures Do Not Comprise a "Conductive Contact" Under the Proper Construction (Limitation [1.f])

186. Petitioner has not shown that Tessariol's dummy structures 60 include a "conductive contact" because Petitioner has not shown that a dummy structure 60 in Tessariol has a conductive structure that permits current flow with an adjoining conductive structure, as required under the proper construction of "conductive contact" (§VIII.C).

187. Claim 1 requires that “each of the dummy source structures comprises a conductive contact.” As I explain in Section VIII.C, “conductive contact” means a conductive structure that permits current flow with an adjoining conductive structure. For example, the ’872 patent shows dummy source structures 246, which are made with conductive material, extending vertically through a staircase structure and an insulation layer to form an exposed conductive contact 244. Ex. 1001, 11:37-39, 16:21-32, 16:63-66.

188. This conductive contact enables the dummy source structure to “function as an interconnect to connect 3D memory device 100 with other peripheral devices” (id., 16:63-66), and in view of this connection, the conductive contact is a conductive structure that permits current flow with an adjoining conductive structure, as required by the proper construction.

189. In contrast, Petitioner has not shown that the dummy structure 60 in Tessariol is a conductive structure that permits current flow with an adjoining conductive structure. I will describe the various sides of the structure as follows.

190. On the sides (e.g. the left and right side of the image as seen in the images disclosed in Tessariol), Tessariol’s dummy structures 60 are covered by an insulating lining 62. Tessariol, [0038], Fig. 16. This insulating liner 62 will reduce or eliminate any electrical conduction paths between structures immediately adjacent to dummy structures 60 (for example, it will reduce or eliminate electrical

conduction through the dummy structure 60 between the stacked layers of conductive material 72).

191. On the top (e.g. top of the image as seen in the images disclosed in the Tessariol), Tessariol's dummy structures 60 do not connect to upper-level interconnects, and instead are covered by insulating material 86. *Id.*, [0046], Fig. 16.

192. On the bottom (e.g. the bottom as seen in the images disclosed in Tessariol) the bottoms of Tessariol's dummy structures 60 land on layer 14. Layer 14 is specified as "conductively-doped source material 14 (e.g., conductively-doped semiconductor material)." *Id.* [0027]. As I have discussed in an earlier declaration (*see* Exhibit 2001) simply landing on a "conductively doped source material" is insufficient to demonstrate that a dummy structure 60 in Tessariol is a conductive structure that permits current flow with an adjoining conductive structure, as required under the proper construction of "conductive contact."

193. In order for the structure to have a conductive contact, special processing (e.g. the semiconductor must be highly-doped with an appropriate species to match the work function of the metal) is required. See also my prior declaration in this proceeding dated July 29, 2024 at ¶¶39-54. As such, a POSITA would not consider the mere description of a metal contacting a semiconductor (e.g. as illustrated in Tessariol Figure 9) to meet the conditions for a "conductive contact" as outlined in '872 patent.

194. Moreover, although Tessariol discloses conductive via 58 as being electrically coupled to one of lines 66 as, “For example, and by way of example only, FIG. 9 shows some alternate ones of operative conductive vias 58 directly electrically coupling to individual conductive lines 66 through source material 14, conductive material 13, and conductive vias 67” ([0039]) there are several issues in applying this disclosure for conductive via 58 to dummy structures 60. First, various depictions of this construction (for example, Fig. 9) illustrate source material 14 in this configuration as being isolated from (and thus not necessarily the same) as source material 14 elsewhere. Second, Tessariol both locates conductive via 58 in a different part of the structure than dummy structure 60, and describes the processing on conductive via 58 differently than dummy structure 60; thus making it inappropriate to assume the structures are identical with respect to layer 14. For example, localized doping regions are used in semiconductor substrates, which makes it inappropriate to assume that the properties of the region under dummy structure 60 would meet the requirements for a conductive contact merely because of operative conductive vias 58 located in a different region of the device. *See Shur* (Ex. 2003) pg. 25 and *Streetman* (Ex 2004) pg. 16-17.

195. Indeed, Petitioner has provided no argument in its Petition that there is a conductive contact with the insulating lining 62, insulating material 86, or source

material 14. Accordingly, Petitioner has not shown that Tessariol's dummy structures comprise a "conductive contact," as required by claim limitation [1.f].

(ii) A POSITA Would Not Have Been Motivated to Couple Tessariol's Dummy Source Structures to Upper-Level Interconnect Lines (Limitation [1.f])

196. Petitioner does not show that a POSITA would have been motivated to modify Tessariol's dummy structures to contact upper-level interconnect lines.

197. Petitioner appears to recognize that Tessariol does not disclose a "conductive contact" in relation to its dummy structures, and so Petitioner makes a conclusory assertion that because Tessariol's conductive vias can couple to upper-level interconnects, it would have been obvious that Tessariol's dummy structures "can" also contact upper-level interconnects. Pet., 90-91.

198. Regardless, Petitioner has not shown that a POSITA would have been motivated to modify Tessariol's dummy structures to couple to upper-level interconnects, as alleged. Indeed, Dr. Banerjee concedes that there is no need for such a modification.

199. As Dr. Banerjee explains, unlike the conductive vias, "interconnects 82 are simply not made on the dummy structures, because there is no need for them to connect to upper-level devices." Ex. 1003 ¶216. I agree with Dr. Banerjee on this point with regards to Tessariol. Saying this another way, the architecture disclosed in Tessariol has isolated the conductive via function to conductive vias 58, which are neither described nor depicted as surrounding the staircase contacts (staircase

contacts are conductive vias 80). Unfortunately, Dr. Banerjee’s initial admission (which I agree with) contradicts his subsequent assertion that “[i]t would therefore have been obvious to a POSITA that dummy source structures 60 can include a contact that could connect to an upper-level interconnect.” *Id.* Overall, I disagree with Dr. Banerjee’s subsequent assertion, as he has not shown that there would be any functional benefit to adding the proposed connection.

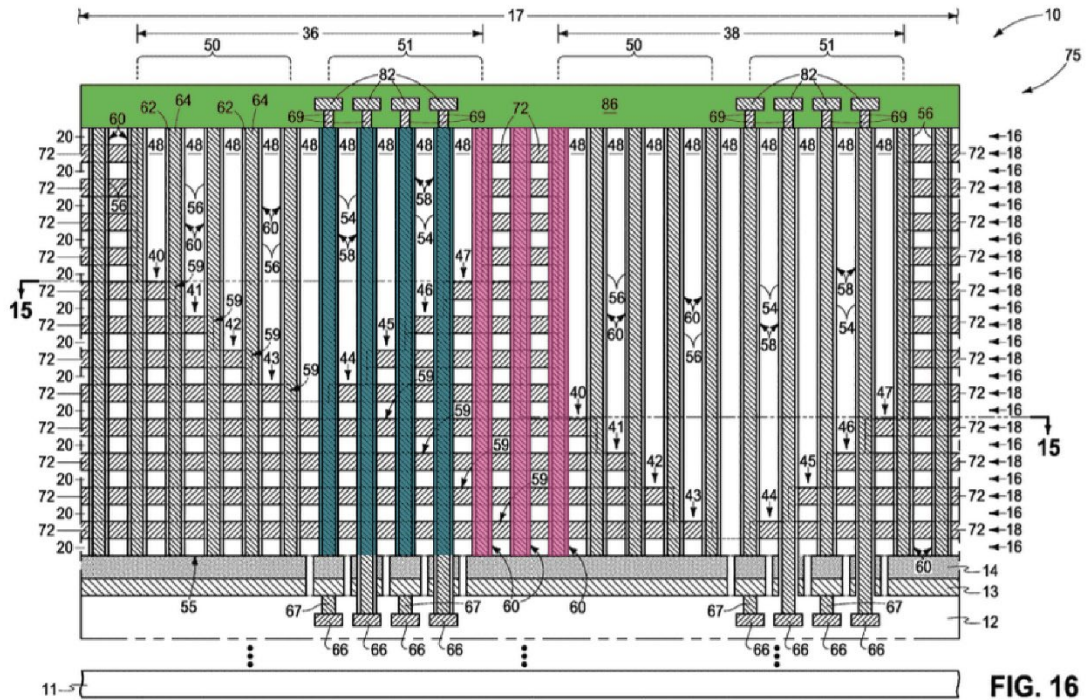
200. Dr. Bannerjee asserts that the proposed modification “reduces time and process steps” (*id.*), but this argument is based on nothing more than conclusory expert testimony. Ex. 1003, ¶¶204, 216. Neither Petitioner nor Dr. Banerjee provides any explanation for how this modification would save process steps—because it would not.

201. Instead, a POSITA would not have been motivated to modify Tessariol’s dummy structures to contact upper-level interconnects because this modification would not eliminate any process steps. As best, this modification would repurpose existing process steps. Petitioner’s only theory is that “dummy structures 60 and operative conductive vias 58 may ... be formed simultaneously” to “save time and process steps,” but Tessariol already discloses that conductive vias 58 and dummy structures 60 are formed “at the same time” in a process that does not include connecting the upper level-interconnects to dummy structures 60. Tessariol, [0038], Fig. 16. Since Tessariol already discloses the simultaneous

formation of dummy structures 60 and operative conductive vias 58, and since Tessariol already discloses upper-level interconnect lines (82), there is no saving in fabrication time or manufacturing costs to also connect the dummy source structures 60 to an upper-level interconnect 82. (In practice, this type of change would be accomplished by changing the mask that supports the upper-level interconnects 82, which would be an added cost, not a cost saving). Overall, there is no saving in fabrication time or manufacturing costs which would motivate a POSITA to add connections between dummy source structures 60 and upper-level interconnects 82.

202. Thus, this alleged reduction in steps does not result from Petitioner's proposed modification and would not have motivated the modification.

203. As shown below in Figure 16 (below), Petitioner's proposed modification would instead complicate the circuit design, because the additional features would need to be deposited above dummy source structures 60, which introduces additional opportunities for manufacturing defects.



204. Moreover, the same insulating material that covers the dummy structures 60 without interconnects (see above) would still need to be deposited to fill the areas surrounding any added interconnects. So even if it were possible to add an interconnect to the dummy structures, Petitioner has not identified any motivation for a POSITA to add upper-level interconnects to the top of the non-functional dummy structures 60.

205. Thus, Petitioner has not shown that Tessariol discloses or renders obvious that the alleged “dummy source structures” comprise a “conductive contact.”

B. Claim 3: Tessariol's Dummy Structures Are Not Nominally Equal Lateral Distance to the Staircase Structure

206. Tessariol discloses “at least two of the plurality of dummy source structures are of nominally equal lateral distances to the staircase contact” as required by Claim 3 because Petitioner’s reliance on Tessariol’s Fig. 15 is insufficient to show that the claimed distance-based requirement is satisfied.

207. Petitioner points to Tessariol’s Fig. 15 as purporting to show uniform distribution, but Fig. 15 does not include a scale, dimensions, or any other means to measure distances between components. Pet., 93.

208. Petitioner does not annotate Figure 15 to attempt to show the relative distances, but even if Petitioner had done so, such arguments would be insufficient.

209. Finally, Petitioner does not argue that it would have been obvious to modify Tessariol such that the alleged dummy structures are of nominally equal lateral distances to the alleged staircase contact.

210. Accordingly, Tessariol does not disclose or render obvious Claim 3 in my opinion.

C. Claim 4: Tessariol's Dummy Structures Are Not of Nominally Equal Lateral Distances to the Staircase Contact

211. For the same reasons explained above for Claim 3, Petitioner’s reliance on Figure 15 is insufficient to show that that the plurality of purported dummy source structures are of “nominally equal” lateral distances to the purported staircase

contact. *See* §XI.B. Petitioner merely points to previous sections in the Petition and provides no new illustrations or arguments for this claim.

II. CONCLUSION

212. For at least the reasons discussed above, it is my opinion that Petitioner has not demonstrated that any of the Challenged Claims of the '872 patent are anticipated or obvious.

213. This declaration represents my opinions that I have formed to date on the specific issues for which I have been asked to opine and based on the material currently available to me. I reserve the right to supplement this declaration to address any new information offered by Petitioner or provided by the Board. Also, I reserve the right to supplement this declaration insofar as Petitioner is permitted to supplement the record with any additional opinions or arguments.

214. I hereby declare that all statements made herein of my own knowledge are true and all statements made herein on information and belief were and are believed by me to be true, and that all statements herein were and are made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code and that any such willful false statements may jeopardize the validity of the application or any patents issued thereon.

APPENDIX A

CURRICULUM VITAE
Dr. Kelin J. Kuhn

CONTACT INFORMATION:

Kelin J. Kuhn
P.O. Box 609
Winthrop, WA 98862
kjkuhn@confluence-tech.com

EDUCATION:

Ph.D., Electrical Engineering, Stanford University, Stanford, CA. June 1985
M.S., Electrical Engineering, Stanford University, Stanford, CA. June 1985
B.S., Electrical Engineering, University of Washington, Seattle, WA. March 1980
(magna cum laude)

PRESENT ROLE:

**Confluence Technology Services, Winthrop, WA (kjkuhn@confluence-tech.com);
present role**

Dr. Kuhn's business (Confluence Technology Services) supports a variety of engineering services in electronics and photonics, with emphasis on CMOS and beyond-CMOS technologies.

**Cornell University, Ithaca, NY; Materials Science and Engineering (kjk236@cornell.edu)
2014 to date**

Position: Adjunct Professor
Key Collaborator: Darrell Schlom

Prof. Kuhn's role is collaborating with a diverse group of faculty (both at Cornell and elsewhere) for establishment of long-term research programs in the area of valleytronics, inverse-design, quantum materials, post-CMOS technology, and spintronics.

CLIENTS / SIGNIFICANT INTERACTIONS POST-2014:

Bayes PLLC: Initiated 2024 and on-going. Technical evaluation and consulting on matters related to *Inter Partes Review of U.S. Patent Nos. 8,803,214 And 10,475,737*.

Pillsbury Winthrop Shaw Pittman LLP: Initiated 2024 and on-going. Technical evaluation and consulting on matters related to *MicroSemi Corporation v. Commissioner of Internal Revenue*.

Ropes and Gray: Initiated 2023 and on-going. Technical evaluation and consulting on the matters related to *Yangtze Memory Technologies Company, LTD. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC, Case No. 5-23-cv-05792*.

Heim, Payne & Chorush: Initiated 2023 and on-going. Technical evaluation and consulting representing *Microchip Corporation* and its subsidiary *Silicon Storage Technology, Inc.* with regards to a dispute with *Taiwan Semiconductor Manufacturing Company*.

Smith Baluch LLP: Initiated 2022 and on-going. Technical evaluation and consultation to advise and assist Smith Baluch LLP matters relating to semiconductor processing.

Carter Arnett: Initiated 2022 and ongoing. Technical evaluation and consultation to advise and assist Carter Arnett PLLC in representing *Katana Silicon Technologies, LLC* in IPR2022-00763 and litigation related to Case No. 6:22-cv-00191 (W.D. Tex), adverse to *GlobalFoundries, Inc., GlobalFoundries, U.S. Inc., and GlobalFoundries U.S. 2 LLC*.

Mintz: Completed 2022-2023. Technical evaluation and consulting representing *Daedalus Prime LLC* with regards to the ITC Case: 337-TA-133, Certain Semiconductor Devices, Mobile Devices Containing Same (Taiwan Semiconductor Manufacturing Company).

Heim, Payne & Chorush: Completed 2021-2023. Technical evaluation and consulting representing *Arigna Technology Limited* with regards to IPR2021-01321 (*Volkswagen*) and IPR2021-01382 (*Infineon*).

Quinn Emanuel Urquhart & Sullivan: Believed complete 2021-2023. Technical evaluation and consulting representing *Hanwha* with regards to ITC Inv. No. 337-TA-1271.

Ropes and Gray: Completed 2021-2023. Technical evaluation and consulting in the matter of *Godo Kaisha IP Bridge 1 v. Micron Technology et al.*

Lawrence and Phillips: Completed 2021-2022. Technical evaluation and consulting in the matter of *Acorn Semi, LLC v. Samsung Electronics et al.* with regards to *inter partes* reviews (IPRs) filed by Samsung.

Wolf Greenfield: Completed 2020-2023. Technical evaluation and consulting in the matter of *Godo Kaisha IP Bridge 1 v. Micron Technology et al.* with regards to *inter partes* reviews (IPRs) filed by Micron.

Hueston Henningan: Completed 2020-22. Technical evaluation and consulting in the matter of *Acorn Semi, LLC v. Samsung Electronics et al.*

Skadden Arps: Initiated 2020 and on-going. Technical consulting for the *Audit Committee of the Intel Board of Directors* on matters related to Technology Development.

PARADIM: Initiated 2016 and on-going. PARADIM's mission is to create new interface materials with unprecedented properties for the next generation of electronic devices. Dr. Kuhn

is a member of the External Advisory Committee. In this role, Dr. Kuhn provides technical and management support with regards to PARADIM operations.

Quinn Emanuel Urquhart & Sullivan: Completed, 2020-2021. Technical evaluation and consulting in the matter of *Godo Kaisha IP Bridge 1 v. Micron Technology et al.*

Susman Godfrey: Completed 202-2023. Technical evaluation and consulting with regards to *Arigna Technology Limited* on matters related to CMOS transistor design.

Womble Bond Dickinson: Completed, 2020. Technical consulting for KIPB LLC (formerly KAIST IP US LLC) on an *ex parte reexamination* (“EPR”) proceeding in the United States Patent and Trademark Office with regards to patent 6,885,055.

Womble Bond Dickinson: Completed, 2019-2020. Technical evaluation and consulting in the matter of *KIPB LLC v. Samsung Electronics et al.* Dr. Kuhn supported this litigation for the plaintiff as an expert witness, including completion of the Infringement and Rebuttal Reports, as well as completing a deposition conducted on the contents of the Infringement and Rebuttal Reports. This case was settled out of court in September 2020.

Lathrop Gage: Completed, 2018-2020. Technical evaluation and consulting for KIPB LLC (formerly KAIST IP US LLC) on Korean Patent 10-0458288 (Korean counterpart to US 6,885,055).

Ropes & Gray: Completed, 2018. Technical evaluation and consulting in the matter of *Godo Kaisha IP Bridge 1 v. Qualcomm Inc. et al.*

GlaserWeil: Completed, 2016-2018. Technical evaluation and consulting in the matter of *KAIST IP US LLC v. Samsung Electronics Co., Ltd., Case No. 2:16-cv-01314*. Dr. Kuhn supported this litigation for the plaintiff as an expert witness. This included IPR proceedings (a total of 6 IPRs were presented to the PTO in this case). This also included completion and submission of the Claim Construction Declaration, the Infringement Report, and the Rebuttal Report, as well as depositions conducted on the contents of these Reports. This case went to trial June 11-15, where Dr. Kuhn presented both Direct testimony on infringement (6/12/18) and Rebuttal (6/14/18) testimony on validity.

yoR Labs Inc.: Completed. 2015-2017. yoR Labs is a medical instrumentation start-up, focusing on non-invasive medical imaging instrumentation. Dr. Kuhn served first as a member of the External Advisory Committee and later as a member of the Board of Directors. In this role, Dr. Kuhn provided technical and management support with regards to yoR labs operations.

Oregon State University, Department of Electrical Engineering and Computer Science: Completed. 2015 to 2018: Professor-courtesy. Prof. Kuhn’s role was establishment of long-term research programs in the area advanced CMOS technology and post-CMOS technology.

FORMER ROLES (2014 and PRIOR)

Intel, Portland, OR, (advanced development / research) 2008-2014 (retired in 2014)

Grade level: 12 (Fellow)

Manager: Mike Mayberry, VP

Dr. Kuhn's role was researching advanced device architectures for Intel processes in the 5-10 year time frame. While much of her work as an Intel Fellow remains proprietary, some of the public domain aspects are captured in her book *CMOS and Beyond: Logic Switches for Terascale Integrated Circuits* (Cambridge, 2015) and her paper "Considerations for Ultimate CMOS Scaling," (IEEE Trans. on Elec. Dev., Vol: 59, No: 7, 2012, pp. 1813 – 1828 which won the Paul Rappaport Award). She received an Intel IAA in 2008 for her work on the TriGate transistor.

Intel, Portland, OR, (45nm Device technology manager in pathfinding) 2004-2008

Grade level: 10/11 (Principal Engineer / Sr. Principal Engineer)

Manager: Mark Bohr, Senior Intel Fellow / Kaizad Mistry, VP

Dr. Kuhn's role was as device technology manager of the pathfinding team responsible for the high-k metal-gate transistor architecture for Intel's 45nm microprocessor processor technology. She received an Intel IAA in 2006 for her work on high-k metal-gate.

Intel, Portland, OR, (90nm communication process manager) 2001-2004+

Grade level: 9/10 (Sr. Engineer / Principal engineer)

Manager: Scott Thompson (was Intel Fellow at the time, now a professor at Univ. of Florida).

Dr. Kuhn's role in this time frame was Process Program Manager of the team responsible for Intel's 90nm communications process technology. Over a 4-year period, this team developed a derivative analog/RF technology (including a SiGe BJT) on top of Intel's premium 90nm microprocessor process.

Other Intel experience:

Intel, Portland, OR, (130nm front-end integration engineer) 1998-2001

Intel, Portland, OR, (0.35um front-end integration engineer) 1997-1998

Grade level: 7-9 (Sr. engineering grades)

During the 130nm generation, Dr. Kuhn was an integration engineer responsible for the isolation section of the flow. 130nm was the last of the "classic" CMOS generations, and her work in that generation was updating the isolation process. She had the satisfaction of watching the work she did in the 130nm successfully scale through 90nm, 65nm, 45nm, and 32nm, with little change in the base process.

Dr. Kuhn joined Intel on the 0.35um generation as a sustaining integration engineer in F15. She was responsible for the silicide section of the flow. Additionally, she participated in the DIVD camera chip project (Intel's historical project to build CMOS camera chips).

Other relevant experience:

Univ. of Washington, Seattle, WA (Assoc. Prof., Ass't. Prof., Res. Ass't. Prof.), 1987-1997

Dr. Kuhn held faculty positions at the University of Washington (in Seattle) for roughly a decade in the order of Research Assistant Professor (Materials Science and Engineering), Assistant Professor (Electrical and Computer Engineering), and Associate Professor (Electrical and Computer Engineering). She left the University in 1997 as a tenured Associate Professor of Electrical and Computer Engineering. While at the Univ. of Washington, she achieved distinction in both research and teaching.

Highlights include:

- University of Washington, Distinguished Teaching Award, 1995 (UW's highest level of achievement for a faculty member)
- NSF Presidential Young Investigator award, 1991-6 (The National Science foundation is the most prestigious funding agency for faculty and the NSF PYI award is the most prestigious national level award for junior faculty).
- Single-author on a textbook, Laser Engineering, Prentice-Hall, 1998, ISBN 0-02-366921-7 (this is a mezzanine text discussing the theory and practice of building conventional and diode laser systems).

BOOKS

Laser Engineering, (sole author) Prentice-Hall, 1998, ISBN 0-02-366921-7

CMOS and Beyond: Logic Switches for Terascale Integrated Circuits (Co-editor with Prof. Tsu-Jae King Liu, Cambridge Press, 2015, ISBN 978-1107043183).

BOOK CHAPTERS

“The Magic of MOSFET Manufacturing,” Chapter in the 75th Anniversary of the Transistor, Wiley-IEEE Press, July 2023, ISBN: 978-1-394-20247-8.

Chapter 1, CMOS and Beyond CMOS: Scaling Challenges” (Book title: “High Mobility Materials for CMOS Applications”, Woodhead Publishing Series in Electronic and Optical Materials, Elsevier, June 2018, ISBN 9780081020616) .

AWARDS:

Elected to the National Academy of Engineering (2023)
IEEE Frederik Philips Award (2016)
IEEE Paul Rappaport Award (2013)
IEEE Fellow (2011)

Intel Achievement Awards (Intel's highest technical award): IAA 2006 (for HiK-MG) and IAA 2008 (for key contributions to Intel's 22nm TriGate technology)

Intel Divisional Awards: Turbo operation (2009), RF Vccmin (2007), TCC (2005), SCD 1213.4 SCD/ICG (2004), LAD NW/Ophir A-1 (2003), SiGe BJT (2002), Hitachi etch (2002), 2um2SRAM (2001), Gamma Test chip (2000), Certification P854.6 (1999), F15 ISO 9000 (1998)

Academic Engineer of the Year Award, Puget Sound Engineering Council, 1996

University of Washington, Distinguished Teaching Award, 1995

College of Engineering, Outstanding Faculty Achievement Award, 1994

NSF Presidential Young Investigator award, 1991-6

NSF Research Initiation Award, 1989-91

IBM Graduate Fellowship, 1983-5

Hertz Graduate Fellowship, 1982-3

National Merit Scholar, 1976-80

JOURNAL PUBLICATIONS:

49. "First principles modeling of defects in the $\text{Al}_2\text{O}_3/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ system", G. Greene-Diniz, K. Kuhn, P. Hurley, and J. Greer, *J. Appl. Phys.*, Vol. 121, No. 7, Jan. 2017.
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1. Implementation of distributed microprocessor systems in custom heavy trucks. Kuhn, K.J. In: Wescon/80 Conference Record. El Segundo, CA, USA: Electron. Conventions, 1980. p. SS2-3/1-8 Conference Paper.

PATENTS

	PAT. NO.	Title
1	11,302,777	Integration methods to fabricate internal spacers for nanowire devices
2	11,195,919	Method of fabricating a semiconductor device with strained SiGe fins and a Si cladding layer
3	11,139,400	Non-planar semiconductor device having hybrid geometry-based active region
4	11,024,714	Nanowire transistor fabrication with hardmask layers
5	10,991,799	Silicon and silicon germanium nanowire structures
6	10,825,752	Integrated thermoelectric cooling
7	10,804,357	Integration methods to fabricate internal spacers for nanowire devices
8	10,636,871	Silicon and silicon germanium nanowire structures
9	10,593,804	Non-planar semiconductor device having hybrid geometry-based active region
10	10,586,868	Non-planar semiconductor device having hybrid geometry-based active region
11	10,580,899	Nanowire structures having non-discrete source and drain regions
12	10,580,860	Integration methods to fabricate internal spacers for nanowire devices
13	10,535,770	Scaled TFET transistor formed using nanowire with surface termination
14	10,424,580	Semiconductor devices having modulated nanowire counts
15	10,283,589	Integration methods to fabricate internal spacers for nanowire devices
16	10,121,861	Nanowire transistor fabrication with hardmask layers
17	10,121,856	Integration methods to fabricate internal spacers for nanowire devices
18	10,115,822	Methods of forming low band gap source and drain structures in microelectronic devices
19	10,109,711	CMOS FinFET device having strained SiGe fins and a strained Si cladding layer on the NMOS channel
20	10,074,573	CMOS nanowire structure
21	10,074,357	Integrated acoustic phase array
22	10,026,829	Semiconductor device with isolated body portion
23	9,978,636	Isolated and bulk semiconductor devices formed on a same bulk substrate
24	9,947,805	Nanowire-based mechanical switching device
25	9,935,205	Internal spacers for nanowire transistors and method of fabrication thereof
26	9,935,107	CMOS FinFET device with dual strained cladding layers on relaxed SiGe fins, and method of fabricating the same
27	9,926,193	Magnetic nanomechanical devices for stiction compensation

28	9,911,835	Tunneling field effect transistors (TFETs) for CMOS architectures and approaches to fabricating N-type and P-type TFETs
29	9,893,167	Integration methods to fabricate internal spacers for nanowire devices
30	9,882,053	Molded dielectric fin-based nanostructure
31	9,859,368	Integration methods to fabricate internal spacers for nanowire devices
32	9,825,130	Leakage reduction structures for nanowire transistors
33	9,812,524	Nanowire transistor devices and forming techniques
34	9,691,843	Common-substrate semiconductor devices having nanowires or semiconductor bodies with differing material orientation or composition
35	9,680,013	Non-planar device having uniaxially strained semiconductor body and method of making same
36	9,673,302	Conversion of strain-inducing buffer to electrical insulator
37	9,614,060	Nanowire transistor with underlayer etch stops
38	9,608,059	Semiconductor device with isolated body portion
39	9,595,581	Silicon and silicon germanium nanowire structures
40	9,583,602	Tunneling field effect transistors (TFETs) for CMOS architectures and approaches to fabricating N-type and P-type TFETs
41	9,583,491	CMOS nanowire structure
42	9,564,522	Nanowire structures having non-discrete source and drain regions
43	9,559,160	Common-substrate semiconductor devices having nanowires or semiconductor bodies with differing material orientation or composition
44	9,508,796	Internal spacers for nanowire transistors and method of fabrication thereof
45	9,484,447	Integration methods to fabricate internal spacers for nanowire devices
46	9,472,613	Conversion of strain-inducing buffer to electrical insulator
47	9,425,212	Isolated and bulk semiconductor devices formed on a same bulk substrate
48	9,412,872	N-type and P-type tunneling field effect transistors (TFETs)
49	9,385,221	Nanowire transistor with underlayer etch stops
50	9,362,074	Nanowire-based mechanical switching device
51	9,355,242	Method and apparatus for managing and accessing personal data
52	9,343,559	Nanowire transistor devices and forming techniques
53	9,287,576	Self-powered internal medical device
54	9,258,114	Quantum key distribution (QSD) scheme using photonic integrated circuit (PIC)
55	9,224,810	CMOS nanowire structure
56	9,183,829	Integrated acoustic phase array

57	9,129,829	Silicon and silicon germanium nanowire structures
58	9,129,827	Conversion of strain-inducing buffer to electrical insulator
59	9,105,344	Shut-off mechanism in an integrated circuit device
60	9,087,863	Nanowire structures having non-discrete source and drain regions
61	9,064,944	Nanowire transistor with underlayer etch stops
62	9,029,221	Semiconductor devices having three-dimensional bodies with modulated heights
63	9,012,284	Nanowire transistor devices and forming techniques
64	8,890,120	Tunneling field effect transistors (TFETs) for CMOS approaches to fabricating N-type and P-type TFETs
65	8,853,741	Junctionless accumulation-mode devices on decoupled prominent architectures
66	8,766,372	Copper-filled trench contact for transistor performance improvement
67	8,753,942	Silicon and silicon germanium nanowire structures
68	8,558,279	Non-planar device having uniaxially strained semiconductor body and method of making same
69	8,507,948	Junctionless accumulation-mode devices on prominent architectures, and methods of making same
70	8,487,348	Methods and apparatus to reduce layout based strain variations in non-planar transistor structures
71	8,269,283	Methods and apparatus to reduce layout based strain variations in non-planar transistor structures
72	8,258,057	Copper-filled trench contact for transistor performance improvement
73	7,999,607	Power switches having positive-channel high dielectric constant insulated gate field effect transistors
74	7,888,710	CMOS fabrication process utilizing special transistor orientation
75	7,737,770	Power switches having positive-channel high dielectric constant insulated gate field effect transistors
76	7,312,485	CMOS fabrication process utilizing special transistor orientation
77	6,627,506	Thin tensile layers in shallow trench isolation and method of making same
78	6,368,931	Thin tensile layers in shallow trench isolation and method of making same
79	4,617,669	Method and apparatus for pumping laser slabs
80	4,563,763	Method and apparatus for cooling a slab laser

INVITED TECHNICAL PRESENTATIONS/SEMINARS :

Invited panel, IEDM, Variation and the End of the World, December, 2013.

Keynote, The End of Scaling?, ICTC, December 2013.

Invited seminar, CMOS and Beyond, Portland State University, October, 2013.

Keynote panel, CMOS and Beyond: Future Device Technology, ENF 2013, Ireland, June 2013.

Invited seminar, CMOS and Beyond: Future Device Technology for the Mobile World, IDF, May 2013.

Invited Workshop, The Future is Already Here: Evolving Concepts in Device and Materials Technology, AMAT, March 2013.

Invited paper, "The Ultimate CMOS Device and Beyond," IEDM 2012, San Francisco.

Invited talk, Beyond Simply Small: Progress in Advanced Transistor Architectures, Cornell, November 2012.

Invited seminar, Demystifying Moore's Law How it Really Works!, IDF, Sept. 2012, San Francisco.

Invited talk, The Ultimate CMOS Device and Beyond, Ireland, April 2012.

Keynote: "MOS scaling for the 22nm node and beyond: Device physics and technology," April 24, 2011, Taiwan, VLSI-TSA

Plenary: "Moore's Crystal Ball: Device Physics and Technology Past the 15nm Generation," INFOS 2011 (June 22, 2011, France)

Keynote: "Beyond the Planar Transistor: Progress in Next Generation Switches," Int'l Symposium on Adv. Gate. Stack Technology, Oct. 19-21, 2011 New York

Invited seminar - "Polishing Moore's Crystal Ball: Advanced Transistor Architectures ...and Beyond," K. Kuhn, March 30th. 2011, MIT, MTL seminar series.

Invited seminar - "Emerging Devices: Moore's Law and Advanced Transistor Architectures," K. Kuhn, Varian Technology Symposium, March 31st. 2011.

Keynote: "Scaling Electronics:Trends and Bottlenecks," K. Kuhn, April 4th. 2011, MIT Microphotonics meeting.

Invited seminar - "Gazing into Moore's Crystal Ball: Transistor Scaling after the 15nm node," K. Kuhn, Feb. 17th, 2010, Berkeley.

IEDM 2010 Short Course chair for 15nm technology, December 2010.

Plenary: Past, Present and Future: SiGe and CMOS Transistor Scaling, ECS 2010, Oct. 10, Las Vegas, CA, USA.

Keynote: Peering into Moore's Crystal Ball, Transistor Scaling beyond the 15nm node, Int'l Symposium on Adv. Gate. Stack Technology, Sept. 29th, 2010; Albany, NY, USA.

Plenary: CMOS transistor scaling past 32nm and implications on variation, 2010 IEEE/SEMI Advanced Semiconductor Manufacturing Conference (ASMC), ASMC'2010, 11-13 July 2010, San Francisco, CA, USA

Keynote: Technology options for 22nm and beyond, K. Kuhn, 2010 International Workshop on Junction Technology (IWJT), IWJT'10, 10-11 May 2010, Shanghai, China, pp. 1-6.

Invited seminar: Next Steps in Moore's Law: Transistor Scaling for the 15nm node and beyond, Nikkei Electronics Symposium / June 29th, 2010.

Plenary - CMOS technology beyond 22nm, K. Kuhn, 12th IEEE International Workshop on Cellular Nanoscale Networks and Applications, CNNA 2010, February 3-5 Berkeley, California

Keynote - Transistor architecture: 45nm and beyond, K. Kuhn, Intel European Research and Innovation Conference, 8-10th September 2009, Leixlip, Co. Kildare.

Plenary - Moore's Law Past 32nm: The Challenges in Physics and Technology Scaling, K. Kuhn, Solid State Devices and Materials Conference (SSDM), September 18, 2009, Sendai, Japan.

Invited talk - CMOS scaling beyond 32 nm: challenges and opportunities, Kuhn, K.J., 2009 46th ACM/IEEE Design Automation Conference (DAC), 26-31 July 2009, San Francisco, CA, USA, Pages: 310-13 Published: 2009

Keynote - Variation in 45nm and Implications for 32nm and Beyond, K. Kuhn, NMI International Conference on CMOS Variability, 12th & 13th May 2009, London, UK.

Invited talk - Moore's law past 32 nm: future challenges in device scaling, Kuhn, K.J., 2009 13th International Workshop on Computational Electronics (IWCE 2009), 27-29 May 2009, Beijing, China, (IWCE 2009) Pages: 6 pp. Published: 2009

Invited – International Electron Device meeting – short course.
http://download.intel.com/pressroom/pdf/kkuhn/Kuhn_22nm_Device.pdf

Invited seminar - "45nm High-k + Metal Gate Logic Technology," K. Kuhn, May 2008, MIT, MTL laboratory.

Invited talk - Reducing variation in advanced logic technologies: approaches to process and design for manufacturability of nanoscale CMOS, Kuhn, K.J., 2007 IEEE International Electron Devices Meeting - IEDM '07, 10-12 December 2007, Washington, DC, USA, IEDM '07 Pages: 471-4

Invited seminar - "CMOS Transistor Architecture Challenges and Opportunities," K. Kuhn, September 2005, MIT, MTL laboratory.

Keynote - "Nanotechnology Challenges and Opportunities," K. Kuhn, January 2005, MIT, MTL laboratory.

Invited seminar - "Transistor Scaling and its Impact on Analog/RF Device Performance", Dr. Kuhn Kuhn, March 2005, Stanford University, invited seminar.

Invited seminar - "Advanced transistor architecture approaches and their implications for device and circuit performance," Dr. Kuhn Kuhn, Intel Fellow's Forum, October 2004.

Invited seminar - "Moore's Law meets Materials Science", Dr. Kuhn Kuhn, September 2004, University of Washington.

Invited seminar - "Centrino, convergence of computing and communications," November 2003, Dr. Kuhn Kuhn, Stanford University, invited seminar.

Invited seminar - "Challenges in the parallel development of the 90nm communications (121x) and microprocessor (1262) process technologies," Dr. Kuhn Kuhn, Intel Fellow's Forum, October 2003.

Invited seminar - "RF/analog integration with 90nm digital CMOS", Dr. Kuhn Kuhn, MIT invited seminar, March 2003

Invited seminar - "Femtosecond pulse laser technology", Dr. Kuhn Kuhn, Oregon State University, March 10, 1997.

Invited talk- "Symbolic Solvers and their impact on engineering education", Dr. Kuhn Kuhn, Fifth annual conference on the teaching of mathematics, Baltimore, Maryland, June 21, 1996.

KELIN J. KUHN: LISTING OF CASE WORK

Trial Experience:

ACORN SEMI, LLC, vs. SAMSUNG ELECTRONICS CO., LTD.; SAMSUNG ELECTRONICS AMERICA, INC.; SAMSUNG SEMICONDUCTOR, INC.; AND SAMSUNG AUSTIN SEMICONDUCTOR, LLC, Case No. 2:19-CV-00347-JRG EASTERN DISTRICT OF TEXAS, MARSHALL DIVISION. Validity: Enablement only. Settlement with Samsung on enablement before trial. I did not attend trial.

KIPB LLC v. SAMSUNG ELECTRONICS CO., LTD. et al., Case No.: 2:19-cv-0056-JRG-RSP. UNITED STATES DISTRICT COURT, EASTERN DISTRICT OF TEXAS, MARSHALL DIVISION. Opening Report and Rebuttal Report. Settlement with Samsung before trial. Trial cancelled.

KAIST IP US LLC v. SAMSUNG ELECTRONICS CO., LTD. et al., GLOBALFOUNDRIES, INC.; et al., and QUALCOMM INC. Case No.: 2:16-cv-01314-JRG-RSP UNITED STATES DISTRICT COURT, EASTERN DISTRICT OF TEXAS, MARSHALL DIVISION. Opening Report and Rebuttal Report. I presented Opening and Rebuttal at trial. Trial 6-11-18 to 6-15-18.

Deposition testimony:

Case No. AU:22-CV-00852-RP. Katana Silicon Technologies LLC -v- GlobalFoundries, Inc., et al. December 10, 2024. Opening and Validity.

ITC Inv. No. 337-TA-1336. Daedalus Prime LLC v. TSMC. July 18, 2023. Validity.

IPR2021-01321. Arigna Technology Limited v. Volkswagen, Inc. '867 patent. August 5, 2022

IPR2021-01382. Arigna Technology Limited v. Infineon Technologies AG. '867 patent. July 11, 2022.

Case No. 6:20-cv-178-ADA. IP Bridge v. Micron. September 17, 2021. Opening and validity.

IPR2020-01183, 01204, 01205, 01206, 01207, 01279 and 01282. Acorn v. Samsung. July 6-7, 2021

IPR2020-01007. IP Bridge v. Micron. '041 patent. May 18, 2021.

IPR2020-01008. IP Bridge v. Micron. '047 patent. May 3, 2021.

Case No. 2:19-CV-00347-JRG. Acorn v. Samsung IPRs. April 6-7, 2021. IPR

Case No. 2:19-CV-00347-JRG. Acorn v. Samsung. December, 26, 2020. Enablement.

Case No.: 2:19-cv-0056-JRG-RSP. KIPB LLC v. Samsung. August 3, 2020. Opening and validity.

Case No.: 2:16-cv-01314-JRG-RSP. KAIST v. Samsung. March 16, 2018. Opening and validity.

Case No.: 2:16-cv-01314-JRG-RSP. KAIST v. Samsung. November 2, 2017. Claim construction.

Reports/Declarations:

Case No. 01-21-0002-5445. TSMC v. SST. August 21, 2024. Trade secret Use.

IPR2024-00789. Yangtze v. Micro, U.S. Patent 10,861,872. July 29, 2024. POPR

Reexam No. 90/015,321. U.S. Patent No. 6,291,861. June 20th, 2024. Declaration/EPR.

Case No. 1:22-CV-852-RP. Katana v. GlobalFoundries. February 23rd, 2024. Validity

Case No. 1:22-CV-852-RP. Katana v. GlobalFoundries. December 20th, 2023. Infringement

Case No. 01-21-0002-5445. TSMC v. SST. July 21, 2023. Opposition to Motion to Compel.

ITC Inv. No. 337-TA-1336. Daedalus Prime LLC v. TSMC. July 18, 2023. Validity.

IPR2021-01321. Arigna Technology Limited v. Volkswagen, Inc. '867 patent. August 5, 2022

IPR2021-01382. Arigna Technology Limited v. Infineon Technologies AG. '867 patent. July 11, 2022.

Case No. 6:20-cv-178-ADA. IP Bridge v. Micron. September 10, 2021. Validity.

Case No. 6:20-cv-178-ADA. IP Bridge v. Micron. August 13, 2021. Opening.

IPR2020-01183, 01204, 01205, 01206, 01207, 01279 and 01282. Acorn v. Samsung. July 6-7, 2021

IPR2020-01007. IP Bridge v. Micron. '041 patent. February 28, 2021.

IPR2020-01008. IP Bridge v. Micron. '047 patent. February 28, 2021.

Case No. 2:19-CV-00347-JRG. Acorn v. Samsung IPRs. April, 21, 2020. IPR

Case No. 2:19-CV-00347-JRG. Acorn v. Samsung. December, 12, 2020. Enablement.

Case No.: 2:19-cv-0056-JRG-RSP. KIPB LLC v. Samsung. July 23, 2020. Opening and validity.

Case No.: 2:16-cv-01314-JRG-RSP. KAIST v. Samsung. 2018. Opening and validity.

Case No.: 2:16-cv-01314-JRG-RSP. KAIST v. Samsung. 2018. IPR.

Case No.: 2:16-cv-01314-JRG-RSP. KAIST v. Samsung. 2017. Claim construction