

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,
Patent Owner

Case No.: IPR2024-00789
U.S. Patent No. 10,861,872
Issue Date: December 8, 2020

Title: THREE-DIMENSIONAL MEMORY DEVICE AND METHOD
FOR FORMING THE SAME

**DECLARATION OF SANJAY BANERJEE, PH.D., IN SUPPORT OF
PETITIONER'S REPLY TO PATENT OWNER'S RESPONSE**

	<u>Page</u>
I. INTRODUCTION	4
II. COMPENSATION	5
III. MATERIALS CONSIDERED	5
IV. UNDERSTANDING OF THE GOVERNING LAW	8
V. CLAIM CONSTRUCTION	8
A. Dummy Source Structure	9
1. “Dummy Source Structure” Is the Structure that Occupies the Void Used for the Gate Line Replacement Process.....	13
2. The Specification Does Not Support PO’s Negative Limitation.....	22
B. Surrounding	28
C. Conductive Contact	33
VI. TESSARIOL	42
A. Claim 1	42
1. Tessariol’s Dummy Vias Disclose a “Conductive Contact”	42
2. Tessariol’s Dummy Vias Render Obvious a “Conductive Contact”	44
B. Claims 3 and 4.....	47
VII. PARK.....	49
A. Claim 1	49
1. Park’s Dummy and Common Source Lines Surround the Staircase Contact.....	49
2. Park’s Common Source Lines Are “Dummy Source Structures”.....	49
B. Claims 2 and 11	50
C. Claims 3 and 4.....	50
D. Claim 5	50
E. Claim 6	50

VIII. DECLARATION.....	51
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I. INTRODUCTION

1. My name is Sanjay Banerjee. I have been retained on behalf of Petitioner Micron Technology, Inc. (“Petitioner” or “Micron”) as an independent consultant in this proceeding before the United States Patent and Trademark Office (“USPTO”).

2. I have already submitted a declaration in this proceeding concerning technical subject matter relevant to the above-captioned *inter partes* review petition (“Petition”) of U.S. Patent No. 10,861,872 (Ex. 1001, the “’872 Patent”). My “Initial Declaration” is Ex. 1003.

3. A summary of my education, professional experience, and other qualifications is included within Paragraphs 5 to 14 in Ex. 1003 and in my CV (Ex. 1004).

4. I have been asked to review the Patent Trial and Appeal Board’s (the “Board”) Institution Decision, issued on October 25, 2024. I have also been asked to review Yangtze Memory Technologies Co., Ltd.’s (“Patent Owner” or “YMTC”) Patent Owner Response (“POR”), and the accompanying exhibits and declarations, and provide my opinions on some of the statements and arguments offered in YMTC’s materials.

5. In this “Reply Declaration,” I do not address every argument or opinion that appears in YMTC’s Patent Owner Response or Dr. Kuhn’s declaration with

which I disagree. Instead, I focus on arguments and opinions that are most likely to be relevant to the outcome of this proceeding. For this reason, the opinions that I express in this Reply Declaration are not exhaustive of my opinions regarding the unpatentability of claims 1-6 and 11-13 of the '872 patent. Importantly, the fact that I do not address a particular point or argument should not be understood to indicate an agreement or concession on my part. And, unless I state otherwise, the opinions I provide below apply equally to both YMTC's Patent Owner Response and Dr. Kuhn's declaration, such that any opinions concerning the Patent Owner Response apply to the corresponding section of Dr. Kuhn's declaration (and vice versa).

6. I have confined my analysis to the materials that were available when I prepared the Declaration. I reserve the right to supplement my Initial Declaration and this Reply Declaration in response to additional evidence that may come to light.

II. COMPENSATION

7. I am being compensated for my work in this matter at an hourly rate of \$650.00 for consulting services. My compensation is not based on the outcome of this matter or on the substance of my opinions.

III. MATERIALS CONSIDERED

8. In preparing this Reply Declaration, I reviewed and considered the following materials, along with any other materials referenced in the body of my Initial Declaration and this Reply Declaration:

Exhibit	Description
1001	U.S. Patent No. 10,861,872 B2 to Liu et al.
1002	File History of U.S. Patent No. 10,861,872 to Liu et al.
1005	U.S. Patent No. 9,859,297 B2 to Park et al. (“Park”)
1006	U.S. Patent Publ. No. 2019/0081061 A1 to Tessariol et al. (“Tessariol”)
1007	Aritome, “NAND Flash Memory Technologies” (2016)
1008	Silvagni, “3D NAND Flash Based on Planar Cells,” Computers 2017
1009	Micheloni et al., “Inside Solid State Drives (SSDs)” (2 nd Ed. 2018)
1010	U.S. Patent No. 10,381,369 B2 to Kim et al.
1011	U.S. Patent No. 10,475,737 B2 to Tang et al.
1012	Certified English Translation of Chinese Patent Application Publ. No. CN108766971 to Liu (“Liu”)
1013	Chinese Patent Application Publ. No. CN108766971 to Liu
1014	U.S. Patent No. 8,945,996 B2 to Tang et al.
1015	YMTC’s Exemplary Infringement Claim Chart for U.S. Patent No. 10,861,872 – (Ex. 49) 128L [PROTECTIVE ORDER MATERIAL – FILED UNDER SEAL]
1016	YMTC’s Exemplary Infringement Claim Chart for U.S. Patent No. 10,861,872 – (Ex. 50) 176L [PROTECTIVE ORDER MATERIAL – FILED UNDER SEAL]
1017	YMTC’s Exemplary Infringement Claim Chart for U.S. Patent No. 10,861,872 – (Ex. 51) 232L [PROTECTIVE ORDER MATERIAL – FILED UNDER SEAL]

Exhibit	Description
1018	Print out from Geographic Wiki, https://www.studycountry.com/wiki/what-is-a-piece-of-land-surrounded-by-water-on-2-side (last visited Mar. 28, 2024)
1019	U.S. Patent No. 9,530,492 to Lee
1023	Micheloni, “3D Flash Memories” (2016)
1031	Complaint for Patent Infringement, Dkt. No. 1, filed Nov. 9, 2023, in <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC</i> , Case No. 3:23-cv-05792-RFL
1032	First Amended Complaint for Patent Infringement, Dkt. No. 29, filed Feb. 2, 2024, in <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC</i> , Case No. 3:23-cv-05792-RFL
1033	Plaintiff and Counterclaim Defendant Yangtze Memory Technologies Company, Ltd.’s Disclosure of Asserted Claims and Infringement Contentions, dated May 6, 2024, in <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC</i> , Case No. 3:23-cv-05792-RFL
1036	Joint Claim Construction and Prehearing Statement (Patent Local Rule 4-3), Dkt. No. 105, in <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC</i> , Case No. 3:23-cv-05792-RFL
1037	U.S. Patent No. 10,559,583 B2 to Park et al., bearing production numbers MYM0084362 - MYM0084410
1038	U.S. Patent No. 9,893,082 B2 to Kim et al., bearing production numbers MYM0069093 - MYM0069154
1039	U.S. Patent No. 11,335,807 B2 to Mehandru et al., bearing production numbers MYM0092210 - MYM0092240

Exhibit	Description
1040	U.S. Patent No. 10,431,686 B1 to Yang et al., bearing production numbers MYM0092241 - MYM0092267
1041	Transcript of the deposition of Dr. Keln Kuhn, dated March 28, 2025, in IPR2024-00789, concerning U.S. Patent No. 10,861,872

9. As stated above, I also reviewed and considered the Board’s Institution Decision (Paper 15), issued on October 25, 2024; YMTC’s Patent Owner Response (Paper 18), filed on January 17, 2025; and the exhibits that YMTC submitted with its Patent Owner Response, including Dr. Kuhn’s declaration (Ex. 2007).

IV. UNDERSTANDING OF THE GOVERNING LAW

10. I am not an attorney but have been instructed on and applied the law as described in my Initial Declaration.

V. CLAIM CONSTRUCTION

11. As I testified to in my original declaration, in my opinion, the term “dummy source structure” would have been understood to mean a “structure that occupies the void that was used for the gate replacement process.” Ex. 1003, ¶ 74.

12. My original declaration applied two alternative constructions of “dummy source structure”: (1) one that requires that the “dummy source structure” be located in the void that is used for the gate-replacement process (applied in the Park Ground 1) and (2) one that does not (applied in the Tessariol Ground 2). Ex. 1003, ¶ 82.

13. I understand that in the Institution Decision, the Board preliminarily did not adopt construction (1) above, and the Board preliminarily construed “dummy source structure” to mean a structure that “does not function as a source.” ID, 11-13. In other words, the Board’s preliminary construction was (2) above with the addition that the structure does not function as a source.

14. For the reasons described below, my opinion is still that a POSITA would have understood “dummy source structure” to mean a “structure that occupies the void that was used for the gate replacement process.” Further, while “dummy” does typically mean an inoperable component that resembles its non-dummy counterpart, a POSITA examining the specification would determine that “dummy source structure” is not being used according to its plain and ordinary meaning in the ’872 specification and “dummy source structure” would not have been understood as not providing a source function.

A. Dummy Source Structure

15. I disagree with Patent Owner that “dummy source structure” has a plain and ordinary meaning. POR, 14.

16. Dr. Kuhn cites certain purposes of dummy structures, e.g., improving yield and providing structural support. Ex. 2007, ¶¶ 73-74. While I agree that these are functions that a “dummy” structure can provide, a “dummy” structure had a clear plain and ordinary meaning, which the ’872 patent is not using.

17. First, looking at the term in whole (“dummy source structure”), a simple Google Search for “dummy source structure” returns only a handful of results, and outside of YMTC patents or applications, relate to results that have nothing to do with the way that the ’872 patent is using the term (only one non-YMTC patent or application is even in the context of semiconductors). I have never heard of “dummy source structure” before reading the ’872 patent. Put simply, there is no plain and ordinary meaning of “dummy source structure.”

18. Second, looking at “dummy” alone as a qualifier for another structure (e.g., in “dummy channel,” “dummy” qualifies “channel”), the plain and ordinary meaning of this term is an inoperable component that resembles the non-dummy component, e.g., a dummy channel structure is an inoperable channel structure. For example, a dummy channel structure assumes the same structure as the non-dummy channel structure, but for example, the dummy component is not interconnected to electrically functional elements (e.g., connected to a bit line, as a bit line usually connects to the top of a channel structure in 3D NAND).

19. I understand, for example, in the district court proceedings that the parties agreed that “dummy structure” means “electrically inoperable structure that mimics a physical property of an operative structure.” Ex. 1036 (Joint Claim Construction Statement), 2 (agreed construction for ’996 Patent). This is consistent with the plain and ordinary meaning for “dummy structure,” such as “dummy

channel structure.” For example, the dummy channels and channels would be made at the same time and using the same process, such that they result in an identical structure. But the interconnects to connect the dummy channels to bit lines would not be manufactured.

20. This plain and ordinary meaning of “dummy” applies in the context of 3D NAND. For example, the Tessariol reference provides an express definition consistent with this plain and ordinary meaning: “In this document, a ‘dummy structure’ refers to a structure which is used to mimic a physical property of another structure (e.g., presence, or physical load-carrying/supporting ability of an operative structure) and which may comprise a circuit inoperable electrical dead end (e.g., is not part of a current flow path of a circuit even if conductive). Openings in which dummy structures are formed may be considered as “dummy-structure openings.” Ex. 1006, [0068]; *see also id.*, [0053] (“In one embodiment, one of the operative conductive vias and one of the dummy structures are side-by-side and extend elevationally through the same one of the conductive steps, and in one such embodiment, the one operative conductive via and the one dummy structure also extend elevationally through another same one of the conductive steps.”).

21. This plain and ordinary meaning of “dummy” can also be seen in the 3D NAND art with reference to dummy channels, i.e., the dummy channels will be made by the same process as channels (so dummy channels will mimic the channels),

but the dummy channels are electrically inoperable. *E.g.*, Ex. 1037 (U.S. Patent No. 10,559,583), 5:33-36 (“The dummy channel structures DCH may not be electrically connected to a bit line, i.e., may be electrically isolated in the device, as distinguished from the cell channel structures CH.”), 13:57-64 (“A process of forming the cell channel structures CH and the dummy channel structures DCH may begin by forming a plurality of channel holes and forming gate insulating layers 361 in the channel holes. Each of the gate insulating layers 361 may include a blocking layer, a charge storage layer, and a tunneling layer sequentially formed from the inner wall of each of the channel holes, and may fill a portion of an internal space of each thereof.”); Ex. 1038 (U.S. Patent No. 9,893,082), 21:7-11 (“The first and second dummy channel structures 200 b, 200 c may not be electrically connected to the bit lines BL and the first and second interconnection layers M1, M2. Thus, the first and second dummy channel structures 200 b, 200 c may be electrically isolated.”); Ex. 1039 (U.S. Patent No. 11,335,807), 7:1-6 (“Other devices or channels regions of that integrated circuit may be in inactive or so-called dummification areas. Such inactive devices and channel regions are generally not part of the functional circuitry.”); Ex. 1040 (U.S. Patent No. 10,431,686), 10:7-10 (“The P-type channel structures 303P(1) and 303P(3) are dummy fins 307P(1) and 307P(3) that are electrically inactive in the FinFET 311, because they are isolated by the capping layer 314.”).

22. But the '872 patent is clear that the dummy source structures do not need to resemble a particular structure or be electrically inoperable. For example, as I discussed in my first declaration, the dummy source structures can be in the shape of channels or GLSs (Ex. 1003, ¶¶ 78-79) and can be electrically operable structure (Ex. 1003, ¶ 80).

23. Thus, a POSTA reviewing the '872 patent would immediately have understood that the '872 patent is departing from the plain and ordinary meaning of “dummy.”

1. “Dummy Source Structure” Is the Structure that Occupies the Void Used for the Gate Line Replacement Process

24. As I discuss below, the '872 patent describes problems with forming gates using gate-line slits (GLSs), i.e., using GLSs with the well-known gate replacement process. Before I address that, a POSITA reviewing the claims of the '872 patent would have understood that the claims to refer to these teachings of overcoming these problems, i.e., using the dummy source structures instead of GLSs.

25. Claim 1 recites both “conductive layers” and “dummy source structures.” For example, claim 1 recites “a memory stack comprising interleaved **conductive layers** and dielectric layers on the substrate.” Ex. 1001, Claim 1. The '872 specification states: “In 3D memory fabrication processes, a gate-replacement process is often used to form interleaved **word line**/dielectric stacks, in which

sacrificial layers are replaced with **conductive layers** to form gate electrodes/word lines.” *Id.*, 4:30-33. Here, a POSITA would have understood the ’872 patent is describing the ability to create “conductive layers” using the gate replacement process. As shown below, the specification details the problems with using GLSs to create these “conductive layers,” such as problems with the “conductive materials” flowing through the voids. Accordingly, the specification teaches replacing the GLSs with “dummy source structures.” Thus, a POSITA reviewing claim 1 would have understood the claimed “dummy source structures” is what allows the void-free insertion of the “conductive layers,” thereby providing the alleged benefits that the ’872 patent teaches. I note that in reviewing the specification, all embodiments refer to these “conductive layers” and all challenged claims include both the “conductive layers” and “dummy source structures.” *Id.*, 1:36, 1:46, 1:66, 2:2, 2:26-27.

26. The ’872 patent is clear that the dummy source structures can “replac[e] the [gate line slits].” Ex. 1001, 5:30-34. As the below details, the ’872 patent explains this is to create “conductive layers” (the gate layers) to allegedly solve the problems with the gate-replacement process that uses GLSs. The ’872 patent details alleged problems using GLSs for the gate replacement process. *Id.*, 4:30-33, 4:37-67. Specifically, recall that the gate replacement process involves (1) etching out

sacrificial gates with an etchant, and (2) depositing conductive materials. And the '872 Patent describes the problem with using GLSs as follows:

Using GLSs to perform the gate-replacement process has drawbacks. For example, in the staircase region, the large lateral distance between adjacent GLSs can cause conductive material to be unevenly filled in the lateral recesses formed after the removal of the sacrificial layers, resulting in voids in the formed gate electrodes. The gate electrode may have an undesirably high resistance. Also, because dummy channel holes are formed between adjacent GLSs, the boundary conditions for the etching of dummy channel holes at different locations can be different due to the existence of large-area GLSs, causing dummy channel holes to have nonuniform lateral dimensions. For example, the lateral dimensions of a dummy channel hole may gradually vary as the dummy channel hole moves farther away from the GLSs, causing potential performance variation of the memory cells. In addition, the large areas occupied by the GLSs limit the usable space on the wafer surface to place other components, such as staircase contacts.

Id., 4:37-67.

27. As can be seen above, the alleged problems center around the flow of the “conductive material” to form the “conductive layers.” For example, the ’872 patent alleges that problems occur with the gate-replacement process due to the positioning of the GLSs. First, “the large lateral distance between adjacent GLS” results in “unevenly” filling the voids after the removing the sacrificial gates. Ex. 1001, 4:37-67. Second, the position of the GLSs define the location of the “dummy channel structures,” namely, these structures are between the GLSs, and that positioning leads to negative effects on the “memory cells.” *Id.* Third, the ’872 patent criticizes the size of the GLSs, limiting the “usable space on the wafer.” *Id.*

28. After describing traditional GLSs, the ’872 patent again describes the positioning of these GLSs as causing problems: “During the gate replacement processes, conductive materials for forming the gate electrodes need to travel a relatively long distance between adjacent GLSs 504 to fill in the lateral recesses formed after the removal of sacrificial layers. This deposition process can be susceptible to formation of voids and/or nonuniformly deposited gate electrodes.” Ex. 1001, 5:17-23.

29. Against this backdrop, the ’872 patent states: “Various embodiments in accordance with the present disclosure provide an improved 3D memory structure scheme suitable for solving the aforementioned issues by replacing the GLSs with dummy source structures.” Ex. 1001, 5:31-34.

30. Next, the '872 patent describes that the positioning of the dummy source structures improves the alleged problems that GLSs cause during the gate-line process. Specifically, first, the '872 patent describes that the positioning of the dummy source structures allegedly solves the GLSs-dummy channel problem: “The dummy source structures may be arranged in a pattern, e.g., an array, so the dummy source structures can be uniformly distributed in the staircase structure. The arrangement of the dummy source structures may improve the uniformity and stability for etching dummy channel holes in the staircase region.” Ex. 1001, 5:43-49. Second, the '872 patent describes that the positioning of the dummy source structures solves the issue of forming uneven gate layers: “Also, the arrangement of the dummy source structures may allow the gate electrodes/word lines to be formed with improved uniformity and quality, reducing the resistivity of the gate electrodes/word lines. For example, the gate-replacement process can be performed to deposit a conductive material through the dummy source holes that subsequently form the dummy source structures. Because the conductive material travels shorter distances to fill up the lateral recesses for forming the gate electrodes, the gate electrodes are less susceptible to voids or density nonuniformity.” *Id.*, 5:49-58.

31. Accordingly, the '872 patent solves the alleged problems with the gate-replacement process by using the voids for the dummy source structures, which the '872 patent refers to as “dummy source holes” that are later occupied by the “dummy

source structures.” In other words, the dummy source holes are used like the conventional GLS trenches (i.e., the voids that are used in the conventional gate line replacement process), and a respective structure fills the respective voids. Thus, the ’872 patent discusses the alleged solution in the context of “dummy source holes.” For example, the ’872 patent discloses that because the “gate-replacement process can be performed to deposit a conductive material ***through the dummy source holes that subsequently form the dummy source structures***,” the “conductive material travels shorter distances to fill up the lateral recesses for forming the gate electrodes.” Ex. 1001, 5:49-58. And the specification defines the “dummy source structures” as what occupies the “dummy source holes”: “dummy source holes that subsequently form the dummy source structures.” *Id.* Thus, when the ’872 patent states that it is “replacing the [gate line slits] with dummy source structures” (*id.*, 5:30-34), a POSITA would have understood that the ’872 patent is “replacing the [gate lines slits] with [dummy source holes in which the dummy source structures are subsequently formed].” *Id.*, 4:65-67. Thus, the GLSs are replaced with dummy source holes, and the dummy source holes are subsequently filled and become dummy source structures.

32. In view of the above, a POSITA would have understood that a “dummy source structure” occupies the void used for the gate replacement process. As can be seen above, this portion of the specification is using “conductive materials” and

“conductive layers” restrictively to refer to the gate replacement process. And it is describing the solution to the gate replacement process as creating the “conductive layers” with flowing the “conductive materials” through the “dummy source holes.”

33. I disagree with the arguments that Patent Owner has raised.

34. First, Patent Owner argues that Petitioner’s construction reads out “dummy” from the term. POR, 19. This argument assumes that “dummy” is being used according to its plain and ordinary meaning, and therefore I disagree (see above). In addition, as I discuss below, the specification actually was written to state that the “dummy source structure” does not function as a source only in some embodiments.

35. Second, Patent Owner argues that Micron’s construction incorporates method step into the term. I am not an attorney and do not offer opinions regarding the meaning of the cases that Patent Owner cites. But as I described above, a POSITA would have understood claim 1 to refer to the “dummy source structures” in which the voids for those structures are used to create the “conductive layers.” Also, Micron’s construction does not limit how the “dummy source structures” are fabricated. The dummy source structures, for example, may be fabricated to be dielectric or conductive cores. Ex.1001, 16:56-63. Consistent with Micron’s construction, a POSITA would have understood that the “dummy source structures” are located in the voids used for gate-replacement, which does not require that the

structure of the dummy source structure be fabricated with, for example, either a dielectric or conductive core. It could be formed by “one or more thin film deposition processes” such as atomic layer deposition, chemical vapor deposition, and physical vapor deposition” (POR at 22). Rather, however “dummy source structures” are formed, they are limited by their location, that is, they have to occupy the voids where gate replacement process occurs, because the alleged novelty of “dummy source structures” is that they “replac[e] the GLS” and solve the various structural issues with GLSs. Ex. 1001, 5:31-34. (“Various embodiments in accordance with the present disclosure provide an *improved 3D memory structure* scheme suitable for solving the aforementioned issues by replacing the GLSs with dummy source structures.”). *Id.*, 5:31-34.

36. Third, Patent Owner cites the following passage:

Also, the arrangement of the dummy source structures may allow the gate electrodes/word lines to be formed with improved uniformity and quality, reducing the resistivity of the gate electrodes/word lines. For example, the gate-replacement process can be performed to deposit a conductive material through the dummy source holes that subsequently form the dummy source structures. Because the conductive material travels shorter distances to fill up the lateral recesses for forming

the gate electrodes, the gate electrodes are less susceptible to voids or density nonuniformity.

Ex. 1001, 5:49-58

37. I understand that Patent Owner argues that because this portion states “for example,” this passage suggests the gate line replacement process is optional. POR, 20-21. This argument takes the entire paragraph and “for example” sentence out of context. The first sentence recites “[a]lso, the arrangement of the dummy source holes.” This is referring to the above paragraph’s discussion of that “arrangement.” Ex. 1001, 5:31-48. As can be seen in that paragraph, 5:31-48 is describing replacing GLSs with dummy source structures to perform the gate-replacement process, and thus the entire 5:49-58 is building on this description of the gate replacement process. The “[f]or example” sentence refers to the fact that the gate-replacement conductive material “can” form the “dummy source structures” as well as the gates. *Id.*, 5:52-55 (“subsequently form the dummy source structures”). Further, it is giving an example of how the “arrangement” can improve the gate-replacement process.

38. Patent Owner also cites column 4:30-33. I discuss this portion above. It starts with the “gate-replacement process is often used.” It then continues and states that when used, “sacrificial layers are replaced with conductive layers to form gate electrodes/word lines.” These “conductive layers” are then what the

specification describes as being formed by the dummy source structures during the gate-replacement process instead of the GLSs (and recall, the claims recite “conductive layers”). Ex. 1001, 4:30-5:58.

39. Patent Owner cites column 16:40-49. This portion is describing forming the dummy source structure after its void was used for the gate replacement process. Ex. 1001, 15:16-49, 16:40-49.

40. Patent Owner argues that Micron’s construction improperly limits the claim scope to a specific embodiment. POR, 22. I disagree. As I noted above, Micron’s construction permits the “dummy source structure” to be, for example, either a dielectric or conductive pillar. These are different embodiments. But in all cases, a POSITA would have understood that the dummy source structure (whether a dielectric or conductive core) would be located in the voids used for the gate replacement process.

2. The Specification Does Not Support PO’s Negative Limitation

41. As described below, the specification discusses a number of functions that the dummy source structure may perform, but never requires a particular function (other than being used for the gate replacement process) or forecloses a particular function.

42. First, the specification states that “[i]n some embodiments, dummy source structures 178 may function as interconnects to connect 3D memory device

100 with other peripheral devices.” Ex. 1001, 5:41-43; *see also id.*, 16:63-66. The “interconnect” is referring to connecting two elements, namely, an element within the memory portion with a peripheral circuit element. Thus, the ’872 patent does not use “dummy” to exclude the dummy source structure from being an operable, functioning element such as a conductive via. As described above, this is a departure from the plain and ordinary meaning of “dummy.” Note that the specification recites that only “[i]n some embodiments,” the dummy source structure “may” function as an interconnect, i.e., the specification uses both non-limiting embodiment language (in some embodiments) and permissive language (may). *Id.* Thus, the dummy source structure may or may not function as an active interconnect. Put simply, the dummy source structure may not be a “dummy” structure, in the common sense of dummy, at all.

43. I also note that the ’872 patent confirms that when it refers to an embodiment having a feature, other embodiments may not include that feature: “It is noted that references in the specification to . . . ‘some embodiments,’ etc., indicate that the embodiment described may include a particular feature, structure, or characteristic, but every embodiment may not necessarily include the particular feature, structure, or characteristic.” Ex. 1001, 3:1-7. This confirms that in other embodiments, a dummy source structure need not be an interconnect.

44. Second, the specification describes how the dummy source structure “may” function depending on its composition. But again, this language is permissive for each composition: “When conductive materials are used to fill dummy source hole 212 (e.g., contact 244), the dummy source structure 246 may function as an interconnect to connect 3D memory device 100 with other peripheral devices. When dielectric materials are used to fill dummy source hole 212, dummy source structure 246 may function as a mechanical support structure to improve the stability of the staircase region.” Ex. 1001, 16:63-17:3.

45. Third, the specification draws a contrast—in some embodiments—between “source structures” and “dummy structures.” Specifically, the ’872 patent recites:

Source structures formed in the inner region may be connected with surround channel structures (e.g., channel structure 220 of memory string 218 shown in FIG. 2E) via a common source, such as a doped region (not shown) in substrate 202. In some embodiments, dummy source structure 246 may not connect to channel structures in the inner region. Instead, dummy source structure 246 may be formed simultaneously with source structures in the inner region, while functioning as a mechanical

supporting structure after gate-replacement process, without connecting to channel structures in the inner region.

Ex. 1001, 16:33-44.

46. As can be seen above, the specification is stating that the source structures “may” function as sources to the memory channels. And “in some embodiments,” dummy source structures may not function as sources to the memory channels. And the specification states a function (support function) that dummy source structures may “[i]stead” perform, that is, a function “[i]stead” of functioning as a source to the memory channels. Thus, read together, (1) in “some embodiments,” the source structures may function as a source, and the dummy source structure may not function as a source, (2) in other embodiments (that is, the embodiments other to the “some embodiments”), the source structures and dummy source structures may function as a source.

47. Recall that the '872 patent confirms that when it refers to an embodiment having a feature, other embodiments may not include that feature: “It is noted that references in the specification to . . . ‘some embodiments,’ etc., indicate that the embodiment described may include a particular feature, structure, or characteristic, but every embodiment may not necessarily include the particular feature, structure, or characteristic.” Ex. 1001, 3:1-7. This confirms that the reference to “in some embodiments,” is not a statement as to all embodiments.

Accordingly, a POSITA would have understood by the '872 patent expressly using the “in some embodiment” language, the dummy source structures may function as a source to channel structures. For these reasons, I disagree with Patent Owner’s construction stating that a dummy source function may not function as a source to channel structures.

48. I understand that Patent Owner argues: “But a dummy source structure’s “connect[ion] to channel structures” does not, on its own, establish that the dummy source structure provides a “source to the memory cells” (i.e., connects the memory cells to source power).” POR, 17. Thus, it appears that Patent Owner argues that the “in some embodiments” language in the above passage of the specification means that the dummy source structure will connect to the channel structures. But Patent Owner appears to be trying to draw a distinction between connecting to the channels and functioning as a support. I disagree with Patent Owner for two reasons.

49. First, the passage above states that “source structures” may function as a source, and I understand that Patent Owner does not dispute this. It then follows that “in some embodiments,” the dummy source structures may not. Naturally, then, when it is referring to the source structures not doing so, it is referring to the dummy source structures not functioning as a source. Thus, in the other embodiments (the not “some embodiments”), it would function as a source.

50. Second, while the '872 patent does not detail how these dummy source and source structures function as sources, it was well known. For example, exhibit 1023 is a textbook on 3D NAND, the below figure illustrates a source line (most right grey cylindrical structure):

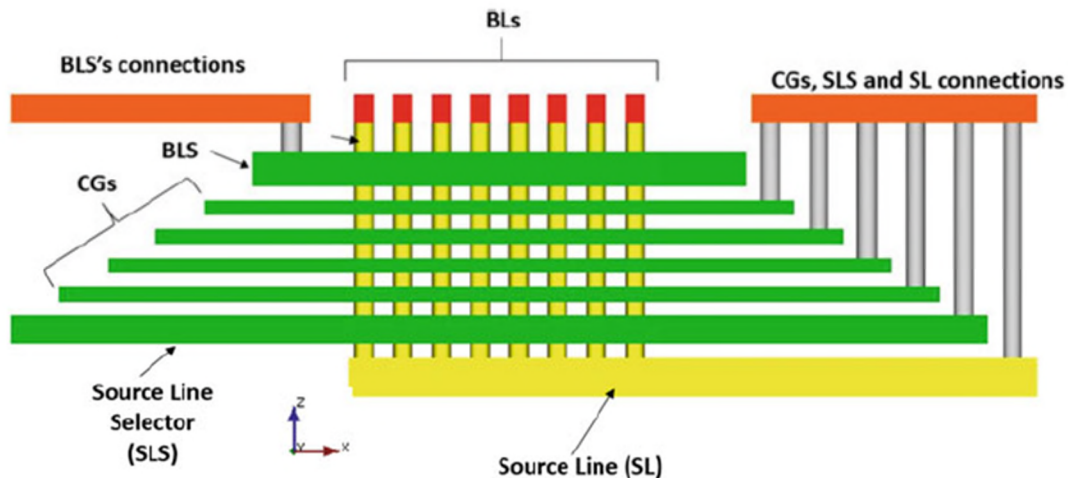


Fig. 4.12 Vertical cross section of BiCS with gate connections

Ex. 1023, 109. As can be seen, the source line (equivalent here to a dummy source structure (in some embodiments) and source structure, these lines have a connection on top (e.g., to a ground voltage), travel through the stack or outside of the stack, and contact the substrate, in which there would be an understood doping that enables an electrical connection to the substrate region in which the channel structure contacts. It appears that Patent Owner is arguing that there would be a dead-end somewhere along this path. But I have not seen any such dead-end, e.g., partial path to the channels, in the '872 patent. Instead, just like a source structure, it would have been understood that there would be a source voltage on top and a path the channel

structures. Indeed, even for source structures, the '872 patent does not depict and describe the source voltage or the path in the substrate between the source or dummy structure to the channel structures.

51. I have been asked to opinion on whether either “the words of the claim” or an “express disclaimer or independent lexicography in the written description” would justify adding that the dummy source structure does not operate as a source to the memory cells. There is neither to me. The claim language does not justify adding this limitation, because the '872 patent does not use the plain and ordinary meaning of “dummy,” e.g., inoperable structure. The specification does not justify the limitation either, because it only describes that in “some embodiments,” the dummy source does not function as a source.

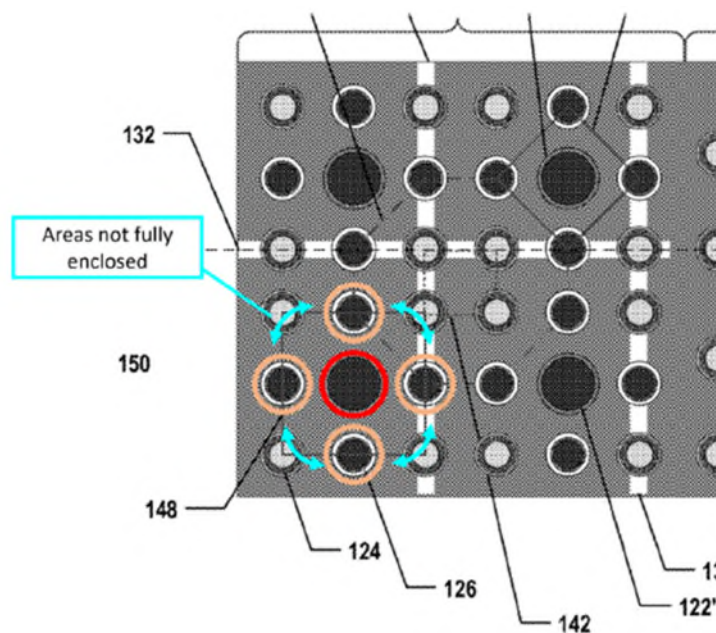
B. Surrounding

52. I understand that the Board, in the Institution Decision, states: “Because we determined that, for purposes of this Decision, ‘surrounding’ does not encompass structures on only two sides of an object, Petitioner does not show that Park teaches this limitation.” ID, 30. In my opinion, in view of the '872 specification, two, long laterally-extending dummy source structures can “surround” a staircase contact for the following reasons.

53. The '872 specification states: “As a result, dummy source structures 178 can laterally separate 3D memory device 100 into multiple memory 45 regions,

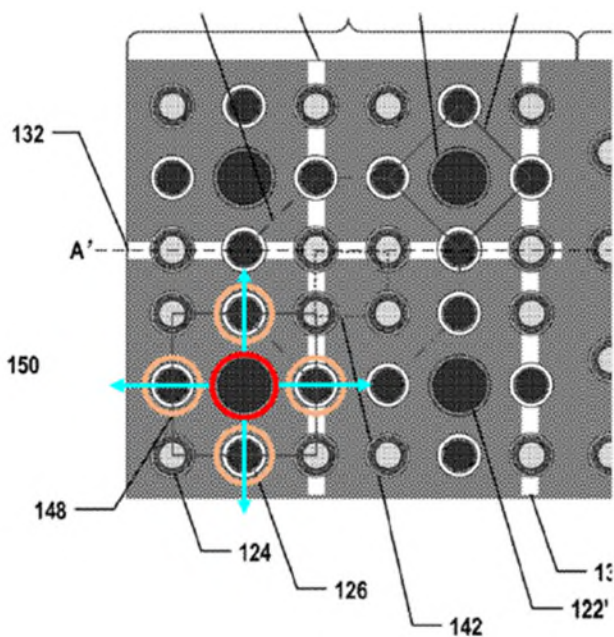
such as memory blocks.” Ex. 1001, 11:44-46. This means that the dummy source structures may assume the form of long, laterally-extending structures. Because these structures are long, laterally-extending members, they divide the memory into blocks, i.e., they divide the memory stacks into block regions. I note that in distinguishing the prior art in the file history, the applicant cited the specification for this point. Ex. 1002, 514 (dummy source structures can “laterally separate 3D memory device”). The specification also states that less than four dummy structures may “surround” a contact. Ex. 1001, 8:8-11.

54. Given these various embodiments of the ’872 patent, in my initial declaration, I described two measures of surrounding. Specifically, one way to consider “surround” is the amount of border that the dummy source structures create, as shown below:



Ex. 1003, ¶ 90.

55. Another measure is to determine whether four radially extending lines, with a 90° separation, intersect to a dummy source structure, like that shown in exemplary '872 embodiments:



Ex. 1003, ¶ 90.

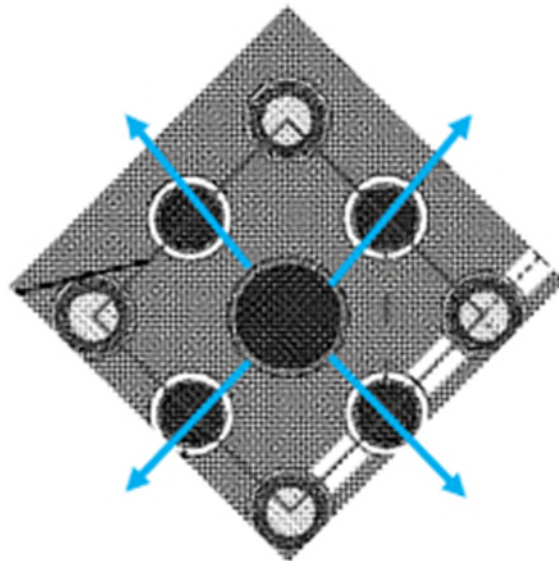
56. I also note that modifying an express embodiment of the '872 patent demonstrates that two objects can “surround” a contact. Recall that the dummy source structures may be laterally-extending members. Ex. 1001, 11:44-46. Thus, one can take the express embodiment in Fig. 1A and modify each set of dummy source structures such that each set becomes a single dummy source structure. This is shown below as orange, laterally-extending members. These two laterally extending dummy source structures must satisfy the “surrounding” limitation, because they surround the contact to a greater degree than the four smaller dummy source structures. These two structures also surround more of the contact’s border

than the embodiment with four dummy source structures. As shown below, one could characterize both the two laterally-extending dummy source structures (on left) and four dummy structures (on right) as surrounding on two sides, but that cannot be the right measure of “surround” given that, clearly, the two long, laterally extending dummy source structure “surround” the contact to a greater degree than the express embodiment of four dummy source structure surrounding the same contact.

Id., Fig. 1A (partial and annotated).

themselves. In other words, it does not mean that the GLSs do not “surround” the holes.

58. I understand that PO attempts to redefine the four radial, intersecting measure of “surround” such that those lines must be drawn from the “center” (0°, 90°, 180°, 270°) of the contact. POR, 26-27. But the '872 specification does not limit the four dummy source structures to being in those locations, for example, one could simply rotate the dummy source structures. Ex. 1001, 8:51-53. This is shown below:



Id., Fig. 1A (partial and annotated). Thus, the proper measure regarding the four radial, intersection lines is whether four lines, with 90° degrees separation, intersect with dummy source structures.

59. I agree with Dr. Kuhn that a single structure can “surround.” Ex. 1041, 138:1-8. Again, the specification says that less than four objects may “surround.”

Because of this, it is appropriate to consider the measures above (four radial lines and extend of coverage around border) to determine whether the dummy source structures surround the contact.

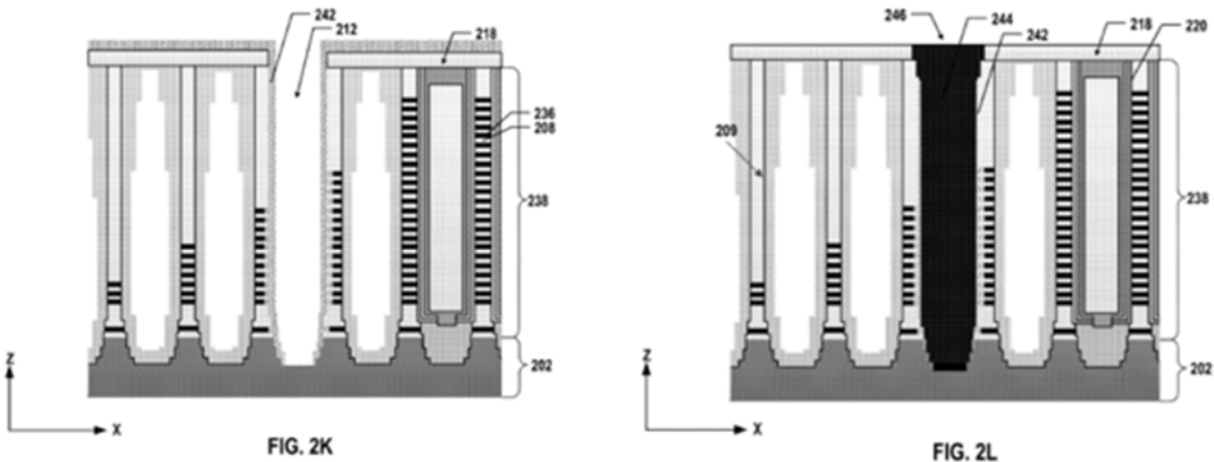
60. In my original declaration, I cite Ex. 1019 (the '492 patent) to demonstrate that POSITAs do use “surround” to refer to two objects surrounding. Ex. 1003, ¶ 92. I understand that Patent Owner argues that with respect to the '492 patent use of “two surrounding NAND cells,” Patent Owner and Dr. Kuhn argue that this passage refers to *more than* “two” NAND cells. POR, 27-28 (citing Ex. 1019, 2:14-16). I disagree. The language in the '492 patent is clear. Also, the '492 patent refers to location information for these two cells are: “in the adjacent left and right BLs,” each bit line corresponding to one NAND cell. Ex. 1019, 2:14-16. This further confirms that “two surrounding NAND cells” refer to two NAND cells.

C. Conductive Contact

61. I understand that Patent Owner argues that “conductive contact” means “a conductive structure that permits current flow with an adjoining conductive structure.” POR, 28. I disagree that a POSITA would have understood “conductive contact” as such, and instead, would have understood the term to refer a conductive material that fills the dummy source hole, i.e., a conductive pillar core.

62. The '872 specification consistently refers to the “conductive contact” as the vertical conductive member that extends through the stack. For example,

sometimes the word “contact” is used to refer to an element that sits on the top of another element and is placed there so another element can connect to it (also known as an interconnect), but the ’872 patent does not ascribe that meaning to “conductive contact” in the specification. The ’872 patent explains that “[a]s illustrated in FIG. 2L, a contact 244 is formed within spacer 242 in dummy source hole 212 (shown in FIG. 2K). Contact 244 can be formed by depositing conductive materials including, not limited to W, Co, Cu, Al, polysilicon, silicides, or any combination thereof, over spacer 242 in the dummy source hole using one or more thin film deposition processes, such as ALD, CVD, PVD, any other suitable processes, or any combination thereof. A dummy source structure 246 including spacer 242 and contact 244 is thereby formed in the dummy source hole, surrounded by a plurality of dummy channel structures 209.” Ex. 1001, 16:21-32. As shown below, the “contact” is simply a fill of conductive metal (246) into a hole (212) with an insulating liner (242). This is a conductive via that provides a conductive path through the stack (with an insulating liner):



Id., Figs. 2K, 2L.

63. The '872 Patent repeatedly characterizes “contact” as simply being the metal inside the dummy source hole:

- “In addition, the method includes forming a spacer along a sidewall of each of the plurality of dummy source holes to cover the conductive layers in the staircase structure and forming a contact within the spacer in each of the plurality of dummy source holes.” Ex. 1001, 2:2-8.
- “In some embodiments, dummy source structure 178 includes a dummy source hole filled with conductive materials as a contact 179.” *Id.*, 11:37-39.
- “Method 300 proceeds to operation 312, as illustrated in FIG. 3, in which a contact is formed within the spacer in the dummy source hole. In the example of method 400 in FIG. 4, at operation 414, a contact is formed within the spacer in the dummy source hole.” *Id.*, 16:13-21.

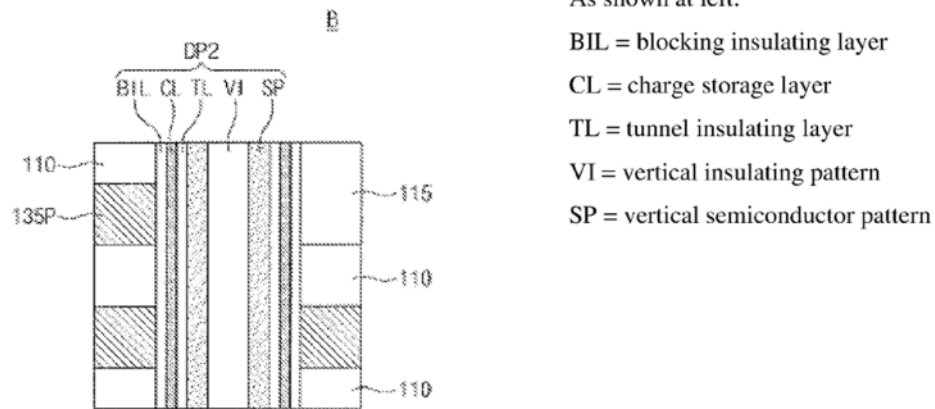
- “In some embodiments, contact 244 may be formed simultaneously with word line contacts by filling conductive materials simultaneously to dummy source hole 212 and staircase contact 122 (shown in FIG. 1A).” *Id.*, 16:50-53.
- “When conductive materials are used to fill dummy source hole 212 (e.g., contact 244), the dummy source structure 246 may function as an interconnect to connect 3D memory device 100 with other peripheral devices.” *Id.*, 16:63-64.
- “A spacer along a sidewall of each of the plurality of dummy source holes is formed to cover the conductive layers in the staircase structure. A contact within the spacer in each of the plurality of dummy source holes is formed.” *Id.*, 18:38-41.

64. None of the figures of the '872 Patent depict the conductive contact connecting to any element.

65. Also, the file history is instructive. The Applicant added this limitation to overcome the prior art. When doing so, the Applicant did not ascribe any functional property to it, but distinguished the prior art by focusing solely on the structural nature of the “conductive contact” and highlighting that it is the conductive core of a pillar:

Jeong does not disclose dummy source structures, but simply discloses dummy pillars. The dummy pillars in Jeong are

different from the claimed “dummy source structure” in amended independent claims 1 and 8 at least because the dummy pillars do not include conductive contacts. Jeong explains the construction of the dummy pillars in FIGs. 4A, 4B, 4C, and 4D. Taking FIG. 4A as an example (because it is the most elaborate example in Jeong), the dummy pillar (DP2) includes the following:



By contrast, FIG. 1D (reproduced below) illustrates an example of a dummy source structure 178, including contact 179 and spacer 177 (see also, FIG. 2L, dummy source structure 178, contact 244, and spacer 244). Nothing in Jeong’s pillar is conductive contact, as the pillar consists of insulating layers, a semiconductor pattern, and a charge storage layer. By contrast, as explained at paragraph [0057] of the present application: “In

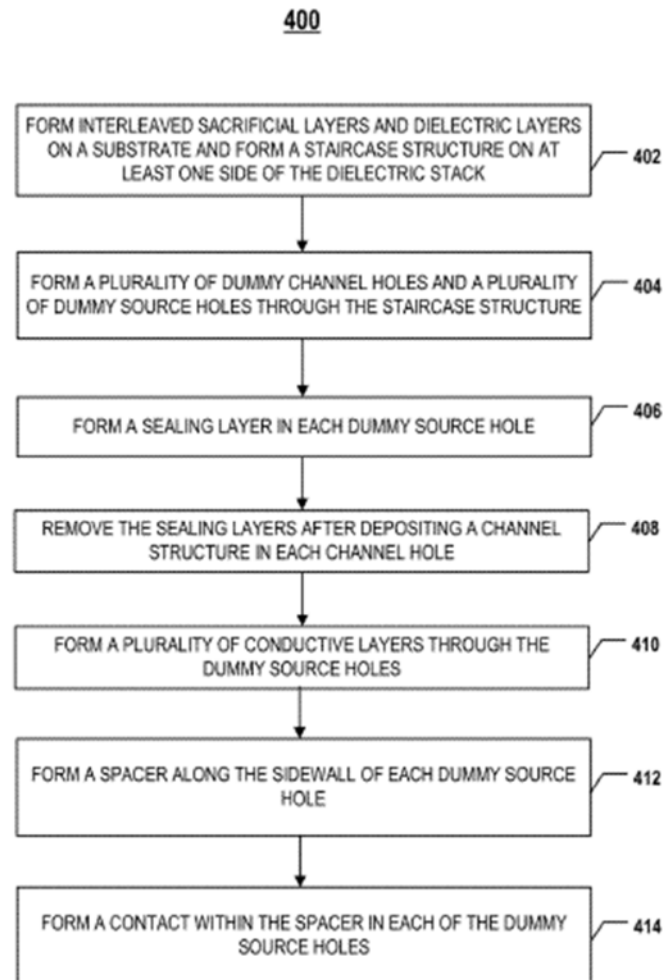
some embodiments, dummy source structure 178 includes a dummy source hole filled with conductive materials as a contact 179. Dummy source structure 178 can further include a spacer 177 made of any suitable dielectric materials (e.g., silicon oxide) between contact 179 and memory stack 160 to electrically separate surrounding conductive layers 106 in memory stack 160 from contact 179. As a result, dummy source structures 178 can laterally separate 3D memory device 100 into multiple memory regions, such as memory blocks.”

Ex. 1002, 514-15.

66. I understand that Patent Owner argues that the meaning of the term “contact” supports requiring that it allows current flow with an “adjoining conductive structure.” POR, 29-30. I disagree for several reasons.

67. First, I generally agree with Dr. Kuhn that “contact” is a broad term, that “contact” does not automatically suggest a functional contact that includes an adjoining structure, and that interpreting “contact” therefore requires studying the specification. Ex. 1041, 31:24-32:10, 155:7-156:14. As I have shown above, the specification consistently describes a “contact” as the conductive core of a pillar without any reference to an adjoining structure.

68. Second, Figure 4 is instructive. Figure illustrates creating the “contact” in step 414 by depositing a conductive material in the dummy source hole. The “contact” is made at this point. There is no step of before, or after, of creating an “adjoining structure.”



Ex. 1001, Fig. 4.

69. Third, I disagree that Micron’s interpretation or construction reads “contact” out of the claim. POR, 29-30. “Contact” would have been understood to be a conductive vertical member extending through the stack that may function as

an interconnect depending on the design. Recall that “dummy” suggests that the structure may be inoperable. Thus, it would run counter to common sense to require that this “dummy source structure” with a “conductive contact” always operate to electrically connect to an adjoining structure, i.e., function as an interconnect.

70. I also understand Patent Owner to argue that its construction does not require that it connect to a peripheral device, because it could connect to a different adjoining structure. In reviewing Dr. Kuhn’s testimony, for example, she states that the conductive contact could connect to “a little block of doping” on the substrate. Ex. 1041, 87:20-89:25. There is no support position in the specification. Figure 2L, for example, demonstrates the conductive core terminating in the substrate. In reviewing Dr. Kuhn’s testimony, she appears to concede that the specification does not describe the bottom of 244 connecting to an adjoining structure that would enable current flow, because the specification never describes any doping in that region. *Id.*, 21:12-21, 28:3-29:4, 72:1-19, 74:22-75:21, 78:7-14, 89:10-90:14 (no doping), 87:20-89:25, 133:24-134:10 (according to PO, doping needed for structure to qualify as a “contact”). In short, she is recognizing that this “little block of doping” would require localized doping right at the bottom where the contact hits the substrate, but it would not extend to any other element. This is not shown in the specification, and I am not aware of why such a “little block of doping,” leading to nowhere, would have any practical benefit.

71. I also understand that Patent Owner argues that “(e.g., contact 244)” in 16:63-66 refers to an example of a “conductive material to form an interconnect.” POR, 31. I disagree, because as I have shown above, the ’872 patent consistently describes the contact as a metal core of a pillar without requiring it to be an interconnect. Also, reviewing the sentence with Patent Owner’s addition renders it illogical, because it effectively states an interconnect can or cannot be an interconnect: “contact 244,” i.e., “conductive material to form an interconnect,” “[may or may not function] as an interconnect.”

72. In my opinion, Patent Owner is advancing a construction that effectively construes “conductive contact” to be an interconnect. I agree with Dr. Kuhn that the ’872 patent uses “interconnect” to refer to an element that electrically connects two elements. Ex. 1041, 34:8-24, 159:24-161:21, 163:9-164:20. For example, the ’872 patent states: “***In some embodiments***, one or more dummy source structures are in contact with the substrate and may provide interconnect between the 3D memory device and peripheral devices.”). Ex. 1001, 5:40-43, 11:47-50 (same), 16:63-67 (same). The ’872 specification, however, distinguishes an interconnect from a “conductive contact,” because it states a “conductive contact” may be an “interconnect” in only some embodiments (*id.*, 5:40-43) and consistently describes a “conductive contact” without reference of any adjoining structure (see above).

73. I understand that Patent Owner cites certain definitions that allegedly support its construction. POR, 33. I disagree that these definitions support Patent Owner's constructions. For example, Patent Owner cites a definition for "electrical contact," not contact. *Id.* This is a more narrow definition than a "contact," because the qualifier "electrical" suggests that it being put to use to electrically couple elements. Patent Owner also cites excerpts from two different definitions. Reading these definitions in full shows that neither is inconsistent with Micron's construction or interpretation. Ex. 2009, for example, states: "or a part or device by which such a connection is made." And Ex. 2010, for example, states: "[a] part or device which serves to open or close an electric circuit. Such a part or device may or may not act with another part or device." A dummy source hole filled with conductive material, i.e., a conductive pillar through the stack, meets these descriptions. This conductive core provides a conductive path through the stack. That conductive core may or may not make an electrical connection depending on whether it functions as an interconnect, e.g., if additional connections are made.

VI. TESSARIOL

A. Claim 1

1. Tessariol's Dummy Vias Disclose a "Conductive Contact"

74. I disagree with Patent Owner that Tessariol's dummy vias do not include a "conductive contact" (POR, 59) because properly understood, a "conductive contact" does not require an adjoining structure. §V.C.

75. I understand that Patent Owner argues that Tessariol's dummy vias cannot permit current flow (i.e., operate as an interconnect), because they land on a substrate and have no connection at top. POR, 60. I disagree, because Patent Owner's argument against assumes the wrong construction of "conductive contact." §V.C.

76. I also note that Patent Owner is effectively distinguishing the "conductive contact" shown in Figure 2L from the claims. The argument also fails because it asks more of the prior art than the '872 patent discloses. As I discuss above in §V.C, Figure 2L and the specification does not, for example, depict or describe this little block of doping that Dr. Kuhn argues is necessary for "conductive contact" under Patent Owner's construction. And Figure 2L, like Tessariol, does not depict any connection on top of the conductive pillar.

77. I also disagree with Patent Owner that a POSITA would assign any weight to an alleged "exposed conductive contact 244" in the '872 patent. POR, 59. Figure 2L of the '872 patent does not depict a final memory device. It is a view similar to Tessariol's dummy via that has an "exposed" top during manufacture. Tessariol, Fig. 12. Like Tessariol, additional steps will provide layers on top, and just like Tessariol, one could fabricate interconnects to connect to the top of the pillars or not.

78. Tessariol discloses this limitation under PO's construction as well. Tessariol's dummy vias land on "conductively-doped semiconductor substrate." Ex. 1006, [0028]. As can be seen in Figure 5 of Tessariol, this is the region that doped that also include the channel structures source side, and that source side electrically couples to this region. Current flows through this region. The dummy vias also land on this spot. This is the localized doping region to which Dr. Kuhn testified about that she considers necessary for there to be a "conductive contact." Ex. 1041, 87:20-89:25, 133:24-134:10.

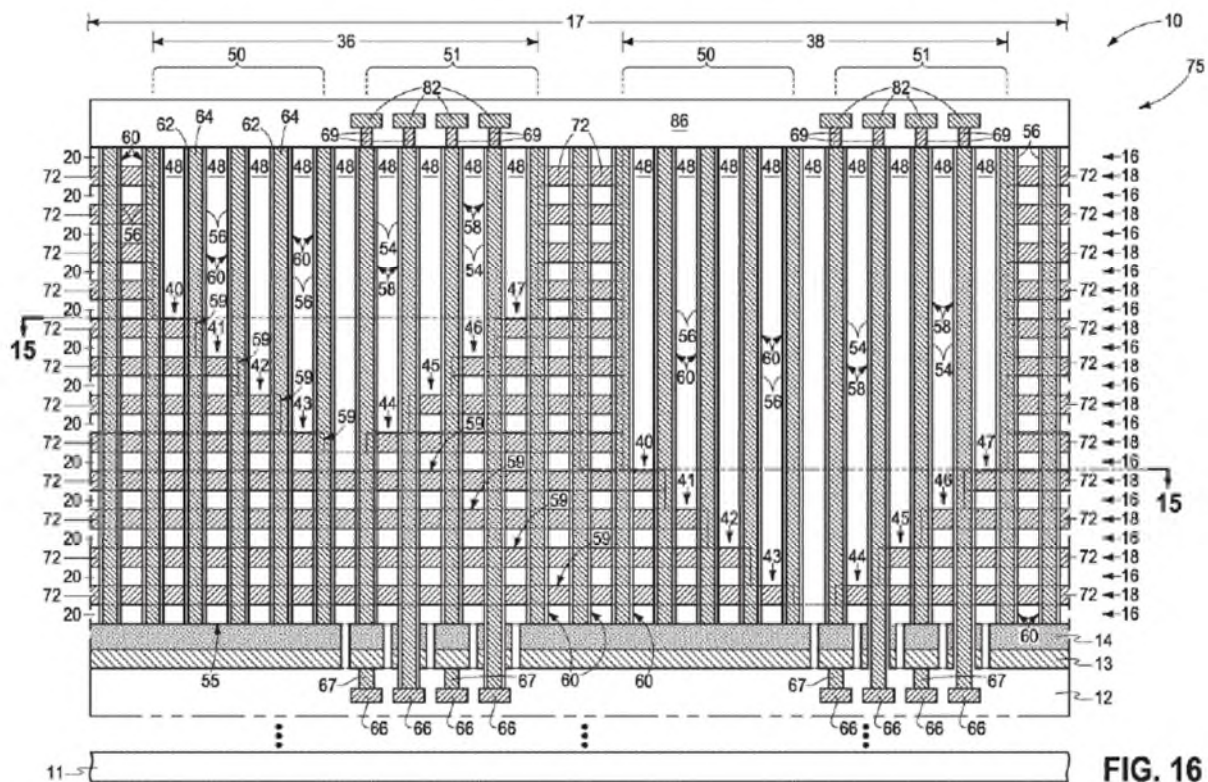
2. Tessariol's Dummy Vias Render Obvious a "Conductive Contact"

79. In my opening declaration, I noted that "at the very minimum, it would have been obvious that Tessariol's dummy structures can contact an upper-level interconnect." Ex. 1003, ¶ 216.

80. I understand that Patent Owner argues that my testimony is conclusory. POR, 62. I disagree. For example, I stated that: "It would simply involve performing the same process to create interconnects 82 on top of the dummy structures. And because the dummy structures 60 and conductive vias are made with the same process, the interconnects would provide the same function for the dummy structures 60 as the conductive vias 58, and thus dummy structures certainly could connect to upper-level interconnects with such interconnects. This demonstrates that the dummy structures 60 are capable as functioning as a conductive via, as all that is

necessary is connecting the dummy structures 60 to upper-level devices in the same way as is done for the conductive vias 58. And Tessariol's process is advantageous. As I explain above under limitation [1.E], it reduces time and process steps." Ex. 1003, ¶ 216.

81. In any event, the process of design involves first the design, creating masks, and the actual fabrication. Dr. Kuhn testified to this in her deposition, and I agree with a number of her statements. Ex. 1041, 32:11-19, 107:21-108:12, 177:1-179:15. To place this testimony (and mine) in context, below is a view of an exemplary Tessariol design:



Ex. 1006, Fig. 16.

82. As shown above, while the conductive pillars (both dummies and operable vias) are in a consistent pattern, the interconnects (69/82) above are not. This requires in the design phase, therefore, repeating this irregular pattern on top, rather than just replicating the consistent pattern. Similarly, when creating the masks, there is an irregular mask pattern that is necessary. It is more straightforward to implement repeating patterns, which adding interconnects onto the dummies would enable, for several reasons. Repeating structures are easier to pattern during lithography, and subsequent reactive ion etching. Lithography at such small geometries is complicated by diffraction effects, which distort the pattern relative to what is designed on the mask. There are also distortions due to so-called proximity effects from close by neighboring structures. If the patterns are regular, the proximity effects are more predictable, leading to more uniform lithographic patterning. These distortions can be more easily corrected for regular geometries by creating an intentionally distorted pattern on the mask generated by inverse modeling of the diffracted pattern. After lithography, the patterns are typically etched by plasma-based reactive ion etching (RIE). Here, too, there can be irregularities in the etch rates due to neighboring structures which can consume the reactant gases, leading to so-called micro-loading effects. If the patterns are regular, there will be more predictable, uniform micro-loading during RIE.

83. I also note that Tessariol states that the dummy structures only “may” comprise an electrical dead end. Ex. 1006, [0068]. Thus, a POSITA would have understood that Tessariol itself suggests these dummies could be made to include interconnects thereon, simplifying the process for the reasons that I explain above. Then, these dummies, too, could connect to peripheral devices under the substrate like the operable vias. *Id.*, [0027], [0039]. In that case, it is true that Tessariol might change its naming convention, and now call them operable vias, but Tessariol is expressly contemplating that these dummies can include interconnects just like the operable vias. If they did not connect to peripherals device to serve as functional vias, they would remain dummies (but the additional interconnects would simplify the manufacturing process for the reasons above).

B. Claims 3 and 4

84. I understand that Patent Owner argues that it improper to rely on the figures for precise measurements. I am not an attorney, but in my opinion, a POSITA would have understood these limitations to be met by the Tessariol figures alone, which the Tessariol specification confirms.

85. First, claims 3 and 4 relate to the “nominal” distance, which the ’872 patent defines as: “a desired, or target, value of a characteristic or parameter for a component or a process operation, set during the design phase of a product or a process, together with a range of values above and/or below the desired value.” Ex.

1001, 4:9-15. Thus, these claims relate to the “design” phase. A POSITA would have understood Tessariol’s figures to represent a layout design. Tessariol’s figure 15, for example, clearly represents a repeating pattern in which there are sets: a contact with four surrounding dummy or operable vias. Given that it is best practice to use repeating patterns in semiconductive designs (which I describe above and actually teach in my classes), a POSITA viewing the Tessariol figures would immediately interpret the figures to include this repeating pattern, in which these objects are of equal distance from the contact.

86. Importantly, Tessariol is not “silent” as to dummy via configuration, as Patent Owner alleges. POR, 65. Tessariol discloses: “Openings 54 and 56 are shown as being collectively arrayed in straight-line rows and columns. However, any alternate configuration may be used including, for example, staggering (not shown) alternating openings 54/56 in rows and/or columns.” Ex. 1006, [0037]. This “arrayed in straight-line rows and columns” expressly refers to this uniform, repeating patterns, that centers the staircase contacts within the four vias.

VII. PARK

A. Claim 1

1. Park's Dummy and Common Source Lines Surround the Staircase Contact

87. I understand that Patent Owner argues that Park's dummy and common source lines cannot surround the staircase contact because the staircase contact is only between those lines. POR, 40-42. I disagree with this for the reasons in §V.B.

88. I understand that PO argues that Park's common source lines cannot surround the staircase contact because these lines are similar to prior art GLSs for the gate-replacement process. POR, 42-44; Ex. 1001, 5:1-48. But in reviewing the specification, it was clear that the "dummy source structures" had a conductive contact that led to allowance, not that they had a particular shape. Pet., 21-22. Also, recall that the '872 specification and file history expressly state that the dummy source structures may be laterally-extending members, just like GLSs.

2. Park's Common Source Lines Are "Dummy Source Structures"

89. I understand that Patent Owner argues that Park's common source lines are not dummy source structures, because they function as a source. POR, 45-47. I disagree that "dummy source structure" should be construed such that it can never function as a source for the reasons in §V.A.2.

B. Claims 2 and 11

90. Patent Owner relies on its same argument regarding never functioning as a source, and I disagree for the same reasons. §V.A.2.

C. Claims 3 and 4

91. I understand that Patent Owner makes a similar argument for these claims as with respect to Tessariol, and I disagree for similar reasons. POR, 48-49. The figures of Park represent its design. This is clear in that Park expressly recognizes its figures are just a design and variations may result due to “manufacturing techniques.” Ex. 1005, 4:65-5:17. Thus, the design clearly indicates a repeating pattern, which again, is easy to manufacture.

D. Claim 5

92. I understand that Patent Owner advances its same construction of “surrounding” (POR, 50) that I disagree with for the reasons in §V.B.

E. Claim 6

93. I understand that Patent Owner argues that the common source lines cannot be in a row from “east to west” because they extend through the cell region. POR, 52. I disagree. I discuss the meaning of a “row” in my opening declaration. Ex. 1003, ¶ 166. The source lines are “objects” (like match sticks) arranged in a straight line from east to west. Patent Owner’s reasoning would exclude rows of certain shapes just because they happen to be long members.

VIII. DECLARATION

94. In signing this declaration, I realize that this declaration will be filed as evidence in a contested case before the Patent Trial and Appeal Board of the USPTO.

95. I am aware that willfully false statements and the like made by me in connection with this declaration are punishable by fine or imprisonment, or both (18 U.S.C. § 1001) and may jeopardize the validity of the Petition. All statements herein made by me of my own knowledge are true and all statements made on information and belief are believed to be true. I declare under penalty of perjury that the foregoing is true and correct.

Executed this 25th day of April 2025 at Austin, Texas.



Sanjay Banerjee, Ph.D.