UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

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MICRON TECHNOLOGY, INC., :

Petitioner,: Case No.

v. : IPR2024-00789

YANGTZE MEMORY TECHNOLOGIES :

COMPANY, LTD., :

Patent Owner.:

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REMOTE STENOGRAPHIC DEPOSITION OF KELIN KUHN, PhD

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Deposition of KELIS KUHN, held remotely, via videoconference at:

VIA VIDEOCONFERENCE

Pursuant to agreement, before Giselle Mitchell-Margerum, Registered Professional Reporter, Certified Reporting Instructor, Licensed Court Reporter (TN), Certified Court Reporter (GA), Certified Court Reporter (NJ), Certified Court Reporter (WA), Certified Shorthand Reporter (OR), Certified Shorthand Reporter (CA), Alabama Certified Court Reporter (ACCR), Certified Court Reporter (NM).

A P P E A R A N C E S

ON BEHALF OF PLAINTIFF:

CHRISTOPHER M. BONNY, ESQ.
ROPES & GRAY
525 University Ave, 8th Floor
Palo Alto, CA US 94301
(650) 617-4000

ON BEHALF OF DEFENDANT:

JASON LANG, ESQ.
ORRICK, HERRINGTON & SUTCLIFFE
1000 Marsh Road
Menlo Park, California 94025
(650) 614 7427

ALSO PRESENT:

ALLEN CROSS
JUAN TORRES, Document Tech

W I T N E S S I N D E X

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P R O C E E D I N G S

COURT REPORTER: Dr. Kuhn, please raise your right hand.

Do you swear to tell the truth, the whole truth, and nothing but the truth?

THE WITNESS: I so swear.

COURT REPORTER: Okay. We can start.

ATTORNEY LANG: For the record, this is Jason Lang on behalf of petitioner, Micron.

Go ahead.

ATTORNEY BONNY: Christopher Bonny, on behalf of patent owner, YMTC, and the witness, Dr. Kuhn. And I'm here with my colleague, Allen Cross, also from Ropes & Gray.

KELIN KUHN

Having been duly sworn testified as follows:

EXAMINATION BY ATTORNEY LANG:

Q. Dr. Kuhn, if we could -- I guess if we can just start, is there any reason you can't testify truthfully today?

A. There is no reason I'm aware of.

Q. And I just want to start by getting my bearings a little bit. So the '872 Patent is in the context of 3D NAND.

Is that right?

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A. That's correct. It's a 3D NAND flash patent.

Q. Okay.

And, you know, outside of this case, do you have professional experience with 3D NAND?

A. My professional experience with 3D and flash largely comes from my experience at Intel. In 2011, we finished the FinFET work and we began to work on gate all around devices. And as you know, NAND flash is a gate all around device.

And at that time, I was very attentive to the work in the 3D NAND flash field, because that was very germane to the work I was doing at Intel.

Q. Okay.

And in 3D NAND, you had mentioned "gate all around." There are memory strings, I guess, that have a gate all around?

A. I'm a little uncertain as to where the question is. Can you try again? I may have misheard.

Q. I guess you had referenced there being gate all around devices in a 3D NAND. To what were you referring?

A. In a 3D NAND flash device -- well, let me be a little more general here.

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In many types of 3D NAND flash devices, there is a vertical channel structure, and the gate encircles the vertical channel structure, or partially encircles it in some geometries, and that is actually where the transistor is.

And in general, a geometry where there is a round or square object, and the gate wraps around that object, is called the "gate all around" architecture.

Q. Okay.

And that vertical structure that you are describing, had you heard that referred to as a memory string?

A. It is common to call the vertical channel structure in NAND flash a memory string. That's correct.

Q. And typically, at the top, that memory string is connected to a bit line. Is that correct?

A. Typically, it's connected to a bit line at the top. There are geometries with a bit line at the bottom as well.

Q. And in the geometries in which there is a bit line at the top, then the bottom of the memory string would connect to a common source region.

Is that right?

A. It is -- in general, and many of these architectures, the bottom of the memory string or the bottom of the conductive channel needs to go to some sort of a source.

The exact architecture of that source varies quite significantly across the different kinds of architectures. There are some that turn around, and come back up, and weave, and things like that.

But one of the many possible versions is to have a source at the bottom of the memory string.

Q. And that version in which the source is at the bottom of the memory string, the memory string extends into that common source region.

Is that correct?

A. Extends in? Help me a little bit with what you mean by "extends in." I don't get a picture in my head when you say that.

Q. Well, I see these memory strings that extend and effectively terminate in the substrate, in a common source region of the substrate.

Are you familiar with that?

A. One of the many ways people build NAND strings is there will be some sort of a semiconductor channel material forming the NAND

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string. And that semiconductor channel material will be touching, and in electrical contact, with a material on the bottom that functions as the source.

Q. And if the common source region is the substrate itself, that substrate has to be heavily doped. Correct?

ATTORNEY BONNY: Objection. Form.

THE WITNESS: This is one of these things where there are a number of architectures out there.

In order to make a good contact between a semiconductor material and a metal, for example, you typically have to architect the doping to have a good electrical contact. It doesn't happen naturally.

ATTORNEY LANG: Okay.

BY ATTORNEY LANG:

Q. Well every reference I read, it talks about the common source region of the substrate being heavily doped. Why is that?

ATTORNEY BONNY: Objection. Foundation.

THE WITNESS: So the common source region needs to be conductive in general. Because you have a lot of NAND strings, and there is a lot of current moving in them.

And as you look over at the broader art, there is current crowding effects, and many bad things that happen, if you're trying to shove too much current through the source, into the NAND strings.

So at a high level, you want to be able to move a lot of current through your source so that it doesn't choke out. But architecturally, how you choose to do that depends on one of the myriad of different architectures.

You could have highly doped semiconductor. You could have a metal. You could have a silicide. Overall, there is this concept, current crowding.

There is a general goal to make that surface as conductive as is consistent with all the other limitations of your architecture.

BY ATTORNEY LANG:

Q. Well, so you had described this memory string having a channel material. A typical channel material is a doped polysilicon. Right?

A. A common channel material is a doped polysilicon. That's correct.

Q. Okay. And that doped polysilicon can

directly contact a doped common source region, and that would allow this electrical current you are referring to, to flow.

Is that correct?

A. It's more --

ATTORNEY BONNY: Objection to form.

THE WITNESS: It's more complicated with that. And especially with NAND flash.

Remember that if I have a doped semiconductor channel region, and I have a doped semiconductor source, I need to watch out that the doping is correct. Because I could just make a PN junction and then not have a good electrical contact.

Across the spectrum of 3D NAND flash patents I have read, I notice that there are many unusual architectures, particularly in the earlier days of NAND flash, where doping is used in different ways to achieve different effects.

So I think generally saying that I have a doped channel hitting a doped semiconductor, that may or may not guarantee a desirable contact for everything.

BY ATTORNEY LANG:

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Q. And one thing you had referred to was, you know, a metal structural contacting an undoped semiconductor substrate. And I think you referred to that doesn't form an ohmic contact.

Is that correct?

A. I actually did not say that. I think you're citing the -- in the last few minutes. I think you're citing from my declaration. Is that where we are going here?

I think we are moving from a specific -- a set of general questions to a set of specific questions. Would you like me to continue to describe things at a high level? Or do you want to go to my declaration?

Q. I can pull up -- I was actually referring to your initial declaration. And I can put that into the -- and I guess I should ask, Dr. Kuhn, do you have any notes in front of you?

A. I have five documents on my computer. All of which are unmarked. I have my two declarations. I have the patent. And I have the two prior art references. They are all the same PDF copies you have.

And I have a notepad off to one side that's blank, in case you and I need to take notes

at some point that could be added to the record.

Q. All right.

So just -- and feel free to use the copies that you have, but for the record, I'll put them into the chat. If you want to download that, you can as well.

ATTORNEY LANG: So I'll put into the chat Exhibit 2001.

(Exhibit 1 marked for identification)

ATTORNEY LANG: Which I will mark as Exhibit 1 of the deposition.

THE WITNESS: And just so that we're all clear, I'm actually going to be using the copy on my computer, which is also Exhibit 2001. It should be identical to the one you are uploading.

ATTORNEY LANG: Yep.

BY ATTORNEY LANG:

Q. And you have a -- and just so we make sure we're talking about the same thing, I can share my screen and make sure we are looking at the same part of it.

So, Dr. Kuhn, we are at paragraph 48 of your initial declaration, Exhibit 2001. And you state:

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"A contact between a semiconductor and a metal is typically not an ohmic contact."

Do you see that?

A. I do see that.

Q. And so, if I understand your testimony correctly, a metal vertical structure that simply terminates in a undoped semiconductor substrate doesn't really allow current to flow?

A. I'm going to say that slightly differently. A metal structure that terminates on a semiconductor structure is typically not a structure that flows current evenly in both directions. That is more technically described as an ohmic contact.

Typically, if you just drop a metal on to a semiconductor without thoughtful processing, you will not get an ohmic contact.

Q. Okay.

And is this the scenario of an electrical dead end that you are referring to, throughout your second declaration?

ATTORNEY BONNY: Objection. Form.

THE WITNESS: So, I'd like to see one of the cites. Because I think the answer is no. I think I'm referring to something different. But before I jump in and commit to that, can

you locate that for me?

ATTORNEY LANG: Yeah. I'll get to that in a second.

BY ATTORNEY LANG:

Q. Now, so if I understand your testimony then -- or strike that.

So if we had this metal structure into a undoped semiconductor substrate, I believe you had testified that current could flow one way. Which way is that?

A. It depends on which -- what metal you have. What the doping of the substrate is. And you will get a junction that will flow current in one or the other directions.

And it's an exponential current. If you look at my paragraph 50 above that, you'll notice I have a plot from Streetman, I believe, showing an exponential change as you go across that barrier. And I have drawn on top of it, a normal ohmic contact like a metal, which is a straight line.

So you have a junction that will typically flow current -- a significant amount of current, as the voltage increases in one direction, and will not flow much current as the voltage is in the other direction.

Q. And I guess your point is that you don't consider that to be a contact?

ATTORNEY BONNY: Objection. Form.

THE WITNESS: I do not consider that to be an ohmic contact. And I'm not alone in this.

The semiconductor community, even at the academic textbook level, in your most basic textbook, spends pages on the difference between an ohmic contact, a straight line uniform contact, and a Schottky contact, which is one that has this rectifying, or dialed-like, or unidirectional behavior.

BY ATTORNEY LANG:

Q. But my question wasn't -- you don't consider --

TECHNICIAN: Sorry to interrupt. You are sharing your screen.

ATTORNEY LANG: Oh. That's fine.

THE WITNESS: Okay. So, Jason, why don't you repeat the question? Because I thought I answered what you asked, but I may have missed it.

ATTORNEY LANG: Yeah. And I'm looking at it here.

BY ATTORNEY LANG:

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Q. My question was, I guess your point is, you don't consider that to be a contact. And you answered as if I asked about an ohmic contact.

So this vertical conductive metal structure that terminates in an undoped semiconductor substrate, is that a contact?

ATTORNEY BONNY: Objection. Form.

THE WITNESS: So I want to make sure that we are not confusing common language in the art against language in the patent.

In the art, "contact" is a very general word. You know, "contact" can be used as a noun, or a verb, or an adjective.

Ohmic contact is a much more specific word. One could call it a term of art. And it's this linear characteristic. Similarly, a Schottky contact is a much more precise term. And I'd illustrated both of those in the picture above paragraph 50.

BY ATTORNEY LANG:

Q. And so, are you reading the claim term, "conductive contact," to mean ohmic contact?

A. Okay. So now, let's talk about conductive contact. Because there has been a progression in presentation between this very early declaration and

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my later declaration.

This early declaration, as you can tell from our discussion about Schottky barriers and things like that, was largely focused to how a POSITA would think about this junction.

And if we look up at the beginning -- somewhere at the beginning, I go -- I discuss what a person of ordinary skill in the art would have understood the '872 Patent to close and teach, as it relates to the term.

Then as time passed, we jump into my later declaration, which is much more recent. And at this point, I actually take a step forward and I am construing the term as opposed to simply describing the physics around it.

So I think a key place to go is my later declaration, paragraph 95, where I am actually construing the term, "conductive contact," as a conductive structure that permits current flow with an adjoining conductive structure.

Q. Are your opinions in your second declaration consistent with your first declaration?

A. I believe so. If there is a place you think they are inconsistent, why don't you point it out and we can talk about it?

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Q. Okay. Does the conductive -- does your -- strike that.

Does your construction of "conductive contact," in your second declaration, include within its scope, a Schottky contact?

ATTORNEY BONNY: Objection. Form.

THE WITNESS: So if we step back and look at my construction, which is a conductive structure that permits current flow with an adjoining conductive structure, an ohmic contact generally meets that.

A Schottky contact may or may not meet that. And, in particular, because a Schottky contact has essentially no conduction at low voltages, if you don't know the voltages involved in your product, it would not meet that.

And last but not least, there are contacts which I did not describe in my first report, because I was being more idealistic. But there's contacts that simply do not flow current at all, for a variety of reasons, of which no doping happens to be one.

BY ATTORNEY LANG:

Q. So your construction of contact -- strike

that.

Your construction of conductor contact in your second declaration excludes certain types of contacts?

ATTORNEY BONNY: Objection. Form.

THE WITNESS: I would say that slightly differently. My construction of conductive contact excludes structures which do not permit current flow between a conductive structure and an adjoining conductive structure.

BY ATTORNEY LANG:

Q. And in that context, does a metal vertical structure extending into an undoped substrate -- does that meet your definition or your construction of a conductive contact?

A. Now, that is going to depend on the details of how that was made. If someone describes an arbitrary metal structure landing on an arbitrary substrate with no additional details, you can't determine whether it's a conductive contact. There is not enough information.

Q. What additional information would you need?

A. You would need to know the metal. Its work function. The nature of the surface it's

landing on, or in your example, embedded in. Its doping. And whether there is a presence of other materials at the surface.

Keep in mind that the interaction of a material with the surface of another material -- or more precisely, a conductive material with the surface of another material, it's that surface that matters a great deal in the art.

You can have a conductive material that is touching another conductive material, and you may not have any current flow because of the nature of that surface. If that surface is not specified, then you can't conclude that it permits current flow.

Q. Do you need additional information other than a tungsten vertical metal core, extending into a undoped semiconductor substrate? Is that a conductive contact under your construction in your second declaration?

A. I would need to know a bit more about -- you said an undoped substrate, which is unusual in the art. Is it undoped? Is it doped with -- in the center? Is it doped peripherally?

People normally don't make undoped anythings in the art.

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Q. Okay. Let's say that you had the -- the substrate has a doped common source region in one section, but yet the other section is undoped. And that tungsten vertical metal core extends and terminates into the undoped portion.

Is that a conductive contact?

A. So, the other thing you would need to know is the product voltage operating range. Given what you've told me so far, I'm tending to believe it's not a conductive contact. Because I don't believe that it's going to permit current flow under the product operating conditions, but I don't know the product operating conditions.

Q. I mean, in that situation, Dr. Kuhn, it wouldn't even make sense to use that tungsten conductive core for any purpose. I mean, why would you use a conductive tungsten core that extends into a undoped semiconductor substrate?

Have you ever heard of that being used, in all of your experience, in a 3D NAND?

ATTORNEY BONNY: Objection. Form.

THE WITNESS: I am very reluctant to try to address a question of how someone would use something when I can't think of it on the spot. You know, in looking at these various patents,

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I am repeatedly struck by, "Wow. That's kind of cool. I didn't know you could do that."

So I have trouble answering that question.

BY ATTORNEY LANG:

Q. But can you think of any time -- strike that.

As you sit here today, can you think, in the 3D NAND context, of a tungsten metal core ever terminating into an undoped semiconductor substrate and being used as a functional component?

ATTORNEY BONNY: Objection. Form.

THE WITNESS: So let me caveat this with undoped substrates are really uncommon. I am not familiar with a tungsten structure contacting a completely undoped semiconductor, having a function that would be useful in 3D NAND that is an electrical function.

BY ATTORNEY LANG:

Q. So the '872 Patent refers to only a portion of the substrate being doped. Does that mean the other portion is undoped?

A. Can you share with me where you are referencing?

Q. Sure. Do you have -- I can put this -- I'll go ahead and put this into the chat.

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A. As with the others, I have a local copy. It's Exhibit 101 and it should identically match yours. It is not annotated.

ATTORNEY LANG: I'll mark as Exhibit 2, Exhibit 1001, which is the '872 Patent.

(Exhibit 2 marked for identification)

ATTORNEY LANG: And it refers to a dope region, such as a dope region not shown in substrate 202.

THE WITNESS: Help me with where you are.

ATTORNEY LANG: I'm sorry. Column 16. Line 37.

ATTORNEY BONNY: Sorry to interject. Did you share the exhibit in the chat? I don't see it popped up yet.

ATTORNEY LANG: Yeah. It should pop up.

THE WITNESS: Okay. I am at --

ATTORNEY BONNY: Could you just pause until I have the exhibit?

THE WITNESS: Oh. Sorry.

ATTORNEY BONNY: It still hasn't popped up. Are you sure you sent it to everyone? I don't have the first one either.

ATTORNEY LANG: Oh. Maybe I didn't send it to everyone.

TECHNICIAN: I'll put it in the chat for you.

ATTORNEY BONNY: Thank you. Okay. I have it.

TECHNICIAN: Okay.

BY ATTORNEY LANG:

Q. And, Dr. Kuhn, I referred you to column 16, line 37, in which there is a doped region in substrate 202.

Do you see that?

A. Thirty-seven.

"Via a common source such as a doped region not shown is substrate 202."

Yes. I see that.

Q. Okay. And does that mean the entire substrate is doped?

A. Well, I've actually addressed this question in my declaration as well. I think it's the same question.

At paragraph 194, I do point out that localized doping regions are used in semiconductor substrates. So assuming doping is one place, does not necessarily require doping somewhere else.

Q. Right. And so, in the '872 Patent, in the regions in which are not doped, what's that

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substrate?

A. I don't understand the question. It's an undoped substrate. And I don't think that's the answer you are looking for.

Q. It is. Because you kept saying that it it's very atypical for there to be undoped --

A. Okay.

Q. -- semiconductor substrate.

A. Okay. Let me qualify this. Because this is actually important. You and I are using "doping" in two different contexts. And let me make sure we are clear about this.

Substrates, as they come, are typically doped one way or another, naturally. They come naturally with some N; or come naturally with some P; or may, in fact, have epitaxial growth on them that's naturally one way or the other.

Then we intentionally dope them one way or the other. And if we want it P doped and it's in that substrate, we put excess PN to flip it.

Your earlier questions all said "undoped substrate." And my caveat on that stands. Undoped substrates that are undoped technically -- they have no doping in them -- are very uncommon.

What we talk about as an undoped substrate

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in the art means a substrate that was not intentionally doped, but has some starting doping.

Q. Okay. What's the starting doping of the '872 substrate?

A. I don't recall. I can spend a few moments and look if you wish.

Q. Well, I don't think you'll find it. Is there a typical starting doping -- strike that.

Is there a typical natural doping on the substrate that a POSITA would understand the '872 to use?

A. If no other information is provided, it is common to assume that the doping is P type.

Q. And is the starting natural doping P type -- this testimony you had about a tungsten pillar extending into that type of doping, would that still not be an ohmic contact?

ATTORNEY BONNY: Objection. Form.

THE WITNESS: Well, first, I don't know enough about what the intrinsic substrate is to give a precise answer.

Typically, the doping level of a semiconductor substrate is relatively low. So whether it is N or P, and depending on the work function of the metal, it's probably not doped

enough to make a high-quality ohmic contact.

Whether that contact is sufficient to meet our construction of conductive contact is a little unclear, unless we knew all the numbers.

BY ATTORNEY LANG:

Q. Dr. Kuhn, have you ever heard of a contact pad?

A. The phrase, "contact pad," is used in the art, and I have heard it.

Q. Okay. And what is a contact pad?

A. In general, a contact pad is a relatively large structure, in comparison to the structures around it, where another structure -- a contact in the noun sense, touches that pad; makes contact with that pad.

And it usually is a large structure, so that variation make sure that the structure that is contacting, or landing, or in direct contact with, is within the contact pad.

Q. And are contact pads always used such that another structure makes contact with it?

ATTORNEY BONNY: Objection. Form.

THE WITNESS: So very few things are always or never in semiconductors. As a very specific example, it is not uncommon to have

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contact pins within a design that are used later in debug. And they have limited function for the product, but if the product breaks, that way, you can come in and test it.

BY ATTORNEY LANG:

Q. And it's still a contact pin even though nothing is contacting it. Correct?

ATTORNEY BONNY: Objection. Form.

THE WITNESS: This is a little bit related to our definition of "conductive contact." A conductive contact permits current flow between two different conductive structures. It's still a conductive contact even if current isn't flowing at that moment.

BY ATTORNEY LANG:

Q. But just the way that you are using the language, I'm trying to understand it. Because it's almost like if I understand your testimony, a contact pad only becomes a contact pad if something else touches it.

Is that right?

A. So I'm going to back up and make a generic comment about the word "contact" in the art. We need to be very careful with the word "contact." Because as I said earlier, it can be a noun; a verb;

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or an adjective, all in the same sentence.

The sentence, "The contact contacted the contact pad and made a good contact," is actually a perfectly reasonable general sentence in the art.

So I think we do need be cautious about general usage of the word "contact," and the specific construction that I have proposed in my declaration, for the phrase, "conductive contact," in relation to the '872 Patent.

Q. Okay. Well let's talk about contact as a noun. Would that be more specific?

A. We can talk about contact as a noun. Yes.

Q. And a contact pad, I'm using the term "contact" as a noun. Correct?

A. Actually, I disagree with that. I think "contact pad," you are using "contact" as an adjective for "pad."

Q. Okay. And you, yourself, have designed products with contact pads. Correct?

A. I certainly worked on; worked with; used; understand contact pads within a product. I can't say I actually drew one and put it -- oh, no. I did. I've done test chips. So the answer is yes.

Q. And in that work, did any of it involve a contact pad that did not have something physically,

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an adjoining structure, making contact with it?

A. Well, in a test chip, the contact pads do not have a conductive structure touching them at the time they are made. They have a conductive structure touching them later on.

Q. And then --

A. Or they may not, if the conductive structure may never touch it. It just happens to be helpful to the layout to have a contact pad in that location.

Q. And sometimes it would be helpful to have a contact pad in a particular location, just because you are going to fabricate a repeating pattern.

Is that correct?

A. It is common in the art to have structures fabricated repeatedly, because it assists other parts of the process. Polish, for example, is very fond of having multiple replicas of a structure. Some of which may not be functional.

Q. Okay.

And you had testified that sometimes a contact pad would only have a conductor structure, you know, later touching it. Did you just call it a pad, and then only when something else touched it, you said, "Okay. Now it's a contact pad?"

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Is that how you are using the word, "contact pad?"

A. Well, big long complicated question there. Let me attempt to clarify my answer.

In my mind, we were talking about contact pads, which is somewhat a term of the art. Which is where some sort of a contact pin; or probe; or something like that, may land on the pad at some point in its life.

And most of the questions I answered subsequent to that were with regards to that understanding of "contact pad." There are other understandings of "contact pad," and we may be talking at cross purposes.

Q. But I just wanted to make sure that, you know, you had testified that some sort of contact pin or probe may land on the pad. Now, it's still a contact pad before that other structure lands on it. Correct?

A. So, typically, when people are laying out, for example, a test chip and they lay out contact pads in the test chips, perhaps as probe pads, it's still called a pad, as it's being drawn and fabricated.

Q. It's still called a contact pad. Correct?

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A. A contact pad or a probe pad. Again, I am speaking specifically to the example as in a test chip, where there is a landing zone for some sort of an electrical probe or contact, and it carries the name, "contact pad," or "probe pad," or something of that nature.

Q. Okay.

Now, what is an interconnect?

A. So, at a high level, an interconnect is, I'm going to say a wirelike object that connects something to something else, with electrical current flowing between the two things.

Q. So that's kind of what "inter" and "interconnect" refers to? The notion that you are connecting two different elements.

Is that right?

A. Yes. In general, interconnect in the art, it's used mostly in the back end. But you also see usage in the front end, as we see in this patent. You are connecting something somewhere to something somewhere else.

The back end of the line layers are almost ubiquitously called "interconnects" because they connect active devices together.

Q. And what's the electrical contact?

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ATTORNEY BONNY: Objection to form.

THE WITNESS: Are we talking generically in layman's terms? Or are we talking in regard to a phrase in a patent, or other document that may have a limitation?

BY ATTORNEY LANG:

Q. I'll just start with, is electrical contact a relevant term, in the context of 3D NAND, around 2018?

A. So, do you have an example? Because this seems like an obvious question, and I have the feeling I'm missing something. Is there a quote or a citation that you are talking to?

Q. Do you, at some point, cite the definition from a dictionary, of "electrical contact?"

A. I do, indeed. That's correct.

Q. And so --

A. And let me find that so we can discuss.

Q. Yes. If you just search for "electrical," it may pop up.

A. I believe I have a dictionary. Yes, I do. The Wiley Electrical Dictionary. Is that where you are going for electrical contact? No. That's contact. You may have to help me with where I am directly referring to it.

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Q. Yeah. Let me --

A. Because Dr. Banerjee uses the term, "electrical contact." You referenced a dictionary definition. I am citing to one. But I'm not getting a close match between what you asked and what's in my report.

So I need some help here.

ATTORNEY LANG: All right. I'm going to mark as Exhibit 3 -- I think I put this into the right chat -- Exhibit 2007, which is Dr. Kuhn's second declaration.

(Exhibit 3 marked for identification)

THE WITNESS: And I believe you are citing to paragraph 110. The McGraw-Hill Dictionary of Scientific and Technical Terms?

ATTORNEY LANG: Yep.

BY ATTORNEY LANG:

Q. And so, if you need some time to read that paragraph, let me know.

A. Okay. I'd actually like to hear the question again. Because now that I know what we're talking about, I would like to hear the question in context with this paragraph.

Q. Okay. What is a electrical -- strike that.

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What is a electric contact in the context of 3D NAND, around 2018?

A. So I am going to point to the '872 Patent. And I'm going to point to the examples where the dummy source, which is not functioning as a source, is functioning as an interconnect, to connect the 3D memory device with other peripheral devices.

And I am specifically citing column 16, 65, and the next two lines, down to the end of the column. So I'm going to say that an interconnect, as used in column 16 at the bottom, is an example of electrical contact per the McGraw-Hill Dictionary definition.

Q. And it's electrical because it's an interconnect, in the sense that it's connecting current flow between two devices? Is that correct?

A. Well, it's electrical in the sense it's not spin, or magnetic loops, or things like that. These are electronic devices and they move charge carriers around. And if the interconnect is metal, the charge carriers are typically electrons.

Q. Okay.

So the term, "electric contact," is "electric" completely redundant? Or does it modify and narrow "contact" in some way?

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ATTORNEY BONNY: Objection. Form.

THE WITNESS: Well, I haven't thought about that at any level. At a -- if I take a short stab at this at a high level, as I mentioned before, the world does have things that are not electrical.

The world has -- the first examples I gave you -- you can tell I'm a device person. The first examples I gave were spin and magnetic loops. But you can also transfer heat through a contact.

You know, thermal -- there is a whole science of thermal contacts that's separate from what we are discussing here.

So there is a lot of impliedness here. These are electronic devices. They are transistors. They are moving charge around; either holes or electrons. They are not spintronic devices. They are not magnetic loop memory. And we are not talking thermal transfer.

So, I think electric is important, in that there are a whole lot of other ways you could contact stuff. But I think it does not appear expressly in '872, because it is within the

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context of an electronic device.

So electric is kind of assumed.

BY ATTORNEY LANG:

Q. So in a sense, a contact forms a pathway and -- strike that.

So in a sense, a contact forms a pathway or a junction, and depending on the mechanism -- the physical mechanism -- it could be electrical. It could be something else -- this pathway is what allows a transfer through the pathway?

ATTORNEY BONNY: Object to form.

THE WITNESS: So I do want to make the caveat that contact has this multiple meaning problem. As I said before, in the art, you can have the contact as a noun. You can have the contact as a verb. You can have the contact as an adjective.

If we look at my construction of conductive contact, there, I have tried to be specific. I will say I didn't use the word, "electronic," but it's a conductive structure that permits current flow within an adjoining conductive structure.

And there is the implication by "current flow," I mean electronic current flow; holes or

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electrons, as opposed to, you know, water; or thermal heat; or phonons; or Lord knows what else. It's just, you know, the electronic carriers.

BY ATTORNEY LANG:

Q. So does a contact pad that does not have an adjoining structure connected to it meet your definition of a conductive contact?

ATTORNEY BONNY: Objection. Form.

THE WITNESS: If you have a structure that does not permit or allow current flow with an adjoining structure, then I don't think it would be a conductive contact.

For an example, if I make a ring of copper, just sitting there on top of an insulator, I could call that a contact pad. I'd probably call it a dummy contact pad, but let's let that by.

But it would not be a conductive contact, by my construction, because it's just sitting there all on its lonesome. It's not a structure that is permitting current flow with another structure.

BY ATTORNEY LANG:

Q. Are you familiar with the gate line

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replacement process in 3D NAND?

A. Yes.

Q. And are you familiar with gate line slits?

A. I'm familiar with them as they are described in the '872 Patent.

Q. Is "gate line slits" not a term of art?

A. Well, that's a good question. Gate line slits is certainly referenced in the '872 Patent. I've certainly seen it in a number of other publications. I haven't opined on whether it's a term of art of not.

Q. What's your understanding of what a gate line slit is?

A. As described in the '827 Patent, the gate line slit -- and let me find the exact location here, because they go into some detail. Hold on a second. Let me make sure I find the right place.

Column four has a nice summary, starting at line 30, speaking to the gate replacement process. And as you run down that summary, it says:

"Expressly, for example, in some 3D memory devices, such as charge trap, 3D NAND memory devices, gate line slits are formed to divide an array of memory strings."

And then I'm going to skip some of the

rest of it --

"...into different memory regions. Often, a gate line slit has large dimensions that's filled with an insulating structure, and so on."

This section also describes the gate replacement process. And I think where you are going with your question, the use of gate line slits, to perform the gate replacement process.

Q. And just to make sure we are on the same page, the gate line replacement process, you know, assumes that you have a stack of dielectric and sacrificial gate layers. Correct?

A. That's an interesting question. It is generally the case that the -- I don't know. That's a really good question. Let me qualify my answer.

In a 3D NAND memory structure, where we are creating NAND strings with a vertical channel, and we are using a replacement gate process, we are creating layers of -- at the beginning, which are sacrificial layers and insulating layers, in a layered cake. And that's correct.

Q. Okay.

And then this process involves etching the gate line slits, which are voids in that stack. Correct?

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A. Yes. There is a variety of ways to do this. The core problem here is you need to remove all that sacrificial material, somehow. And so, you have to pull it up through something else.

And one of the many techniques that exist in the art is to use the gate line slit as a way of getting that sacrificial material out, and then putting your final material in.

Q. But you are saying pulling it out, when, in fact, you actually source etchings into those gate line slits to etch out the sacrificial gates. Correct?

A. I do want to clarify something here in responding to your question. We've got -- in addition to four uses of the word, "contact," we have two uses of the word, "source."

I do want to clarify that the '872 Patent exclusively uses the word, "source" to describe the source of a transistor. I believe in the sentence you just said, you are using source in a fabrication context.

So I just want to clarify that the way I would say this is that you are using an etchant to remove the sacrificial material. Sometimes I say "suck out," which is not exactly correct. But it's

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typically, although not always, a wet etch, it removes the sacrificial material.

Q. And what's the source of the etchant?

A. The etchant is whatever process is being used. Sometimes it's a wet etch. And in my experience, it's almost always a wet etch. But I recognize I've read some patents and I've seen some art that suggest dry etches can also be used.

Q. I'm not sure how effectively. Where does the etchant come from?

A. Whatever etch chamber the thing is in.

Q. There is a source --

A. If there is --

Q. You agree there is a source of etchant somewhere?

A. So the tool itself delivers etchant, whatever it is. Whether it's a vapor; or a plasma; or a liquid, depending on whatever process is being used.

The tool that the wafer is sitting in delivers that etchant to the sacrificial layers in some fashion. Depends on the tool. Depends on the technology.

Q. All right.

ATTORNEY LANG: Well, I was going to pull

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up another exhibit now, so I don't know, kind of around about how often you want to take breaks?

THE WITNESS: This is a good point for a break. I was about to ask for one. I glanced at the clock and my tea is empty. Want to do 10 minutes, just for a bio break and tea?

ATTORNEY LANG: Yes.

THE WITNESS: Sounds good.

ATTORNEY LANG: We can go off the record.

COURT REPORTER: Okay. We are off the record.

ATTORNEY LANG: Thank you.

(Short break.)

COURT REPORTER: We are back on the record.

BY ATTORNEY LANG:

Q. Dr. Kuhn, are you familiar with the term, "completely surrounded?"

A. That term appears in many places in the documentation for '872. We discussed that.

Q. Okay. And are you familiar with the term, "partially surrounded?"

A. Okay. So let me back up. I have the feeling you are about to reference some location

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somewhere. Could we go there? Because my memory may be failing me and I may be making random statements that aren't precisely correct.

Q. Sure. And I don't believe you have this one, so I'm going to put it in the chat for you.

A. All right. Let me figure out how to get it out of the chat.

ATTORNEY LANG: And I'll mark as Exhibit 4, U.S. Patent No. 9,129,827.

(Exhibit 4 marked for identification)

THE WITNESS: Okay. I think I downloaded it. No. Let me try that again. Well, I have it open, so I did something right.

ATTORNEY LANG: Great.

BY ATTORNEY LANG:

Q. And Exhibit 4, Dr. Kuhn, I assume you recognize it. It seems to be one of your patents.

A. I do, indeed.

Q. And do you recall what this technology relates to?

A. As I recall, we were making an SOI-like structure, by reacting the piece underneath the device itself.

Q. Right. I assume that's safe to say it's semiconductor technology?

A. Yes. Sorry. I may -- I actually gave a little too much detail.

Q. Okay. Now, I'd just like to direct you to column 13, line 51.

A. Okay. So I am at column 13. There is a sentence that starts at 50 and goes for a while. Is that the sentence of interest?

Q. Yeah. And, in particular, there is a term, "completely surrounded."

A. Yes.

Q. Do you see that?

A. I will actually read the sentence into the record.

"In one embodiment, the channel region of each nano wire is discreet in that it is completely surrounded by the gate electrode stack without any intervening material, such as underlying substrate material or overlying channel fabrication materials."

Q. Okay. And now, I'd like you to go to column 10, line 27 through 28.

A. In the version I downloaded, that's highlighted. Is that where you are going?

Q. Oh. That's fine. Yeah.

A. Okay. There is a highlighted section that

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states, "With a gate electrode at least partially surrounding a portion of the channel region."

Q. Okay. Now, and I believe this is referring to Figure 4A. Correct?

A. That's what the section is entitled. The section begins with Figure 4A -- not entitled, but that's the contents of that section. That's correct.

Q. Okay. And if we go to 4A -- and I am showing you my screen here?

A. Okay. Give me a second.

Q. As I understand it correctly, you describe the gate electrode partially surrounding the channel region, as shown in 4A?

ATTORNEY BONNY: Objection. Form.

THE WITNESS: So this section here is around, or is describing 4A. And I want to be careful here.

"As can be seen, the semiconductor device formed in the example embodiments illustrated includes a FinFET having a semiconductor body (Fin), formed on a buffer layer, and configured with source drain and channel regions, with a gate electrode at least partially surrounding a portion of the channel region."

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I realize I didn't answer your question, but I'm trying to put your question in context. So could you re-ask it?

ATTORNEY LANG: Yeah.

BY ATTORNEY LANG:

Q. And my first question is, so your opinion with respect to "surrounding" in the '872 Patent, are you reading "surrounding" as completely surrounding? Partially surrounding?

There seems to be these different versions that you refer to.

A. So my --

ATTORNEY BONNY: Objection. Form.

THE WITNESS: -- opinion with regards to the '872 Patent is formed upon the language within the '872 Patent itself. I formed that opinion based on the specifications; the images in the patent which are part of the specifications; and on the claims themselves.

I did not form that opinion based, perhaps, on language used in a gate all around patent in April 2012.

BY ATTORNEY LANG:

Q. So you didn't just use a plain and ordinary meaning of "surrounding?"

ATTORNEY BONNY: Objection. Form.

THE WITNESS: I used a plain and ordinary meaning, as interpreted by a POSITA who is reading the language in '872. One can actually argue that my gate all around patents are less the plain and ordinary meaning than what is done in '872.

ATTORNEY LANG: Okay.

BY ATTORNEY LANG:

Q. And in the '872, does "surrounding" mean "fully encircling?"

ATTORNEY BONNY: Objection. Form.

THE WITNESS: So in '872 -- and let me jump to my declaration here. Because '872 is quite careful about how it defines "surrounding."

Give me a second. My computer just did something wonky, and I think maybe when I downloaded that patent, I did something bad. So let me fiddle for a moment and then recover this.

Okay. What I'm doing is I'm opening up my '872; the longer declaration. And -- hang on. I'm trying to get it to open. And I'm going to be going to the section starting on page 38,

where I discuss "surrounding" in some detail.

And in particular, what I am doing in this section is I am interpreting the plain and ordinary meaning of "surrounding" and of "between," based on the language in the patent.

And with regards to your point of a minute ago, I am agnostic to the fully encircling language. This is mostly a discussion about "between" and "surrounding."

BY ATTORNEY LANG:

Q. So did the specification confirm the plain and ordinary meaning? Or did you -- you said you interpreted the plain and ordinary meaning. I'm confused by what -- your process.

A. So -- and I may have the wrong legal words for this, so be patient with me.

There is kind of two types of plain and ordinary meaning. There is a layman's plain and ordinary meaning, which is what you get when you stop someone coming out of McDonald's and ask them what something means.

And then there is a plain and ordinary meaning, as recognized by a POSITA, in the context of the patent. And I'm doing the second one. There is -- the way the term, "surrounding" is used in the

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patent is not at odds with the layman's plain and ordinary meaning.

But the patent has been very specific about what "surrounding" means versus what "between" means, to a level that I think is greater than you get just asking somebody coming out of McDonald's.

Q. Okay. We'll get to that later.

And back on Exhibit 4 --

A. Was Exhibit 4 my patent?

Q. Correct.

A. Okay.

Q. The '827 Patent. And that --

A. Oh, sorry. My bad for asking that. This is funny. There is an '827, which is the Cappellani Kuhn patent, and there is '872, which is the patent at issue.

When you said "your patent," which one did you mean?

Q. The '827.

A. Okay.

Q. The one where you are an inventor.

A. All right. We are good.

Q. Okay. So if you could go to column five? Line 50. And I'll share my screen just to make sure you are looking at the same spot.

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A. Okay. Various conductors. Okay. Yes. We are looking at a spot that says, "various conductors, e.g. runs and contact pads."

Q. And you had testified a bit earlier about contact pads. Do you recall that testimony?

A. I had testified about contact pads. And at the time we were talking about it, I was primarily testing about -- testifying about them in their usage as a probe pad. That's correct.

Q. Okay. And I guess the contact pads here are conductive material? Is that correct?

A. So, it has been a long time since I've looked at this patent, but the sentence says "various conductors, e.g. runs, contact pads, et cetera."

So I think that would be interpreted that the contact pad was conductive. Or was a conductor, more correctly.

Q. And what -- what's the adjoining structure that contacts the contact pads in your '827 Patent?

A. The '827 Patent does not discuss contact pads.

Q. That's --

A. Oh. I'm sorry. My bad. My bad. I just pulled an '872, '827 flip. Repeat the question

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again and I will stop switching it with the other patent.

Q. Yeah. What's the adjoining structure that makes contact with the conductor contact pad in your '827 Patent?

A. It's not specified. "Contact pad" is used very generically in this sentence.

Q. Okay.

And is it still a conductive contact pad if an adjoining structure does not make contact with it?

ATTORNEY BONNY: Objection. Form.

THE WITNESS: And the computer glitched just the moment you said something, so I got the last half of it. One more try?

ATTORNEY LANG: Sure.

BY ATTORNEY LANG:

Q. Now, the conductive contact pad in your '827 Patent is still a conductive contact pad if adjoining structure does not make contact with it. Correct?

ATTORNEY BONNY: Objection. Form.

THE WITNESS: So first, if we look at the language of the '827 Patent, the exact sentence we are discussing is, "various conductors,

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e.g., runs, contact pads, et cetera."

All that this patent is describing is that there is a structure called a "contact pad," and it's a conductor. I'm not sure contact pads are even drawn in here.

If you look at the paragraph:

"At a broader perspective, once fully formed, the device layer may include, for example, active componentry such as transistors and/or diodes, and may further include passive componentry as well, such as capacitors, inductors, and various conductors, e.g. runs, contact pads, et cetera."

That's pretty generic. It's not at all clear what specific structure is meant by "contact pad."

BY ATTORNEY LANG:

Q. I'm just trying to help us establish a simple point. It is still a conductive contact pad, regardless of whether or not an adjoining structure connects to it?

A. So first --

ATTORNEY BONNY: Objection. Form.

THE WITNESS: -- the language, "conductive contact," is language that we are construing

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for the '872 Patent. And second, this patent -- which I don't believe even uses that language, but we can check -- but this particular sentence in here is on a different topic, unrelated to our discussion.

You know, the words -- as I've said before, the word "contact" is really common. All this sentence seems to say is that there are conductors on the wafer, and we will call some of these conductors "contact pads."

It's unclear how this couples to the '872 Patent, and the very specific language that's used in that patent.

BY ATTORNEY LANG:

Q. Is the, quote/unquote, "contact pad" in the '872 Patent still contact pad, even if an adjoining structure doesn't ultimately make contact with a respective pad?

A. Can you check your realtime? I want to make sure you have the right patent number in that.

Q. Oh. I'll strike the question.

Is the, quote/unquote, "contact pad" in the '827 Patent still a contact pad, even if an adjoining structure doesn't ultimately make contact with the respective pad?

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A. I have no idea -- sorry. That's not the correct statement.

I no longer remember, is more accurate. I no longer remember what I had in mind when we wrote this sentence, "contact pads," et cetera.

I think we would need a picture of the structure to answer that question accurately. Because as I've said several times in this deposition, "contact" is used in a number of ways in the art.

A contact pad can have a number of meanings. When I answered these questions earlier in my testimony, I had in mind a probe style pad. I no longer remember what the word "contact pad" meant at the time we were putting together this patent. This patent is 13 years old, or something.

ATTORNEY LANG: I'm going to put Exhibit 5 -- I'm going to put this in the chat too, Dr. Kuhn.

(Exhibit 5 marked for identification)

ATTORNEY LANG: This is -- I don't think you have it.

THE WITNESS: Okay. Hang on a second, let me close these down.

ATTORNEY BONNY: And just a reminder. If

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you could just make sure that you leave enough time for me to lodge an objection if I have one.

THE WITNESS: Yes. Thank you for reminding me. I get all wrapped up in Jason's questions and forget to give everybody time to do what they need to do.

Jason, I'm not seeing any -- oh yes, I am. Is this '059?

ATTORNEY LANG: No. This is -- yeah. '059. Yeah. Yeah. It's the application 2022/0059656.

THE WITNESS: Okay. I'm having a little static on you. Is it me? Or is it you? Can other people hear Jason's static.

COURT REPORTER: Yes, Mr. Lang. Your audio isn't very good right now.

ATTORNEY LANG: I'll mark as Exhibit 5, U.S. application 2022/0059656. Dr. Kuhn is listed as the inventor.

BY ATTORNEY LANG:

Q. Dr. Kuhn, have you had an opportunity to open Exhibit 5?

A. I have it open. I have it on the screen.

Q. Okay.

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And you are an inventor of -- or a listed inventor on this patent application. Correct?

A. That's correct.

Q. Do you recall Exhibit 5?

A. Yeah. This is one of several patents we did at this time, where we were putting string layers on FinFETs to strain the FinFET itself. And there's several that are very similar.

I remember the group of them. Right this second, I'm having trouble differentiating which specific one it was, but I certainly remember when we did this.

Q. And I think you had mentioned, your FinFET work is relevant to your experience on this case. Correct?

A. I actually had not intended that implication I think the way you mean it. Let me clarify it.

Clearly, FinFETs are relevant to the case because they are an example of a 3D device. But when I was answering the question about work I had done for NAND, that was gate all around work, that work all followed the work I had done on FinFETs.

Q. Okay. And I just have a couple questions about paragraph 63.

A. Okay. Paragraph 63.
Q. I've highlighted it for you.
A. I have to laugh. I should go down memory lane when I look at these.
Q. Okay --
A. It's easy to get distracted. Let me find paragraph 63.
Okay. And it actually has a highlight on it as well.
Q. Yeah. And I should not that for the record, there is some highlighting on these exhibits.
A. So I am looking at paragraph 63.
Q. Okay.
And I notice that you mentioned there, "metal contacts." Do you see that?
A. I do see that.
Q. And then it continues -- I'll just read the sentence for the record.
"In this case, back end techniques can be utilized to form metal contacts, metallization layers, and interlayer dielectrics to interconnect various transistors together into functional integrated circuits, such as microprocessors."
Do you see that?

A. I do.

Q. And I guess the point is, is that these are the techniques that ultimately function as this interconnect that connects the two devices together, for example?

A. So, I disagree a little bit with your read of that sentence. I read that sentence as more a definition of what back end technique is.

That back end techniques includes the metal contact, metallization layers, interlayer dielectrics, and include the interconnect function, as we have talked about before.

That the use of the word, "interconnect" is commonly connected to the back end of the line, which I mentioned earlier in my testimony.

Q. And here, "interconnect" is being used as a -- is it being used as a noun or a verb?

A. In this particular sentence, it looks like "interconnect" is being used as a verb.

Q. Okay. And so, "interconnect" as a verb is referring to the fact that you are connecting two devices together.

Is that right?

A. Yes. In this sentence -- the sentence is a little strange, by the way. Because it says,

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"metallization layers and interlayer dielectrics to interconnect," where one can argue that an interlayer dielectric is not a connector.

But I think at a higher level, this is a more generic description of the back end, where metallization layers can interconnect various transistors together, which is a common description of the back end.

Q. And so, "interconnect," as a verb, is referring to these -- getting these two devices to connect to each other, but as a noun, is referring to actually the structure that connects the two devices.

Is that right?

A. When you typically see these back end of the line descriptions, your statement is accurate. "Interconnect" is used to describe the structure, and interconnect, or the interconnects. But they also, as with "contact," use as -- for example, here as a verb, to interconnect the transistors together.

Q. Now, I'm going to shift to the '872 Patent.

A. May I close down the '656 Patent?

Q. Sure.

And I'll mark as Exhibit -- well, I don't

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need to do that. I already -- I think it's Exhibit 2, Dr. Kuhn. Exhibit 1001, the '872 Patent, I had some questions about.

A. I have that open.

Q. Okay. I just want to start with the figures.

A. Okay. Did you have a particular one in mind.

Q. Yeah. Figure 1A.

A. I have Figure 1A open.

Q. Okay.

And if you need to reference the patent, just let me know. The specification. But 116 is referring to the inner region. Correct?

A. So, I -- let me double-check these. Off the top of my head, 116 is the array. But I believe they may have a different word. So just give me a moment to get organized so I can check these as I go.

[Witness reviewed document.]

A. Yes. You are correct. In some embodiments, inner region 116. So inner region 116. And let me specifically put your attention to column six.

"Memory region 150 may include an inner

region 116, also known as a core array region."

Q. Okay. And this core array region is where the memory strings are. Right?

A. Typically, that's correct. There may also be dummies there. But the active arrays will be in there as well.

Q. Okay. Why may there be dummies in the -- in the memory array region?

A. So --

ATTORNEY BONNY: Objection to form.

THE WITNESS: Let me be a little careful here, because I may have generically answered a question that is not relevant to the '872 Patent.

So let me stick with what the patent itself says, as opposed to a broader answer that covers many kinds of embodiments of other things.

The '872 Patent specifies this as a core array region, and specifies that the memory strings are within that region and may be arranged in any suitable pattern.

Did that answer your question? Or did I get sidetracked?

ATTORNEY LANG: It answered it. I'm just

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writing something down.

BY ATTORNEY LANG:

Q. Now, in a real device, are there more memory strings than what are shown in 1A?

A. In a real device, if it's offered for sale, there should be.

Q. I mean, there might be billions. Right?

A. These memory strings in real life, in modern devices, are very large. Not the strings themselves. The size of the memory array can be very large.

Q. Over a million. Right?

A. I'd have to look at today's specs for exactly how many they have. But will you accept very large?

Q. Yes.

Now, I just want to get to some basics here. How is the memory strings laid out? Like in what type of pattern, typically?

ATTORNEY BONNY: Objection. Form.

THE WITNESS: So I have seen different patterns in the course of this case. I haven't spent any time thinking about them for this deposition.

They are certainly arranged in an array,

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but I don't think I can speak more carefully to, you know, whether the array is a hexagonal array, or closely packed cubic array, or whatever. The patent simply says "array."

ATTORNEY LANG: Okay.

BY ATTORNEY LANG:

Q. But in the picture, they at least look like they are equal distance apart in the X direction. As a POSITA, would you understand the memory strings to have a repeating pattern in the X direction?

ATTORNEY BONNY: Objection. Form.

THE WITNESS: So one of the problems with patent pictures is that the patent pictures are repeatedly stated to not necessarily be to scale.

Now, that being said, I think a POSITA, using their knowledge of NAND flash, would recognize that 116 is an array; and that array repeats; and that array is probably a regular pattern.

But whether this particular block has a gap in it, or something, is unknown.

BY ATTORNEY LANG:

Q. But, Dr. Kuhn, you are well aware of the

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fact that it is much easier to fabricate repeating patterns than irregular patterns in semiconductor fabrication?

A. You know, I had to laugh. I think the via patterning people would object to that. That point, I think, is more debatable than you might think. I am willing to say that there is a regular pattern in 116. I'm less willing to admit that regular patterns are somehow intrinsically easier to make.

I can think of examples from my own experience, where regular patterns are actually very hard to make, because they are on a very tight pitch and they have huge patterning issues.

Q. So when you rang up hundreds or millions of elements in semiconductor fabrication, they are just randomly spaced apart from one another? That's typical?

A. So when you are designing a chip with thousands or millions of devices, there is a lot of attention spent on secondary manufacturing issues. And I'll list a few.

There is the patterning problems I mentioned earlier. You know, sometimes regular arrays are harder to pattern than certain kinds of distributions because of interactions between the

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elements.

You can get interesting standing -- and that's not quite the right word -- but you can get interesting lithographic effects that are undesirable when you have something that's regular or semi-regular.

There are, you know, issues or challenges with etch and polish with certain kinds of layouts. I certainly remember in times at Intel where we would have elaborate computer models to check layouts, because it is not intuitively obvious that a certain layout has desirable properties until you model it.

You know, humans like certain kinds of things and humans can be wrong. And so, there is sometimes a significant amount of computation required to figure out if a particular layout is going to have a particular issue.

Q. But as a POSITA, you look at Figure 1A and you recognize that the memory strings are fabricated in a pattern?

A. So the little block 116 clearly has a pattern. How that pattern replicates is unclear. As one specific example, that you could have a block of 116 to the right with a space in between, for

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some manufacturing reason, that is not apparent, just glancing at the figure.

Q. And you had mentioned some problems with fabricating a pattern. One is that on the edge of that pattern, there is often edge defects. Correct?

A. Edges of just about everything have edge effects. That's correct.

Q. And the staircase region is region 118 in Figure 1A. Right?

A. Let me just double-check that. Yes. And I cite you to column six, line 19. The outer region 118, also known as the "staircase region."

Q. Okay.

And now, 116, we had talked about a doped -- additionally doped substrate region. And 116 is going to have a doped common source region underneath it. Correct?

ATTORNEY BONNY: Objection. Form.

THE WITNESS: May or may not. It needs a source somewhere. But I don't recall from the patent, whether the region under 116, the source architecture is precisely defined.

BY ATTORNEY LANG:

Q. Well, maybe you need to look at the other figures. I don't --

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A. I actually am looking at the other figures. What's the staircase --

[Witness reviewed document.]

Q. And it might help you to direct you to column 16. Line 37.

A. One second. Column 16, line 37, says:

"Source structures formed in the inner region may be connected with surrounding channel structures via common source such as a doped region not shown in substrate 202."

So I do agree, based upon column 16, that there is an option of a doped source region, but the language does not limit it to a dope source region.

Q. And you notice it says, starting at -- I believe you started reading at line 34, "source structures formed in the inner region may be connected with," yadda, yadda, yadda, "such as a doped region."

And the inner region is 116. Correct?

A. The inner region is 116. That's correct.

Q. Okay.

So going back to Figure 1A, the '872 Patent discloses that the substrate in region 116 may be doped?

A. Yes. Due to the language, "such as doped

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region not shown." It does not however, limit it to a doped region. Other options are permitted by this language.

Q. Okay.

And you had testified earlier about localized doping. Is that what you were referring to when you doped a substrate region, such as 116, to form a common source?

ATTORNEY BONNY: Objection. Form.

THE WITNESS: When I refer to localized doping, I'm referring to that as more of a generic concept. That it is possible to form localized doping regions within a semiconductor product.

I was not intending in that discussion to point out any specific region as, for example, somewhere within 116.

ATTORNEY LANG: Oh. Okay. I meant more 116 relative to the whole substrate.

ATTORNEY BONNY: Objection --

ATTORNEY LANG: Yeah. And I'll formulate a question.

THE WITNESS: Yeah. Let's try that. I'm not getting it.

BY ATTORNEY LANG:

Q. Now, there's two regions of the device 100, looking at Figure 1A. Region 118, the staircase region. And then the inner region, 116. Right?

A. That's correct.

Q. Okay.

And the '872 discloses as an example, the substrate in region 116 being doped?

A. Or it could be doped. It disclosed it as an option.

Q. Okay.

And the '872 Patent never discloses as an option, doping region 118; does it?

ATTORNEY BONNY: Objection to form.

THE WITNESS: I don't believe it either discloses it or limits it. I don't believe it discusses it either way.

ATTORNEY LANG: Okay.

BY ATTORNEY LANG:

Q. And if 118 was doped along with 116, then a dummy source structure in 118 could connect to the common -- via the common source region that's memory cells?

A. Hold that question for a second. Because I've got stuck on your previous question and was

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checking to see if there was any other disclosure of doping.

So why don't you try that question again? Because I'm now attentive.

Q. Okay. Now, I'll start with an earlier foundational question.

Because the '872 Patent discloses an option of 116 being doped -- the substrate being doped -- that allows a connection through the substrate to the memory cells?

A. So, the language in column 16 is reasonably precise, that the common source is what's under discussion, and that one option is a doped common source region.

Q. And that enables those dummy source structures to connect to the memory strings?

A. It doesn't enable dummy source structures to connect to the memory strings. It enables real source structures to connect to the memory strings. I'm missing something here.

Q. Okay.

So, because you have the substrate doped, it allows the dummy source structures to connect to the memory strings?

A. You --

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ATTORNEY BONNY: Objection.
THE WITNESS: I don't know if it's misspeaking or -- you keep using the word --
ATTORNEY LANG: Okay.
THE WITNESS: "-- dummy source structure."
ATTORNEY LANG: Okay. Let me strike -- I'll strike it. Let me strike it and ask again.

BY ATTORNEY LANG:

Q. Because the substrate in region 116 is doped, it allows the source structures to connect to the memory cells?

A. Yes. As disclosed in column 16, the common source in region -- inner region 116 can be a doped region. A doped region which just happens to not be illustrated.

But they are pretty clear in column 16 that it's a common source region. It may be a doped region. And that this applies -- let me be careful here. Yes. And that it applies to source structures in the inner region.

Q. And does the '872 Patent disclose that the substrate in region 118 may be doped?

A. I do not recall if it discloses it or describes it in any way. I checked a few minutes

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ago, and it did not jump out at me. If you have a location where you believe it's disclosed, we can talk about it. But I don't think it says either direction.

Q. Okay.

And, therefore, if the dummy source structure contacted a undoped substrate in 118, your testimony would be that it wouldn't be able to connect to the memory channels?

A. So, I actually have that condition described in my deposition, which I think is the same thing you are talking about. And I reference my paragraph 194.

"For example, localized doping regions are used in semiconductor substrates, which makes it inappropriate to assume that the properties of the region under dummy structure 60 would meet the requirements for a conductive contact."

I believe that's the same point you are making; is that the fact that the substrate is doped somewhere does not mean it's doped everywhere.

Q. Right. And basically, because 118 is not doped, you end up with that dead end scenario that you were talking about in your declaration?

A. Well, I disagree with that question.

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Because I don't think we know if 118 is doped or not. And I also disagree because I don't believe we've talked about dead end yet. So we are using a word that we have not discussed.

Q. Okay. Well, we can get to that, because you discussed it in your declaration.

A. I have. But we have not yet discussed it in my testimony. And it's kind of embedded in a more complicated question.

Q. Now, let's go to Figure 2L.

A. Hang on a second. I just had something crash. Figure 2L of '872?

Q. Yes, Ma'am.

A. I have Figure 2L.

Q. Does Figure 2L depict a finished device?

A. I don't know. Let me check.

[Witness reviewed document.]

So the only reference to Figure 2L that might clarify that is column 16.

"As illustrated in Figure 2L, a contact 244 is formed within spacer 242."

Then there is a bunch of detailed discussion.

"A dummy source structure is formed in the source hole."

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And a bunch of discussion. There is a discussion of embodiments. There is a discussion of more embodiments. There is a discussion of more embodiments.

It's unclear for me, reading this, that whether it is complete or not complete. Is there perhaps a place that you want to reference, that supports one or the other of these points?

Q. I'm just looking at, you know, from the perspective of a POSITA, when you look at Figure 2L, is there going to be any additional layers added to the top of that.

A. So, it's certainly clear that Figure 2L is further along in the process than Figure 2K. But it is not clear -- in fact, it is perhaps intrinsically clear, that there is more stuff to follow, because many of the additional structures that occur, bit lines in the light do not appear to be shown.

However, the patent is not clear if it's describing a partial section of a completed structure, or a structure partway through fabrication.

I would have to look at this in some detail to figure it out. Because the way this patent is structured is, they talk about 2L, and

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then there is like three pages of embodiments. So it's difficult to do this on the fly.

Q. So, and Figure 2L, this is in the staircase region 118 that we had talked about earlier. Correct?

A. Yes. Figure 2L is in the staircase.

Q. And you had testified that you don't know that the substrate portion, 202 and Figure 2L, whether it's doped or not?

A. I have not found any language in the patent, sitting here today, to clarify that. You and I clarified the doping in the array region, but there does not appear to be enough information, either way, in the staircase region.

Q. Okay.

And where is the -- between what two points do the current flow with respect to element 244 in 2L?

A. Is this in regards to the construction of conductive contact?

Q. No. I'm just asking from the perspective as a POSITA, is there two points in which current is flowing from and into 244 and out of 244?

A. So 244 is as illustrated, just in Figure 2L. If a POSITA is looking just at Figure 2L

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and looking just at element 244 without reference to anything else, it would be difficult for a POSITA to understand other potential wiring around 244.

Q. So there could be a wire on the top of 244 that's not shown in 2L?

A. One can speculate there could be all sorts of things. I mean, there could be a layer of silica nitride on top of that too. It's a little unclear to me how we would speculate beyond what the patent has illustrated and described.

Q. Now, typically, if you look at Figure 2L, you would expect there to be an inter layer -- a dielectric inner layer -- deposited on top of what you see in Figure 2L. Correct?

A. So, Figure 2L shows a 244. And just for the record, 244 is a contact structure. And a -- so a conductive material is in 244.

And in 244, it's ambiguous as to it is not clear in that picture what is connected to it, although there is a description elsewhere. So at this point, I mean, we could speculate anything we wanted above that.

You know, you asked if we could speculate an ILD layer. We could certainly speculate an ILD layer, but I'm not sure quite where you are going

with this question.

Q. And then, if you had an ILD layer, then you could have contacts through the ILD layer or -- strike that.

If you had an ILD layer on top of what you see in Figure 2L, you could have interconnects between the ILD layer and the vertical structure shown in Figure 2L?

A. So the patent reads at -- in column 16:

"When conductive materials are used to fill dummy source hole 212, e.g. contact 244, the dummy source structure may function as an interconnect to connect 3D memory devices with other peripheral devices."

So the patent is clear that this may function as an interconnect. The patent is not clear as to exactly how this could be done.

Q. Is there a preferable device shown in Figure 2L?

A. No.

Q. Where would a preferable device be in Figure 2L, if one were to place a preferable device in 2L?

A. Well, you have two choices.

ATTORNEY BONNY: Objection. Form.

THE WITNESS: You place it underneath the array, or you place it above the array. I suppose you could also place it to the left; and the right; and the top; and the bottom of the array.

The peripheral devices in the art these days can be placed on all sides of the structure, above it and below it.

ATTORNEY LANG: Okay.

BY ATTORNEY LANG:

Q. So in Figure 2L, it would either be above it or below 202. Is that correct -- strike that.

The peripheral device, if it was in Figure 2L, would be above what you see or, in fact, be below 202?

A. Or it could --

ATTORNEY BONNY: Objection. Form.

THE WITNESS: -- be to the side.

BY ATTORNEY LANG:

Q. Or to the side?

A. Yeah. The patent is clear that you can connect to a peripheral device. But in glancing through the patent, I'm not aware that they specified whether the peripheral device is above, or below, or to the sides.

Keep in mind that there is examples of all of these in the art. You know, memory arrays that historically had peripheral devices on the edges. They have had peripheral devices above. And in more recent years, they have had peripheral devices below.

So I don't think we can take Figure 2L and assume either above or below, because all of these options are possible in the art.

Q. If we go to Figure 3, this kind of summarizes the process for making the general structures described in the '872 Patent. Correct?

A. Figure 3. Yes. Figure 3 is the flow chart. That's correct.

Q. Okay. And you see in step 304 where it says, "dummy source holes were formed?"

A. Yes, I do. 304 states:

"From a plurality of dummy channel holes in a plurality of dummy source holes in the staircase structure."

That's correct.

Q. Okay. And then in step 310, a spacer is formed in the dummy source hole. Correct?

A. 310 itself simply says, "form a spacer." That's correct.

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Q. And then 312 says, "form a contact within the spacer and each of the dummy source holes." Correct?

A. You read that correctly. That's correct.

Q. Okay.

Now, where is the adjoining structure for the contact formed in the process described in Figure 3?

A. When you say "adjoining structure," are you referencing the construction for a conductive contact?

Q. Yes.

A. Okay. And your question is if we look at the flow chart 300, which -- your question is, which two are the structures? Is that the way the question is being formed?

Q. In Figure 3, where is this adjoining structure formed that you are talking about?

ATTORNEY BONNY: Objection. Form.

BY ATTORNEY LANG:

Q. It's not in Figure 3, is it?

A. I'm checking the specification for Figure 3.

[Witness reviewed document.]

A. So, I'm referencing column 12, referring

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to Figure 3. "Method 300 starts at operation 302." And I do point out that in column 12 above, it says:

"It is understood that operations shown in Methods 300 and 400 are not exhaustive and other operations can be formed as well, before or after in between any of these operations."

So then, back to column 12, line 11, we have a discussion about Fig 3 at Method 300, starting at operation 302.

It then discusses the interlay stack layers; the dielectric layers, and so on. But I believe your question is why aren't there two conductive structures shown. And my answer would be column 12, line six. This is not an exhaustive figure.

Q. Okay. So it admits the -- Figure 3 admits the step of forming the adjoining structure?

A. Or saying this another way, Figure 3 is not complete. There are other steps before, or after, or in between.

And in glancing at Figure 3, it is not immediately obvious to me where the two structures are, but that does not mean that they are not present in the entirety of the device.

Q. Do any of the figures in the '872 Patent

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depict a dummy source structure in contact with adjoining structure?

ATTORNEY BONNY: Objection. Form.

THE WITNESS: We have the problem in these figures that silicon substrate 202 is not completely described. And we have discussed this earlier in my testimony.

So in places where one might expect that to be shown, 102 or 202 is not completely described in the specification.

BY ATTORNEY LANG:

Q. And so, looking at Figure 2L, if 202 was doped, then element 244 could be connected to the memory cells via a common source region?

A. Hang on one second.

ATTORNEY BONNY: Objection to form.

THE WITNESS: Okay. So let me go back. You asked a question and I was trying to get a better answer to your previous question. Your question was, if I may repeat it -- why don't you repeat it?

ATTORNEY LANG: Sure.

BY ATTORNEY LANG:

Q. And so, if in Figure 2L, in region 202 was doped, then element 244 could connect to the memory

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cells?

ATTORNEY BONNY: Objection. Form.

THE WITNESS: If region 202 had a doping section underneath 244, it wouldn't necessarily connect.

BY ATTORNEY LANG:

Q. Column 16, line 34 -- starting at 34 -- says, "Source structures formed in the inner --" are you there yet?

A. I'm not there yet. I got column 16 and I'm just making my way to 34. So I'm at 34 now.

Q. Okay. It says:

"Source structures formed in the inner region may be connected with surround channel structures..."

A. I see that.

Q. "...via common source such as doped region and substrate 202."

A. I see that.

Q. Okay.

So if that doping was applied to 202 in Figure 2L, then structure 244 could connect to the memory cells?

A. And there are multiple speculations buried in that statement. The first speculation is,

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exactly how the doping in -- let me find 2L. Hang on. Let's look at it.

It's speculation as to where the doping is in Figure 2L. You could have doping surrounding 244 that's not present elsewhere. And for that matter, could have doping anywhere you wanted in there, that's not present elsewhere.

You could have a block of doping that has an intrinsic region in between. My point of a minute ago stands.

What's happening in the array does not necessarily determine what's happening in Figure 2L. You could have a doped region under 244, creating the current path into that doped region. And then that doped region may just stop and not go anywhere.

So, I don't think we can jump to the conclusion that there is any particular doping in 202, as shown in 2L in the staircase, based on what's happening in the array.

Q. And so, that would mean the bottom of 244 is effectively a dead end?

A. So let's talk about dead end for a moment. Because I don't want to embed language that we haven't discussed. What I'd like to do is give me a second to review dead end and how I've used it in my

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declaration.

ATTORNEY LANG: And maybe before you do that, we've gone about an hour again. I guess we should talk about whether we want to go a little bit more and take an early lunch, or take a break and then do lunch at about 12:30.

THE WITNESS: You got me right in the middle of dead end. So what I suggest is let's finish this particular module and reach a stopping point, and then do something around maybe 11:30; 11:45?

Does that work for you?

ATTORNEY LANG: For lunch? Yeah.

THE WITNESS: Okay.

So where we left here is, I want to make sure that we are communicating on what "electrical dead end" means. And to do this, I'm reviewing my declaration to see the use of the words, "electrical dead end."

And I want to reference you to page 52, where I do have dead end. This happens to be with regards to Tessariol, but it provides the use of "dead end" that we may agree on.

A dead end being a part of a current flow part -- sorry. A dead end is something that is

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not part of a current flow path of a circuit, even if conductive.

Is that the definition that you are using?

ATTORNEY LANG: Correct.

THE WITNESS: Okay. Cool.

So now, you can go back and ask the question. Because now I think we have agreed on what we are using as the terminology.

BY ATTORNEY LANG:

Q. So in Figure 2L, the bottom of 244 is a dead end, unless 202 is sufficiently doped, such that it would connect to the memory strings.

A. So in Figure 2L, as drawn, where there is nothing illustrated on the top and nothing illustrated at the bottom, and as we have seen elsewhere, the doping is not shown.

Then if there were a little block of doping underneath 202 -- sorry -- underneath 244, within 202, that's not shown, that would have the two conductive parts would be a conductive contact.

And in the language we've agreed on, it would be a dead end, because that little block doesn't go anywhere. It is not part of the current flow path of the circuit, even though it does comprise a conductive contact.

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Q. And you said that there was a little block of doping underneath. What if there was no block of doping underneath 244?

A. Then we are back in the discussion we had earlier about contact materials on semiconductors.

Now, note that the use of the word "doping" immediately means that it is the semiconductors, or generally means that.

So if you have a metal that is interacting with the semiconductor, and we have not clearly defined the doping, so it's lightly doped, and we don't know what sign the doping is; we don't know what part the doping is, we don't know if the conditions for conductive contact are met.

Q. Okay.

THE WITNESS: Have you hit a stopping point? Do you want to do lunch now?

ATTORNEY LANG: Yeah. I'm glad to.

THE WITNESS: Okay. You kind of act like you are at your stopping point and want to think about the next thing. So I would suggest we do lunch.

ATTORNEY LANG: I am done with this.

(Luncheon break.)

BY ATTORNEY LANG:

Q. Dr. Kuhn, continuing with the '872 Patent, which is Exhibit 1001, I'd like to focus your attention on column five, lines 31 through 34.

A. Okay. I am on -- oh. I'm not. My apologies.

Okay. I am at column five, lines 30 to 35.

Q. Okay. And the '872 Patent states:

"Various embodiments in accordance with the present disclosure, provide an improved 3D memory structure scheme, suitable for solving the aforementioned issues by replacing the gate line slits with dummy source structures."

Do you see that?

A. I see that.

Q. Okay.

And what does that '872 Patent mean by replacing the gate line slits with dummy source structures?

A. So, if one looks to figures -- and I may switch to my declaration because they are colored. Let me actually do that. Hold on a second.

So I am going to go to my declaration, and I am also going to go to page 58. And page 58 is Figure 5 of the '872 Patent. And it's important,

because it has the gate line slits in bright blue so you can clearly see them.

And then going back up in my patent -- sorry -- in my declaration, to -- hang on a second here. I should have gone to -- it would have been better if I had gone to page 18, because page 18 has the same picture, a little easier to see.

And then Figure 1A, 1B, and 1C, on page 21 and 22, show how the structure in Figure 5 has been transmuted into this structure shown in 1A, 1B, and 1C, where it has the dummy source structures as individual elements, as opposed to slits.

Q. Okay.

So the '872 Patent is saying that the -- it removes the gate line slits from the device and instead uses dummy source structures?

A. I don't think the word "remove" is used. Let me just check that language. To be precise, it's replacing the gate line slits with dummy source structures.

Q. And how would a POSITA understand the '872 Patent to be using "replace?"

A. I think in the '872 Patent, the key understanding comes by looking at Figure 5 versus Figures 1A, 1B, and 1C, as the figures are very

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similar in the array portion.

And from that, one can see the differences that are proposed in the staircase portion.

Q. And how does replacing -- strike that.

But by replacing the gate line slits with the dummy source structure, the '872 Patent is referring to using the dummy source structures for the gate line replacement process instead of the gate line slits?

ATTORNEY BONNY: Objection. Form.

THE WITNESS: So as one of the embodiments, the '872 Patent does describe using the dummy source structures for the gate replacement process.

ATTORNEY LANG: Okay.

BY ATTORNEY LANG:

Q. Is there any embodiment in which a dummy source structure is not used for the gate line replacement process?

A. In '872, there are several locations where the gate line -- sorry -- where the gate replacement process is not disclosed in an embodiment or disclosed only as an option.

And let me share two examples. In column one of the '872 Patent, the patent opens with four

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examples. And it says:

"Embodiments of 3D memory devices and methods for forming the same are disclosed herein."

And there is one example; and another example; and a further example. And then on the next page, and yet another example.

Of these four examples, two of them are not gate replacement processes. The first two are -- do not describe a sacrificial layer, and thus can be concluded to not be a replacement gate.

Q. And where are you referencing on the '872 Patent?

A. I'm referencing column one. And -- actually, I'm referencing column one and column two. Starting at line 30 in column one, there is the "Summary" section. And it starts out with:

"Embodiments of 3D memory devices and methods for forming the same are disclosed herein."

And then there's four examples given. One starting at column 134. One at column 144. One at column 155. And then in column two, there is column two, line seven.

And so, the patent discloses here, four broad examples of the use of the patent. Two of which are gate replacement, and two of which are

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not.

Q. Okay.

And how does the -- if the -- and you are saying that in these embodiments, the dummy source structures not used for the gate line replacement process?

A. I'm saying that these two embodiments here -- sorry. That was not helpful.

I'm saying the embodiments in column one, starting at 34; column one, starting at 44, those two embodiments do not cite to the gate replacement process.

I also do point out, and as I describe in my declaration, the gate replacement process is not an essential part of the claimed invention. And that can be illustrated both as I did in these four examples at the beginning of the patent, and other examples that we can go through, that I cite in my declaration.

Q. Okay.

How does the dummy source structure solve the problems associated with the gate line slit if it's not used for gate line replacement process?

A. The whole point of the patent is not just solving the problems of the gate line slit that are

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indicated in that one paragraph. The patent has a number of additional advantages and benefits.

We were just focused on gate line slit for the purpose of the prior question.

Q. Okay.

Can you find an example in the '872 Patent where the dummy source hole is used for something else other than the gate line replacement process?

A. I may be misunderstanding your question. There's several uses for the dummy source hole. One of which is as an interconnect.

Q. And that interconnect is formed in the hole. But I'm looking for an example where a dummy source hole is described, and it's described with no description of it being used for the gate line replacement -- the gate -- strike that.

In the detailed description, is there any description of fabricating a device that does not use the dummy source hole for the gate line replacement process?

A. So, let me -- first, I haven't gone through the patent in detail to find that, but I am going to address your previous question which was, the only benefit of the dummy source structures is the gate line slit replacement.

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And I can demonstrate that's not correct in column five, line 45, where an additional benefit -- at least one additional benefit of improving the uniformity and stability for etching is described.

It's sort of a pattern density type of advantage, which has nothing to do with the replacement gate process.

Q. And where are you pointing to?

A. Hang on. I managed to just lose it. Give me a second.

Column five, line 45, discusses the arrangement of the dummy source structures for an etch type of advantage. The subsequent paragraph -- sorry. I misspoke there.

And so, now let me address your other question, which is, is there any place that the gate line -- the '872 is teaching, other than the gate line source process.

And let me point to my declaration at paragraph 79, where I describe a multiplicity of methods for fabricating the dummy source structures, including a variety of different CBD methods, and so on, which does not limit it to just a replacement gate process.

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Q. So going back to your discussion on column five, line 43 -- I think you are referring to 43 to 49. So it's your opinion that the gate line slits are replaced with dummy source structures, even outside of the context of the gate line replacement process?

A. So the patent describes a particular layout of the dummy source structures, which is shown in Figures 1A through C, and also discussed in the specifications.

The patent has multiple examples that do not reference the replacement gate process. In my declaration at paragraph 78, I have a number of citations that illustrate that the gate replacement process is an example.

As I mentioned before, there are techniques described in the patent for fabrication, and there is language described in the patent, of which that column five quote was one, that are not limited to the gate replacement process.

Q. What paragraph in your declaration are you referring to?

A. Paragraphs 78 -- paragraph 78 has a list of citations about the gate replacement process being an example. And paragraph 79 describes that

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there are several different fabrication techniques discussed.

Q. Paragraph 78, it states -- you say the statement is merely an example of how the claimed dummy source structures can be formed.

Is your point, is that when a POSITA reads exemplary language in the context of the '872 Patent, that's not limiting?

ATTORNEY BONNY: Objection. Form.

THE WITNESS: That feels a little bit like a legal conclusion. Let me rephrase it to what I think I'm trying to say.

The '872 Patent provides -- expressly provides four examples at the beginning. Two of which are not replacement gate. Language that I've cited both in this discussion and in my report, illustrate that the gate replacement process is an example, but not the sole example.

There is language in here of benefits that have nothing to do with the gate replacement process. So I think a POSITA reading this would interpret it as written. It is an example, but it's not the only possibility.

BY ATTORNEY LANG:

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Q. Well, you have quotes around "can" and you apparently found that word important. So why did you emphasize, quote/unquote, "can?"

A. I believe that I picked those words because some of these quotations in here used did not limit. For example, a gate replacement process is often used. In some embodiments, the dummy source structure may function. In some embodiments, it may still reach.

The language throughout the patent, including the two examples that don't describe replacement gate, it does not suggest that it's limiting.

Q. Okay. If we can go to the '872 Patent again? The '872 Patent; 564.

A. The '872 Patent; 564. Hang on. Okay. I'm there.

Q. It says, "Further, the dummy --" strike that.

"Further, both the dummy channel holes, and the dummy source holes, and the staircase region can be formed by the same process that forms the channel holes and the inner region."

What does that mean?

A. This paragraph or that statement is part

of a larger paragraph that has some, I would say, extension comments about things you can do with the dummy source.

The paragraph begins with, "The dummy source holes can have the same diameter as the dummy channel holes, and can be formed by the same process."

I read that as describing a series of kind of short embodiments. That the dummy source holes can have certain properties related to the dummy channel. The dummy source holes and the dummy channel holes can be formed by the same process. And there is a whole string of these.

You know, if I had to be very specific and I was doing kind of an embodiment by embodiment analysis, I would say each one of those sentences kind of opens up a class of embodiments.

Q. Well, what does it mean, the same process? Does that mean the same type of etch? The same type of etch chemistry? What does that mean?

A. So, a POSITA seeing a phrase, "in the same process" or "formed by the same process," would typically interpret that as it's the same steps in the process flow, and it's the same masks. You haven't gone off someplace else and done something

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else separately.

So, for example, I'll give a "what if" that's very simple. I could drill a channel hole, and then I could stop and put a bunch of stuff on the wafer; and take a bunch of stuff off the wafer; and put a bunch of stuff on the wafer. And I could drill a different hole. Those would be two separate processes.

Alternatively, I could drill the two holes at the same time, and that would generally be interpreted as being formed by the same process.

Q. Now, do the dummy source holes need to be circular? Strike that.

Do the dummy source structures need to be circular or cylindrical?

A. I don't recall anywhere in the patent that the exact geometry is described.

Q. All right. Maybe I can find it for you.

A. That would be good. If there is a place you know about, that would simplify things. I don't recall, though, the cylinder -- circular being specified.

Q. Well, I'll find -- okay, before we go to break.

A. Going back to the claims, yeah. If we

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want to talk about this, we need to find it. And I'm not seeing it.

Q. Yeah.

A. Okay.

Q. Now, if you could read column three, line one? The first paragraph on column three?

A. Okay. Hold on. The first paragraph on column three is:

"It is noted that references in the specification to one embodiment, an embodiment, an example embodiment, some embodiments, et cetera, indicate that the embodiment described may include a particular feature, structure, or characteristic, but every embodiment may not necessarily include the particular feature, structure, or characteristic."

Q. Right. And when you were talking about the patent and your understanding of whether the gate line essential -- gate line replacement process was essential, you had referenced some of the disclosures being -- you know, using permissive language.

Does this further support that when there is a reference to an embodiment that the '872 Patent isn't talking about, that that necessarily is present in all embodiments?

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ATTORNEY BONNY: Objection. Form.

THE WITNESS: That was a long question. I think my short answer to it is to cite that column three, lines five and six.

"Every embodiment may not necessarily include the particular feature, structure, or characteristic."

BY ATTORNEY LANG:

Q. And the --

A. So --

Q. -- expressed directive of the '872 Patent when there is a reference to some embodiment. The '872 Patent says not every embodiment necessarily has that. Correct?

A. Sorry. It glitched or I lost focus. Repeat the question.

Q. Yeah. So the '872 Patent is expressly saying in column three, that if an embodiment has a feature, that doesn't mean that other embodiments necessarily include that feature?

A. That is what I believe is written in column three, line five. That's correct.

Q. Let's go to your declaration. At paragraph 16.

A. Sixteen?

Q. Yeah.
A. Okay. I'm at paragraph 16.
Q. Yeah. And I wanted to focus on some of your work. You had talked about solar cells and flash.
A. Okay.
Q. So let's start with solar cells. Was that a design that you worked on, that had multiple solar cells?
A. No. This was a patent about a particular device configuration.
Q. But the technology. Is this a technology with like an array of solar cells?
A. It's been a while since I've done this one, but my memory is the entirety of the patent was focused on a single cell, and that the claims and specifications of the patent were all wrapped up in this cell, and it didn't go into discussion of what you did with more than one.
Q. And were you ever involved in the design or research of a device that included an array of solar cells?
A. No. As a device person, when I get into areas that are more in my photonics background -- because my earlier work in my career was in

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photonics, so every once in a while, I get one of these "devicey photonicky" projects. It tends to be on the device aspects. Not on the array aspects.

Q. And were you ever involved in a research or design of a device that included an array of flash cells?

A. Yes.

Q. Okay. And how many flashes cells were on one of those devices?

A. Oh lord. These were large memory arrays. I would have to go back and review my notes for, you know, how many hundred thousand or million they were. And it's typical flash. There's a lot of them.

And you would have to go remember which generation is, and how many were in the array.

Q. And were those flash cells laid out in a pattern?

A. The flash cells were -- I have to say this carefully. Because the flash cells had a global pattern, but they also had local patterns as well. It was not like an entire field of corn or something, all planted in exactly a perfect array.

There were breaks in the array. There were places where the array had other structures in

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it, for a variety of reasons. So there was a regularity to it, but it wasn't like a perfect crystal.

Q. And was the -- I'll try to get out of the same terminology. Was the local pattern, for example, a block or a sub-array?

A. Typically, yes.

Q. Okay. And in that sub-array of flash cell, were those flash cells equally spaced apart?

A. It depended. Some of this work -- there is always this tension in these technologies on what the bit line does. And for particularly older technologies, there would be what might be called "irregular layouts," to try to make the bit lines less difficult to fabricate.

There is a period of time in sort of early to middle flash, where every generation had some different compromise on the patterning problems for the bit lines versus the patterning problems for the cells themselves.

Q. And how is a repeating pattern created on a mask?

A. How is a repeating pattern created on a mask? Or how are repeated patterns created on a wafer?

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Q. On a mask.

A. The usual way -- and one can go down a whole lot of -- there's other ways to do this, but for example, as we see in databases, there will be a physically drawn cell, or group of cells, or block of cells, that is drawn with great precision and has a name.

And then that group is replicated through the remainder of the design.

Q. And a typical way to replicate it is shifting it?

A. Shifting it or shifting it with an offset.

Q. All right. If we can go to paragraph 41?

A. Sorry. I'm at 41.

Q. Okay. You said:

"One fabrication change arises when certain device openings called gate line slits are used to deposit conductive material into trenches."

That's referring to the gate line replacement process. Correct?

A. Well, that has a citation and -- has two citations, actually. So let me review those and remind myself. Because you can certainly get problems in putting material into trenches that has nothing to do with gate line slit.

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So the 444 to 49 is with respect to the gate line slit process. And 517 is also with respect to the gate line process. That being said, I do note that the first sentence at 444.

"Often, a gate line slit has large dimensions filled with an installation structure formed in the trench that extends laterally in the array."

One can frequently have fabrication issues simply to -- related to the fact something is a large trench, without the necessity of the gate line slit.

So my sort of summary answer to the question is, the citations cited below are mostly about gate line slit in relation to replacement gates, but not exclusively.

Q. Okay. And then you describe, continuing in paragraph 41, this issue of unbalanced variations.

Do you see that?

A. I see that.

Q. Okay.

And that's because of the distance that the materials have to flow through the gate line slit to fill the voids for the alternately

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conductive gate. Right?

A. So let's be a little careful here. Because unbalanced variations of wafer flatness can arise from long thin structures, such as those shown, whether or not they were used in the replacement gate process.

You know, I've talked about pattern density before, and I've talked about issues with, you know, both regular and irregular patterns.

Ignoring gate line slit for a moment, if I make a great big long trench down the wafer, and I put something in it that's stressful, like a metal, I'm going to have wafer flatness and wafer warpage issues, independent of whether it's a gate line slit used for replacement gate or not.

Q. In paragraph 43, you summarize in the '872 Patent, in the second sentence -- you say:

"The dummy source structures are arranged in a pattern, meaning a arrangement that is repeated at a regular interval."

Do you see that?

A. I see that.

Q. Okay.

And do you mean that there is a repeating pattern, meaning that the dummy source structures

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are, you know, equal distance away from each other? Or do you mean the set of dummy source structures collectively or repeated, as a pattern?

A. So that's actually almost a direct citation from the patent. It starts at the bottom of column seven.

"For example, dummy source structures 126 may be arranged in a pattern, e.g., arrangement with a same shape repeated at a regular interval in the planned view. And in some embodiments, dummy source structures are arranged in an array."

Q. And in a 3D memory device, are vertical structures, such as a memory string, easier to repeat in a pattern if they are the same distance apart?

A. That's actually an interesting question.

ATTORNEY BONNY: Objection. Form.

THE WITNESS: You know, I haven't thought about that one. From the standpoint of, "Gee, is it easier to draw," that is one aspect of the question.

You know, if everything is a perfectly regular array, it's a lot easier to draw. Whether it's easier to process is more complicated.

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Remember I talked a little bit about my other projects with flash memory and the tension between the bit line and the array location?

Because especially in the earlier days of memory, people would do really interesting things with the shape of the bit line in order to make the fabrication of the array cells easier.

So it's putting tension in one place to take tension off another place. And I haven't thought through the tradeoffs on that.

The bit line architecture in a lot of these NAND flash arrays is just remarkable. It's just this itty bitty tiny little via that connects in the bit line, and I'm not sure how that tension plays out.

BY ATTORNEY LANG:

Q. Do you know whether in 2018, commercial 3D NAND had the memory channels equally spaced apart?

A. I have not looked into that.

Q. So paragraph 49 -- I have it highlighted here. I'm trying to direct you to about, I guess the second full sentence.

A. I better look at your highlighting,

because there are so many in there, let me see if I can figure it out. You know, I have to move some stuff around.

Okay. In making this an argument. Sorry. I may sneeze here in a second. Okay. I see the sentence of interest.

Q. Okay. And this is your summary of the file history of the '872 Patent. Right?

A. This entire section is. That's correct. Starting at paragraph 47 and trekking its way down to 51.

Q. And you say that:

"The applicant cited a section of the specification that additionally states that the claim dummy source structures can function to laterally separate the 3D memory device into memory regions."

A. That's not what you have highlighted. I'm confused.

Q. I'm looking at paragraph 49.

A. Okay. Why don't you read it again? As you were speaking, it didn't seem to be what was there. But maybe I was just missing something.

Q. Yeah. "In making this an argument --"

A. Okay. I have that.

Q. "-- the applicant cited to a section of the specification and additionally states that the claimed 'dummy source structure,' can function to laterally separate the 3D device into multiple memory regions."

A. I see that.

Q. So what would the shape of a dummy source structure be in this case?

A. I haven't thought about this. The use of the dummy source structure to laterally separate the 3D memory device in multiple memory regions is not something I have spent any time thinking through.

Q. I mean, in view of this, do you think that a dummy source structure has to be cylindrical?

A. Again, I have not thought through this specific question of laterally separating the 3D memory devices using the dummy source structure.

Q. The gate line slit laterally separates the memory into memory regions. Correct?

A. It depends on how it's fabricated.

Q. Well, how could a dummy source structure laterally separate the 3D device -- let me strike that.

What does "laterally separate" mean?

ATTORNEY BONNY: Objection. Form.

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THE WITNESS: I have not closely reviewed the language here, closely enough, to be able to offer an opinion on "laterally separate."

BY ATTORNEY LANG:

Q. The '872 Patent, on column four, line 44, says:

"Often, a GLS has large dimensions and is filled with an insulation structure formed in a trench that extends laterally in the array."

Do you see that?

A. I haven't caught up with you. Remind me of the column and paragraph again.

Q. Column --

A. Oh. I found it. Forty-four. So it says:

"Often, a GLS has large dimensions and is filled with an insulation structure formed in a trench that extends laterally in the array."

I see that.

Q. And so, is "laterally," in the '872 Patent referring to the X direction?

A. So, I have not opined on this. However, we do have a picture of the gate line slit, and we can suggest that the direction in that picture, which is Figure 5, is in agreement with the statement in the '872 Patent.

So, in Figure 5, which is the prior art, the gate line slit trench extends in the X direction. So without a lot of thought, just simply applying the information there to Figure 5, I think we can say that at least with regards to Figure 5, that gate line slit is extending in the X direction.

Q. And then when you talked about the dummy source structure laterally separating, then the dummy source structure would extend in the X direction as well.

Is that right?

A. I think when --

ATTORNEY BONNY: Objection. Form.

THE WITNESS: Yeah.

I don't think you could conclude that. We are taking -- "lateral" is a word that can even mix up in the same patent. I've seen patents where they switched the X and Y axes within the patent.

"Lateral" is one of these words that needs to really be looked at in context. If I wanted to offer an opinion on this section that you have highlighted, I would need to go back to the spec and need to go back to what the applicant said, and go sort that out.

BY ATTORNEY LANG:

Q. So what's confusing about "lateral?" It extends in either at least the X or the Y direction. Right?

A. The confusion here is not the -- well, there is some confusion with regards to whether lateral is in the X and Y directions. But setting that aside for the moment, the statement that we are discussing is the statement about the claimed dummy source structure here -- your share just went away, and I was reading the highlighted region.

Q. I'm pulling something else up.

A. Okay.

Q. Go ahead. Keep going.

A. So I'll switch back to mine, but you are going to have to remind me what page and paragraph it was.

Q. It was paragraph 49.

A. Okay. See, that's what happens when I actually read from the screen. I get nailed.

Q. Yeah. I'm just going to try to pull something --

A. Okay.

Q. -- else up.

A. Nothing wrong with that. Except I made

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the mistake of reading off the screen.

Okay. So the point I'm trying to make here is there is a statement in paragraph 49 that is describing, the claimed dummy source structure can function to laterally separate the three dimensional memory device in multiple memory regions. And I have not thought through exactly that language.

Now, the subsequent language about the dummy source structure including a spacer, is a different sort of a concept.

So again, I'm not in a position to offer an opinion on shapes, or structures, or orientations of a dummy source structure to perform lateral separation in multiple memory regions. I just haven't thought through that.

And you said you were pulling something else up?

ATTORNEY LANG: Yeah.

BY ATTORNEY LANG:

Q. I will share my screen. I'm looking back at the '872 Patent, column 11.

A. Yes. And I'll bet you're looking at 11, line 47 -- sorry, 44 to 47 -- where they discuss:

"An embodiment laid in the patent, about dummy source structures 178 can laterally separate

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3D memory device into multiple memory regions, such as memory blocks, and --"

Hold on one second here. My previous answer pretty much stands. This is not something I have opined on at this point in the process.

Q. Okay. Going back to your declaration, I'll skip to paragraph 58. And I see that you have, at the beginning of paragraph 58:

"The term, 'dummy source structure' should be construed according to its plain and ordinary meaning."

Do you see that?

A. I see that.

Q. Okay.

Have you ever heard of a dummy source structure before working on this case?

A. I've certainly heard the word, "dummy" applied to numerous semiconductor features. It is not uncommon for the word, "dummy" to sit in front of a semiconductor feature that resembles some important feature, but is missing something. Dummy transistors. Dummy interconnects. Dummy memory regions.

So the use of the word, "dummy" to describe an object that resembles another object but

is missing some key functionality, is recently common.

Q. Okay.

If I understood your testimony, what was common was the use of "dummy" to qualify a different structure as something that mimics that other structure?

A. I would say --

ATTORNEY BONNY: Objection to form.

THE WITNESS: -- resembles, but is missing key functionality.

So if I say "a dummy transistor," to give one example, the object under discussion resembles a transistor but is missing some key functionality.

It's hooked up, or it doesn't have implants, or something.

BY ATTORNEY LANG:

Q. But the whole term, "dummy source structure." It won't surprise me, you agree, you have never heard the full term, "dummy source structure," before working on the case?

ATTORNEY BONNY: Objection. Form.

THE WITNESS: And I am not certain -- I'm trying to think about epitaxial dummy sources,

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which I have heard of. I think it is fair to say that I've not heard the word "dummy source structure" applied to 3D NAND in the way '872 does, prior to this case.

But I'm thinking of some instances where the use of the word, "dummy source," or "dummy source drain," has shown up with regards to dummy source drains and epitaxial sources and drains.

BY ATTORNEY LANG:

Q. And in that context, you are referring to the source of a transistor?

A. Yes.

Q. And paragraph 61 here, I highlighted two sentences. The first sentence, you say:

"The '872 Patent discloses that the dummy source structures function as a mechanical supporting structure."

And so --

A. That's -- sorry.

Q. And so, in all cases, do the dummy source structures function as a mechanical supporting structure?

A. I don't think --

ATTORNEY BONNY: Objection to form.

THE WITNESS: -- the patent anywhere requires all. I think the patent discloses that they may function as a mechanical supporting structure, but not that they necessarily always, and all of them do.

ATTORNEY LANG: Okay.

BY ATTORNEY LANG:

Q. And that's why I am asking you about this question. I read your opinion here as that they always do. But I guess you are saying that you would correct this by putting "may" in front of "function?"

A. So let's talk a little bit about "always" and "never" in relation to semiconductor devices. Let me say, for the moment, that I have some sort of a support structure, and it won't be a dummy source for this. It's some support structure for packaging. Right?

And I have a zillion of these things across the wafer, because it turns out I want to be very safe. And I've done some simulation. And I need 20,000, and I did 40,000, just to be safe.

It's not necessarily true that every single one of those is serving as a support structure. And, in particular, if I went and

measured one, the fact that it might not have any stress on it, does not mean the all the ones around it aren't doing something.

Q. Okay.

And your point is by using the permissive "may," that it may, in fact, or may not act as a support function?

A. I'm trying to avoid a situation of necessarily acting as a support function. Because in the real word of semiconductors, in particular, with regards to measurements of things, there are always circumstances where some of the structures are different than the others.

So if I had some structural support -- and again, I'm not talking about dummy sources here. I'm just saying I have put in something for the sole and only purpose of being a structural support in manufacturing.

I still may go in and find some of the more structural support, just because the requirement that every single one of something do something is inappropriate for this structure.

And we can have discussions about bit cells and yield, but for a structure that is not a sale feature of the wafer, or of the die, "always"

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is a little bit extreme.

Q. Okay. Well, the next sentence, you say, and while the dummy source structure may function as interconnects, you know, the patent doesn't prescribe them as functioning as a source to memory cells.

Could the dummy source structure be a mechanical supporting structure and an interconnect?

A. I see no language in the patent that says it can't be both a mechanical support structure and an interconnect.

Q. Well, if it's an interconnect, what would also make it a support structure?

A. If we visualize the staircase region of -- actually, let me do an idealized one for the moment because it's more straightforward.

If I have an idealized pad in a semiconductor device, that's going to be used for packaging. So there is a ridiculous amount of stress on it at one point in the process.

That pad may end up having the bump on the top. And then it has this support pad underneath, so that when I wham the thing into the packaging tool, I don't squash the wafer.

I may have a whole bunch of structures

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underneath that pad. Some of them may be electrically conductive. Some of them may not. But some of them are going to be mechanical. Some of them are going to be electrical. Some of them are going to be both.

And I may not be able to tell in advance which is which, because there's little subtle variations that determine that.

Q. You referred to a pad. Is that a contact pad?

A. A bump pad, perhaps. If I -- and again, I'm trying to use an example that's very simple and straightforward.

The most commonplace we have structural issues in the broader semiconductor world is when we are doing packaging. Because we are taking these little delicate things, and then we are slamming them into a package and doing bad things to them.

And it is not uncommon to have physical and electrical supports for that operation, where a structure is built up that is both an electrical structure to conduct current into the package, and a mechanical structure, so that when you put the thing in the package, you don't squash it.

Q. Now, I've got some questions about your

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paragraph 64, if you can just read it and refresh your memory.

A. Okay. So I will read it into the record.

"I disagree with the petitioner's suggestion that there is no dispute that this dummy source structure may not be a dummy."

And I'll read this and then we can talk more about it.

"The '872 Patent does not teach dummy source structures functioning as actual source structures. Just that the dummy source structures can function as interconnects."

Q. Okay.

So I guess one thing that the dummy source structures have the ability to function as is an interconnect. And you had talked about that they could be a support member as well. So those are two examples of what a dummy source structure can do.

Is that right?

A. Yes. It could perform a mechanical support. It could function as an interconnect. I have talked about those.

Q. And when the patent is saying that it can do something, that doesn't mean it must always do it?

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ATTORNEY BONNY: Objection. Form.

THE WITNESS: So I think we need to be careful about large numbers of objects in real life versus patent limitations.

My example of a minute ago is that I was objecting to "always" and "never" language in the description of large numbers of mechanical support structures.

All those structures were intended to be mechanical support structures, but in real life, some of them may actually just be sitting there.

BY ATTORNEY LANG:

Q. Is the claim --

A. And so -- sorry.

Q. Is the claimed dummy source structure in the '872 Patents always an interconnect?

A. It's clear that these dummy source structures can function as interconnects. There is no limitation that they must function as interconnects.

Q. And interconnect, one example the patent gives, is that it would connect something to a peripheral device. So the interconnect would connect those two kind of objects?

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A. That's connect -- that's correct. And give me a second here. Because I managed to shut down my version of the patent.

But the patent has, in multiple locations, that the dummy source structure may function as an interconnect, but never states that it must function as an interconnect.

Q. Okay. Took me a while to understand this, but just go ahead and read 66 to get yourself familiar with it.

A. Okay. So 66 is:

"Dummy source structures do not function as a source to memory cells."

And I'm going to add a little parenthetical comment. That's why it is a dummy source. If it functions as a source, it's no longer a dummy.

Continuing:

"I understand the petitioner relies on the following passage to argue otherwise, but the passage never says that the dummy source structure is the same thing as a source structure."

And I apologize for the kind of clunky writing. I probably should have said, "and this passage is --" in quotes -- "and this passage is, in

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some embodiments, dummy source structure 246 may not connect to channel regions in the inner region."

And then back discussing that again, even if the use of the permissive "may" language in the '872 suggests embodiments of the dummy source structures may or may not connect to channel structures, neither disclosure suggests that dummy source structures function as a source to the memory cells.

This is a long winded and not as clear as I might write it today discussion. The core point being is, a dummy source is not a source.

Q. Yeah. And this is why I was asking you so many questions about Figure 2L. And I'll go back to Figure 2L of the '872 Patent.

And so, I think what you are saying is that, Dr. Kuhn, if you look at Figure 2L, you can't tell from Figure 2L whether the bottom of 244 is actually electrically coupled to the memory cells, because that area on 202 may be a dead end. It may not develop. And, therefore, is not functions as a source.

Do I have that understanding correct?

A. Yes. The understanding that we should have, as we speculate around Figure 2L, is that

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this -- if it's describing a dummy source object, it cannot be a real source. Because a dummy source is not a source. So it is isolated from the source in some electrical way.

It however can still function as an interconnect to a peripheral, and it can function -- and we talked about this earlier.

Since the drawing is not as complete as one might like, one can speculate that it could connect to the peripheral via the top.

And I believe I actually have that language in my deposition -- sorry, in my declaration -- as this exposed conductive contact enables the dummy source structure -- exposed conductive contact would be the one at the top.

But since the drawing is not complete, there is also the possibility of it connecting underneath, in an undisclosed way, or to the sides in an undisclosed way.

Q. Right.

A. The only point one can say about Figure 2L is there is nothing on the top, which certainly opens up that possibility. But other things are possible as well.

Q. I'm confused. Because I'm looking at

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Figure 2L and it sure looks like 244 is buried into the substrate.

Am I misunderstanding Figure 2L?

A. Yes. We had this discussion before with regards to what is, and what is not, in 202. Recall our discussion about substrate doping; and about the definition of conductive contact; and about whether or not the conductive contact is contacting the source? And also about our discussion of dead end?

One could have Figure 2L as a conductive contact, by our definition, but non-uniform doping would mean that it's not necessarily connected to the source. So it meets the definition.

I append a little bit to that. As we discussed earlier, some of these images do not have enough information to make the conclusion, based on the information provided in the patent.

In particular, this one, you know, it is common to have doped and undoped regions underneath structures. The language of it's a dummy source, says it's not connected to the source. Our definition of "conductive contact" permits doping underneath.

And then, of course, it can function as an interconnect. This particular one is ambiguous as

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to whether it's wired that way.

Q. But just to make sure I understand your testimony, there is not a -- do you agree 244 is depicted as being buried into the substrate?

A. Two fifty-four shows the point of the contact in 202. That's correct.

Q. Okay. And 244 is making contact with the substrate?

ATTORNEY BONNY: Objection to form.

THE WITNESS: This is back to the point we discussed earlier with regards to the conductivity of that little part of 202 to the rest of the source.

ATTORNEY LANG: Oh. Okay.

BY ATTORNEY LANG:

Q. So you are saying that it could be a conductive contact, depending on the doping in 202?

A. Depending on the regional doping, or the localized doping in 202. The fact that something might be a conductive contact, I mean, as an example, I could have a strip of dopant running right underneath the black, and one array cell over, drop something down to a peripheral device underneath the array.

And, you know, there is my peripheral

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contact. There is my interconnect. And I'm not connecting to the source. I could remove that peripheral thing and I'm still a conductive contact. I'm just not contacted to the source.

I reference you to my declaration, paragraph 194. For example, "Localized doping regions are used in semiconductor substrates."

My point being is, nobody required that 202 be doped everywhere identically the same. And if there is use of features out in the staircase, the structure labeled 244 could be a conductive contact per our definition, and yet still not be connected to the source.

Q. And so, if it was not connected to a peripheral device -- well, let me strike that. Back up.

So your testimony is, because it's a dummy source structure, it's not connected to the memory cells. Correct?

A. Well, more precisely, if it's not -- if it's a dummy source structure, it is not functioning as a source.

Q. So it's not -- okay.

And then your testimony is that it could somehow have a dope region down here, and then be

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connected to a peripheral device off somewhere else?

A. I'm going to do my testimony in smaller pieces. The first piece is, if it's a dummy source, it does not connect to the source.

The second piece is, if it's a dummy source and it is a conductive contact, at the bottom, it needs to meet the conditioning of the two conductors, able to flow current. And that can be achieved easily with a localized doping region.

There may be --

Q. Okay.

A. And third, a localized doping region may exist for reasons more than making this a conductive contact. It may exist also to connect some of these into peripheral devices.

Q. Okay.

And why would you have a localized dopant region down here if you weren't connecting it to your peripheral device?

A. An example of that might be you have a string of these things in a row, and you didn't want to make a complicated mask. You just doped them all and you are only putting current through some of them.

Keep in mind that creation of localized

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doped regions and semiconductor products is really easy. And so, the use of a localized doped region can be kind of moved around at will.

Q. Paragraph 89 --

A. Hang on --

ATTORNEY LANG: At this point, I think I'm going to be able to watch my son's baseball game tonight. It's been about an hour, if you want to take a 10-minute break?

THE WITNESS: You know, that would be nice. Let's do 10 and refresh our tea.

ATTORNEY LANG: Yes.

THE WITNESS: Okay.

ATTORNEY LANG: And just if anybody has any logistical planning things, I can't imagine that we are not done by 3:00 o'clock.

THE WITNESS: Okay.

(Off the record.)

BY ATTORNEY LANG:

Q. Dr. Kuhn, staying on your declaration, I'd like to turn to paragraph 89?

A. Okay. I have 89.

Q. And you state:

"Further, it is irrelevant that the specification contemplates less than four dummy

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source structures that surround the word line contact."

Do you see that?

A. I do see that.

Q. Okay.

Now, do you agree that three dummy source structures could surround a word line contact?

A. I've not opined on three. What I want to do here for a second, is I want to pull up that section. Because the language in that section is a little odd. So give me a moment.

And this is at 88211. And the language is -- and it actually references dummy channel structures, by the way. It's:

"The number of dummy source structures surrounding a number of dummy channel structures may be more or less that eight, six, or four."

And so, the use of the word, "surrounding" followed by the "more or less than eight, six, or four," has this construction that less than four constitutes surrounding.

And we know from all of the extensive discussion about "between," that I document in my report -- and I think we have talked at some level -- that two does not constitute surrounding.

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So this could imply that three constitutes surrounding. It could also be an oddball use of the language, because if you look at that one phrase, that's a little ambiguous.

So the place I am resting is, I haven't opined on three.

Q. Can you envision a scenario when three dummy source structures surround a word line contact?

A. I can certainly speculate wildly, since the patent doesn't speak to that, or illustrate it, or even ambiguously -- unambiguously allow it. It would be speculation.

Q. How would you speculate three dummy source structures could surround a word line contact?

A. So let me make the caveat, I'm uncomfortable doing this, because I'm uncomfortable that this more or less phrase at 811 even permits three.

But for the sake of the argument, if they were three, it would likely follow the same type of symmetric. Not only the same length structure, as what has been illustrated in Figures 1A through C.

Q. Okay. What object -- strike that. I'll use a real world example.

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Do you have a fence around your property?

A. I do.

Q. And a single fence can surround a home. Correct?

A. I would agree that a single connected fence can surround a home. It's a "surround" more in the sense of a spacer lining the inside of a channel type of surround.

Q. Right. So when you are looking at whether something surrounds, you have to look at the extent of the object as well?

ATTORNEY BONNY: Objection to form.

THE WITNESS: Yeah. I wonder if this only applies to acreage. I notice nowhere in the patent has there been any discussion of extent.

BY ATTORNEY LANG:

Q. Well, okay. Let me go to your declaration at 90. You had drawn this picture at the bottom of the paragraph, or you reproduced the petitioner's image on the bottom of paragraph 90.

Do you see that?

A. Yes. That's your annotation. That's, you know, not our annotation.

Q. Okay.

And you agree that these four dummy source

structures surround the word line contact?

A. Following the '872 definition. That's correct.

Q. All right.

ATTORNEY LANG: Let me give you an exhibit.

(Exhibit 6 marked for identification)

THE WITNESS: Okay. Hang on a second. Because last time I pulled an exhibit up, I managed to turn everything off. Let's see if I can avoid that. Is it in the chat box?

ATTORNEY LANG: Yes.

THE WITNESS: All right. Let's see what happens. Okay. I have a PowerPoint slide open.

ATTORNEY LANG: I'll mark as Exhibit 6, an annotated version of the figure that Dr. Kuhn reproduced in -- or I should say a modified version of the image that Dr. Kuhn reproduced in her declaration, at the bottom of page 90 -- or paragraph 90.

BY ATTORNEY LANG:

Q. So, Dr. Kuhn, I guess you had said earlier, you don't have an opinion on whether a dummy source structure has to be cylindrical.

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Is that correct?

A. So, I did not offer that opinion, to my knowledge. We briefly discussed whether the patent disclosed it. And you mentioned it did, and we were going to discuss that, and then we got sidetracked.

So it kind of was a half-done testimony, because I might modify my answer if you illuminated a place where cylindrical was clearly disclosed in the patent.

Q. Oh. We can go back. We did briefly touch on this. If you look at the '872? And we looked at column 11, line 44, that said:

"As a result, dummy source structures can laterally separate the 3D memory device."

And my question is, given that it says that the dummy source structures can laterally separate, wouldn't you understand that the dummy source structure can be a lateral structure and extend laterally?

ATTORNEY BONNY: Objection. Form.

THE WITNESS: Yeah. We did have this discussion. And I disagreed with your position. We had a discussion about laterally separating.

Where we left this one is I did not agree

with your position on this, and I needed to study this whole section more to understand what was suggested by "laterally separating" into multiple memory regions.

BY ATTORNEY LANG:

Q. It also --

A. It doesn't affect any of my conclusions, though.

Q. It also says "such as memory blocks." Do you see that?

A. I see that.

Q. Aren't memory blocks usually, you know, rectangles?

A. Yes. But what does that have to do with -- there is no picture shown. There is no significant discussion. There is a sentence that's really ambiguous.

Q. Okay. And so, we go back to Exhibit 6 and the reproduced picture.

If the dummy source structures, two of them, as shown kind of on the top left, were merged together into one structure, and the two kind of on the bottom right were merged together in another structure, such that you only had two dummy source structures, do those two dummy source structures

shown in Exhibit 6 not surround the word line contact?

ATTORNEY BONNY: Objection. Form.

THE WITNESS: If we follow the language of the patent, this would be described as being a between situation.

BY ATTORNEY LANG:

Q. Well, no. The patent says that the word line contact is between -- here, it would be saying it's between the dummy source structures. But --

A. So -- sorry. Keep going.

Q. -- my question is, do the two dummy source structures shown in Exhibit 6 surround the word line contact?

ATTORNEY BONNY: Objection. Form.

THE WITNESS: So if I rotate this -- your orange structures, for the sake of the debate -- if I rotate them 45-degrees, I have a somewhat miniaturized version of the same gate line slit architecture -- it's just shorter -- that we have discussed earlier.

And that architecture, multiple times in the patent, is described as a between configuration. Not a surround configuration.

BY ATTORNEY LANG:

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Q. We can go to that part of the specification if you like. What it says is that the word line contact is between the other two objects.

I'm not talking about if the word line contact is between those two objects. I'm talking about whether the two objects surround the word line contact.

ATTORNEY BONNY: Objection. Form. Asked and answered.

THE WITNESS: The use of the word, "surround" in the '872 Patent, with the one exception of the oddball terminology that is in that one location that may open up the possibility of three, the use of the word, "surround," is never two. It's generally four or more.

And again, this looks like just a version of the gate line slit rotated, which is described as between. Not surround.

BY ATTORNEY LANG:

Q. What is described as between?

A. The gate line slit architecture has the staircase contact described as being between the gate line slits.

Q. Correct. I'm not asking you if the word

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line contact is between the dummy source structures.

A. Okay.

Q. I'm asking you if the dummy source structures surround the word line contact.

ATTORNEY BONNY: Objection. Form.

THE WITNESS: And I'm saying, in the patent, as I see it, my opinion is that the word, "surround" has been reserved for more than two objects. And there are two objects here.

BY ATTORNEY LANG:

Q. And then, you just said that a single object like a fence can surround a whole house. So why doesn't the two objects shown in Exhibit 6 surround the word line contact?

A. Well, first, we are not showing an image of a fence around a house. We have switched from a broad use of the word "surrounding" with respect to acreage, to the more specific language that's used in the patent.

And the patent illustrates layouts that are not dissimilar to this -- this is a miniaturized version -- that the word, "surround" is not used.

Q. Do you agree that the two dummy source structures shown in Figure 6 -- Exhibit 6 enclose

more of the border of the word line contact than in the version with four dummy source structures?

ATTORNEY BONNY: Objection. Form.

THE WITNESS: So, if we -- let me start out by saying that there is no place in the '872 Patent where area, subtended angle, mathematical relationships, is ever discussed.

So yes, your drawing has those lines longer than the individual diameters of the source regions. But that's never used in the patent anywhere, to clarify language around "surround" versus "between."

BY ATTORNEY LANG:

Q. Well, I guess what I am confused about is the '872 Patent does not seem to associate "surround" with a specific number, because as we read, "surround" could include with less than four. Right?

A. So --

ATTORNEY BONNY: Objection. Form.

THE WITNESS: I disagree rather strongly. The '872 Patent repeatedly distinguishes "surround" as being a number that is greater than two.

If they had not been interested in the

differentiation between two and more than, they would have never used "surround." They would just use "between" everywhere. Or, alternatively, they would use "surround" everywhere.

But the patent is repeatedly using "between" every time it has something that is a two-structure configuration, and repeatedly uses the word, "surround" when it's a more than two-structure configuration.

BY ATTORNEY LANG:

Q. Do you agree that one dummy source structure could surround a word line contact if it was structured like a fence? A continuous fence around the word line contact?

ATTORNEY BONNY: Objection. Form.

THE WITNESS: So I have not opined on that. Because I didn't have to opine on that. Because there is no example of that in any of the prior art.

I'm reluctant to opine on it in this context, because it might take a certain amount of analysis to go through everything and understand if that fit the definition of "surround" as given in the patent.

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But that being said, I don't need to opine on that because I don't need that.

ATTORNEY LANG: I'm just going to make a new exhibit.

(Exhibit 7 marked for identification)

ATTORNEY LANG: I'll put this in the chat in a second. Let me just do that now. I'll mark as Exhibit 7, another PowerPoint presentation, PP slide 2.

BY ATTORNEY LANG:

Q. And, Dr. Kuhn, do you have an opinion if the dummy source structure was expanded such that they were all merged together in a circle, fully encircling the word line contact, as one structure?

Would that surround the word line contact?

ATTORNEY BONNY: Objection. Form. Asked and answered.

THE WITNESS: So, I've already discussed this. I did not form an opinion on this. I didn't need to form an opinion on this because it does not appear anywhere in the prior art or anywhere in the patent itself.

It's also pretty speculative. Because had the patent wanted to disclose this configuration, for all we know, they could have

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called that a mote and used a totally different word.

So if I start naming a configuration that's never discussed and never described in the patent, I'm going way outside of the scope of what the patent has disclosed.

BY ATTORNEY LANG:

Q. Okay. So your opinion is that "surround," as used in the '872 Patent, may exclude fully encircling?

A. No.

ATTORNEY BONNY: Objection to form.

THE WITNESS: No. Because surrounding is used in multiple contexts in the patent.

Surrounding is used to describe, for example, the spacer, which is a different structure in a different instance, and is what you would call a fully surrounded architecture.

This is specific to the question of the dummy source structure and the dummy source structured layout, and what the name is for each of these various types of layouts.

And the patent is clear that if the dummy source structure is centered, or roughly centered between two of them, it's a between

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thing. And if it's roughly centered between, in general, four or more, it's a surround thing. And the patent does not disclose a name for this configuration.

And you are speculating that's surrounding and I could just as easily speculate that that would be called a mote. We are putting limitations in place for nomenclature in places not in the patent.

BY ATTORNEY LANG:

Q. Well, I just want to focus on the claim limitation that says the dummy source structures surround the word line contact. Okay?

A. Okay.

Q. And do you have any opinion of if there is a single dummy source structure, as shown on slide two of Exhibit 7, that fully encircles the word line contact, whether that satisfies that limitation?

A. I have not offered that opinion.

Q. Okay.

Let's go back to your declaration. I'm kind of confused by your paragraph 93. If you need to read it to get refreshed, feel free. I'm just going to focus on those highlighted portions.

A. Yes. And this one is complex because I am

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citing your petition back at you. And I didn't understand either, the way that this affected the '872 Patent.

It may be helpful to pull the '492 Patent up. Because I saw no indication that two NAND cells surround these things.

Q. Well, the '492 Patent says:

"Strongly affected by stored VTs of two surrounding NAND cells."

Is that a mistake in the '492 Patent?

ATTORNEY BONNY: Objection. Form.

THE WITNESS: What do the stored VTs of the two surrounding NAND cells in patent '492 have to do with the '872 Patent? It's a different patent. It's a different set of issues. It's different language.

BY ATTORNEY LANG:

Q. What I'm trying to figure out is you quote the '492 Patent, and it says "two surrounding NAND cells." And then you end the quote -- now, this is your testimony -- this passage is merely referring to the effect of NAND cells in the surrounding.

When you say "the effects of the NAND cells," are you referring to more than two cells?

A. Well, when I read '492, and I probably

need to go review it again, because it's been a while since I've looked at this -- I understood the patent to be discussing the VTs and how they were impacted by the set of cells that surrounded the NAND cells.

And the two surrounding was referring to the two adjacent ones, but not only the two adjacent ones. Which is where I get this passage referring to the effective NAND cells in the surroundings.

Q. Well, even though the '492 Patent says "two surrounding cells," you interpret that to mean more than two cells?

A. Well, there are certainly not only two NAND cells involved in these operations. And I don't think the '492 Patent isolates out two cells and says these are the only cells.

Q. It says "two surrounding NAND cells." Did I read that right?

A. So, I think we can debate at some length, the '492 Patent. But let me step up a level. This doesn't have any relationship to the dummy sources; and staircase contacts; and all of that that is described in the '872 Patent.

It appears to simply be a patent that happens to contain the phrase, "two surrounding NAND

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cells," but it's not deeply relevant to what we are discussing in '872.

Q. Okay.

So you didn't consider the plain and ordinary meaning of "surrounding" when you were interpreting "surrounding the '872 Patent?"

ATTORNEY BONNY: Objection.

THE WITNESS: Yeah.

We've had this discussion before. The plain and ordinary meaning of "surrounding" in the '872 Patent needs to be viewed in light of a POSITA's understanding of the specification in claims of a patent.

And '872 is very consistent about what it means by "surrounding;" what "surrounding" looks like. What the term looks like. And it is very consistent about the use of "between" versus "surrounding."

It is not in conflict with the larger plain and ordinary meaning. But it is very specific to the configurations that are illustrated and described, relevant to staircase; architecture; the staircase contacts; and the dummy source contacts that I see in the staircase.

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And we are taking this other patent and trying to force fit it into this usage. And I think that's inappropriate.

ATTORNEY LANG: Okay. Let me just make sure I understand your testimony.

BY ATTORNEY LANG:

Q. The '492 Patent refers to two surrounding NAND cells. You agree with that. Right?

A. The '492 Patent has the statement in it that is cited in my declaration, that says "two surrounding NAND cells dispersed in the adjacent left and right blocks."

Q. And then, you characterized a quote by --

A. I believe that's blocks. It's -- sorry.

Q. You characterized a quote by saying:

"This passage is merely referring to the effects of NAND cells in the surroundings."

When you say "effects of NAND cells," are you referring to more than two cells?

A. So when I initially read this, I read this as this language describing the two surrounding NAND cell, but also, incorporating other cells in the surroundings.

Q. Okay. --

A. Now, I may have misread that, but that was

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my read of it the first time I read that patent.

Q. Okay.

In paragraph 95, you set forth a construction of "conductive contact." And I'll read it. You say:

"It should be construed as a conductive structure that connects current flow with an adjoining conductive structure."

That's how you believe the term should be construed. Correct?

A. That's correct.

Q. Okay.

Now, so the construction -- your construction or interpretation means that there has to be an adjoining conductive structure, or you can't have a conductive contact?

A. Yes. There has to be an adjoining conductive structure. So, for example, if you dropped the conductive -- sorry. If you dropped a conductive structure on a sheet of oxide, you would not be able to do this.

Saying this another way, my construction for "conductive contact" requires the conductive structure itself. It requires the current flow was permitted. And it requires an adjoining conductive

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structure.

As an example of one that does not work, if I took a conductive structure and placed it on top of a block of glass, that would not be a conductive contact.

Q. Okay.

So this goes back to what we talked about in the morning. So if you had a contact pad -- it's actually not a contact pad in a test chip, because it's not connected to an adjoining structure. Right?

A. So we had a long discussion about contact pads this morning. And one of the problems that we are having is that "contact pad" is a very broad term. And it's going to depend on the exact layout of whatever kind of contact pad you have.

We talked at one end of a contact pad that was simply a round circle of metal, that didn't do anything. And that would not be a conductive contact.

We talked at the other end, as a contact pad as having some architecture that connected it to, perhaps, a transistor, but did not have current flow at the time of fabrication. And that would be a conductive contact.

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Q. I guess, you had mentioned that "contact" is a broad term. So when you interpreted it, it's important that you have to interpret it specifically in the context of the '872 Patent.

Is that right?

A. I'm going to repeat back an answer, but I'm not sure I'm answering your question. I made the point earlier in our discussion that "contact" is an unusually broad word. It can be used as a noun. It can be used as a verb. It can be used as an adjective.

And one has to be unusually sensitive to context. And in this particular case, the context of the '872 Patent.

Q. Now, you had said that the -- in paragraph 100, you make this point that it requires a structure that permits current flow with the adjoining conductive structure, gives proper meaning, because the contact structure is what permits conductive material to conduct current with the adjoining structure.

So if we look at this vertical conductive member in the '872 Patent, are you talking about like the top of it? The bottom of it? Any particular portion of it that must permit this

current flow?

A. So I'm going to step a little bit back to basic physics to make this point. And this also ties to some things I did in my earlier declaration.

In the actual achievement of a conductive electrical structure, we need a contact itself in the noun sense. We need a connection between the contact itself in the noun sense, and another material. And we need the other material to be conductive. And all these three things have to happen.

And in real life, it turns out the middle one, which is the place where the first conductive object interacts with the second conductive object, is really important.

You can have two conductive objects, and the one in between does not work, and you do not have a conductive contact, because there is no possibility of current flow.

The simplest example is I have a piece of insulator in between when I'm done. I do not have the possibility of conducting current.

Another example we have discussed is I may have any appropriate process conditions, or any appropriate product conditions, so that at the

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voltages of the product or the exact nature of the process, I can't conduct that current across that junction either. It acts like an insulator.

And then, there's all the other cases where I could potentially conduct current across that intersection. I may or may not be actually conducting current at the time, but I could.

Q. That was helpful.

So if you have a vertical pillar through the memory stack that is the dielectric, current is not going to flow through that vertical pillar. Right?

A. Right. If I have a vertical pillar and I make it out of boron nitride, or something, I don't meet the first part of this. I don't have a conductive structure. I don't even get to the other two parts.

Q. Okay.

And then, now, once I have a conductive structure, current can flow through that, but you need these other two pieces you are talking about -- the adjoining structures on each side -- so that you have a circuit or a current path?

A. A little --

ATTORNEY BONNY: Objection to form.

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THE WITNESS: Yeah. A little more subtle than that. I need the first structure. So, for example, a pillar of boron nitride does not work. So we have a pillar of tungsten.

Then I need something to conduct to. A block of boron nitride doesn't work. You know, if I put the boron nitride in the pillar, I'm done. If I put the boron nitride underneath the pillar, I'm done.

But let's say, just for the sake of debate, I have a tungsten pillar and a tungsten block underneath. I'm still not done. Because I need to make sure that when I touch A to B, it's conductive.

Now, this becomes particularly important when I have a piece of metal on one hand and a piece of semiconductor on the other hand. Because there are a number of conditions both, process and product, or that may not work.

And thus, we get some ambiguity about whether certain process and product conditions constitute a conductive contact.

BY ATTORNEY LANG:

Q. Well, maybe this will help with that. I'm looking at paragraph 102. And you have in here:

"For example, dummy source structure that can contact another structure, such as a peripheral device, and, therefore, permit current flow to another conductive structure."

Do you see that?

A. Yes.

Q. And now, on the top of the dummy source structure would have to be, presumably, some type of voltage source or, you know, a voltage signal that then would flow through the dummy source structure, down to the peripheral device. Correct?

A. I think --

ATTORNEY BONNY: Objection to form.

THE WITNESS: Okay.

Your example is a little too specific. All the patent says is that it has to contact a structure, such as a peripheral device, and permit current flow to that device. It doesn't say where it is or how you get there.

BY ATTORNEY LANG:

Q. I guess what --

A. So --

Q. I guess what --

A. You can go up. You can go down. Or you could go sideways. It just -- it has to flow

current to the device to make this condition.

So we have two types of these things. We have these things that have the possibility to flow current because they meet those three conditions in my construction.

And we have the ones that actually are conducting current, because there is something somewhere that a voltage somewhere runs through this thing and goes to a peripheral device somewhere else.

Q. Yeah. I guess what I -- and maybe I'm just not understanding your testimony.

You seem to be describing an open circuit to me. If you have a dummy source structure that on the bottom, for example, connects to a peripheral device, and the top connects to nothing, I don't understand how current is going to flow.

A. That's fair. And I was imprecise. If there is a peripheral circuit described, there is the implied assumption that there is a voltage somewhere to drive it.

Q. Okay.

And so, that's what I was getting at. And so, when you are talking about this example here of current flowing, you know, there is basically, you

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know, a connection to the top of the dummy source structure, e.g., you know, something driving it. And there is a connection to the bottom, e.g., the threshold device.

Is that right?

A. Not necessarily. The top and bottomness is not the important thing. You could have a voltage line underneath on the bottom, and the peripheral device is driven from the top.

You could have a voltage on the bottom and the peripheral device has a wire on the top, but the wire goes off to the peripheral device on the side. The exact top or bottomness of the wiring is not specified in any way in the patent.

I agree that the exact voltage is not specified, but that's implied. If you are going to a peripheral device, you are going to be wanting to use that device, and that says you are driving voltage to it.

But whether that voltage came in from the top or the bottom, the patent is not specific about that.

Q. Yeah. And I'm just trying to get to something. I'm not trying to focus on top or bottom. But it's this notion of a dead end.

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What I'm trying to get to is that you actually have a circuit where this vertical conductive pillar has two connections. One, for example, to a voltage source, and one, for example, to a peripheral device.

Is that fair?

A. I'm not sure I heard the question. It seemed like more of an expository comment.

Q. Let me try this again. This notion that you are describing, permitting current to flow, that would involve basically a connection on one side, e.g., a voltage source; and a connection on the other side, e.g., a peripheral device?

A. Not quite. Remember we have two cases of these things. One case of these things is easier to discuss in this kind of discussion, which is the case that it is driving a peripheral device.

And that case, we have a voltage source somewhere that connects into one side or the other of this thing. And we have a peripheral device some place, that connects into the other side of this thing.

And we are using it as a pathway to get current to that peripheral device. That's reasonably straightforward. It's acting like a

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conventional back end via the --

Q. Or you could say interconnect, because it's connecting those two things?

A. And the interconnect is better. That's the language the patent uses.

Q. Okay.

A. The other case is more subtle because it is describing a condition that is there but not activated.

The case where I have the metal pillar on the properly doped substrate, of all the right features and everything, but it's a dead end, that case is still a conductive contact.

And the way I think about it is, it's not intrinsically dead. I could bring pico probes in and run current through it. I just don't happen to have current through it at that moment.

And I contrast that to the same geometry, but with an insulator in between. But no matter what I do, I can't run current through it.

Q. Okay.

And in this other case that you are talking about, you said that the -- not the interconnect case, but the other case -- you had said that the metal pillar would land on a properly

doped substrate of all the right features and everything?

A. I was giving that example. Yes.

Q. Okay. And where is that doping described in the '872 Patent?

A. Recall that the conditions under which you create good contacts versus failed contacts are extremely well-known in the art. Every POSITA goes to school and takes the little class in semiconductor physics, and spends two weeks talking about metal semiconductor contacts.

So the patent does not need to go into gruesome detail about something that is textbook material in the community.

Q. Now, one reason you might properly dope that substrate is so that dummy source structure can connect to the memory strings. Correct?

A. And the moment you would dope it to connect to the memory strings, it is no longer a dummy source structure. It's a true source structure.

Q. And one other reason you described for properly doping the substrate was so that it could actually connect to a peripheral device.

Do you remember that?

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A. You just swapped topics really fast. Let me make sure that we are clear on the previous answer.

The reason that properly doping underneath a dummy source structure to connect it to the channel is not applicable to the case of dummy source, it's because it's not a dummy anymore. It's a real source. So that goes off to one side.

And then to your second point, I discussed a situation a while back, where you might elect to conduct current through a dummy source, into the substrate, underneath the dummy source, and go do something with that, as a polysilicon, or a silicon interconnect, or a resistor.

And you selectively dope underneath it, and then you are running it off to a peripheral circuit of some type. And that would be a dummy source, because it's not a source, but it's conducting current very cheerily, off to some other application.

Q. Like I think you mentioned a peripheral device. Right?

A. A peripheral device. A resistor. It's very common to make a resistor by doping something and running through it. You know, it's a peripheral

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device but it's not an active device. It's a resistor.

Q. Okay.

So I've been doing 3D NAND for almost 10 years, Dr. Kuhn. Can you name for me, in real life, an example of when a metal pillar is buried into the substrate -- into a dope substrate -- properly doped, as you said, for any other reason than connecting to a peripheral device, such that you still have an ohmic contact, as you say?

ATTORNEY BONNY: Objection. Form.

THE WITNESS: Yeah. Can you make that either a shorter sentence or multiple sentences? Because I don't even know what the question is on that one.

ATTORNEY LANG: I can try to make it multiple. It might be easier.

THE WITNESS: Okay. Let's do multiple.

BY ATTORNEY LANG:

Q. You are positing a scenario where you properly doped a substrate, such that you have an ohmic contact.

Are we on the same page so far?

A. So I am positing a scenario where someone has taken a pillar of metal. They have correctly

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doped the substrate underneath that pillar, and they are going to do something with it.

Q. Okay. And one thing is, it could connect to a peripheral device. Correct?

A. That's correct.

Q. Okay.

I want you to give me a real life example of using that properly dopant amount for application other than a peripheral device.

ATTORNEY BONNY: Objection. Form.

THE WITNESS: Okay. So what you want me to do is give you an example of the situation I just described, where it goes to something other than a peripheral device?

ATTORNEY LANG: Yes.

THE WITNESS: So before I go down that question, let's make sure we understand what a peripheral device is.

What kind of language are you using? Do you mean an active device? Do you mean a transistor? Do you -- what do you mean?

BY ATTORNEY LANG:

Q. The language of the '872 Patent.

A. Okay. So the language of the '827 Patent27 Patent actually defines that. And if

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you look at -- let me see if I got the right page -- column nine.

It defines:

"Peripheral devices, including any suitable digital, analogue, and/or mixed signal peripheral circuits, useful for facilitating operation of 3D memory devices, such as page buffers, decoders and latches..."

Et cetera, et cetera, et cetera.

So they are describing peripheral device as a whole set of things. And you simply want me to say a speculative example of one of that set of things?

Q. You had described that for a metal pillar contacting the substrate, or for it to be a contact, you would have to have it properly doped. Correct?

A. We have agreed on that. Yes. And have some other features. But for the sake of this discussion, "properly doped" is a fine way of just, you know, condensing that idea.

Q. And one reason you said you'd do that is so that it can connect to a peripheral device?

A. No. Actually, one reason I said that is so it would be a conductive contact.

Q. And now that you have a conductive

contact, one thing it can do is connect to a peripheral device. Right?

A. You have two choices for connecting to a peripheral device. You can go a connection to the bottom or you can go a connection through the top.

And in my experience, people run connections both ways. They can run connections to the substrate, where they are typically not as good, or they can run connection to the metal lines, where they are on top of things.

And so, I think you are asking me to speculate about some sort of an architecture where this device goes to a semiconductor material, which then goes off to some circuitry, either underneath or aside, that happens to be wired with a semiconductor, rather than a metal.

Q. But my question was different, so I must have framed it poorly. If you are going to use that proper dopant amount to create a contact --

A. Yes?

Q. -- give me an example of that, other than in the context of connecting to a peripheral device.

A. People do that all the time. That's the normal way you make a conductive contact in the semiconductor industry. Is you dope the

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semiconductor substrate immediately underneath where the contact lands.

Q. And could you give me --

A. That's --

Q. Could you give me an example of a vertical metal pillar in 3D NAND? A real life example of that?

A. I can give you a real life example from generic transistor physics, because there is, I believe one already referenced in my declaration.

Q. You can't give me a real example in 3D NAND. Right?

A. Because I haven't had a chance to go research it. That's a very specific question that I was not asked.

Q. [Indiscernible] would do it than just use it for examples of supporting pillar.

ATTORNEY BONNY: Objection. Form.

ATTORNEY LANG: Let's go to paragraph 102.

I've probably got about 15 minutes. Do you want to try to finish up? Or do you need another break, Dr. Kuhn?

THE WITNESS: Let's run this through to the end. And then we'll see if Chris has any questions. If he is thinking of some, then we

can take a short break while he collects himself.

ATTORNEY LANG: Okay.

THE WITNESS: You started a question around 102?

ATTORNEY LANG: Yeah. I decided to skip it.

THE WITNESS: Okay.

BY ATTORNEY LANG:

Q. Now, I see you have here, 108, you said:

"Construing 'conductive contact' as a conductive structure that permits current flow with an adjoining conductive structure also does not limit the location of the 'contact' on the dummy source structures (whether the contact is on top of the dummy source structure or elsewhere)."

Do you see that?

A. Yes.

Q. And so, just to be clear, your view of the claim contact is it's at the location of where that adjoining structure is.

Is that right?

A. That's a little subtle. Because my view of the claimed conductive contact is the structure that permits the flow with the adjoining structure.

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And thus, implicitly includes the actual interface between the two.

Q. Does it contact the whole thing? Or just the interface?

A. Well, the -- it's a conductive contact. So the conductive contact is, in some sense, the whole thing. The contact itself -- again, this goes back to the fact that "contact" has a number of context-based definitions.

I think the way we need to stick to it to avoid confusing ourselves is the conductive contact is the structure that permits the flow within the adjoining conductive structure, and implicitly requires this conductive piece that is the landing zone, or the whatever you want to call it. The area of contact.

Sorry I keep doing this, but there is only so many words in the English language, and "contact" seems to be used for all of these things -- the direct interface.

Q. If we were to look at Figure 2L, and let's say that the bottom was connected to a peripheral device, so the conductive contact would then be the bottom portion.

Is that right?

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ATTORNEY BONNY: Objection. Form.

THE WITNESS: No. The conductive contact is the whole thing. The bottom portion is what makes it is conductive contact.

ATTORNEY LANG: Okay.

BY ATTORNEY LANG:

Q. So it's actually the peripheral device that makes 244 the conductive contact?

A. No --

ATTORNEY BONNY: Objection.

THE WITNESS: It's the fact that the conductive structure permits the current flow.

The way I understand this is to flip it around. If I put an insulator inside 244, I've still got a metal. I've still got a conductive pillar. But that pillar just -- I'm not getting current out of the bottom of that pillar, so I don't -- I cannot permit current flow with an adjoining conductive structure.

The moment I remove that insulator, the conductive structure is the whole thing. But inherent in my construction is that the bottom of it has to permit current flow.

ATTORNEY LANG: Okay.

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BY ATTORNEY LANG:

Q. So, Dr. Kuhn, if I had a peripheral device connected to the bottom of 244 and 2L and it's a conductive contact; if I rip away that peripheral device, it's no longer a conductive contact. Right?

A. Wrong.

Q. Wrong? Okay.

A. The fact that the conductive contact permits current flow with an adjoining conductive structure, there's still an adjoining conductive structure there, even if you took the peripheral device away.

It's still a conductive contact. It's just not an interconnect.

Q. Okay.

Now, I notice you cite this definition of dummy structure in Tessariol on paragraph 117. And you highlight "which may comprise a circuit inoperable electrical dead end."

So are you interpreting "may" as actually to mean "will?"

A. Usually, when I run into "may," I interpret "may" as a possibility. Not a requirement.

Q. Okay. And so, in Tessariol, the dummy

structure may, or may not, have an inoperable dead end?

A. The use of the word "may," in general, I do not assume limits it to always be in that configuration.

ATTORNEY LANG: Marking the last exhibit and just a couple questions.

(Exhibit 8 marked for identification)

BY ATTORNEY LANG:

Q. And this will be Tessariol, if you happen to have it.

A. Okay. Hang on, let me load that up. Give me a second here to shut the other one down, or we'll have a repeat of the '827, 872 confusion. Okay. I have Tessariol up.

Oh heck. Sorry. I just managed to crash everything. Give me a second to reload. I don't know what I'm doing that's causing this.

Okay. I think I have everything back live again.

Q. Okay.

I just want to focus you on -- and I'll mark as Exhibit 8, the Tessariol patent, for U.S. application number 2019/0081061. I just want to ask you a couple questions about Figure 16.

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A. Okay. Give me a second, let me locate it. Okay. So I have Figure 16 up.

Q. Okay.

A. Where would you like me to go with Figure 16?

Q. Do you see this layer on the top, 86? I've kind of got my cursor over it, if it helps.

A. I do see layer 86 there on the top.

Q. Okay. And that's an insulating layer -- that's an insulating layer in which dielectric interconnects are going to be formed through. Correct?

A. That's an insulating layer. Correct.

Q. And do you see those element 69 in that layer?

A. Yes, I do.

Q. And --

A. There is --

Q. Oh. Go ahead.

A. Sorry. My headphones just fell off. Give me a second here. I see element 69.

Q. And the way those are going to be formed is that a layer such as 86 is going to be deposited, and then a mask with a pattern is going to be deposited over 86.

And then holes are going to be etched to form -- to ultimately form the 69 contacts; or interconnects; or what have you.

Does that sound right?

A. Yes. There is obviously multiple ways to do this, but at some point, you have to pattern it, whether you do it the way you described, in kind of a Damascene way. You put something down. You cut a hole in it. You fill it with metal.

Or whether you do it the other way around. You put the metal down, and you etch it. Either way, you have a pattern in step.

Q. Okay.

And we talked about this a little bit earlier today. One way to form that mask, you could simply replicate -- strike that. Let me ask a few foundational questions.

So you see that there is four element 69 on the right, and four element 69 on the left?

A. I see that.

Q. Okay. And those element 69 on the right, that looks like a pattern of four?

A. Sure. I will say there is a pattern of four on the right.

Q. Okay.

And we had talked about making masks earlier today. One way to do that would be you would take that pattern of four and you would just replicate that pattern on the mask. Right?

A. I will be more precise. I'll say you take that pattern of four and you replicate it in the drawn layout. So when the mask is fabricated, they are where they -- where you want them in the final design.

Q. Right. But instead, what they have done is this is actually an irregular pattern. Because there's four -- a pattern of four. And then an irregular space. And then the pattern of four is repeated. Right?

A. I agree.

Q. Okay.

ATTORNEY LANG: That's all I had, Chris. Unless you have something else.

ATTORNEY BONNY: Could I just take a 10-minute break to make sure I don't have any further questions? Or even five minutes I think would be fine.

THE WITNESS: Actually, I would like a 10-minute break. Because I need a little bio break.

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ATTORNEY BONNY: Okay.

THE WITNESS: And this would be a perfect time to let you look at your notes, and let me get my little break.

ATTORNEY BONNY: Okay. Let's go off the record then.

THE WITNESS: Okay.

COURT REPORTER: Okay. We are off the record.

(Short break.)

COURT REPORTER: We are back on the record.

ATTORNEY BONNY: Okay. I have no redirect.

ATTORNEY LANG: No further questions.

COURT REPORTER: Okay. Can I get the orders for the transcript, please.

ATTORNEY LANG: Yeah. I think I need like five days.

COURT REPORTER: Okay. Do you need the rough draft?

ATTORNEY LANG: Yeah. I won't look at it -- I won't need it tonight or tomorrow.

COURT REPORTER: Okay. I'll get it to you by tomorrow.

ATTORNEY LANG: That's fine. I'm not going to read it today or tomorrow. No rush.

COURT REPORTER: Mr. Bonny, can I get your order, please.

ATTORNEY BONNY: We'd like the rough, and for the transcript, if we can just go with the normal time.

COURT REPORTER: Okay. Thank you.

(Whereupon, the deposition adjourned at 2:34 p.m.)

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REPORTER'S CERTIFICATE

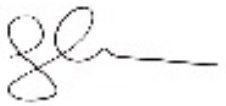
I, GISELLE MITCHELL-MARGERUM, the undersigned, a Registered Professional Reporter, Certified Reporting Instructor, Licensed Court Reporter, and Certified Court Reporter, do hereby certify:

That the witness, KELIN KUHN, before examination was remotely duly sworn to testify to the truth, the whole truth, and nothing but the truth.

That the foregoing deposition was taken remotely stenographically by me on Friday, March 28, 2025, and thereafter was transcribed by me, and that the deposition is a full, true, and complete transcript of the testimony, including questions and answers, and objections, motions and exceptions made by counsel.

That reading and signing was not requested; and that I am neither attorney nor counsel for, nor related to or employed by, any of the parties to the action in which this deposition was taken; and that I have no interest, financial or otherwise, in this case.

IN WITNESS WHEREOF, I have hereunto set my hand this 3rd day of April, 2025.



GISELLE MITCHELL-MARGERUM, RPR, CRI, CCR, LCR, ACCR, CSR

CALIFORNIA CSR 14424

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CERTIFICATE OF DEPONENT

I, KELIN KUHN, hereby certify that I have read the foregoing pages, numbered 1 through 181, of my deposition of testimony taken in these proceedings on Friday, March 28, 2025 and, with the exception of the changes listed on the next page and/or corrections, if any, find them to be a true and accurate transcription thereof.

Signed: .....

Name: KELIN KUHN

Date: .....

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ERRATA SHEET

Case Name: Micron v. YMTC
Witness Name: KELIN KUHN
Date:

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Subscribed and sworn to before

me this date day of month , 2025.

_____

KELIN KUHN

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