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Transcript of Sanjay Banerjee, Ph.D.

Date: May 29, 2025

Case: Micron Technology, Inc. -v- Yangtze Memory Technologies Company, LTD.
(PTAB)

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WORLDWIDE COURT REPORTING & LITIGATION TECHNOLOGY

YMTC Ex. 2014
Micron v. YMTC
IPR2024-00789 Page 1

1
2
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UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE PATENT TRIAL AND APPEAL BOARD

- - - - - x
MICRON TECHNOLOGY, INC. :
Petitioner, : Case IPR2024-00789
v. :
YANGTZE MEMORY TECHNOLOGIES : U.S. Patent No.
COMPANY, LTD., : 10,861,872
Patent Owner. :
- - - - - X

Videotaped Deposition of SANJAY BANERJEE, Ph.D.
Conducted Virtually
Thursday, May 29, 2025
10:01 a.m. EDT

Job No.: 585435
Pages 1 - 29
Reported by: Debra A. Whitehead

1 Videotaped Deposition of SANJAY BANERJEE, Ph.D.,
2 conducted virtually.
3
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5 Pursuant to notice, before Debra Ann Whitehead,
6 E-Notary Public in and for the Commonwealth of
7 Virginia.
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A P P E A R A N C E S

ON BEHALF OF PETITIONER:

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ALSO PRESENT:

KELLI WELCH, Video Specialist

C O N T E N T S

EXAMINATION OF SANJAY BANERJEE, Ph.D.	PAGE
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By Mr. Cross	6
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EXHIBITS MARKED IN TODAY'S SESSION

(None marked)

EXHIBITS MARKED IN PRIOR SESSIONS

(Not attached)

DEPOSITION EXHIBIT	PAGE
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Exhibit 1001	9
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Exhibit 1023	29
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Exhibit 1035	18
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1	P R O C E E D I N G S	10:00:40
2	VIDEO SPECIALIST: Here begins Media	10:00:40
3	Number 1 in the videotaped deposition of Sanjay	10:00:46
4	Banerjee, Ph.D.; in the matter of Micron	10:00:49
5	Technology, Inc., V Yangtze Memory Technologies	10:00:54
6	Company, LTD; in the United States Patent and	10:00:55
7	Trademark Office, before the Patent Trial and	10:00:57
8	Appeal Board; Case Number IPR2024-00789.	10:00:59
9	Today's date is May 29th, 2025. The time	10:01:04
10	on the video monitor is 10:01 a.m. eastern time.	10:01:06
11	The remote videographer today is Kelli Welch,	10:01:10
12	representing Planet Depos. All parties of this	10:01:12
13	video deposition are attending remotely.	10:01:14
14	Would counsel please voice-identify	10:01:18
15	themselves and state whom they represent.	10:01:20
16	MR. CROSS: Allen Cross with Ropes &	10:01:20
17	Gray, on behalf of Yangtze Memory Technologies.	10:01:23
18	MR. LANG: Jason Lang from Orrick, on	10:01:26
19	behalf of Petitioner Micron.	10:01:28
20	VIDEO SPECIALIST: The court reporter	10:01:32
21	today is Debbie Whitehead, representing Planet	10:01:32
22	Depos.	10:01:32

Transcript of Sanjay Banerjee, Ph.D.
Conducted on May 29, 2025

6

1	The witness will now be sworn.	10:01:46
2	SANJAY BANERJEE, Ph.D.,	10:01:46
3	having been duly sworn, testified as follows:	10:01:46
4	EXAMINATION BY COUNSEL FOR PATENT OWNER	10:01:47
5	BY MR. CROSS:	10:01:47
6	Q Good morning, Dr. Banerjee.	10:01:49
7	A Good morning.	10:01:51
8	Q Thank you for joining.	10:01:51
9	So I know you've gone through a few of	10:01:54
10	these. But if we can just go through a few	10:01:57
11	preliminaries briefly.	10:02:00
12	Can you state where you're currently	10:02:01
13	located?	10:02:05
14	A Austin, Texas.	10:02:05
15	Q Do you have any materials in front of	10:02:06
16	you, any --	10:02:11
17	A So I have unmarked copies of my recent	10:02:12
18	declaration, then my original declaration, a copy	10:02:14
19	of the '872 patent, a copy of the Tessariol	10:02:18
20	patent, and just the cover page of the Park	10:02:25
21	patent, all unmarked.	10:02:29
22	Q Sorry, cover page of?	10:02:31

1	A	The Park patent. I didn't print out the	10:02:33
2		whole thing.	10:02:35
3	Q	Oh, okay. And the two declarations	10:02:36
4		you're referring to, those are the two that you	10:02:41
5		filed regarding the '872 patent. Correct?	10:02:42
6	A	That's correct.	10:02:47
7	Q	Do you have any other electronic devices	10:02:47
8		with you?	10:02:51
9	A	I have my cell phone. But, yeah, I will	10:02:54
10		not access that.	10:03:03
11	Q	You understand you're under oath today?	10:03:04
12	A	Yes.	10:03:05
13	Q	And I'll be asking questions and you'll	10:03:05
14		be answering them. If you don't mind, if you can	10:03:07
15		wait for me to finish, I'll wait for you?	10:03:10
16	A	Yes.	10:03:13
17	Q	Is there any reason why you can't testify	10:03:13
18		truthfully and fully today?	10:03:16
19	A	No.	10:03:17
20	Q	And if I ask a question that you don't	10:03:18
21		understand, do you agree to ask for clarification?	10:03:22
22	A	Yes.	10:03:25

1	Q	Otherwise I'll assume you understand the	10:03:25
2		question.	10:03:28
3		Is that fair?	10:03:28
4	A	Yes.	10:03:30
5	Q	And how did you prepare for today's	10:03:30
6		deposition?	10:03:33
7	A	I reviewed the two declarations, the '872	10:03:36
8		patent, Park and Tessariol, as well as other	10:03:42
9		relevant documents, Dr. Kuhn's reports, my	10:03:50
10		deposition testimony, Micron's petitions, patent	10:03:53
11		owner's replies.	10:04:00
12	Q	Did you review anything outside of what	10:04:03
13		you cited in your declarations, other than the	10:04:08
14		patent owner response and the reply?	10:04:10
15	A	Not in preparation for this deposition.	10:04:16
16		Not that I recall. I've been studying quite hard	10:04:21
17		yesterday, so ...	10:04:29
18	Q	And did you start your review yesterday?	10:04:30
19	A	No. I've been reviewing for the past few	10:04:33
20		days, but the bulk of the review the day before	10:04:37
21		the deposition.	10:04:40
22	Q	And can you tell me what your occupation	10:04:40

1	is?	10:04:52
2	A I'm the Cockrell Chair Professor of	10:04:54
3	Electrical and Computer Engineering at the	10:04:57
4	University of Texas in Austin. And until January	10:04:59
5	this year I was also the director of the	10:05:04
6	Microelectronics Research Center; I was the	10:05:08
7	director from 1999 to 2025.	10:05:11
8	Q So can you tell me, in the context of	10:05:17
9	semiconductor fabrication, what a VIA is?	10:05:19
10	MR. LANG: Objection to form.	10:05:24
11	A I mean, I haven't opined on that	10:05:30
12	specifically in the context of this patent. But	10:05:32
13	in general, it's a vertical -- I believe VIA is an	10:05:34
14	acronym for vertical interconnect access. So we	10:05:42
15	have -- if you have multilayer interconnects, the	10:05:45
16	vertical conductive layer between an upper level	10:05:49
17	and interconnect, the lower level interconnect.	10:05:54
18	MR. CROSS: I'm going to upload to the	10:06:05
19	chat the '623 patent, which was previously marked	10:06:07
20	as Exhibit 1001.	10:06:12
21	(Exhibit 1001, previously marked, not	10:06:17
22	attached.)	10:06:18

1	Q If you already have a copy in front of	10:06:18
2	you, that's fine. But just let me know once you	10:06:20
3	have Exhibit 1001 open.	10:06:28
4	A You said '623 patent or '872 patent?	10:06:33
5	Q I meant the '872 patent. I've had a	10:06:36
6	couple of these depositions. So, yeah, so in front of	10:06:39
7	you should be Exhibit 1001, which is the U.S.	10:06:43
8	Patent Number 10,861,872.	10:06:48
9	Do you have that up in front of you?	10:06:52
10	A Yes.	10:06:54
11	Q All right.	10:06:54
12	MR. LANG: One second. I'm having	10:07:01
13	trouble downloading it.	10:07:03
14	MR. CROSS: You know what? Let me -- I	10:07:18
15	think I -- I'm trying to redo this.	10:07:19
16	MR. LANG: There we go, I've got it.	10:07:31
17	MR. CROSS: You've got it? Okay.	10:07:33
18	Q If we can turn to Figure 2, starting with	10:07:43
19	Figure 2J.	10:07:56
20	A Are you trying to share your screen, by	10:07:58
21	the way, because I can't see it.	10:08:00
22	Q No, I'm not.	10:08:01

1	A	Okay. Fine. I have a hard copy.	10:08:03
2	Q	I'm happy to share my screen if you want,	10:08:04
3		but ...	10:08:07
4	A	You said Figure 2J?	10:08:08
5	Q	Yeah. It's on Page 11.	10:08:10
6	A	Yes, I see that.	10:08:12
7	Q	Can you tell me what Element 212 is?	10:08:13
8	A	I believe that's a cavity, which is	10:08:26
9		useful from the -- what '872 calls the dummy	10:08:33
10		source structure.	10:08:38
11	Q	And can you tell me what Element 230 is?	10:08:39
12		If it's helpful, you can turn to Column	10:09:30
13		14, starting at Line 44.	10:09:32
14	A	It says 230 is an insulating layer, and	10:10:04
15		it gives some examples, silicon dioxide.	10:10:09
16	Q	And if you can turn to Figure 2L on Page	10:10:32
17		12.	10:10:45
18	A	Yes.	10:10:45
19	Q	Can you confirm that that insulating	10:10:45
20		layer is still present?	10:10:50
21	A	Comparing Figures 2J and 2L, it appears	10:11:38
22		to be still present. Let me see the description.	10:11:41

1	Yeah, there's nothing in the text in	10:12:47
2	Column 16 which explicitly describes the layer.	10:12:49
3	But comparing Figures 2J and 2L, I believe it's	10:12:53
4	still present.	10:12:56
5	Q And does the insulating layer cover the	10:12:57
6	dummy source structure --	10:13:06
7	MR. LANG: Objection to the form.	10:13:10
8	Q -- in Figure 2L?	10:13:11
9	MR. LANG: Objection to form. Scope.	10:13:13
10	A I don't believe I've opined on that in my	10:13:24
11	report. Could you point me to my report if I	10:13:27
12	have?	10:13:30
13	Q Are you unable to tell from the figure	10:13:30
14	alone whether or not the insulating layer is	10:13:33
15	covering the dummy source structure in Figure 2L?	10:13:35
16	MR. LANG: Same objections.	10:13:40
17	A Also keep in mind that these figures are	10:13:47
18	often in a high-level sketches which won't	10:13:52
19	necessarily show every aspect of the invention.	10:13:58
20	Having said that, if one looks at Figure	10:14:03
21	2L in isolation, the layer 230 doesn't appear to	10:14:06
22	cover this black region in the dummy source	10:14:12

1	structure.	10:14:19
2	Q What is Element 244?	10:14:21
3	A In Column 16, Line 23, it says, "Contact	10:14:42
4	244 can be formed" by depositing -- "by depositing	10:14:52
5	conductive materials including, not limited to,	10:14:56
6	tungsten and cobalt, copper, aluminum,	10:14:59
7	polysilicon, silicides, or any combination	10:15:02
8	thereof."	10:15:05
9	Q Can you turn to Column 14, Line 61?	10:15:10
10	A Okay.	10:15:29
11	Q And if you can read through Column 15,	10:15:30
12	Line 5, and let me know when you're done.	10:15:45
13	A Okay.	10:16:34
14	Q Does that passage describe removing a	10:16:34
15	portion of the insulating layer above the dummy	10:16:40
16	source hole 212 in Figure 2F?	10:16:44
17	MR. LANG: Objection to form. Scope.	10:16:48
18	A I don't think I've opined on those	10:16:55
19	aspects in my report. But having said that, at a	10:16:57
20	high level it appears to talk about using a mask	10:17:05
21	to pattern the photoresist, which is layer 232, to	10:17:16
22	create an opening above the dummy source	10:17:23

1 structure. And in Column 15 the patent says part
2 of the -- well, Column 14 and 15, part of the
3 insulation layer 230 right above the dummy source
4 called 212, and the ceiling layer 214 that fills
5 in and covers the dummy source hole 212,
6 parentheses, shown in Figure 2F, are removed using
7 wet etching and/or dry etching processes since
8 they're not covered by photoresist layer 232,
9 parentheses, shown in Figure 2F. Dummy source
10 holes 212 are thereby reopened for later
11 processes.

10:17:26

10:17:38

10:17:42

10:17:46

10:17:51

10:17:56

10:18:01

10:18:04

10:18:09

10:18:13

10:18:16

12 But I've not analyzed those aspects in my
13 report.

10:18:18

10:18:25

14 Q Looking at Figure 2K, can you tell me
15 what Element 242 is?

10:18:25

10:18:40

16 A In Column 16, Lines 1 onwards, it says
17 that 242 is a spacer which is formed along the
18 side wall of dummy source hole 212 and in recesses
19 240, and using various deposition techniques such
20 as atomic layer deposition, chemical vapor
21 deposition, physical vapor deposition, any other
22 suitable processes, or any combination thereof.

10:19:29

10:19:35

10:19:38

10:19:42

10:19:49

10:19:50

10:19:51

1 And there are some exemplary materials that are 10:19:55
2 described. Could be a single or composite layer 10:20:01
3 of dielectric materials, which is silicon oxide 10:20:04
4 and silicon nitride. 10:20:07

5 Q Are you familiar with these thin film 10:20:10
6 deposition processes? 10:20:14

7 A Yes. I used them extensively in my 10:20:16
8 research over the last 40 years. 10:20:19

9 Q And have you ever used such thin film 10:20:21
10 deposition processes to put a layer of dielectric 10:20:28
11 within a cavity such as the dummy source hole 212? 10:20:31

12 A I've used this deposition techniques 10:20:38
13 extensively in my research to deposit such 10:20:40
14 dielectrics in -- on various semiconductor 10:20:43
15 structures. 10:20:48

16 Q So looking at Figure 2K, would a thin 10:20:54
17 film deposition put the uniform layer of the 10:21:00
18 spacer along the entire X axis? 10:21:10

19 MR. LANG: Objection. Form. 10:21:17

20 A Well, this figures, as I told you before, 10:21:24
21 are, you know, high-level sketches. So one should 10:21:30
22 always interpret them with caution. 10:21:34

1	Having said that, the film thickness	10:21:38
2	appears to be uniform along the side walls. And	10:21:42
3	if that's true, based on my knowledge of the	10:21:48
4	technology, I'd suspect they use something like	10:21:51
5	ALD or CVD, which tend to give what I call	10:21:56
6	conformal depositions, which means that the film	10:22:04
7	conforms to the topography on the substrate.	10:22:06
8	And they probably wouldn't be using PVD,	10:22:09
9	or physical deposition techniques, such as	10:22:12
10	sputtering for example. Those tend to be	10:22:17
11	nonconformal. But all depends on context.	10:22:19
12	I've not analyzed any of these in my	10:22:21
13	report, so you will have to give me more specifics	10:22:23
14	and I can give you a more definitive answer.	10:22:26
15	Q Sorry. For PVD, you would expect a more	10:22:29
16	or less uniform deposition both on the top and on	10:22:43
17	the side walls?	10:22:46
18	Is that what you're saying?	10:22:47
19	A No. I said for ALD, you would expect	10:22:48
20	uniform deposition. PVD is not going to give you	10:22:54
21	uniform deposition.	10:22:56
22	Q My mistake. Sorry.	10:22:57

1	So for -- what does ALD stand for?	10:22:59
2	A Stands for atomic layer deposition. And	10:23:02
3	I've been using ALD for many years in my research.	10:23:04
4	Q And would that also put a layer of this	10:23:07
5	spacer down at the bottom of the cavity?	10:23:14
6	A It general in would. It tends to be	10:23:20
7	conformal.	10:23:23
8	Q So it would have to be removed if you	10:23:24
9	were trying to make a contact between the dummy	10:23:28
10	source structure and the substrate?	10:23:31
11	MR. LANG: Objection to form. Scope.	10:23:36
12	A I don't recall discussing any of that in	10:23:43
13	my report. I'd be happy to discuss those if you	10:23:46
14	can point me to that.	10:23:55
15	But having said that, in looking at	10:23:56
16	Figure 2K, keeping in mind these are highly	10:23:59
17	stylized versions of the structure, the patentee	10:24:03
18	appears to have etched off the spacer 242 at the	10:24:11
19	bottom of the trench.	10:24:17
20	Q I'm going to load into the chat a copy of	10:24:26
21	your reply declaration. If you can open that up,	10:24:44
22	that would be great.	10:24:58

1	(Exhibit 1035, previously marked, not	10:25:01
2	attached.)	10:25:04
3	Q It should be in the chat now. Let me	10:25:04
4	know when you have it open.	10:25:33
5	A I have the hard copy in front of me.	10:25:34
6	Q Can you turn to Page 27 of your	10:25:36
7	declaration, Paragraph 50?	10:25:46
8	A Okay.	10:25:54
9	Q Can you tell me what's illustrated in	10:25:55
10	Paragraph 50?	10:26:06
11	A It is a schematic cross-section of a 3D	10:26:20
12	NAND flash memory showing the staircases on two	10:26:24
13	sides and then the memory core in the middle.	10:26:30
14	Q And can you tell me what the green layers	10:26:37
15	are?	10:26:42
16	A I have a black-and-white copy. So give	10:26:48
17	me -- sorry. I wanted to save -- save ink.	10:26:50
18	Q Sure. Let me see if I can -- are you	10:26:55
19	able to open up the copy that I put into chat or I	10:27:00
20	can share my screen.	10:27:04
21	A Okay. Let me -- let me do it. Okay.	10:27:04
22	Yes, I've got it open now.	10:27:28

1	Q	So can you tell me what the green layers	10:27:32
2		are in this figure?	10:27:35
3	A	Yes. These would be the control gates,	10:27:40
4		which are also known as word lines.	10:27:43
5	Q	Are there any other green layers?	10:27:52
6	A	Yes. There is a layer at the top, BLS,	10:27:57
7		and one at the bottom. The one at the bottom is a	10:28:03
8		source line selector. And the one on the top I	10:28:06
9		believe is a bit line selector.	10:28:13
10	Q	Okay. Why are these all the same color?	10:28:15
11		MR. LANG: Objection. Form. Scope.	10:28:24
12	A	I've not discussed those aspects in my	10:28:34
13		report. But at a high level, I could tell you	10:28:36
14		that, you know, they're made out of the same	10:28:45
15		conductive material.	10:28:49
16	Q	So you don't know they're different	10:28:54
17		thicknesses, they're all conductive layers?	10:28:58
18		MR. LANG: Same objections.	10:29:03
19	A	Yeah, these are conductive layers. The	10:29:13
20		thicknesses will depend on the thicknesses of the	10:29:16
21		original sacrificial layers. And then you fill	10:29:21
22		out the cavities after you etch off the	10:29:24

1	sacrificial layers with the conductive material.	10:29:28
2	Q And are you familiar with this type of 3D	10:29:32
3	NAND structure BiCS?	10:29:40
4	A Yes.	10:29:45
5	Q And is BiCS a gate-first or a gate-last	10:29:45
6	device?	10:29:52
7	MR. LANG: Objection to form. Scope.	10:29:58
8	A I haven't analyzed or described those in	10:30:02
9	my report. I believe BiCS stands for bit-cost	10:30:04
10	scalable structures. I haven't reviewed it	10:30:14
11	recently, so I'm speaking from memory. And I	10:30:16
12	teach these in my classes. I believe those are	10:30:20
13	gate-first, but I could be wrong. I haven't	10:30:26
14	looked at the details in a while.	10:30:29
15	Q And you got this figure from a book.	10:30:39
16	Is that correct?	10:30:47
17	A Yes. Yes, a textbook.	10:30:48
18	MR. CROSS: I will now load up to chat a	10:30:53
19	textbook which has been marked as Exhibit 1023.	10:30:56
20	(Exhibit 1023, previously marked, not	10:31:00
21	attached.)	10:31:10
22	Q And if you can open that up on your	10:31:10

1	computer.	10:31:12
2	A Okay.	10:31:40
3	Q And is this a book that you took that	10:31:40
4	figure from?	10:31:49
5	A Yes.	10:31:51
6	Q And can you turn to Page 131?	10:31:51
7	MR. LANG: You mean the endorsed page or	10:32:03
8	the textbook page?	10:32:11
9	MR. CROSS: The Bates-stamped page. At	10:32:13
10	the bottom of the page it should read Page 131.	10:32:17
11	A Yes, I see that. Yes.	10:32:20
12	Q Can you read to yourself the last	10:32:21
13	paragraph on that page.	10:32:27
14	A Yes, I see that.	10:32:47
15	Q So does this confirm that BiCS is a	10:32:48
16	gate-first process?	10:32:56
17	A Yes.	10:32:56
18	Q Can you briefly explain to me what a	10:32:56
19	gate-first process is?	10:33:01
20	A Yes. So in a gate-first process, as the	10:33:03
21	term describes, you make -- I think these	10:33:08
22	terminologies are from MOSFET literature.	10:33:13

1 So in a gate-first process you make a 10:33:18
2 deposit and pattern and etch the gate electrodes 10:33:24
3 first. And then using that as a self-aligned 10:33:27
4 implant mask, one implants the source drains on 10:33:34
5 either side of the gate. 10:33:38

6 As opposed to a gate-last process, where 10:33:40
7 one uses a dummy gate, you pattern the dummy gate, 10:33:44
8 use that to do self-aligned source drain implants. 10:33:49
9 You etch off the dummy gate, then fill up the 10:33:53
10 cavity which is the channel region with the gate 10:33:57
11 dielectric, and then gate refill, making it a 10:34:00
12 gate-last. So one takes that terminology from 10:34:04
13 MOSFET technology. 10:34:08

14 With 3D NAND flash, so if one makes the 10:34:12
15 gate or the word lines first, it will be a 10:34:16
16 gate-first process, as in the BiCS technology. 10:34:19
17 Alternatively, if you make a stack of two 10:34:25
18 different dielectrics, one of which is going to be 10:34:29
19 a sacrificial dielectric, you make part of the 10:34:35
20 structure, etch off the sacrificial layers, and 10:34:41
21 then you refill that with conductive material, 10:34:43
22 which would be your word lines or gates. That 10:34:46

1 will be a gate-last process, as in the '872 10:34:49
2 patent. 10:34:53

3 Q So when you refer to the gate-last 10:34:53
4 process, this is -- is that similar to what this 10:34:59
5 textbook is referring to as the gate-replacement 10:35:06
6 in that paragraph? 10:35:09

7 A Yes, I believe so. 10:35:13

8 Q And so in BiCS you wouldn't have the 10:35:14
9 gate-replacement process. Correct? 10:35:21

10 A Yeah, in BiCS you deposit a stack of 10:35:25
11 these gate electrodes, very often highly doped 10:35:28
12 polycrystalline silicon, interspersed with 10:35:33
13 dielectric layers. And then you pattern and etch 10:35:35
14 the staircase structure. So you leave the gate 10:35:40
15 material in place. 10:35:46

16 Q All right. So just to confirm, in BiCS 10:35:52
17 you wouldn't use gate-replacement process. 10:35:58

18 Correct? 10:36:01

19 MR. LANG: Objection to form. Scope. 10:36:01

20 A I haven't opined on any of those aspects 10:36:08
21 in my report. But, you know, based on my general 10:36:10
22 knowledge in the field, BiCS is not -- BiCS is a 10:36:14

1	gate-first process.	10:36:23
2	Q And when you say it's a gate-first	10:36:28
3	process, you're confirming that BiCS doesn't use	10:36:42
4	gate replacement. Correct?	10:36:45
5	MR. LANG: Same objections.	10:36:47
6	A I haven't analyzed those aspects for the	10:36:53
7	purpose of this report. But from what I recall,	10:36:55
8	that's correct.	10:36:59
9	Q Dr. Banerjee, I think -- why don't we	10:37:01
10	take a five-minute break.	10:37:37
11	THE WITNESS: Okay.	10:37:38
12	VIDEO SPECIALIST: We are going off the	10:37:39
13	record at 10:37.	10:37:40
14	(A recess was taken.)	10:37:41
15	VIDEO SPECIALIST: We're back on the	10:43:31
16	record at 10:43.	10:43:36
17	BY MR. CROSS:	10:43:40
18	Q Dr. Banerjee, we were previously looking	10:43:42
19	at Figure 2K of the '872 patent. You mentioned	10:43:46
20	that you suspect that they use ALD or CVD, which	10:43:49
21	you called conformal depositions. Correct?	10:43:54
22	A ALD is very conformal. CVD, depending on	10:43:59

1	the parameters, can be conformal.	10:44:03
2	Q And you suspected that they don't use	10:44:07
3	something like PVD or physical deposition	10:44:12
4	techniques, or sputtering techniques. Correct?	10:44:16
5	MR. LANG: Objection to form. Scope.	10:44:21
6	A Yeah, physical deposition techniques such	10:44:25
7	as sputtering generally are not conformal, so you	10:44:27
8	will not get uniform thickness of the deposited	10:44:33
9	film on the side walls.	10:44:36
10	Q So what would -- would -- strike that.	10:44:39
11	Using PVD or other sputtering techniques,	10:44:55
12	would you still get a deposition at the bottom of	10:45:00
13	the cavity?	10:45:03
14	MR. LANG: Objection to form. Scope.	10:45:08
15	A What happens during PVD depends on the	10:45:13
16	deposition parameters. For example, the	10:45:17
17	deposition pressure in the chamber, which in turn	10:45:20
18	will determine what's called the mean free path of	10:45:25
19	the species that are being deposited. So that	10:45:28
20	then will determine the thickness of the	10:45:31
21	deposition of the side walls and the bottom. And	10:45:36
22	in general they will not be uniform.	10:45:39

1 But having said that, in general with PVD 10:45:40
2 you would get some -- I would expect some 10:45:45
3 deposition at the bottom. 10:45:47

4 MR. CROSS: I have no further questions. 10:45:51

5 Thank you. 10:45:52

6 MR. LANG: None from me. 10:45:55

7 MR. CROSS: Great. 10:45:57

8 VIDEO SPECIALIST: This marks the end of 10:45:58
9 the deposition of Dr. Sanjay Banerjee. We're 10:45:59
10 going off the record at 10:46 a.m. eastern time. 10:46:02

11 (Off the record at 10:46 a.m. EDT.)
12
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ACKNOWLEDGMENT OF DEPONENT

I, SANJAY BANERJEE, Ph.D., do hereby
acknowledge that I have read and examined the
foregoing testimony, and the same is a true,
correct and complete transcription of the
testimony given by me, and any corrections appear
on the attached Errata sheet signed by me.

(DATE)

(SIGNATURE)

C E R T I F I C A T E

I, Debra Ann Whitehead, E-Notary Public in and for
the Commonwealth of Virginia, do hereby certify:

That SANJAY BANERJEE, Ph.D., the witness
whose deposition is hereinbefore set forth, was duly
sworn by me before the commencement of such
deposition and that such deposition was taken
virtually and is a true record of the testimony
given by such witness.

I further certify that the adverse party,
MICRON TECHNOLOGY, INC., was represented by counsel
at the deposition.

I further certify that the deposition of
SANJAY BANERJEE, Ph.D., occurred virtually, on
Thursday, May 29th, 2025, from 10:01 a.m. to 10:46
a.m. EDT.

1 I further certify that I am not related to
2 any of the parties to this action by blood or
3 marriage, I am not employed by or an attorney to any
4 of the parties to this action, and that I am in no
5 way interested, financially or otherwise, in the
6 outcome of this matter.

7
8 IN WITNESS WHEREOF, I have hereunto set my
9 hand this 3rd day of June, 2025.

10
11 My commission expires:
12 October 31, 2027

13
14 A handwritten signature in cursive script, likely of the notary, is written over a dashed line.



15 -----
16 E-NOTARY PUBLIC IN AND FOR THE
17 COMMONWEALTH OF VIRGINIA
18
19
20
21
22

Transcript of Sanjay Banerjee, Ph.D.
Conducted on May 29, 2025

30

A			
able	aluminum	austin	23:10, 23:16,
18:19	13:6	6:14, 9:4	23:22, 24:3
about	always	avenue	bit
13:20	15:22	3:12	19:9
above	analyzed	axis	bit-cost
13:15, 13:22,	14:12, 16:12,	15:18	20:9
14:3	20:8, 24:6		black
access	ann	B	12:22
7:10, 9:14	2:5, 28:2	back	black-and-white
acknowledge	answer	24:15	18:16
27:3	16:14	banerjee	blood
acknowledgment	answering	1:13, 2:1, 4:2,	29:2
27:1	7:14	5:4, 6:2, 6:6,	bls
acronym	any	24:9, 24:18,	19:6
9:14	6:15, 6:16,	26:9, 27:2,	board
action	7:7, 7:17, 13:7,	28:5, 28:17	1:2, 5:8
29:2, 29:4	14:21, 14:22,	based	book
adverse	16:12, 17:12,	16:3, 23:21	20:15, 21:3
28:12	19:5, 23:20,	bates-stamped	both
after	27:6, 29:2, 29:3	21:9	16:16
19:22	anything	because	bottom
agree	8:12	10:21	17:5, 17:19,
7:21	appeal	been	19:7, 21:10,
ald	1:2, 5:8	6:3, 8:16,	25:12, 25:21,
16:5, 16:19,	appear	8:19, 17:3,	26:3
17:1, 17:3,	12:21, 27:6	20:19	break
24:20, 24:22	appears	before	24:10
all	11:21, 13:20,	1:2, 2:5, 5:7,	briefly
5:12, 6:21,	16:2, 17:18	8:20, 15:20,	6:11, 21:18
10:11, 16:11,	asking	28:7	bulk
19:10, 19:17,	7:13	begins	8:20
23:16	aspect	5:2	C
allen	12:19	behalf	california
3:10, 5:16	aspects	3:2, 3:9, 5:17,	3:6
alone	13:19, 14:12,	5:19	call
12:14	19:12, 23:20,	being	16:5
along	24:6	25:19	called
14:17, 15:18,	assume	believe	14:4, 24:21,
16:2	8:1	9:13, 11:8,	25:18
already	atomic	12:3, 12:10,	calls
10:1	14:20, 17:2	19:9, 20:9,	11:9
also	attached	20:12, 23:7	can't
3:17, 9:5,	4:9, 9:22,	between	7:17, 10:21
12:17, 17:4,	18:2, 20:21,	9:16, 17:9	case
19:4	27:7	bics	1:5, 5:8
alternatively	attending	20:3, 20:5,	caution
22:17	5:13	20:9, 21:15,	15:22
	attorney	22:16, 23:8,	
	29:3		

cavities 19:22	commission 29:11	18:16, 18:19	day 8:20, 29:9
cavity 11:8, 15:11, 17:5, 22:10, 25:13	commonwealth 2:6, 28:3, 29:17	core 18:13	days 8:20
ceiling 14:4	company 1:8, 5:6	correct 7:5, 7:6, 20:16, 23:9, 23:18, 24:4, 24:8, 24:21, 25:4, 27:5	dc 3:13
cell 7:9	comparing 11:21, 12:3	corrections 27:6	debbie 5:21
center 9:6	complete 27:5	could 12:11, 15:2, 19:13, 20:13	debra 1:22, 2:5, 28:2
certify 28:3, 28:12, 28:16, 29:1	composite 15:2	counsel 5:14, 6:4, 28:13	declaration 6:18, 17:21, 18:7
chair 9:2	computer 9:3, 21:1	cover 6:20, 6:22, 12:5, 12:22	declarations 7:3, 8:7, 8:13
chamber 25:17	conducted 1:14, 2:2	covered 14:8	definitive 16:14
channel 22:10	conductive 9:16, 13:5, 19:15, 19:17, 19:19, 20:1, 22:21	couple 10:6	depend 19:20
chat 9:19, 17:20, 18:3, 18:19, 20:18	confirm 11:19, 21:15, 23:16	court 5:20	depending 24:22
chemical 14:20	confirming 24:3	cover 6:20, 6:22, 12:5, 12:22	depends 16:11, 25:15
cited 8:13	conformal 16:6, 17:7, 24:21, 24:22, 25:1, 25:7	covering 12:15	deponent 27:1
clarification 7:21	conforms 16:7	covers 14:5	depos 5:12, 5:22, 10:6
classes 20:12	contact 13:3, 17:9	create 13:22	deposit 15:13, 22:2, 23:10
cobalt 13:6	context 9:8, 9:12, 16:11	cross 3:10, 4:3, 5:16, 6:5, 9:18, 10:14, 10:17, 20:18, 21:9, 24:17, 26:4, 26:7	deposited 25:8, 25:19
cockrell 9:2	control 19:3	cross-section 18:11	depositing 13:4
color 19:10	copies 6:17	currently 6:12	deposition 1:13, 2:1, 4:10, 5:3, 5:13, 8:6, 8:10, 8:15, 8:21, 14:19, 14:20, 14:21, 15:6, 15:10, 15:12, 15:17, 16:9, 16:16, 16:20, 16:21, 17:2, 25:3, 25:6, 25:12, 25:16, 25:17,
column 11:12, 12:2, 13:3, 13:9, 13:11, 14:1, 14:2, 14:16	copper 13:6	cvd 16:5, 24:20, 24:22	
combination 13:7, 14:22	copy 6:18, 6:19, 10:1, 11:1, 17:20, 18:5,	D	
commencement 28:7		date 5:9, 27:10	

25:21, 26:3, 26:9, 28:6, 28:8, 28:14, 28:16 depositions 16:6, 24:21 describe 13:14 described 15:2, 20:8 describes 12:2, 21:21 description 11:22 details 20:14 determine 25:18, 25:20 device 20:6 devices 7:7 dielectric 15:3, 15:10, 22:11, 22:19, 23:13 dielectrics 15:14, 22:18 different 19:16, 22:18 dioxide 11:15 director 9:5, 9:7 discuss 17:13 discussed 19:12 discussing 17:12 documents 8:9 done 13:12 doped 23:11 down 17:5	downloading 10:13 dr 6:6, 8:9, 24:9, 24:18, 26:9 drain 22:8 drains 22:4 dry 14:7 duly 6:3, 28:6 dummy 11:9, 12:6, 12:15, 12:22, 13:15, 13:22, 14:3, 14:5, 14:9, 14:18, 15:11, 17:9, 22:7, 22:9 during 25:15 E e-notary 2:6, 28:2, 29:16 eastern 5:10, 26:10 edt 1:16, 26:11, 28:19 either 22:5 electrical 9:3 electrodes 22:2, 23:11 electronic 7:7 element 11:7, 11:11, 13:2, 14:15 employed 29:3 end 26:8	endorsed 21:7 engineering 9:3 entire 15:18 errata 27:7 esquire 3:3, 3:10 etch 19:22, 22:2, 22:9, 22:20, 23:13 etched 17:18 etching 14:7 ever 15:9 every 12:19 examination 4:2, 6:4 examined 27:3 example 16:10, 25:16 examples 11:15 exemplary 15:1 exhibit 4:10, 4:11, 4:12, 4:13, 9:20, 9:21, 10:3, 10:7, 18:1, 20:19, 20:20 exhibits 4:5, 4:8 expect 16:15, 16:19, 26:2 expires 29:11 explain 21:18	explicitly 12:2 extensively 15:7, 15:13 F fabrication 9:9 fair 8:3 familiar 15:5, 20:2 few 6:9, 6:10, 8:19 field 23:22 figure 10:18, 10:19, 11:4, 11:16, 12:8, 12:13, 12:15, 12:20, 13:16, 14:6, 14:9, 14:14, 15:16, 17:16, 19:2, 20:15, 21:4, 24:19 figures 11:21, 12:3, 12:17, 15:20 filed 7:5 fill 19:21, 22:9 fills 14:4 film 15:5, 15:9, 15:17, 16:1, 16:6, 25:9 financially 29:5 fine 10:2, 11:1 finish 7:15 first 22:3, 22:15 five-minute 24:10
--	---	---	---

flash 18:12, 22:14 follows 6:3 foregoing 27:4 form 9:10, 12:7, 12:9, 13:17, 15:19, 17:11, 19:11, 20:7, 23:19, 25:5, 25:14 formed 13:4, 14:17 forth 28:6 free 25:18 front 6:15, 10:1, 10:6, 10:9, 18:5 fully 7:18 further 26:4, 28:12, 28:16, 29:1 G gate 22:2, 22:5, 22:7, 22:9, 22:10, 22:11, 22:15, 23:11, 23:14, 24:4 gate-first 20:5, 20:13, 21:16, 21:19, 21:20, 22:1, 22:16, 24:1, 24:2 gate-last 20:5, 22:6, 22:12, 23:1, 23:3 gate-replacement 23:5, 23:9, 23:17	gates 19:3, 22:22 general 9:13, 17:6, 23:21, 25:22, 26:1 generally 25:7 give 16:5, 16:13, 16:14, 16:20, 18:16 given 27:6, 28:10 gives 11:15 go 6:10, 10:16 going 9:18, 16:20, 17:20, 22:18, 24:12, 26:10 gone 6:9 good 6:6, 6:7 gray 3:11, 5:17 great 17:22, 26:7 green 18:14, 19:1, 19:5 H hand 29:9 happens 25:15 happy 11:2, 17:13 hard 8:16, 11:1, 18:5 harrington 3:4 helpful 11:12	here 5:2 hereby 27:2, 28:3 hereinbefore 28:6 hereunto 29:8 high 13:20, 19:13 high-level 12:18, 15:21 highly 17:16, 23:11 hole 13:16, 14:5, 14:18, 15:11 holes 14:10 I illustrated 18:9 implant 22:4 implants 22:4, 22:8 inc 1:4, 5:5, 28:13 including 13:5 ink 18:17 insulating 11:14, 11:19, 12:5, 12:14, 13:15 insulation 14:3 interconnect 9:14, 9:17 interconnects 9:15 interested 29:5 interpret 15:22 interspersed 23:12	invention 12:19 ipr 1:5, 5:8 isolation 12:21 J january 9:4 jason 3:3, 5:18 job 1:20 joining 6:8 june 29:9 K keep 12:17 keeping 17:16 kelli 3:18, 5:11 know 6:9, 10:2, 10:14, 13:12, 15:21, 18:4, 19:14, 19:16, 23:21 knowledge 16:3, 23:22 known 19:4 kuhn's 8:9 L lang 3:3, 5:18, 9:10, 10:12, 10:16, 12:7, 12:9, 12:16, 13:17, 15:19, 17:11, 19:11, 19:18, 20:7,
---	--	--	---

21:7, 23:19, 24:5, 25:5, 25:14, 26:6 last 15:8, 21:12 later 14:10 layer 9:16, 11:14, 11:20, 12:2, 12:5, 12:14, 12:21, 13:15, 13:21, 14:3, 14:4, 14:8, 14:20, 15:2, 15:10, 15:17, 17:2, 17:4, 19:6 layers 18:14, 19:1, 19:5, 19:17, 19:19, 19:21, 20:1, 22:20, 23:13 leave 23:14 less 16:16 level 9:16, 9:17, 13:20, 19:13 limited 13:5 line 11:13, 13:3, 13:9, 13:12, 19:8, 19:9 lines 14:16, 19:4, 22:15, 22:22 literature 21:22 llp 3:4, 3:11 load 17:20, 20:18 located 6:13 looked 20:14	looking 14:14, 15:16, 17:15, 24:18 looks 12:20 lower 9:17 M made 19:14 make 17:9, 21:21, 22:1, 22:17, 22:19 makes 22:14 making 22:11 many 17:3 marked 4:5, 4:6, 4:8, 9:19, 9:21, 18:1, 20:19, 20:20 marks 26:8 marriage 29:3 marsh 3:5 mask 13:20, 22:4 material 19:15, 20:1, 22:21, 23:15 materials 6:15, 13:5, 15:1, 15:3 matter 5:4, 29:6 mean 9:11, 21:7, 25:18 means 16:6 meant 10:5	media 5:2 memory 1:7, 5:5, 5:17, 18:12, 18:13, 20:11 menlo 3:6 mentioned 24:19 microelectronics 9:6 micron 1:4, 5:4, 5:19, 28:13 micron's 8:10 middle 18:13 mind 7:14, 12:17, 17:16 mistake 16:22 monitor 5:10 more 16:13, 16:14, 16:15 morning 6:6, 6:7 mosfet 21:22, 22:13 multilayer 9:15 N nand 18:12, 20:3, 22:14 necessarily 12:19 nitride 15:4 nonconformal 16:11 none 4:6, 26:6	nothing 12:1 notice 2:5 number 5:3, 5:8, 10:8 nw 3:12 O oath 7:11 objection 9:10, 12:7, 12:9, 13:17, 15:19, 17:11, 19:11, 20:7, 23:19, 25:5, 25:14 objections 12:16, 19:18, 24:5 occupation 8:22 occurred 28:17 october 29:12 office 1:1, 5:7 often 12:18, 23:11 oh 7:3 okay 7:3, 10:17, 11:1, 13:10, 13:13, 18:8, 18:21, 19:10, 21:2, 24:11 once 10:2 one 10:12, 12:20, 15:21, 19:7, 19:8, 22:4, 22:7, 22:12, 22:14, 22:18
--	---	---	---

onwards 14:16 open 10:3, 17:21, 18:4, 18:19, 18:22, 20:22 opening 13:22 opined 9:11, 12:10, 13:18, 23:20 opposed 22:6 orick 3:4 original 6:18, 19:21 orrick 5:18 other 7:7, 8:8, 8:13, 14:21, 19:5, 25:11 otherwise 8:1, 29:5 out 7:1, 19:14, 19:22 outcome 29:6 outside 8:12 over 15:8 owner 1:9, 3:9, 6:4, 8:14 owner's 8:11 oxide 15:3	21:7, 21:8, 21:9, 21:10, 21:13 pages 1:21 paragraph 18:7, 18:10, 21:13, 23:6 parameters 25:1, 25:16 parentheses 14:6, 14:9 park 3:6, 6:20, 7:1, 8:8 part 14:1, 14:2, 22:19 parties 5:12, 29:2, 29:4 party 28:12 passage 13:14 past 8:19 patent 1:1, 1:2, 1:7, 1:9, 3:9, 5:6, 5:7, 6:4, 6:19, 6:20, 6:21, 7:1, 7:5, 8:8, 8:10, 8:14, 9:12, 9:19, 10:4, 10:5, 10:8, 14:1, 23:2, 24:19 patentee 17:17 path 25:18 pattern 13:21, 22:2, 22:7, 23:13 pennsylvania 3:12 petitioner 1:5, 3:2, 5:19	petitions 8:10 ph 1:13, 2:1, 4:2, 5:4, 6:2, 27:2, 28:5, 28:17 phone 7:9 photoresist 13:21, 14:8 physical 14:21, 16:9, 25:3, 25:6 place 23:15 planet 5:12, 5:21 please 5:14 point 12:11, 17:14 polycrystalline 23:12 polysilicon 13:7 portion 13:15 preliminaries 6:11 preparation 8:15 prepare 8:5 present 3:17, 11:20, 11:22, 12:4 pressure 25:17 previously 9:19, 9:21, 18:1, 20:20, 24:18 print 7:1 prior 4:8 probably 16:8	process 21:16, 21:19, 21:20, 22:1, 22:6, 22:16, 23:1, 23:4, 23:9, 23:17, 24:1, 24:3 processes 14:7, 14:11, 14:22, 15:6, 15:10 professor 9:2 public 2:6, 28:2, 29:16 purpose 24:7 pursuant 2:5 put 15:10, 15:17, 17:4, 18:19 pvd 16:8, 16:15, 16:20, 25:3, 25:11, 25:15, 26:1
Q			
question 7:20, 8:2 questions 7:13, 26:4 quite 8:16			
R			
read 13:11, 21:10, 21:12, 27:3 reason 7:17 recall 8:16, 17:12, 24:7 recent 6:17			
page 4:2, 4:10, 6:20, 6:22, 11:5, 11:16, 18:6, 21:6,			

recently 20:11 recess 24:14 recesses 14:18 record 24:13, 24:16, 26:10, 26:11, 28:9 redo 10:15 refer 23:3 referring 7:4, 23:5 refill 22:11, 22:21 regarding 7:5 region 12:22, 22:10 related 29:1 relevant 8:9 remote 5:11 remotely 5:13 removed 14:6, 17:8 removing 13:14 reopened 14:10 replacement 24:4 replies 8:11 reply 8:14, 17:21 report 12:11, 13:19, 14:13, 16:13, 17:13, 19:13, 20:9, 23:21, 24:7	reported 1:22 reporter 5:20 reports 8:9 represent 5:15 represented 28:13 representing 5:12, 5:21 research 9:6, 15:8, 15:13, 17:3 response 8:14 review 8:12, 8:18, 8:20 reviewed 8:7, 20:10 reviewing 8:19 right 10:11, 14:3, 23:16 road 3:5 ropes 3:11, 5:16	27:2, 28:5, 28:17 save 18:17 say 24:2 saying 16:18 says 11:14, 13:3, 14:1, 14:16 scalable 20:10 schematic 18:11 scope 12:9, 13:17, 17:11, 19:11, 20:7, 23:19, 25:5, 25:14 screen 10:20, 11:2, 18:20 second 10:12 see 10:21, 11:6, 11:22, 18:18, 21:11, 21:14 selector 19:8, 19:9 self-aligned 22:3, 22:8 semiconductor 9:9, 15:14 session 4:5 sessions 4:8 set 28:6, 29:8 share 10:20, 11:2, 18:20 sheet 27:7 should 10:7, 15:21,	18:3, 21:10 show 12:19 showing 18:12 shown 14:6, 14:9 side 14:18, 16:2, 16:17, 22:5, 25:9, 25:21 sides 18:13 signature 27:10 signature-plkal 29:13 signed 27:7 silicides 13:7 silicon 11:15, 15:3, 15:4, 23:12 similar 23:4 since 14:7 single 15:2 sketches 12:18, 15:21 some 11:15, 15:1, 26:2 something 16:4, 25:3 sorry 6:22, 16:15, 16:22, 18:17 source 11:10, 12:6, 12:15, 12:22, 13:16, 13:22, 14:3, 14:5, 14:9, 14:18, 15:11, 17:10, 19:8, 22:4, 22:8
--	--	---	---

spacer 14:17, 15:18, 17:5, 17:18 speaking 20:11 specialist 3:18, 5:2, 5:20, 24:12, 24:15, 26:8 species 25:19 specifically 9:12 specifics 16:13 sputtering 16:10, 25:4, 25:7, 25:11 stack 22:17, 23:10 staircase 23:14 staircases 18:12 stand 17:1 stands 17:2, 20:9 start 8:18 starting 10:18, 11:13 state 5:15, 6:12 states 1:1, 5:6 still 11:20, 11:22, 12:4, 25:12 strike 25:10 structure 11:10, 12:6, 12:15, 13:1, 14:1, 17:10, 17:17, 20:3, 22:20, 23:14 structures 15:15, 20:10	studying 8:16 stylized 17:17 substrate 16:7, 17:10 suitable 14:22 sure 18:18 suspect 16:4, 24:20 suspected 25:2 sutcliffe 3:4 sworn 6:1, 6:3, 28:7 T take 24:10 taken 24:14, 28:8 takes 22:12 talk 13:20 teach 20:12 techniques 14:19, 15:12, 16:9, 25:4, 25:6, 25:11 technologies 1:7, 5:5, 5:17 technology 1:4, 5:5, 16:4, 22:13, 22:16, 28:13 tell 8:22, 9:8, 11:7, 11:11, 12:13, 14:14, 18:9, 18:14, 19:1, 19:13 tend 16:5, 16:10	tends 17:6 term 21:21 terminologies 21:22 terminology 22:12 tessariol 6:19, 8:8 testified 6:3 testify 7:17 testimony 8:10, 27:4, 27:6, 28:9 texas 6:14, 9:4 text 12:1 textbook 20:17, 20:19, 21:8, 23:5 th 5:9, 28:18 thank 6:8, 26:5 themselves 5:15 thereby 14:10 thereof 13:8, 14:22 thickness 16:1, 25:8, 25:20 thicknesses 19:17, 19:20 thin 15:5, 15:9, 15:16 thing 7:2 think 10:15, 13:18, 21:21, 24:9 through 6:9, 6:10,	13:11 thursday 1:15, 28:18 time 5:9, 5:10, 26:10 today 5:11, 5:21, 7:11, 7:18 today's 4:5, 5:9, 8:5 told 15:20 took 21:3 top 16:16, 19:6, 19:8 topography 16:7 trademark 1:1, 5:7 transcription 27:5 trench 17:19 trial 1:2, 5:7 trouble 10:13 true 16:3, 27:4, 28:9 truthfully 7:18 trying 10:15, 10:20, 17:9 tungsten 13:6 turn 10:18, 11:12, 11:16, 13:9, 18:6, 21:6, 25:17 two 7:3, 7:4, 8:7, 18:12, 22:17
--	--	---	--

type 20:2	vertical 9:13, 9:14, 9:16	whitehead 1:22, 2:5, 5:21, 28:2	26:10, 26:11, 28:18
U	via 9:9, 9:13	whole 7:2	10,861,872 1:8, 10:8
unable 12:13	video 3:18, 5:2, 5:10, 5:13, 5:20, 24:12, 24:15, 26:8	within 15:11	1000 3:5
under 7:11	videographer 5:11	witness 6:1, 24:11, 28:5, 28:10, 29:8	1001 4:11, 9:20, 9:21, 10:3, 10:7
understand 7:11, 7:21, 8:1	videotaped 1:13, 2:1, 5:3	wouldn't 16:8, 23:8, 23:17	1015 3:6
uniform 15:17, 16:2, 16:16, 16:20, 16:21, 25:8, 25:22	virginia 2:7, 28:3, 29:17	wrong 20:13	1023 4:12, 20:19, 20:20
united 1:1, 5:6	virtually 1:14, 2:2, 28:9, 28:17	Y	1035 4:13, 18:1
university 9:4	voice-identify 5:14	yangtze 1:7, 5:5, 5:17	11 11:5
unmarked 6:17, 6:21	W	yeah 7:9, 10:6, 11:5, 12:1, 19:19, 23:10, 25:6	12 11:17
until 9:4	wait 7:15	year 9:5	131 21:6, 21:10
upload 9:18	wall 14:18	years 15:8, 17:3	14 11:13, 13:9, 14:2
upper 9:16	walls 16:2, 16:17, 25:9, 25:21	yesterday 8:17, 8:18	15 13:11, 14:1, 14:2
use 16:4, 22:8, 23:17, 24:3, 24:20, 25:2	want 11:2	yourself 21:12	16 12:2, 13:3, 14:16
useful 11:9	wanted 18:17	0	18 4:13
uses 22:7	washington 3:13	00789 1:5, 5:8	1999 9:7
using 13:20, 14:6, 14:19, 16:8, 17:3, 22:3, 25:11	way 10:21, 29:5	01 1:16, 5:10, 28:18	2
V	we're 24:15, 26:9	1	20006 3:13
vapor 14:20, 14:21	welch 3:18, 5:11	10 1:16, 5:10, 24:13, 24:16,	202 3:14
various 14:19, 15:14	wet 14:7		2024 1:5, 5:8
versions 17:17	whereof 29:8		2025 1:15, 5:9, 9:7, 28:18, 29:9
	whether 12:14		2027 29:12

Transcript of Sanjay Banerjee, Ph.D.
Conducted on May 29, 2025

39

2099 3:12 212 11:7, 13:16, 14:4, 14:5, 14:10, 14:18, 15:11 214 14:4 23 13:3 230 11:11, 11:14, 12:21, 14:3 232 13:21, 14:8 240 14:19 242 14:15, 14:17, 17:18 244 13:2, 13:4 27 18:6 29 1:15, 1:21, 4:12, 5:9, 28:18 2f 13:16, 14:6, 14:9 2j 10:19, 11:4, 11:21, 12:3 2k 14:14, 15:16, 17:16, 24:19 21 11:16, 11:21, 12:3, 12:8, 12:15, 12:21 3 31 29:12 37 24:13 3d 18:11, 20:2,	22:14 3rd 29:9 4 40 15:8 43 24:16 44 11:13 46 26:10, 26:11, 28:18 4708 3:14 5 50 18:7, 18:10 508 3:14 585435 1:20 6 61 13:9 614 3:7 623 9:19, 10:4 650 3:7 7 7427 3:7 8 872 6:19, 7:5, 8:7, 10:4, 10:5, 11:9, 23:1, 24:19 9 94025 3:6		
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