

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,

Petitioner,

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,

Patent Owner.

Case No.: IPR2024-00789
U.S. Patent No. 10,861,872

PATENT OWNER'S SUR-REPLY

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<i>Synopsys, Inc. v. ATopTech, Inc.</i> , 685 Fed. App’x 951 (Fed. Cir. 2017).....	19

LIST OF EXHIBITS

Exhibit	Description
Ex. 2001	July 29, 2024, Declaration of Dr. Kuhn (“Kuhn(I)”)
Ex. 2002	CV of Dr. Kuhn
Ex. 2003	Shur, “Introduction to Electronic Devices” (1996) (“Shur”)
Ex. 2004	Streetman, “Solid State Electronic Devices” (1995) (“Streetman”)
Ex. 2005	US Patent No. 8,766,336 (“Grupp”)
Ex. 2006	Declaration of Jonathan Bradford
Ex. 2007	January 17, 2025, Declaration of Dr. Kuhn (“Kuhn(II)”)
Ex. 2008	Deposition Transcript of Dr. Banerjee
Ex. 2009	Contact, New Oxford American Dictionary, Third Edition, 2010
Ex. 2010	Contact, Wiley Electrical and Electronics Engineering Dictionary, 2004
Ex. 2011	Electric Contact, McGraw-Hill Dictionary of Scientific and Technical Terms, Sixth Edition, 2002
Ex. 2012	Micron’s Preliminary Claim Constructions
Ex. 2013	Plaintiff’s Proposed Claim Constructions
Ex. 2014	Transcript to May 29, 2025, Deposition of Dr. Banerjee

LIST OF ABBREVIATIONS

Abbreviation	Term
'872	U.S. Pat. No. 10,861,872
'872FH	File History of U.S. Pat. No. 10,861,872
Banerjee(I)	April 17, 2024, Declaration of Sanjay Banerjee, Ph.D., in Support of Petition for <i>Inter Partes</i> Review of U.S. Patent No. 10,861,872
Banerjee(II)	April 25, 2025, Declaration of Sanjay Banerjee, Ph.D., in Support of Petitioner's Reply to Patent Owner's Response
Challenged Claims	'872, Claims 1-6 and 11-13
DI	Decision Granting Institution for <i>Inter Partes</i> Review of U.S. Patent No. 10,861,872 (IPR2024-00789, Paper 15)
Park	U.S. Pat. No. 9,859,297
Petition or Pet.	Petition for Inter Partes Review of U.S. Patent No. 10,861,872 (IPR2024-00789, Paper 1)
Patent Owner or PO	Yangtze Memory Technologies Co. Ltd.
Petitioner	Micron Technology, Inc.
POR	Patent Owner's Response
POSITA	Person of ordinary skill in the art
Reply	Petitioner's Reply
Tessariol	U.S. Patent Pub No. 2019/0081061

I. INTRODUCTION

Petitioner's Reply fails to address the issues raised in the POR, misunderstands the prior art, and misrepresents PO's positions. In addition, the Reply introduces new arguments, which the Board should disregard, as Petitioner needed to make its case in the Petition. 37 C.F.R. § 42.23(b); *Henny Penny Corp. v. Frymaster LLC*, 938 F.3d 1324, 1330-31 (Fed. Cir. 2019) (rejecting attempts to broaden the petition's ground in its reply). Because Petitioner has not been able to remedy the deficiencies in its Petition, the Board should uphold the validity of all Challenged Claims.

With respect to Ground 1, Park does not disclose the claimed dummy source structures surrounding the stair contact as required by each of the challenged claims. Petitioner's arguments rely on erroneous claim constructions of "dummy source structure" and "surrounding" based on misrepresentations of the '872 that the Board already preliminarily rejected in its decision to institute ("DI"). As the Board correctly observed, the '872 "distinguishes between dummy source structures and source structures" and "does not describe the dummy source structure as functioning as a source for the memory cells." DI 12-13. Moreover, "'surrounding' in claim 1...does not encompass structures on only two sides" because the "Specification repeatedly uses 'between' to describe objects in the middle of two structures." DI

13-16. In its Reply, Petitioner rehashes its claim construction arguments without substantively addressing the evidence cited by the Board and in the POR.

Regarding Ground 2, Tessariol does not disclose or render obvious the challenged claims because it fails to meet key requirements of the independent claim, especially those relating to the “dummy source structures.” The structures identified—namely, conductive vias 58 and dummy structures 60—do not individually or collectively satisfy all the limitations required by the claims. Conductive vias 58 are not dummy source structures under the proper construction and do not “surround” the staircase contact as expressly required. Meanwhile, dummy structures 60 lack a “conductive contact,” and Petitioner any motivation for a person of ordinary skill in the art (POSITA) to modify Tessariol to add this feature.

In its Reply, Petitioner repeats its arguments that the “conductive core” of dummy structures 60 is a conductive contact—it is not. Nor would it have been obvious to add a conductive contact, particularly when Petitioner’s expert, Dr. Banerjee, admits “there is no need for them to connect to upper-level devices.” Banerjee(I), ¶216. Petitioner also improperly introduces two new arguments in its Reply: first, that Tessariol’s dummy source structures land on a “conductively-doped substrate”; but Petitioner provides no evidence that the conductive core “allows current flow” to the substrate, and Dr. Banerjee testified contact to the substrate requires additionally etching the spacer. Banerjee Tr. at 15:5-17:19. And second,

Petitioner claims the “dummy source structure” has an “‘exposed’ top during manufacture”; but the relevant device in the trial ground is the finished memory device, not an intermediate product. Pet. 37-39.

As explained in the POR and further explained herein, the Petitioner’s Grounds fail to make the required showing of obviousness.

II. CLAIM CONSTRUCTION

A. “dummy source structure”

1. Patent Owner’s Construction Is Supported by the Intrinsic Evidence

The term “dummy source structure,” as used in the claims, should be given its plain and ordinary meaning: “a structure that does not function as a source to memory cells.” This interpretation is supported by the intrinsic evidence, including the patent specification, which distinguishes dummy source structures from actual source structures and never describes dummy source structures as providing source to memory cells. Instead, dummy source structures serve other roles, such as mechanical support or interconnection with peripheral devices, but not as a source for memory cells themselves. Under this proper construction, Ground 1 necessarily fails because it does not adopt PO’s construction. Reply 26.

As detailed in the POR (POR 19-20) and recognized by this Board (DI 9-11), the ’872 clearly differentiates “dummy source structures” from “source structures.”

Source structures provide source to the memory cells via the common source. '872, 16:34-38. And by using the qualifier “dummy,” the '872 distinguishes dummy source structures from actual source structures. '872, 16:38-44. While dummy source structures may serve as interconnects, or connect to channel structures, the '872 never describes them as providing source to the memory cells. '872, 5:40-43, 11:46-49; Kuhn(II) ¶¶61-63; *contra* Reply 14. Every embodiment in the specification supports PO's construction.

Petitioner's argument that the phrase “dummy source structure” has no plain and ordinary meaning is inapposite because the term “dummy” is used to modify “source structure” in accordance with the plain meaning of the term. As Dr. Kuhn testified, the use of “dummy” is commonly “applied to ... semiconductor features” “to describe an object that resembles another object but is missing some key functionality.” Ex. 1041, 1119:14-120:17. This is in accordance with the plain and ordinary meaning of “dummy,” and therefore, “a structure that does not provide source to the memory cells” accurately distinguishes a “source structure” from “dummy source structure” as providing source to the memory cells is the key functionality of a source structure in the context of the '872.

Petitioner's argument that the plain and ordinary meaning of “dummy” as a qualifier is an “inoperable component that structurally resembles the non-dummy component” is unsupported. *Contra* Reply 2-3 (citing Ex. 1036, 2). This

construction, specific to an unrelated Micron patent, does not claim to be plain and ordinary.¹ Ex. 1036, 2.

As for Petitioner’s “negative limitation” arguments (Reply 7-10) they are unavailing. First, PO’s construction does not “read in” a negative limitation, as it does not preclude the claimed device from using a structure that provides source to the memory cells—i.e., an actual source structure. But instead, the construction simply reflects the ordinary meaning of the claim language in light of the specification, which, as the Board recognized, properly distinguishes source structures from dummy source structures. DI 12-13.

Second, Petitioner’s argument that an express disclaimer or lexicography is required to support the construction is misplaced. *Contra* Reply 9-10 (citing *Ethicon LLC v. Intuitive Surgical, Inc.*, 847. Fed. App’x 901, 907 (Fed. Cir. 2021)). There is no need for an express disclaimer or special definition in the specification to support this construction, as it is grounded in the claim language itself and the ordinary meaning of the terms in light of the specification. As stated in *Ethicon*, negative limitations are appropriate if they are apparent from “the words of the claim.” 847. Fed. App’x at 91. Here, “dummy” is used to modify “source structure”

¹ In contrast, the parties agreed that “dummy channel structure[s]” for YMTC’s ’872 should have its “Plain and ordinary meaning.” Ex. 1036, 2.

to distinguishes itself from an actual “source structure.” The construction at issue does not import a limitation from the specification, but rather gives effect to the distinction drawn by the term itself.

2. Petitioner’s Proposed Construction Renders the Term “Dummy” Superfluous in Meaning, and Improperly Limits the Term “Dummy Source Structure” to a Process of Manufacture

Unlike PO’s construction, which give meaning to each word, Petitioner’s proposed construction of “the structure that occupies the void used for the gate line replacement process” improperly reads the word “dummy” out of the claims, thereby conflating dummy and non-dummy source structures. Moreover, Petitioner’s construction impermissibly reads into the claims a specific manufacturing process (the gate replacement process), contrary to established legal principles. In its Institution Decision, the Board has already correctly construed the term in line with PO’s position.

Petitioner’s reliance on *Andersen Corp. v. Fiber Composites, LLC* is inapposite. Reply 4-5 (citing 474 F.3d 1361, 1367 (Fed. Cir. 2007)). The term “dummy source structure” is never used “restrictively” as the structure that occupies the void used for the gate line replacement process. In fact, the two first embodiments described in the ’872’s summary of the invention describes the invention as using dummy source structures without ever mentioning the gate-last

process.² '872, 1:32-55. Petitioner's apparent attempts to tie the mention of "conductive layers" in the embodiments and claims to the gate-last process falls flat. Reply 3-4. As Dr. Banerjee admits, the 3D NAND memory device illustrated in his declaration "is a gate-first process" and has "conductive layers." Banerjee Tr. at 18:6-21:17. And Petitioner's suggestion that its construction does not limit the claim by its method of manufacture is unreasonable—the language of the construction expressly requires gate replacement. Reply, 5-7. That the construction "embraces that the 'dummy source structure' may be either a dielectric or conductive pillar" is inapposite. Simply because Petitioner's proposed construction does not improperly limit one aspect of the term does not mean that the construction avoids such an improper limit in another aspect of the same term to a specific embodiment. *Contra* Reply 7. Indeed, Petitioner attempts to do precisely that by construing "dummy source structure" as "the structure that occupies the void used for the gate line replacement process."

² In contrast to the first two embodiments, the third and fourth embodiments do describe using dummy source structures during the gate replacement process. '872 1:55-2:28.

B. “surrounding”

As reflected in the Board’s preliminary construction, the term “surrounding” should be given its plain and ordinary meaning, which requires features that are more than just on two sides with another structure “between.” DI 13-16; *see also* POR 23-28. The Board should maintain its preliminary construction because Petitioner does not, and simply cannot, identify any configuration in which the conductive contact is surrounded—i.e., by more than two structures—as required by the claims and specification. Under this construction, Petitioner’s Ground 1 necessarily fails.

The intrinsic evidence repeatedly and consistently distinguish between the concepts of “surrounding” and “between.” As the POR explained (POR 24-26), the ’872 uses the term “between” to describe the configuration of exactly two structures around a central object and uses the term “surrounding” (or “surround”) to refer to the configuration where four or more structures are around a central object. *See, e.g.*, ’872, 6:38-7:28, 4:56-61. This distinction is even evident in the language of the claims themselves, such as Claim 17, which describes a structure “surrounded by at least eight dummy source structures,” versus Claim 11, which describes a structure “located between the first and second staircase structure.” ’872, cls. 11, 17. And, while the ’872 contemplates “less than four dummy source structures that ‘surround’ a word line contact” (’872, 8:8-11)), the dispute here is not whether less than four (*e.g.*, three) dummy structures can “surround” a word line contact, but only

whether exactly two parallel dummy structures can “surround” a word line contact. Kuhn(II), ¶¶87-89.

Petitioner’s argument that the ’872 does “not speak to whether the GLSs ‘surround’ holes” but only describes the holes as “between” two GLSs (Reply 12) misses the mark. The ’872 repeatedly and consistently uses the terms “between” and “surrounding” to distinguish when a centralized structure has structures to just either side and when it has more than two structures around it. Indeed, the ’872 address the very parallel configuration of Park as being “between adjacent GLS.” ’872, 4:56-61. Ultimately, Petitioner fails to identify a single instance where the ’872 refers to just two objects as “surrounding” a central structure.

Notably, the size of the two structures and the extent to which those structures extend around the central object is immaterial. Petitioner rehashes its failed arguments from the Petition that parallel structures “can surround a contact to the same (or a greater) degree as four dummy source structures.” Reply, 10-14; Pet. 29-32. But, as explained in the POR, the distinction the ’872 is making is not one of degree or extent (i.e., the amount to which something is encircled) but the number

of structures around the object. POR 25-27.³ As Dr. Kuhn testified, “nowhere in the patent has there been any discussion of extent.” Ex. 1041, 138:9-15.

C. “conductive contact”

The term “conductive contact” should be interpreted as “a conductive structure that permits current flow with an adjoining conductive structure” based on both the intrinsic and extrinsic evidence.

As set forth in the POR, the claims of the ’872 specifically require a “conductive contact,” not merely a conductive material or core. POR 29. The use of the word “contact” in the claims indicates that the structure must do more than simply exist as a conductive material; it must serve as a structure that enables current

³ Petitioner mischaracterizes Dr. Kuhn’s testimony. Dr. Kuhn did not admit that a single structure can “surround,” in the context of the ’872, but that “a single fence could surround a home” as it applies to “acreage” (Ex. 1041, 138:1-15)—e.g., four sections of fence on each of the north, south, east, and west sides of the house would collectively surround the house. Petitioner fails to explain how this fence analogy applies to the ’872 where a single dummy source structure fully encircling a conductive contact would render that contact inoperable—by disconnecting it from the memory array.

to flow to another conductive structure. In contrast to Petitioner’s interpretation, PO’s construction gives full effect to the term “contact,” rather than reading it out of the claim or conflating it with a generic conductive core. The specification and drawings further support this construction by describing dummy source structures that form a “contact” with other structures, such as peripheral devices, thereby permitting current flow. For example, unlike Tessariol, the ’872 describes a dummy source structure that extends through an insulation layer to form an exposed conductive contact, which functions as an interconnect to other devices. ’872, 16:63-66; Kuhn(II) ¶¶103-106. As pointed out during the prosecution history (POR 11; *contra* Reply 21 (arguing PO ignored the prosecution history)), the ’872 explains “dummy source structure 178 includes a dummy source hole filled with conductive materials **as a contact** 179”—dummy source structure 178 conductive core behaves as a contact and not just as a pillar.⁴ Ex. 1002 (Part 2 of 2), 514-15; ’872, 11:37-39. This demonstrates that the “conductive contact” is not just any conductive material, but a conductive structure to permit current flow with another conductive structure.

Even Petitioner’s expert describes a “contact” as “a conductive via that provides a conductive path.” Ex. 1035, ¶62. And Dr. Banerjee has further explained that the term “via” in semiconductor fabrication is “an acronym for vertical

⁴ All emphasis and color annotations have been added unless otherwise noted.

interconnect access,” that is “a vertical conductive layer between an upper level [] interconnect [and] lower level interconnect.” Banerjee Tr. at 9:8-17. As even Dr. Banerjee’s testimony concedes, a “conductive contact” should not be reduced to any metal core that terminates in an insulating layer, which would clearly prevent interconnect access.

Contrary to Petitioner’s argument, that PO’s construction for “conductive contact” excludes certain types of “contacts” does not render the construction “improper” (Reply 15), but rather gives meaning to both “conductive” and “contact.” Indeed, there are many types of contacts that are not necessarily “conductive contacts,” e.g., inductive contacts, thermal contacts, and Schottky contacts (Kuhn ¶¶47-49).

On Reply, Petitioner also appears to conflate the terms “conductive contact” and “dummy source structure.” There is no requirement that all “conductive contacts” be a “vertical member extending through the stack” (Reply 16-17). That the ’872 discloses forming a conductive contact in the dummy source structure does not mean that all conductive contacts are part of dummy source structures and thus a “vertical member extending through the stack.” Regardless, PO’s constructions for “conductive contact” and “dummy source structure” are not “internally inconsistent.” *Contra* Reply 14-15. Petitioner fails to show the inconsistency of PO’s argument that the claims are directed towards “dummy source structure” (i.e.,

a structure that does not function as a source to memory cells), which includes a “conductive contact” (i.e., “a conductive structure that permits current flow with an adjoining conductive structure”). For example, the claims could be satisfied by a dummy source structure that either serves as an interconnect to peripheral devices without supplying source to the memory cells, or one that contacts an interconnect at one end but is an operative dead end on the other. As explained in the POR, the conductive contact does not require the flow of current but permits flow to an adjoining structure.

Petitioner takes issue with PO’s construction because it would “electrically connect to an adjoining structure...but not necessarily to a peripheral device.” Reply 17-18. But the ’872 does disclose structures that have a conductive contact to adjoining structures other than peripheral devices, *e.g.*, an actual “[s]ource structures...connected...via a common source.” ’872, 16:34-38. And the ’872 teaches that “dummy source structure” may “connect to channel structure” (’872, 16:38-40), which would be through a conductive contact to the adjoining substrate. See POR 17. Regardless, Petitioner’s argument is inapposite, there is no requirement that the specification disclose every possible configuration or use.⁵

⁵ Dr. Banerjee’s arguments regarding BiCS 3D NAND structure arguments are circular as there is no showing that the illustrated device includes a dummy source

The specification supports PO's construction by describing dummy source structures that contact other structures, such as peripheral devices, allowing current flow between conductive structures (POR, 30; Kuhn(II), ¶102). Petitioner faults PO's reliance on Fig. 2L because, standing by itself, does not show conductive contact adjoining another structure. But as explained in the POR and by Dr. Kuhn, a POSITA would have understood that the contact of Figure 2L is intentionally exposed (by extending past the insulating layer) to enable the dummy source structure to "function as an interconnect...with other peripheral devices." POR 30; '872, 16:63-66;⁶ Kuhn(II), ¶103; *see also* Banerjee Tr. at 12:5-13:1 (confirming

structure and are in direct contradiction with his earlier opinions. *Compare* Banerjee(II), ¶50 ("how these dummy source and source structures function as sources [] was well known") *with* ¶17 ("I have never heard of 'dummy source structure' before reading the '872").

⁶ Petitioner misrepresents Dr. Kuhn's testimony (Reply 18) by suggesting she confirmed there is no adjoining structure by admitting "nothing is shown on the top of the contact." First, the questions were limited to "just looking at...Figure 2L" without the context of the written specification. Ex. 1041 at 77:9-12. And second, Dr. Kuhn states "it is perhaps *intrinsically clear, that there is more stuff to follow,*

insulating layer in Fig. 2L does not “cover...the dummy source structure”). Notably, neither Petitioner nor Dr. Banerjee provides any other reason for why the “conductive contact” would be left exposed in Fig. 2L.

Moreover, Petitioner mischaracterizes PO’s position regarding the patent’s statement that “[w]hen conductive materials are used to fill dummy source hole 212 (e.g., contact 244), the dummy source structure 246 may function as an interconnect to connect 3D memory device 100 with other peripheral devices,” (’872, 16:63-66). Reply 19. The POR does not “admit this sentence means that the contact ‘may or may not function as an interconnect,’” but only makes clear that “contact 244” is provided as an example where the dummy source structure functions as an interconnect—consistent with PO’s construction. POR 31. The unaltered quote is “that the **‘dummy source structure’ with ‘conductive material’** [that] may or may not function as an interconnect.” POR 31 (emphasis in original).

Finally, Petitioner’s attempts to distinguish the dictionary definitions provided in the POR fall flat. First, Petitioner faults PO for “cit[ing] a definition for ‘electrical contact,’ not contact,” but fails to appreciate the full definition, which reads: “A physical contact that permits current flow between conducting parts. **Also**

because many of the additional structure that occur, bit lines in the light do not appear to be shown.” Ex. 1041 at 77:15-18.

known as contact.” Ex. 2011, 690. Second, PO did not “cherry pick” a definition from Wiley Electrical and Electronics Engineering Dictionary, but instead identified the most relevant definition, which describes an “electric contact”; Petitioner, on the other hand, relies on the definition that the dictionary ascribes to components like a “button, switch, or relay” that “serve to open and close.” See Ex.2010, 142-43. As for the New Oxford definition (Ex. 2009), Petitioner fails to explain how it is inconsistent with Patent Owner’s construction.

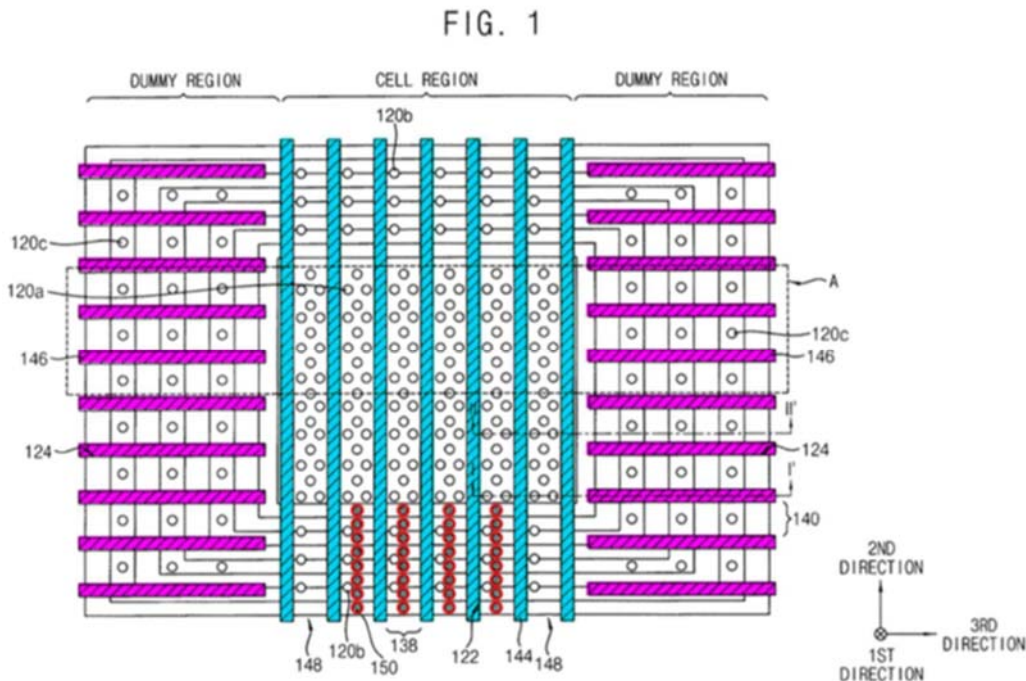
III. GROUND 1: PARK DOES NOT DISCLOSE OR RENDER OBVIOUS CLAIMS 1-6, 11, AND 13

A. Claim 1

1. Park’s Common Source Lines and Dummy Source Lines, Alone or in Combination, Are Not “Surrounding” the Contact Plugs (limitation [1.e])

Park’s common source lines do not “surround” the contact plugs as required by the Challenged Claims because, under the proper construction of “surrounding,” it is not sufficient for the contact plugs to simply be “between” two dummy source structures. The claims specifically require that a plurality of dummy source structures “surround” the staircase contact, which means more than just being present on two sides of the contact plug. See §II.B *supra*; Kuhn ¶¶82-85.

In Park, Petitioner maps the claimed “staircase contact” to Park’s contact plugs 150 (red) and the claimed “dummy source structures” to both Park’s common source lines 144 (blue) and dummy source lines 146 (pink):



Park, Fig. 1 (PO’s annotations in color). However, Petitioner’s Reply focuses solely on Park’s common source lines 144. Reply 25-26.

As explained in the POR, Park’s arrangement is identical to the prior art that the invention sought to improve upon, where the contacts are also just “between” parallel lines, not surrounded. On Reply, Petitioner argues only that the ’872 contemplates “laterally-extending” dummy source structures—without engaging with whether Park’s structures “surround” the conductive contact under the Board’s preliminary and PO’s construction—they do not. *Contra* Reply 25-26. Instead,

Petitioner argues only that “Park’s lines ‘surround’...to a greater degree” than the ’872’s express embodiments—but the ’872 nowhere suggests that the measure of “surrounding” is one of degree. It is not. *See* §II.B *supra*; Kuhn ¶¶88-91.

As the Board correctly recognized in its preliminary decision, the plain meaning of “surrounding” requires more than being flanked on two sides. DI 14-16. Structures that are only on two sides of an object, leaving the object merely “between” them, do not satisfy this requirement. There is no dispute that Park’s common source lines 144 fail to disclose or render this limitation obvious under Board’s preliminary construction.

2. Park’s Common Source Lines Are Not “Dummy Source Structures” (Limitation [1.e])

Park’s common source lines are not “dummy source structures” because they serve as sources for memory cells, which is contrary to the correct construction of a dummy source structure in the ’872. As correctly noted in the Board’s preliminary construction, a dummy source structure does not function as a source to memory cells. DI 11-13. In Park, the common source lines (144) are specifically designed and described as providing the source connection necessary for the operation of the memory cells, making them actual source structures—not dummy source structures. Kuhn(II) ¶¶139-142; Park, 6:1-11, 7:59-60, 13:39-41. On Reply, Petitioner only

argues that the Board should reject PO's construction of "dummy source structure."

Reply 26. Petitioner's argument fails for at least the reasons provided in §II.A.

B. Claim 2:

Park does not disclose dummy source structures located adjacent to the staircase contact as required. The structures identified by Petitioner (common source lines 144) are not dummy source structures because they serve as actual sources for memory cells, not as non-functional or "dummy" structures. POR 48. Petitioner's Reply only refers to its claim construction arguments for claim 1 (Reply 27), which fail for the reasons above.

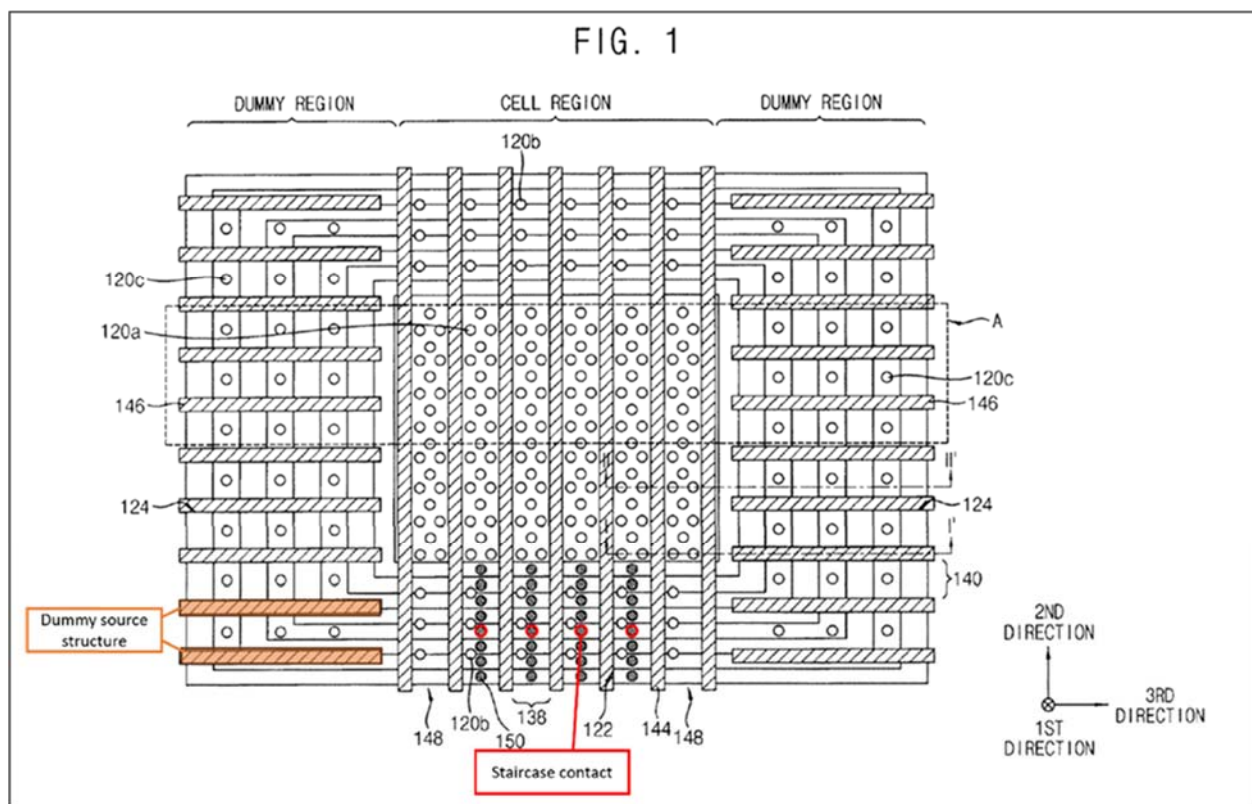
C. Claims 3-4:

Park does not show that at least two dummy source structures are of nominally equal lateral distances to the staircase contact as required by Claims 3 and 4. Petitioner relies on Park's Figure 1 to argue for uniform distribution, but the figure lacks scale or dimensions, making it impossible to determine actual distances. Federal Circuit law does not allow reliance on unscaled drawings for such measurements, and Petitioner does not argue that it would have been obvious to modify Park to meet this requirement. POR 48-49. Petitioner's reliance on *Synopsys, Inc. v. ATopTech, Inc.* is inapposite. Reply 24 (citing 685 Fed. App'x 951, 954 (Fed. Cir. 2017)). *Synopsys* makes no mention of deciphering relative dimensions from

figures but instead reversed the Board's anticipation ruling where the prior art figures failed to disclose eliminating “superfluous levels of hierarchy above said atomic blocks” of an FPGA.

D. Claims 5-6:

Park does not disclose dummy source structures arranged in a first row that extends along a first lateral direction as required by claim 5. For claim 5, Petitioner relies on dummy source lines 146 (orange below):



Pet. 69 (annotating Park Fig.1). On Reply, Petitioner fails to address “dummy source lines 146” and presumably no longer argues that these structures surround the staircase contact as required by parent claim 1. Reply 25-26. Petitioner’s reference

to its “surrounding” claim construction arguments for claim 1 (Reply 27) also do not cure this deficiency.

Claim 6 depends from claim 5 and fails for at least the same reasons. Moreover, Park does not disclose at least two dummy source structures arranged in a second row perpendicular to the first lateral direction. The mapped common source lines span the entire cell region and are not organized in a row as required by the claim. Instead, they extend across the whole region, failing to meet the organizational requirement. POR 51-52. On Reply, Petitioner only reiterates its arguments from the petition but fails to address PO’s arguments. Reply 70.

E. Claim 11:

Park does not disclose a dummy source structure located between first and second staircase contacts. The structures identified by Petitioner (common source lines 144) are not dummy source structures, as they function as actual sources for the memory cells. Petitioner’s Reply only refers to its claim construction arguments for claim 1 (Reply 27), which fail for the reasons above.

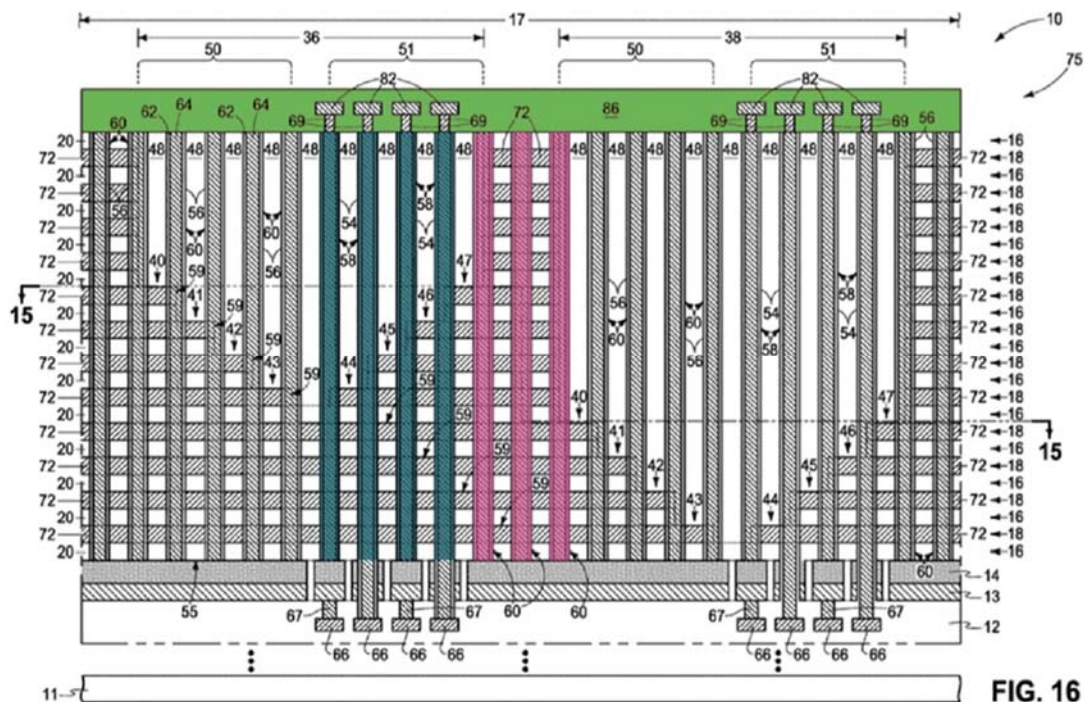
IV. GROUND 2: TESSARIOL DOES NOT DISCLOSE OR RENDER OBVIOUS CLAIMS 1-6, AND 11-13

A. Tessariol’s Dummy Structures Do Not Comprise a “Conductive Contact” Under the Proper Construction (Limitation [1.f])

Tessariol’s dummy structures do not have conductive vias because they are intentionally designed and constructed to lack the required “conductive contact” as

defined by the claims. Specifically, a “conductive contact” is more than just a piece of conductive material; it is a conductive structure that permits current flow with an adjoining conductive structure. *See* §II.C *supra*.

In Tessariol, the dummy structures (pink) with conductive cores do not permit flow with an adjoining conductive structure because the core is surrounded on the sides by insulating lining 62 and on the top by insulating material 86 (green), which effectively prevents any electrical connection to other structures:⁷



⁷ Petitioner does not address the POR arguments that Tessariol’s conductive vias are not dummy source structures and instead directs its arguments to Tessariol’s dummy vias. Reply 21.

Tessariol, Fig. 16; *see also* Kuhn(II) ¶186-195.

Petitioner’s arguments that PO “asks more of the prior art than the ’872,” is wrong. Unlike Tessariol’s conductive core that is covered on all sides and the top by insulator, the ’872 shows that the dummy source structure’s conductive contact is exposed. And, where the ’872 explains that the dummy source structure can act as an interconnect, Tessariol explains that while its dummy structures may be conductive, they are not part of a circuit because they only mimic the physical properties (not the functional properties) of their operative counterparts. Ex. 1006, [0068]; POR 22-23. Petitioner’s argument that Tessariol’s conductive core is exposed “during manufacture,” is not only new—and should be rejected for that reason alone—but it is also irrelevant. Reply 23. The claims are not directed to a half-manufactured “three-dimensional (3D) memory device,” but a complete device. Regardless, the trial grounds did not show that such half-manufactured device meets each of the claim limitations.

As for Petitioner’s argument about the bottom of Tessariol’s dummy structures (Reply 22-23), this should be rejected as another new improper argument, and nonetheless fails. Even if Tessariol’s dummy vias “land on ‘conductively-doped semiconductor substrate,’” Petitioner has failed to show that the “conductive core” makes contact with the doped substrate and that it permits current flow to the doped substrate. First, as Petitioner’s expert Dr. Banerjee testified, the deposition of

insulating liner/spacer of an opening through the stack would result in insulating material deposited at the bottom of the hole. Banerjee Tr. at 15:5-17:19, 25:11-26:3. As such, there is no disclosure that the conductive core would land on the substrate directly, and thus no disclosure that it would permit current flow to the substrate. Indeed, a POSITA would not expect to remove this insulating liner of dummy structure 60, which only mimics the physical properties and not functional properties of conductive vias. Ex. 1006, [0068]. And, even if the conductive core lands directly on the substrate, which Petitioner has failed to show, just because the substrate is “conductively doped” does not mean the conductive core would permit current to flow to the substrate. As Dr. Kuhn explained, “special processing (e.g. the semiconductor must be highly-doped with an appropriate species to match the work function of the metal) is required to form a conductive contact between metal and semiconductor.” Kuhn(II) ¶¶192-193.

B. A POSITA Would Not Have Been Motivated to Couple Tessariol’s Dummy Source Structures to Upper-Level Interconnect Lines (Limitation [1.f])

Not only does Tessariol not disclose conductive contacts in its dummy structures, but Petitioner has also not shown why it would have been obvious to add a conductive contact. There is no motivation or functional reason for a person of ordinary skill in the art to add such contacts, as doing so would not simplify the

manufacturing process or reduce process steps. Instead, such a modification would only serve to complicate the design with needless additional features—as Dr. Banerjee explains, unlike the conductive vias, “interconnects 82 are simply not made on the dummy structures, because **there is no need for them to connect to upper-level devices.**” Banerjee(I), ¶216; *see also* Kuhn(II), ¶¶199-205.⁸ Expert testimony confirms that conductive material surrounded by insulation cannot serve as a conductive contact, and that a metal-to-semiconductor interface does not form a conductive contact unless specifically engineered with high levels of doping. Kuhn(I), ¶51; Kuhn(II), ¶193. Because Tessariol’s dummy structures are intentionally isolated by insulation and do not permit current flow with adjoining conductive structures, they fail to meet the requirements of limitation [1.f]. The technical details and expert analysis confirm that these dummy structures do not, and would not, include conductive vias or contacts.

Petitioner also mischaracterizes Dr. Kuhn’s statements regarding patterning. Dr. Kuhn did not admit that “by including the interconnects on the dummy vias, this allows for a consistent, repeating interconnect pattern, which simplifies design and fabrication and enables other benefits.” Reply 23. Rather, as Dr. Kuhn explained

⁸ That PO relied on, and restated Dr. Kuhn’s reasoned opinion does not diminish the weight of her testimony.

when asked about the specifics of “via patterning” (the issue with the proposed modification of Tessariol), she refused to admit that “regular patterns are [] intrinsically easier to make” and then provided several examples from her experience, “where regular patterns are actually very hard to make, because they are on a very tight pitch.” Ex. 1041, 67:4-68:18 (listing secondary manufacturing issues with patterning regular arrays including: difficulty patterning regular arrays “because of interactions between the elements,” “lithographic effects that are undesirable,” “challenges with etch and polish” requiring “elaborate computer models”). Regardless, belying Petitioner’s purported motivation (Reply 23), the evidence shows that adding interconnects 82 (orange) to Tessariol’s dummy source structures 60 (pink) would **not** “simplif[y] processing and reduce[] costs”:

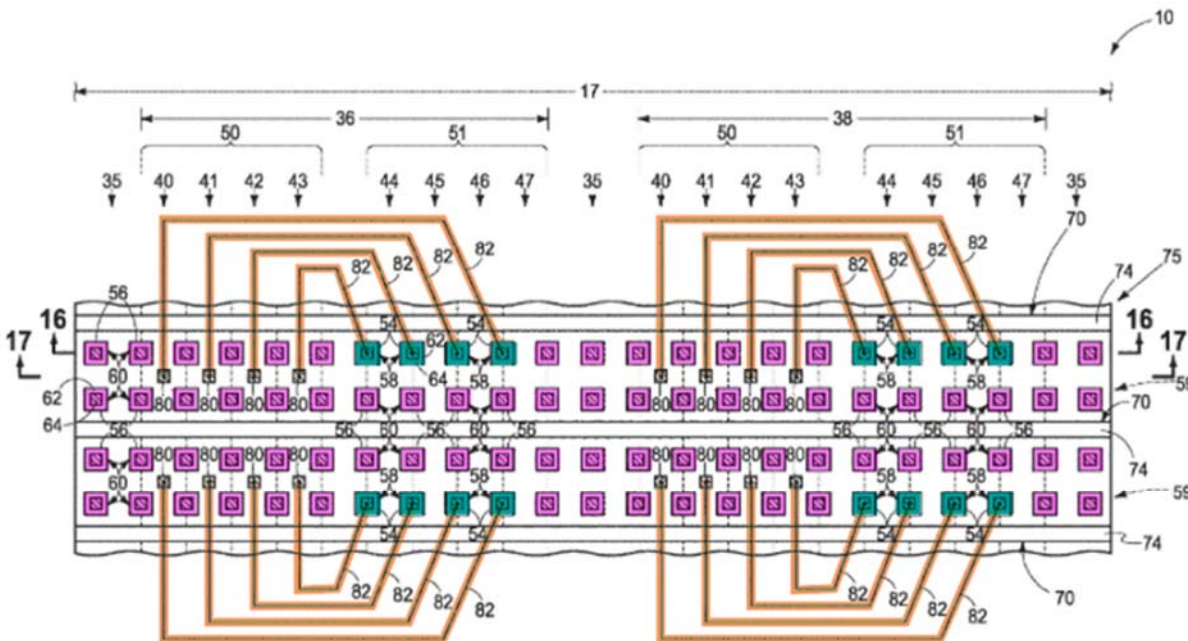


FIG. 15

Tessariol, Fig. 15 (highlighting dummy structures 60 (pink) and existing interconnects 82 (green) from conductive vias 58 (blue)); *see also* (Kuhn(II) ¶¶198-204.

C. Claims 3-4

As explained in the POR, Tessariol does not disclose, either expressly or inherently, that at least two of the plurality of dummy source structures are of nominally equal lateral distances to the staircase contact, as required by Claims 3 and 4. The only figure cited by Petitioner, Figure 15, does not provide any scale, dimensions, or reference points that would allow a person of ordinary skill in the art to determine the actual or designed distances between the dummy structures and the staircase contact. Without such information, it is not possible to conclude that the required distance relationship is present in Tessariol.

Petitioner faults PO for “fail[ing] to appreciate Tessariol’s complete disclosure” and provides new quotes from Tessariol regarding “arrayed” openings 54 and 56. Reply 25 (quoting Tessariol, [0037]). But this paragraph was not directly cited in Petitioner’s mapping of Claims 3-4 and only provided by through a cross reference to an earlier section. *See* Pet. 93-94 (cross referencing §XI.A.6 which,

citing the relevant paragraph, makes no mention of arrayed openings).⁹ And while the quote mentions the openings may be “arrayed” there is no discussion about relative distances to conductive contacts. As to Petitioner’s “nominal” arguments, there is no evidence that Tessariol’s Figure reflects a “design,” which in semiconductor fabrication would need to be drawn to-scale. Petitioner also refers to the same flawed case law and “design” arguments made for the Park Ground. Reply 23-24. It fails for the reasons provided in §III.C above.

V. CONCLUSION

Petitioner has failed to demonstrate by a preponderance of the evidence that any of the Challenged Claims of the ’872 is anticipated or obvious. Accordingly, the Board should uphold the validity of all Challenged Claims.

Dated: June 6, 2025

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⁹ Claiming the Petition demonstrates Tessariol’s disclosure of these claims, the Reply point back to the Petition’s discussion of Park without explaining its relevance. See Reply 24 (citing Pet., 65-67).

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CERTIFICATE OF WORD COUNT

The undersigned certifies that the foregoing PATENT OWNER'S SUR-REPLY 37 under C.F.R. § 42.23 complies with the type-volume limitation in 37 C.F.R. § 42.24(c). According to the word-processing system's word count, the brief contains 5,550 words, excluding the parts of the brief exempted by 37 C.F.R. § 42.24(c).

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CERTIFICATE OF SERVICE

The undersigned certifies that the foregoing PATENT OWNER'S SUR-REPLY was served in its entirety by filing through the Patent Trial and Appeal Case Tracking System (P-TACTS), as well as providing a courtesy copy via e-mail to the following attorneys of record for Petitioner listed below:

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