

Micron Technology, Inc.
Petitioner
v.
Yangtze Memory Technologies Company, Ltd.
Patent Owner

IPR2024-00789 (U.S. Patent No. 10,861,872)

Micron's Hearing Demonstratives

July 29, 2025

Roadmap

1. The 872 IPR Grounds
2. The 872 Patent
3. The Tessariol Ground
 - A. The Petition, Preliminary Response, and Institution Decision
 - B. Claim Construction: “Conductive Contact”
 - C. POR Arguments Fail
4. The Park Ground
 - A. The Petition, Preliminary Response, and Institution Decision
 - B. Claim Construction
 1. “Dummy Source Structure”
 2. “Surrounding”
 - C. POR Arguments Fail

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872 Instituted Grounds

- Tessariol Ground: applicable under Board’s preliminary construction of “dummy source structure”
 - Claims 1-6 and 11-13 are obvious over Tessariol (Ground 2)
 - For claim 1, PO argues only that Tessariol does not disclose, or render obvious, that its dummy source structure comprises a “conductive contact.”
 - For claims 3-4, PO argues only that Tessariol does not disclose its dummy source structures being “nominally equal lateral distances” to the staircase contact.

872 Petition (Paper 1), 8; 872 Reply (Paper 22), 1, 24.

- Park Ground: applicable under Micron’s construction of “dummy source structure”
 - Claims 1-6, 11, and 13 are obvious over Park (Ground 1)
 - For claim 1, PO argues only that Park does not disclose, or render obvious, “dummy source structures surrounding the staircase contact.”
 - For claims 3-4 and 6, PO raises the same “nominally equal lateral distances” argument and disputes that Park’s dummy source structures are in a row from east to west.

872 Petition (Paper 1), 8; 872 Reply (Paper 22), 27.

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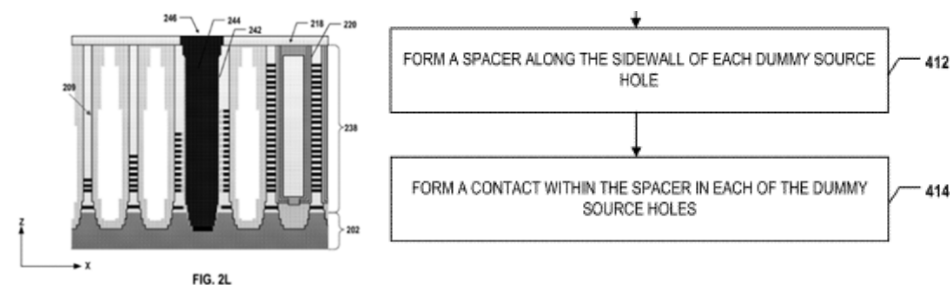
Specification of 872 Patent: “Dummy Source Structure” Includes a “Conductive Contact”

- Dummy source structure with a conductive contact:

tures and/or staircase contacts in the staircase region. Each dummy source structure may include an insulating spacer layer in a dummy source hole and a conductive contact within the spacer layer. In some embodiments, one or more dummy source structures are in contact with the substrate and may provide interconnect between the 3D memory device and peripheral devices. The dummy source structures

872 Patent, 5:37-43 (Petition (Paper 1), 84).

Petition (Paper 1), 84.



872 Patent, Figs. 2L, 4 (partial) (Reply (Paper 22), 17, 63).

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Petition's Showing: "Dummy Source Structures Surrounding the Staircase Contact"

- The Petition demonstrates that four Tessariol dummy vias (60), i.e., “dummy source structures” “surround[] the staircase contact”:

Petition (Paper 1), 88.

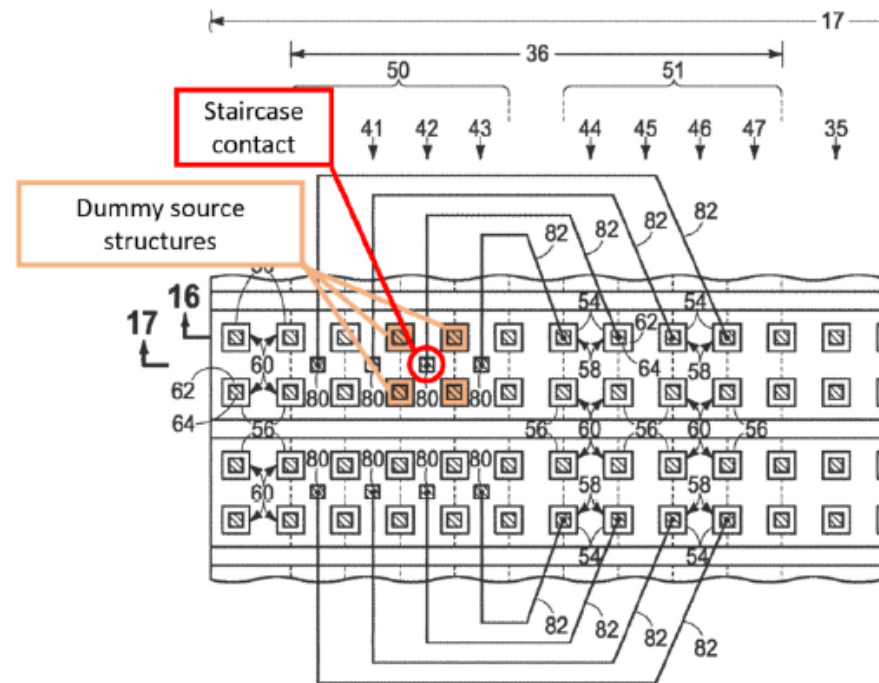


FIG. 15

Tessariol, Fig. 15 (Petition (Paper 1), 88).

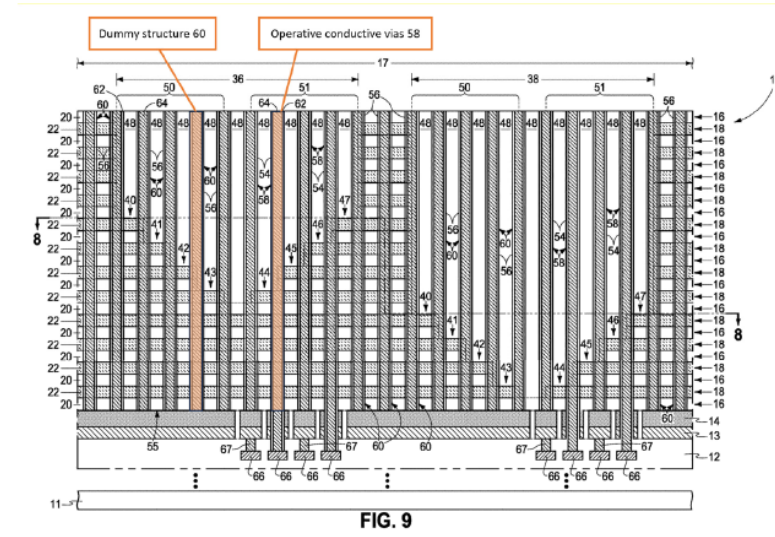
Petition's Showing: Tessariol's Dummy Vias Have a Conductive Contact

- The Petition demonstrates that Tessariol discloses a “conductive contact” because it discloses a conductive pillar through the stack, just like the 872 patent’s “conductive contact.”
 - “In some embodiments, dummy source structure 178 includes a dummy source **hole filled with conductive materials as a contact 179.**”

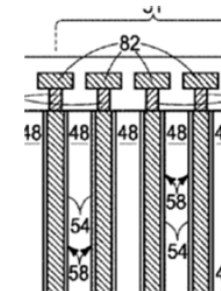
872 Patent, 11:37-39 (Petition (Paper 1), 89).

- Further, the Petition demonstrates it would have been obvious for the Tessariol dummy vias to include the same structure as the active vias to reduce processing time and cost.

Petition (Paper 1), 90.



Tessariol, Fig. 9 (Petition (Paper 1), 85).



Tessariol, Fig. 16 (Petition (Paper 1), 91).

POPR and Preliminary Sur-reply Argument, and the Board's Institution Decision

- PO argued that “conductive contact” is a “a functional property, not just a physical property, of the operative structure.”

POPR (Paper 11), 41.

- The Board correctly rejected this argument, reasoning:
 - “[i]n some *embodiments*, one or more dummy source structures are in contact with the substrate and may provide interconnect between the 3D memory device and peripheral devices.’ Ex. 1001, 5:37–43 (emphasis added). Thus, it follows that, in some embodiments, a dummy source structure comprising a conductive contact *does not contact* the substrate or provide interconnect with peripheral devices.”
 - “The ’872 patent also teaches that, ‘[w]hen conductive materials are used to fill dummy source hole 212 (e.g., contact 244), the dummy source structure 246 *may function* as an interconnect to connect 3D memory device 100 with other peripheral devices.’ *Id.* at 16:63–66. Here, the permissive use of “may function” indicates that dummy source structure 246 might not function as an interconnect, even when it comprises a contact made of conductive materials.”
 - “Moreover, the ’872 patent does not clearly express an intent to require dummy structures comprising conductive contacts to physically contact another structure or to act as an interconnect to peripheral devices.”

ID (Paper 15), 23-24.

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Claim Construction: The POR Doubles Down On Its Erroneous Interpretation of “Conductive Contact”

- PO argues that “conductive contact” should be construed to mean “a conductive structure that permits current flow with an adjoining conductive structure.”

Reply (Paper 22), 14 (citing POR (Paper 18), 28).

1. PO’s construction runs contrary to:
 - a) Its own interpretation of “dummy source structure”;
 - b) The specification; and
 - c) The file history.
2. Legally, PO’s construction would require a disclaimer or definitional language, and PO cites none.
3. At bottom, PO and its expert attempt to construe “conductive contact” to be an “interconnect,” which the 872 Patent expressly distinguishes from a “conductive contact.”

Reply (Paper 22), 14-21.

“Conductive Contact”: (1)(a) PO’s Inconsistent Positions

- PO argues that a “dummy source structure” (which “comprises a conductive contact”) can be a mechanical support member with an electrical dead-end.

Reply (Paper 22), 14-15 (citing POR, 15, 17).

function as a source to the memory cells. KuhnII, ¶61. For example, the “dummy source structures”—as the qualifying term “dummy” suggests—“function[] as a mechanical supporting structure.” Ex. 1001, 16:38-44. And while the ’872 patent

POR (Paper 18), 15.

(i.e., connects the memory cells to source power). For example, while one end of the dummy source structure may connect to channel structures via the substrate (or the source plane), the other end of the dummy source structure may be an electrical dead end (e.g., floating) or may connect to peripheral devices instead of a ground source. Accordingly, the cited portion of the specification does not support

POR (Paper 18), 17.

“Conductive Contact”: (1)(a) PO’s Inconsistent Positions

- PO argues that a “dummy source structure” (which “comprises a conductive contact”) must “permit current flow.”

Reply (Paper 22), 14-15 (citing POR, 28, 32).

C. “conductive contact” (Claims 1, 13)

The term “conductive contact” should be construed as **a conductive structure that permits current flow with an adjoining conductive structure.** KuhnII, ¶¶95-111. This construction properly gives meaning to the word “contact” in the claims

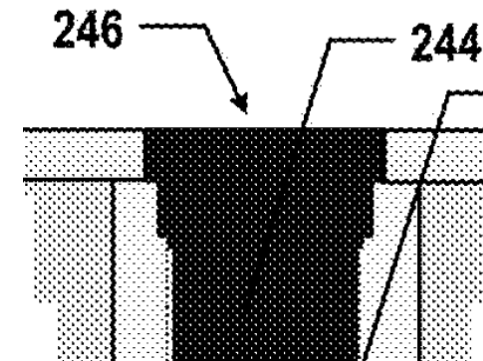
POR (Paper 18), 28.

“Conductive Contact”: (1)(b) The Specification Uniformly Describes the “Conductive Contact” as the Conductive Fill

- The specification describes the conductive contact as the conductive material that fills the dummy source hole:

Reply (Paper 22), 15.

holes. As illustrated in FIG. 2L, a contact 244 is formed within spacer 242 in dummy source hole 212 (shown in FIG. 2K). Contact 244 can be formed by depositing conductive materials including, not limited to, W, Co, Cu, Al, polysilicon, silicides, or any combination thereof, over spacer 242 in the dummy source hole using one or more thin film deposition processes, such as ALD, CVD, PVD, any other suitable processes, or any combination thereof. A dummy source structure 246 including spacer 242 and contact 244 is thereby formed in the dummy source hole, surrounded by a plurality of dummy channel structures 209. In the inner



872 Patent, 16:21-32, Fig. 2L (Reply (Paper 22), 15-16).

- The specification uniformly describes the “conductive contact” to be this vertical, conductive structure through the stack: 872 Patent, 2:2-8, 5:37-43, 11:37-39, 16:13-21, 16:50-53, 18:38-41.

Petition (Paper 1), 84; Reply (Paper 22), 16-17.

“Conductive Contact”: (1)(b) The Specification Describes the Forming of the “Conductive Contact” without Reference to an “Adjoining Structure”

- The specification describes completing fabrication of the “conductive contact” without reference to any adjoining structure:

Reply (Paper 22), 16-17.

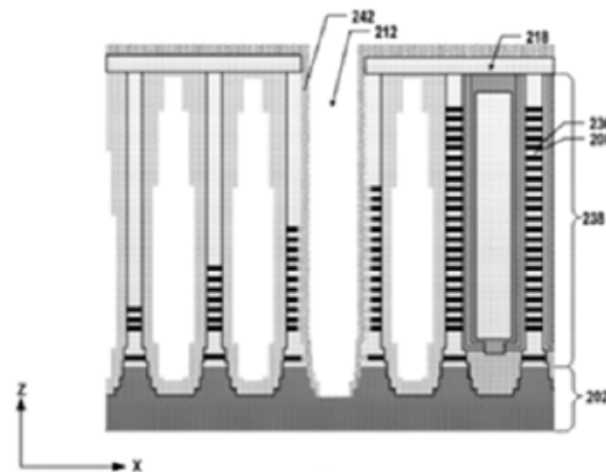


FIG. 2K

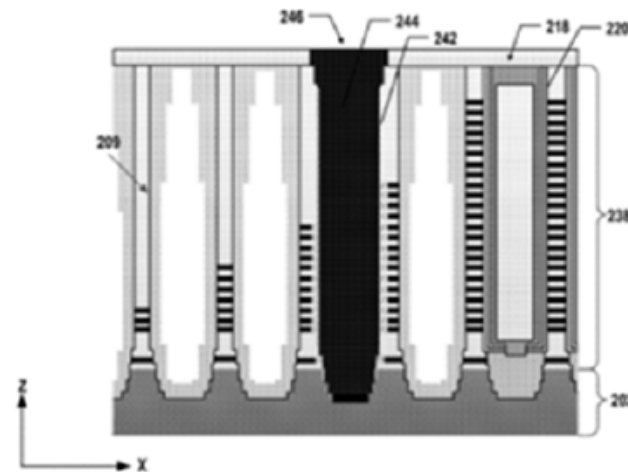
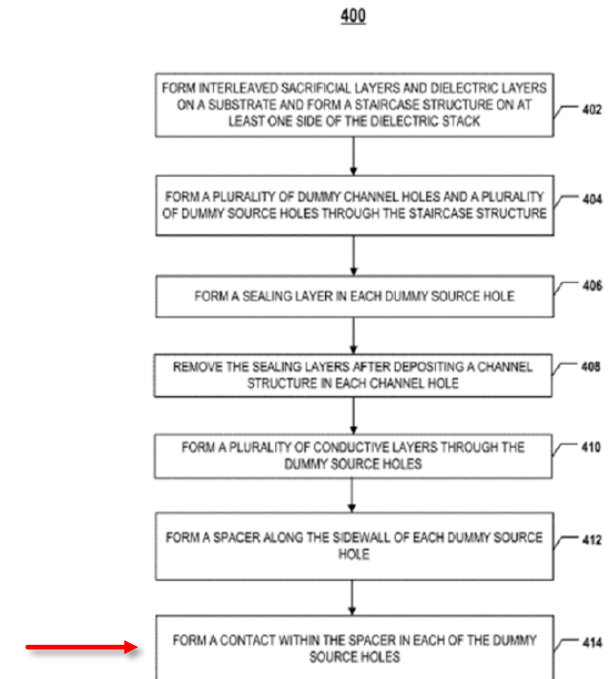


FIG. 2L



872 Patent, Figs. 2K, 2L, Fig. 4 (Reply (Paper 22), 16-17).

“Conductive Contact”: (1)(b) PO Cannot Explain Away the Specification’s Permissive Language

- The specification uses permissive language when explaining that a dummy source structure may function as an interconnect, i.e., connect different elements—after all, it is a “dummy” structure:

within the spacer layer. In some embodiments, one or more dummy source structures are in contact with the substrate and may provide interconnect between the 3D memory device and peripheral devices. The dummy source structures

Petition (Paper 1), 27; Reply (Paper 22), 18-19.

thereof. When conductive materials are used to fill dummy source hole 212 (e.g., contact 244), the dummy source structure 246 may function as an interconnect to connect 3D memory device 100 with other peripheral devices. When

872 Patent, 5:40-43 (Petition (Paper 1), 27).

872 Patent, 16:63-67 (Reply (Paper 22), 18-19).

- PO’s argument that “contact” the bottom passage refers to an example of a “conductive material to form an interconnect” (POR, 31) rewrites the sentence to: “contact 244,” i.e., “conductive material to form an interconnect” “[may or may not function] as an interconnect.”

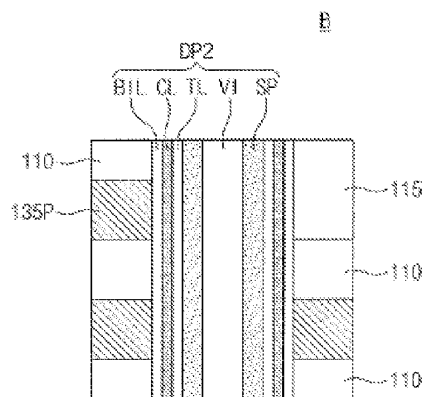
Reply (Paper 22), 19.

“Conductive Contact”: (1)(c) The File History Confirms “Conductive Contact” Is the Conductive Fill

- The File History distinguishes the **non-conductive fill in the Jeong prior art reference** from the conductive fill in the 872 Patent’s dummy source hole, that is, the “conductive contact.”

Jeong

Jeong does not disclose dummy source structures, but simply discloses dummy pillars. The dummy pillars in Jeong are different from the claimed “dummy source structure” in amended independent claims 1 and 8 at least because the dummy pillars do not include conductive contacts. Jeong explains the construction of the dummy pillars in FIGs. 4A, 4B, 4C, and 4D. Taking FIG. 4A as an example (because it is the most elaborate example in Jeong), the dummy pillar (DP2) includes the following:



As shown at left:

BIL = blocking insulating layer

CL = charge storage layer

TL = tunnel insulating layer

VI = vertical insulating pattern

SP = vertical semiconductor pattern

*Ex. 1002 (File History), 514
(Reply (Paper 22), 21).*

“Conductive Contact”: (1)(c) The File History Confirms “Conductive Contact” Is the Conductive Fill

- The File History distinguishes the non-conductive fill in the Jeong prior art reference from **the conductive fill in the 872 Patent’s dummy source hole, that is, the “conductive contact.”**

872 Patent

By contrast, FIG. 1D (reproduced below) illustrates an example of a dummy source structure 178, including contact 179 and spacer 177 (see also, FIG. 2L, dummy source structure 178, contact 244, and spacer 244). Nothing in Jeong’s pillar is conductive contact, as the pillar consists of insulating layers, a semiconductor pattern, and a charge storage layer. By contrast, as explained at paragraph [0057] of the present application: “In some embodiments, dummy source structure 178 includes a dummy source hole filled with conductive materials as a contact 179. Dummy source structure 178 can further include a spacer 177 made of any suitable dielectric materials (e.g., silicon oxide) between contact 179 and memory stack 160 to electrically separate surrounding conductive layers 106 in memory stack 160 from contact 179. As a result, dummy source structures 178 can laterally separate 3D memory device 100 into multiple memory regions, such as memory blocks.”

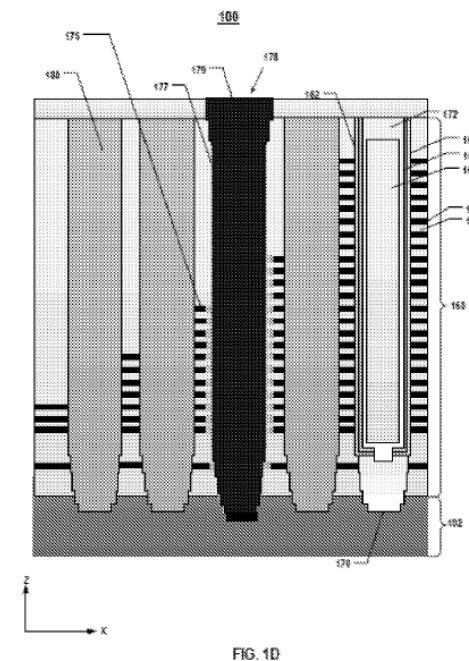


FIG. 1D

Ex. 1002 (File History), 514-15 (Reply (Paper 22), 21).

“Conductive Contact”: (2) PO’s Expert Establishes that PO’s Construction Legally Requires a Disclaimer or Definition—Which PO Fails to Offer

- Dr. Kuhn concedes that the term “contact” is an “***unusually broad word***”

Ex. 1041, 155:7-156:14, (Reply (Paper 22), 15).

- Dr. Kuhn concedes that a “contact” does not require a functional contact that connects to an adjoining structure.

Ex. 1041, 31:24-32:10, (Reply (Paper 22), 15, 15 n.3) (see also Ex. 1041, 20:1-23 (“But there's contacts that simply do not flow current at all, for a variety of reasons, of which no doping happens to be one’)).

Q. And in that work, did any of it involve a contact pad that did not have something physically, an adjoining structure, making contact with it?

A. Well, in a test chip, the contact pads do not have a conductive structure touching them at the time they are made. They have a conductive structure touching them later on.

Q. And then --

A. Or they may not, if the conductive structure may never touch it. It just happens to be helpful to the layout to have a contact pad in that location.

“Conductive Contact”: (2) PO’s Expert Establishes that PO’s Construction Legally Requires a Disclaimer or Definition—Which PO Fails to Offer

- Dr. Kuhn concedes that PO’s construction excludes certain “contacts.”

Ex. 1041, 20:3-23 (Reply (Paper 22), 15, n. 3).

Does your construction of "conductive contact," in your second declaration, include within its scope, a Schottky contact?

ATTORNEY BONNY: Objection. Form.

THE WITNESS: So if we step back and look at my construction, which is a conductive structure that permits current flow with an adjoining conductive structure, an ohmic contact generally meets that.

A Schottky contact may or may not meet that. And, in particular, because a Schottky contact has essentially no conduction at low voltages, if you don't know the voltages involved in your product, it would not meet that.

And last but not least, there are contacts which I did not describe in my first report, because I was being more idealistic. But there's contacts that simply do not flow current at all, for a variety of reasons, of which no doping happens to be one.

“Conductive Contact”: (3) PO’s Construction Amounts to “Interconnect”—Which the Patentee Expressly Chose Not to Claim

- Dr. Kuhn recognizes that the 872 Patent uses “interconnect” to refer to an element that connects two structures:

Q. Or you could say **interconnect**, because
it's connecting those two things?

A. And the interconnect is better. **That's**
the language the patent uses.

Ex. 1041, 164:2-5 (Reply (Paper 22), 19).

- The 872 Patent:

regions, such as memory blocks. **In some embodiments, dummy source structures 178 may function as interconnects to connect 3D memory device 100 with other peripheral devices.**

872 Patent, 11:46-49 (Reply (Paper 22), 19).

- Federal Circuit precedent holds that it would be error to construe “contact” to have the meaning of “interconnect,” because patentee expressly chose to use different language.

Reply (Paper 22), 19 (citing Acumed LLC v. Stryker Corp., 483 F.3d 800, 807 (Fed. Cir. 2007)).

“Conductive Contact”: PO’s Extrinsic Evidence Does Not Support Its Position

- PO cites to Ex. 2011 for a definition of “electrical contact,” not “contact,” and Dr. Kuhn admits that an “electrical contact” is an “interconnect.”

Reply (Paper 22), 20 (citing Ex. 1041, 35:14-37:13).

- PO cites Ex. 2009-2010 that are consistent with Micron’s interpretation: The conductive core provides a path through the stack, which may or may not make an electrical connection depending on whether it is an interconnect.

- Ex. 2010: includes “[a] part or device which serves to open or close an electric circuit. **Such a part or device may or may not act with another part or device.**”
- Ex. 2009: includes “or a part or device **by which such a connection is made**”

Reply (Paper 22), 20.

- PO’s interpretation of this evidence is legally irrelevant, because it is error to rely on “extrinsic evidence that [is] inconsistent with the more reliable intrinsic evidence.”

Tempo Lighting, Inc. v. Tivoli, LLC, 742 F.3d 973, 977 (Fed. Cir. 2014) (Reply (Paper 22), 20.).

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Summary

- Claim 1: PO argues Tessariol does not disclose, or render obvious, a “conductive contact.”
 1. PO relies on its legally erroneous claim construction of “conductive contact”;
 2. PO demands more of the prior art than the 872 Patent discloses;
 3. Even under its legally erroneous claim construction, Tessariol discloses a “conductive contact”; and
 4. Even under its legally erroneous claim construction, Tessariol renders obvious a “conductive contact.”

Reply (Paper 22), 21-24 (POR, 58-65).

Claim 1: (1) PO Relies on Its Legally Erroneous Claim Construction

- PO relies on its incorrect construction of "conductive contact" that amounts to "interconnect":

1001, 11:37-39, 16:21-32, 16:63-66; KuhnII, ¶187. This conductive contact enables the dummy source structure to "function as an interconnect to connect 3D memory device 100 with other peripheral devices" (*id.*, 16:63-66), and in view of this connection, the conductive contact structure is a conductive structure that permits current flow with an adjoining conductive structure, as required by PO's construction. KuhnII, ¶188.

In contrast, Petitioner has not shown that dummy structures 60 in Tessariol is a conductive structure that permits current flow with an adjoining conductive structure. KuhnII, ¶189. On the sides, Tessariol's dummy structures 60 are covered

POR, 59-60.

- The Board should reject PO's legally erroneous claim construction.

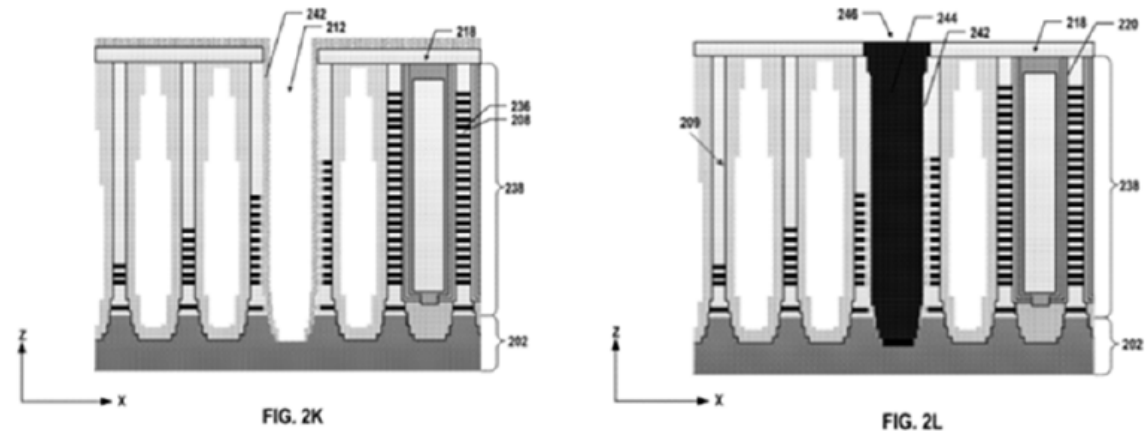
POR, 60 (Reply (Paper 22), 19, 21).

Claim 1: (2) PO Cannot Demand More from the Prior Art than What the 872 Patent Discloses

- The 872 Patent and Tessariol disclose the same conductive core as a “conductive contact.”
 - E.g., Dr. Kuhn concedes that the 872 Patent depicts no doping under the dummy source structure.

Reply (Paper 22), 18, 22 (citing Ex. 1041, 21:12-21 (need doping), 28:3-29:4 (same), 72:1-19 (does not describe doping in region 118), 74:22-75:21 (same), 78:7- 14 (same), 89:10-90:14 (no doping), 87:20-89:25 (same).

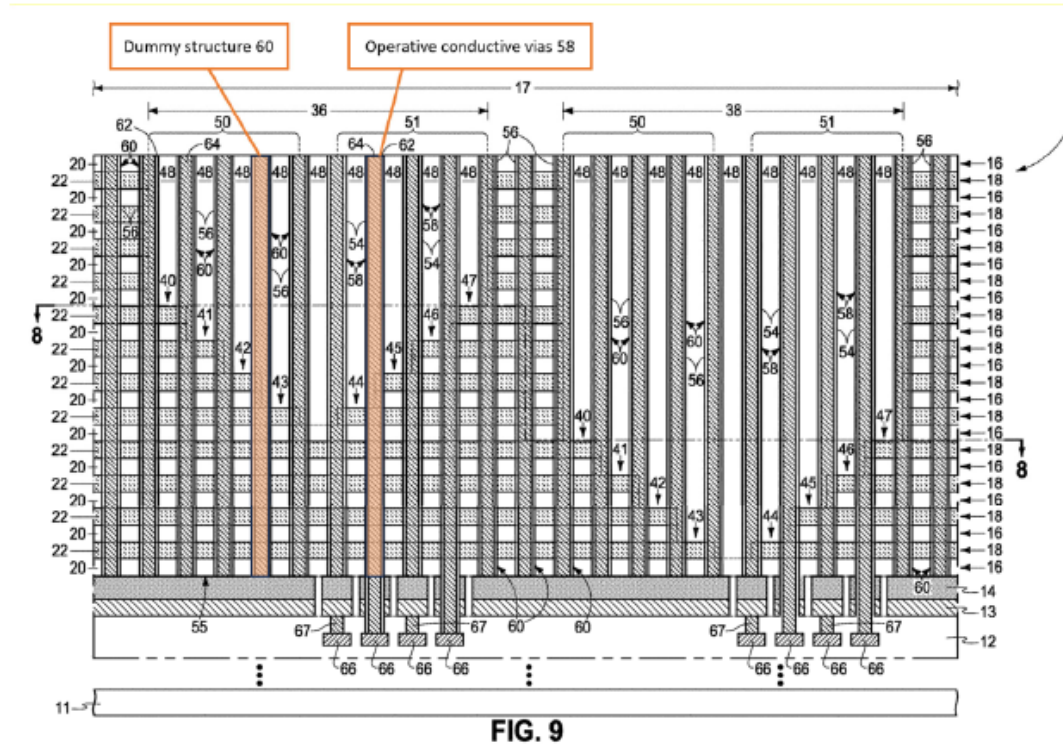
holes. As illustrated in FIG. 2L, a contact 244 is formed within spacer 242 in dummy source hole 212 (shown in FIG. 2K). Contact 244 can be formed by depositing conductive materials including, not limited to, W, Co, Cu, Al, polysilicon, silicides, or any combination thereof, over spacer 242 in the dummy source hole using one or more thin film deposition processes, such as ALD, CVD, PVD, any other suitable processes, or any combination thereof. A dummy source structure 246 including spacer 242 and contact 244 is thereby formed in the dummy source hole, surrounded by a plurality of dummy channel structures 209. In the inner



872 Patent, 16:21-32, Figs. 2K-2L (Reply (Paper 22), 15-16, 22).

Claim 1: (2) PO Cannot Demand More from the Prior Art than What the 872 Patent Discloses

- Tessariol and the 872 Patent disclose the same conductive core as a “conductive contact.”



Tessariol, Fig. 9 (Petition (Paper 1), 85); Reply (Paper 22), 22.

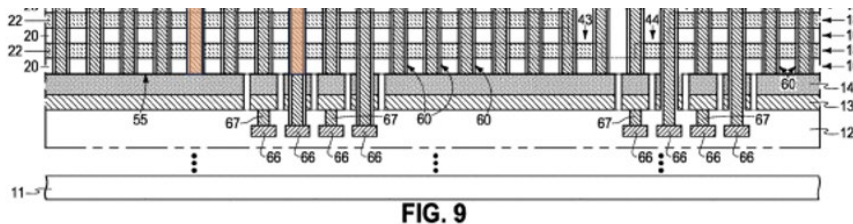
Claim 1: (3) Tessariol Discloses a “Conductive Contact” Under PO’s Incorrect Construction

- Dr. Kuhn describes that PO’s construction requires “an adjoining structure,” such as a “block of doping” under the dummy source structure.

Then if there were a little block of doping underneath 202 -- sorry -- underneath 244, within 202, that's not shown, that would have the two conductive parts would be a conductive contact.

Ex. 1041, 89:17-20 (Reply (Paper 22), 18, 22-23).

- Tessariol discloses doping under its dummy source structures.



may also be considered as an array. Above base substrate 11 are example substrate material 12 (e.g., insulating material and/or semiconductor material), conductive material 13 (e.g., metal material), and conductively-doped source material 14 (e.g., conductively-doped semiconductor material).

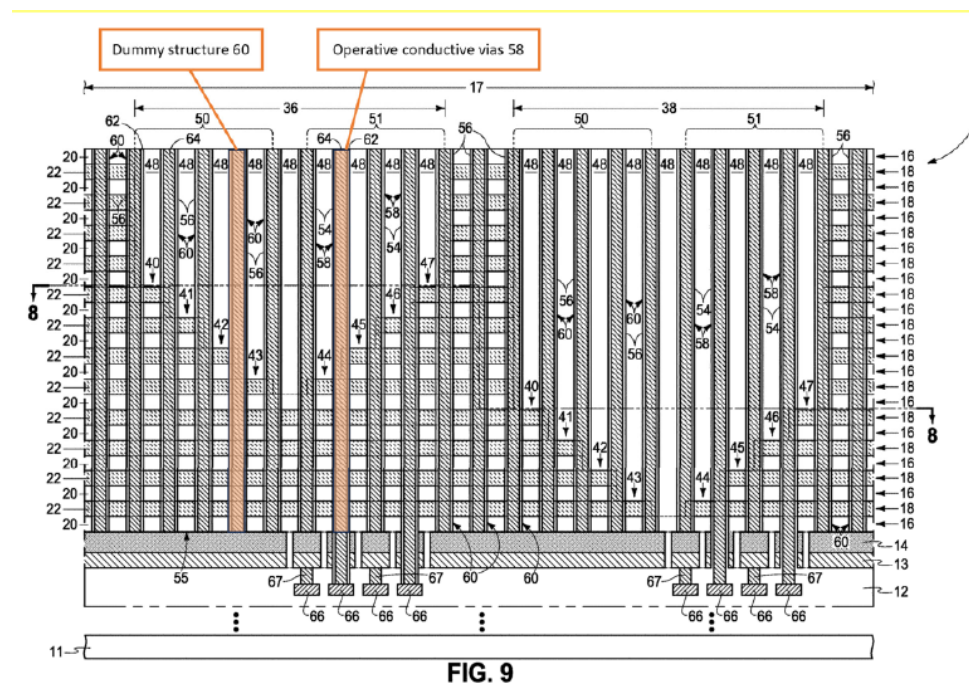
Tessariol, [0027], Fig. 9 (Reply (Paper 22), 22-23) (Petition (Paper 1), 37-38).

Claim 1: (3) Tessariol Discloses a “Conductive Contact” Under PO’s Incorrect Construction

- Tessariol describes forming the dummy vias and active vias at the same time.

[0038] Operative conductive vias 58 have been formed within via openings 54, thereby individually extending elevationally through insulating material 48, through one of steps 40-47, and through vertically-alternating tiers 16, 18 of first and second stacks 24, 30, respectively, at least to bottom 55 of vertically-alternating tiers 16, 18. Dummy structures 60 have been formed within dummy openings 56, thereby also individually extending elevationally through insulating material 48, through vertically-alternating tiers 16, 18, and through one of steps 40-47 at least to bottom 55 of vertically-alternating tiers 16, 18. In one embodiment, operative conductive vias 58 and dummy structures 60 are formed at the same time. In one embodiment and as shown, dummy structures 60 and operative conductive vias 58 are formed to comprise an insulative lining 62 (e.g., silicon dioxide and/or silicon nitride) and a conductive core 64 (e.g., metal material). In one embodiment, insulative linings 62 and conductive cores 64 in dummy-structure openings 56 and in via openings 54 are formed at the same time.

Tessariol, [0038] (Petition (Paper 1), 84).

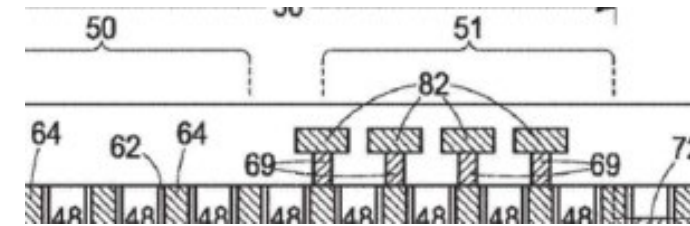


Tessariol, Fig. 9 (Petition (Paper 1), 85).

Claim 1: (4) Tessariol Renders Obvious a “Conductive Contact” Under PO’s Incorrect Construction: the Petition

- The Petition explains that each dummy via may have the same structure as the active vias, because that design reduces processing time and cost:

Second, at the very minimum, it would have been obvious that Tessariol’s dummy structures would include the same structure as the conductive vias that do *contact* the upper-level interconnect, and thus include a *contact* even under PO’s erroneous argument (i.e., they can contact an upper-level interconnect). Again,



Petition (Paper 1), 90-91 (Tessariol, Fig. 16).

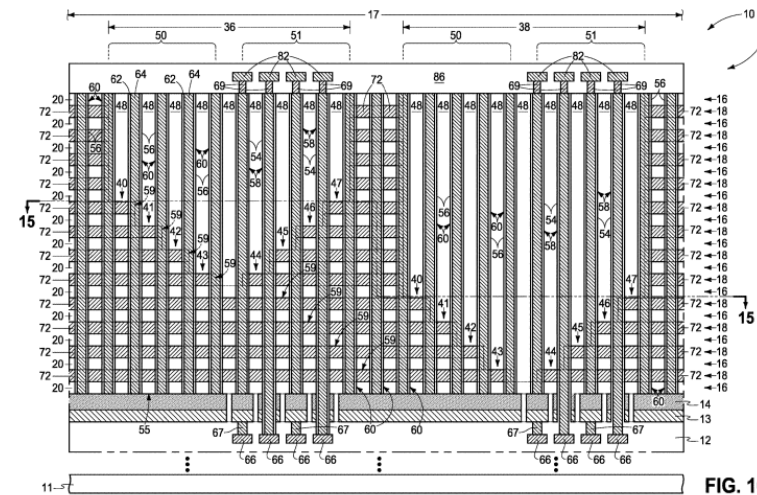


FIG. 16

Tessariol, Fig. 16 (Petition (Paper 1), 90-91).

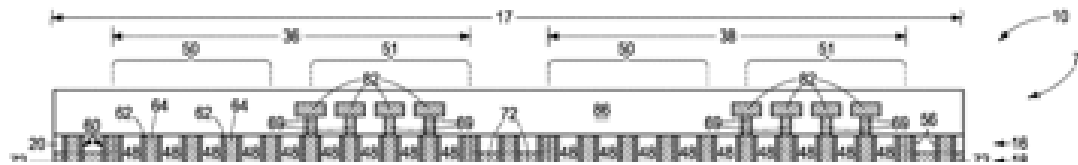
Claim 1: (4) Tessariol Renders Obvious a “Conductive Contact” Under PO’s Incorrect Construction: The Reply

- Tessariol states: “a ‘dummy structure’ refers to a structure **which is used** to mimic a physical property of another structure . . . **and which may comprise a circuit inoperable electrical dead end** (e.g., is not part of a current flow path of a circuit even if conductive).”

Reply (Paper 22), 23-24 (citing Tessariol, [0068]).

- Dr. Banerjee details it would be obvious to add the top structure to improve fabrication due to regular pattern.

Reply (Paper 22), 23-24.



Tessariol, Fig. 16 (Petition (Paper 1), 90-91).

82. As shown above, while the conductive pillars (both dummies and operable vias) are in a consistent pattern, the interconnects (69/82) above are not. This requires in the design phase, therefore, repeating this irregular pattern on top, rather than just replicating the consistent pattern. Similarly, when creating the masks, there is an irregular mask pattern that is necessary. It is more straightforward to implement repeating patterns, which adding interconnects onto the dummies would enable, for several reasons. Repeating structures are easier to pattern during lithography, and subsequent reactive ion etching. Lithography at such small geometries is complicated by diffraction effects, which distort the pattern relative to what is designed on the mask. There are also distortions due to so-called proximity effects from close by neighboring structures. If the patterns are regular, the proximity effects are more predictable, leading to more uniform lithographic patterning. These distortions can be more easily corrected for regular geometries by creating an intentionally distorted pattern on the mask generated by inverse modeling of the diffracted pattern. After lithography, the patterns are typically etched by plasma-based reactive ion etching (RIE). Here, too, there can be irregularities in the etch rates due to neighboring structures which can consume the reactant gases, leading to so-called micro-loading effects. If the patterns are regular, there will be more predictable, uniform micro-loading during RIE.

Claim 1: (4) Tessariol Renders Obvious a “Conductive Contact” Under PO’s Incorrect Construction: Dr. Kuhn’s Testimony

- Dr. Kuhn concedes that a repeating pattern can simplify fabrication.

Q. And sometimes it would be helpful to have a contact pad in a particular location, just because you are going to fabricate a repeating pattern.

Is that correct?

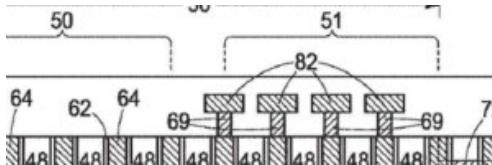
A. It is common in the art to have structures fabricated repeatedly, because it assists other parts of the process. Polish, for example, is very fond of having multiple replicas of a structure. Some of which may not be functional.

Q. On a mask.

A. The usual way -- and one can go down a whole lot of -- there's other ways to do this, but for example, as we see in databases, there will be a physically drawn cell, or group of cells, or block of cells, that is drawn with great precision and has a name.

And then that group is replicated through the remainder of the design.

- Dr. Kuhn concedes that, without the dummy vias having structures 82, it is an irregular pattern.



Q. Right. But instead, what they have done is this is actually an irregular pattern. Because there's four -- a pattern of four. And then an irregular space. And then the pattern of four is repeated. Right?

A. I agree.

Ex. 1041, 32:11-19, 108:1-9,
179:10-15 (Reply (Paper 22), 23).

33

Claim 1: (4) Tessariol Renders Obvious a “Conductive Contact” Under PO’s Incorrect Construction: Dr. Kuhn’s Testimony

- Dr. Kuhn’s testimony about her personal work:

Q. And in that work, did any of it involve a contact pad that did not have something physically, an adjoining structure, making contact with it?

A. Well, in a test chip, the contact pads do not have a conductive structure touching them at the time they are made. They have a conductive structure touching them later on.

Q. And then --

A. Or they may not, if the conductive structure may never touch it. It just happens to be helpful to the layout to have a contact pad in that location.

Ex. 1041, 31:24-32:10 (Reply (Paper 22), 15).

Summary

- Claims 3-4: PO argues that Tessariol does not disclose its dummy source structures being “nominally equal distance” from the staircase contact
 1. PO ignores the specification’s definition of “nominally”;
 2. PO ignores Tessariol’s express disclosure; and
 3. PO misstates the law.

Reply (Paper 22), 24-25.

Claims 3-4: (1) PO Ignores that “Nominal Distance” Refers to a Target Value During Design

- Claims 3 and 4 require that the “dummy source structures” be “nominally equal lateral distances to the staircase contact.”
- The specification makes clear this refers to a target (a desire) during the design phase only:

As used herein, the term “nominal/nominally” refers to a desired, or target, value of a characteristic or parameter for a component or a process operation, set during the design phase of a product or a process, together with a range of values above and/or below the desired value. The range of values can be due to slight variations in manufacturing processes or tolerances. As used herein, the term “about”

872 Patent, 4:9-15 (Reply (Paper 22), 25).

Claims 3-4: (2) Tessariol Discloses Its Design Includes Regular Spacing that Result in Equal Distance Apart

- Tessariol's design includes a uniform pattern with dummy vias an equal distance from the staircase contacts:

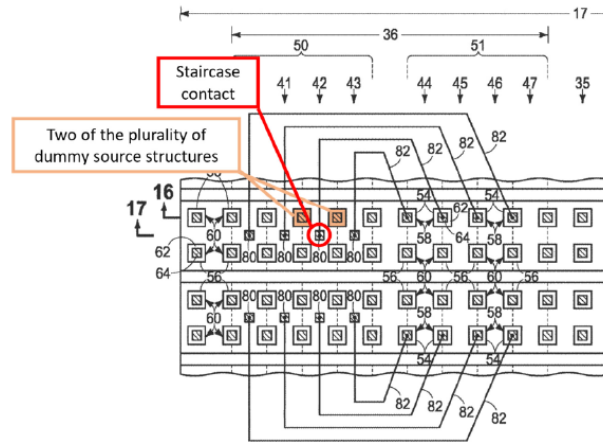


FIG. 15

*Tessariol, Fig. 15 (Petition (Paper 1), 93);
Reply (Paper 22), 25.*

- Tessariol's specification confirms this regular spacing:

relative one another. Openings 54 and 56 are shown as being collectively arrayed in straight-line rows and columns. However, any alternate configuration may be used including, for example, staggering (not shown) alternating openings 54/56 in rows and/or columns.

Tessariol, [0037] (Reply (Paper 22), 25).

Claims 3-4: (3) PO Misstates the Law

- *Hockerson-Halberstadt* holds that it is improper to rely on prior art figures—without more—for “precise proportions” and “particular sizes.” *Hockerson-Halberstadt, Inc. v. Avia Group Int’l*, 222 F.3d 951, 956 (Fed. Cir. 2000).
- Relative dimensions are properly decipherable from figures.

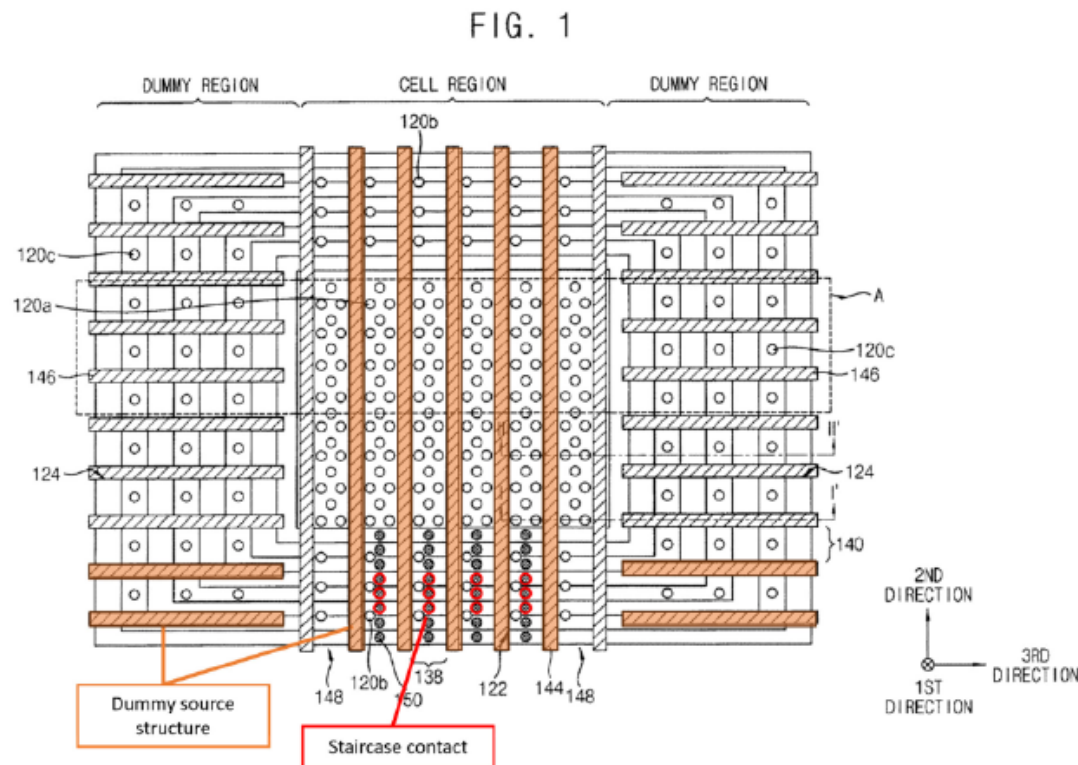
Reply (Paper 22), 24.

Roadmap

1. The 872 IPR Grounds
2. The 872 Patent
3. The Tessariol Ground
 - A. The Petition, Preliminary Response, and Institution Decision
 - B. Claim Construction: “Conductive Contact”
 - C. POR Arguments Fail
4. The Park Ground
 - A. The Petition, Preliminary Response, and Institution Decision
 - B. Claim Construction
 1. “Dummy Source Structure”
 2. “Surrounding”
 - C. POR Arguments Fail

Petition's Showing—"Dummy Source Structures Surrounding the Staircase Contact"

- The Petition demonstrates that two Park common source lines (144) surround a staircase contact:



Park, Fig. 1 (Petition (Paper 1), 59).

Park: POPR's and Preliminary Sur-reply's Argument, and the Board's Institution Decision

- “Dummy source structure”

- The Board did not adopt Micron's construction (“structure that occupies the void that was used for the gate replacement process”). On the preliminary record, it was “not persuaded that the gate replacement process is an essential part of the claimed invention, such that it should be treated as a part of the claimed 3D memory device.”

ID (Paper 15), 12-13.

- The Board preliminarily construed “dummy source structure” to mean “is a structure that does not function as a source to the memory cells.”

ID (Paper 15), 11.

- “Surrounding”: the Board preliminarily construed to “require[] more than structures on two sides of the object.”

ID (Paper 15), 13-16.

- Based on these findings, the Board preliminary found that the Park's common source lines (1) are not “dummy source structures,” because they function as a source, and (2) do not “surround” the staircase contact, because they are on only two sides of it.

ID (Paper 15), 28-30.

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 - A. The Petition, Preliminary Response, and Institution Decision
 - B. Claim Construction
 1. “Dummy Source Structure”
 2. “Surrounding”
 - C. POR Arguments Fail

Claim Construction (Dummy Source Structure): Micron's Construction Is Correct

- Micron's construction: "structure that occupies the void that was used for the gate replacement process."
 1. The 872 Patent does not use the plain and ordinary meaning of "dummy source structure."
 2. The 872 Patent states that the "dummy **source structures**" replace the conventional gate replacement structures to provide the alleged invention's improvements.
 3. The Challenged Claims effectively refer to the gate replacement process, rendering the gate replacement process part of the alleged invention.
 4. There is no meaningful other limitation that would identify a "dummy source structure."

Petition (Paper 1), 24-27; Reply (Paper 22), 2-5.

Claim Construction (Dummy Source Structure): (1) The 872 Patent Does Not Use the Plain and Ordinary Meaning of "Dummy"

- Micron demonstrates that the plain and ordinary meaning of “dummy” refers to an electrically inoperable structure that resembles the non-dummy, electrical operable structure.

Reply (Paper 22), 2-3 (citing Ex. 1037, 5:33-36, 13:57-64, Ex. 1038, 21:7-11; Ex. 1039, 7:1-6; Ex. 1040, 10:7-10; Ex. 1006, [0053], [0068]).

- And Dr. Kuhn agrees “dummy” refers to a structure that resembles its counterpart structure.

Have you ever heard of a dummy source structure before working on this case?

A. I've certainly heard the word, "dummy" applied to numerous semiconductor features. It is not uncommon for the word, "dummy" to sit in front of a semiconductor feature that resembles some important feature, but is missing something. Dummy transistors. Dummy interconnects. Dummy memory regions.

Ex. 1041, 119:15-23 (Reply (Paper 22), 3).

- As that meaning does not apply here, the specification is critical in interpreting “dummy source structure.”

Reply (Paper 22), 3.

Claim Construction (Dummy Source Structure: (2) The Specification Describes that the “Dummy Source Structure” Replaces the Conventional Gate Replacement Structure

- The 872 Patent details alleged problems with the gate replacement process and that the “dummy source structures” allegedly solve these problems.

Problems and Solution

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3 It is noted that references in the specification to “one embodiment,” “an embodiment,” “an example embodiment,” “some embodiments,” etc., indicate that the embodiment described may include a particular feature, structure, or characteristic, but every embodiment may not necessarily include the particular feature, structure, or characteristic. Moreover, such phrases do not necessarily refer to the same embodiment. Further, when a particular feature, structure or characteristic is described in connection with an embodiment, it would be within the knowledge of a person skilled in the pertinent art to affect such feature, structure or characteristic in connection with other embodiments whether or not explicitly described.

4 In general, terminology may be understood at least in part from usage in context. For example, the term “one or more” is as used herein, depending at least in part upon context, may be used to describe any feature, structure, or characteristic in a singular sense or may be used to describe combinations of features, structures or characteristics in a plural sense. Similarly, terms, such as “a,” “an,” or “the,” again, may be understood to convey a singular usage or to convey a plural usage, depending at least in part upon context. In addition, the term “based on” may be understood as not necessarily intended to convey an exclusive set of factors and may, instead, allow for existence of additional factors not necessarily expressly described, again, depending at least in part upon context.

5 It should be readily understood that the meaning of “on,” “above,” and “near” in the present disclosure should be interpreted in the broadest manner such that “on” not only means “directly on” something but also includes the meaning of “on” something with an intermediate feature or a layer therebetween, and that “above” or “over” not only means the meaning of “above” or “over” something but can also include the meaning in “above” or “over” something with an intermediate feature or layer therebetween (i.e., directly on something).

6 Further, spatially relative terms, such as “between,” “below,” “above,” “upper,” and the like, may be used herein for ease of description to describe one element or feature’s relationship to another element(s) or feature(s) as illustrated in the figures. The spatially relative terms are intended to encompass different orientations of the device in use or operation in addition to the orientation depicted in the figures. The apparatus may be otherwise oriented (rotated 90 degrees or at other orientations) and the spatially relative descriptions used herein may likewise be interpreted accordingly.

7 As used herein, the term “substrate” refers to a material onto which subsequent material layers are added. The substrate itself can be patterned. Materials added on top of the substrate can be patterned or can remain unpatterned. Furthermore, the substrate can include a wide array of semiconductor materials, such as silicon, germanium, gallium arsenide, indium phosphide, etc. Alternatively, the substrate is undecisively high resistance. Also, because dummy channel holes can be made from an electrically non-conductive material, such as a glass, a plastic, or a ceramic.

8 As used herein, the term “layer” refers to a material portion including a region with a thickness. A layer can extend over the entirety of an underlying or overlying structure or may have an extent less than the extent of an underlying or overlying structure. Further, a layer can be a region of a homogeneous or inhomogeneous continuous structure that has a thickness less than the thickness of the entire structure. For example, a layer can be located between any pair of horizontal planes between, or at a top surface and a bottom surface of the continuous structure. A layer can extend horizontally, vertically, and/or along a topmost surface. A substrate can be a layer, can include one or more layers therein, and/or can have one or more layers thereupon, therebelow, and/or therebetween. A layer can include multiple layers. For example, an intermediate layer can include one or more conductive and contact layers (in which conductive material and/or vias or contacts are formed) and one or more dielectric layers.

9 As used herein, the term “normal/usually” refers to a desired, or a process operation, set during the design phase of a product or a process, together with a range of values above and/or below the desired value. The range of values can be due to slight variations in manufacturing processes or tolerances. As used herein, the term “about” indicates the value of a given quantity that can vary based on a particular technology used associated with the subject semiconductor device. Based on the particular technology used, the term “about” can indicate a value of a given quantity that varies within, for example, 10-90% of the value (e.g., ±10%, ±20%, or ±30% of the value).

10 As used herein, the term “3D memory device” refers to a semiconductor device with vertically oriented strings of memory cell transistors (referred to herein as “memory strings”), such as NAND memory strings on a laterally oriented substrate so that the memory strings extend in the vertical direction with respect to the substrate. As used herein, the term “vertical/vertically” means nominally perpendicular to the lateral surface of a substrate.

11 In 3D memory fabrication processes, a gate-replacement process is performed to form interwoven word lines/dielectric stacks, in which sacrificial layers are replaced with conductive layers to form gate electrodes/word lines. Dummy channel structures (e.g., formed by filling dummy channel holes with dielectric materials) can be used in staircase structures of a 3D memory device to prevent oxide layer bending. As 3D memory devices continue to scale down, the gate-replacement process can become more challenging. For example, in some 3D memory devices such as charge trap 3D NAND memory devices, gate line dies (GLDs) are formed to divide an array of memory strings (e.g., in the lateral region of a 3D memory device) and/or dummy channel structures (e.g., in the staircase region of the 3D memory device) into different memory regions. Often, a GLD has large dimensions and is filled with an insulation structure formed in a trench that extends laterally in the array. The gate-replacement process in such a 3D memory device often includes etching away the sacrificial layers and depositing a conductive material through the trench. Using GLDs to perform the gate-replacement process has drawbacks. For example, in the staircase region, the large lateral distance between adjacent GLDs can cause conductive material to be unintentionally filled in the lateral recesses for removal of the sacrificial layers, resulting in voids in the formed gate electrodes. The gate electrode is undecisively high resistance. Also, because dummy channel holes are formed between adjacent GLDs, the boundary conditions for the etching of dummy channel holes at different locations can be different due to the existence of large-size GLDs, causing dummy channel holes to have nonuniform lateral dimensions. For example, the lateral dimensions of a dummy channel hole may gradually vary as the dummy channel hole moves farther away from the GLDs, causing potential performance variations of the channel holes. In addition, the large areas occupied by the GLDs limit the usable space on the wafer surface to place other components, such as staircase contacts.

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5 For example, FIG. 5 illustrates a plan view of an exemplary 3D memory device 500 having GLDs 504. 3D memory device 500 includes an array of NAND memory strings 502 in an inner region 510, an array of dummy channel structures 506 in a staircase region 520, and multiple parallel GLDs 504, which divide arrays of NAND memory strings 502 and dummy channel structures 506 into different memory regions (e.g., memory string fingers or blocks). As shown in FIG. 5, each GLD 504 extends laterally along the word line direction in a straight-line pattern in the plan view (parallel to the wafer plane). It is noted that x and y axes are included in FIG. 5 to illustrate two orthogonal directions in the wafer plane. The x-direction is the word line direction, and the y-direction is the bit line direction. 3D memory device 500 also includes staircase contacts 508 for forming word line contacts in the staircase region.

6 holes may further result in channel holes with more uniform diameters. Meanwhile, the number of dummy channel holes formed in the staircase region can be flexibly diminished, e.g., based on design and/or fabrication requirements.

7 FIGS. 1A-1C illustrate plan views of exemplary 3D memory devices, according to some embodiments. FIG. 1D illustrates a cross-sectional view of the 3D memory device shown in FIG. 1A. FIGS. 1A-1D illustrate various stages of an exemplary fabrication process, according to some embodiments. FIGS. 3 and 4 each illustrate an exemplary method to form a 3D memory device, according to some embodiments.

8 FIG. 1A illustrates a plan view of an exemplary 3D memory device 100. 3D memory device 100 may include a memory region 106. Memory region 106 may include an inner region 116 (also known as a “core array region”) and an outer region 118 (also known as a “staircase region”). In some embodiments, inner region 116 is the center region of memory region 106 where an array of memory strings 104 (e.g., NAND memory strings) are formed, and outer region 118 is the remaining region of memory region 106 surrounding inner region 116 (including the sides and edges) without memory strings 104.

9 Memory strings 104 may be arranged in an array in inner region 116. Memory strings 104 may be arranged in any suitable pattern, depending on the fabrication and/or design requirements, any suitable number of memory strings 104 may be formed in inner region 116.

10 Staircase region 118 may include a plurality of staircase contacts 122, a plurality of dummy channel structures 124, and a plurality of dummy source structures 126 distributed among dummy channel structures 124 and staircase contacts 122. Staircase contacts 122, dummy channel structures 124, and/or dummy source structures 126 may be arranged in any suitable pattern, such as an array, in staircase region 118. As shown in FIG. 1A, multiple dummy source structures, such as the four dummy source structures indicated by a diamond shape 146, may surround a staircase contact, such as staircase contact 122. The four dummy source structures indicated by 146 may be located adjacent to staircase contact 122 (e.g., there is no other components such as dummy channel structures, dummy source structures, and staircase contacts between staircase contact 122 and each of the four dummy source structures). The four dummy source structures indicated by 146 may be spaced with nonuniformly equal lateral distances to staircase contact 122. In other words, the four dummy source structures indicated by 146 may be evenly or uniformly distributed around staircase contact 122.

11 As shown in FIG. 1A, at least two dummy source structures 146 may surround a staircase contact. The four dummy channel holes indicated by 146 may be arranged in a second row 124 that extends along a second lateral direction (e.g., y-direction) that is perpendicular to the first lateral direction (e.g., x-direction). For example, row 124 includes two dummy source structures, such as the two dummy source structures indicated by 146, which can be formed by the same process that forms the dummy channel holes, so the formation of the dummy source holes has minimal impact on the lateral uniformity of lateral distances to the staircase contact, as shown in FIG. 1A. In other words, the dummy channel structures surrounding a staircase contact may be evenly distributed around the staircase contact.

12 Also, the arrangement of the dummy source structures may allow the gate electrodes/word lines to be formed with improved uniformity and quality, reducing the possibility of the gate electrodes/word lines being formed with defects. For example, the gate-replacement process can be performed to deposit a conductive material through the dummy source holes that subsequently form the dummy source structures. Because the conductive material travels shorter distance to fill up the lateral recesses for forming the gate electrodes, the gate electrodes are less susceptible to voids or density nonuniformity.

13 In the present disclosure, the dummy source holes, which can have the same diameter as the dummy channel holes, can be formed by the same process that forms the dummy channel holes, so the formation of the dummy source holes has minimal impact on the lateral uniformity of lateral distances to the staircase contact. Further, both the dummy channel holes and the dummy source holes in the staircase region can be formed by the same process that forms the channel holes in the inner region. The etching process to form the channel

Various embodiments in accordance with the present disclosure provide an improved 3D memory structure scheme suitable for solving the aforementioned issues by replacing the GLSs with dummy source structures. The 3D

872 Patent, 5:31-34 (Reply (Paper 22), 4).

872 Patent, 4:30-5:58 (Reply (Paper 22), 4).

Claim Construction (Dummy Source Structure): (3) The Claims Effectively Recite the Gate Replacement Process

- The 872 Patent uses “conductive layers” in reference to the gate replacement process and problems therewith.

In 3D memory fabrication processes, a gate-replacement process is often used to form interleaved word line/dielectric stacks, in which sacrificial layers are replaced with conductive layers to form gate electrodes/word lines. Dummy

872 Patent, 4:30-33 (Reply (Paper 22), 4).

- The claims refer to these “conductive layers.”

1. A three-dimensional (3D) memory device, comprising:
a substrate;
a memory stack comprising interleaved conductive layers
and dielectric layers on the substrate;

872 Patent, Claim 1 (partial) (Reply (Paper 22), 4).

Claim Construction (Dummy Source Structure): (4) No Meaningful Other Limitations to Identify a “Dummy Source Structure”

- The specification does not limit the structure of “dummy source structure” in any other meaningful way.
 - The specification embraces “[d]ifferent layouts, patterns, and designs” (872 Patent, 8:51-53);
 - The dummy source structures may or may not be made using the same process as dummy channel holes (*id.*, 13:3-5);
 - The dummy source structures may or may not be the same size as dummy channel holes (*id.*, 8:11-19);
 - The dummy source structures may or may not assume the same shape as a gate line slit (*id.*, 11:44-46); and
 - The dummy source structure may even be an operable structure (*id.*, 5:41-43, 16:63-66).

Petition (Paper 1), 26-27.

Claim Construction (Dummy Source Structure): PO's Arguments Fail

- PO advances four arguments that lack merit:
 1. Micron does not read “dummy” out of the term;
 2. Micron does not read a method step into the apparatus claims;
 3. PO's “for example” specification citations do not support its position; and
 4. Micron's construction does not limit “dummy source structure” to a particular embodiment.

Reply (Paper 22), 5-7.

Claim Construction (Dummy Source Structure): (1) Micron Does Not Read “Dummy” Out of the Term

- The specification states that the “dummy source structure” may function as a source.

Reply (Paper 22), 5.

- “Connect” is an electrical connection.

structures may also be formed. Source structures formed in the inner region may be connected with surround channel structures (e.g., channel structure 220 of memory string 218 shown in FIG. 2E) via a common source, such as a doped region (not shown) in substrate 202. In some embodiments, dummy source structure 246 may not connect to channel structures in the inner region. Instead, dummy source structure 246 may be formed simultaneously with source structures in the inner region, while functioning as a mechanical supporting structure after gate-replacement process, without connecting to channel structures in the inner region. In some

872 Patent, 16:34-44; Reply (Paper 22), 9.

- By stating that a dummy source structure may not function as a source in some embodiments, “[i]t follows that [in] other embodiments,” the dummy source structure may function as a source.

*Guardant Health, Inc. v. Vidal, No. 2021-1104, 2023 WL 3262962, at *2 (Fed. Cir. May 5, 2023) (nonprecedential) (Reply (Paper 22), 9).*

Claim Construction (Dummy Source Structure): (2) Micron Does Not Import a Method Step into an Apparatus Claim that Gate Replacement Is Optional

- Micron’s construction: “structure that occupies the void that was used for the gate replacement process.”

Petition (Paper 1), 24.

- Nothing about this construction requires a method step. Instead, regardless of how they are formed, they are limited by their location.

Reply (Paper 22), 5-6.

Claim Construction (Dummy Source Structure): (3) PO's Specification Citations Do Not Support its Position that Gate Replacement Is Optional

- The entire second paragraph, which includes the “for example,” refers back to the first paragraph that discusses replacing GLSs with dummy source structures.
- The “for example” sentence merely states that the gate line replacement process may form the conductive core of the dummy source structures.
- Indeed, the dummy source structures may include a dielectric core (872 Patent, 16:56-58).

872 Patent, 5:31-58 (Reply (Paper 22), 6).

Various embodiments in accordance with the present disclosure provide an improved 3D memory structure scheme suitable for solving the aforementioned issues by replacing the GLSs with dummy source structures. The 3D memory structure includes a plurality of dummy source structures distributed in the array of dummy channel structures and/or staircase contacts in the staircase region. Each dummy source structure may include an insulating spacer layer in a dummy source hole and a conductive contact within the spacer layer. In some embodiments, one or more dummy source structures are in contact with the substrate and may provide interconnect between the 3D memory device and peripheral devices. The dummy source structures may be arranged in a pattern, e.g., an array, so the dummy source structures can be uniformly distributed in the staircase structure. The arrangement of the dummy source structures may improve the uniformity and stability for etching dummy channel holes in the staircase region.

Also, the arrangement of the dummy source structures may allow the gate electrodes/word lines to be formed with improved uniformity and quality, reducing the resistivity of the gate electrodes/word lines. For example, the gate-replacement process can be performed to deposit a conductive material through the dummy source holes that subsequently form the dummy source structures. Because the conductive material travels shorter distances to fill up the lateral recesses for forming the gate electrodes, the gate electrodes are less susceptible to voids or density nonuniformity.

Claim Construction (Dummy Source Structure): (3) PO's Specification Citations Do Not Support its Position

- 4:30-33 describes the gate-replacement process and creating the “conductive layers” of the claims with it.
- 16:40-49 discusses various options to fill the dummy source hole after carrying out the gate-replacement process.

In 3D memory fabrication processes, a gate-replacement process is often used to form interleaved word line/dielectric stacks, in which sacrificial layers are replaced with conductive layers to form gate electrodes/word lines. Dummy

872 Patent, 4:30-33 (Reply (Paper 22), 7).

structures in the inner region. Instead, dummy source structure 246 may be formed simultaneously with source structures in the inner region, while functioning as a mechanical supporting structure after gate-replacement process, without connecting to channel structures in the inner region. In some embodiments, dummy source structure 246 may not reach substrate 202. For example, dummy source structure 246 may be above substrate 202 while still reach the lower part of the dielectric stack to carry out the gate-replacement process.

872 Patent, 16:40-49 (Reply (Paper 22), 7).

Claim Construction (Dummy Source Structure): (4) Micron's Construction Does Not Read Out Embodiments

- Micron's construction: "structure that occupies the void that was used for the gate replacement process."

Petition (Paper 1), 24.

- Micron's constructions embraces, for example, both a conductive core and a dielectric core.

Reply (Paper 22), 7.

Claim Construction (Dummy Source Structure): PO's Negative Limitation—"Does Not Function as a Source"—Is Legally Erroneous

- PO argues that “dummy source structure” should be construed “as a structure that does not function as a source to memory cells.”

POR (Paper 18), 14.

- This argument fails for two reasons:
 1. The specification explains only that “in some embodiments,” a “dummy source structure” does not function as a source to memory cells; and
 2. The specification does not support grafting a negative limitation onto “dummy source structure.”

Reply (Paper 22), 7-10.

Claim Construction (Dummy Source Structure): PO's Negative Limitation Contradicts the Specification

- The specification says that “source structures” “may” function as sources to memory cells.
- And “in some embodiments,” “dummy source structures” “may not.” “Instead,” they may perform another function.
 - By stating that a dummy source structure may not function as a source in some embodiments, “[i]t follows that [in] other embodiments,” the dummy source structure may function as a source.

Guardant Health, Inc. v. Vidal, No. 2021-1104, 2023 WL 3262962, at *2 (Fed. Cir. May 5, 2023) (Reply (Paper 22), 9).

structures may also be formed. Source structures formed in the inner region may be connected with surround channel structures (e.g., channel structure 220 of memory string 218 shown in FIG. 2E) via a common source, such as a doped region (not shown) in substrate 202. In some embodiments, dummy source structure 246 may not connect to channel structures in the inner region. Instead, dummy source structure 246 may be formed simultaneously with source structures in the inner region, while functioning as a mechanical supporting structure after gate-replacement process, without connecting to channel structures in the inner region. In some

872 Patent, 16:34-44; Reply (Paper 22), 7-10.

Claim Construction (Dummy Source Structure): PO's Negative Limitation Contradicts the Specification

- While PO now concedes that this passage means that dummy source structures may “connect” to the channel structures, it argues that it does not suggest such structures may “function as a source to memory cells.”

POR (Paper 18), 17; Reply (Paper 22), 9; Sur-reply (Paper 24), 4.

- PO's argument tortures the structure of the passage.

structures may also be formed. Source structures formed in the inner region may be connected with surround channel structures (e.g., channel structure 220 of memory string 218 shown in FIG. 2E) via a common source, such as a doped region (not shown) in substrate 202. In some embodiments, dummy source structure 246 may not connect to channel structures in the inner region. Instead, dummy source structure 246 may be formed simultaneously with source structures in the inner region, while functioning as a mechanical supporting structure after gate-replacement process, without connecting to channel structures in the inner region. In some

872 Patent, 16:34-44; Reply (Paper 22), 9.

- PO's argument renders “connect” meaningless.

Reply (Paper 22), 9.

Claim Construction (Dummy Source Structure): PO's Negative Limitation Has No Legal Basis in the Specification

- The Federal Circuit has explained that negative limitations are only appropriate if they are apparent from “the words of the claim” or through an “express disclaimer or independent lexicography” *Ethicon LLC v. Intuitive Surgical, Inc.*, 847. F. App'x 901, 907 (Fed. Cir. 2021) (*Reply (Paper 22)*, 10).
- It is not apparent from claim language, because the specification does not use the plain and ordinary meaning of “dummy” (*see supra*).
- There is no express disclaimer or independent lexicography.

structures may also be formed. Source structures formed in the inner region may be connected with surround channel structures (e.g., channel structure 220 of memory string 218 shown in FIG. 2E) via a common source, such as a doped region (not shown) in substrate 202. In some embodiments, dummy source structure 246 may not connect to channel structures in the inner region. Instead, dummy source structure 246 may be formed simultaneously with source structures in the inner region, while functioning as a mechanical supporting structure after gate-replacement process, without connecting to channel structures in the inner region. In some

872 Patent, 16:34-44; Reply (Paper 22), 9.

Roadmap

1. The 872 IPR Grounds
2. The 872 Patent
3. The Tessariol Ground
 - A. The Petition, Preliminary Response, and Institution Decision
 - B. Claim Construction: “Conductive Contact”
 - C. POR Arguments Fail
4. The Park Ground
 - A. The Petition, Preliminary Response, and Institution Decision
 - B. Claim Construction
 1. “Dummy Source Structure”
 2. “Surrounding”
 - C. POR Arguments Fail

Claim Construction (Surrounding): The Relevant Issue Is When Laterally-Extending Dummy Source Structures “Surround” a Staircase Contact

- There can be no reasonable dispute that the 872 Patent describes that “dummy source structures,” just like gate-line slits (GLSs), can be laterally-extending structures.

GLSs

gate-replacement process can become more challenging. For example, in some 3D memory devices such as charge trap 3D NAND memory devices, gate line slits (GLSs) are formed to divide an array of memory strings (e.g., in the inner region of a 3D memory device) and/or dummy channel structures (e.g., in the staircase region of the 3D memory device) into different memory regions. Often, a GLS has

Dummy Source Structures

As a result, dummy source structures 178 can laterally separate 3D memory device 100 into multiple memory regions, such as memory blocks. In some embodiments,

872 Patent, 4:38-44, 11:44-46 (Petition (Paper 1), 26-27) (Reply (Paper 22), 10).

Claim Construction (Surrounding): The Relevant Issue Is When Laterally-Extending Dummy Source Structures “Surround” a Staircase Contact

- There can be no reasonable dispute that four structures are not necessary to “surround” an object.

872 Patent

more or less than two dummy channel structures. In some embodiments, the number of dummy source structures surrounding one or more dummy channel structure 124 may be more or less than eight, six, or four. The lateral dimensions

872 Patent, 8:8-11 (Petition (Paper 1), 28).

Claim Construction (Surrounding): PO's Expert, Dr. Kuhn, Simply Did Not Consider When Such Laterally-Extending Structures "Surround" an Object

- Dr. Kuhn's testimony:

Q. "-- the applicant cited to a section of the specification and additionally states that the claimed 'dummy source structure,' can function to laterally separate the 3D device into multiple memory regions."

A. I see that.

Q. So what would the shape of a dummy source structure be in this case?

A. I haven't thought about this. The use of the dummy source structure to laterally separate the 3D memory device in multiple memory regions is not something I have spent any time thinking through.

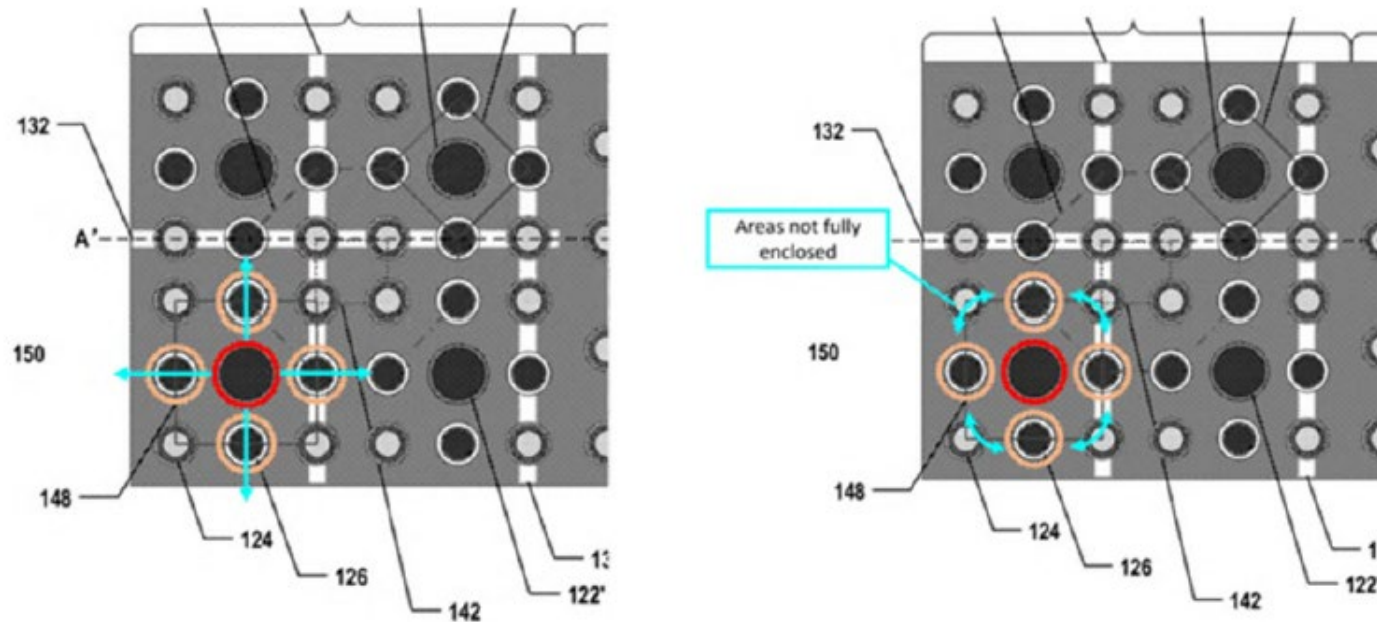
Q. I mean, in view of this, do you think that a dummy source structure has to be cylindrical?

A. Again, I have not thought through this specific question of laterally separating the 3D memory devices using the dummy source structure.

Ex. 1041, 114:1-17 (Reply (Paper 22), 13).

Claim Construction (Surrounding): The Petition Demonstrates That “Surrounding” Must Be Met in Two Cases

- Surrounding must be met in two cases: (1) when four lines are drawn radially from the staircase contact, they intersect with a dummy source structure or (2) when the extent of the enclosed border around the staircase contact is greater than shown in the '872 embodiments.



872 Patent, Fig. 1A (Petition (Paper 1), 30-31).

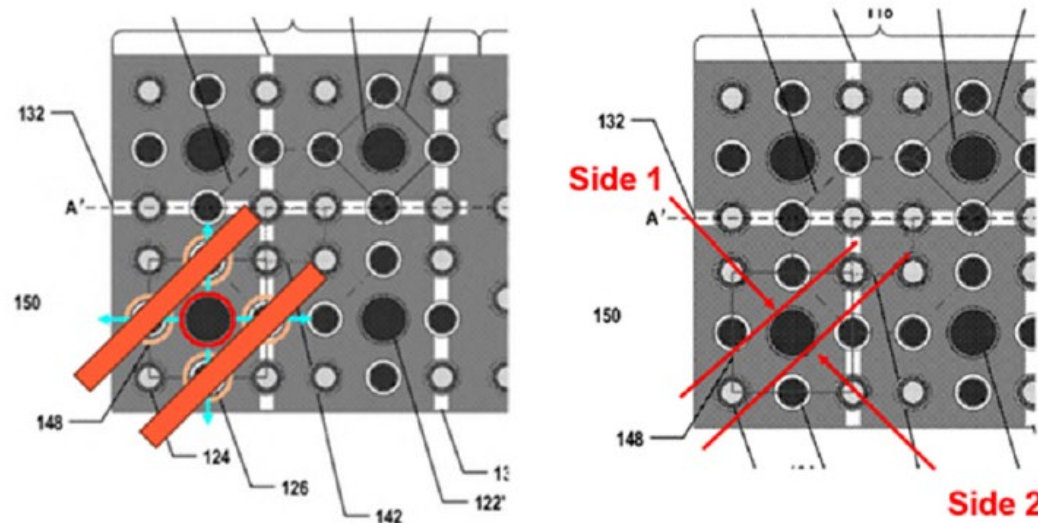
Claim Construction (Surrounding): Summary—PO's Arguments Fail

- Each of PO's arguments that two structures cannot "surround" fails.
 1. Two structures can "surround" an object to the same extent as four structure can "surround" that same object; and
 2. The specification's use of "between" does not mean that two objects cannot "surround" a structure.

Reply (Paper 22), 11-14.

Claim Construction (Surrounding): (1) Two Structures Can “Surround” to a Greater Degree as Four Structures

- As shown below using orange bars, if the dummy source structures were to become laterally wider (see 872 Patent, 8:8-11, 11:44-46) in the express embodiment, one could characterize the dummy source structures as surrounding the contact only on two sides.
- Yet these two dummy source structures surround the staircase contact to a greater degree than the four dummy source structures.



872 Patent, Fig. 1A (Reply (Paper 22), 11-12).

Claim Construction (Surrounding): (1) Two Structures Can “Surround” to a Greater Degree as Four Structures

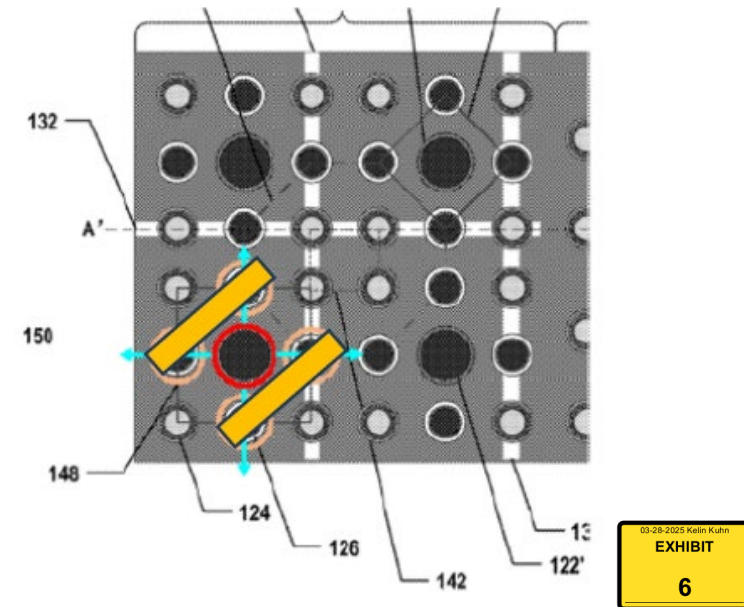
- PO's expert, Dr. Kuhn, admits that two structures can surround more of the contact border than four dummy source structures.

Q. Do you agree that the two dummy source structures shown in Figure 6 -- Exhibit 6 enclose more of the border of the word line contact than in the version with four dummy source structures?

ATTORNEY BONNY: Objection. Form.

THE WITNESS: So, if we -- let me start out by saying that there is no place in the '872 Patent where area, subtended angle, mathematical relationships, is ever discussed.

So yes, your drawing has those lines longer than the individual diameters of the source regions. But that's never used in the patent anywhere, to clarify language around "surround" versus "between."



Exs. 1041, 144:24-145:12 (Reply (Paper 22), 11).

Claim Construction (Surrounding): (1) “Surround” Does Not Require a Certain Number of Objects

- The specification does not define surrounding by the number of objects:

dummy source structures indicated by a diamond 149. Any suitable number of dummy channel structures may be surrounded by any suitable number of dummy source structures.

more or less than two dummy channel structures. In some embodiments, the number of dummy source structures surrounding one or more dummy channel structure 124 may be more or less than eight, six, or four. The lateral dimensions

872 Patent, 7:40-43, 8:8-11 (Petition (Paper 1), 28, 31).

- Yet PO in Sur-reply:

32. But, as explained in the POR, the distinction the '872 is making is not one of degree or extent (i.e., the amount to which something is encircled) but the number of structures around the object. POR 25-27.³ As Dr. Kuhn testified, “nowhere in

Sur-reply (Paper 24), 9-10.

Claim Construction (Surrounding): (1) Extrinsic Evidence Demonstrates That Two Structures Can “Surround” an Object

- PO’s expert, Dr. Kuhn, admits she may have “misread” Micron’s extrinsic evidence that two structures can “surround” an object.

In other words, the conventional SBPI operations are strongly affected by the stored Vts of two surrounding NAND cells dispersed in the adjacent left and right BIs.

Q. You characterized a quote by saying:

"This passage is merely referring to the effects of NAND cells in the surroundings."

When you say "effects of NAND cells," are you referring to more than two cells?

A. So when I initially read this, I read this as this language describing the two surrounding NAND cell, but also, incorporating other cells in the surroundings.

Q. Okay. --

A. Now, I may have misread that, but that was my read of it the first time I read that patent.

Ex. 1019, 2:14-16; Ex. 1041, 153:15-154:1 (Reply (Paper 22), 13-14).

Claim Construction (Surrounding): (2) The Specification's Use of "Between" Is Not Inconsistent with the Fact That Two Structures Can Surround an Object

- The specification uses "between" to refer to the fact that "dummy channel holes" are between the GLSs.
- This does not address whether the GLSs "surround" the "dummy channel holes."

undesirably high resistance. Also, because dummy channel holes are formed between adjacent GLSs, the boundary conditions for the etching of dummy channel holes at different locations can be different due to the existence of large-area GLSs, causing dummy channel holes to have nonuniform lateral dimensions. For example, the lateral

872 Patent, 4:56-61 (Reply (Paper 22), 12).

Roadmap

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Claim 1 (“Dummy Source Structures”): PO’s Arguments Fail

- PO’s argument entirely relies on its construction that a “dummy source structure” is a structure that does not “function as a source to the memory cells.”

POR (Paper 18), 46.

- The Board should reject grafting this negative limitation onto “dummy source structure.”

Reply (Paper 22), 26-27.

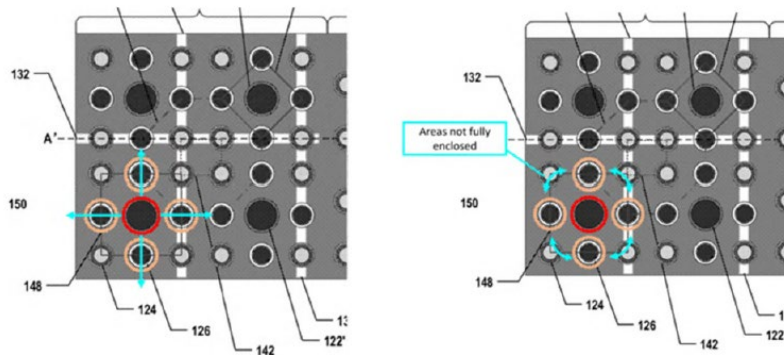
Claim 1 (“Surrounding”): PO Relies on Its Legally Erroneous Claim Construction

- PO’s argument entirely relies on its construction that “surround[]” cannot be met by Park’s two, laterally-extending common source line structures (POR, 40-42).

Reply (Paper 22), 26.

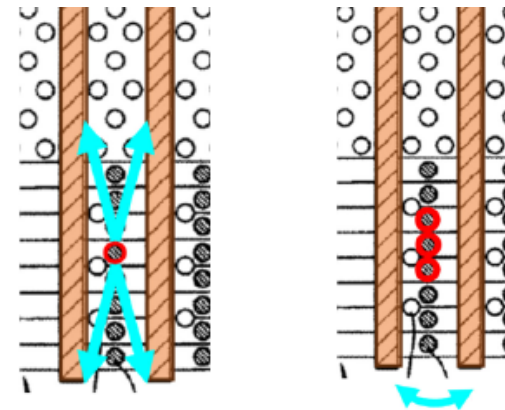
- Park’s common source lines, however, “surround” the staircase contact to a greater degree than the 872 Patent.

872 Patent



872 Patent, Fig. 1A (Petition (Paper 1), 30-31).

Park



Park, Fig. 1 (Petition (Paper 1), 60-61).

Claim 1 (“Surrounding”): PO’s GLS Argument Fails

- PO argues that Park’s common source lines cannot “surround” because they are similar to prior art GLSs (POR, 42-44). This argument fails for two reasons.
- The 872 Patent states that dummy source structures may be laterally-extending structures.

As a result, dummy source structures 178 can laterally separate 3D memory device 100 into multiple memory regions, such as memory blocks. In some embodiments,

872 Patent, 11:44-46 (Petition (Paper 1), 26) (Reply (Paper 22), 26).

- The shape of the dummy source structures was not the reason for allowance—the additional requirement of a “conductive contact” was the reason.

872 Patent, 4:38-44 (Petition (Paper 1), 21-22) (Reply (Paper 22), 26).

Summary

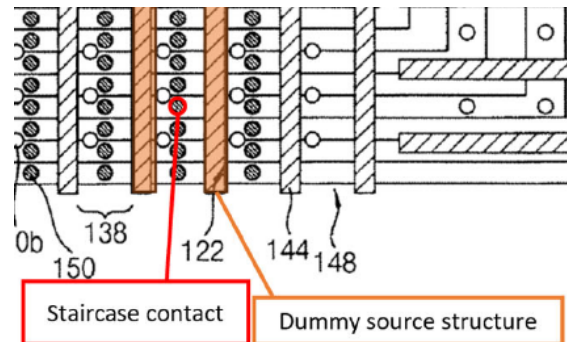
- Claims 3-4: PO argues that Park does not disclose its dummy source structures being “nominally equal lateral distance” from the staircase contact (POR, 48-49).
 1. PO ignores the specification’s definition of “nominally” (*see supra*);
 2. PO ignores Park’s express disclosure; and
 3. PO misstates the law (*see supra*).
- Claim 6: PO argues that Park’s common source lines cannot be in a row, because they extend through the cell region (POR, 52). This argument fails, because PO does not dispute Micron’s definition of a “row.”

Reply (Paper 22), 27-28.

Claims 3-4: (2) Park Discloses Its Figures Illustrate Its Design, and These Figure Illustrate Equal Distance Spacing

- Park discloses that its figures illustrate its design, which is precisely what claims 3-4's “nominally equal distance requirement” requires.

Example embodiments are described herein with reference to cross-sectional illustrations that are **schematic illustrations** of idealized example embodiments (and intermediate structures). As such, **variations from the shapes of the illustrations as a result, for example, of manufacturing techniques and/or tolerances**, are to be expected. Thus,



Park, 4:65-5:3, Fig. 1 (Reply (Paper 22), 27); (Petition (Paper 1), 67).

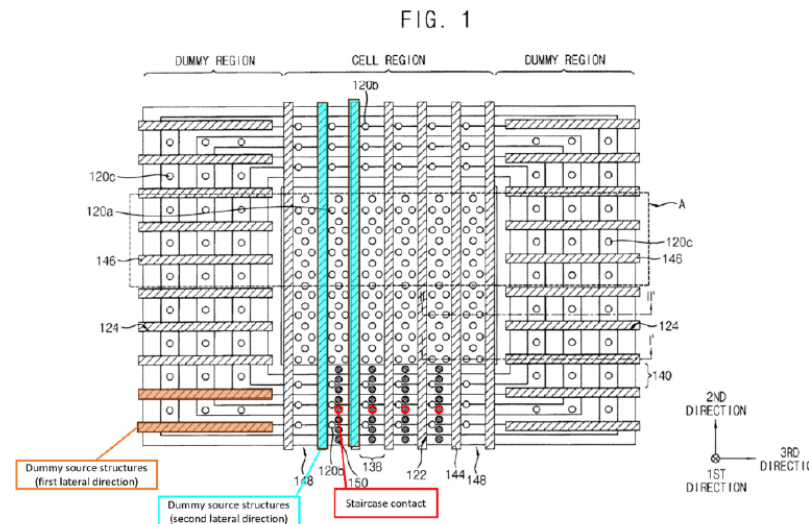
Claim 6: Park Discloses a “Row” from East to West

- Park discloses a row from east to west. That the structures resemble match sticks has no bearing on whether this is a “row.”

Note that a row is “a number of objects arranged in a usually straight line.”
(<https://www.merriam-webster.com/dictionary/row>). The above row is like a row

Petition (Paper 1), 69.

- The common source lines (teal blue) are in a row from east to west.



Park, Fig. 1; (Petition (Paper 1), 71).

