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Paper 37
Date: October 23, 2025

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner,

v.

YANGTZE MEMORY TECHONOLOGIES COMPANY, LTD.,
Patent Owner.

IPR2024-00789
Patent 10,861,872 B2

Before JO-ANNE M. KOKOSKI, KIMBERLY McGRAW, and MICHAEL T. CYGAN, *Administrative Patent Judges.*

KOKOSKI, *Administrative Patent Judge*.

JUDGMENT
Final Written Decision
Determining All Challenged Claims Unpatentable
35 U.S.C. § 318(a)

I. INTRODUCTION

We have jurisdiction to conduct this *inter partes* review under 35 U.S.C. § 6, and issue this Final Written Decision pursuant to 35 U.S.C. § 318(a). For the reasons that follow, we determine that Micron Technology, Inc. ("Petitioner") shows by a preponderance of the evidence that claims 1–6 and 11–13 (the "challenged claims") of U.S. Patent No. 10,861,872 B2 ("the '872 patent," Ex. 1001) are unpatentable.

A. Procedural Background

Petitioner filed a Petition to institute an *inter partes* review of claims 1–6 and 11–13 of the '872 patent. Paper 1 ("Pet."). Yangtze Memory Technologies Company, Ltd. ("Patent Owner") filed a Preliminary Response. Paper 11. With Board authorization (Paper 12), Petitioner filed a Preliminary Reply (Paper 13), and Patent Owner filed a Preliminary Sur-reply (Paper 14), to the Preliminary Response.

Pursuant to 35 U.S.C. § 314(a), we instituted an *inter partes* review of claims 1–6 and 11–13 on the grounds advanced in the Petition. Paper 15 ("Institution Decision" or "Dec."). After institution of trial, Patent Owner filed a Patent Owner Response ("PO Resp.," Paper 18), Petitioner filed a Reply ("Pet. Reply," Paper 22), and Patent Owner filed a Sur-reply ("PO Sur-reply," Paper 24).

We held an oral hearing on July 29, 2025, and a transcript is included in the record. Paper 36 ("Tr.").

B. Real Parties in Interest

Petitioner identifies "Micron Technology Inc. and its subsidiaries, including Micron Consumer Products Group LLC" as the real parties in interest. Pet. 7. Patent Owner identifies itself as the real party in interest. Paper 5 (Mandatory Notice), 2.

C. Related Matters

The parties indicate that the ’872 patent is asserted in *Yangtze Memory Techs. Co., Ltd. v. Micron Tech. Inc.*, Case No. 3:23-cv-05792-RFL (N.D. Cal.). Pet. 7; Paper 5, 2.

D. The ’872 Patent

The ’872 patent relates “to three-dimensional (3D) memory devices” that include “a substrate, a memory stack including interleaved conductive layers and dielectric layers on the substrate, and a staircase structure on one side of the memory stack” with a plurality of dummy source structures vertically extending through the staircase structure that surround the staircase contact. Ex. 1001, 1:15–17, 1:35–43.

Figure 1A is reproduced below.

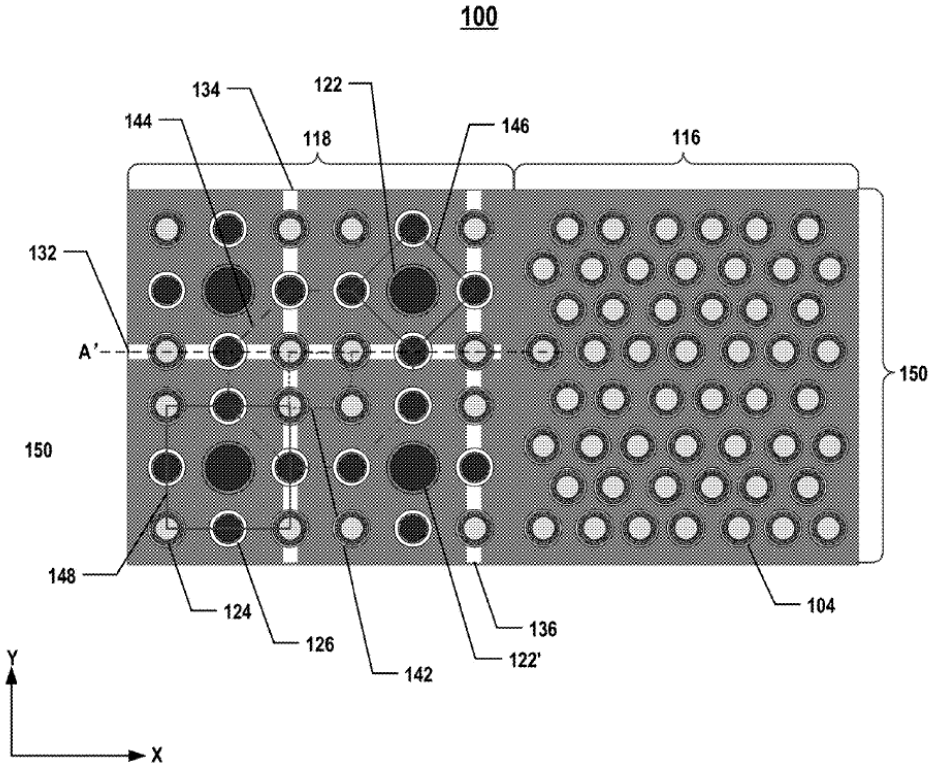

FIG. 1A

Figure 1A illustrates a plan view of a 3D memory device described in the ’872 patent. Ex. 1001, 2:38–40. Memory device 100 includes memory region 150, which further includes inner region 116 (the “core array region”), and outer region 118 (the “staircase region”). *Id*. at 6:15–19. Staircase region 118 includes staircase contacts 122, plurality of dummy channel structures 124, and plurality of dummy source structures 126 distributed among dummy channel structures 124 and staircase contacts 122. *Id*. at 6:31–35. Staircase contacts 122, dummy channel structures 124, and/or dummy source structures 126 may be arranged in any suitable pattern, such as the dummy source structures indicated by diamond shape 146 that surrounds staircase contact 122. *Id*. at 6:35–41. At least two dummy source structures may be arranged in each of first row 132 that extends along a first lateral direction (x direction), second row 134 that extends in a second lateral direction (y direction) perpendicular to the first lateral direction, and third row 136 that extends in a third lateral direction in parallel with the first or the second lateral direction. *Id*. at 6:51–58, 7:1–4.

The ’872 patent teaches that the four dummy structures comprising diamond shape 146 “may be located adjacent to staircase contact 122” such that “there is no other components such as dummy channel structures, dummy source structures, and staircase contacts between staircase contact 122 and each of the four dummy source structures.” Ex. 1001, 6:43–46. Also, the four dummy source structures “may be spaced with nominally equal lateral distances to staircase contact 122.” *Id*. at 6:47–48.

E. Illustrative Claim

Petitioner challenges claims 1–6 and 11–13 of the ’872 patent. Claim 1, the only independent claim challenged, is illustrative of the claimed subject matter and is reproduced below.

1. [1.PRE] A three-dimensional (3D) memory device, comprising:

[1.A] a substrate;

[1.B] a memory stack comprising interleaved conductive layers and dielectric layers on the substrate;

[1.C] a staircase structure on one side of the memory stack;

[1.D] a staircase contact in the staircase structure; and

[1.E] a plurality of dummy source structures each extending vertically through the staircase structure, the plurality of dummy source structures surrounding the staircase contact,

[1.F] wherein each of the dummy source structures comprises a conductive contact.

Ex. 1001, 20:5–16 (bracketed material added).

F. Asserted Grounds

Petitioner asserts that claims 1–6 and 11–13 would have been unpatentable on the following grounds:

Claim(s) Challenged	35 U.S.C. §	Reference(s)/Basis
1–6, 11–13	103[1]	Tessariol[2]
1–6, 11, 13	103	Park[3]

Pet. 8. Petitioner relies on the Declarations of Sanjay Banerjee, Ph.D. (Ex. 1003; Ex. 1035). Patent Owner relies on the Declarations of Kelin Kuhn, Ph.D. (Ex. 2001; Ex. 2007).

[1] The Leahy-Smith America Invents Act ("AIA"), Pub. L. No. 112–29, 125 Stat. 284 (2011), revised 35 U.S.C. §§ 102 and 103 effective March 16, 2013. Because the '872 patent has an effective filing date after March 16, 2013 (Ex. 1001, codes (22), (63)), we refer to the AIA version of Sections 102 and 103.
[2] Tessariol, US 2019/0081061 A1, published Mar. 14, 2019 (Ex. 1006).
[3] Park, US 9,859,297 B2, issued Jan. 2, 2018 (Ex. 1005).

II. ANALYSIS

A. Level of Ordinary Skill in the Art

Petitioner contends that a person of ordinary skill in the art ("POSITA") would have had "a bachelor of science degree in electrical engineering or a similar discipline" with "2–3 years of professional experience working with (e.g., researching, designing, or teaching) monolithic 3D structures and NAND memory devices," or "an equivalent level of skill, knowledge, and experience (e.g., an advanced degree may replace some of the professional experience)." Pet. 33. Petitioner further contends that a "POSITA would have been aware of and generally knowledgeable about 3D NAND's structure, how it is manufactured, and its component parts." *Id*. (citing Ex. 1003 ¶¶ 40–43). Patent Owner states that it does not object to the definition of a POSITA proffered by Petitioner. PO Resp. 13 (citing Pet. 33).

In the Institution Decision, we adopted the assessment offered by Petitioner. Dec. 5–6. Because Petitioner's definition of the level of skill in the art is consistent with the '872 patent and the asserted prior art, we maintain it for purposes of this Final Written Decision. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir 2001).

B. Claim Construction

We construe each claim "in accordance with the ordinary and customary meaning of such claim as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent." 37 C.F.R. § 42.100(b). Under this standard, claim terms are generally given their plain and ordinary meaning as would have been understood by a person of ordinary skill in the art at the time of the invention and in the context of the entire patent disclosure. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1313 (Fed.

Cir. 2005) (en banc). Only those terms in controversy need to be construed, and only to the extent necessary to resolve the controversy. *Realtime Data LLC v. Iancu*, 912 F.3d 1368, 1375 (Fed. Cir. 2019).

1. "dummy source structure"

In the Institution Decision, we preliminarily construed "dummy source structure" to mean "a structure that does not function as a source to the memory cells." Dec. 11. Patent Owner agrees with this preliminary construction, contending that it is supported by the intrinsic evidence that "distinguishes dummy source structures from actual source structures and never describes dummy source structures as providing source to memory cells." PO Sur-reply 3; *see also* PO Resp. 14–18 (arguing that construing "dummy source structure" as a structure that does not function as a source to the memory cell is consistent with its plain and ordinary meaning and the intrinsic record).

Petitioner replies that the overall term "dummy source structure" is a term specific to the '872 patent and does not have a plain and ordinary meaning. Pet. Reply 2. Petitioner does not dispute that both the term "dummy" and "source structure" have a plain and ordinary meaning and admits that the term "dummy" as "a qualifier typically refers to an inoperable component that structurally resembles the non-dummy component." *Id.* at 2 (emphasis omitted). Petitioner further admits "'dummy structure' in a 3D NAND patent means 'electrically inoperable structure that mimics a physical property of an operative structure" and that this "is the plain and ordinary meaning of 'dummy' in 3D NAND prior art." *Id.* at 2–3. Petitioner further asserts that "if 'dummy source structure' did have a plain and ordinary meaning, it would be an inoperable structure that resembles a source structure." *Id.* at 3. Petitioner, however, asserts that this

meaning does not apply here because the Specification states that a dummy source structure can be "an operable structure" and imposes no meaningful structural limitations. *Id.* at 3; *see also* Pet. Reply 10 (stating "the '872 patent departs from the plain meaning of 'dummy'"). Petitioner also contends that "the specification makes clear that a 'dummy source structure' occupies the void used for the gate replacement process" and "does not impose any meaningful limitation on the actual structure of the dummy source structure (the claims only require that the structures include a conductive contact)." Pet. 26. In particular, Petitioner argues that the '872 patent seeks to address structural issues that arise during the gate replacement process by replacing the gate line slits with dummy source structures. Pet. 24–27; Pet. Reply 3–7. According to Petitioner, "the term 'dummy source structure' would have been understood to mean a 'structure that occupies the void that was used for the gate replacement process.'" Pet. 24.

Having considered the parties' respective arguments and evidence presented at trial, we maintain our construction and find that "dummy source structure" means "a structure that does not function as a source to the memory cells."

We begin our analysis with the language of claims. *Phillips*, 415 F.3d at 1312; *see also SuperGuide Corp. v. DirecTV Enterprises, Inc.*, 358 F.3d 870, 874–875 (Fed. Cir. 2004) ("There is a 'heavy presumption' that the terms used in the claims 'mean what they say and have the ordinary meaning that would be attributed to those words by persons skilled in the relevant art."). Claim 1 states that the memory device comprises "a plurality of dummy source structures each extending vertically through the staircase structure, the plurality of dummy source structures surrounding the staircase

contact, wherein each of the dummy source structures comprises a conductive contact." Ex. 1001, 20:11–16. The claim text further states that the staircase structure is on one side of the memory stack, and the memory stack comprises interleaved conductive layers and dielectric layers. *Id.* at 20:7–9. A plain reading of the claim text reveals that each "dummy source structure" extends vertically through the interleaved conductive and dielectric layers on one side of the memory stack, comprises a conductive contact, and that a "plurality of dummy source structures" surround the staircase contact. Other than requiring the presence of a conductive contact, the claim is silent as to the structure and purpose of the dummy source structure.

We turn next to the Specification. *Phillips*, 415 F.3d at 1315; *see also id.* at 1321 (stating "[p]roperly viewed, the 'ordinary meaning' of a claim term is its meaning to the ordinary artisan after reading the entire patent"). The Specification teaches that "[e]ach dummy source structure may include an insulating spacer layer in a dummy source hole and a conductive contact within the spacer layer." Ex. 1001, 5:37–40. Referring to Figure 1D, the Specification explains that "[d]ummy source structure 178 can further include a spacer 177 made of any suitable dielectric materials (e.g., silicon oxide) between contact 179 and memory stack 160 to electrically separate surrounding conductive layers 106 in memory stack 160 from contact 179." *Id.* at 11:39–43.

The Specification further explains that "dummy source structures 178 can laterally separate 3D memory device 100 into multiple memory regions, such as memory blocks." Ex. 1001, 11:44–46. The arrangement of the dummy source structures "may improve the uniformity and stability for etching dummy channel holes in the staircase region" and "may allow the

gate electrode/word lines to be formed with improved uniformity and quality, reducing the resistivity of the gate electrodes/word lines." *Id*. at 5:43–52; *see also id*. at 8:49–53 ("The symmetrical architecture of dummy channel structures and dummy source structures can improve the performance and efficiency of etching processes. Different layouts, patterns, and designs may be adopted based on the size of the staircase region.").

The Specification additionally teaches that "[i]n some embodiments, one or more dummy source structures are in contact with the substrate and may provide interconnect between the 3D memory device and peripheral devices." Ex. 1001, 5:40–43; *see also id.* at 11:46–49 ("dummy source structures 178 may function as interconnects to connect 3D memory device 100 with other peripheral devices"). Such peripheral devices include "any suitable digital, analog, and/or mixed-signal peripheral circuits used for facilitating the operation of 3D memory device 100, such as page buffers, decoders, and latches." *Id*. at 9:34–42. The Specification also teaches that when a dummy source hole is filled in a separate step from forming the word line contact, "any suitable materials can be used to form" the dummy source structure, "including dielectric materials, conductive materials, or any combination thereof." *Id.* at 16:58–63.

The Specification goes on to explain that the material used to fill the dummy source hole results in different functions for the resulting dummy source structure:

> When conductive materials are used to fill dummy source hole 212 (e.g., contact 244), the dummy source structure 246 may function as an interconnect to connect 3D memory device 100 with other peripheral devices. When dielectric materials are used to fill dummy source hole 212, dummy source structure 246 may function as a mechanical support structure to improve the stability of the staircase region.

Ex. 1001, 16:63–17:3. Notably, the Specification does not describe the dummy source structure as functioning as a source for the memory cells. Instead, the Specification distinguishes between dummy source structures and source structures. In particular, the Specification teaches that "[s]ource structures formed in the inner region may be connected with surround channel structures . . . via a common source, such as a doped region" in the substrate. *Id.* at 16:34–38. Dummy source structures, however, "may not connect to channel structures in the channel region," and instead "may be formed simultaneously with source structures in the inner region, while functioning as a mechanical supporting structure after gate-replacement process, without connecting to channel structures in the inner region." *Id.* at 16:38–44.

Read as a whole, the Specification supports the conclusion that a "dummy source structure" does not function as a source for the memory cells. Dummy source structures are variously described as being (1) electrically separated from the conductive layers of the memory stack, (2) used to laterally separate 3D memory device 100 into multiple memory regions, (3) used as a mechanical support structure, and (4) used as an interconnect to peripheral devices. None of these functions are directed to sourcing the memory cells. Moreover, the Specification describes a "source structure" as being connected with a channel structure of a memory string via a common source, such as a doped region in the substrate. That a dummy source structure does not function as a source to the memory cells is consistent with this description of source structure.

It is also consistent with the use of the modifier "dummy," which is indicative of inoperability as compared to a non-dummy counterpart. *See* Ex. 1003 ¶ 80 (Dr. Banerjee testifying that "a POSITA generally would have

understood 'dummy' to refer to an inoperable component"). In this case, it indicates that the "dummy source structure" is inoperable as compared to a source structure. *See* Ex. 2007 ¶ 63 (Dr. Kuhn testifying that "[t]he specification does not suggest that a dummy source structure can function as a source to the memory cells, as that functionality would contradict the label 'dummy source structure'"). A dummy source structure functioning as an interconnect to peripheral circuits used for facilitating the operation of the 3D memory device (such as page buffers, decoders, and latches) is not inconsistent with this understanding, as the dummy source structure is not sourcing the memory cells when it is used as an interconnect.

Petitioner also points to the Specification's statements that, *inter alia*, in "some embodiments, dummy source structure 246 may not connect to the channel structures in the inner region" to mean that in some embodiments, dummy source structures may function as a source. *See* Pet. Reply 7–10; *see also id.* at 8 (quoting Ex. 1001, 16:33–44). Petitioner contends that because the Specification states "a dummy source structure may not function as a source" in some embodiments, it follows that in other embodiments may function as a source. *Id.* at 9 (citing, *inter alia*, Ex. 1035 ¶¶ 41–47).

Contrary to Petitioner's assertions, however, the '872 patent does not state that "a dummy source structure may not function as a source." *See, e.g.*, Pet. Reply 9. Rather, the cited portions of the '872 patent merely state that dummy source structures *may not connect to channel structures in the inner region*. *See* Ex. 1001, 16:33–44. Even if we agree that that the '872 patent discloses embodiments in which dummy source structures *do connect* to the channel structures located in the inner region, Petitioner has not sufficiently shown that such dummy source structures *function as a source to the memory cells*.

In its Reply, Petitioner contends that dummy source structures connected to channel structures are source structures because the '872 patent's use of the term "connect" can "only refer to an electrical connection" in which the source and dummy source electrically connect to provide the source voltage. Pet. Reply 9 (citing Ex. 1035 ¶¶ 48–52); *see also id.* (stating the '872 patent never discloses an embodiment lacking such a connection). Dr. Banerjee testifies that even though "the '872 patent does not detail how these dummy source and source structures function as sources, it was well known." Ex. 1035 ¶ 50. For support, Dr. Banerjee cites to a figure in a 3D NAND textbook of a BiCS (Bit-Cost Scalable) device with a gate connection depicting a source line, which Dr. Banerjee describes as the "equivalent . . . to a dummy source structure (in some embodiments) and source structure." *Id.* ¶ 50 (citing Ex. 1023, 109, Fig. 4.12[4]). Dr. Banerjee states that these source lines have a connection on top to a ground voltage, travel through or outside of the stack, and contact a doped substrate that enables an electrical connect to the substrate region in which the channel structure contacts. *Id.* Dr. Banerjee disagrees with Patent Owner's argument that "there would be a dead-end somewhere along this path" involving dummy source structures. *Id.* Dr. Banerjee explains that although "the '872 patent does not depict and describe the source voltage or the path in the substrate between the source or dummy structure to the channel structures," he has "not seen any such dead-end, e.g., partial path to the channels in the '872 patent." *Id.* Dr. Banerjee states that "[i]nstead, just

[4] We note that although Dr. Banerjee asserts that the vertically depicted most right grey cylindrical structure is a source line, the figure itself labels the horizontal yellow structure as the "Source Line (SL)." Ex. 1023, Fig. 14.2; Ex. 1035 ¶ 50.

like a source structure, it would have been understood that there would be a source voltage on top and a path the channel structures." *Id.*

Petitioner's and Dr. Banerjee's arguments are not persuasive. The arguments are circular as they assert that a POSITA would have understood that dummy source structure must have a complete path (i.e., not have a partial path, or dead-end) like a source structure because the source structure must have a complete path. *See, e.g.*, Ex. 1035 ¶ 50. Similarly, the argument that the '872 patent's use of "connect" can only refer to an electrical connection between dummy source structure 246 and the channel structures is based on a figure depicting a source line as having an electrical connection and Dr. Banerjee's unsupported assertion that the source line is a dummy source line (in some embodiments). Pet. Reply 9; Ex. 1035 ¶ 50. Again, Dr. Banerjee's evidence is circular as it asserts the dummy source structure must have a complete path because the figure depicts a source line having a complete path, and therefore dummy source lines (in some embodiments) must have a complete path. *Id.* To the extent Dr. Banerjee asserts that it was "well known" that dummy source structures function as sources or source structures, any such assertion is not credible in light of his testimony that he had never heard of dummy source structures. *See* Ex. 1035 ¶¶ 17 (stating he "never heard of 'dummy source structure' before reading the '872 patent"), 50 (stating "how these dummy source and source structures function as sources . . . was well known").

Thus, Petitioner's assertion that the '872 patent teaches a dummy source structure may connect to channel structures in the inner region is insufficient to show that the dummy source structure acts as a source to the memory cells.

Accordingly, we determine that "dummy source structure" means "a structure that does not function as a source to the memory cells."

2. "conductive contact"

Claim 1 recites that "each of the dummy source structures comprises a conductive contact." Ex. 1001, 20:15–16. Patent Owner asserts that "conductive contact" should be construed as "a conductive structure that permits current flow with an adjoining conductive structure." PO Resp. 28 (citing Ex. 2007 ¶¶ 95–111). Patent Owner argues that this construction is supported by the Specification because "it describes, for example, dummy source structures that contact another structure such as a peripheral device, and therefore permit current flow to another conductive surface." *Id.* at 30 (citing Ex. 2007 ¶ 102); *see* PO Sur-reply 14–15. Patent Owner also argues that this construction "does not require that the conductive contact actually have current passing through it" or "limit the location of the 'contact' on the dummy source structures (e.g., whether the contact is on top of the dummy source structures or elsewhere)." PO Resp. 32 (citing Ex. 2007 ¶ 107).

Petitioner responds that "the '872 patent describes the 'conductive contact' as a uniform vertical conductive member that extends down towards the substrate." Pet. Reply 15 (citing Ex. 1001, 16:21–32). In that regard, Dr. Banerjee testifies that a POSITA would have understood "conductive contact" to refer to "a conductive material that fills the dummy source hole, i.e., a conductive pillar core." Ex. 1035 ¶ 61. Petitioner contends that "the specification never states or suggests a 'conductive contact' must interconnect two elements," and "it would be legal error to interpret 'conductive contact' contrary to its specification's description and, instead, as 'interconnect.'" *Id.* at 19 (citing *Acumed LLC v. Stryker Corp.*, 483 F.3d 800, 807 (Fed. Cir. 2007)).

Having reviewed the parties' arguments and the supporting evidence, we determine that "conductive contact" as used in the claims of the '872 patent means "a conductive material that fills the dummy source hole."

The Specification indicates that filling a dummy source hole with conductive material results in a dummy source structure that comprises a conductive contact. Ex. 1001, 11:37–39; *see also id.* at 16:23–28 ("Contact 244 can be formed by depositing conductive materials including, but not limited to, W, Co, Cu, Al, polysilicon, silicides, or any combination thereof, over spacer 242 in the dummy source hole using one or more thin film deposition processes, such as ALD, CVD, PVD, and any other suitable processes, or any combination thereof."), 16:50–53 ("contact 244 may be formed simultaneously with word lines contacts by filling conductive materials simultaneously to dummy source hole 212 and staircase contact 122"). The Specification also indicates that the dummy source structure may function as an interconnect to a peripheral device when, for instance, the dummy source structure also contacts the substrate. *Id.* at 5:40–43 ("one or more dummy structures are in contact with the substrate and may provide interconnect between the 3D memory device and peripheral devices"), 16:63–66 ("When conductive materials are used to fill dummy source hole 212 (e.g., contact 244), the dummy source structure 246 may function as an interconnect to connect 3D memory device 100 with other peripheral devices.").

But there is nothing in the Specification that clearly expresses an intent to require dummy source structures comprising conductive material to physically contact another structure or to actually act as an interconnect to peripheral devices. Instead, the Specification describes the dummy source structure as having the *capability* to act as an interconnect to a peripheral

device, whether or not it actually functions as one. Ex. 1001, 5:40–43, 16:63–66. In other words, a conductive contact allows current flow when connected to a peripheral device, but does not require that the conductive contact connects to another device or that current flows through the conductive contact. This understanding is consistent with the Specification's teachings that a dummy source structure "may function" as an interconnect, which indicates that the dummy source structure may not function as an interconnect, even when it is made of conductive materials. In other words, the structure of the conductive contact is the same when it functions as an interconnect to a peripheral device (i.e., "any suitable digital, analog, and/or mixed-signal peripheral circuits used for facilitating the operation of 3D memory device 100, such as page buffers, decoders, and latches") and when it does not.[5] *Id.* at 9:34–42.

In view of the foregoing, we construe "conductive contact" to mean "a conductive material that fills the dummy source hole." No further construction of the term is required to resolve the issues in dispute.

3. Other Terms

We determine that no other term requires express construction to resolve the controversy between the parties. *Realtime Data*, 912 F.3d at 1375. To the extent further discussion of the meaning of any claim term

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[5] At the oral hearing, Patent Owner's counsel acknowledged that "conductive contact" does not require the presence of an adjoining structure. *See* Tr. 34:9–12 (Mr. Radsch stating that "[w]e're not saying that, in our construction, there must be the presence of any particular adjoining structure, but it certainly has to allow the current flow and the interface with an adjoining structure"); *see also id.* at 36:3–17 (Mr. Radsch agreeing that a conductive contact that is shrink-wrapped with a non-conducting material is still a conductive contact "because that's the structure of it in its surroundings").

is necessary to our decision, we provide that discussion below in our analysis of the asserted grounds of unpatentability.

C. Asserted Obviousness over Tessariol

Petitioner contends that claims 1–6 and 11–13 would have been obvious over Tessariol. Pet. 74–101.

1. Overview of Tessariol

Tessariol is directed "to devices, to methods used in forming a circuit structure, and to methods used in forming an array of elevationally-extending transistors and a circuit structure adjacent thereto." Ex. 1006 ¶ 1. Tessariol teaches construction 10 comprises base substrate 11 and various materials formed elevationally over base substrate 11. *Id.* ¶ 27. Figure 9 is reproduced below.

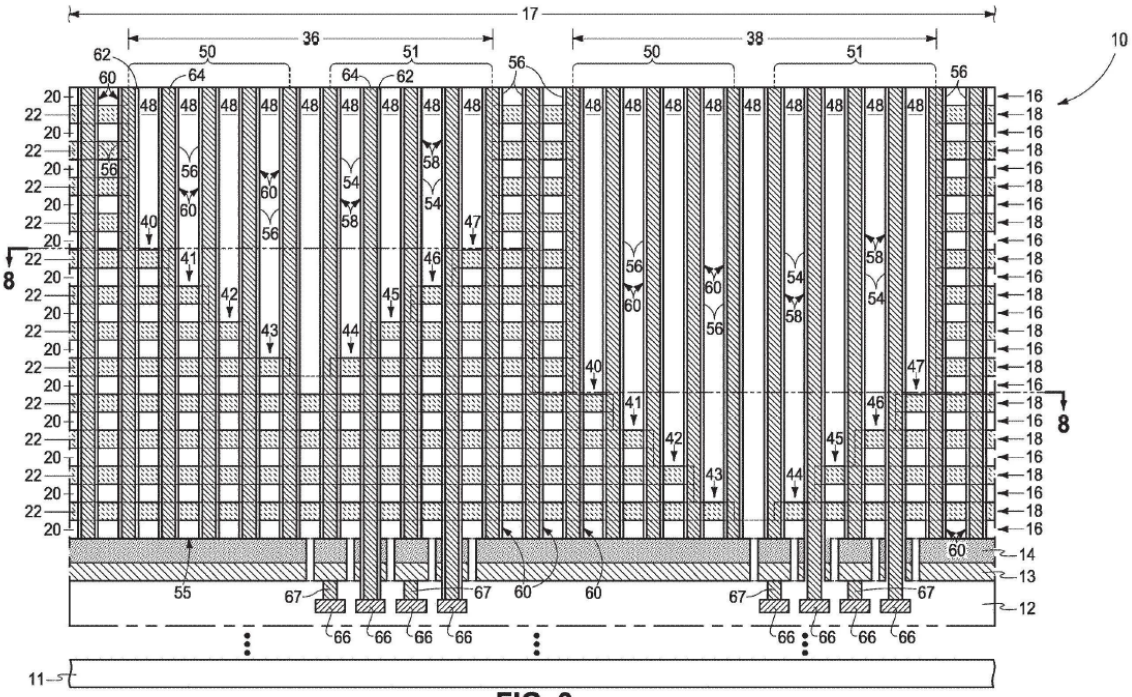

FIG. 9

Figure 9 is a diagrammatic cross-sectional view of a portion of a substrate construction in process as described in Tessariol. *Id.* ¶ 16. Dummy-structure openings 56 and via openings 54 are formed through insulating

material 48 and vertically-alternating tiers 16 and 18. *Id.* ¶ 37. Operative conductive vias 58 are formed within via openings 54, and dummy structures 60 are formed within dummy-structure openings 56. *Id.* ¶ 38. Operative conductive vias 58 and dummy structures 60 comprise insulative lining 62 and conductive core 64. *Id.* Some alternate ones of operative conductive vias 58 are directly electrically coupled to individual conductive lines 66 through source material 14, conductive material 13, and conductive vias 67, and other alternate ones of operative conductive vias 58 are directly electrically coupled to individual conductive lines 66 through materials 14 and 13 to be directly against individual conductive lines 66. *Id.* ¶ 39.

Figure 15 is reproduced below.

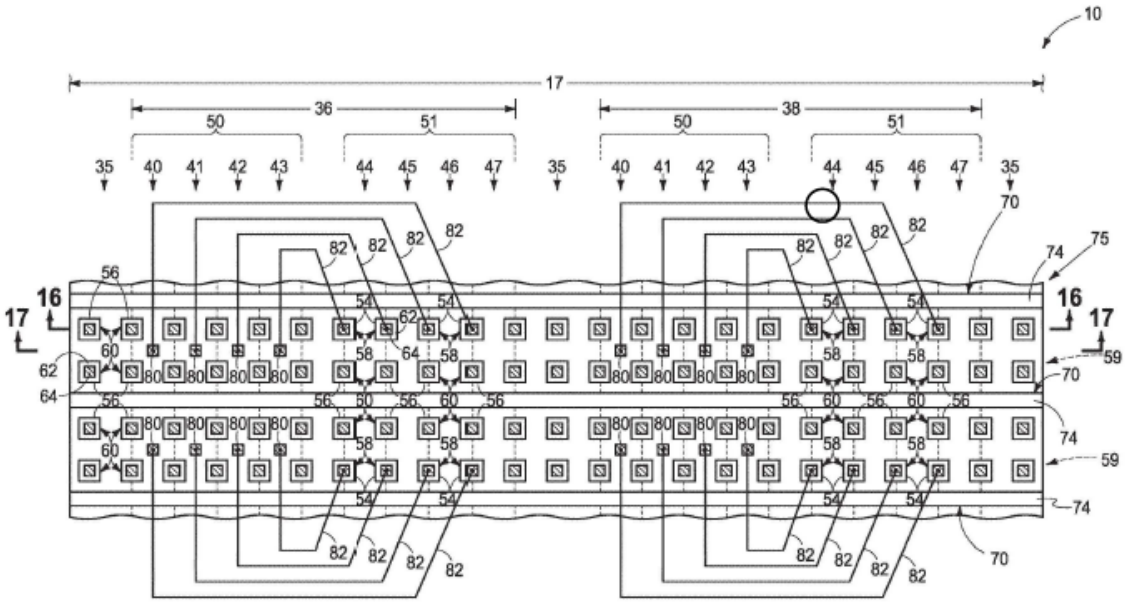

FIG. 15

Figure 15 is a diagrammatic cross-sectional view of a portion of a substrate construction at a later processing step. Ex. 1006 ¶ 22. Operating conducting vias 80 individually extend to and directly electrically couple with conductive material 72. *Id.* ¶ 46. Interconnect lines 82 individually directly electrically couple together different individual operating conducting vias 80

to different individual operating conductive vias 58 through conductive extensions 69. *Id*. Strings 87 of transistors 85 connect with individual conductive lines 84 through conductive extensions 81. *Id*. Insulator material 86 surrounds conductive components 69, interconnect lines 82, conductive extensions 81, and conductive lines 84. *Id*.

Tessariol teaches that "[t]he circuit structures comprises a stair step structure (e.g., any of 34, 36, and 38) comprising vertically alternating tiers (e.g., 16, 18) comprising conductive steps . . . that are at least partially elevationally separated from one another by an insulative material (e.g., 20)." Ex. 1006 ¶ 48. Tessariol also teaches that "[d]ummy structures (e.g., 60) individually extend elevationally through one of the conductive steps at least to the bottom of the vertically-alternating tiers." *Id*. ¶ 48. Tessariol defined "dummy structure" as "a structure which is used to mimic a physical property of another structure (e.g., presence, or physical load-carrying/supporting ability of an operative structure) and which may comprise a circuit inoperable dead end (e.g., is not part of a current flow path of a circuit even if conductive.)" *Id*. ¶ 68.

2. Claim 1

Petitioner contends that Tessariol teaches all of the elements of independent claim 1. Pet. 74–91; Pet. Reply 21–24. For example, Petitioner contends Tessariol teaches "a substrate" (base substrate 11), "a memory stack comprising interleaved conductive layers and dielectric layers on the substrate" (stacks 24 and 30, which comprise alternating layers 20 and 72 on substrate 11), "a staircase structure on one side of the memory stack" (staircase in adjacent region 17 next to array region 15), and "a staircase contact in the staircase structure" (operating conductive via 80). *Id*. at 75–83 (citing Ex. 1006 ¶¶ 27–29, 31, 34, 41, 46, Figs. 1, 2, 5, 6, 17; Ex. 1003

¶¶ 183–201). Patent Owner argues that Tessariol does not disclose "a plurality of dummy source structures each extending vertically through the staircase structure, the plurality of dummy source structures surrounding the staircase contact" (limitation [1.E]) or "each of the dummy source structures comprises a conductive contact" (limitation [1.F]). PO Resp. 55–64.

a) Limitation [1.E]

With respect to limitation [1.E] ("a plurality of dummy source structures each extending vertically through the staircase structure, the plurality of dummy source structures surrounding the staircase contact"), Petitioner contends that Tessariol's dummy structures 60 and conductive vias 58 are the claimed "plurality of dummy source structures" because they comprise insulative lining 62 and conductive core 64, and "are formed in dummy structure openings 56 and elevationally extending via openings 54 that are formed through a memory stack comprised of insulating and conductive materials." Pet. 84 (citing Ex. 1006 ¶¶ 37–38). Petitioner provides an annotated partial version of Tessariol's Figure 15, reproduced below, to illustrate its contentions with respect to the "the plurality of dummy source structures surrounding the staircase contact" element of limitation [1.E].

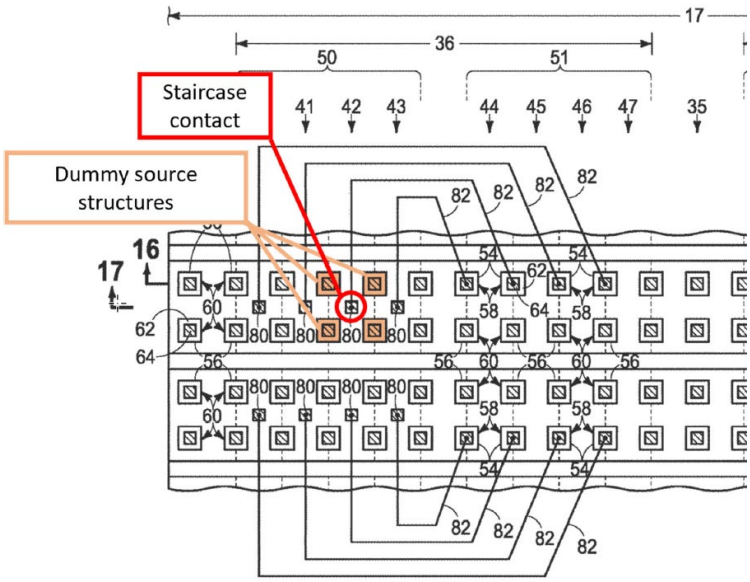

FIG. 15

Annotated partial Figure 15 is a diagrammatic cross-sectional view of a portion of a substrate construction in process as described in Tessariol, with Petitioner's addition of a red circle labeled "Staircase contact" and peach shading labeled "Dummy source structures." Pet. 88; Ex. 1006 ¶ 22. Petitioner contends that four dummy source structures (dummy structures 60, shaded peach) surround each staircase contact 80 (circled in red). Pet. 85–88; Ex. 1003 ¶¶ 202–210.

Patent Owner responds that Petitioner fails to show that Tessariol's conductive vias 58 are dummy source structures that surround the staircase contact. PO Resp. 55–58. In particular, Patent Owner argues that conductive vias 58 are not in the same region of the memory device as operative conductive via 80 (the claimed "staircase contact"), and, therefore, do not surround conductive via 80. *Id.* at 56–58 (citing Ex. 2007 ¶¶ 177–182). Patent Owner also argues that Petitioner fails to show that Tessariol's conductive vias 58 are dummy source structures because "Petitioner does not show that conductive vias 58 are structures that do not function as a

source to memory cells." *Id.* at 55. We agree with Patent Owner that Petitioner does not show that conductive vias 58 are dummy structures that surround the staircase contact as recited in limitation [1.E]. Petitioner only maps dummy structures 60, not conductive vias 58, to the "surrounding the staircase contact" element of claim 1. *Id.* at 87–88 (citing Ex. 1006, Fig. 15; Ex. 1003 ¶¶ 202–210). Indeed, Petitioner acknowledges that dummy structures 60 and conductive vias 58 are in different regions, noting that "dummy support structures 60 are in regions 50 and the conductive vias 58 are in regions 51." Pet. 86 (citing Ex. 1006, Fig. 11). Petitioner's identification of Tessariol's operating conducting vias 80 as the recited "staircase contact" depicts operative conductive vias 80 in regions 50 (where dummy structures 60 are located), but not in regions 51 (where conductive vias 58 are located). *Id.* at 87 (citing Ex. 1006 ¶ 46, Fig. 15). Accordingly, we determine that conductive vias 58 do not satisfy limitation [1.E].

We are persuaded, however, that Tessariol's dummy structures 60 are "dummy source structures," i.e., structures that do not function as a source for the memory cells. Tessariol teaches that

> a "dummy structure" refers to a structure which is used to mimic a physical property of another structure (e.g., presence, or physical load-carrying/supporting ability of an operative structure) and which may comprise a circuit inoperable electrical dead end (e.g., is not part of a current flow path of a circuit even if conductive).

Ex. 1006 ¶ 68. Accordingly, Tessariol teaches that dummy structures 60 are structures that do not function as a source to the memory cells.

We are also persuaded by Petitioner's undisputed contention that Tessariol's dummy structures 60 surround operating conductive vias 80 (the "staircase contact"). As depicted in Tessariol's Figure 15 (annotated partial

version reproduced above), four dummy structures surround each operating conductive via 80. *See* Pet. 88 (providing a partial, annotated version of Figure 15 that identifies four dummy structures 60 in relation to operating conductive via 80); *see also* Ex. 1001, 6:61-67 (stating that Fig. 1A depicts four dummy channel structures indicated by square shape 148 surrounding a staircase contact).

Accordingly, we find that Petitioner establishes, by a preponderance of the evidence, that Tessariol teaches limitation [1.E].

b) Limitation [1.F]

With respect to the "each of the dummy source structures comprises a conductive contact" limitation of claim 1, Petitioner contends that "Tessariol discloses dummy structures 60 and operative conductive vias 58 that comprise 'an insulative lining 62 (e.g., silicon dioxide and/or silicon nitride) and a conductive core 64 (e.g., metal material),'" which "is like an embodiment of the '872 Patent in which the dummy structures have a conductive core and insulating liner." Pet. 89 (citing Ex. 1006 ¶ 38; Ex. 1001, 11:34–49) (footnote omitted). According to Petitioner, Tessariol's dummy source structures include a conductive core, and "[t]he claim requires nothing more." *Id.* at 90 (citing Ex. 1003 ¶ 214).

Patent Owner argues that "Petitioner has not shown that dummy structure[] 60 in Tessariol is a conductive structure that permits current flow with an adjoining conductive structure." PO Resp. 60 (citing Ex. 2007 ¶ 189). Patent Owner argues that dummy structures 60 are covered by insulating materials 86, do not connect to upper-level interconnects, and the bottoms of dummy structures 60 land on a substrate. *Id.* (citing Ex. 2007 ¶¶ 190–192).

As set forth above, we construe "conductive contact" to mean "a conductive material that fills the dummy source hole." *See* § II.B.2, *supra* (also stating that a conductive contact allows current flow if connected to a peripheral device, but does not require that the conductive contact connects to another device or that current flows through the conductive contact). Petitioner sufficiently shows that Tessariol's dummy structures are conductive contacts. In particular, Tessariol teaches that "dummy structures 60 and operative conductive vias 58 are formed to comprise an insulative lining 62 (e.g., silicon dioxide and/or silicon nitride) and a conductive core 64 (e.g., metal material)." Ex. 1006 ¶ 38. Tessariol also teaches that "operative conductive vias 58 and dummy structures 60 are formed at the same time." *Id.* More specifically, Tessariol teaches that "insulative linings 62 and conductive cores 64 in dummy-structure openings 56 and in via openings 54 are formed at the same time." *Id.* Accordingly, Tessariol's dummy source holes (dummy-structure openings 56) are filled with a conductive material (conductive core 64).

For these reasons, we determine that Petitioner establishes, by a preponderance of the evidence, that Tessariol teaches limitation [1.F].

c) Conclusion: Claim 1

Having reviewed the parties' arguments and evidence, we are persuaded that Petitioner's discussion of the particular structures in Tessariol, and the explanations in the Banerjee Declaration, shows that Tessariol teaches all the limitations of claim 1. Accordingly, we determine that Petitioner shows, by a preponderance of the evidence, that claim 1 would have been obvious over the teachings of Tessariol.

3. *Claims 3 and 4*

Claim 3 depends from claim 1 and further recites "at least two of the plurality of dummy source structures are of nominally equal lateral distances to the staircase contact." Ex. 1001, 20:20–22. Claim 4 depends from claim 1 and further recites "the plurality of dummy source structures are of nominally equal lateral distances to the staircase contact." *Id.* at 20:23–25. Petitioner provides an annotated version of a portion of Tessariol's Figure 15, reproduced below, to illustrate its contentions with respect to claims 3 and 4.

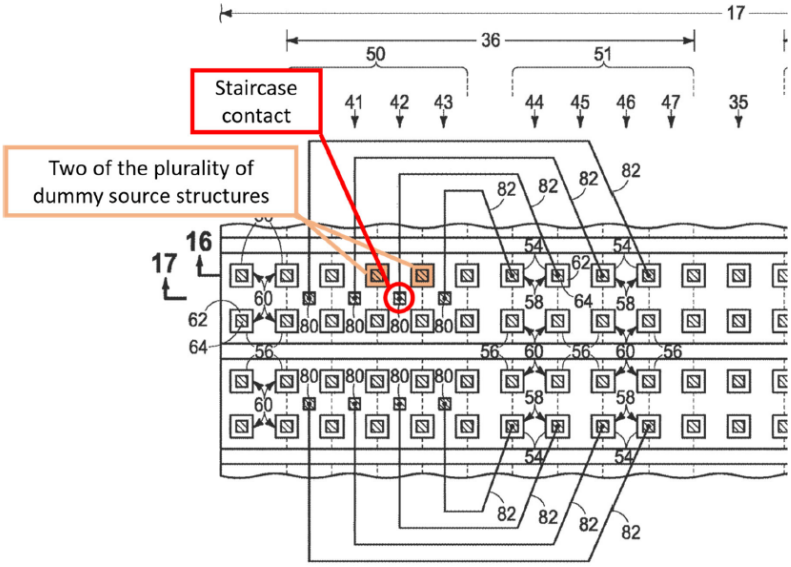

FIG. 15

Annotated partial Figure 15 is a diagrammatic cross-sectional view of a portion of a substrate construction in process as described in Tessariol, with Petitioner's addition of a red circle labeled "Staircase contact" and peach shading labeled "Two of the plurality of dummy source structures." Pet. 93; Ex. 1006 ¶ 22. Petitioner argues that "[a]nnotated Figure 15 discloses that at least two of the dummy structures 60 (i.e., dummy source structures) are of nominally equal lateral distances to the operating conductive via 80 (i.e.,

staircase contact)." Pet. 93 (citing Ex. 1006, Fig. 15; Ex. 1003 ¶ 219) (emphasis omitted); *see also id.* at 94 (referring to Petitioner's discussion of limitation [1.F] and claim 3 with respect to claim 4).

Patent Owner responds that "Petitioner's reliance on Tessariol's Figure 15 is insufficient to show that the claimed distance-based requirement is satisfied." PO Resp. 65 (citing Ex. 2007 ¶ 206). Patent Owner asserts that "Fig. 15 does not include a scale, dimensions, or any other means to measure distances between components," and contends that "Petitioner does not explain how distances are measured or what (if any) scale is being used to measure the distances in the figure." *Id.* (citing Pet. 93; Ex. 2007 ¶¶ 207–208); *see* PO Sur-reply 27–28.

After considering the complete record, we are persuaded that Petitioner sufficiently establishes that Tessariol teaches "at least two of the plurality of dummy source structures are of nominally equal lateral distances to the staircase contact" and "the plurality of dummy source structures are of nominally equal lateral distances to the staircase contact" as recited in claims 3 and 4. As an initial matter, we note that the '872 patent defines "nominal/nominally" as follows:

> As used herein, the term "nominal/nominally" refers to a desired, or target, value of a characteristic or parameter for a component or a process operation, set during the design phase of a product or a process, together with a range of values above and/or below the desired value. The range of values can be due to slight variations in manufacturing, processes or tolerances.

Ex. 1001, 4:9–15. Referring to Figure 1A, the '872 patent also teaches that "[t]he four dummy source structures indicated by 146 may be spaced with nominally equal lateral distances to staircase contact 122. In other words, the four dummy source structures indicated by 146 may be evenly or

uniformly distributed around staircase contact 122." *Id.* at 6:46–50. Accordingly, we understand "nominally equal lateral distances" as used in claims 3 and 4 to include evenly or uniformly distributed structures. *See* Ex. 1003 ¶ 162 (Dr. Banerjee testifying that "[n]ominally lateral distances to, in the context of the '872 Patent, includes being 'evenly or uniformly distributed.'").

Tessariol's Figure 15 illustrates that dummy structures 60 are evenly distributed around operating conductive vias 80. Ex. 1006, Fig. 15. The figure is consistent with Tessariol's teaching that dummy-structure openings 56 (which become dummy structures 60) are "collectively arrayed in straight-line rows and columns" and "any alternate configuration may be used including, for example, staggering . . . alternating openings 54/56 in rows and/or columns." *Id.* ¶ 37. We also credit Dr. Banerjee's testimony that "it is best practice to use repeating patterns in semiconductive designs" and "a POSITA viewing the Tessariol figures would immediately interpret the figures to include this repeating pattern, in which these objects are of equal distance from the contact." Ex. 1035 ¶ 85.

We disagree with Patent Owner that Tessariol's Figure 15 is insufficient to show that the dummy source structures are of nominally equal lateral distances to the staircase contact. The Federal Circuit has held that "the speculative modeling premised on unstated assumptions in prior art patent drawings cannot be the basis for challenging the validity of claims *reciting specific dimensions not disclosed directly in such prior art*." *Nystrom v. TREX Co.*, 424 F.3d 1136, 1148 (Fed. Cir. 2005) (emphasis added). Here, claims 3 and 4 recite relative positioning ("nominally equal lateral distances"), not specific dimensions or proportions. Accordingly, we find Petitioner's reliance on Tessariol's Figure 15 to establish the placement

of dummy structures 60 relative to operative conducting via 80 is proper, particularly given Dr. Banerjee's credible testimony regarding best practices in semiconductor design and that a POSITA viewing the Tessariol figures would have understood the objects are of equal distance from the contact. *See* Ex. 1035 ¶ 85.

Based on our consideration of the entire record, and for the reasons set forth above, we determine that Petitioner shows, by a preponderance of the evidence, that claims 3 and 4 would have been obvious over the teachings of Tessariol.

4. Claims 2, 5, 6, and 11–13

Petitioner contends that Tessariol teaches all of the limitations of claims 2, 5, 6, and 11–13 that depend, directly or indirectly, from claim 1. Pet. 92, 94–101. Patent Owner does not dispute that Tessariol teaches the limitations of these claims. *See* PO Resp. Having reviewed the parties' arguments and evidence, we are persuaded that Petitioner's discussion of the particular structures in Tessariol, and the explanations in the Petition and the Banerjee Declaration, shows that Tessariol teaches all of the limitations of dependent claims 2, 5, 6, and 11–13.

Accordingly, we determine that Petitioner establishes by a preponderance of the evidence that claims 2, 5, 6, and 11–13 would have been obvious over the teachings of Tessariol.

D. Asserted Obviousness over Park

Petitioner contends that claims 1–6, 11, and 13 would have been obvious over the teachings in Park. Pet. 40–74.

1. Overview of Park

Park relates "to semiconductor devices including vertical channels and methods of manufacturing the same." Ex. 1005, 1:22–25. Park teaches that

the "semiconductor device includes a substrate, first channel structures, gate lines, cutting lines, dummy patterns and dummy lines" and provides "improved structural and electrical reliability." *Id*. at 1:36–41.

Figure 2 is reproduced below.

FIG. 2

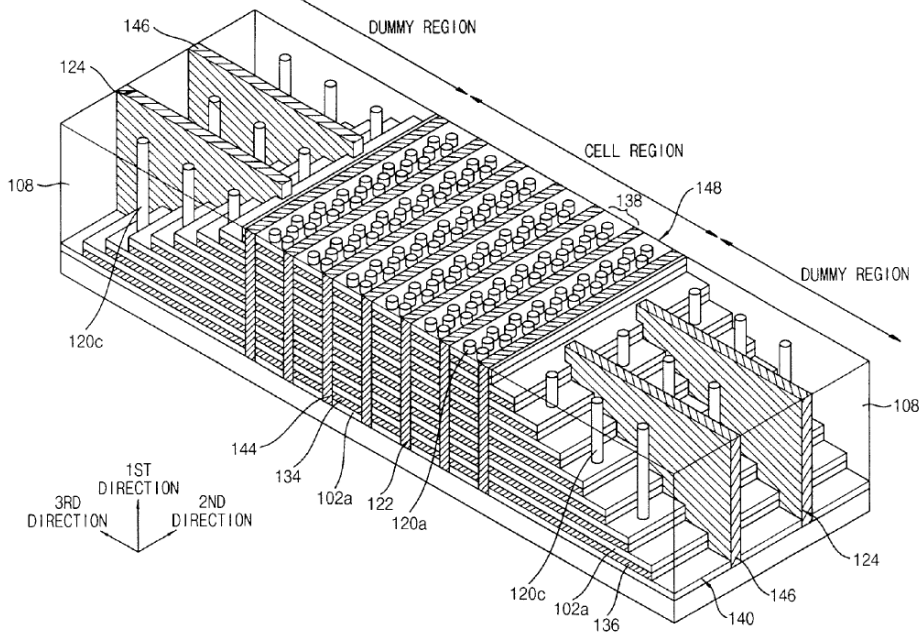

Figure 2 illustrates a perspective view of a semiconductor device described in Park. Ex. 1005, 3:35–37. The semiconductor device includes a memory cell structure disposed on a cell region of substrate 100 and a dummy structure disposed on a dummy region of substrate 100. *Id*. at 6:1–4. The memory cell structure includes first and second channel structures 120a and 120b, gates lines 134, and common source line (CSL) 144. *Id*. at 6:9–11. Gate lines 134 are formed on outer sidewalls of first and second channel structures 120a and 120b, extend in the second direction,[6] and are spaced

[6] Park explains that "[a] direction substantially vertical to the top surface of the substrate is referred to as a first direction, and two directions substantially parallel to the top surface of the substrate and substantially

apart from each other along the first direction. *Id*. at 6:11–15. Park teaches that the lowermost gate line of gate lines 134 may serve as a ground selection line (GSL), the uppermost gate line of the gate lines 134 may serve as a string selection line (SSL), and gate lines 134 in between may serve as word lines. *Id*. at 7:11–15.

Insulating interlayer pattern 102a is interposed at each level between gate lines 134, and insulating interlayer pattern 102a and gate lines 134 may be alternately stacked along the first direction to define first structure 138, which may extend in the second direction. Ex. 1005, 7:19–26. "Both lateral portions of the first structure 138 in the second direction may serve as a wiring region and have a stepped shape," such that "different wirings may be connected to different gate lines 134 included in the first structure 138 so that an electrical signal may be individually applied to each gate line 134." *Id*. at 7:26–31. First opening 122 may be formed between first structures 138 neighboring each other and may extend through the alternating stack of insulating interlayer patterns 102a and gate lines 134 to the top of substrate 100. *Id*. at 7:52–56.

The dummy structure includes second structure 140 and dummy source line 146. *Id*. at 8:1–2. A plurality of second structures 140 may be arranged and spaced apart from each other along the second direction, with a plurality of dummy source lines 146 extending between the neighboring second structures 140. *Id*. at 8:3–6. Second structure 140 may include alternately stacked insulating interlayer patterns 102a and dummy patterns 136. *Id*. at 8:7–9. Park teaches that insulating interlayer

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crossing each other are referred to as a second direction and a third direction." Ex. 1005, 5:57–61.

pattern 102a in second structure 140 may be the same as insulating interlayer pattern 102a in first structure 138, and that dummy patterns 136 may be formed at levels corresponding to gate lines 134 in first structure 138. *Id*. at 8:13–18. Second opening 124 may be formed between neighboring second structures 140 and may extend to the top surface of substrate 100. *Id*. at 8:27–31. Dummy source line 146 may be disposed in second opening 124 and may be in contact with the top of substrate 100. *Id*. at 8:49–51.

2. Analysis

Petitioner contends that Park teaches all of the elements of independent claim 1. Pet. 40–74. For example, Petitioner contends Park teaches "a substrate" (substrate 100), "a memory stack comprising interleave conductive layers and dielectric layers on the substrate" (layers 102a and 134 in the cell region, which is a stack on substrate 100), "a staircase structure on one side of the memory stack" (stepped regions on each side of the main cell region), and "a staircase contact in the staircase structure" (contact plug 150 in the step structure wiring area). *Id*. at 41–50 (citing Ex. 1005, 5:48–50, 6:1–4, 7:6–10, 7:19–37, 9:38–46, 10:7–10; Figs. 1–3; Ex. 1003 ¶¶ 115–137).

As to limitation [1.E] ("a plurality of dummy source structures each extending vertically through the staircase structure, the plurality of dummy source structures surrounding the staircase contact"), Petitioner contends that Park's common source lines 144 and dummy source lines 146 are the claimed "plurality of dummy source structures" because "[d]uring the gate replacement process, first openings 122 and second openings 124 are etched in the insulating/sacrificial layer stack," and "are the voids that are used for the gate replacement process." Pet. 50–52 (citing Ex. 1005, 11:66–12:4,

Fig. 9). Petitioner further contends that after the gate replacement process, first opening 122 and second opening 124 "are each lined with an insulating layer and then filled with conductive material to form a common source line 144 and a dummy source line 146, respectively." *Id*. at 53 (citing Ex. 1005, 13:39–41). Petitioner contends that "[t]he '872 Patent describes almost identical dummy source structures" to "Park's common source lines 144 and dummy source lines 146" because "the '872 Patent states that 'dummy source structures 178 can laterally separate 3D memory device 100 into multiple memory regions, such as memory blocks," and "Park's common source lines 144 and dummy source lines 146 do the same." *Id*. at 54 (citing Ex. 1001, 11:44–46; Ex. 1005, 12:5–18). Petitioner also contends that Park's common source lines 144 "are an interconnect for a source connection," like the '872 Patent's dummy source structures that "may provide interconnect between the 3D memory device and peripheral devices." *Id*. at 55–56 (citing Ex. 1001, 5:41–43, 16:63–66; Ex. 1005, 7:63–64; Ex. 1003 ¶ 146.

Patent Owner argues that Park's common source lines 144 "function as a common source lines and therefore are not 'dummy source structures' as properly construed." PO Resp. 44–45 (citing Ex. 2007 ¶¶ 135–145). Patent Owner asserts that "Park expressly distinguishes between the 'common source line' for the memory cell structure, which functions as the source line, and a 'dummy source line.'" *Id.* at 46 (citing Ex. 1005, 6:1–11, 7:59–60, 13:39–41). Patent Owner also argues that Park's dummy source lines 146 cannot be the claimed dummy source structures because "Petition maps only the common source lines to other limitations of the claims relating to the dummy source structure, such as the requirement of 'the

plurality of dummy source structures surrounding the staircase contact.'" *Id.* at 45 (citing Pet. 50–62).

After reviewing the parties' arguments and evidence, we determine that Petitioner does not establish that Park discloses or teaches "dummy source structures" as recited in limitation [1.E]. As set forth above, we construed "dummy source structure" to mean "a structure that does not function as a source to the memory cells." *See* § II.B.1, *supra*. Park distinguishes common source lines 144 that are included on the memory cell structure with first and second channel structures 120a and 120b, and gate lines 134 from dummy source lines 146 that are included on the dummy region with second structure 140 and third channel structure 120c that "may not serve as a channel of the memory cell, and may merely serve as a supporting pillar of the second structure 140." Ex. 1005, 6:9–11, 8:1–2, 8:57–60. That common source lines 144 are disposed on the cell region of the substrate while dummy source lines 146 are disposed on the dummy region alone indicates that the common source lines 144 and dummy source lines 146 do not operate in the same way or serve the same purpose. Moreover, Petitioner does not dispute Patent Owner's contention that Park's common source lines 144 "function as a common source lines and therefore are not 'dummy source structures' under the Board's construction. *See* Pet. Reply 26. Rather, Petitioner implicitly acknowledges that Park's common source lines 144 are not dummy source structures when it responds to Patent Owner's argument by stating only that "the Board should reject the negative claim limitation on which this argument depends." Pet. Reply 26.

Although Petitioner also identifies dummy source lines 146 as the claimed "dummy source structures," Petitioner relies only on common source lines 144 with respect to the "surrounding" element of claim [1.E].

See Pet. 59 ("Common source lines 144 alone surround the staircase contacts, and that is all that is necessary to satisfy claim 1."). Because Petitioner does not rely on dummy source lines 146 with respect to all the properties that are relevant to the claimed "dummy source structure," we also determine that Petitioner does not adequately establish that dummy source lines 146 are "dummy source structures" as recited in claim 1.

For these reasons, we determine that Petitioner does not establish, by a preponderance of the evidence, that independent claim 1, and claims 2–6, 11, and 13 that depend therefrom, would have been obvious over the teachings in Park.

III. CONCLUSION

After reviewing the parties' arguments and weighing the evidence offered by both parties, we determine that Petitioner shows, by a preponderance of the evidence, that claims 1–6 and 11–13 of the '872 patent would have been obvious over the teachings in Tessariol. We also determine that Petitioner does not show, by a preponderance of the evidence, that claims 1–6, 11, and 13 would have been obvious over the teachings in Park.

In summary:

Claim(s)	**35 U.S.C. §**	**Reference(s)/Basis**	**Claim(s) Shown Unpatentable**	**Claim(s) Not Shown Unpatentable**
1–6, 11–13	103	Tessariol	1–6, 11–13	
1–6, 11, 13	103	Park		1–6, 11, 13
Overall Outcome			1–6, 11–13	

IV. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that Petitioner has established by a preponderance of the evidence that claims 1–6 and 11–13 of the ’872 patent are unpatentable; and

FURTHER ORDERED that, because this is a Final Written Decision, parties to the proceeding seeking judicial review of the Decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

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