

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,
Patent Owner

Case No.: IPR2024-00790
U.S. Patent No. 10,868,031
Issue Date: December 15, 2020

Title: MULTIPLE-STACK THREE-DIMENSIONAL MEMORY DEVICE
AND FABRICATION METHOD THEREOF

**PETITION FOR *INTER PARTES* REVIEW
OF U.S. PATENT NO. 10,868,031
PURSUANT TO 35 U.S.C. §§311-319 AND 37 C.F.R. §42**

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LISTING OF EXHIBITS

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1001	U.S. Patent No. 10,868,031 to Liu et al.
1002	File History of U.S. Patent No. 10,868,031 to Liu et al.
1003	Declaration of Dr. Sanjay Banerjee (“Banerjee”)
1004	<i>Curriculum Vitae</i> of Dr. Sanjay Banerjee
1005	U.S. Patent No. 10,381,369 to Kim et al. (“Kim”)
1006	U.S. Patent Publ. No. 2019/0081061 A1 to Tessariol et al. (“Tessariol”)
1007	Aritome, “NAND Flash Memory Technologies” (2016)
1008	Silvagni, “3D NAND Flash Based on Planar Cells,” Computers 2017
1009	Micheloni et al., “Inside Solid State Drives (SSDs)” (2 nd Ed. 2018)
1010	U.S. Patent No. 10,475,737 to Tang et al.
1011	U.S. Patent No. 10,559,583 to Park et al.
1012	U.S. Patent No. 9,768,186 to Shimabukuro et al.
1013	U.S. Patent No. 9,728,499 to Shimabukuro et al.
1014	U.S. Patent No. 9,299,641 to Sekar et al.
1015	U.S. Patent No. 11,244,725 to Goda et al.
1016	U.S. Patent No. 9,142,302 to Dong et al.
1017	Minute Order, Dkt. No. 42, dated February 22, 2024 in <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC</i> , Case No. 3:23-cv-05792-RFL

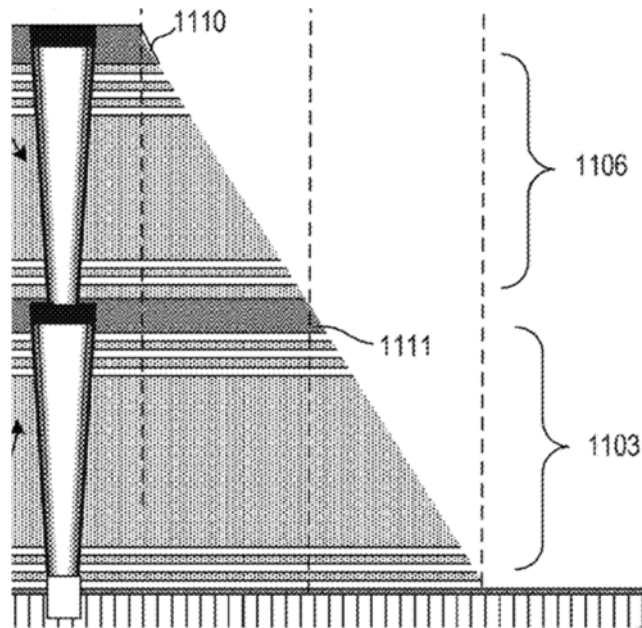
Exhibit	Description
1018	Combined Civil and Criminal Federal Court Management Statistics (December 31, 2023), available at https://www.uscourts.gov/sites/default/files/data_tables/fcms_na_distcomparison1231.2023.pdf
1019	Docket from <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC</i> , Case No. 3:23-cv-05792-RFL
1020	Micheloni, “3D Flash Memories” (2016)
1021	Top Seiko Co., Ltd., Guide to Materials
1022	Sharpe, W.N., et al., “Mechanical Properties of MEMS Materials,” DARPA, AFRL-IF-RS-TR-2004-76 (March 2004)
1023	Wolf. S., et al., “Silicon Processing for the VLSI Era, Volume 1 – Process Technology, Chapter 15, Multilevel Interconnects for ULSI,” (2 nd Ed. 2000)

I. INTRODUCTION

Petitioner Micron Technology, Inc. (“Micron” or “Petitioner”) respectfully requests *Inter Partes* Review (“IPR”) of Claims 1-5 (“the Challenged Claims”) of U.S. Patent Number 10,868,031 (“the ’031 Patent”). There is more than a reasonable likelihood that Petitioner will prevail with respect to at least one claim.

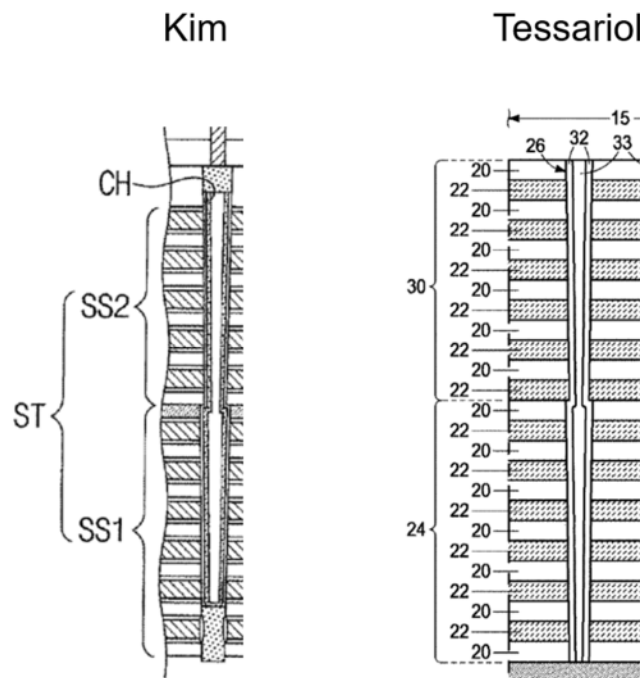
The ’031 Patent relates to 3D NAND memory devices. Typical prior art 3D NAND devices are formed from alternating layers of conductive and insulating material stacked on a substrate. The ’031 Patent admits that 3D NAND devices with multiple stacks, *i.e.*, stacks stacked on top of one another, were known in the prior art. Ex. 1001, 1:23-38. The ’031 Patent also admits that it was known in 3D NAND devices to use both vertical channel structures and supporting pillars in the same device. *Id.* The ’031 Patent, however, alleges that the fabrication process for channel structures and supporting pillars in a multi-stack 3D NAND is “time-consuming and costly.” *Id.*, 1:34-38. Accordingly, the ’031 Patent describes and claims multi-stack 3D NAND devices that include supporting pillars with ***aligned sidewalls*** and channel structures with ***unaligned sidewalls***. Although the claims do not recite any method steps, the ’031 Patent describes a ***one-step etch process*** that creates the supporting pillars with ***aligned sidewalls*** and a ***two-step etch process*** that creates the channel structures with ***unaligned sidewalls***, which purportedly overcomes the alleged prior art deficiencies.

That the claims require ***unaligned*** channel structures was the reason for allowance. During prosecution, the Examiner issued only a single rejection over the prior art. The Applicant overcame that rejection by noting that unlike the pending claims, the prior art two-stack structures had aligned channel structures. The '031 Patent depicts a channel structure with unaligned sidewalls below:



Ex. 1001, Fig. 11 (partial). As is evident from the above figure, the unaligned sidewalls are the result of two etches: a first etch through the first stack (1103) and a second etch through the second stack (1100). This is because a typical etch will create a hole with a diameter that is widest at the top of the hole and that tapers down in size towards the bottom of the hole. The result is the unaligned sidewall at the interface between the two stacks.

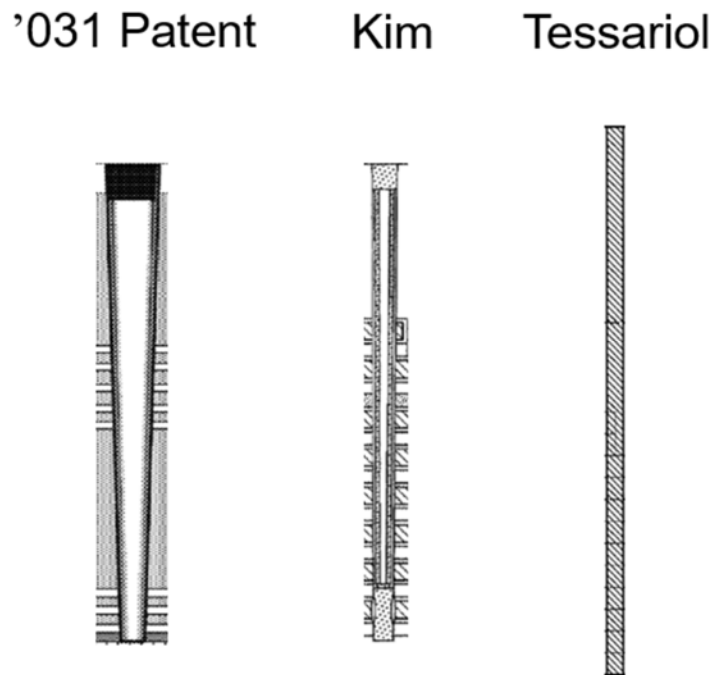
The Petition relies on two primary references: Kim and Tessariol. Neither reference was before the Examiner during prosecution. Each discloses a *one-step etch process* that creates the supporting pillars with *aligned sidewalls* and a *two-step etch process* that creates the channel structures with *unaligned sidewalls*. As to the '031 Patent's supposed point of novelty, as shown below, Kim and Tessariol disclose the exact same unaligned channel structures as the '031 Patent:



Kim, Fig. 4B; Tessariol, Fig. 5. As can be seen above in Kim's Figure 4B, the two etches (one through stack SS1 and a second through stack SS2) create the same unaligned sidewalls as the '031 Patent claims. And as can be seen above in Tessariol's Figure 5, the two etches (one through stack 24 and a second through stack 30) create the same unaligned sidewalls as the '031 Patent claims.

What's more, Kim expressly teaches that the unaligned sidewalls are the result of the two-step etch process: “[t]he vertical channel structure can have a side wall with a stepped profile at a level in the vertical channel structure where the upper structure meets the lower structure.” Kim, 1:45-48. Kim also discloses that etch holes may be “misaligned.” *Id.*, 11:32-35.

And just like the '031 Patent, Kim and Tessariol both disclose a *one-step etch process* that creates the supporting pillars with *aligned sidewalls*:



Ex. 1001, Fig. 4; Kim, Fig. 4B; Tessariol, Fig. 9. As can be seen above, because the '031 Patent, Kim, and Tessariol use a one-step etch process to create dummy pillars, the pillars have aligned sidewalls without the stepped profile at the interface between the stacks. And in contrast to a two-step etch process, Kim expressly teaches that the aligned sidewalls are the result of a one-step etch process: “the vertical dummy

structure can have a side wall with a planar profile at the level where the upper structure meets the lower structure.” Kim, 1:51-53.

Petitioner requests that the Board institute trial and find the Challenged Claims unpatentable as obvious under §103.

II. REQUIREMENTS FOR PETITION FOR *INTER PARTES* REVIEW

A. Grounds for Standing (37 C.F.R. §42.104(a))

Petitioner certifies that the '031 Patent is available for IPR and that Petitioner is not barred or estopped from requesting IPR of the Challenged Claims of the '031 Patent on the grounds identified herein.

B. Notice of Lead and Backup Counsel and Service Information (37 C.F.R. §§42.8(b)(3-4), 41.10(a))

Pursuant to 37 C.F.R. §§42.8(b)(3-4) and 42.10(a), Petitioner provides the following designation of Lead and Back-Up counsel.

Lead Counsel	Back-Up Counsel
Jeremy Jason Lang Registration No. 73,604 (jlang@orrick.com) Postal & Hand-Delivery Address: Orrick, Herrington & Sutcliffe LLP 1000 Marsh Road Menlo Park, CA 94025-1015 T: 650-614-7400; F: 650-614-7401	Jared Bobrow <i>Pro Hac Vice</i> to be submitted (jbobrow@orrick.com) Postal & Hand-Delivery Address: Orrick, Herrington & Sutcliffe LLP 1000 Marsh Road Menlo Park, CA 94025-1015 T: 650-614-7400; F: 650-614-7401 K. Patrick Herman Registration No. 75,018 (pherman@orrick.com) Postal & Hand-Delivery Address: Orrick, Herrington & Sutcliffe LLP 51 West 52nd Street New York, NY 10019 T: 212-506-5000; F: 212-506-5151

Petitioner consents to service by electronic mail at the following addresses: PTABDocketJJL2@orrick.com, P52PTABDocket@orrick.com, PTABDocketJ3B3@orrick.com, and micron-ymtc_ohs@orrick.com. Pursuant to 37 C.F.R. §42.10(b), Petitioner’s Power of Attorney is attached.

C. Notice of Real-Parties-in-Interest (37 C.F.R. §42.8(b)(1))

Petitioner Micron Technology, Inc., and its subsidiaries, including Micron Consumer Products Group LLC, are the real-parties in interest.

D. Notice of Related Matters (37 C.F.R. §42.8(b)(2))

According to USPTO assignment records, the ’031 Patent is currently assigned to Yangtze Memory Technologies, Co., Ltd. (“YMTC” or “Patent

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Owner”). YMTC has asserted the ’031 Patent and U.S. Patent Nos. 10,658,378, 10,861,872, 10,937,806, 10,950,623, 11,468,957, 11,501,822 and 11,600,342 in a co-pending litigation, *Yangtze Memory Technologies Co., Ltd. v. Micron Technology, Inc. & Micron Consumer Products Group, LLC*, Case No. 3:23-cv-05792-RFL (N.D. Cal., filed November 9, 2023) (“Co-Pending Litigation”).

In addition to this Petition, Petitioner is filing petitions for *inter partes* review of each asserted patent in the Co-Pending Litigation: Petition for *Inter Partes* Review of U.S. Patent No. 10,658,378, IPR2024-00788, Petition for *Inter Partes* Review of U.S. Patent No. 10,861,872, IPR2024-00789, Petition for *Inter Partes* Review of U.S. Patent No. 10,937,806, IPR2024-00791, Petition for *Inter Partes* Review of U.S. Patent No. 10,950,623, IPR2024-00794, Petition for *Inter Partes* Review of U.S. Patent No. 11,468,957, IPR2024-00792, Petition for *Inter Partes* Review of U.S. Patent No. 11,501,822, IPR2024-00795 and Petition for *Inter Partes* Review of U.S. Patent No. 11,600,342, IPR2024-00793.

The Director and the Board should allow this Petition under 35 U.S.C. §314(a), 325(d), and/or 37 C.F.R. §42.108(a).

E. Fee for *Inter Partes* Review

The Director is authorized to charge the fee specified by 37 C.F.R. §42.15(a), and any other required fees, to Deposit Account No. 15-0665.

F. Proof of Service

Proof of service of this Petition on the Patent Owner at the correspondence addresses of record for the '031 Patent is attached.

III. IDENTIFICATION OF CLAIMS BEING CHALLENGED (§42.104(B))

The application for the '031 Patent was filed on September 10, 2018 and claims priority to an earlier-filed PCT publication No. PCT/CN2018/097432, filed on July 27, 2018. This Petition assumes that July 27, 2018 is the priority date for the '031 Patent (the “Priority Date”).

Petitioner relies on the following references under the grounds presented in the following table:

Ground	Claim(s)	Prior Art Asserted
1	1-4	Obvious under §103 based on U.S. Pat. No. 10,381,369 (Ex. 1005, “Kim”) ¹
2	1-2 and 4-5	Obvious under §103 based on U.S. App. Pub. No. 2019/0081061 (Ex. 1006, “Tessariol”) ²
3	4	Obvious under §103 based on Kim in view of Tessariol
4	1-2 and 4-5	Obvious under §103 based on Tessariol in view of Kim

¹ Kim was filed December 14, 2017 and is prior art under at least AIA §102(a)(2).

² Tessariol was filed September 14, 2017 and is prior art under at least AIA §102(a)(2).

None of the references on which these grounds are based was cited or discussed by the Examiner during prosecution of the '031 Patent.

These grounds are supported by the Declaration of Dr. Sanjay Banerjee (“Banerjee,” Ex. 1003).

IV. INSTITUTION SHOULD BE GRANTED

Petitioner has established a reasonable likelihood of success on the merits. All other requirements for IPR have been met. The Board should institute IPR.

A. There Are No Grounds For A § 314 Discretionary Denial In This Case

There is a pending district court action involving the '031 Patent. The PTAB has explained that it “will not ... discretionarily deny institution in view of a parallel district court litigation where a petition presents compelling evidence of unpatentability.” 6/21/22 Interim Procedure, 2, 4-5. Petitioner submits that it presents a compelling case here: the claims of the '031 Patent are unambiguously unpatentable.

Petitioner also notes that the factors considered by the Board when assessing whether to institute IPR in light of a parallel proceeding collectively weigh in favor of institution. *See Apple Inc. v. Fintiv, Inc.*, Case No. IPR2020-00019, Paper No. 11 (Mar. 20, 2020) (precedential) (“Fintiv”). In particular: the district court may stay the case, any potential trial will occur years from now, little district court work has

occurred, petitioner diligently prepared this petition, and the petition is substantively strong.

1. Possibility of a Stay

Petitioner intends to seek a stay if the Board institutes IPR. Until this issue is adjudicated, any attempt to predict the outcome would require speculation. This factor is neutral. *See Sand Revolution II, LLC v. Continental Intermodal Group – Trucking LLC*, IPR2019-01393, Paper 24 at 7 (PTAB June 16, 2020) (informative) (“Sand Revolution”); Fintiv at 12 (similar).

2. Proximity of the Court’s Trial Date

On February 22, 2024, the district court entered a scheduling order which set a trial date of December 1, 2025. *See* Ex. 1017. As a result, if IPR proceedings are instituted, they should be completed well before the scheduled trial date. *See also* Ex. 1018 (statistics indicating that it takes on average 48.9 months to reach trial in district). This weighs strongly in favor of institution.

3. Investment in the Parallel Proceeding

To date, the parties and Court have invested very little in the parallel proceeding. Indeed, beyond engaging in some motion practice regarding the pleadings, no substantive progress has been made. The parties are months away from the exchange of infringement and invalidity contentions and have not taken any depositions. Fact discovery is in its infancy. No claim construction positions have been exchanged, no claim construction order has issued, no infringement or

invalidity expert discovery has occurred, and no summary judgment motions have been filed. This weighs in favor of institution. *See Sand Revolution* at 11.

The Board also has explained that institution is appropriate where “the petitioner filed the petition expeditiously....” *Fintiv* at 11. Here, Patent Owner asserted eight different patents against Petitioner. *See* Ex. 1019. Yet, Petitioner proceeded with diligence filing approximately 5 months after being served with the original complaint and approximately 2 months after the filing of an amended complaint. *See id.* This also weighs strongly in favor of institution.

4. Issue Overlap

Given the early stage of the parallel proceeding, it is not yet possible to determine the amount of overlap. Patent Owner has not yet served infringement contentions or identified the asserted claims. Moreover, should the Board institute, Micron stipulates that it will not advance in District Court any invalidity defense that formed the basis of any of the grounds in this Petition. Micron submits that this eliminates any potential overlap in issues between the proceedings here and in District Court. The Board has found that such stipulations weigh in favor of institution. *Sand Revolution* at 11-12.

5. Party Overlap

Both Petitioner and Patent Owner are parties in the parallel proceeding. This, however, is of little moment as there is often party overlap when there is a parallel proceeding.

6. Other Circumstances

Here, Petitioner submits that its petition has significant substantive merit. It is premised on clear, understandable prior art that the Patent Office did not previously consider. Thus, this factor also weighs in favor of institution.

B. Denial Under § 325(d) Would Be Inappropriate

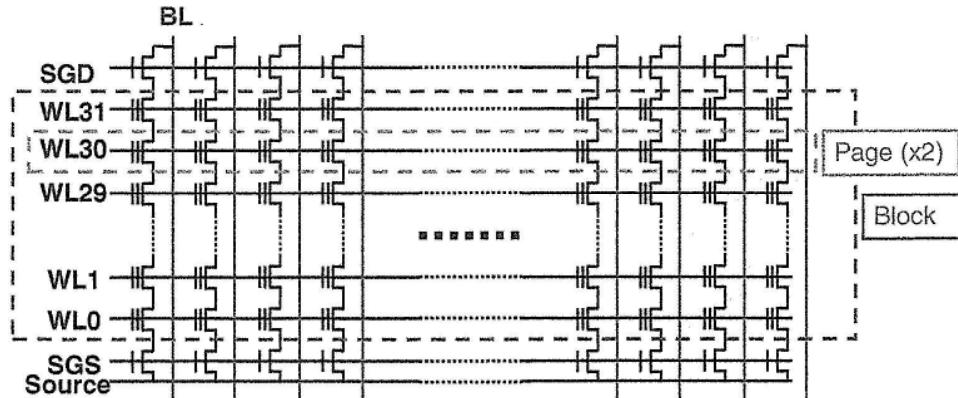
The Examiner did not cite or discuss any of the references on which these grounds rely. What's more, the Examiner allowed the claims of the '031 Patent because the prior art that was considered did not disclose unaligned channel structures. *See* Section V.C. The uncited prior art in this Petition—Kim and Tessariol—clearly disclose unaligned channel structures. As such, this Petition presents new prior art and arguments for the Board to consider. Sections IX.A.7, X.A.7.

V. THE '031 PATENT

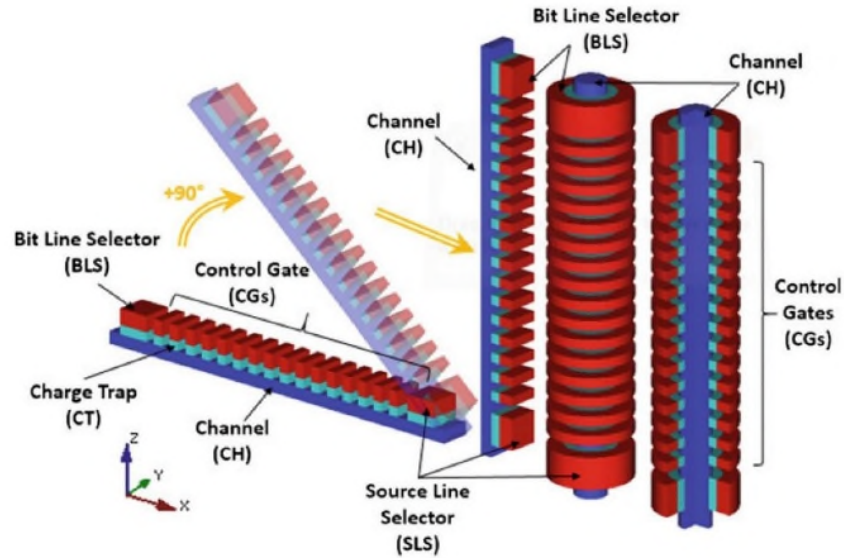
A. Technology Background

The '031 Patent and the prior art discussed in this Petition relate to three-dimensional (3D) memory devices, *e.g.*, 3D NAND memory devices. Banerjee, ¶¶ 47-53.

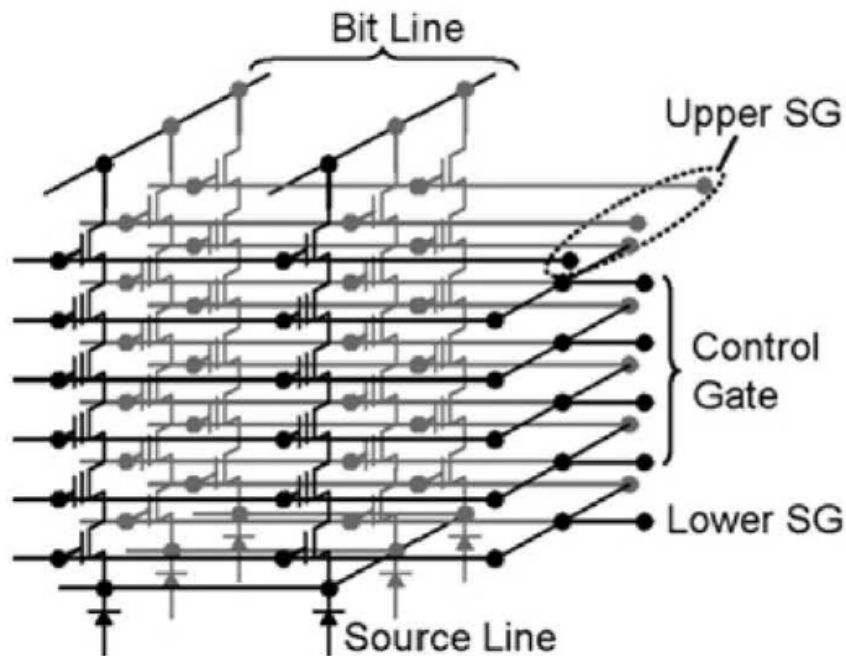
In NAND memory devices, NAND cells are arranged in “strings” with multiple cells “connected in series.” Ex. 1007, 38. Early NAND devices were formed as two-dimensional arrays of cells on a substrate surface. *Id.*, 58.



Id., 40. As shown, the cells are grouped into “page[s]” extending along the word lines and “block[s].” *Id.* “[T]o further scale down the memory cell size,” “three-dimensional (3D) NAND flash cells” were developed. *Id.*, 292. “Conceptually, a modern 3D NAND structure could be conceived by starting from the 2D NAND string building block” and “turning the 2D NAND string upside,” “resulting” in a “3D structure” with a “vertical channel.” Ex. 1008, 3.



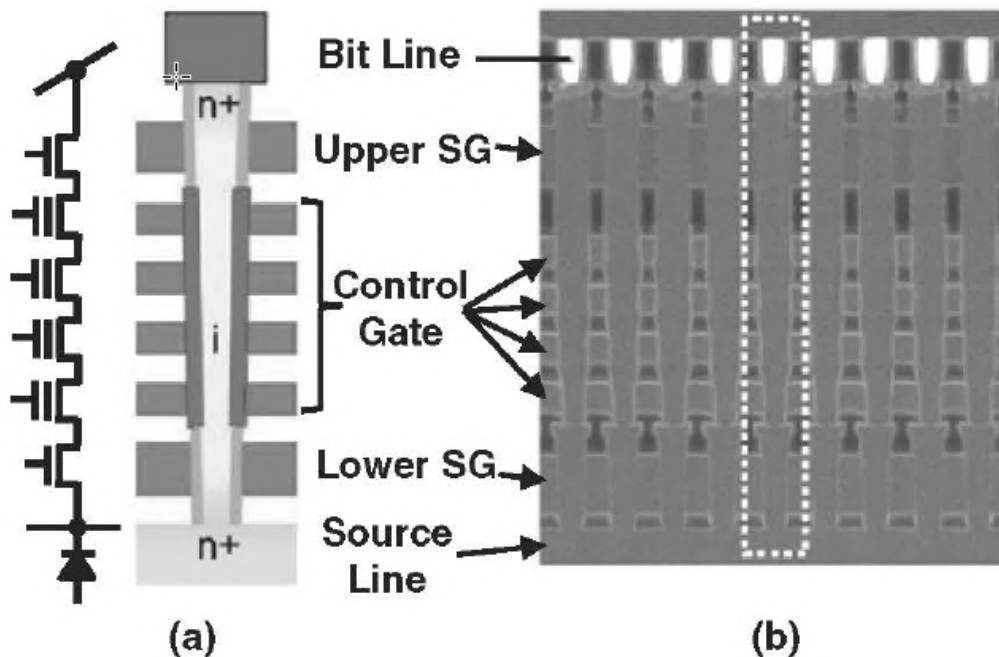
Ex. 1009, 122. Multiple such vertical channels are then repeated in a three-dimensional array:



Ex. 1007, 296; *see also* Banerjee, ¶¶ 54-55.

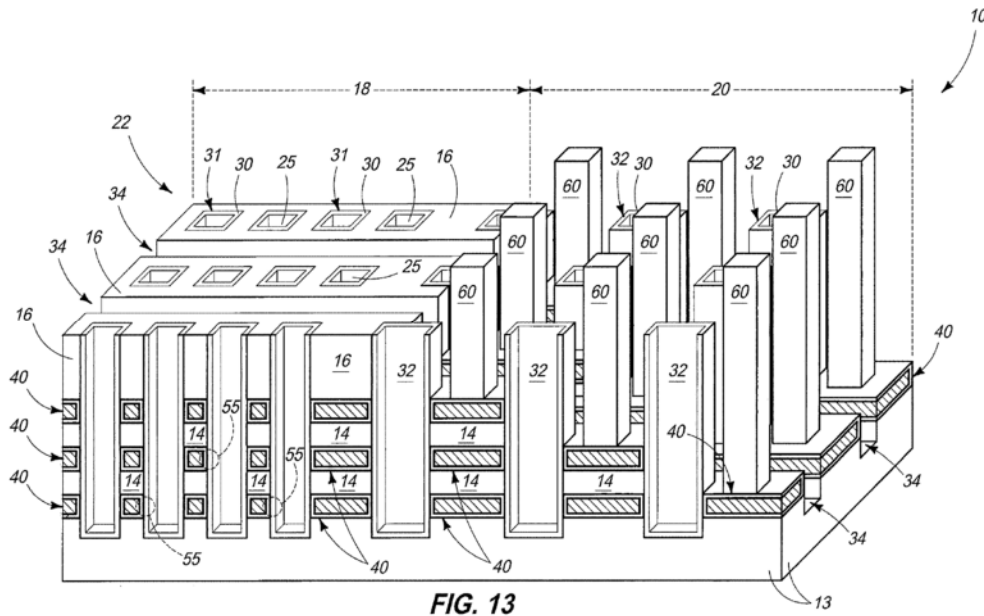
3D NAND includes “multi-stacked layers of gate (plate)” material alternated with “dielectric” in a “[s]tack.” Ex. 1007, 294. A “through-hole[]” channel (also

known as a channel structure) “filled by memory film ... and channel poly-Si” passes through the layers to form the string of vertically arranged memory cells. *Id.*, 295. “Each” layer of “electrode plate acts as a control gate.” *Id.* A particular vertical memory cell “string is selected by a bit line and an upper select gate (upper SG).” *Id.*, 295-296. A memory cell “is located in the intersection of a control gate plate” and the memory film/poly-Si channel. *Id.* The lowest layer is a “select gate (lower SG)” allowing the strings to connect to a lower “common source.” *Id.*, 295, 297. An example 3D NAND vertical memory cell string is shown below:



Id., 296; Banerjee, ¶¶ 56-57.

To access each memory cell via its control gate (also known as a word line), it was well known to use staircase structures, which provide landing areas on the control gates for contacts (below, the contacts 60 connect to different control gates):

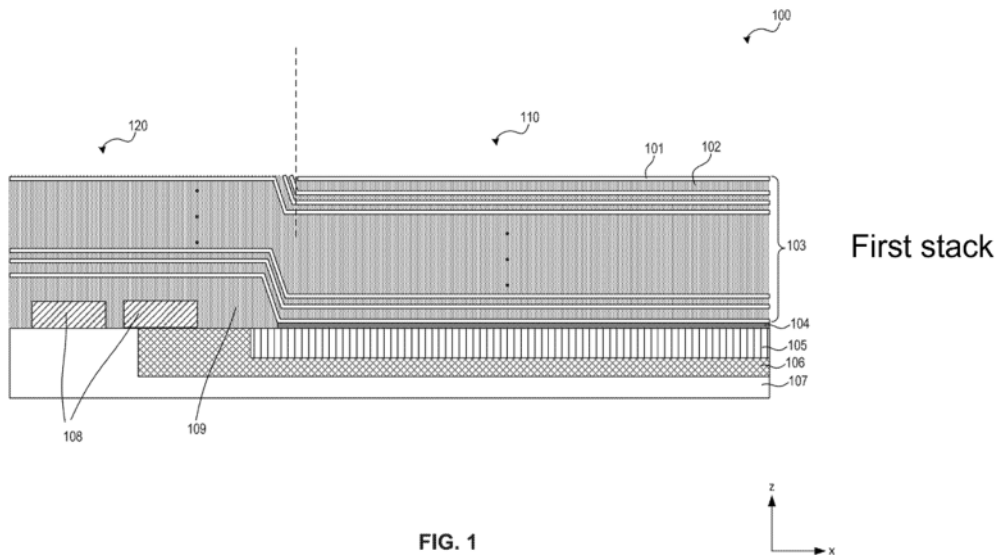


Ex. 1010 (U.S. Pat. No. 10,475,737), Fig. 13, 4:56-64, 8:45-56.

In forming such 3D NAND devices, it was known to first create an alternating stack of dielectric layers and sacrificial layers, and then later replace the sacrificial layers with conductive control gate layers. Ex. 1010, 4:25-55. Further, it was known to use supporting pillars that extend through the stack, because the supporting pillars provide mechanical support during the process of replacing the sacrificial gate layers with conductive gate layers. *Id.*, 7:44-8:3; Banerjee, ¶¶ 57-62.

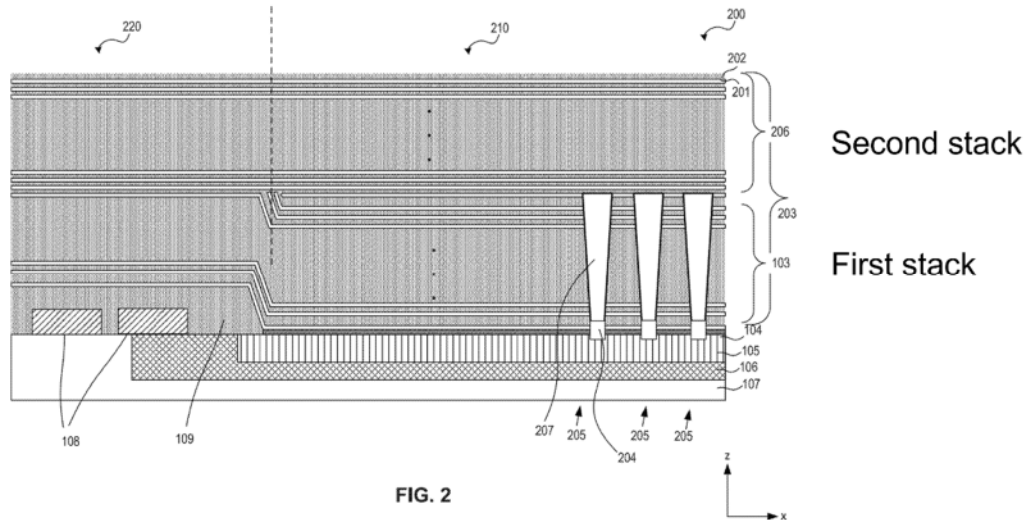
B. '031 Patent Overview

The '031 Patent relates to multiple-stack three-dimensional (3D) memory devices, *e.g.*, 3D multiple-stack NAND devices. Ex. 1001, 1:15-38. The '031 Patent admits that such devices were known. *Id.* The '031 Patent illustrates a first stack (103) of alternating dielectric and sacrificial layers (101 and 102):



Id., Fig. 1 (annotated), 11:6-34.

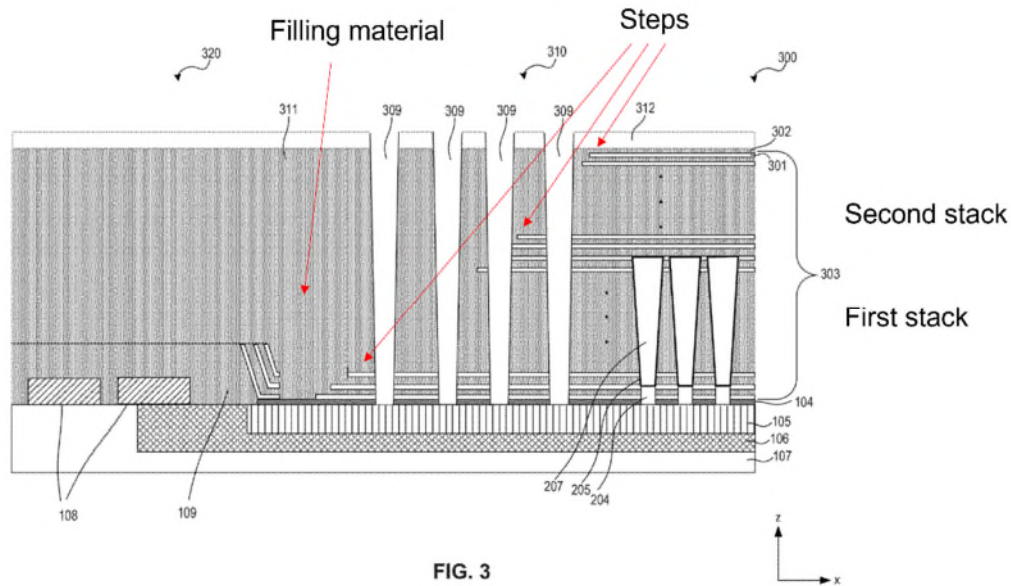
The '031 Patent discloses forming a second stack (206) of alternating dielectric and sacrificial layers (201 and 202) on top of the first stack, thereby creating a multi-stack structure:



Ex. 1001, Fig. 2 (annotated), 11:44-60, 12:65-13:10.

The '031 Patent refers to “staircase structure[s]” as “having stepped surfaces.”

Ex. 1001, 9:39-52. The '031 Patent discloses etching the multi-stack structure to form the steps for a staircase portion of each stack (which thereby becomes the “staircase structure 303,” also known as “multiple-stack staircase structure 303” or “two-stack staircase structure 303”) and depositing a filling material (311) (*e.g.*, dielectric) over the void left by forming the steps:

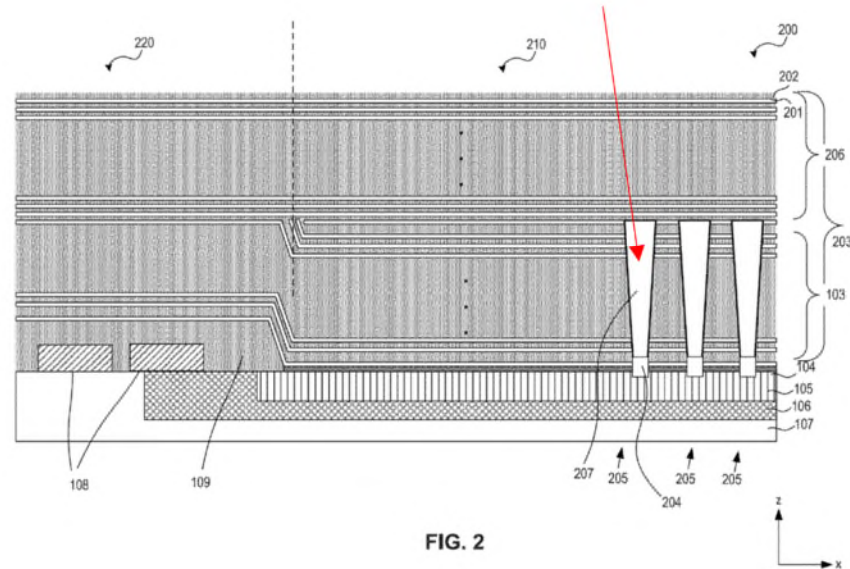


Id., Fig. 3 (annotated), 11:44-60, 12:65-13:64. As can be seen above, there is a staircase region in each stack. Banerjee, ¶¶ 65-67.

The '031 Patent alleges that in multi-stack structures, “the fabrication processes of semiconductor channels and supporting pillars are time-consuming and costly.” Ex. 1001, 1:37-38. In view of these alleged problems, as detailed below, the '031 Patent describes creating the channel structures with a two-step etch process and creating supporting pillars with a one-step etch process.

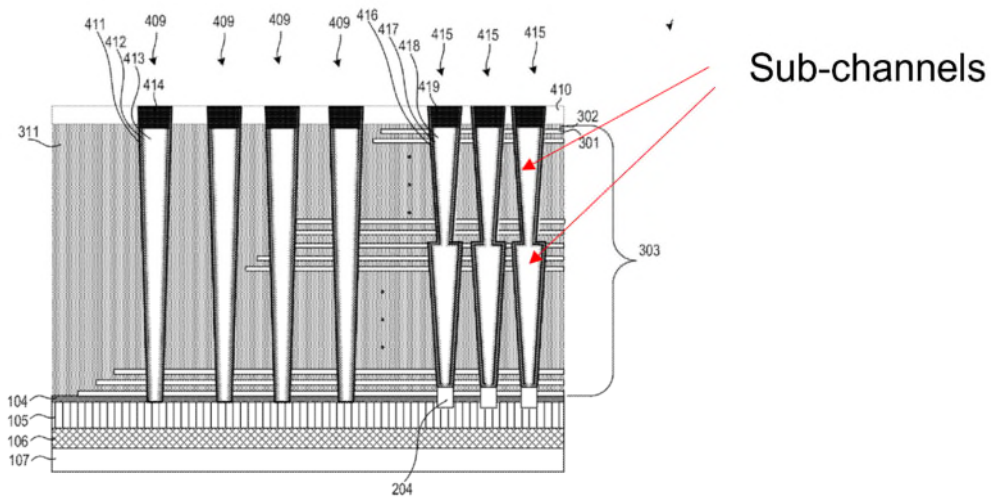
First, as shown below, the '031 Patent creates “sub-channel” structures (207), which requires a first etch in the first stack before depositing the second stack (206) on the first stack (103):

Sub-channel



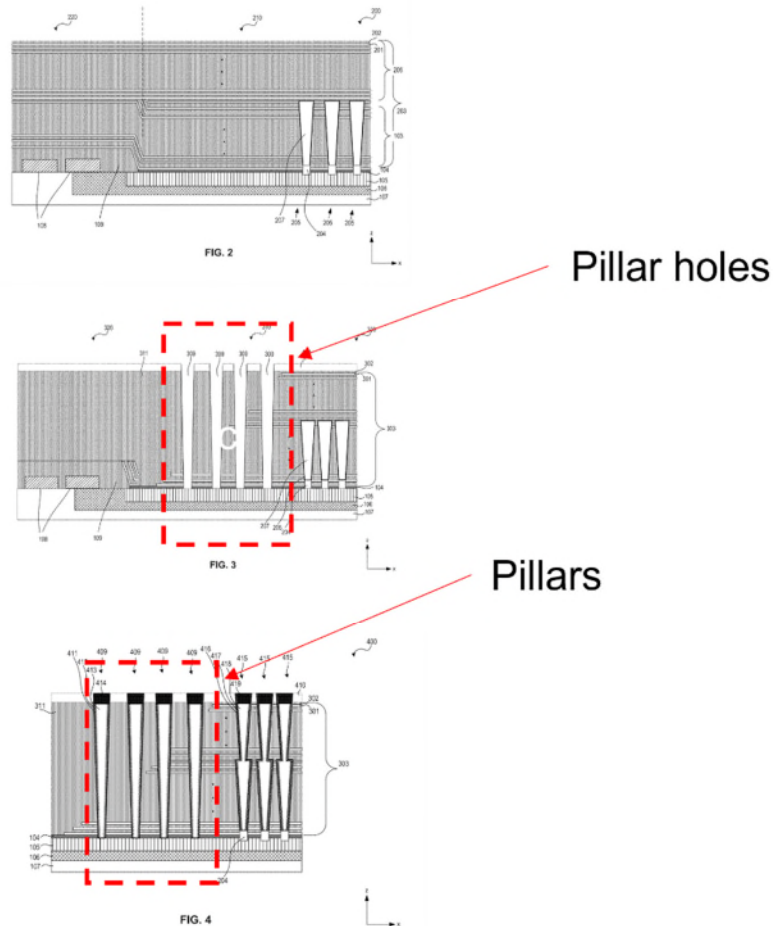
Ex. 1001, Fig. 2 (annotated), 11:44-60.

After forming the second stack (206), a second etch forms a sub-channel hole above the first sub-channel structure, and then subsequent processing ultimately creates vertical sub-channels:



Ex. 1001, Fig. 4 (annotated), 14:35-44; Banerjee, ¶¶ 68-70.

Second, unlike the process steps for forming the channels, the '031 Patent discloses forming the pillar structures with a single etch after the formation of both stacks:



Ex. 1001, Figs. 2-4 (annotated), 13:65-14:44; Banerjee ¶ 71.

As to the channel structures, the '031 Patent describes the channels as having “unaligned” sidewalls, because the formation process involves a separate etch through each stack, which creates a wider hole at the top portion of each stack. Ex. 1001, 8:32-53. The '031 Patent states that “unaligned surfaces can refer to the

inconsistent hole dimensions caused by etching holes with high aspect-ratio (e.g., greater than 4).” *Id.*, 8:41-43. In contrast, the ’031 Patent describes the pillar sidewalls as being “aligned” because, as seen above, such pillars are formed using a single etch. *Id.*, 2:45-50; Banerjee, ¶ 72.

C. Prosecution History of the ’031 Patent

On January 7, 2020, the Examiner rejected the claims as anticipated by Chae (US Publ. No. 2010/0133599). Ex. 1002, 827. On April 2, 2020, Applicant argued that Chae’s channels are “smooth and straight,” and thus are not unaligned as the claims require. *Id.*, 853. On July 1, 2020, the Examiner allowed the claims, specifically crediting Applicant’s argument that Chae fails to disclose unaligned channel sidewalls. *Id.*, 864; Banerjee, ¶¶ 73-75.

VI. CLAIM CONSTRUCTION

The Board applies the same *Phillips* claim construction standard used by district courts. *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc). For purposes of this Petition, Petitioner submits that the terms of the ’031 Patent’s claims do not require further construction and can be afforded their plain and ordinary meaning. Banerjee, ¶ 76-77.

VII. LEVEL OF ORDINARY SKILL IN THE ART

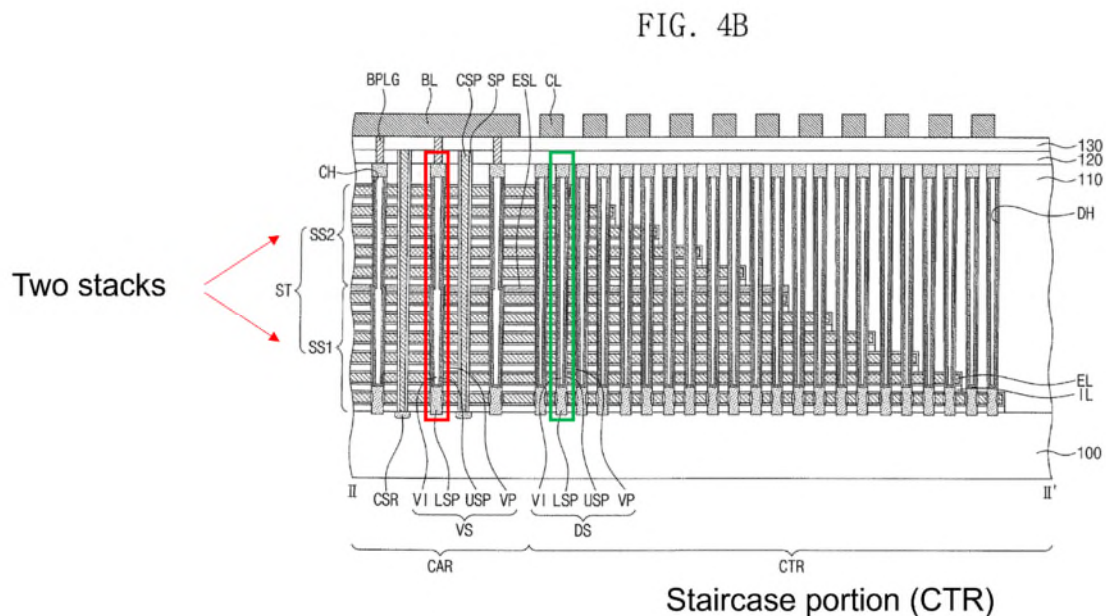
A POSITA in the field of the ’031 Patent would have had a bachelor of science degree in electrical engineering or a similar discipline, along with 2-3 years of professional experience working with (e.g., researching, designing, or teaching)

monolithic 3D structures and NAND memory devices, or an equivalent level of skill, knowledge, and experience (*e.g.*, an advanced degree may replace some of the professional experience). This POSITA would have been aware of and generally knowledgeable about 3D NAND's structure, its component parts, how it operates, and how it is controlled. Banerjee, ¶¶ 41-44.

VIII. PRIOR ART OVERVIEW

A. Kim

Kim relates to a “three-dimensional (3D) semiconductor memory device,” *e.g.*, 3D NAND memory device. Kim, 4:56-58, 8:27-29. As explained below, just like the '031 Patent, Kim discloses a multi-stack staircase structure (stacks SS1 and SS2), unaligned channel structures (CH, shown in red), and aligned supporting pillars (DS, shown in green):



Id., Fig. 4B (annotated); Banerjee ¶¶ 81-88.

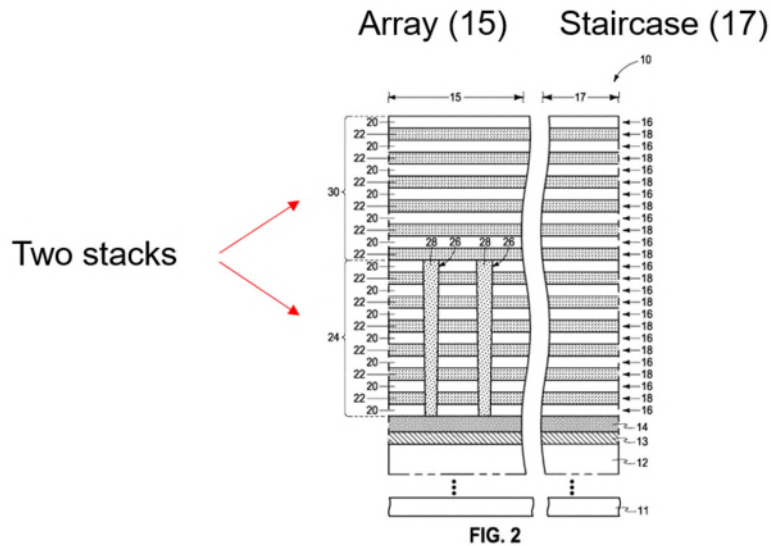
Specifically, Kim discloses “lower structure SS1” and “upper structure SS2,” which each include a staircase structure portion in region CTR, thereby forming a multi-stack staircase structure. Kim, 5:60-6:11, 6:30-40. Kim further discloses “vertical channel holes CH” through the multi-stack staircase structure (stacks SS1 and SS2) in region CAR, which may include therein “vertical structures VS,” *i.e.*, vertical channel structures comprising the memory cells. *Id.*, 7:4-24. Further, Kim discloses “dummy structures DS” that “may physically support the stack structure.” *Id.*, 9:30-38.

Importantly, just like the '031 Patent, Kim discloses that the channel structures include unaligned sidewalls, *e.g.*, “misaligned” sidewalls, because the channel structures in each stack are formed separately from those in the other stack. Kim, 11:32-35; *see also id.*, 1:44-48, Figs. 7-11. Unlike its *channel structures*, however, Kim discloses that its *support pillars* are aligned, because these pillars are formed in a single processing step after the formation of both stacks. *Id.*, 12:58-67.

B. Tessariol

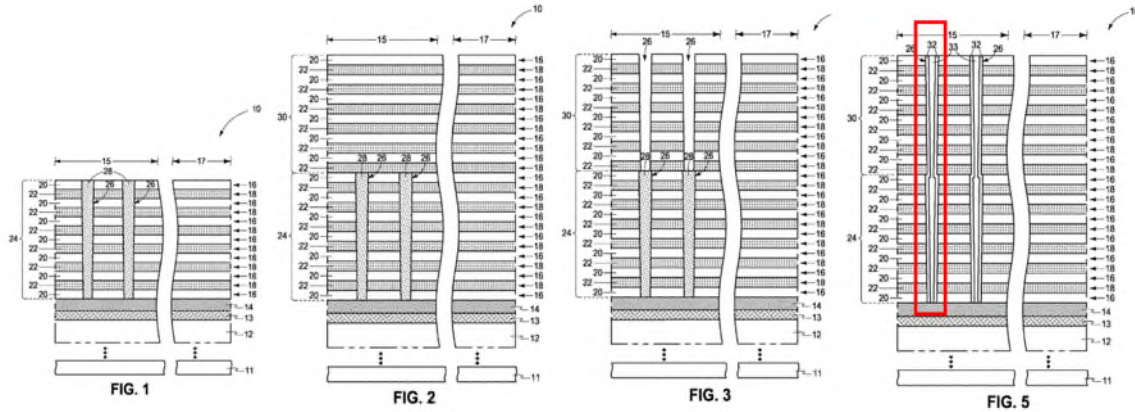
Tessariol also relates to 3D NAND. Tessariol, [0006], [0027]. As explained below, just like the '031 Patent, Tessariol discloses a multi-stack staircase structure, unaligned channel structures, and aligned supporting pillars. Banerjee, ¶¶ 89-93.

First, Tessariol discloses a multi-stack staircase structure with “first stack 24” and “second stack 30.” Both stack structures include an “array portion 15” with channel structures and an “adjacent portion 17” with a stair step portion and supporting pillars:



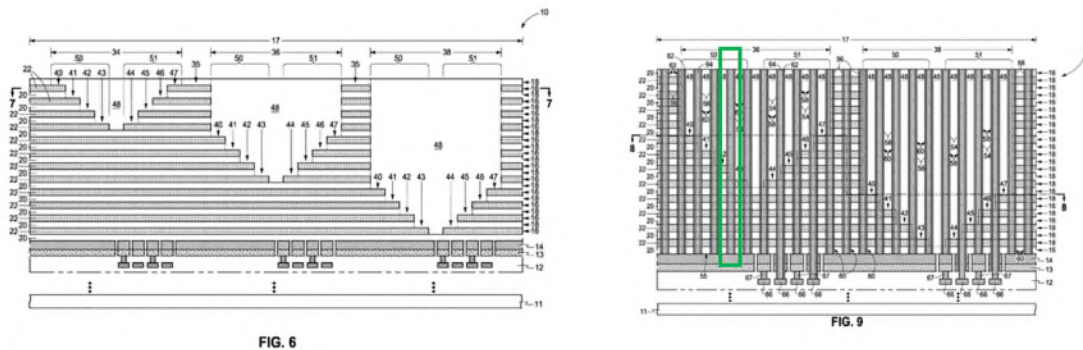
Tessariol, Fig. 2 (annotated), [0028], [0029], [0031], [0034].

Importantly, just like the '031 Patent, Tessariol discloses that its “channel” structures have unaligned sidewalls, because the channel structures are formed with two separate etch steps:



Tessariol, Figs. 1-3, 5, [0030]-[0033].

Unlike its *channel structures*, however, Tessariol discloses that its *support pillars* (“dummy-support structures 60” and “operative conductive vias 58” that function to “support” the stack structures) are aligned, because these pillars are made in one etch step after the formation of both stacks:



Tessariol, Figs. 6, 9, [0036] (forming staircase after completion of channel structures), [0037] (forming openings through both stacks with one etch), [0041] (support function).

IX. GROUND 1: INDEPENDENT CLAIM 1 AND DEPENDENT CLAIMS 2-4 ARE OBVIOUS OVER KIM

Ground 1 demonstrates that claims 1-4 are obvious in view of Kim and the knowledge of a POSITA. Banerjee, ¶ 94.

A. Claim 1:

1. [1.PRE] “A memory device comprising:”

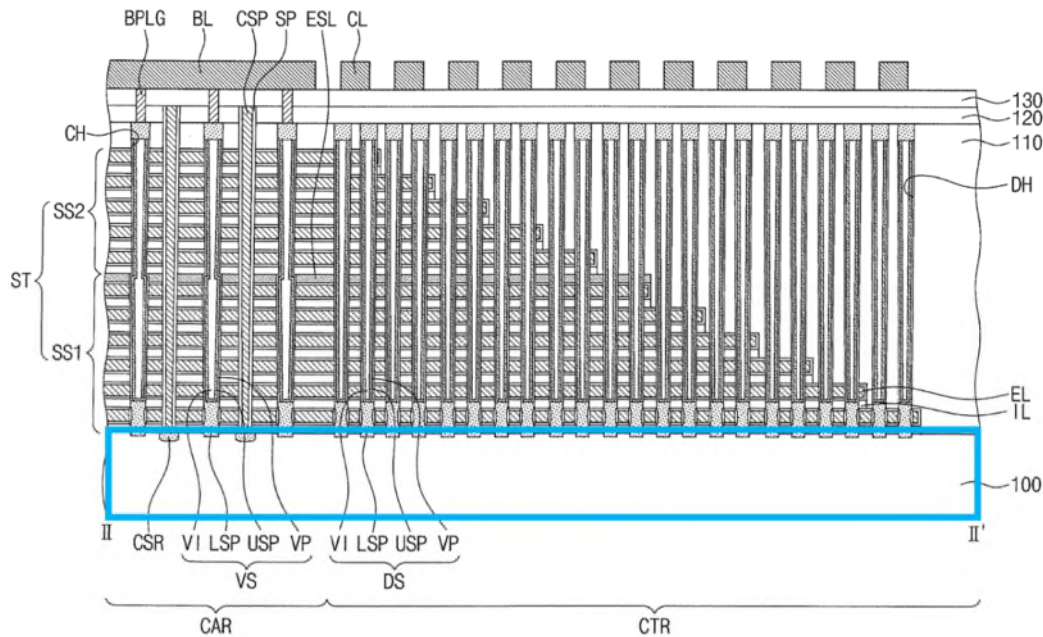
To the extent that claim 1’s preamble is limiting, Kim discloses it. Specifically, Kim discloses that “[e]mbodiments of the inventive concepts relate to . . . a three-dimensional (3D) semiconductor memory device.” Kim, 1:17-20; *id.*, 1:38-41 (disclosing “vertical semiconductor memory device structures including vertical channel structures and vertical dummy structures and methods of forming the same”). Therefore, Kim discloses a *memory device*³ (e.g., “semiconductor memory device”). Banerjee, ¶ 96.

2. [1.A] “a substrate;”

Kim discloses this limitation. Specifically, Kim discloses “a substrate 100” that includes “a cell array region CAR and a connection region CTR.” Kim, 5:53-59. The substrate 100 is shown in light blue below:

³ This Petition uses red and italics for claim language in the claim mapping for the convenience of the Board.

FIG. 4B



Id., Fig. 4B (annotated).

Thus, Kim discloses a *substrate* (e.g., substrate 100). Banerjee, ¶ 97.

3. [1.B] “a multiple-stack staircase structure comprising a plurality of staircase structures stacked over the substrate,”

Kim discloses this limitation.

As an initial matter, the '031 patent states: “‘staircase structure’ or a ‘stepped cavity structure,’ or similar refer to a structure having stepped surfaces.” Ex. 1001, 9:39-41. The claim uses *staircase structure* to refer to a structure that includes a staircase region, not to refer to only the staircase region. Similarly, *multiple-stack staircase structure* refers to the structure that includes a staircase region, not to refer to only the staircase region. This is also evident from Limitation [1.E] that requires *a semiconductor channel extending through the multiple-stack staircase structure*.

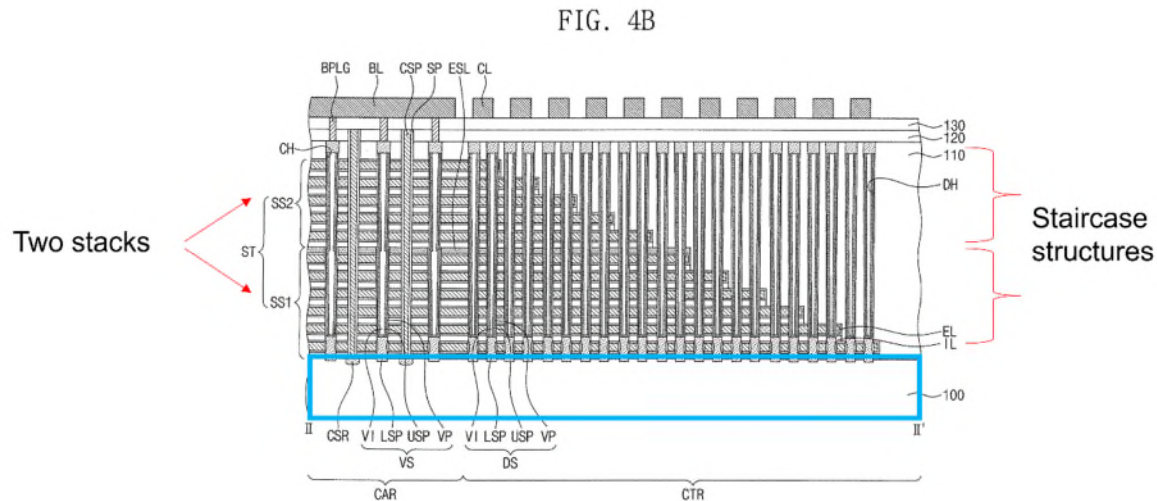
In all embodiments of the '031 patent, the semiconductor channel extends through the cell region, not the staircase region. *E.g., id.*, Fig. 12.

First, Kim discloses that its memory device is “*a multiple-stack*” structure. Specifically, Kim discloses “stack structures ST” that includes “lower structure SS1” and “upper structure SS2.” Kim, 5:60-66. Each stack structure includes “insulating layers IL and electrodes layers EL which are vertically alternately stacked (sometimes referred to as alternating electrode layers and insulating layers).” *Id.*, 5:61-6:1. Kim discloses forming the stacks separately. *Id.*, 10:50-59.

Second, Kim further discloses that its “*multiple-stack*” structure is a “*staircase structure comprising a plurality of staircase structures*.” Kim expressly discloses that “the electrodes EL are arranged in a staircase structure on the connection region CTR . . .” Kim, 9:11-13; *see also id.*, 10:60-62 (disclosing that “the mold structure MT disposed on the connection region CTR may be formed into a staircase structure”). As shown below, in the CTR region, each of the SS1 and SS2 structures include a stairstep formation on the right. Note that there is an optional ESL (etch stop layer) between the two staircase structures.⁴ *Id.*, 6:41-54, 10:8-16, 13:41-50.

⁴ Even if the ESL were always present, it would not matter, because the '031 Patent claims specify that a structure may exist between the decks. Ex. 1001, claim 6 (“a

Third, Kim discloses that the “*staircase structures*” are “*stacked over the substrate.*” Kim discloses that the upper structure is “stacked” on the lower structure, which is over the substrate (100). Kim, 10:50-59. Thus, after the staircase is formed, there are two stacked staircase structures.⁵ *Id.*



Kim, Fig. 4B (annotated).

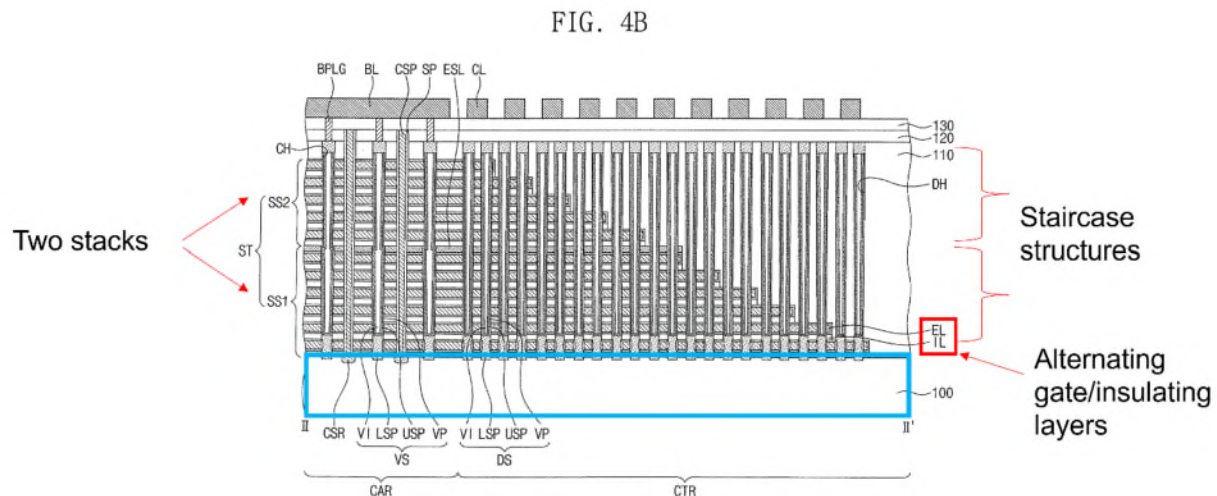
Thus, Kim discloses a *multiple-stack staircase structure comprising a plurality of staircase structures stacked over the substrate* (e.g., stack structure ST including the lower and upper structures SS1 and SS2). Banerjee, ¶¶ 99-104.

connection layer in the semiconductor channel between two adjacent staircase structures”).

⁵ Note that the '031 Patent discloses forming both stacks and then creating the multi-stack staircase structure in the same way as Kim. Ex. 1001, Figs. 2-3, 13:11-21.

4. [1.C] “wherein each of the plurality of staircase structures comprises a plurality of conductor layers, wherein each of the plurality of conductor layers is located between two insulating layers;”

Kim discloses this limitation. Specifically, the plurality of staircase structures, *i.e.*, the “lower structure SS1” and “upper structure SS2” each includes “insulating layers IL and electrodes layers EL which are vertically alternately stacked (sometimes referred to as alternating electrode layers and insulating layers).” Kim, 5:61-64. “The electrodes EL may be vertically isolated from each other by the insulating layers IL disposed there between.” *Id.*, 6:30-35. The electrode layers may be various types of conductive materials. *Id.*, 6:55-63. And the insulating layers IL “may include a silicon oxide layer.” *Id.*, 6:59-61.



Id., Fig. 4B (annotated).

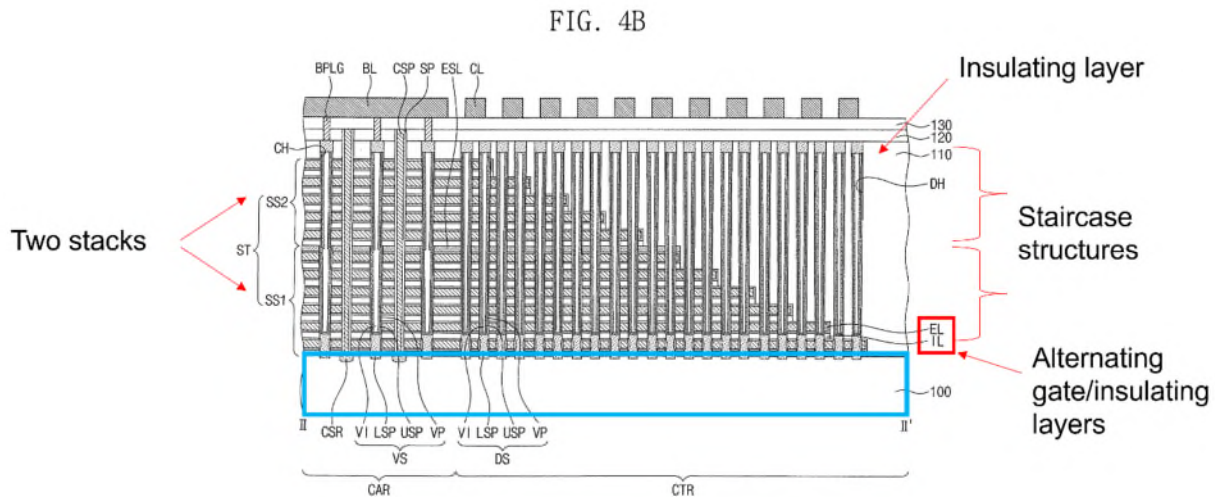
Thus, Kim discloses that the plurality of staircase structures comprises “*a plurality of conductor layers, wherein each of the plurality of conductor layers is*

located between two insulating layers” (e.g., the EL and IL layers). Banerjee, ¶¶ 105-06.

5. [1.D] “a filling structure surrounding the multiple-stack staircase structure;”

Kim discloses, or at least renders obvious, this limitation.

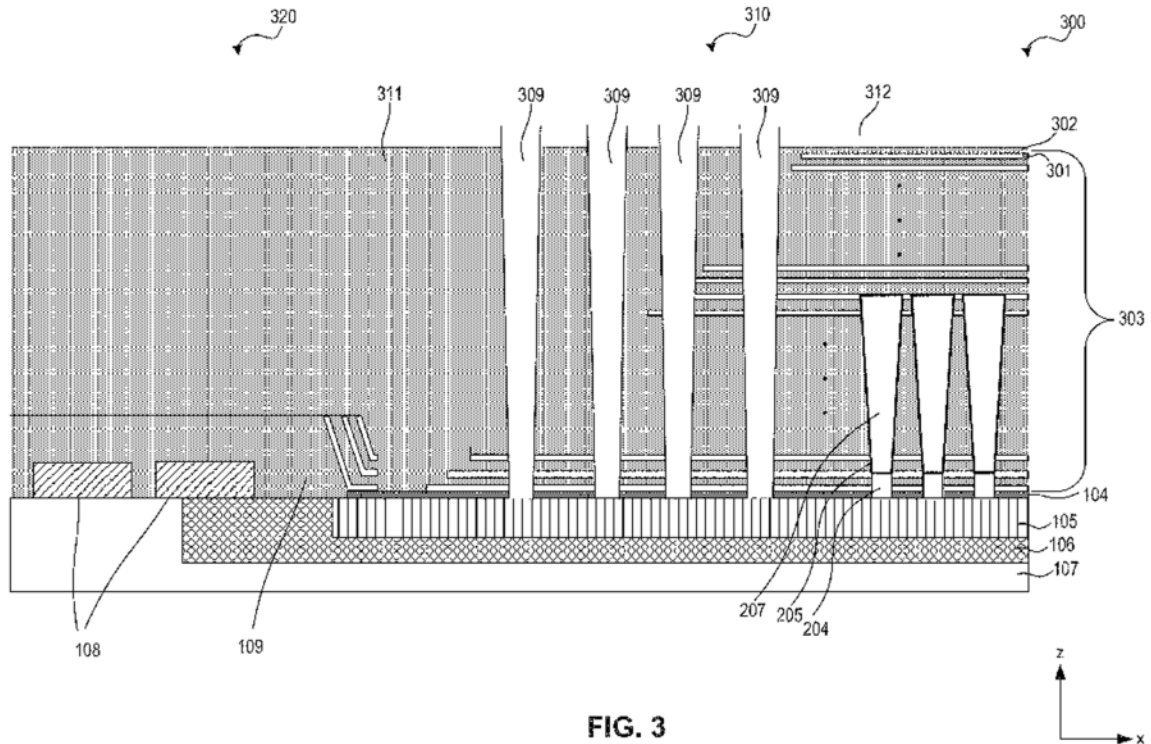
Specifically, Kim discloses a “filling insulating layer 110” that “may be disposed on the substrate 100 and may cover the stack structures ST. The filling insulation layer 110 may have a planarized top surface.” Kim, 9:53-56. More specifically, after forming the staircase structures, the insulating layer 110 fills the voids. *Id.*, 10:60-11:21, Figs. 9-10.



Id., Fig. 4B (annotated).

Kim’s filling insulating layer 110 “*surrounds*” the multi-stack structure (ST). As shown in Figure 3 below, after forming the staircase, the ’031 Patent depicts a “deposited dielectric filling material (e.g., over staircase structure 303 and isolation

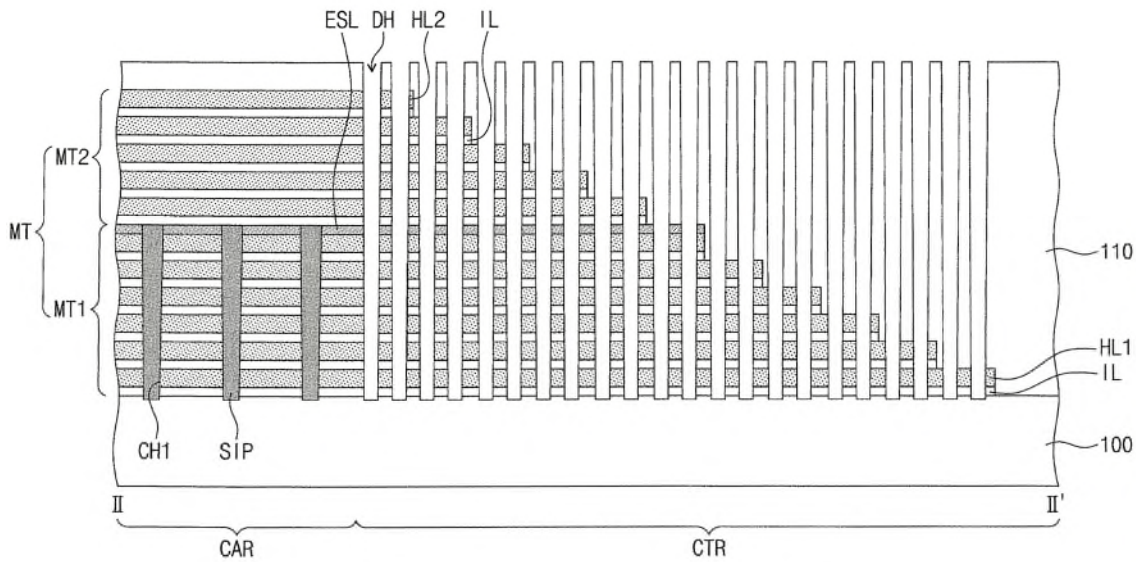
layer 109)” to form “dielectric filling structure 311 that surrounds staircase structure 303.” Ex. 1001, 13:44-48.



Id., Fig. 3.

Kim discloses the same filling material. As shown in Figure 10 below, after forming the staircase region, Kim further discloses forming insulation layer 110 to fill all voids. Kim, 11:10-21.

FIG. 10



Id., Fig. 10. Note that Figures 6-13 describe the manufacturing process and label the stacks MT1 and MT2 instead of ST1 and ST2. *Id.*, 10:4-7; Banerjee, ¶¶ 107-110.

To the extent PO argues that “surrounding” requires the dielectric filling structure be on all sides of the multi-stack staircase structure, such an interpretation is inconsistent with all embodiments of the ’031 Patent, which never describes or illustrates the filling structure on each and every side of the multi-stack structure. Regardless, Kim discloses this or at least renders it obvious for at least three reasons.⁶

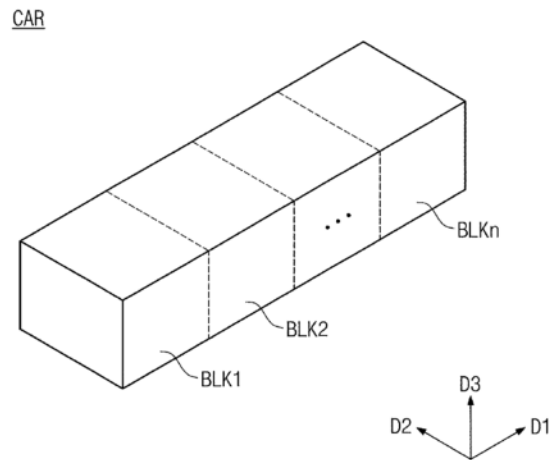
⁶ Kim does not disclose surrounding the bottom side of the staircase structure, because of course the bottom of the staircase sits on the substrate.

First, recall that Kim discloses a “filling insulating layer 110” that “may be disposed on the substrate 100 and may cover the stack structures ST. The filling insulation layer 110 may have a planarized top surface.” Kim, 9:53-56; *see also id.*, 11:11-21 (“Referring to FIGS. 3 and 10, a filling insulation layer 110 may be formed on an entire top surface of the substrate 100 to cover the mold structure MT.”). Because Kim discloses depositing the filling insulating layer onto “substrate 100” to cover the stacks and planarizing the material on the top surface, this means that the filling material will encase the memory device. Banerjee, ¶ 112.

Second, in Figure 10 above, Kim discloses filling material on the outer edge of where the staircase region ends (*e.g.*, all the way to the right). Thus, consistent with this filling pattern, it would have been understood by a POSITA, and certainly obvious, that the filling material would extend to the outer edge in the other directions, namely, on the other three sides of the structure. Banerjee, ¶ 112.

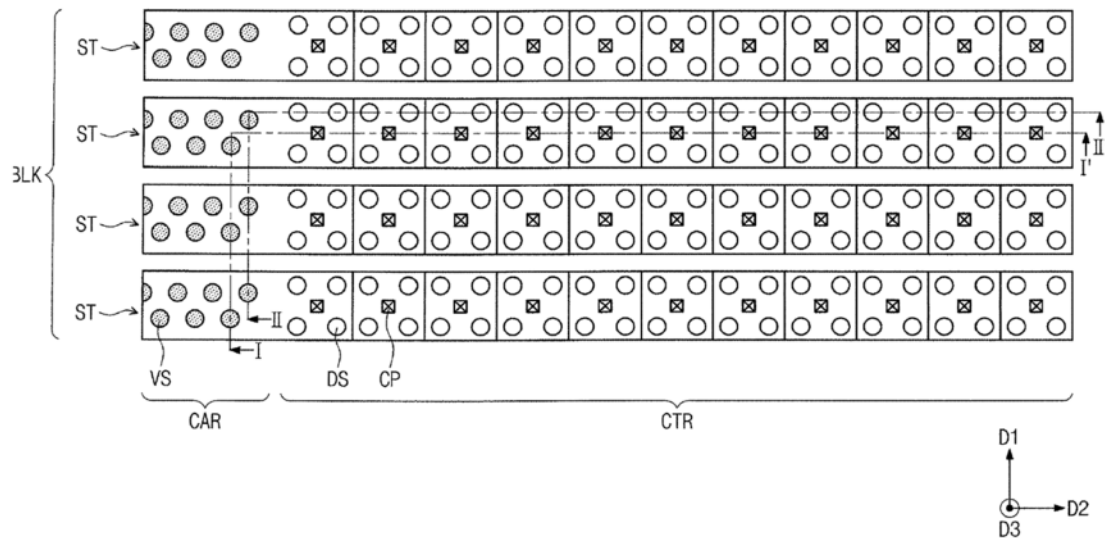
Third, in view of Figure 3 and the knowledge of a POSITA, it also would have been understood, and at least obvious, that the insulating layer 110 (or similar dielectric fill) would surround all sides of the multiple-stack structure. As shown below, Kim contemplates a multi-block memory:

FIG. 2



Kim, Fig. 2, 5:29-42. In Figure 3, Kim depicts a block:

FIG. 3



Id., Fig. 3, 5:43-52.

It was well known that with such a block arrangement, a common technique was to isolate the blocks with, *e.g.*, common source lines 102, as shown below:

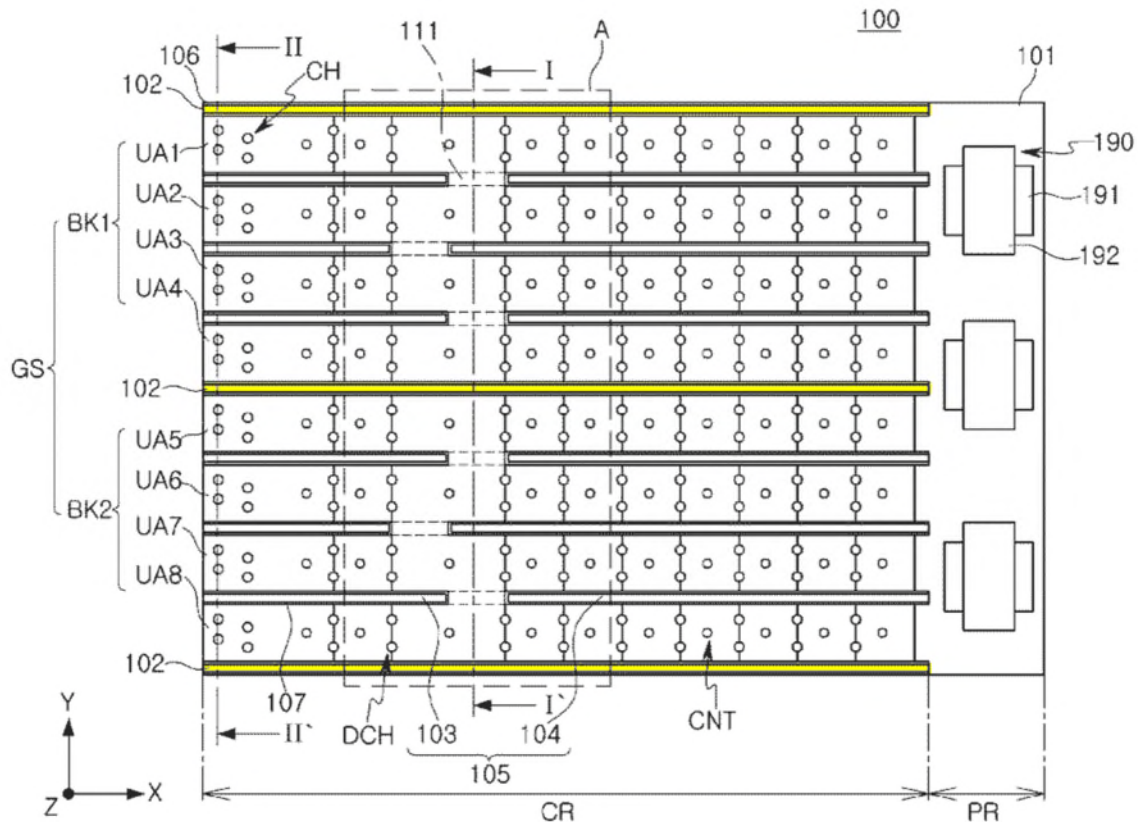


FIG. 3

Ex. 1011 (U.S. Pat. No. 10,559,583 to Park), Fig. 3. Lines 102 are structures that include an isolating liner. *Id.*, 5:65-6:12, 10:46-11:8, Fig. 11. These common source lines create, in effect, a wall with an outer portion of insulting material that runs (1) the entirety of direction 2 in Kim's Figure 3 and (2) from the substrate to the top of the multiple-stack structure. *Id.* In other words, along direction 2 of Kim, this additional insulating liner *surrounds* the multiple-stack structure. Thus, Kim would have been understood to disclose (or at least render obvious) that additional insulating material (filling structure) would exist that encases the array and staircase

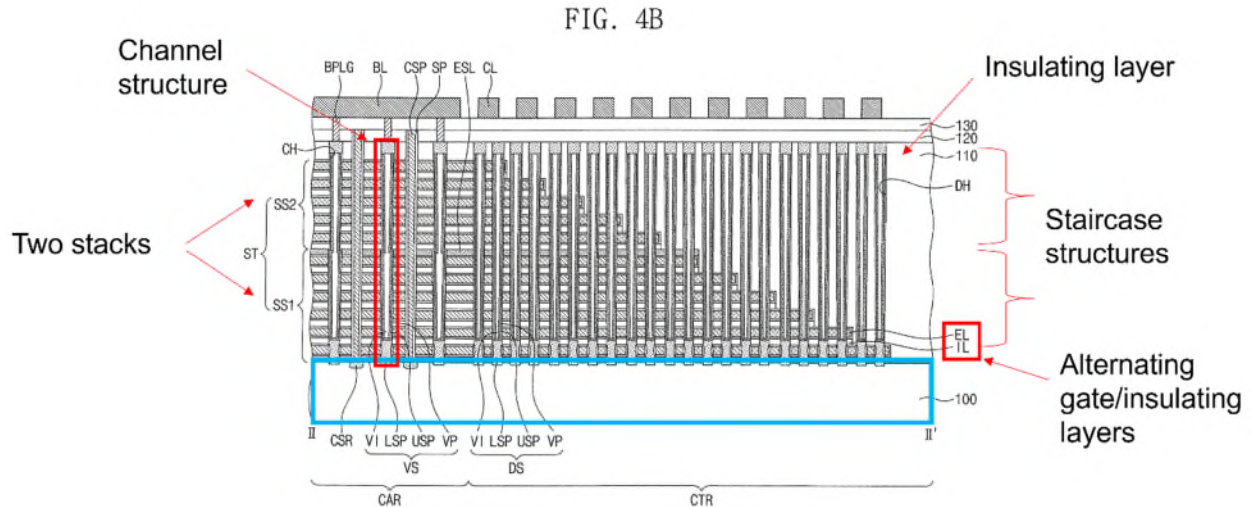
portions, resulting in a filling structure on all sides of the staircase structures. Banerjee, ¶¶ 114-117.

Fourth, as a general matter, it was well known that there is a requirement to use filling to create a planar top surface for the upper-level metal layers (each of which, in turn, require a planar layer). Banerjee ¶ 112 (citing Ex. 1023).

Thus, Kim discloses, or at least renders obvious, “*a filling structure surrounding the multiple-stack staircase structure*” (e.g., insulation layer 110).

6. [1.E] “a semiconductor channel extending through the multiple-stack staircase structure,”

Kim discloses this limitation. Specifically, Kim discloses “[a] memory cell array (or a cell array) including a plurality of memory cells may be disposed in the cell array region CAR.” Kim, 5:1-3. Kim further discloses that the cell array region CAR includes a “stack structure [ST]. . . coupled to a plurality of vertical structures [VS] (e.g., *semiconductor pillars*) to constitute memory cells three-dimensionally arranged.” *Id.*, 5:37-39 (emphasis added). More specifically, Kim discloses that these vertical memory device structures are “channels,” namely, the VS structures (see below) are “vertical channel structure[s] that vertically penetrate[] through an upper structure [SS2] and a lower structure [SS1] of a stack structure [ST] in a cell array region of the device.” *Id.*, 1:42-45.



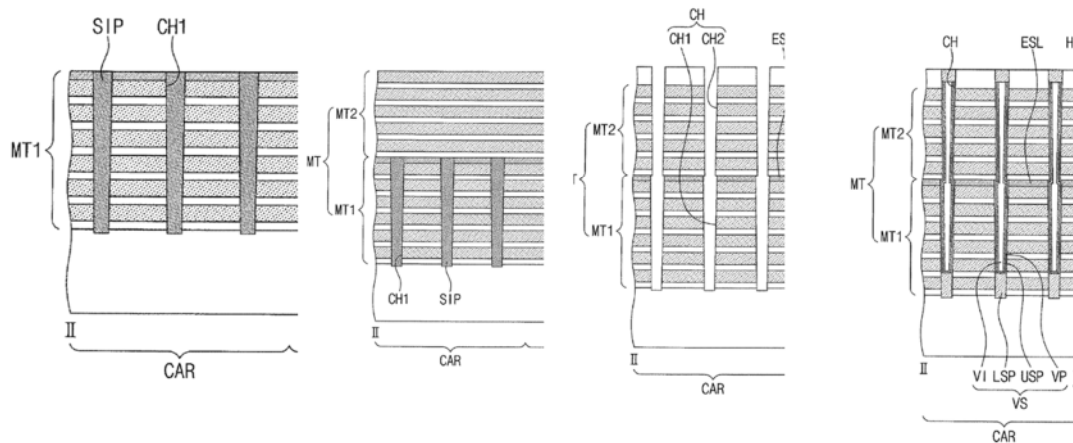
Id., Fig. 4B (annotated), 7:15-24 (semiconductor channel material).

Thus, Kim discloses a *semiconductor channel* (e.g., vertical channel structure VS) *extending through the multiple-stack staircase structure* (e.g., stack structure ST). Banerjee, ¶¶ 118-19.

7. [1.F] “wherein the semiconductor channel comprises unaligned sidewall surfaces; and”

Kim discloses this limitation. Specifically, Kim discloses that “[t]he vertical channel structure can have a side wall with a stepped profile at a level in the vertical channel structure where the upper structure meets the lower structure.” Kim, 1:45-48. Kim explains the reason for the unaligned sidewalls of the channels, namely, Kim discloses forming the channels by etching a channel hole (CH1) in the first stack, forming the second stack, then etching another hole (CH2) in the top stack, and finally forming the channel structure (VS):

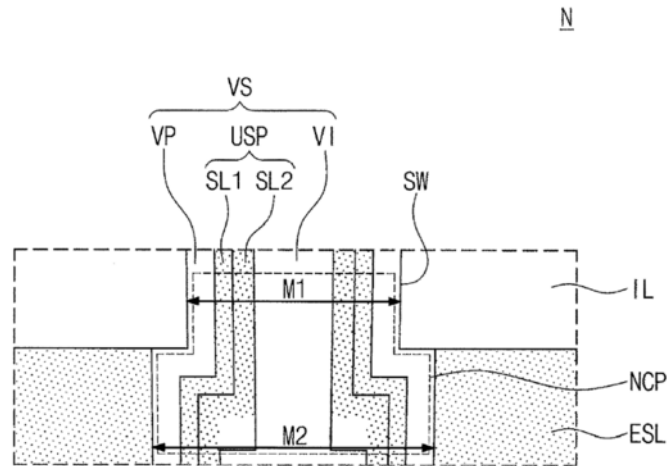
Figures 7, 8, 11, 12



Id., Figs. 7, 8, 11, 12 (figures are all partial), 10:26-12:9.

As a result of the two-step etch process, Kim explains that the top portion of the sub-channel in the first stack (CH1 in MT1) will have a wider diameter than the bottom portion of the sub-channel in the second stack (CH2 in MT2). Kim, 7:65-8:20. Kim refers to interface region as the “NCP” area, and expressly discloses “[t]he diameter of the portion NCP may increase [sic] (sharply) at an interface the upper structure SS2 and the lower structure SS1.” *Id.*, 8:15-17. Kim depicts these unaligned sidewall surfaces of the channel in Figure 5B:

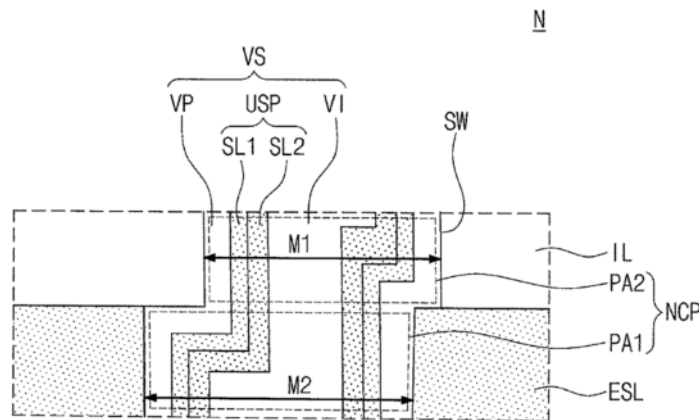
FIG. 5B



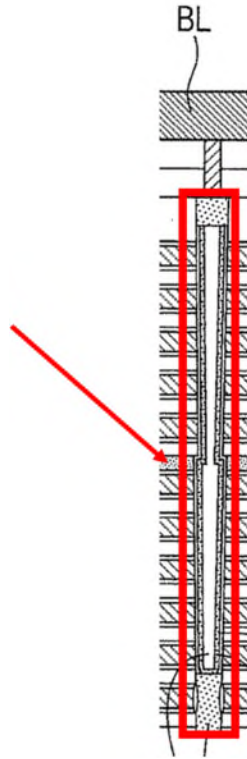
Id., Fig. 5B.

Kim further discloses in other embodiments that “the second channel holes CH2 may be misaligned with the first channel holes CH1 when the second channel holes CH2 are formed (see FIG. 5C).” Kim, 11:32-35.

FIG. 5C



Id., Fig. 5C. A POSITA would have understood that Kim’s processes, namely, the two separate etch steps, result in the unaligned sidewall surfaces. Banerjee ¶¶ 120-21. The unaligned sidewall channel surfaces can be seen in Figure 4B as well:



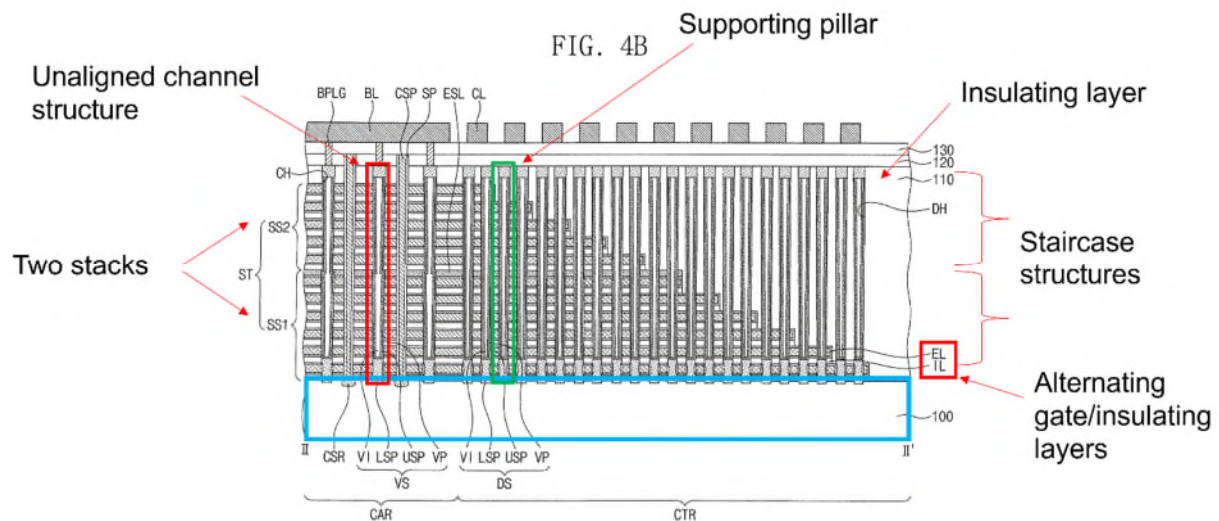
Kim, Fig. 4B (partial and annotated).

Thus, Kim *discloses semiconductor channels comprising unaligned sidewall surfaces* (e.g., the channel structures, namely, vertical structures VS). Banerjee, ¶¶ 120-123.

8. [1.G] “a supporting pillar extending through at least one of the multiple-stack staircase structure and the filling structure,”

Kim discloses this limitation. As an initial matter, and consistent with the plain and ordinary meaning of the term, the '031 Patent uses “supporting pillar” to refer to a tall vertical column that functions to support the stack. Ex. 1001-7:22-25.

Kim discloses “dummy structures DS may physically support the stack structures ST on the connection region CTR.”⁷ Kim, 9:30-31; 16:60-62 (same). The dummy structures DS “penetrate through the staircase structure.” *Id.*, 1:49-50. More specifically, recall that the CTR region is a region of the multiple-stack staircase structure. *Id.*, 9:4-19. Kim discloses that “[a] plurality of dummy holes DH may penetrate a filling insulation layer 110 and the stack structure ST on the connection region CTR. A dummy structure (sometimes referred to as a vertical dummy structure) DS may be provided in each of the dummy holes DH, respectively.” *Id.*, 9:20-24.



Id., Fig. 4B (annotated).

⁷ A POSITA would have understood that Kim refers to the dummy structures as providing “support” because these structures support, *e.g.*, the stack, during the sacrificial gate layer removal. Kim, 9:30-31, 10:8-16; Banerjee, ¶ 125.

Thus, Kim discloses *supporting pillars* (e.g., dummy structures DS) *extending through at least one* (both) of the *multiple-stack staircase structure* (e.g., stack structure ST, including lower structure SS1 and upper structure SS2) and the *filling structure* (e.g., filling insulation layer 110). Banerjee, ¶¶ 124-27.

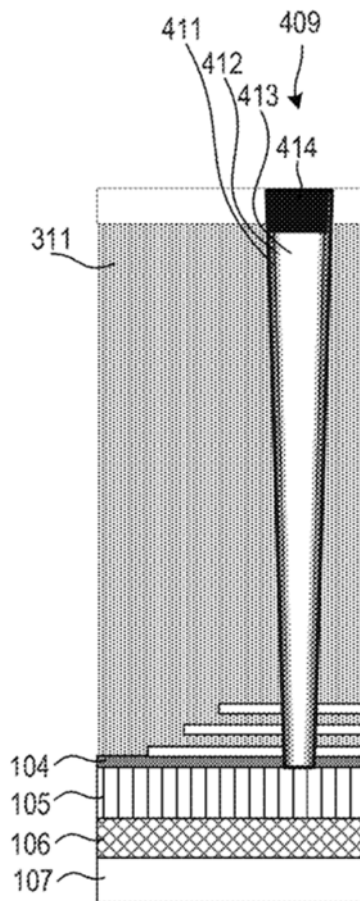
9. [1.H] “wherein the supporting pillar comprises aligned sidewall surfaces.”

Kim discloses this limitation. Specifically, Kim discloses that “[a] diameter of the dummy structure DS may become progressively less toward the substrate 100. The diameter of the dummy structure DS may become continuously less from the upper structure SS2 to the lower structure SS1. In other words, unlike the vertical structure VS described above, the diameter of the dummy structure DS may not be sharply changed, rather a side wall of the dummy structure DS may have a planar profile.” Kim, 9:39-46.

More specifically, unlike the process that Kim uses to form the vertical channel structures VS, Kim discloses forming the supporting pillars (dummy structures DS) in a one-step etching process after formation of the multi-stack structure ST: “[i]n the manufacturing method according to some embodiments of the inventive concepts, the dummy holes DH may be formed by one etching process after the formation of the lower mold structure MT1 and the upper mold structure MT2 [(stack structure ST)]. Thus, the process of forming the dummy holes DH may be simpler than the process of forming the channel holes CH, which includes two

etching processes (i.e., the etching process for forming the first channel holes CH1 and the etching process for forming the second channel holes CH2).” Kim, 12:58-67. Because of this one-etch process (unlike the two-step process to form the channel structures), Kim discloses that “the vertical dummy structure can have a side wall with a planar profile at the level where the upper structure meets the lower structure.” *Id.*, 1:51-53.

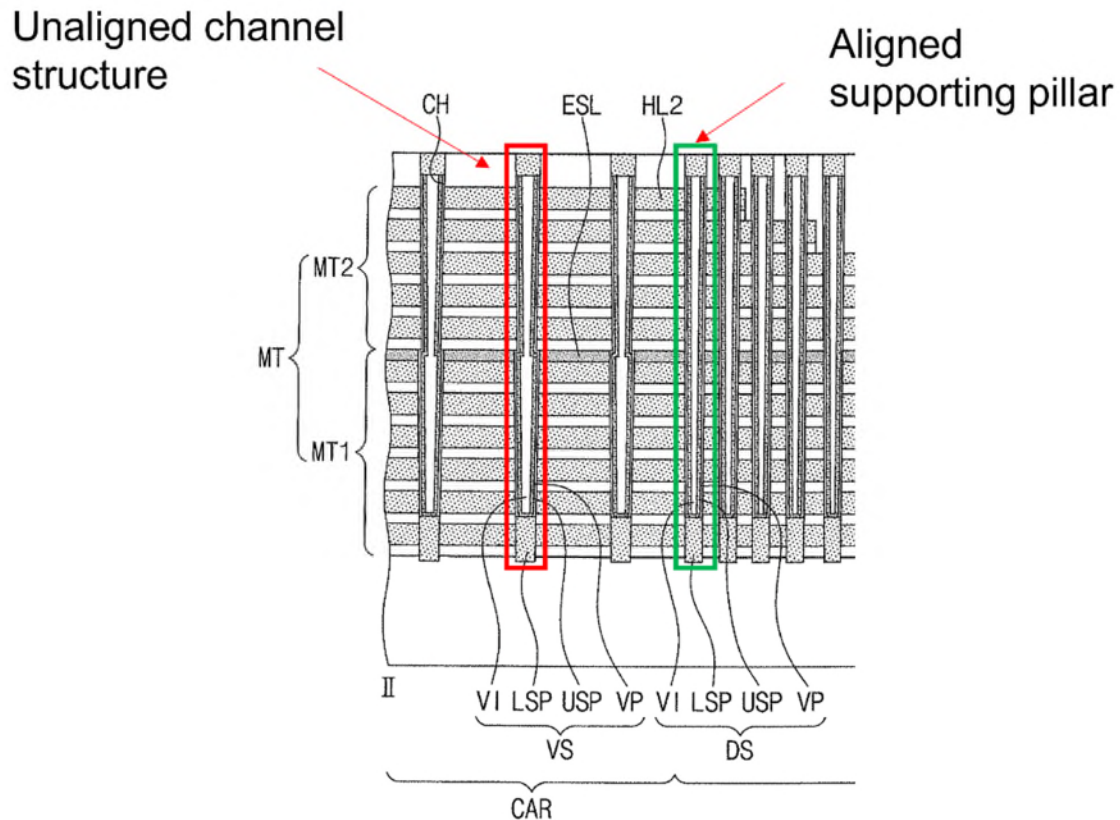
Kim’s pillars have the same profile as the ’031 Patent:



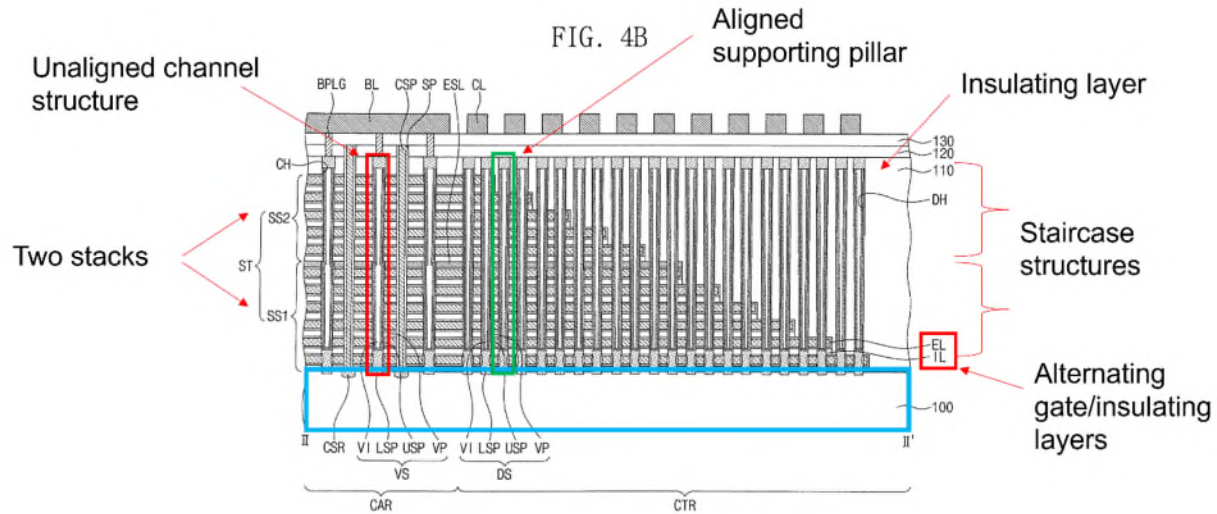
Ex. 1001, Fig. 4 (partial), 9:4-12 (“[p]illar holes through the multiple-stack staircase structure can be formed after the formation of the multiple-stack staircase structures

by one patterning process. Pillar holes can be formed . . . after the formation of the channel holes of the upper dielectric stack”); *see also* Banerjee, ¶¶ 128-32.

The contrast between the aligned dummy structures and unaligned channel structures is best seen in Figure 12 of Kim but is also clearly present in Figure 4B:



Kim, Fig. 12 (partial and annotated).



Id., Fig. 4B (annotated).

Thus, Kim discloses *supporting pillars* (e.g., dummy structures DS) comprising *aligned sidewall surfaces*.

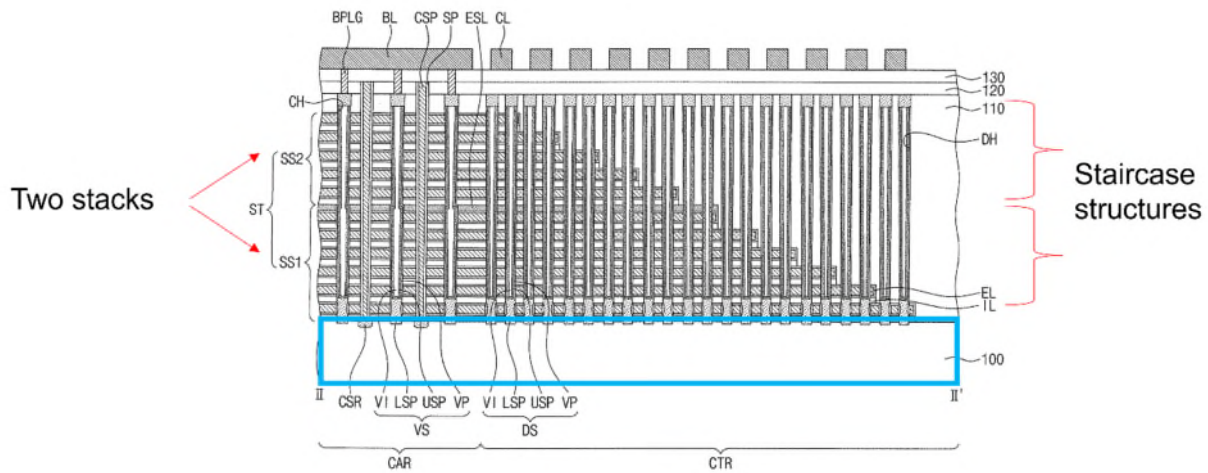
B. Claim 2:

Claim 2 depends on claim 1 and further requires:

1. [2.A] “the multi-stack staircase structure comprises a first staircase structure over the substrate and a second staircase structure over the first staircase structure; and”

Kim discloses this limitation. Specifically, as the analysis under limitation [1.B] demonstrates, Kim discloses that the upper staircase structure (SS2) is “stacked” on the lower staircase structure (SS1), which is over the substrate (100), and each structure includes a staircase portion in the CTR region. Kim, 10:50-59; Banerjee, ¶ 134.

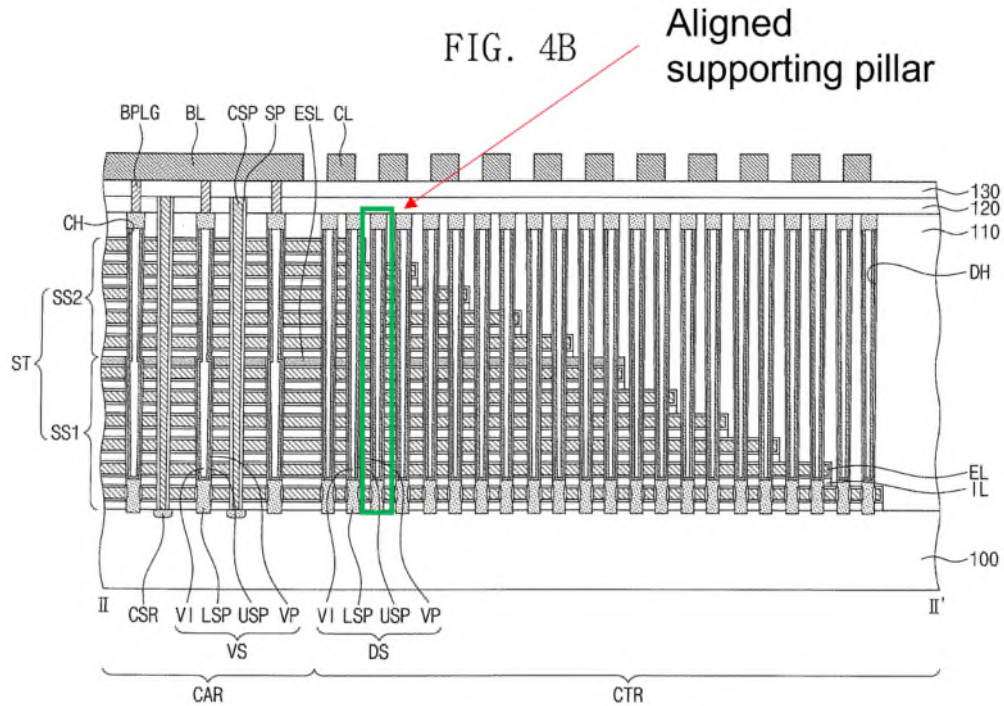
FIG. 4B



Kim, Fig. 4B (annotated).

2. [2.B] “the supporting pillar extends from a top surface of the second staircase structure to a bottom surface of the first staircase structure.”

Kim discloses this limitation. As the analysis under limitation [1.G] demonstrates, Kim discloses that the dummy structures (DS) are supporting pillars. Note that the pillars include an LSP (lower semiconductor pattern) region. Kim, 9:32-34, 11:54-62. As can be seen, the dummy structures extend from the top of the second staircase structure to the bottom of the first staircase structure (and into the substrate):



Id., Fig. 4B (annotated); Banerjee, ¶ 135.

C. Claim 3:

Claim 3 depends on claim 2 and further requires:

1. [3.A] “the supporting pillar and the semiconductor channel comprise same filling layers; and”

Kim discloses this limitation. Specifically, Kim discloses that in some embodiments, “[e]ach of the vertical structures VS may include a vertical insulating layer VP, an upper semiconductor pattern USP, a lower semiconductor pattern LSP, and a filling insulation pattern VI” (Kim, 7:16-19), and that “[e]ach of the dummy structures DS may include a vertical insulating layer VP, an upper semiconductor pattern USP, a lower semiconductor pattern LSP, and a filling insulation pattern VI, like the vertical structure VS (i.e., the vertical dummy structures and the vertical

channel structures may include the identical layers in some embodiments)” (*id.*, 9:32-38). Banerjee ¶ 135.

2. [3.B] “the supporting pillar and the semiconductor channel are each filled with at least one of a charge trapping film, a semiconductor channel film, and a dielectric core.”

Kim discloses, or renders obvious, this limitation. As the analysis above for limitation [3.A] demonstrates, the pillar and channel structures may be made with identical layers. The subsections below address each separate claim element with reference to disclosures about the channel structures (VS), but the dummy structures may include these same materials. Kim, 9:32-38.

a. Charge trapping film

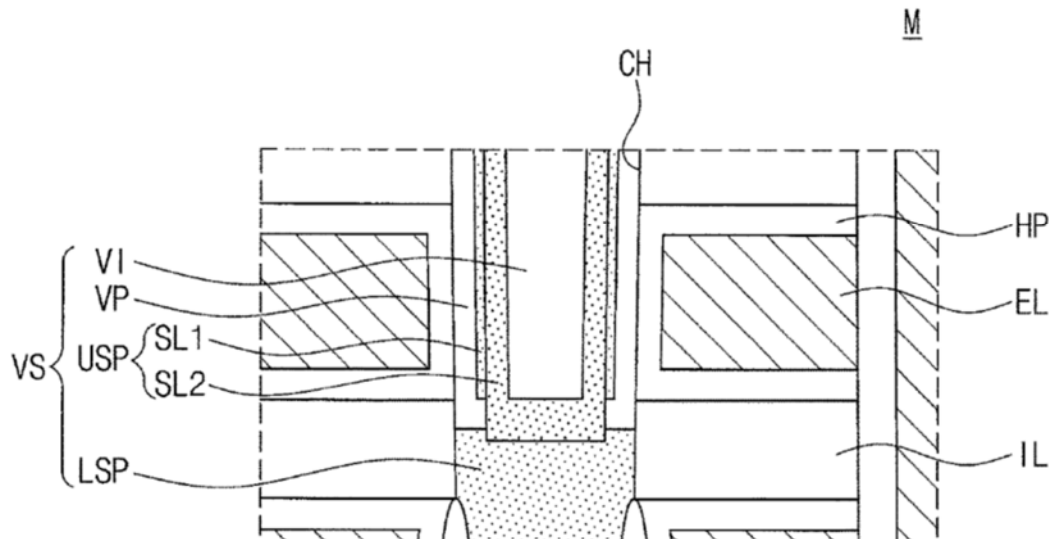
Kim discloses this limitation.

As an initial matter, the '031 Patent discloses that the charge trapping film 416 “is deposited over the sidewall of the channel holes and pillar holes” and can include “*a storage unit layer* (memory layer) over and surrounded by the block dielectric layers for trapping charges and forming a plurality of charge storage regions along the z axis,” and “*a tunneling layer* (e.g., tunneling dielectric) over and surrounded by the memory layer,” wherein “[c]harge tunneling can be performed through the tunneling layer under a suitable electric bias” occurs. Ex. 1001, 15:44-57 (emphasis added); *see also id.*, Fig. 4. The storage unit layer “can include a charge trapping material ... (e.g. silicon nitride).” *Id.*, 16:17-20. And the tunneling

layer “can include silicon oxide, silicon nitride, silicon oxynitride, dielectric metal oxides, dielectric metal oxynitride, dielectric metal silicates, alloys, and/or other suitable materials.” *Id.*, 16:24-28.

Kim discloses the same. With reference to Figure 5A below, Kim discloses that its 3D memory device may be a NAND flash memory device with a “data storage layer,” which comprises horizontal insulating layers HP and the vertical insulating layer VP, disposed between the electrodes (gate layers), wherein the data storage layer includes a charge storage layer and a tunnel insulating layer. Kim, 8:23-33.

FIG. 5A



Id., Fig. 5A (partial).

Kim further discloses that the charge storage layer “may include a silicon nitride layer, a silicon oxynitride layer, or a silicon-rich nitride layer,” and the tunnel

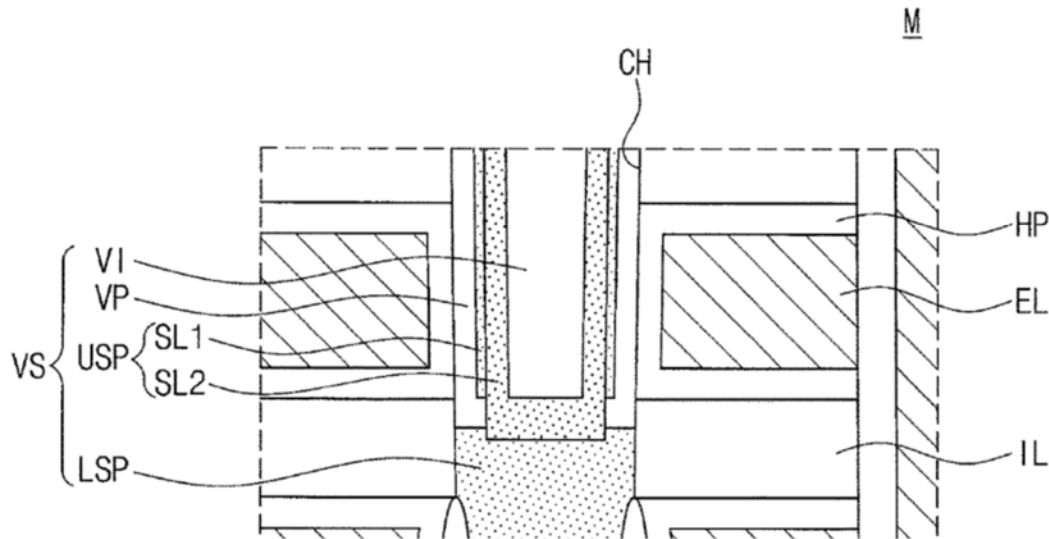
insulating layer “may include a material of which an energy band gap is greater than that of the charge storage layer” and “may include at least one of a high-k dielectric layer (e.g., an aluminum oxide layer or a hafnium oxide layer) or a silicon oxide layer.” Kim, 8:42-51. These exemplary materials for Kim’s charge storage layer overlap with those materials set forth by the ’031 Patent and would have been understood to be a charge trapping film. Ex. 1001, 15:44-57, 16:17-20. Further, Figures 4-5 of Kim disclose a continuous charge storage layer, which confirms a charge-trap memory. Ex. 1020, 105 (charge trap), 145 (conductive floating gates); Banerjee, ¶¶ 139-46.

b. Semiconductor channel film

Kim discloses this limitation. As an initial matter, the ’031 Patent discloses that “a semiconductor channel film 417 can be formed over the charge trapping film in the channel holes and pillar holes,” and can include “one or more layers of any suitable semiconductor materials such as silicon, silicon germanium, germanium . . . and/or other suitable semiconductor materials.” Ex. 1001, 16:32-38.

Kim discloses the same. As shown below, Kim discloses an upper semiconductor pattern USP, including first and second semiconductor patterns SL1 and SL2, that “may cover an inner side wall of the vertical insulating layer VP [a component of the data storage]” (Kim, 7:21-23), and “may include silicon (Si), germanium (Ge) or a mixture thereof” (*id.*, 7:54-57).

FIG. 5A



Id., Fig. 5A (partial).

These exemplary materials for Kim's SL1 and SL2 overlap with those set forth by the '031 Patent and would have been understood to be a semiconductor channel film. Ex. 1001, 15:44-57, 16:17-20; Banerjee, ¶ 147-49.

c. Dielectric core

Kim discloses, or renders obvious, this limitation. As an initial matter, the '031 Patent discloses that "a dielectric core 418 can be formed by depositing a suitable dielectric material over semiconductor channel films in channel holes and pillar holes," that "[d]ielectric core 418 can fill the space at the center of the channel hole and the pillar hole," and that "[d]ielectric core 418 can include a suitable dielectric material such as silicon oxide." Ex. 1001, 16:49-55.

Fig. 1 is a cross-sectional view of a semiconductor device. The device features a central channel (CH) surrounded by a gate stack. The gate stack includes a channel layer (CH) and a gate dielectric layer (VS). The gate dielectric layer (VS) is composed of a first layer (VI) and a second layer (VP). The channel layer (CH) is divided into two regions (SL1 and SL2) by a central barrier layer (LSP). The channel layer (CH) is also surrounded by a gate dielectric layer (HP) and a gate dielectric layer (EL). The gate dielectric layer (HP) is composed of a first layer (IL) and a second layer (SP). The gate dielectric layer (EL) is composed of a first layer (CSP) and a second layer (CSR). The device is formed on a substrate (100).

It would have been understood, and certainly obvious, that the insulating pattern inside the center of the hole is a dielectric material. First, Kim describes other “insulating” features expressly as being made with dielectric materials. Kim, 6:59-61, 8:42-51. Second, it was conventional to use “a core filler dielectric” to fill the middle of charge-trap memory cell strings. Ex. 1016 (U.S. Pat. No. 9,142,302), 7:33-52; *see also* Ex. 1020, 105 (describing core filler). Indeed, Kim

already discloses depositing dielectric materials into pillar holes, illustrating its ease. Kim, 8:42-51. Further, use of dielectric materials, such as silicon oxide, was advantageous because of its compatibility with semiconductor processing. Banerjee ¶¶ 150-51.

D. Claim 4:

Claim 4 depends on claim 2 and further requires:

1. [4.A] “the supporting pillar and the semiconductor channel are filled with different filling layers; and”

Kim discloses this limitation. Kim states “[i]n some embodiments . . . each of dummy structures DS may include a dummy pattern. A layer or component of each of the dummy structures DS [*supporting pillar*] may be different from the layer(s) or component(s) of each of the vertical structures VS [*semiconductor channel*].” Kim, 13:28-33. Further, as the below demonstrates, it would be obvious for the dummy structures to be made with completely different filling materials than the channel, namely, made with a metal core.

2. [4.B] “the supporting pillar is filled with at least one of an insulating material and a pillar-support material surrounded by the insulating material,”

Kim discloses renders obvious this limitation.

Kim discloses embodiments wherein the dummy structure DS is different than the channel structures. Kim, 13:28-33. Given the knowledge of a POSITA, a POSITA would have understood that Kim’s dummy structures could have been

made with a conductive core (the supporting material) and insulating liner. Banerjee, ¶ 156 (citing Ex. 1012). For example, Tessariol discloses that supporting pillars may be either conductive vias or dummy versions of the conductive vias. Tessariol, [0037], [0038], [0041]. Accordingly, it would have been obvious simply to use conductive vias or dummy vias (which have an insulating liner and conductive core), and this would have been beneficial because the process to form them would use the same process steps as the conductive vias. Banerjee, ¶ 157. In addition, because it was known, as taught by, *e.g.*, Tessariol, that supporting pillars could be either dummy support pillars (here, inactive conductive vias) or active conductive vias (here, active conductive vias), the supporting pillar as an active conductive via beneficially could serve two roles (support and interconnect) and reduce the need for additional structures. *Id.*

3. [4.C] “and the semiconductor channel is filled with at least one of a charge trapping film, a semiconductor channel film, and a dielectric core.”

Kim discloses semiconductor channels filled with at least one of a charge trapping film, a semiconductor channel film, and a dielectric core for the reasons set forth above for limitation [3.B].

X. GROUND 2: INDEPENDENT CLAIM 1 AND DEPENDENT CLAIMS 2 AND 4-5 ARE OBVIOUS OVER TESSARIOL

Ground 2 demonstrates that claims 1, 2, and 4-5 are obvious in view of Tessariol and the knowledge of a POSITA. Banerjee, ¶ 159.

A. Claim 1:

1. [1.PRE] “A memory device comprising:”

To the extent the preamble is limiting, Tessariol discloses it. Tessariol discloses that “[e]mbodiments disclosed herein pertain to devices, to methods used in forming a circuit structure, and to methods used in forming an array of elevationally-extending transistors and a circuit structure adjacent thereto.” Tessariol, [0001]. Tessariol describes its embodiments in the context of “a construction 10.” *Id.*, [0027]. Construction 10 would have been understood to be a memory device. For example, Tessariol discloses that construction 10 may include “memory cells.” *Id.*, [0042]. An embodiment of construction 10 is a 3D NAND.

Thus, Tessariol discloses a *memory device* (e.g., construction 10). Banerjee, ¶ 160.

2. [1.A] “a substrate;”

Tessariol discloses this limitation. Specifically, as shown below in light blue, Tessariol discloses that “construction 10 comprises a base substrate 11.” Tessariol, [0027].

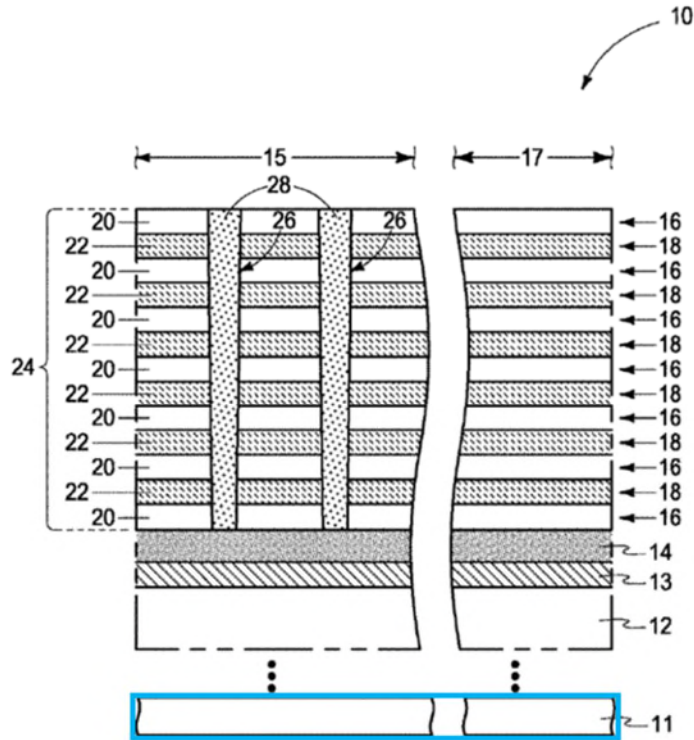


FIG. 1

Id., Fig. 1 (annotated).

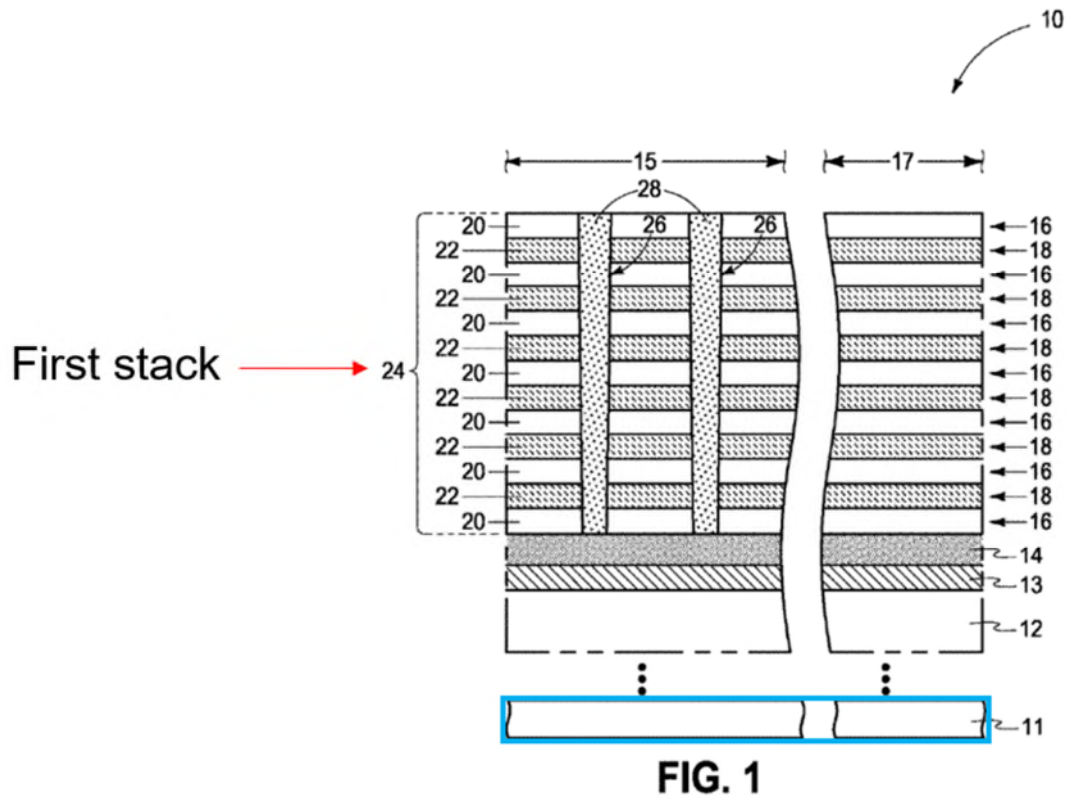
Thus, Tessariol discloses a *substrate* (e.g., base substrate 11). Banerjee ¶ 161.

3. [1.B] “a multiple-stack staircase structure comprising a plurality of staircase structures stacked over the substrate,”

Tessariol discloses, or at a minimum renders obvious, this limitation.

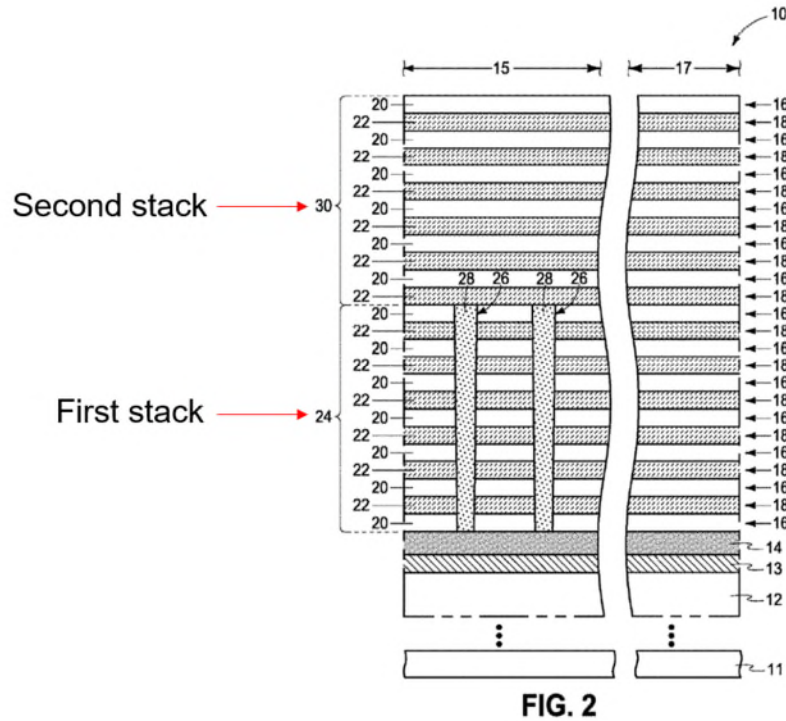
First, Tessariol discloses “*a multiple-stack staircase structure comprising a plurality of staircase structures.*” Tessariol begins its discussion by stating that “[t]he discussion largely proceeds with a fabrication method forming two stacks.” Tessariol, [0028]. Specifically, Tessariol discloses a multiple-stack structure that includes “vertically-alternating tiers 16 and 18 of different composition first [20] and second materials [22], with the vertically-alternating tiers comprising an array

portion [15] and a portion adjacent to the array portion [17].” *Id.* As shown below, Tessariol discloses first forming “a **first stack 24** of vertically-alternating tiers 16 and 18.” *Id.*, [0029] (emphasis added).



Id., Fig. 1 (annotated).

Then, as shown below, Tessariol discloses forming “a **second stack 30** of vertically alternating tiers 18, 16, of different composition materials 22, 20 . . . over first stack 24.” Tessariol, [0031] (emphasis added).



Id., Fig. 2 (annotated).

The two stacks each comprise a region 17 (*see* above) that is the staircase portion of Tessariol’s multi-stack structure, and Tessariol discloses exemplary staircases in Figures 6-7: “FIGS. 6 and 7 show an expanded, yet reduced-scale, version of adjacent portion 17 as comprising three stair step structures 34, 36, and 38.” Tessariol, [0034].

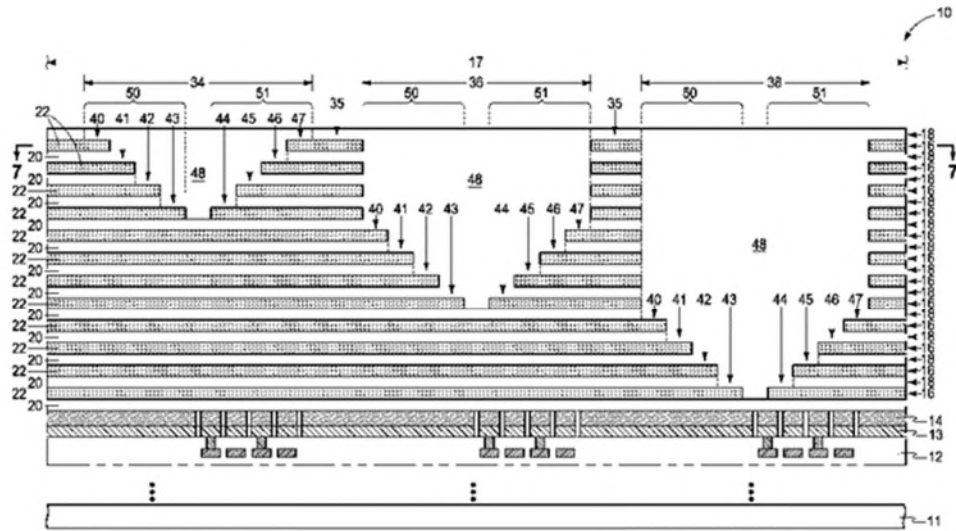


FIG. 6

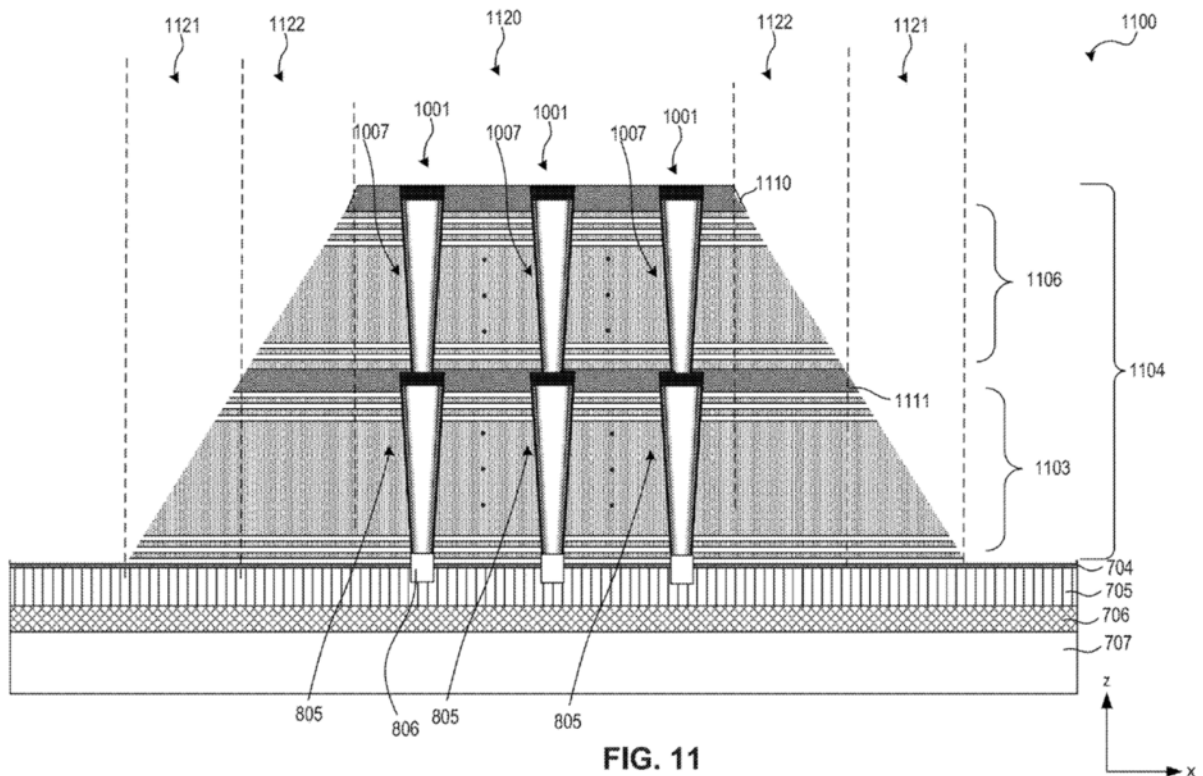
Id., Fig. 6.

The '031 Patent notes that “[a] ‘stack’ refers to a pile of objects, arranged along a designated direction.” Ex. 1001, 7:12-13. As the above demonstrates, Tessariol discloses two such stacks, each of which comprises a staircase portion, thereby forming a “*multiple-stack staircase structure comprising a plurality of staircase structures.*” Banerjee, ¶¶ 163-70.

To the extent PO argues that claim 1 is limited to one staircase portion with continuous steps for each stack of a multi-stack structure, *i.e.*, only two staircase portions in a two-stack structure, PO would be incorrect, because the claim language does not limit the type of “staircase structure.” And the '031 patent states: “‘staircase structure’ or a ‘stepped cavity structure,’ or similar refer to a structure having stepped surfaces.” Ex. 1001, 9:39-41. In other words, the '031 patent does not

define “staircase structure” to correspond to only one step region per stack or to a continuous series of steps. Regardless, Tessariol would have been understood to disclose one staircase of continuous steps per stack and it certainly would have at least been obvious. Notably, Tessariol discloses that “[a]dditionally, only one stair step structure, two stair step structures, or more than three stair step structures may be formed. Such may be formed by any suitable existing or yet-to-be-developed technique, with photolithographic patterning and etch being one example.” Tessariol, [0034]. Tessariol further discloses “[i]n one embodiment and as shown, stair step structures 34, 36, and 38 individually comprise opposing first and second sets/ flights 50, 51, respectively, of steps 40-47. Alternately, by way of examples only, only one flight of steps may be formed” *Id.*, [0035]. As Ground 1 explains, Kim discloses two staircase portions corresponding to two stacks and demonstrates the knowledge of a POSITA. *See* Section IX.A.3. Accordingly, in view of Tessariol’s option of two stair step structures and single-flight staircases, and knowledge of a POSITA (*e.g.*, Kim’s exemplarily two-staircase structure), it at least would have been obvious to employ two staircase portions, one for each stack, with continuous steps (one flight) for each stack. And it would have been routine to implement, as Tessariol expressly recognizes that many such options are available and readily applicable to its invention. Banerjee, ¶¶ 170-72.

Second, Tessariol discloses that its “*staircase structures [are] stacked over the substrate.*” As an initial matter, the claims do not include any requirement that the staircase regions of the *staircase structures* be vertically aligned. And more generally, the '031 Patent uses “*stacked*” in this context to refer to the staircase structures (each having a staircase region) being on top of each other; it does not require that the staircase regions of those structures be on top of each other. This is evident in Figure 11 of the '031 Patent:



Ex. 1001, Fig. 11.

As shown above, there is a “first staircase region 1121” and “second staircase region 1122.” Ex. 1001, 22:27-32. As can be seen, the upper staircase region of

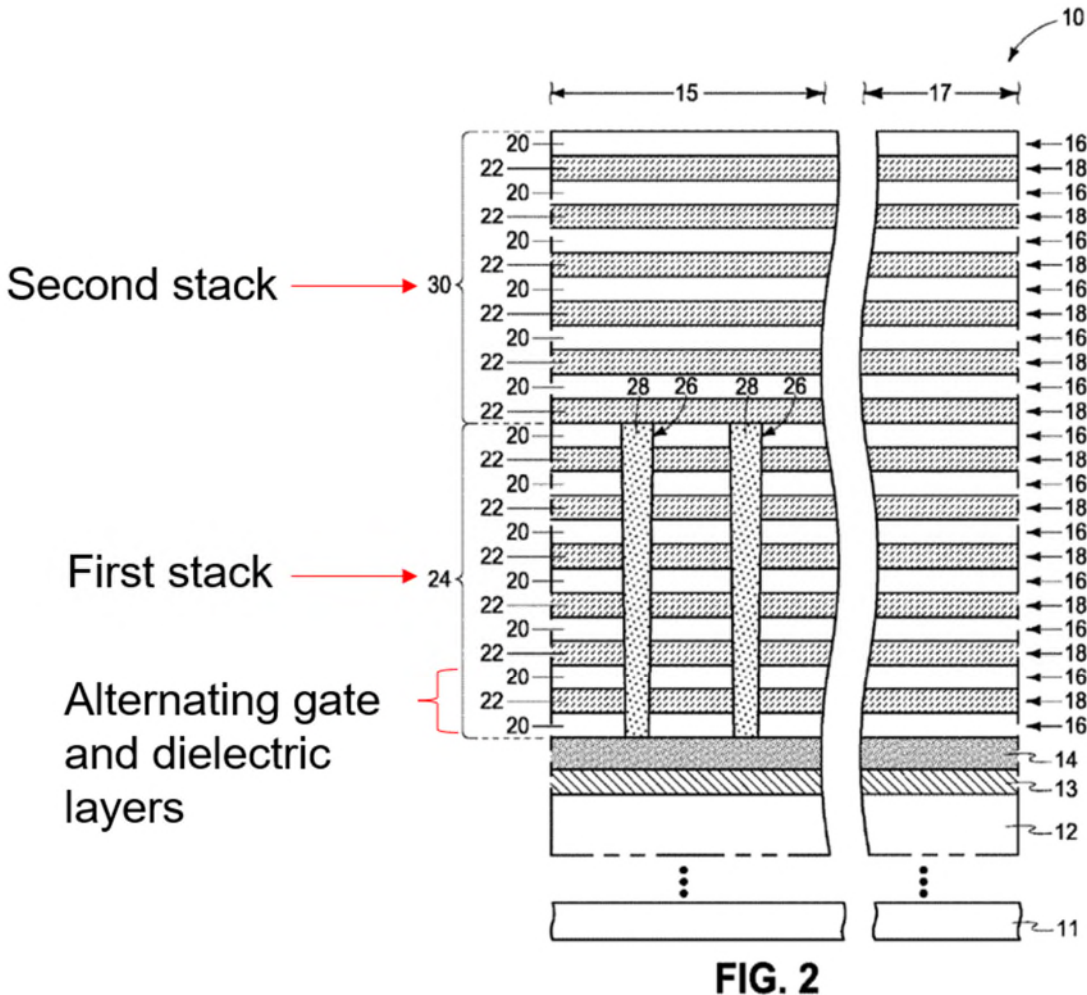
stack structure 1106 is not on top of the lower staircase region of stack structure 1103. But both stacks include a staircase region and thus are staircase structures, and one staircase structure is on top of the other. The discussion above demonstrates that Tessariol discloses the same stacks, each with a staircase structure, one on top of the other. Banerjee, ¶¶ 173-74.

Thus, Tessariol discloses, or at least renders obvious, a *multiple-stack staircase structure* (e.g., first stack 24 and second stack 30, having staircase regions, e.g., 34, 36, 38) *comprising a plurality of staircase structures* (e.g., the first stack 24 and second stack 30, both of which have staircase regions, e.g., 34, 36, 38 or the two staircase variation) *stacked over the substrate* (e.g., base substrate 11).

4. [1.C] “wherein each of the plurality of staircase structures comprises a plurality of conductor layers, wherein each of the plurality of conductor layers is located between two insulating layers;”

Tessariol discloses this limitation. Specifically, first and second stacks 24 and 30, which include staircases (e.g., stair step regions 34, 36, and 38), include “[v]ertically-alternating tiers 16 and 18 of different composition first and second materials 20 and 22.” Tessariol, [0029]. Tessariol discloses that “[i]deally, materials 20 and 22 are of the same relative compositions with respect to one another in first stack 24 and second stack 30.” *Id.*, [0031]. Tessariol further discloses that “[f]irst material 20 comprises an insulative material” and “[s]econd material 22 . . . may comprise any one or more of conductive, semiconductive, and insulative materials.

Id., [0029]. The first material layers surround the second material layers (which are gate lines):



Id., Fig. 2 (annotated).

Note that the layers 22 are etched away and replaced with gate layers 72. Tessariol, [0041] (“FIGS. 11-13 show the void space (not shown) resulting from etching away material 22 (not shown) as having been filled with conductive material 72 (e.g., metal material). Steps 40-47 now comprise conductive steps due to presence

of conductive material 72 and that are at least partially elevationally separated from one another by insulative material 20.”).

Thus, Tessariol discloses a *plurality of staircase structures* (e.g., the first stack 24 and second stack 30, both of which have staircase regions, e.g., 34, 36, 38 or the two staircase variation) comprising a *plurality of conductor layers*, (e.g., tiers 18 composed of second material 22) *wherein each of the plurality of conductor layers* (e.g., tiers 18 composed of second material 22, or in embodiment in which second material 22 is sacrificial material, material 72 that replaces the sacrificial material) *is located between two insulating layers* (e.g., tiers 16 composed of first material 20). Banerjee, ¶¶ 176-78.

5. [1.D] “a filling structure surrounding the multiple-stack staircase structure;”

Tessariol discloses, and at least renders obvious, this limitation. Specifically, as shown in Figure 6 below, Tessariol discloses that “[a]n insulating material 48 (e.g., silicon dioxide and/or silicon nitride) is above steps 40-47.” Tessariol, [0034].

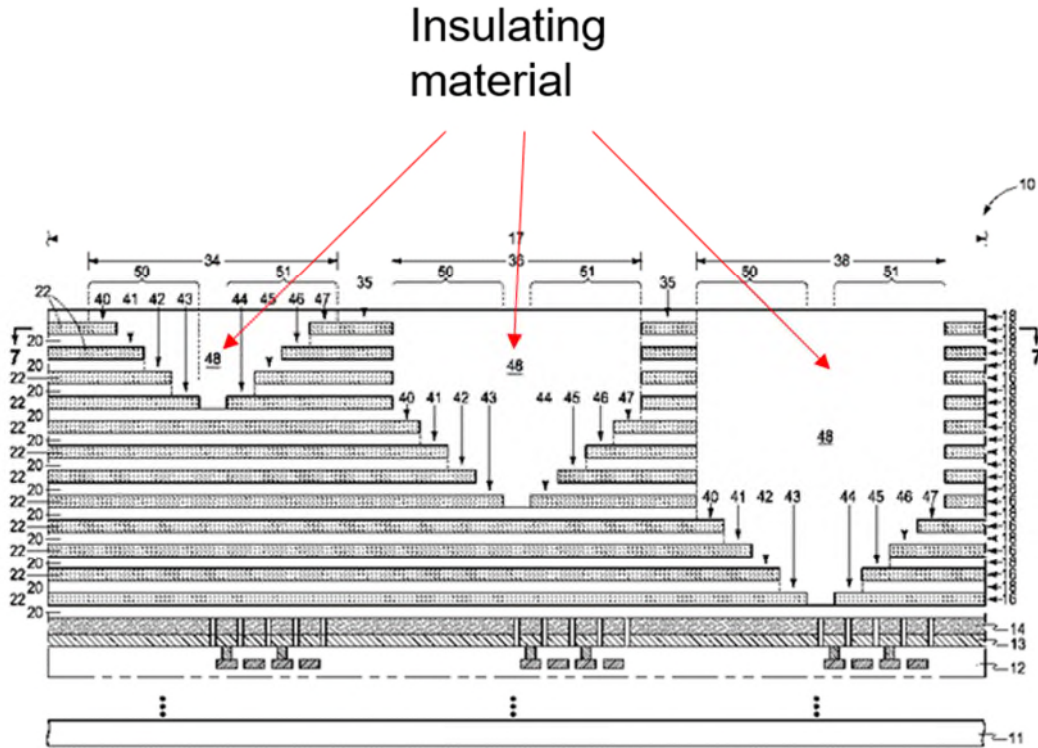


FIG. 6

Id., Fig. 6 (annotated).

Tessariol additionally discloses the deposition of “dielectric material 74” around the staircase structures. Tessariol, [0043].

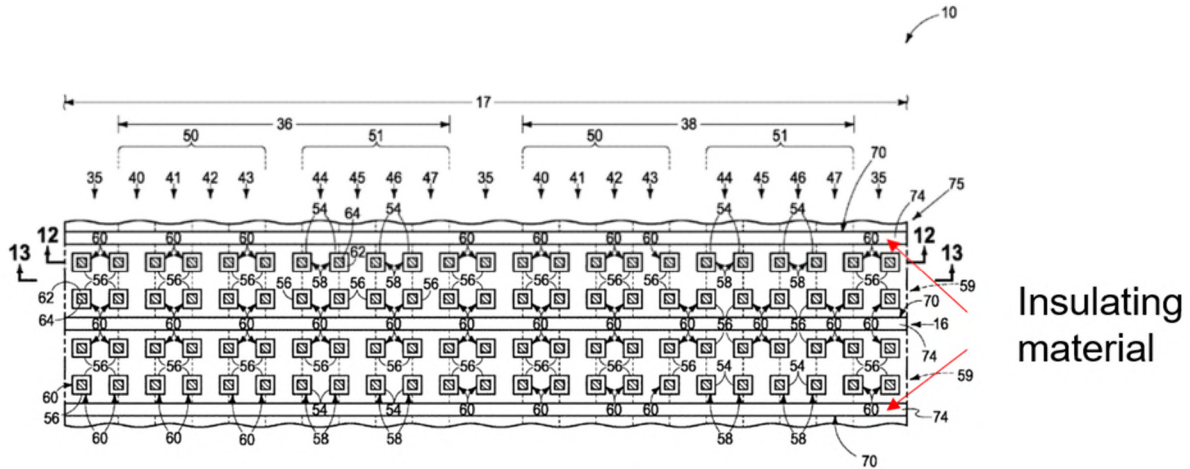
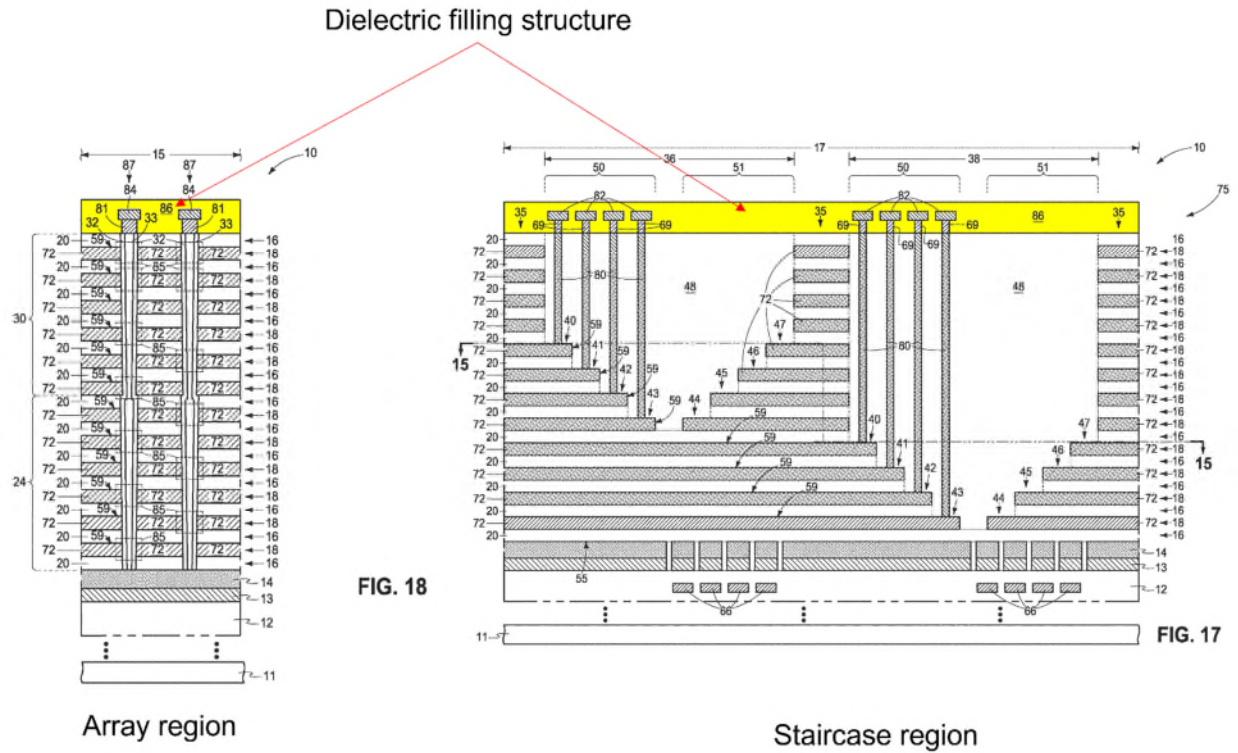


FIG. 11

Id., Fig.11 (annotated). Note that Tessariol discloses that the dielectric material 74 may extend through the array region. *Id.*, [0043].

Further, Tessariol discloses an additional dielectric filling structure (86). Tessariol, [0046] (“Insulator material 86 (e.g., silicon nitride and/or silicon dioxide) is shown surrounding components 69, 82, 81, and 84.”). As shown in the below figures, this encases the entire stack structure to provide a region for metal layer connections to the lower layers:



Id., Figs. 17, 18. This dielectric filling structure (86) “surround[s]” the conductive extensions 69, interconnect lines 82 (both of which are in the staircase region), conductive extensions 81, and conductive lines 84 (both of which are in the array region). Banerjee, ¶¶ 179-81.

To the extent PO argues that “surrounding” requires the dielectric filling structure to be on all sides of the multi-stack staircase structure, such an interpretation is inconsistent with all embodiments of the ’031 Patent, which never describes or illustrates the filling structure on each and every side of the multi-stack structure. Regardless, Tessariol discloses this, as shown above, or at least renders it obvious.

A POSITA would have understood, or at least found obvious, that as taught by Kim, Tessariol's "dielectric material 74" and "insulator material 86" is like Kim's "filling insulating layer 110" that "may be disposed on the substrate 100 and may cover" the entire stack structure, and "may have a planarized top surface." Kim, 9:53-56; *see also id.*, 11:11-21 ("Referring to FIGS. 3 and 10, a filling insulation layer 110 may be formed on an entire top surface of the substrate 100 to cover the mold structure MT."). This electrically isolates the structure and was a conventional, routine insulating technique. Banerjee, ¶ 183. This step would encase all sides of the device, like Kim. And it provides the planarized surface for the interface between the upper-level metal layers for interconnects. Note that Tessariol does not expressly depict the lateral ends of the device. *E.g.*, Tessariol, [0008] ("FIG. 1 is a diagrammatic cross-sectional view of a portion of a substrate construction in process in accordance with an embodiment of the invention."). But a POSITA would have understood that filling structures 48 and 86 encase the entire array and staircase regions for the reasons above. Banerjee ¶ 184.

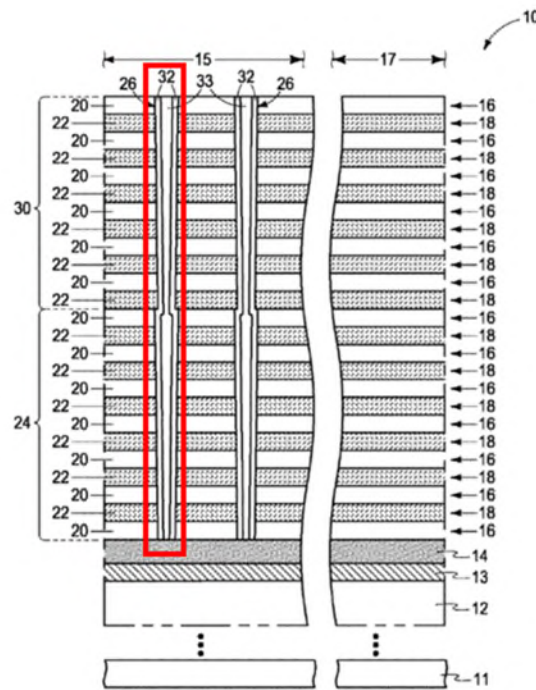
Again, it was well known that there is a requirement to use filling to create a planar top surface for the upper-level metal layers (each of which, in turn, require a planar layer). Banerjee ¶ 112 (citing Ex. 1024).

Therefore, Tessariol discloses, or at least renders obvious, a *filling structure* (*e.g.*, insulating material 48, dielectric material 74, and insulator material 86)

surrounding the multiple-stack staircase structure (e.g., first stack 24 and second stack 30, having staircase regions, e.g., 34, 36, 38 or a two-staircase variation).

6. [1.E] “a semiconductor channel extending through the multiple-stack staircase structure,”

Tessariol discloses this limitation. Specifically, Tessariol discloses “[r]eferring to FIG. 5, transistor material 32 has been formed in individual channel openings 26 in each of first stack 24 and second stack 30. Such may comprise, for example and in order of deposition, a charge-blocking material (e.g., silicon dioxide and/or silicon nitride), a charge-storage material (e.g., floating gate material such as doped or undoped silicon, etc. or charge-trapping material such as silicon nitride, metal dots, etc.).” Tessariol, [0033].



Id., Fig. 5 (annotated).

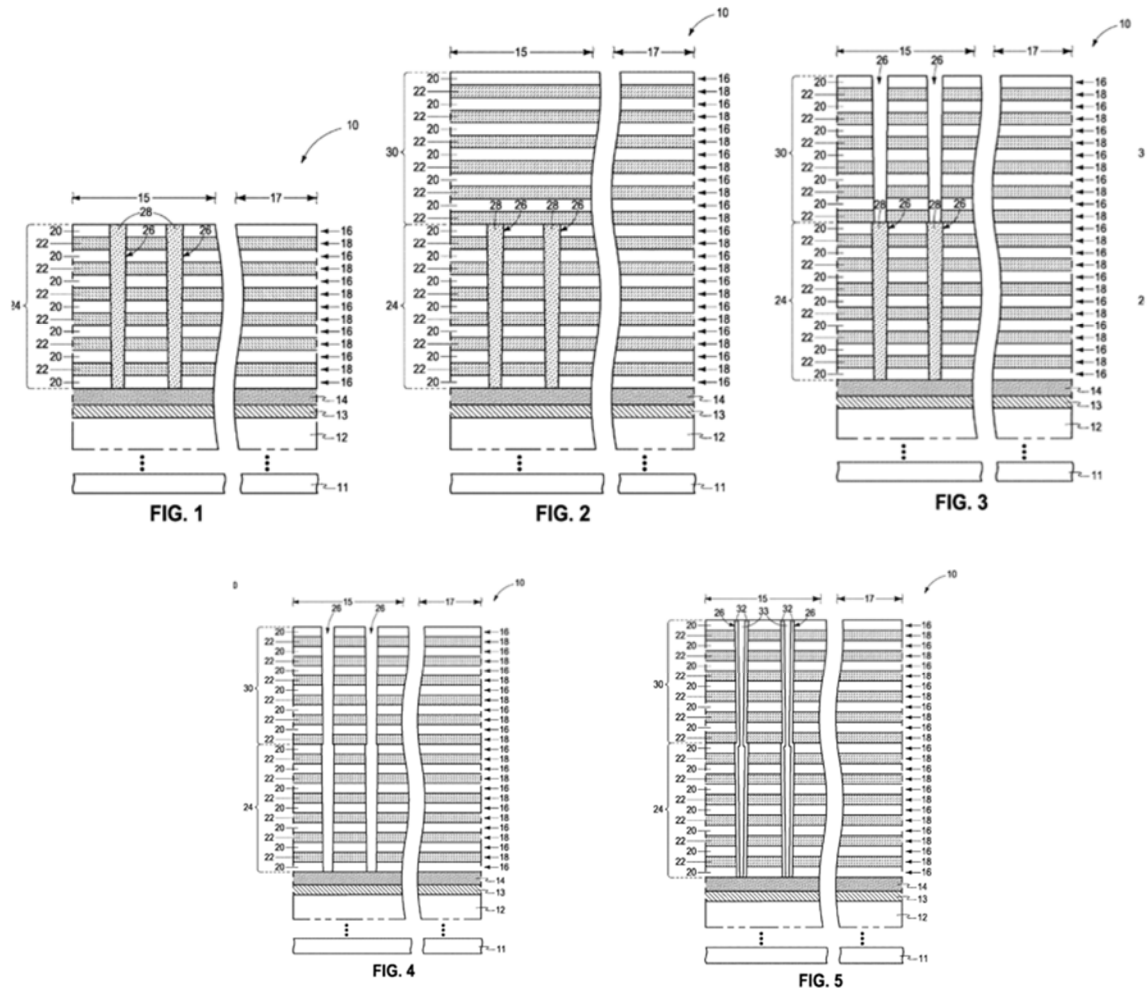
A POSITA would have understood that the structure of Fig. 5 is a semiconductor channel for, *e.g.*, a charge-trap memory string. Banerjee, ¶ 187. Additionally, as shown in Fig. 5 above, Tessariol further discloses a semiconductor channel extending through the multi-stack structure (first stack 24 and second stack 30).

Therefore, Tessariol discloses a *semiconductor channel* (*e.g.*, within channel opening 26, a transistor material 32) *extending through the multiple-stack staircase structure* (*e.g.*, first stack 24 and second stack 30, having staircase regions, *e.g.*, 34, 36, 38). Banerjee, ¶¶ 186-88.

7. [1.F] “wherein the semiconductor channel comprises unaligned sidewall surfaces; and”

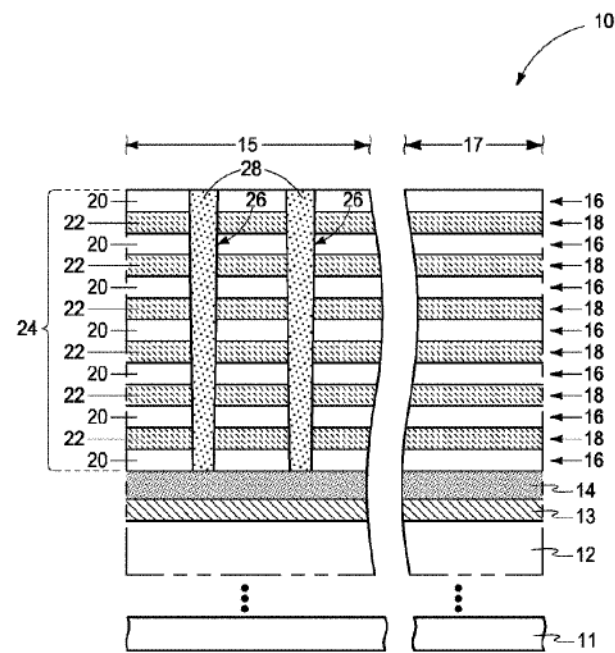
Tessariol discloses, or at least renders obvious, this limitation.

First, as shown below, Tessariol discloses a two-step etch process to form the channel structures in channel openings 26:



Tessariol, Figs. 1-5.

Specifically, Tessariol discloses the formation of channel openings 26 in first stack 24. Tessariol, [0030]. Such openings are then filled with a second sacrificial material 28. *Id.* As shown in Fig. 1 below, and consistent with typical etches, channel openings 26 in first stack 24 progressively taper in diameter as they approach base substrate 11. Banerjee, ¶ 190.



Tessariol, Fig. 1.

As shown in Figure 3 below, following the formation of second stack 30 over first stack 24, Tessariol discloses forming channel openings 26 in second stack 30. Tessariol, [0032].

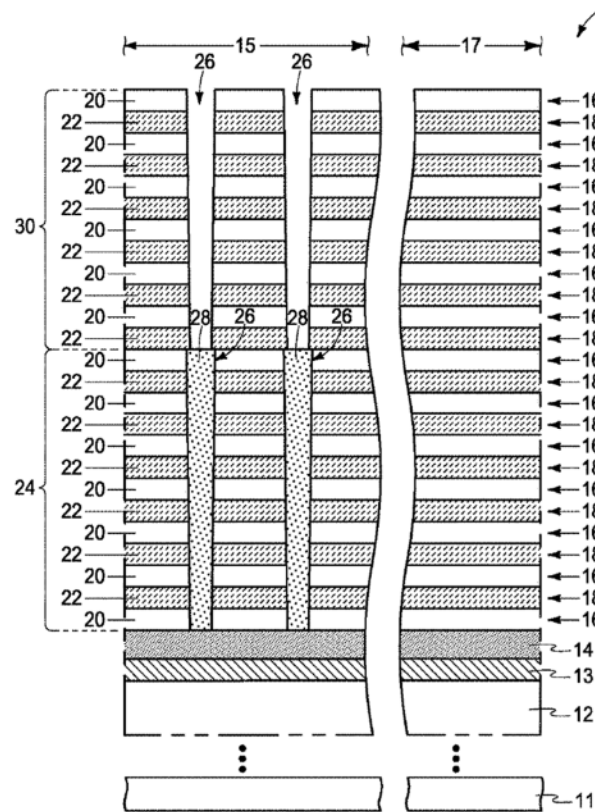
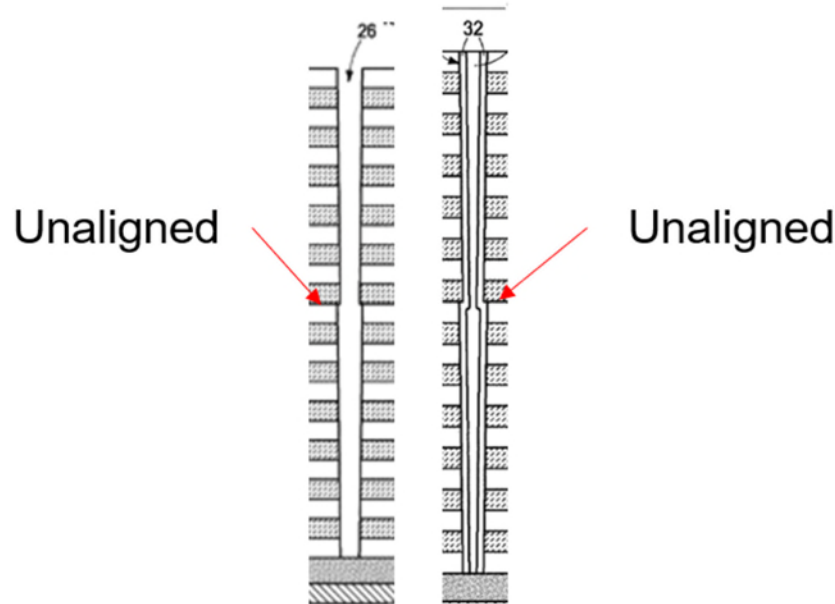


FIG. 3

Id., Fig. 3.

As shown in Fig. 3, channel openings 26 in second stack 30 progressively taper in diameter as they approach base substrate 11 and become misaligned with channel openings 26 in first stack 24. Banerjee, ¶ 192. Next, Tessariol discloses removal of “second sacrificial material 28 . . . from channel opening 26 in first stack 24 through channel openings 26 in second stack 30.” Tessariol, [0032]. As shown in Fig. 4, the resulting joined channel openings 26 of first and second stacks 24 and 30 have unaligned sidewalls. Finally, Tessariol discloses forming the channel

structure. *Id.*, [0034]. As can be seen, both the channel opening and channel structures have unaligned sidewall surfaces:



Tessariol, Figs. 4-5 (partial and annotated).

Thus, Tessariol discloses that the *semiconductor channel comprises unaligned sidewall surfaces* (e.g., sidewalls of transistor material in channel holes 26).

Banerjee, ¶¶ 192-93.

To the extent that PO argues that Tessariol’s disclosure is insufficient because it does not expressly recite “unaligned,” Tessariol at least renders obvious “unaligned sidewalls” in view of the knowledge of a POSITA of two-step etch processes. For example, Kim discloses a process, just like Tessariol, that etches separate channel holes (CH1) and second channel holes (CH2). Kim, 11:49-50. Kim discloses that this results in misaligned channel holes. *See* Section IX.A.7. In view

of Kim's teaching, it would have been obvious that Tessariol results in misaligned channel holes. Banerjee, ¶ 194.

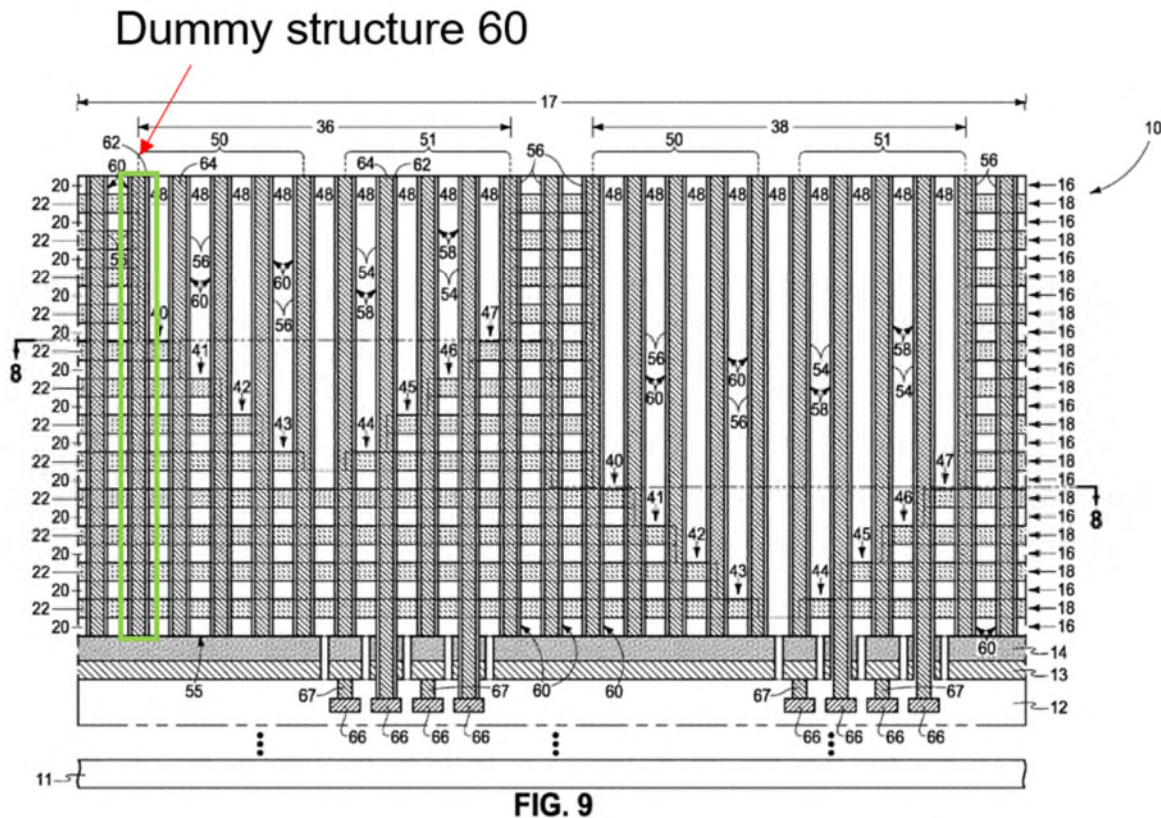
8. [1.G] “a supporting pillar extending through at least one of the multiple-stack staircase structure and the filling structure,”

Tessariol discloses this limitation. Specifically, Tessariol discloses the formation of elevationally-extending dummy-structure openings 56 that are “formed through insulating material 48 [filling structure] and vertically-alternating tiers 16 and 18 in adjacent portion 17.”⁸ Tessariol, [0037]. Similarly, Tessariol discloses forming via openings 54. *Id.* Then, dummy structures 60 are “formed within dummy openings 56, thereby also individually extending elevationally through . . . vertically - alternating tiers 16, 18. . .” *Id.*, [0038]. Operative vias 58 are formed in the via openings. *Id.* Both the dummy structures 60 and operative vias 58 of Tessariol are supporting pillars. Banerjee, ¶¶ 195-96. Specifically, Tessariol discloses that vertically-alternating tiers 16, 18 are “elevationally supported and prevented from collapsing within array portion 15 by transistor material 32 and by both dummy-support structures 60 and operative conductive vias 58 within the stair step structures in adjacent portion 17.” Tessariol, [0041]. Further, Tessariol discloses that “‘a dummy structure’ refers to a structure which is used to mimic a physical property of

⁸ These also extend through the insulating layer 86. Tessariol, Fig. 16.

another structure (e.g., presence, or physical load-carrying supporting ability of an operative structure) and which may comprise a circuit inoperable electrical dead end (e.g., is not part of a current flow path of a circuit even if conductive.” *Id.*, [0068].

An exemplary dummy structure is shown below:



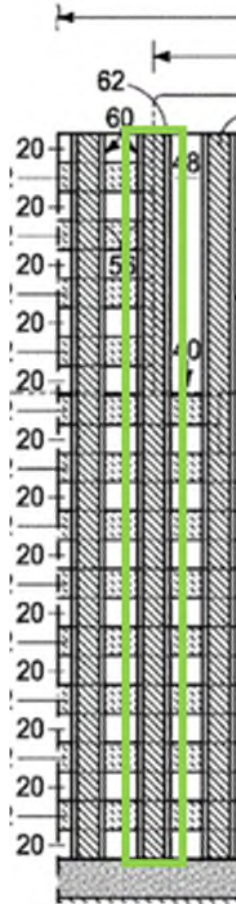
Id., Fig. 9 (annotated).

Therefore, Tessariol discloses a *supporting pillar* (e.g., dummy structures 60 and operative vias 58) *extending through at least one of* [in fact, both] *the multiple-stack staircase structure* (e.g., first stack 24 and second stack 30, having staircase

regions, *e.g.*, 34, 36, 38) and the *filling structure* (*e.g.*, portions of insulating material 48, dielectric material 74, and insulator material 86).

9. [1.H] “wherein the supporting pillar comprises aligned sidewall surfaces.”

Tessariol discloses, or at least renders obvious, this limitation. Unlike the formation of channel openings 26, which requires a two-step etch process, Tessariol discloses the formation of dummy structure openings 56 and via openings 54 using a single etch step: “dummy-structure openings 56 and via openings 54 are formed using a single masking step (*e.g.*, using masking material [not shown] formed atop structure 10).” Tessariol, [0037]. As shown in Fig. 9 below, and consistent with conventional one-etch processes, the dummy structures 60 have aligned sidewalls.



Id., Fig. 9 (partial, annotated). As seen in the full figure, the operative vias include the same aligned sidewalls. *Id.*; Banerjee, ¶¶ 198.

To the extent that PO argues that Tessariol’s disclosure is insufficient because it does not expressly recite “aligned,” Tessariol would at least render obvious “aligned sidewalls” in view of the knowledge of a POSITA of one-step etch processes. For example, Kim discloses a manufacturing method wherein “the dummy holes DH may be formed by one etching process after the formation of the lower mold structure MT1 and the upper mold structure MT2 [(stack structure ST)].” Kim, 12:58-67. Moreover, Kim discloses that “[a] dummy structure . . . DS may be

provided in each of the dummy holes DH. . . .” *Id.*, 9:20-24. Kim also expressly discloses that the vertical dummy structures DS “have a side wall with a planar profile at the level where the upper structure meets the lower structure.” *Id.*, 1:51-53. As Tessariol has the same basic dummy process formation as Kim, a POSITA would have understood Tessariol to disclose aligned dummy pillars and aligned conductive vias, and/or certainly would have found it obvious. Banerjee, ¶ 199.

Thus, Tessariol discloses the *supporting pillar comprises aligned sidewall surfaces* (e.g., dummy structures 60 and operative vias 58).

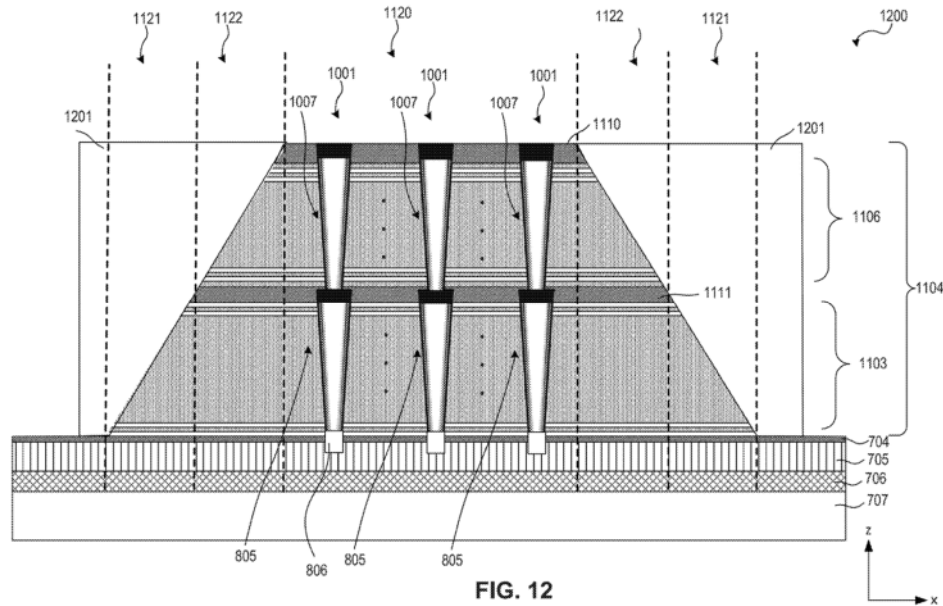
B. Claim 2:

Claim 2 depends on claim 1 and further requires:

1. **[2.A] “the multi-stack staircase structure comprises a first staircase structure over the substrate and a second staircase structure over the first staircase structure; and”**

Tessariol discloses a multi-stack staircase structure comprising a first staircase structure over the substrate and a second staircase structure over the first staircase structure for reasons set forth above for elements [1.A] and [1.B].

Note that while this claim uses “over,” the claim does not require the staircase portion of one staircase structure to be on top of the other. This is evident in Figure 12 of the ’031 Patent:



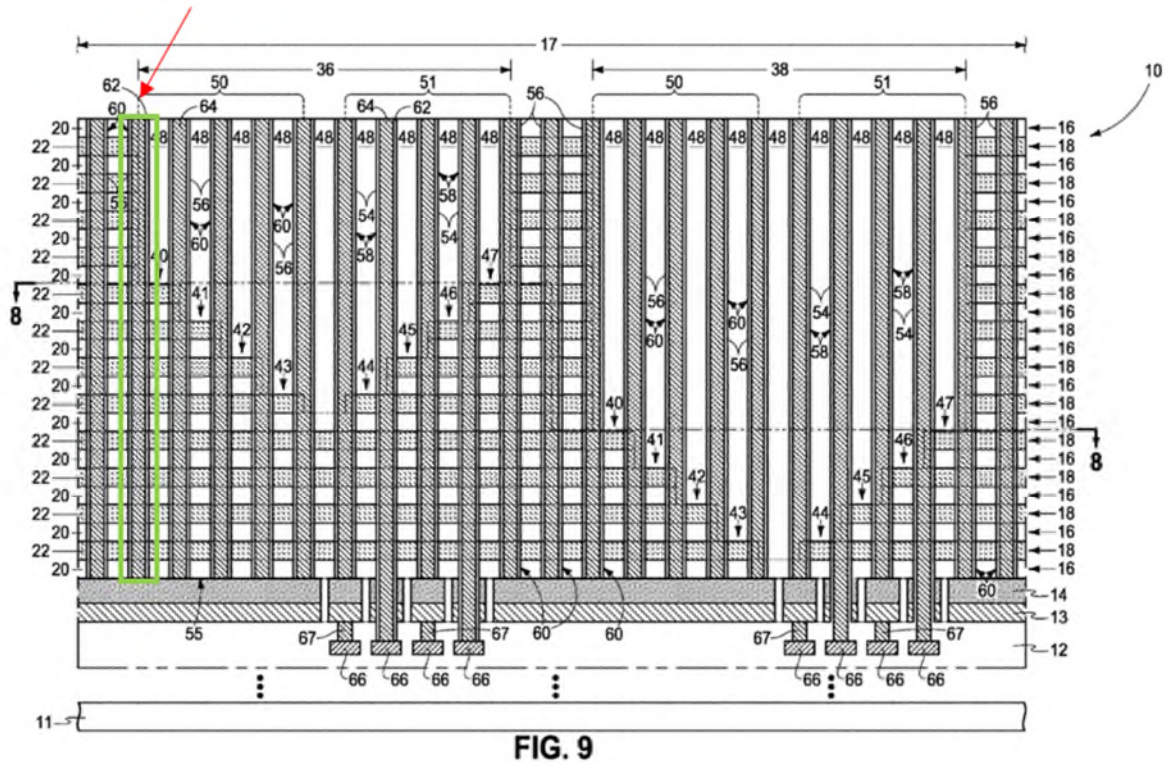
Ex. 1001, Fig. 12.

As shown above, there is a “first staircase region 1121” and “second staircase region 1122.” Ex. 1001, 22:27-32. As can be seen, the upper staircase region of stack structure 1106 is not on top of the lower staircase region of stack structure 1103. But the staircase stacks, which each include a staircase region and are thus staircase structures, are on top of one another. Banerjee, ¶¶ 202-03.

2. [2.B] “the supporting pillar extends from a top surface of the second staircase structure to a bottom surface of the first staircase structure.”

Tessariol discloses a supporting pillar extending from a top surface of the second staircase structure to a bottom surface of the first staircase structure for the reasons set forth above for element [1.G]. As can be seen, both the dummy pillars and operative vias extend from the top of the upper stack to the bottom surface of the first staircase:

Dummy structure 60



Tessariol, Fig. 9 (annotated). Banerjee, ¶ 204.

C. Claim 4:

Claim 4 depends on claim 2 and further requires:

1. [4.A] “the supporting pillar and the semiconductor channel are filled with different filling layers; and”

Tessariol discloses embodiments wherein the semiconductor channels (channel openings 26) and support pillars (dummy structures 60) have different filling layers. For example, Tessariol discloses that transistor material 32 is “formed in individual channel openings 26 in each of the first stack 24 and second stack 30,” and can “comprise, for example and in order of deposition, a charge-blocking material (e.g., silicon dioxide and/or silicon nitride), a charge-storage material (e.g.,

floating gate material such as doped or undoped silicon, etc. or charge-trapping material such as silicon nitride, metal dots, etc.), a charge-passage material (e.g., a bandgap-engineered structure having nitrogen-containing material such as silicon nitride laterally sandwiched between two insulating oxide layers such as silicon dioxide), and transistor channel material (e.g., suitably doped polysilicon, etc.).” Tessariol, [0033]. Tessariol further discloses that dummy structures 60 comprise only two components: “an insulative lining 62 . . . and a conductive core.” *Id.*, [0038]. The operative vias 58 also have this insulative lining and conductive core. *Id.*

2. [4.B] “the supporting pillar is filled with at least one of an insulating material and a pillar-support material surrounded by the insulating material, and”

Tessariol discloses this limitation. Specifically, “the dummy structures may individual [sic] comprise a conductive core (e.g., 64) and an insulative periphery (e.g., 62).” Tessariol, [0049]. Here, the pillar-support material is the conductive core, which is surrounded by the insulating liner. *Id.* The operative vias 58 have these same elements. *Id.*; Banerjee, ¶ 208

3. [4.C] “the semiconductor channel is filled with at least one of a charge trapping film, a semiconductor channel film, and a dielectric core.”

Tessariol discloses this limitation.

Tessariol discloses that transistor material 32 of the semiconductor channels “may comprise, for example and in order of deposition, a charge-blocking material (e.g., silicon dioxide and/or silicon nitride), a charge-storage material (e.g., floating gate material such as doped or undoped silicon, etc. or ***charge-trapping material*** such as silicon nitride, metal dots, etc.), a charge-passage material (e.g., a bandgap-engineered structure having nitrogen-containing material such as silicon nitride laterally sandwiched between two insulating oxide layers such as silicon dioxide), and ***transistor channel material (e.g., suitably doped polysilicon, etc.)***. Material 22 may be laterally recessed back (not shown) from original channel openings 26 prior to deposition of the example charge-blocking material. ***Central portions of channel openings 26 may be filled with*** transistor material (not shown), ***solid insulator material*** 33, or be hollow (not shown).” Tessariol, [0033] (emphases added). A POSITA would have understood that the charge-trapping material is a ***charge trapping film***, the channel material is the ***semiconductor channel film***, and the solid insulator material is the ***dielectric core***. Banerjee, ¶ 209.

D. Claim 5:

Claim 5 depends on claim 4 and further requires:

1. **“wherein the insulating material comprises silicon oxide and the pillar-support material comprises at least one of copper, cobalt, nickel, and aluminum.”**

Tessariol discloses, or at least renders obvious, this limitation.

Tessariol discloses that dummy structures 60 are “formed to comprise an insulative lining [insulative periphery] 62 (e.g., silicon dioxide and/or silicon nitride) and a conductive core 64 (e.g., metal material).” Tessariol, [0038]. The conductive vias include the same materials.

First, silicon dioxide is a “silicon oxide.” Banerjee, ¶ 210.

Second, a POSITA would have understood that by disclosing that the conductive core can be a “metal material,” Tessariol discloses that the pillar-support material may be one of “copper, cobalt, nickel, and aluminum.” Banerjee, ¶ 211. Tessariol discloses that the dummy structures and metal vias may be the same material. Tessariol, [0038]. Copper, a metal material, was a well-known interconnect material, including in 3D NAND devices. Ex. 1014 (U.S. Pat. No. 9,299,641), 2:32-43 (copper interconnects); Ex. 1015 (U.S. Pat. No. 11,244,725), 11:36-44 (copper interconnects); Banerjee, ¶ 211.

XI. GROUND 3: DEPENDENT CLAIM 4 IS OBVIOUS OVER KIM IN VIEW OF TESSARIOL

Ground 1 demonstrates that in view of Kim’s disclosures and the knowledge of a POSITA, claim 4 is unpatentable at least because it would have been obvious to a POSITA to employ dummy pillars with a conductive core and insulating liner as Kim’s dummy structures (“*supporting pillars*”). Section IX.D.2. Ground 1 uses Tessariol to show that the use of such dummy structures was well known to a POSITA. *Id.* Ground 3 expressly combines Kim with Tessariol to demonstrate the

same point: Kim in view of Tessariol would render obvious employing a conductive core and insulating liner as the dummy pillars in Kim. Ground 3 relies on the same disclosures as Ground 1 for claims 1 and 2, and the below only addresses claim 4.

As to claim 4, in view of Tessariol, a POSITA would have been motivated to employ supporting pillars with a conductive core and insulating liner as Kim's dummy structures DS with a reasonable expectation of success.

A. Motivation To Combine And Expectation Of Success

A POSITA would have been motivated to employ Tessariol's teaching of conductive cores with a conductive liner as Kim's dummy structures (“*supporting pillars*”) for several reasons. First, because Kim states that the function of the dummy structure is to “support the stack structure ST,” a POSITA would have been motivated to consider a variety of support structures. Kim, 9:30-31; Banerjee, ¶ 214. And Tessariol describes pillars that provide this same function, namely, to “support[] and prevent[] [the stack] from collapsing.” Tessariol, [0041]. Second, Kim's dummy pillars include various thin layers, which unlike the solid metal core of Tessariol's vias, are an inferior support member, and the overall structure provides less support than Tessariol's metal core. Ex. 1012 (U.S. Pat. No. 9,768,186), 4:60-5:12; Banerjee, ¶ 215. Third, Kim expressly recites that the dummy structures need not be the same material as the channel structures. Kim, 13:28-33. This would have motivated a POSITA to consider other types of support pillars, and Tessariol

provides such other types. Tessariol, [0037], [0038], [0041]; Banerjee, ¶ 216. Fourth, and notably, Tessariol describes its supporting pillars as either dummy conductive vias or active conductive vias. Tessariol, [0041]. A POSITA would have understood that using active conductive vias as supporting pillars in Kim would be advantageous because they enable a dual-role function: the pillars would provide both a support function and an interconnect function. Banerjee, ¶ 217.

A POSITA would have had a reasonable expectation of success for several reasons. First, Tessariol's support pillars extend through the stack. Tessariol, Fig. 9. Kim already etches through the stack to form its dummy channel structures. Kim, Fig. 4B. Second, Tessariol's support pillars include an insulating liner and a conductive core. Kim already employs such structures that extend through the stack, namely, a common source line. *Id.*, 6:24-30. Third, the processing techniques to create supporting conductive vias, such as those in Tessariol, were well known. Banerjee, ¶ 218.

B. Claim 4:

Claim 4 depends on claim 2 and further requires:

1. **[4.A] “the supporting pillar and the semiconductor channel are filled with different filling layers; and”**

Kim in view of Tessariol renders this limitation obvious.

Kim describes a semiconductor channel that includes semiconductor and memory elements. Section IX.A.6.

Kim states “[i]n some embodiments . . . each of dummy structures DS may include a dummy pattern. A layer or component of each of the dummy structures DS [*supporting pillar*] may be different from the layer(s) or component(s) of each of the vertical structures VS [*semiconductor channel*].” Kim, 13:28-33. As Section XI.A demonstrates, a POSITA would have been motivated to employ a conductive core with an insulating liner as Kim’s dummy structures, which are *different filling layers* than Kim’s semiconductor channel. Tessariol, [0037], [0038], [0041]; Section IX.A.6; Banerjee, ¶ 220.

2. **[4.B] “the supporting pillar is filled with at least one of an insulating material and a pillar-support material surrounded by the insulating material,”**

Kim in view of Tessariol renders this limitation obvious.

As Section XI.B.1 demonstrates, a POSITA would have been motivated to employ a conductive core with an insulating liner as Kim’s supporting pillar. Tessariol, [0037], [0038], [0041]; Banerjee, ¶ 221. In Tessariol, the conductive core is a support material, and the insulating material surrounds the core. *Id.*

3. **[4.C] “and the semiconductor channel is filled with at least one of a charge trapping film, a semiconductor channel film, and a dielectric core.”**

Kim discloses semiconductor channels filled with at least one of a charge trapping film, a semiconductor channel film, and a dielectric core for the reasons set forth above for limitation [3.B] in Ground 1.

XII. GROUND 4: INDEPENDENT CLAIM 1 AND DEPENDENT CLAIMS 2 AND 4-5 ARE OBVIOUS OVER TESSARIOL IN VIEW OF KIM

Ground 2 demonstrates that claims 1, 2, and 4-5 are obvious in view of Tessariol and the knowledge of a POSITA. Ground 2 uses Kim to show the knowledge of a POSITA in three areas: (1) for limitation [1.B], that a two-stack staircase structure was well known, (2) for limitation [1.D], that filling techniques to encase the 3D structure were conventional and routine to employ, (3) for limitation [1.F], that a two-step etch process will typically create unaligned sidewalls, and (4) for limitation [1.H], that a one-step etch process will typically create aligned sidewalls. To the extent that PO were to argue that Ground 2 must expressly include Kim to consider Kim's teachings (which would be incorrect, because an obviousness ground always considers the knowledge of a POSITA), Ground 4 combines Tessariol and Kim. For all other limitations, Ground 4 relies on the same disclosures as Ground 2. Thus, the sections below only address limitations [1.B], [1.F], and [1.H].

A. Motivation To Combine And Expectation Of Success

A POSITA would have been motivated to combine Kim's teaching as to staircase regions, insulative filling, two-step etch profiles, and one-step etch profiles with Tessariol, including with a reasonable expectation of success, for several reasons.

As to staircase regions, first, Tessariol expressly leaves its invention open to use virtually any type of staircase region. Tessariol, [0034] (disclosing that “only one stair step structure, two stair step structures, or more than three stair step structures may be formed” and such structures “may be formed by any suitable existing or yet-to-be-developed technique, with photolithographic patterning and etch being one example”), [0035] (disclosing the use of different flight configurations). This would have motivated a POSITA to consider other staircase region teachings, such as Kim. Second, Tessariol’s and Kim’s staircase regions provide the same architecture, namely, landing pads for contacts to the wordlines. Kim, Figs. 4A, 18 (showing contacts to staircase), Tessariol, Fig. 17 (showing contacts to staircase). This would have motivated a POSITA to consider Kim’s staircase region. Third, Tessariol’s staircase region requires dummy structures because it uses a sacrificial gate replacement process. Section X.A.7. Kim’s staircase region includes dummy support pillars. Section IX.A.7. Given Tessariol’s staircase region requirements, and given that Kim’s staircase region meets those requirements, this would have motivated a POSITA to consider Kim’s staircase region. Fourth, half of Tessariol’s staircase regions are not used. Tessariol, Fig. 17 (the right portion, 44-47, of each staircase is not used). In other words, half of the steps that were made are non-functional. A POSITA would have been motivated to

consider more efficient staircase regions, such as those in Kim, which are not made of non-functional steps. Banerjee, ¶¶ 226-229.

A POSITA would have had a reasonable expectation of success in applying Kim's staircase teachings to Tessariol for several reasons. First, recall that Tessariol states that its staircase region "may be formed by any suitable existing or yet-to-be-developed technique, with photolithographic patterning and etch being one example." Tessariol, [0034]. A POSITA would have recognized that Tessariol is disclosing that its memory device does not require a specific type of staircase region. And Kim's staircase region is suitable for Tessariol, for example, because it allows for support pillars, which Tessariol's memory requires. Section X.A.7; Section IX.A.7. Second, staircase technology was well known at the time of the alleged invention, and it would have been routine to apply staircase teachings from one 3D NAND design to another 3D NAND design. Section V.A; Banerjee, ¶ 230.

As to the filling techniques, first, Tessariol and Kim both depict a planar surface that is an interface to upper metal layers. Kim, Fig. 4A (110/120/130), Tessariol, Fig. 17 (86). Thus, a POSITA would have been motivated to consider Kim's fill techniques to provide for the planarized surface. And both Tessariol and Kim employ a multi-stack staircase structure that include large voids that require filling. *See* Grounds 1 and 2. Thus, a POSITA would have found Kim's teachings particular applicable to Tessariol. It would have been routine to apply Kim's filling

teachings to Tessariol, because both Kim and Tessariol have the same fundamental structures, and because the deposition of such fills was textbook material. Banerjee, ¶ 231.

As to etch profile teachings, first, Tessariol employs a one- and two-step etch process to form, respectively, supporting pillars and dummy channel structures in 3D NAND devices. Sections X.A.1, 6, 8. Kim discloses the same, but expressly discusses the effect of the these etches on the sidewall profiles. Sections IX.A.1, 6, 8. Thus, a POSITA would have been motivated to consider Kim's etch teachings to improve and understand the structures in Tessariol. Second, both Tessariol and Kim use the supporting pillars and channel structures for the same purposes. Sections X.A.1, 6, 8; IX.A.1, 6, 8. This would have further motivated a POSITA to consider Kim, because Kim's etch teachings are directly relevant to the same structures in Tessariol. Banerjee, ¶ 232.

A POSITA would have had a reasonable expectation of success in applying Kim's etch teachings to Tessariol for several reasons. First, as described above, Kim's etch teachings relate to the same structures, namely, supporting pillars and channel structures. Second, not only do the teachings relate to the same structures, but those structures are within the same type of device, namely, 3D NAND. Sections X.A.1, 6; Sections IX.A.1, 6, 8; Banerjee, ¶ 233.

B. Claim 1:

1. [1.B] “a multiple-stack staircase structure comprising a plurality of staircase structures stacked over the substrate,”

Tessariol in view of Kim render this limitation obvious.

As Section X.A.3 demonstrates, Tessariol discloses a multi-stack structure with a “a *first stack 24*” and “a *second stack 30*.” Section X.A.3; Tessariol, [0029], [0031] (emphasis added). Tessariol further discloses that each stack includes a staircase portion. *Id.*, [0034]. As Section XII.A demonstrates, it would have been obvious to apply Kim’s staircase teachings to Tessariol. Kim employs a continuous staircase region for each stack, and applying this to Tessariol would result in a continuous staircase region for each stack (as Kim illustrates, Fig. 4B). Section X.A.3; Banerjee ¶ 234. This Ground proposes no other changes to Tessariol’s stack structure, *e.g.*, the alternating layer materials of the staircase region as set forth by Tessariol and Ground 1.

Thus, Tessariol in view of Kim renders obvious a *multiple-stack staircase structure* (*e.g.*, first stack 24 and second stack 30, having two continuous staircase structures) *comprising a plurality of staircase structures* (*e.g.*, each of the first stack 24 and second stack 30, both of which have a continuous staircase structure portion) *stacked over the substrate* (*e.g.*, base substrate 11).

2. [1.F] “wherein the semiconductor channel comprises unaligned sidewall surfaces; and”

Tessariol in view of Kim render this limitation obvious.

As Section X.A.6 demonstrates, Tessariol employs a two-step etch process to create its channel structures. Section X.A.6; Tessariol, Figs. 1-5, [0030], [0032], [0034]. Kim discloses a process, just like Tessariol, that etches separate first channel holes (CH1) and second channel holes (CH2) to form the channel structures. Kim, 11:49-50. Kim discloses that this results in misaligned channel structures. Section X.A.6. In view of Kim's teaching, it would have been obvious that Tessariol's two-step etch process will result in unaligned channel sidewalls. Banerjee, ¶ 236.

Thus, Tessariol in view of Kim renders obvious that the *semiconductor channel comprises unaligned sidewall surfaces* (e.g., sidewalls of transistor material in channel holes 26).

3. [1.H] “wherein the supporting pillar comprises aligned sidewall surfaces.”

Tessariol in view of Kim render this limitation obvious.

As Sections X.A.7-8 demonstrate, Tessariol employs a one-step etch process to create its supporting pillars. Section X.A.8; Tessariol, [0037]. Like Tessariol, Kim discloses a manufacturing method wherein “the dummy holes DH may be formed by one etching process after the formation of the lower mold structure MT1 and the upper mold structure MT2 [(stack structure ST)].” Kim, 12:58-67. Kim teaches that this results in aligned dummy structures. Section X.A.7. In view of Kim's teaching, it would have been obvious that Tessariol's one-step etch process will result in aligned supporting pillars. Banerjee, ¶ 238.

Thus, Tessariol in view of Kim renders obvious that the *supporting pillar comprises aligned sidewall surfaces* (e.g., dummy structures 60 and operative vias 58).

XIII. SECONDARY CONSIDERATIONS

Petitioner is unaware of any applicable secondary considerations of nonobviousness. None were identified during prosecution. *See generally* Ex. 1002. Even if such considerations existed, none would overcome the strong *prima facie* showing of obviousness.

XIV. CONCLUSION

Petitioner respectfully requests that the Board enter a final written decision finding the Challenged Claims unpatentable.

Petition for *Inter Partes* Review of U.S. Patent No. 10,868,031

Respectfully submitted,

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Dated: April 18, 2024

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CERTIFICATE OF COMPLIANCE

The undersigned certifies that the foregoing PETITION FOR *INTER PARTES* REVIEW complies with the type volume limitation in 37 C.F.R. § 42.24(a). According to the utilized word-processing system's word count, the petition—excluding the caption, table of contents, table of exhibits, mandatory notices, certificate of word count, and certificate of service—contains 13,541 words.

Dated: April 18, 2024

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CERTIFICATE OF SERVICE

The undersigned hereby confirms that the foregoing Petition for *Inter Partes* Review and associated exhibits were caused to be served on April 18, 2024 via overnight courier upon the following counsel of record for Patent Owner:

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