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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.	4123.0350001
First Named Inventor	Jun LIU
Title	See 1 in Addendum
Priority Mail Express® Label No.	

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

1. [ ] **Fee Transmittal Form** (PTO/SB/17 or equivalent)
2. [ ] **Applicant asserts small entity status.** See 37 CFR 1.27
3. [ ] **Applicant certifies micro entity status.** See 37 CFR 1.29. Applicant must attach form PTO/SB/15A or B or equivalent.
4. [X] **Specification** [*Total Pages* 44] Both the claims and abstract must start on a new page. *(See MPEP § 608.01(a) for information on the preferred arrangement)*
5. [X] **Drawing(s)** (35 U.S.C. 113) [*Total Sheets* 13]
6. **Inventor's Oath or Declaration** [*Total Pages* ____] *(including substitute statements under 37 CFR 1.64 and assignments serving as an oath or declaration under 37 CFR 1.63(e))*
   a. [ ] Newly executed (original or copy)
   b. [ ] A copy from a prior application (37 CFR 1.63(d))
7. [X] **Application Data Sheet** ** See note below.* See 37 CFR 1.76 (PTO/AIA/14 or equivalent)
8. **CD-ROM or CD-R** in duplicate, large table, or Computer Program (*Appendix*)
   [ ] Landscape Table on CD
9. **Nucleotide and/or Amino Acid Sequence Submission** (*if applicable, items a. – c. are required*)
   a. [ ] Computer Readable Form (CRF)
   b. [ ] Specification Sequence Listing on:
      i. [ ] CD-ROM or CD-R (2 copies); or
      ii. [ ] Paper
   c. [ ] Statements verifying identity of above copies

ADDRESS TO:

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

ACCOMPANYING APPLICATION PAPERS

10. [ ] **Assignment Papers** (cover sheet & document(s))
    Name of Assignee Yangtze Memory Technologies Co., Ltd.
11. [ ] **37 CFR 3.73(c) Statement** (*when there is an assignee*) [X] **Power of Attorney**
12. [ ] **English Translation Document** (*if applicable*)
13. [ ] **Information Disclosure Statement** (PTO/SB/08 or PTO-1449)
    [ ] Copies of citations attached
14. [ ] **Preliminary Amendment**
15. [ ] **Return Receipt Postcard** (*MPEP § 503*) (*Should be specifically itemized*)
16. [ ] **Certified Copy of Priority Document(s)** (*if foreign priority is claimed*)
17. [ ] **Nonpublication Request** Under 35 U.S.C. 122(b)(2)(B)(i). Applicant must attach form PTO/SB/35 or equivalent.
18. [X] **Other:** Authorization under 37 CFR 1.136(a)(3)

***Note**: (1) Benefit claims under 37 CFR 1.78 and foreign priority claims under 1.55 **must** be included in an Application Data Sheet (ADS).
(2) For applications filed under 35 U.S.C. 111, the application must contain an ADS specifying the applicant if the applicant is an assignee, person to whom the inventor is under an obligation to assign, or person who otherwise shows sufficient proprietary interest in the matter. See 37 CFR 1.46(b).

19. CORRESPONDENCE ADDRESS

[X] The address associated with Customer Number: **26111** **OR** [ ] Correspondence address below

Name					
Address					
City		State		Zip Code	
Country		Telephone		Email	

Signature	/Donald J. Featherstone/	Date	9/10/18
Name (Print/Type)	Donald J. Featherstone	Registration No. (Attorney/Agent)	33,876

This collection of information is required by 37 CFR 1.53(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

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Addendum

1. MULTIPLE-STACK THREE-DIMENSIONAL MEMORY DEVICE AND FABRICATION METHOD THEREOF

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventors: LIU *et al.*	Confirmation No.: *To Be Assigned*
Applicant: Yangtze Memory Technologies Co., Ltd.	Art Unit: *To Be Assigned*
Application No.: *To Be Assigned*	Examiner: *To Be Assigned*
(*Continuation of Appl. No. PCT/CN2018/097432; Filed: July 27, 2018*)	Atty. Docket: 4123.0350001
Filed: *Herewith*	

Title: **MULTIPLE-STACK THREE-DIMENSIONAL MEMORY DEVICE AND FABRICATION METHOD THEREOF**

Authorization to Treat a Reply as Incorporating an Extension of Time Under 37 C.F.R. § 1.136(a)(3)

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Commissioner:

The U.S. Patent and Trademark Office is hereby authorized to treat any concurrent or future reply that requires a petition for an extension of time under this paragraph for its timely submission, as incorporating a petition for extension of time for the appropriate length of time. The U.S. Patent and Trademark Office is hereby authorized to charge all required extension of time fees to our Deposit Account No. 19-0036, if such fees are not otherwise provided for in such reply.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

/Donald J. Featherstone/

Donald J. Featherstone
Attorney for Applicant
Registration No. 33,876

Date: 9/10/18

1100 New York Avenue, N.W.
Washington, D.C. 20005-3934
(202) 371-2600
9960906_1.docx

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	4123.0350001
	Application Number	
Title of Invention	MULTIPLE-STACK THREE-DIMENSIONAL MEMORY DEVICE AND FABRICATION METHOD THEREOF	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

Secrecy Order 37 CFR 5.2:

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Inventor Information:

Inventor 1 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Jun		LIU	

Residence Information (Select One) ○ US Residency ◉ Non US Residency ○ Active US Military Service

City	Wuhan, Hubei	Country of Residence [i]	CN

Mailing Address of Inventor:

Address 1	Yangtze Memory Technologies Co., Ltd.		
Address 2	18 Gaoxin 4th Rd., East Lake High-Tech Dev. Zone		
City	Wuhan, Hubei	**State/Province**	
Postal Code		**Country** [i]	CN

Inventor 2 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Zongliang		HUO	

Residence Information (Select One) ○ US Residency ◉ Non US Residency ○ Active US Military Service

City	Wuhan, Hubei	Country of Residence [i]	CN

Mailing Address of Inventor:

Address 1	Yangtze Memory Technologies Co., Ltd.		
Address 2	18 Gaoxin 4th Rd., East Lake High-Tech Dev. Zone		
City	Wuhan, Hubei	**State/Province**	
Postal Code		**Country** [i]	CN

Inventor 3 Remove

Legal Name

Micron Ex. 1002, p. 5
Micron v. YMTC
IPR2024-00790

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	4123.0350001
	Application Number	
Title of Invention	MULTIPLE-STACK THREE-DIMENSIONAL MEMORY DEVICE AND FABRICATION METHOD THEREOF	

Prefix	Given Name	Middle Name	Family Name	Suffix
	Li Hong		XIAO	

Residence Information (Select One) ○ US Residency ◉ Non US Residency ○ Active US Military Service

City	Wuhan, Hubei	Country of Residence [i]	CN

Mailing Address of Inventor:

Address 1	Yangtze Memory Technologies Co., Ltd.
Address 2	18 Gaoxin 4th Rd., East Lake High-Tech Dev. Zone

City	Wuhan, Hubei	State/Province	
Postal Code		**Country** [i]	CN

Inventor 4 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Zhenyu		LU	

Residence Information (Select One) ○ US Residency ◉ Non US Residency ○ Active US Military Service

City	Wuhan, Hubei	Country of Residence [i]	CN

Mailing Address of Inventor:

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City	Wuhan, Hubei	State/Province	
Postal Code		**Country** [i]	CN

Inventor 5 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Qian		TAO	

Residence Information (Select One) ○ US Residency ◉ Non US Residency ○ Active US Military Service

City	Wuhan, Hubei	Country of Residence [i]	CN

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Postal Code		**Country** [i]	CN

Micron Ex. 1002, p. 6
Micron v. YMTC
IPR2024-00790

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	4123.0350001
	Application Number	
Title of Invention	MULTIPLE-STACK THREE-DIMENSIONAL MEMORY DEVICE AND FABRICATION METHOD THEREOF	

Inventor 6 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Yushi		HU	

Residence Information (Select One) ○ US Residency ◉ Non US Residency ○ Active US Military Service

City	Wuhan, Hubei	Country of Residence [i]	CN

Mailing Address of Inventor:

Address 1	Yangtze Memory Technologies Co., Ltd.
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City	Wuhan, Hubei	State/Province	
Postal Code		**Country** [i]	CN

Inventor 7 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Sizhe		LI	

Residence Information (Select One) ○ US Residency ◉ Non US Residency ○ Active US Military Service

City	Wuhan, Hubei	Country of Residence [i]	

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City	Wuhan, Hubei	State/Province	
Postal Code		**Country** [i]	CN

Inventor 8 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Zhao Hui		TANG	

Residence Information (Select One) ○ US Residency ◉ Non US Residency ○ Active US Military Service

City	Wuhan, Hubei	Country of Residence [i]	CN

Mailing Address of Inventor:

Address 1	Yangtze Memory Technologies Co., Ltd.
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Micron Ex. 1002, p. 7
Micron v. YMTC
IPR2024-00790

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	4123.0350001
	Application Number	
Title of Invention	MULTIPLE-STACK THREE-DIMENSIONAL MEMORY DEVICE AND FABRICATION METHOD THEREOF	

City	Wuhan, Hubei	State/Province	
Postal Code		Country [i]	CN

Inventor 9 — Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Yu Ting		ZHOU	

Residence Information (Select One) ○ US Residency ◉ Non US Residency ○ Active US Military Service

City	Wuhan, Hubei	Country of Residence [i]	CN

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City	Wuhan, Hubei	State/Province	
Postal Code		Country [i]	CN

Inventor 10 — Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Zhaosong		LI	

Residence Information (Select One) ○ US Residency ◉ Non US Residency ○ Active US Military Service

City	Wuhan, Hubei	Country of Residence [i]	CN

Mailing Address of Inventor:

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City	Wuhan, Hubei	State/Province	
Postal Code		Country [i]	CN

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. — Add

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below.
For further information see 37 CFR 1.33(a).

☐ **An Address is being provided for the correspondence Information of this application.**

Customer Number	26111		
Email Address		Add Email	Remove Email

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	4123.0350001
	Application Number	
Title of Invention	MULTIPLE-STACK THREE-DIMENSIONAL MEMORY DEVICE AND FABRICATION METHOD THEREOF	

Application Information:

Title of the Invention	MULTIPLE-STACK THREE-DIMENSIONAL MEMORY DEVICE AND FABRICATION METHOD THEREOF		
Attorney Docket Number	4123.0350001	**Small Entity Status Claimed** ☐	
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	13	**Suggested Figure for Publication (if any)**	

Filing By Reference:

Only complete this section when filing an application by reference under 35 U.S.C. 111(c) and 37 CFR 1.57(a). Do not complete this section if application papers including a specification and any drawings are being filed. Any domestic benefit or foreign priority information must be provided in the appropriate section(s) below (i.e., "Domestic Benefit/National Stage Information" and "Foreign Priority Information").

For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32).
Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.

Please Select One:	◉ Customer Number	○ US Patent Practitioner	○ Limited Recognition (37 CFR 11.9)
Customer Number	26111		

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	4123.0350001
	Application Number	
Title of Invention	MULTIPLE-STACK THREE-DIMENSIONAL MEMORY DEVICE AND FABRICATION METHOD THEREOF	

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, 365(c), or 386(c) or indicate National Stage entry from a PCT application. Providing benefit claim information in the Application Data Sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.
When referring to the current application, please leave the "Application Number" field blank.

Prior Application Status	Pending	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
	Continuation of	PCT/CN2018/097432	2018-07-27

Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the **Add** button.

Foreign Priority Information:

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55. When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX)[i] the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(i)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

			Remove
Application Number	Country[i]	Filing Date (YYYY-MM-DD)	Access Code[i] (if applicable)

Additional Foreign Priority Data may be generated within this form by selecting the **Add** button.

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

☐ This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.
NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	4123.0350001
	Application Number	
Title of Invention	MULTIPLE-STACK THREE-DIMENSIONAL MEMORY DEVICE AND FABRICATION METHOD THEREOF	

Authorization or Opt-Out of Authorization to Permit Access:

When this Application Data Sheet is properly signed and filed with the application, applicant has provided written authority to permit a participating foreign intellectual property (IP) office access to the instant application-as-filed (see paragraph A in subsection 1 below) and the European Patent Office (EPO) access to any search results from the instant application (see paragraph B in subsection 1 below).

Should applicant choose not to provide an authorization identified in subsection 1 below, applicant **must opt-out** of the authorization by checking the corresponding box A or B or both in subsection 2 below.

NOTE: This section of the Application Data Sheet is **ONLY** reviewed and processed with the **INITIAL** filing of an application. After the initial filing of an application, an Application Data Sheet cannot be used to provide or rescind authorization for access by a foreign IP office(s). Instead, Form PTO/SB/39 or PTO/SB/69 must be used as appropriate.

1. Authorization to Permit Access by a Foreign Intellectual Property Office(s)

A. Priority Document Exchange (PDX) - Unless box A in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the State Intellectual Property Office of the People's Republic of China (SIPO), the World Intellectual Property Organization (WIPO), and any other foreign intellectual property office participating with the USPTO in a bilateral or multilateral priority document exchange agreement in which a foreign application claiming priority to the instant patent application is filed, access to: (1) the instant patent application-as-filed and its related bibliographic data, (2) any foreign or domestic application to which priority or benefit is claimed by the instant application and its related bibliographic data, and (3) the date of filing of this Authorization. See 37 CFR 1.14(h)(1).

B. Search Results from U.S. Application to EPO - Unless box B in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the EPO access to the bibliographic data and search results from the instant patent application when a European patent application claiming priority to the instant patent application is filed. See 37 CFR 1.14(h)(2).

The applicant is reminded that the EPO's Rule 141(1) EPC (European Patent Convention) requires applicants to submit a copy of search results from the instant application without delay in a European patent application that claims priority to the instant application.

2. Opt-Out of Authorizations to Permit Access by a Foreign Intellectual Property Office(s)

☐ A. Applicant **DOES NOT** authorize the USPTO to permit a participating foreign IP office access to the instant application-as-filed. If this box is checked, the USPTO will not be providing a participating foreign IP office with any documents and information identified in subsection 1A above.

☐ B. Applicant **DOES NOT** authorize the USPTO to transmit to the EPO any search results from the instant patent application. If this box is checked, the USPTO will not be providing the EPO with search results from the instant application.

NOTE: Once the application has published or is otherwise publicly available, the USPTO may provide access to the application in accordance with 37 CFR 1.14.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	4123.0350001
	Application Number	
Title of Invention	MULTIPLE-STACK THREE-DIMENSIONAL MEMORY DEVICE AND FABRICATION METHOD THEREOF	

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Applicant 1

If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.

Clear

○ Assignee	○ Legal Representative under 35 U.S.C. 117	○ Joint Inventor
◉ Person to whom the inventor is obligated to assign.	○ Person who shows sufficient proprietary interest	

If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:

Name of the Deceased or Legally Incapacitated Inventor:

If the Applicant is an Organization check here. ☒

Organization Name	Yangtze Memory Technologies Co., Ltd.		
Mailing Address Information For Applicant:			
Address 1	18 Gaoxin 4th Road		
Address 2	East Lake High-Tech Development Zone		
City	Wuhan, Hubei	**State/Province**	
Country	CN	Postal Code	
Phone Number		Fax Number	
Email Address			

Additional Applicant Data may be generated within this form by selecting the Add button.

Assignee Information including Non-Applicant Assignee Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Micron Ex. 1002, p. 12
Micron v. YMTC
IPR2024-00790

PTO/AIA/14 (02-18)
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	Application Number	
Title of Invention	MULTIPLE-STACK THREE-DIMENSIONAL MEMORY DEVICE AND FABRICATION METHOD THEREOF	

Assignee 1

Complete this section if assignee information, including non-applicant assignee information, is desired to be included on the patent application publication. An assignee-applicant identified in the "Applicant Information" section will appear on the patent application publication as an applicant. For an assignee-applicant, complete this section only if identification as an assignee is also desired on the patent application publication.

If the Assignee or Non-Applicant Assignee is an Organization check here. ☒

Organization Name	Yangtze Memory Technologies Co., Ltd.

Mailing Address Information For Assignee including Non-Applicant Assignee:

Address 1	18 Gaoxin 4th Road		
Address 2	East Lake High-Tech Development Zone		
City	Wuhan, Hubei	**State/Province**	
Country i	CN	Postal Code	
Phone Number		Fax Number	
Email Address			

Additional Assignee or Non-Applicant Assignee Data may be generated within this form by selecting the Add button.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	4123.0350001
	Application Number	
Title of Invention	MULTIPLE-STACK THREE-DIMENSIONAL MEMORY DEVICE AND FABRICATION METHOD THEREOF	

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MULTIPLE-STACK THREE-DIMENSIONAL MEMORY DEVICE AND FABRICATION METHOD THEREOF

BACKGROUND

[0001] Flash memory devices have undergone rapid development. Flash memory devices can store data for a considerably long time without powering, and have advantages such as high integration level, fast access, easy erasing, and rewriting. To further improve the bit density and reduce cost of flash memory devices, three-dimensional NAND flash memory devices have been developed.

[0002] A three-dimensional (3D) NAND memory device includes one or more stacks of word lines (or gate electrodes) arranged over a substrate, with a plurality of semiconductor channels, through and intersecting word lines, into the substrate. A stack of word lines includes word lines of different levels/tiers stacking along a direction perpendicular to the substrate, where a different level/tier represents a different height from the surface of the substrate.

[0003] A multiple-stack (or multiple-level) 3D NAND memory device often includes multiple stacks of word lines arranged along the direction perpendicular to the substrate. Channel holes are respectively formed in each stack for the subsequent formation of semiconductor channels through the multiple-stack 3D memory device. This arrangement can have the advantages of, e.g., allowing more memory cells to be formed along the direction perpendicular to the substrate, reducing the number of photomasks during staircase formation, and avoiding substrate over etch during high aspect ratio etches. To form this multiple-stack memory device, supporting pillars are used in the fabrication process to provide mechanical support and prevent pattern collapse. However, the fabrication processes of semiconductor channels and supporting pillars are time-consuming and costly.

BRIEF SUMMARY

[0004] Embodiments of three-dimensional memory device architectures and fabrication methods therefore are disclosed herein. The disclosed structures and methods provide numerous benefits, including, but not limited to simplifying the fabrication process, reducing

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the size of the three-dimensional memory device, and improving the space utility of the chip which the three-dimensional memory device is formed on.

[0005] In some embodiments, a memory device includes a substrate and a multiple-stack staircase structure. The multiple-stack staircase structure can include a plurality of staircase structures stacked over the substrate. Each of the plurality of staircase structures can include a plurality of conductor layers, and each of the plurality of conductor layers is located between two insulating layers. In some embodiments, the memory device also includes a filling structure surrounding the multiple-stack staircase structure, a semiconductor channel extending through the multiple-stack staircase structure, and a supporting pillar extending through the multiple-stack staircase structure and the filling structure. The semiconductor channel can include unaligned sidewall surfaces, and the supporting pillar can include aligned sidewall surfaces.

[0006] In some embodiments, the multi-stack staircase structure includes a first staircase structure over the substrate and a second staircase structure over the first staircase structure.

[0007] In some embodiments, the supporting pillar extends from a top surface of the second staircase structure to a bottom surface of the first staircase structure.

[0008] In some embodiments, supporting pillar and the semiconductor channel include same filling layers.

[0009] In some embodiments, the supporting pillar and the semiconductor channel is each filled with at least one of a charge trapping film, a semiconductor channel film, and a dielectric core.

[0010] In some embodiments, the supporting pillar and the semiconductor channel are filled with different filling layers.

[0011] In some embodiments, the supporting pillar is filled with at least one of an insulating material and a pillar-support material surrounded by the insulating material. In some embodiments, the semiconductor channel is filled with at least one of a charge trapping film, a semiconductor channel film, and a dielectric core.

[0012] In some embodiments, the insulating material includes silicon oxide and the metal material includes at least one of copper, cobalt, nickel, and aluminum.

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[0013] In some embodiments, the memory device further includes a joint insulating layer between the first staircase structure and the second staircase structure, and an insulating cap layer over the second staircase structure.

[0014] In some embodiments, the memory device further includes a drain region over the semiconductor channel.

[0015] In some embodiments, the memory device further includes a connection layer in the semiconductor channel between two adjacent staircase structures. The connection layer can include a doped semiconductor material, and portions of the semiconductor channel separated by the connection layer can each form a semiconductor sub-channel.

[0016] In some embodiments, a method for forming a memory device includes forming a plurality of dielectric stacks stacked on one another over a substrate to create a multiple-stack staircase structure. Each one of the plurality of dielectric stacks can include a plurality of dielectric pairs arranged along a direction perpendicular to a top surface of the substrate. In some embodiments, the method further includes forming a multiple-stack staircase structure based on the plurality of dielectric stacks, forming a filling structure that surrounds the multiple-stack staircase structure, and forming a semiconductor channel extending through the multiple-staircase structure. The semiconductor channel can include unaligned sidewall surfaces. The method can further include forming a supporting pillar extending through at least one of the multiple-staircase structure and the filling structure. The supporting pillar can include aligned sidewall surfaces.

[0017] In some embodiments, forming the supporting pillar includes forming a photoresist layer over at least one of the filling structure and the multiple-stack staircase structure, and patterning the photoresist layer to form a patterned photoresist layer with an opening that exposes a portion of the filling structure. A location of the opening can correspond to a location of the supporting pillar. In some embodiments, forming the supporting pillar further includes using the patterned photoresist layer as an etch mask to etch through at least one of the filling structure and the multiple-stack staircase structure to form a pillar hole, wherein a bottom of the pillar hole contacts the substrate, and filling the pillar hole with a first material.

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[0018] In some embodiments, forming the semiconductor channel includes forming a first sub-channel hole in a first dielectric stack of the plurality of dielectric stacks and filling the first sub-channel hole with a sacrificial filling material to form a sacrificial filling structure. The method further includes forming a second dielectric stack over the first dielectric stack and forming a second sub-channel hole in the second dielectric stack. In some embodiments, the second sub-channel hole aligns with the sacrificial filling structure along the direction perpendicular to the top surface of the substrate and the second sub-channel hole adjoins the first sub-channel hole to form a channel hole through the plurality of dielectric stacks and into the substrate. In some embodiments, the method also includes removing the sacrificial filling structure in the first sub-channel hole, and filling the channel hole with a second material.

[0019] In some embodiments, the first material is same as the second material and are formed by same fabrication operations, and the same fabrication operations includes sequentially depositing at least one of a charge trapping film, a semiconductor channel film, and a dielectric core into the channel hole and the pillar hole.

[0020] In some embodiments, the pillar hole is formed before a formation of the second sub-channel hole.

[0021] In some embodiments, the pillar hole is formed before the formation of the second sub-channel hole and after the sacrificial filling structure.

[0022] In some embodiments, the pillar hole is formed after a formation of the first sub-channel hole and the second sub-channel hole.

[0023] In some embodiments, the first material is different from the second material and is formed by a different deposition operation than the second material.

[0024] In some embodiments, the first material includes at least one of an insulating material and a pillar-support material surrounded by the insulating material, and the second material includes at least one of a charge trapping film, a semiconductor channel film, and a dielectric core.

[0025] In some embodiments, the insulating material includes silicon oxide and the pillar-support material includes at least one of copper, cobalt, nickel, and aluminum.

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[0026] In some embodiments, forming the semiconductor channel includes forming a first semiconductor sub-channel in the first dielectric stack, forming a connection layer over the first semiconductor sub-channel, wherein the connection layer comprises a doped semiconductor material, and forming a second dielectric stack and a second semiconductor sub-channel in the second dielectric stack. The second semiconductor sub-channel can align with and adjoin the first semiconductor sub-channel to form a semiconductor channel extending through the plurality of dielectric stacks and into the substrate.

[0027] In some embodiments, forming the first semiconductor sub-channels includes forming a first sub-channel hole in the first dielectric stack of the plurality of dielectric stacks and depositing a second material into the first sub-channel hole. In some embodiments, forming the second semiconductor sub-channel hole includes forming the second dielectric stack over the first dielectric stack of the plurality of dielectric stacks and a second sub-channel hole in the second dielectric stack, and depositing the second material into the second sub-channel hole. The second sub-channel hole can align with and adjoin the first sub-channel hole along the direction perpendicular to the top surface of the substrate.

[0028] In some embodiments, the first material is same as the second material and are formed by same fabrication operations and the same fabrication operations includes sequentially depositing at least one of a charge trapping film, a semiconductor channel film, and a dielectric core into the channel hole and the pillar hole.

[0029] In some embodiments, the pillar hole is formed before a formation of the second sub-channel hole.

[0030] In some embodiments, the pillar hole is formed after the formation of the first semiconductor sub-channel and before the second sub-channel hole.

[0031] In some embodiments, the pillar holes are formed after a formation of the first semiconductor sub-channel and the second sub-channel hole.

[0032] In some embodiments, the first material is different from the second material and is formed by a different deposition operation than the second material.

[0033] In some embodiments, the first material includes at least one of an insulating material and a pillar-support material surrounded by the insulating material, and the second

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material includes at least one of a charge trapping film, a semiconductor channel film, and a dielectric core.

[0034] In some embodiments, the insulating material includes silicon oxide and the pillar-support material includes at least one of copper, cobalt, nickel, and aluminum.

[0035] In some embodiments, the pillar hole is formed after a formation of the multiple-stack staircase structure and the first sub-channel hole.

[0036] In some embodiments, a method for forming a memory device includes depositing a plurality of dielectric stacks one another over a substrate to form a multiple-dielectric-stack structure. Each one of the plurality of dielectric stacks can include a plurality of first material layer and second material layer alternatingly arranged along a direction perpendicular to a top surface of the substrate. The method can also include forming a first semiconductor sub-channel in a first dielectric stack of the plurality of dielectric stacks, and forming a second dielectric stack of the plurality of dielectric stacks over the first dielectric stack. The method can further include forming a second semiconductor sub-channel in the second dielectric stack. The second semiconductor sub-channel can align with the first semiconductor sub-channel along the direction perpendicular to the top surface of the substrate. The method can further include patterning the multiple-dielectric-stack structure to form a multiple-stack staircase structure.

[0037] In some embodiments, patterning the multiple-dielectric-stack structure includes a single staircase-forming patterning process.

[0038] In some embodiments, the staircase-forming patterning process includes forming a photoresist layer over the multiple-dielectric-stack structure, trimming the photoresist layer along a first direction parallel to a top surface of the substrate, and etching the multiple-dielectric-stack structure, using the trimmed photoresist layer as an etch mask to form a staircase.

[0039] In some embodiments, forming the first semiconductor sub-channel and the second semiconductor sub-channel include forming a first sub-channel hole in the first dielectric stack and a second sub-channel hole in the second dielectric stack, and filling the first sub-channel hole and the second sub-channel hole each with channel-forming layer.

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[0040] In some embodiments, the channel-forming materials include at least one of a charge trapping film, a semiconductor channel film, and a dielectric core.

[0041] In some embodiments, the method further includes forming a joint insulating material layer between the first dielectric stack, forming an opening in the joint insulating material layer to expose the first semiconductor sub-channel, and performing a recess etch to remove a top portion of the channel-forming layers of the first semiconductor sub-channel and form a recess region. The method can also include forming a connection layer in the recess region and patterning the joint insulating material layer to form a joint insulating layer.

[0042] In some embodiments, forming the connection layer includes depositing a doped semiconductor material.

[0043] In some embodiments, the doped semiconductor material includes doped silicon.

[0044] In some embodiments, the method further includes forming a drain region over the second semiconductor sub-channel.

BRIEF DESCRIPTION OF THE DRAWINGS

[0045] Aspects of the present disclosure are best understood from the following detailed description when read with the accompanying figures. It is noted that, in accordance with the common practice in the industry, various features are not drawn to scale. In fact, the dimensions of the various features may be arbitrarily increased or reduced for clarity of illustration and discussion. Multiple instances of an element may be duplicated where a single instance of the element is illustrated, unless absence of duplication of element is expressly described or clearly indicated otherwise.

[0046] FIGs. 1-12 are each an illustration of a cross-sectional view of a 3D memory device at different stages of an exemplary fabrication process, according to some embodiments.

[0047] FIG. 13 is an exemplary fabrication process to form a 3D memory device, according to some embodiments.

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DETAILED DESCRIPTION

[0048] Although specific configurations and arrangements are discussed, it should be understood that this is done for illustrative purposes only. A person skilled in the pertinent art will recognize that other configurations and arrangements can be used without departing from the spirit and scope of the present disclosure. It will be apparent to a person skilled in the pertinent art that the present disclosure can also be employed in a variety of other applications.

[0049] It is noted that references in the specification to "one embodiment," "an embodiment," "an example embodiment," "some embodiments," etc., indicate that the embodiment described may include a particular feature, structure, or characteristic, but every embodiment may not necessarily include the particular feature, structure, or characteristic. Moreover, such phrases do not necessarily refer to the same embodiment. Further, when a particular feature, structure or characteristic is described in connection with an embodiment, it would be within the knowledge of a person skilled in the pertinent art to effect such feature, structure or characteristic in connection with other embodiments whether or not explicitly described.

[0050] In general, terminology may be understood at least in part from usage in context. For example, the term "one or more" as used herein, depending at least in part upon context, may be used to describe any feature, structure, or characteristic in a singular sense or may be used to describe combinations of features, structures or characteristics in a plural sense. Similarly, terms, such as "a," "an," or "the," again, may be understood to convey a singular usage or to convey a plural usage, depending at least in part upon context.

[0051] It should be readily understood that the meaning of "on," "above," and "over" in the present disclosure should be interpreted in the broadest manner such that "on" not only means "directly on" something but also includes the meaning of "on" something with an intermediate feature or a layer therebetween, and that "above" or "over" not only means the meaning of "above" or "over" something but can also include the meaning it is "above" or "over" something with no intermediate feature or layer therebetween (i.e., directly on something).

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[0052] Further, spatially relative terms, such as "beneath," "below," "lower," "above," "upper," and the like, may be used herein for ease of description to describe one element or feature's relationship to another element(s) or feature(s) as illustrated in the figures. The spatially relative terms are intended to encompass different orientations of the device in use or operation in addition to the orientation depicted in the figures. The apparatus may be otherwise oriented (rotated 90 degrees or at other orientations) and the spatially relative descriptors used herein may likewise be interpreted accordingly.

[0053] As used herein, the term "substrate" refers to a material onto which subsequent material layers are added. The substrate itself can be patterned. Materials added on top of the substrate can be patterned or can remain unpatterned. Furthermore, the substrate can include a wide array of semiconductor materials, such as silicon, germanium, gallium arsenide, indium phosphide, etc. Alternatively, the substrate can be made from an electrically non-conductive material, such as a glass, a plastic, or a sapphire wafer.

[0054] As used herein, the term "layer" refers to a material portion including a region with a thickness. A layer can extend over the entirety of an underlying or overlying structure, or may have an extent less than the extent of an underlying or overlying structure. Further, a layer can be a region of a homogeneous or inhomogeneous continuous structure that has a thickness less than the thickness of the continuous structure. For example, a layer can be located between any pair of horizontal planes between, or at, a top surface and a bottom surface of the continuous structure. A layer can extend horizontally, vertically, and/or along a tapered surface. A substrate can be a layer, can include one or more layers therein, and/or can have one or more layer thereupon, thereabove, and/or therebelow. A layer can include multiple layers. For example, an interconnect layer can include one or more conductor and contact layers (in which contacts, interconnect lines, and/or vias are formed) and one or more dielectric layers.

[0055] As used herein, the term "nominal/nominally" refers to a desired, or target, value of a characteristic or parameter for a component or a process operation, set during the design phase of a product or a process, together with a range of values above and/or below the desired value. The range of values can be due to slight variations in manufacturing processes or tolerances. As used herein, the term "about" indicates the value of a given quantity that

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can vary based on a particular technology node associated with the subject semiconductor device. Based on the particular technology node, the term "about" can indicate a value of a given quantity that varies within, for example, 10–30% of the value (e.g., ±10%, ±20%, or ±30% of the value).

[0056] As used herein, the term "3D memory device" refers to a semiconductor device with vertically oriented strings of memory cell transistors (referred to herein as "memory strings," such as NAND strings) on a laterally-oriented substrate so that the memory strings extend in the vertical direction with respect to the substrate. As used herein, the term "vertical/vertically" means nominally perpendicular to the lateral surface of a substrate.

[0057] In the present disclosure, for ease of description, "tier" is used to refer to elements of substantially the same height along the vertical direction. For example, a word line and the underlying gate dielectric layer can be referred to as "a tier," a sacrificial layer and the underlying insulating layer can together be referred to as "a tier," a word line and the underlying insulating layer can together be referred to as "a tier," word lines of substantially the same height can be referred to as "a tier of word lines" or similar, and so on.

[0058] The trend in three-dimensional NAND memory industry includes the reduction of device dimensions and the simplification of fabrication process. In a multiple-stack 3D memory device, word lines (control gate electrodes) of multiple stacks are arranged along a direction perpendicular to the top surface of a substrate. A "stack" refers to a pile of objects, arranged along a designated direction. These word lines are arranged to form a multiple-stack staircase structure. Memory cells for storing data are embedded in stacks of word lines, and the semiconductor channels formed through the stacks of word lines. This configuration allows more memory cells to be formed within a unit area.

[0059] To form a multiple-stack 3D NAND memory device, word lines of different tiers in different stacks are formed by replacing sacrificial material layers with a conductive material in the multiple-stack staircase structure. Supporting pillars are formed through the multiple-stack staircase structure to prevent pattern collapse during the formation of word lines. In an example, multiple dielectric stacks or multiple stacks of dielectric pairs (e.g., sacrificial material layer/insulating material layer pairs) are formed sequentially along a direction perpendicular to the surface of a substrate. The multiple dielectric stacks can

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include the same number of different numbers of dielectric stairs, e.g., 32 tiers, 48 tiers, and 64 tiers. The dielectric stack at the bottom (e.g., a lower dielectric stack that is closest to the top surface of the substrate) is first formed, and sub-channel holes and sub-pillar holes are formed in this stack. A patterning process is performed on the dielectric pairs of the lower dielectric stack to form a staircase structure (e.g., a lower staircase structure). Another dielectric stack is then formed over the lower dielectric stack and undergoes a similar fabrication process to form an upper staircase structure with sub-channel holes and sub-pillar holes. The sub-channel holes and the sub-pillar holes in the upper staircase structure align and adjoin the sub-channel holes and the sub-pillar holes in the lower staircase structure along the direction perpendicular to the surface of the substrate. The upper staircase structure and the lower staircase structure form the multiple-stack staircase structure. The adjoined sub-channel holes and adjoined sub-pillar holes are then filled with suitable materials to form semiconductor channels and supporting pillars, respectively. In the present disclosure, sub-channel holes and sub-pillar holes respectively refer to the cavity structures formed in one dielectric stack/staircase structure, and are used to merely distinguish the channel hole and pillar hole (adjoined cavity structure) through the multiple-stack staircase structure. The terms "sub-channel hole" and "sub-pillar hole" do not imply any difference in other aspects such as fabrication order or functions.

[0060] In this fabrication process, dielectric stacks (e.g., upper dielectric stack and lower dielectric stack) are patterned separately to form respective staircase structures (e.g., upper staircase structure and lower staircase structure), and separate photomasks are used to perform the patterning processes. Sub-channel holes and sub-pillar holes of different staircase structure are formed before the deposition of next dielectric stack. Semiconductor channels and supporting pillars through the multiple-stack staircase structure are then often formed by respectively adjoining sub-channel holes and sub-pillar holes of adjacent dielectric staircase structures along the direction perpendicular to the surface of the substrate and filling the adjoined sub-channel holes and sub-pillar holes with suitable materials, such as materials that fill semiconductor channels.

[0061] The fabrication process described above can have several issues. First, because a different photomask (or a different set of photomasks) is often used to pattern sub-channel

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holes and sub-pillar holes of each dielectric stack, the number of photomasks and corresponding photolithography operations used to form multiple-stack staircase structures can be undesirably large, increasing cost and processing time of the fabrication process. Second, because an upper dielectric stack is often formed after the formation of the lower staircase structure and its dielectric filling structure (e.g., the lower dielectric filling structure), processing (e.g., etching) on the lower staircase and the lower dielectric filling structure often affect film qualities of the upper dielectric stack. For example, topography of the lower staircase and the lower dielectric filling structure can cause defects in the upper dielectric stack, adversely affect the film quality of the upper dielectric stack. Third, sub-channel holes and sub-pillar holes of the same dielectric stack often have different dimensions and are often formed from the same patterning/etching process, making it challenging to form them together with high uniformity, Further, because channel holes and pillar holes through the multiple-stack staircase structure are formed by adjoining sub-channel holes and sub-pillar holes of each staircase structure along the direction perpendicular to the surface of the substrate, the etching and aligning of sub-channel holes and sub-pillar holes may require higher precision control.

[0062] Inner sidewall (or sidewall) of a pillar hole through the memory structure can be formed by respectively adjoining sidewalls of supporting pillars of the multiple staircase structures stacked together. A supporting pillar formed by the fabrication processes described above can be referred to having an "adjoined/connected sidewall," which can include one or more connection portion formed by the adjoining of sub-pillar holes (e.g., at the interface of two adjoined sidewalls). The sidewall can thus have unaligned (or disjointed) surfaces at the connection portions. The unaligned surfaces can refer to the inconsistent hole dimensions caused by etching holes with high aspect-ratio (e.g., greater than 4). For example, when a first sub-pillar hole adjoins a second sub-pillar hole underneath, the diameter of the bottom of the first sub-pillar hole can be smaller than the diameter of the top of the second sub-pillar hole, creating unaligned surfaces along the vertical direction at the adjoining interface. In contrast, a pillar hole formed without adjoining sub-pillar holes can be referred to having a sidewall of aligned (or non-disjointed) surfaces. For example, the pillar hole formed by the

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present disclosure can extend through the memory structure and can have aligned sidewall surfaces.

[0063] For simplicity, the fabrication process of repeatedly etching dielectric pairs of a dielectric stack to from a staircase structure based on the dielectric stack is referred to as a "staircase-forming patterning" process. Each staircase-forming pattern can include a plurality of repeated etching/patterning of dielectric pairs of the respective dielectric stack. In some embodiments, two staircase-forming patterning processes are often employed to form a two-stack staircase structure.

[0064] The present disclosure describes structures and methods for forming a 3D memory device. According to the disclosed structures and methods, dielectric pairs of multiple stacks that form a multiple-stack memory device are patterned by one staircase-forming patterning process to form the multiple-stack staircase structure. Etching of the dielectric pairs of the multiple dielectric stacks can be performed after the dielectric pairs of the multiple dielectric stacks are deposited. Pillar holes through the multiple-stack staircase structure can be formed after the formation of the multiple-stack staircase structures by one patterning process. Pillar holes can be formed, e.g., before or after the formation of the channel holes of the upper dielectric stack. Supporting pillars of the memory device can be formed by filling the pillar holes with any suitable materials, e.g., the same material that forms the semiconductor channels employing the film deposition of semiconductor channels. Similar processes can also be used to form supporting pillars in a double-channel memory device.

[0065] By using the disclosed structures and methods, multiple-stack staircase structures can be formed by one staircase-forming patterning process, thereby avoiding multiple patterning of different dielectric stacks. A reduced number of photomasks and photolithography processes can be used to form multiple-stack staircase structures with semiconductor channels and supporting pillars. The formation of 3D memory devices can be simplified and less time consuming. Meanwhile, formation of supporting pillars is compatible with the formation of multiple-stack staircase structures. Less patterning is needed for the formation of supporting pillars and the fabrication process of the 3D memory

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device is thus simplified and less costly which can in turn improves device yield and performance.

[0066] For illustrative purposes, a 3D NAND memory device is used to describe the present disclosure. The exemplary 3D NAND memory device includes an upper stack of word lines and a lower stack of word lines, which are respectively formed from an upper dielectric stack and a lower dielectric stack. The disclosed methods can be used to form any suitable multiple-stack memory device with an increased number of stacks. In various embodiments, the upper dielectric stack can represent the last dielectric stack of the multiple dielectric stacks.

[0067] In the present disclosure, a "staircase structure" or a "stepped cavity structure," or similar refer to a structure having stepped surfaces. In the present disclosure, "stepped surfaces" refer to a set of surfaces that include at least two horizontal surfaces (e.g., along x-y plane) and at least two (e.g., first and second) vertical surfaces (e.g., along the z axis) such that each horizontal surface is adjoined to a first vertical surface that extends upward from a first edge of the horizontal surface, and is adjoined to a second vertical surface that extends downward from a second edge of the horizontal surface. A "step" or "staircase" refers to a vertical shift in the height of a set of adjoined surfaces. In the figures of the present disclosure, x axis propagates along a direction perpendicular to the y-z plane.

[0068] In the present disclosure, a dielectric stack or a stack of dielectric pairs refers to a pile of (or a plurality of) dielectric pairs stacked along the direction perpendicular to the top surface of the substrate. The dielectric stack can undergo a patterning and/or etching process to form a staircase structure. For example, a lower/bottom dielectric stack can be patterned/etched to form a lower/bottom staircase structure, and so on. Accordingly, multiple dielectric stacks, one on top of another over the substrate, can be patterned/etched to form a multiple-stack staircase structure. Channel holes formed in each staircase structure can align with and adjoin channel holes of adjacent (e.g., upper or lower) staircase structure to form adjoined/combined channel holes through the multiple-stack staircase structure. The term "through" an object refers to being from the top surface/portion to the bottom surface/portion of the object. For example, channel holes through each staircase structure can be adjoined to form channel holes through the multiple-stack staircase structure, and pillar holes can be

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formed to be through the memory structure. For descriptive simplicity, "multiple-stack staircase structure" can be interchangeable with "staircase structure" in the embodiments.

[0069] Fabrication processes to form a 3D memory device are illustrated. FIGs. 1-6 illustrate exemplary processes to form supporting pillars through a multiple-stack staircase structure of a 3D multiple-stack memory device, and FIGs. 7-12 illustrate an exemplary process to form the multiple-stack staircase structure in the 3D multiple-stack memory device.

[0070] FIG. 1 illustrates a cross-sectional view of a memory structure 100 at the beginning of a fabrication process to form a 3D NAND memory device, according to some embodiments. As shown in FIG. 1, memory structure 100 includes a substrate 107, a first doped region 106 in substrate 107, a second doped region 105 in first doped region 106, a dielectric layer 104 over substrate 107, a plurality of transistors 108 over substrate 107 and covered by an isolation layer 109, and a first dielectric stack 103 over dielectric layer 104 and isolation layer 109. Memory structure 100 can be divided into a core region 110 and a periphery region 120, for illustrative purposes. Periphery region 120 can include the plurality of transistors 108 for providing control signals and can surround core region 110. Periphery region 120 can also be under core region 110, depending on the type of the memory device.

[0071] In core region 110, first dielectric stack 103 (e.g., lower dielectric stack) can include a plurality of dielectric pairs repeatedly arranged along a direction perpendicular to the top surface of substrate 107 (e.g., the z axis). A dielectric pair can include a sacrificial material layer and an insulating material layer. First dielectric stack 103 can include sacrificial material layers and insulating material layers alternatingly stacked along the z axis. In a dielectric pair, 102 and 101 can each be one of a sacrificial material layer and an insulating material layer. In the present disclosure, 102 represents an insulating material layer and 101 represents a sacrificial material layer. The sacrificial material layers 101 and the insulating material layers 102 can include different materials. In some embodiments, sacrificial material layers 101 includes silicon nitride and insulating material layers 102 include silicon oxide. In subsequent fabrication processes, memory cells can be formed in core region 110. In some embodiments, dielectric layer 104 is a gate dielectric layer and includes a suitable oxide, e.g., silicon oxide.

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[0072] Periphery region 120 includes any peripheral devices (e.g., represented by transistors 108), isolation layer 109 over the peripheral devices, and a plurality of dielectric pairs repeatedly arranged over the peripheral devices. Isolation layer 109 can include any suitable insulating materials (e.g., silicon oxide) and can protect and isolate the peripheral devices from other devices or structures. In some embodiments, first doped region 106 includes a deep N-well (DNW) and second doped region 105 includes a high-voltage P well (HVPW). For illustrative purposes, only elements relevant to the present disclosure are depicted and labeled in the figures. In some embodiments, peripheral devices are formed prior to the deposition of first dielectric stack 103. Due to the height of the peripheral devices, dielectric pairs of first dielectric stack 103 can have a vertical shift in the height between core region 110 and peripheral region 120.

[0073] In some embodiments, substrate 107 includes any suitable material for forming the three-dimensional memory device. For example, substrate 107 can include silicon, silicon germanium, silicon carbide, silicon on insulator (SOI), germanium on insulator (GOI), glass, gallium nitride, gallium arsenide, and/or other suitable III-V compound. First doped region 106 and second doped region 105 can each be formed by a suitable doping process such as ion implantation.

[0074] Memory structure 100 provides the base for the fabrication of the 3D memory device and can be formed using any suitable processes. For example, memory structure 100 can be formed by depositing a dielectric material stack (not shown) over substrate 107 and planarizing the dielectric material stack. In some embodiments, substrate 107 with first doped region 106 and second doped region 105 is provided, and peripheral devices (e.g., the plurality of transistors 108) and isolation layer 109 are formed over substrate 107. A dielectric film can be deposited over substrate 107 and patterned to form dielectric layer 104. A dielectric material stack can be formed over dielectric layer 104 and isolation layer 109 by alternatingly depositing insulating material layers 102 and sacrificial material layers 101 over substrate 107. Sacrificial material layer 101 and insulating material layer 102 can have same or different thicknesses. A sacrificial material layer 101 can include any suitable material different from an insulating material layer 102. For example, in some embodiments, sacrificial material layers 101 can include poly-crystalline silicon, silicon nitride, poly-

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crystalline germanium, and/or poly-crystalline germanium-silicon. In some embodiments, sacrificial material layers 101 include silicon nitride. Insulating material layers 102 can include any suitable insulating materials, e.g., silicon oxide. The deposition of sacrificial material layers 101 and insulating material layers 102 can include any suitable deposition methods such as plasma-enhanced CVD (PECVD), sputtering, atomic layer deposition (ALD), and so on.

[0075] Further, a planarization process can be performed to planarize the dielectric material stack into a suitable thickness. First dielectric stack 103 can thus be formed. In some embodiments, the top surface of core region 110 levels with the top surface of periphery region 120. In some embodiments, sacrificial material layer 101 is exposed in core region 110 by the planarization process. In some embodiments, the planarization process includes a chemical mechanical planarization (CMP) process.

[0076] FIG. 2 illustrates a cross-sectional view of memory structure 200 formed based on memory structure 100, according to some embodiments. As shown in FIG. 2, memory structure 200 can be formed by forming a plurality of first sub-channel holes 205 in first dielectric stack 103, filling first sub-channel holes 205 with a sacrificial filling structure 207, and forming a second dielectric stack 206 (e.g., upper dielectric stack) over first dielectric stack 103. First dielectric stack 103 and second dielectric stack 206 can form two-stack dielectric stack 203 (the term "dielectric stack 203" can also refer to two-stack dielectric stack 203). For illustrative purposes, memory structure 200 is divided into core region 210 and periphery region 220, each respectively corresponding to core region 110 and periphery region 120 of FIG. 1. In some embodiments, the top surface of core region 210 levels with the top surface of periphery region 220.

[0077] Memory structure 200 can be formed using any suitable processes. In some embodiments, first sub-channel holes 205 are first formed in first dielectric stack 103 before second dielectric stack 206 is deposited thereon. First sub-channel holes 205 can be formed by, e.g., patterning a photoresist layer using photolithography over first dielectric stack 103 to form openings in the patterned photoresist layer, and performing an etching process to remove the dielectric materials in first dielectric stack 103 defined by the openings. The locations of the openings can correspond to the locations of first sub-channel holes 205. The

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etching process can include any suitable wet etch and/or dry etch. In some embodiments, an anisotropic etch is performed to remove the materials vertically (e.g., along the z axis). First sub-channel holes 205 can extend through first dielectric stack 103 and substantially into second doped region 105 and/or extend into substrate 107. In some embodiments, first sub-channel holes 205 can have a substantially rectangular cross-section shape. In some embodiments, first sub-channel holes 205 can have a substantially trapezoidal cross-section shape. In some embodiments, the horizontal dimension (e.g., along the x axis) of first sub-channel hole 205 can, e.g., decrease towards the substrate due to fabrication processes. Any variation of the shape of first sub-channel hole 205 is still within the scope of the present disclosure.

[0078] A sacrificial filling material can further be deposited to fill in first sub-channel holes 205. Any suitable deposition process can be performed to deposit the sacrificial filling material into first sub-channel holes 205 and other areas over first dielectric stack 103. The sacrificial filling material deposited in first sub-channel hole 205 can form sacrificial filling structure 207. Any suitable planarization method (e.g., CMP) and/or recess etch (e.g., dry etch and/or wet etch) can be performed to remove any excessive sacrificial filling material over first dielectric stack 103. The sacrificial filling material can include any suitable non-conductive material (e.g., amorphous silicon, polysilicon, silicon germanium, amorphous carbon, silicon nitride, diamond-like carbon, and porous organosilicate glass), and can be deposited by any suitable deposition method such as CVD and/or spin coating.

[0079] In some embodiments, an insulating layer (not shown in FIG. 2) can be deposited over first dielectric stack 103. The insulating layer can include a suitable insulating material such as one or more materials that form first dielectric stack 103. The insulating layer can be formed before the formation of first sub-channel holes 205 or after the deposition of the sacrificial filling material. If the insulating layer is formed before the formation of first sub-channel holes 205, the formation of first sub-channel holes 205 can include forming openings in the insulating layer and removing portions of first dielectric stack 103 exposed by the openings. A suitable planarization method (e.g., CMP) and/or recess etch (e.g., dry etch and/or wet etch) can be performed to remove any excessive material of the insulating layer over first dielectric stack 103.

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[0080] In some embodiments, a channel epitaxial portion 204 can be formed at the bottom of a first sub-channel hole 205 by a suitable deposition process. Channel epitaxial portion 204 can function as a portion of a semiconductor channel. For example, a selective epitaxial deposition can be performed to deposit a semiconductor material at the bottom of first sub-channel hole 205. In some embodiments, channel epitaxial portion 204 includes a single crystalline semiconductor in epitaxial alignment (e.g., same crystal orientation) with second doped region 105. In some embodiments, channel epitaxial portion 204 includes single crystalline silicon. The top surface of channel epitaxial portion 204 can be between a pair of sacrificial material layers 101 and the periphery of epitaxial channel portion 204 can be in physical contact with insulating material layers 102.

[0081] Further, second dielectric stack 206 can be formed over first dielectric stack 103. In some embodiments, second dielectric stack 206 is formed over core region 210 and periphery region 220. Second dielectric stack 206 can include a plurality of dielectric pairs, each including a sacrificial material layer 201 and an insulating material layer 202. Sacrificial material layers 201 and insulating material layers 202 can be arranged alternatingly along the z axis. First dielectric stack 103 and second dielectric stack 206 can form a dielectric stack 203. The structure and deposition methods to form second dielectric stack 206 can refer to the structure and deposition methods of first dielectric stack 103.

[0082] FIG. 3 illustrates an exemplary memory structure 300 formed based on memory structure 200, according to some embodiments. As shown in FIG. 3, memory structure 300 can be formed by forming a two-stack staircase structure 303 from dielectric stack 203, filling space formed by the formation of staircase structure 303 with a dielectric filling structure 311, and forming a plurality of pillar holes 309. For illustrative purposes, memory structure 300 is divided into core region 310 and periphery region 320, each respectively corresponding to core region 210 and periphery region 220 of FIG. 2.

[0083] The portion of dielectric stack 203 in periphery region 320 can be removed and the top surface of isolation layer 109 can be exposed. Staircase structure 303 can be formed by repetitively patterning/etching sacrificial material layers 201 and insulating material layers 202 of dielectric stack 203 in core region 310. Dielectric pairs of different tiers can be etched to form staircases extending along the x-y plane. Each staircase can include an insulating

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layer (e.g., 302) and a pairing sacrificial layer (e.g., 301). The dielectric stacks can be patterned/etched through one staircase-forming patterning process to form staircase structure 303 (or multiple-stack staircase structure 303 or two-stack staircase structure 303). Details of the formation of staircase structure 303 are described in FIGs. 7-12.

[0084] Further, a dielectric filling material can be deposited after staircase structure 303 is formed to fill in the space formed by the removal of the portions of dielectric stack 203. Dielectric filling structure 311 is deposited in periphery region 320 and core region 310 to fill in the space formed by the removal of the portions of dielectric stack 203. A suitable planarization method (e.g., CMP and/or recess etch) can be performed to remove any excessive dielectric filling material overlying the topmost surface of staircase structure 303. The remaining portion of the deposited dielectric filling material (e.g., over staircase structure 303 and isolation layer 109) can form dielectric filling structure 311 that surrounds staircase structure 303. Dielectric filling structure 311 can be retro-stepped. In the present disclosure, a retro-stepped element refers to an element that has stepped surfaces and a horizontal cross-section area that increases monotonically as a function of a vertical distance from a top surface of a substrate on which the element is present. Dielectric filling structure 311 can include any suitable dielectric material that provides electrical insulation for staircase structure 300 and can be deposited by any suitable deposition methods such as CVD, ALD, and/or PVD. In some embodiments, dielectric filling structure 311 includes silicon oxide and is formed by CVD. An insulating cap material layer can be deposited to cover staircase structure 303 and dielectric filling structure 311. The insulating cap material layer can have sufficient thickness along the z axis to allow drain regions to be formed within. The insulating cap material layer can include any suitable insulating material such as silicon oxide.

[0085] Further, pillar holes 309 can be formed in memory structure 300. Pillar holes 309 can be formed in any suitable location in core region 310, e.g., intersecting with staircase structure 303. In some embodiments, pillar holes 309 can be formed adjacent to first sub-channel holes 205. In some embodiments, pillar holes 309 can be formed in the staircase structure. In some embodiments, some pillar holes 309 can be formed in a portion of peripheral region 320. Pillar holes 309 can be formed by, e.g., patterning a photoresist layer

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using photolithography over the insulating cap material layer over staircase structure 303 and dielectric filling structure 311 to form openings in the patterned photoresist layer that correspond to the locations of pillar holes 309, and performing an etching process (e.g., using the patterned photoresist layer as an etch mask) to remove the portions of insulating cap material layer and portions of staircase structure 303 exposed/defined by the openings. The etching process can include any suitable wet etch and/or dry etch. In some embodiments, an anisotropic etch is performed to etch portions of the insulating cap material layer, staircase structure 303 and dielectric filling structure 311 to form pillar holes 309. The patterned photoresist layer can then be removed after the formation of pillar holes 309. Insulating cap layer 312 can then be formed. Pillar hole 309 can extend from a top surface of insulating cap layer 312 to substrate 107. The cross-section of pillar hole 309 along the x-z plane can have a trapezoid shape. In some embodiments, a horizontal dimension (e.g., along the x axis) of pillar hole 309 can, e.g., decrease towards the substrate due to fabrication processes. Any variation of the shape of pillar hole 309 is still within the scope of the present disclosure. In some embodiments, pillar holes 309 are formed before the formation of second sub-channel holes of upper dielectric stack. In some embodiments, pillar holes 309 are formed after the formation of second sub-channel holes of upper dielectric stack.

[0086] FIG. 4 illustrates an exemplary memory structure 400 formed based on memory structure 300, according to some embodiments. As shown in FIG. 4, memory structure 400 can be formed by forming a plurality of second sub-channel holes over first sub-channel holes 205, filling the first and second sub-channel holes and pillar holes 309 to form semiconductor channels 415 and supporting pillars 409, and forming drain regions 419 over semiconductor channels 415 and dummy drain regions 414 over supporting pillars 409. For illustrative purposes, core region is described in FIG. 4.

[0087] To form second sub-channel holes, a photoresist layer can be formed over insulating cap layer 410. The photoresist layer can cover/close the top portions of pillar holes 309 so that the subsequent etching of second sub-channel holes has little or no impact on pillar holes 309. The photoresist layer can then be patterned to form openings that expose portions of insulating cap layer 410 and correspond to the locations of the second sub-channel holes. The patterned photoresist layer can be used as an etch mask to remove

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portions of insulating cap layer 410 and portions of staircase structure 303 exposed/defined by the openings. Insulating cap layer 410 can be formed. The horizontal projection (e.g., on the x-y plane) of the second sub-channel holes can substantially overlap with the horizontal projection of first sub-channel holes 205. In some embodiments, the second sub-channel holes substantially align with respective first sub-channel holes 205 along the z axis. In some embodiments, the number of second sub-channel holes equals to the number of first sub-channel holes 205, and the horizontal projection of each second sub-channel hole overlaps with the horizontal projection of a respective first sub-channel hole 205 underneath. The patterned photoresist layer can then be removed after the formation of the second sub-channel holes.

[0088] In some embodiments, the second sub-channel holes can each adjoin respective first sub-channel hole 205 so that the formed channel hole combines the volumes of first sub-channel hole 205 and the respective second sub-channel hole, and extends through staircase structure 303. In some embodiments, the bottom of second sub-channel hole exposes sacrificial filling structure 207 of the respective first sub-channel hole 205.

[0089] Inner sidewall (or sidewall) of a channel hole extending through staircase structure 303 can be formed by respectively adjoining sidewalls of first sub-channel holes 205 and respective second sub-channel holes stacked together. A semiconductor channel formed by these fabrication operations can be referred to having an "adjoined/connected sidewall," which can include one or more connection portion formed by the adjoining of sub-pillar holes (e.g., at the interface of two adjoined sidewalls). The sidewall can thus have unaligned surfaces at the connection portions. The unaligned surfaces can refer to the inconsistent hole dimensions caused by etching holes with high aspect-ratio (e.g., greater than 4). For example, when a second sub-channel hole adjoins a first sub-channel hole, the diameter of the bottom of the second sub-channel hole can be smaller than the diameter of the top of the first sub-pillar hole, creating unaligned surfaces along the vertical direction at the adjoining interface. In contrast, a channel hole formed without adjoining sub-pillar holes can be referred to having a sidewall of aligned surfaces. For example, the channel hole formed by the present disclosure can extend through the memory structure and can have unaligned sidewall surface.

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[0090] Sacrificial filling structures 207 can then be removed by a suitable etching process (e.g., dry etch and/or wet etch). For example, a selective etch can be performed. The selective etch can be an isotropic etching process or an anisotropic etching process.

[0091] Further, channel holes and pillar holes 309 can be filled by the same fabrication operations (e.g., at the same time). A series of channel-forming layers can be sequentially deposited into the channel holes (e.g., having the combined volume of first sub-channel holes 205 and adjoined second sub-channel holes) and pillar holes 309 to fill in the channel holes and pillar holes 309.

[0092] In some embodiments, a charge trapping film 416 (e.g., or sacrificial film) is deposited over the sidewall of channel holes and pillar holes 309. Charge trapping film 416 can include one or more block dielectric layers over the sidewall of channel hole to insulate other layers in the channel hole from staircase structure 303. Charge trapping film 416 can also include a storage unit layer (memory layer) over and surrounded by the block dielectric layers for trapping charges and forming a plurality of charge storage regions along the z axis. Charge trapping film 416 can also include a tunneling layer (e.g., tunneling dielectric) over and surrounded by the memory layer. Charge tunneling can be performed through the tunneling layer under a suitable electric bias.

[0093] The one or more block dielectric layers can include a first block layer, which includes a dielectric metal oxide layer with a relatively high dielectric constant. The term "metal oxide" can include a metallic element and non-metallic elements such as oxygen, nitrogen, and other suitable elements. For example, the dielectric metal oxide layer can include aluminum oxide, hafnium oxide, lanthanum oxide, yttrium oxide, tantalum oxide, silicates, nitrogen-doped compounds, alloys, etc. The first block layer can be deposited, for example, by CVD, ALD, pulsed laser deposition (PLD), liquid source misted chemical deposition, and/or other suitable deposition methods.

[0094] The one or more block dielectric layers can also include a second block layer, which includes another dielectric layer over the dielectric metal oxide. The other dielectric layer can be different from the dielectric metal oxide layer. The other dielectric layer can include silicon oxide, a dielectric metal oxide having a different composition than the first block layer, silicon oxynitride, silicon nitride, and/or other suitable dielectric materials. The

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second block layer can be deposited, for example, by low pressure chemical vapor deposition (LPCVD), ALD, CVD, and/or other suitable deposition methods. In some embodiments, the one or more block dielectric layers include silicon oxide, which is formed by CVD.

[0095] The storage unit layer can be sequentially formed over the one or more block dielectric layers. The storage unit layer can include a charge trapping material, e.g., a dielectric charge trapping material (e.g., silicon nitride) and/or a conductive material (e.g., doped polysilicon). In some embodiments, the dielectric charge trapping material includes silicon nitride and can be formed by CVD, ALD, PVD, and/or other suitable deposition methods.

[0096] The tunneling layer can be sequentially formed over the memory layer. The tunneling layer can include silicon oxide, silicon nitride, silicon oxynitride, dielectric metal oxides, dielectric metal oxynitride, dielectric metal silicates, alloys, and/or other suitable materials. The tunneling layer can be formed by CVD, ALD, PVD, and/or other suitable deposition methods. In some embodiments, the tunneling layer includes silicon oxide, which is formed by CVD.

[0097] Further, a semiconductor channel film 417 can be formed over charge trapping film in channel holes and pillar holes 309. Semiconductor channel film 417 can include one or more layers of any suitable semiconductor materials such as silicon, silicon germanium, germanium, III-V compound material, II-VI compound material, organic semiconductor material, and/or other suitable semiconductor materials. Semiconductor channel film 417 can be formed by a suitable deposition method such as metal-organic chemical vapor deposition (MOCVD), LPCVD, CVD, and/or other suitable deposition methods. In some embodiments, semiconductor channel film 417 is formed by depositing a layer of amorphous silicon using CVD, followed by an annealing process such that the amorphous silicon is converted to single-crystalline silicon. In some embodiments, other amorphous material can be annealed to be crystallized to form semiconductor channel film 417.

[0098] Further, dielectric core 418 can be formed by depositing a suitable dielectric material over semiconductor channel films in channel holes and pillar holes. Dielectric core 418 can fill in the space at the center of the channel hole and the pillar hole. Dielectric core 418 can include a suitable dielectric material such as silicon oxide and/or organosilicate

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glass. Dielectric core 418 can be formed by a suitable conformal deposition method (e.g., LPCVD) and/or self-planarizing deposition method (e.g., spin coating). In some embodiments, dielectric core 418 includes silicon oxide and is formed by LPCVD. In some embodiments, a suitable planarization process (e.g., CMP and/or recess etch) is performed to remove any excessive materials over the top of staircase structure 303.

[0099] When different layers (e.g., charge trapping film 416, semiconductor channel film 417, and dielectric core 418) are being formed in the channel holes, the materials for forming those layers can also be respectively deposited in pillar holes 309. Because these layers have little or no active electrical functions, for illustrative purposes, these layers in pillar holes 309 are referred to as dummy charge trapping films 411, dummy semiconductor channel films 417, and dummy dielectric cores 413. Supporting pillars 409 can thus be formed.

[0100] Further, top portions of supporting pillars 409 and semiconductor channels 415 can be removed by any suitable recess etching processes. In some embodiments, a selective etch is performed to remove top portions of supporting pillars 409 and semiconductor channels 415. In some embodiments, the depth of the recess region is substantially equal to the thickness of insulating cap layer 410.

[0101] Further, drain regions 419 (e.g., over semiconductor channels 415) and dummy drain regions 414 (e.g., over supporting pillars 409) can be formed in the recess regions. Drain regions 419 and dummy drain regions 414 can be formed by, e.g., depositing a doped semiconductor material in the recess regions. The deposition can include any suitable deposition methods, such as CVD and/or area selective deposition (ASD). Optionally, an ion implantation process is employed to adjust the doping level of the recess region. The doped semiconductor material can include, for example, doped polysilicon. The doped semiconductor material can have a conductivity type that is opposite from the conductivity type of substrate 107. Excess portions of the deposited doped semiconductor material can be removed from above the top surface of insulating cap layer 410 by, e.g., CMP and/or a recess etch.

[0102] FIG. 5 illustrates an exemplary memory structure 500 formed based on memory structure 200, according to some embodiments. Different from memory structure 400, in memory structure 500, pillar holes 509 can be formed after the formation of staircase

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structure 303, semiconductor channels 501, and drain regions 505. Semiconductor channels 501, drain regions 505, and insulating cap layer 510 can respectively be the same as or similar to semiconductor channels 415, drain regions 419, and insulating cap layer 410 of FIG. 4. Charge trapping film 502, semiconductor channel film 503, and dielectric core 504 can be respectively the same as or similar to charge trapping film 416, semiconductor channel film 417, and dielectric core 418 of FIG. 4.

[0103] In an example, after the formation of dielectric filling structure 311 and the insulating cap material layer, second sub-channel holes can be formed in staircase structure 303. The second sub-channel holes can be the same as or similar to the second-channel holes depicted in FIG. 4. The second sub-channel holes can be formed by any suitable process. For example, a photoresist layer can be formed to cover at least a top surface of staircase structure 303. The photoresist layer can be patterned to form openings that expose portions of the insulating cap material layer. The locations of the openings can correspond to the locations of the second sub-channel holes. The patterned photoresist layer can then be used as an etch mask to remove portions of exposed insulating cap material layer and staircase structure 303 to form second sub-channel holes each extending from the top surface of the insulating cap layer 510 to the respective first sub-channel hole. Channel holes that extend from the top surface of the staircase structure 303 into substrate 107 can be formed. The patterned photoresist layer can be removed after the formation of the second sub-channel holes.

[0104] Channel-forming layers (similar to or the same as the channel-forming layers depicted in FIG. 4) can be formed to fill in the channel holes and form semiconductor channels 501. Further, top portions of semiconductor channels 501 can be removed and filled with a doped semiconductor material (e.g., doped polysilicon) to form drain regions 505. Drain regions 505 can have a thickness that is substantially the same as the insulating cap layer 510. A patterned photoresist layer with openings that define the locations of the pillar holes 509 can then be formed over the insulating cap layer 510. In some embodiments, the openings expose portions dielectric filing structure 311. A suitable etching process (e.g., dry etch and/or wet etch) can be performed (e.g., using the patterned photoresist layer) to remove portions of staircase structure 303 and dielectric filling structure 311 so that pillar holes 509

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can be formed through insulating cap layer 510, staircase structure 303, and dielectric filling structure 311.

[0105] Any suitable pillar-filling materials (e.g., insulating materials such as silicon oxide and/or silicon nitride) can be deposited to fill in pillar holes 509 and form supporting pillars. In some embodiments, the pillar-filling materials can include pure dielectric materials such as pure silicon oxide and/or pure silicon nitride. In some embodiments, suitable dopants/impurities can be doped into the silicon oxide and/silicon nitride to enhance support. In some embodiments, the pillar-filling material includes an insulating liner/spacer layer is formed over the sidewalls of pillar holes 509 and another support material that fills up the rest of pillar holes 509. In some embodiments, the insulating liner/spacer layer surrounds the support material. Any suitable material with sufficient stiffness and/or support functions can be used as the support material. For example, the support material can include one or more of copper, cobalt, nickel, and aluminum.

[0106] FIG. 6 illustrates another memory structure 600 formed based on memory structure 200, according to some embodiments. Different from memory structures 400 and 500, memory structure 600 (e.g., multiple-channel structure) can include semiconductor channels each including more than one semiconductor sub-channels stacked along the z axis. Multiple-channel structure can further increase memory cell density of the 3D memory device. In some embodiments, as shown in FIG. 6, semiconductor channel 601 extends through staircase structure 603 and includes semiconductor sub-channel 601-1 (e.g., formed in the lower staircase structure) and 601-2 (e.g., formed in the upper staircase structure). Semiconductor sub-channels 601-1 and 601-2 can be connected by a connection layer 606. In some embodiments, semiconductor sub-channels (e.g., 601-1 and 601-2) have same or similar functions as semiconductor channels 415 and 501 of FIGs. 4 and 5.

[0107] In an example, supporting pillars 613 can be formed by similar fabrication operations as in FIGs. 1-5. That is, pillar holes can be formed before or after the formation of sub-channel holes that form semiconductor sub-channels 601-2. The filing of the pillar holes can be performed at the same time with or after the filling of sub-channel holes of semiconductor sub-channels 601-2.

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[0108] In contrast to the fabrication operations illustrated in FIGs. 1-4, to form memory structure 600, before the deposition of second dielectric stack (e.g., upper dielectric stack), semiconductor sub-channels 601-1 can be formed in the first dielectric stack (e.g., lower dielectric stack) before the deposition of second dielectric stack (e.g., upper dielectric stack). In the description of FIG. 6, the first dielectric stack and the second dielectric stack (e.g., the same as or similar to first dielectric stack 103 and second dielectric stack 206) can each include a plurality of alternatingly arranged sacrificial material layers and insulating material layers. In some embodiments, semiconductor sub-channels 601-2 are formed by, e.g., forming first sub-channel holes of semiconductor sub-channels 601-2 in first dielectric stack, respectively depositing charge trapping film 602, semiconductor channel film 604, and dielectric core 605 in the first sub-channel holes. The formation of the first sub-channel holes and the deposition of the films in the first sub-channel holes can be referred to the operations that form first sub-channel holes 205 and charge trapping film 502, semiconductor channel film 503, and dielectric core 504, respectively. Optionally, a recess etch (e.g., dry etch and/or wet etch) and/or a planarization process (e.g., CMP) can be performed to remove excessive dielectric material over the top surface of first dielectric stack.

[0109] Memory structure 600 can include a joint insulating layer 618 between semiconductor sub-channels 601-1 and 601-2 and a plurality of connection layers 606 in joint insulating layer 618. Connection layers 606 can function as drain regions and can connect semiconductor sub-channels 601-1 and 601-2. Joint insulating layer 618 can insulate connection layers 606 from one another. can be formed over the first dielectric stack before the formation of the first sub-channel holes. In some embodiments, joint insulating layer 618 includes silicon oxide and connection layers 606 include doped silicon. The formation of joint insulating layer 618 and connection layers 606 can be referred to the formation of insulating cap layer 410 and drain regions 419. The deposition can include any suitable deposition methods, such as CVD and/or area selective deposition (ASD). Optionally, an ion implantation process is employed to adjust the doping level of the recess region. The conductivity type of connection layer 606 can be the same as the conductivity type of semiconductor sub-channels 601-1. Optionally, a recess etch (e.g., dry etch and/or wet etch) and/or a planarization process (e.g., CMP) can be performed to remove excessive doped

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semiconductor material over the top surface of first dielectric stack. Optionally, an additional dielectric material can be deposited over the top surface of second dielectric stack to cover semiconductor sub-channels 601-1. The additional dielectric material can include one or more of the dielectric materials that form first dielectric stack 103.

[0110] Further, the second dielectric stack can be formed over the first dielectric stack, and staircase structure 603 can be formed by repeatedly etching/patterning the dielectric stack formed by the first dielectric stack and the second dielectric stack. A dielectric filling material can be deposited over staircase structure 603 to filling the space formed by the removal of portions of dielectric pairs and dielectric filling structure 611 (e.g., similar to dielectric filling structure 311) can be formed.

[0111] Semiconductor sub-channels 601-2 can be formed by any suitable methods after staircase structure 603 is formed. In some embodiments, second sub-channel holes of semiconductor sub-channels 601-2 are formed over semiconductor sub-channels 601-1. The bottom of the second sub-channel hole of semiconductor sub-channel 601-2 can expose connection layers 606. Further, a sequence of layers can be deposited into the second sub-channel holes to form second semiconductor sub-channels 601-2. The formation of the second sub-channel holes of semiconductor sub-channels 601-2, charge trapping film 607, semiconductor channel film 608, dielectric core 609, drain regions 612, and insulating cap layer 610 can be similar to the second sub-channel holes of semiconductor channels 415, charge trapping film 416, semiconductor channel film 417, dielectric core 418, drain regions 419, and insulating cap layer 410.

[0112] Supporting pillars 613 can be formed by the same fabrication operations that form semiconductor sub-channels 601-2 or after the formation of semiconductor sub-channels 601-2. The formation of dummy charge trapping film 614, dummy semiconductor channel film 615, dummy dielectric core 616, and dummy drain region 617 can be similar to or the same as the formation of dummy charge trapping film 411, dummy semiconductor channel film 412, dummy dielectric core 413, and dummy drain region 414.

[0113] FIGs. 7-12 illustrate an exemplary process to form a two-stack staircase structure from two dielectric stacks employing one staircase-forming patterning process, according to some embodiments. For viewing simplicity, FIGs. 7-12 depict the fabrication process to form

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the staircase structure in the core region shown in FIGs. 1-6. Same or similar operations performed in the method illustrated by FIGs. 7-12 can be referred to the operations described in FIGs. 1-6. For illustrative purposes, the formation of a double-channel structure (e.g., similar to memory structure 600 of FIG. 6) is described.

[0114] FIG. 7 illustrates memory structure 700 similar to core region 110 of FIG. 1, according to some embodiments. Memory structure 700 can include a first dielectric stack 703 over gate dielectric layer 704, which is further over substrate 707. Substrate 707 can include a first doped region 706, and a second doped region 705. First dielectric stack 703 can include a plurality of dielectric pairs, each including a sacrificial material layer 701 and an insulating material layer 702. Respectively, substrate 707, first doped region 706, second doped region 705, gate dielectric layer 704, and first dielectric stack 703 can be the same as or similar to substrate 107, first doped region 106, second doped region 105, dielectric layer 104, and first dielectric stack 103. Description of structure and formation methods of memory structure 700 can be referred to the description of memory structure 100.

[0115] FIG. 8 illustrates memory structure 800 formed based on memory structure 700, according to some embodiments. Memory structure 800 can be formed from memory structure 700 by forming a plurality of channel epitaxial regions 806 extending from first dielectric stack 703 to second doped region 705, a joint insulating material layer 810 over first dielectric stack 703, a plurality of first sub-channel holes 801 extending from the top surface of joint insulating material layer 810 into channel epitaxial regions 806, and filling first sub-channel holes 801 with a series of channel-forming layers 802 (charge trapping film, semiconductor channel film, and dielectric core) to form semiconductor sub-channels 805 . A plurality of connection layers 804 can be formed in joint insulating material layer 810 and can each be over a semiconductor sub-channel 805. In some embodiments, a recess etch and/or a suitable planarization process (CMP) can be performed to remove any excessive material of channel-forming layers 802 from the top surface of memory structure 800.

[0116] As an example, a joint insulating material layer can first be formed over first dielectric stack 703. A plurality of first sub-channel holes 801 can then be formed in first dielectric stack 703 to extend from the top surface of the joint insulating material into channel epitaxial regions 806. Joint insulating material layer 810 can be formed from the

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joint insulating material layer and first dielectric stack 803 can be formed from first dielectric stack 703. A series of channel-forming layers 802 can then be deposited to fill in first sub-channel holes 801. A suitable recess etch (e.g., dry etch and/or wet etch) can be performed to remove a top portion of channel-forming layers 802 in each first sub-channel hole 801 and a doped semiconductor material can be deposited into first sub-channel holes 801 to form connection layers 804 in joint insulating material layer 810. Optionally, additional insulating material can be deposited over connection layers 804 to insulate connection layers 804 from neighboring structures that are formed in subsequent operations. Details of the formation of semiconductor sub-channels 805 and connection layers 804 can be referred to the description of semiconductor channels 501 and drain regions 505.

[0117] FIG. 9 illustrates an exemplary memory structure 900 formed based on memory structure 800, according to some embodiments. Memory structure 900 can be formed by forming second dielectric stack 906 over first dielectric stack 803. Similar to first dielectric stack 703 and 103, second dielectric stack 906 can include a plurality of dielectric pairs arranged over first dielectric stack 703 (e.g., joint insulating layer 810) along the z axis. Each dielectric pair can include a sacrificial material layer 901 and an insulating material layer 902. First dielectric stack 803 and second dielectric stack 906 can form dielectric stack 903 (e.g., two-stack dielectric stack). In some embodiments, an insulating cap material layer 910 (e.g., similar to the joint insulating material layer of FIG. 8 and the insulating cap material layer of FIG. 3) is formed over second dielectric stack 906. In some embodiments, second dielectric stack 906 is similar to first dielectric stack 703. Description of structure and formation methods of second dielectric stack 906 and insulating cap material layer 910 can be referred to the description of first dielectric stack 103 and the insulating cap material layer of FIG. 3.

[0118] FIG. 10 illustrates an exemplary memory structure 1000 formed based on memory structure 900, according to some embodiments. Memory structure 1000 can be formed by forming a plurality of second semiconductor sub-channels 1007 that alight with and adjoin semiconductor sub-channels 805 to form semiconductor channels 1001 through dielectric stack 1003, and a plurality of drain regions 1005 in insulating cap material layer 1010. Dielectric stack 1003 can be formed from dielectric stack 903 after the formation of second

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semiconductor sub-channels 1007, and insulating cap material layer 1010 can be formed from insulating cap material layer 910 after the formation of second sub-channel holes 1002. In some embodiments, second semiconductor sub-channels 1007 are formed by depositing a series of channel-forming layers 1004 (charge trapping film, semiconductor channel film, and dielectric core) into second sub-channel holes 1002. In some embodiments, drain regions 1005 are formed by forming a recess region in insulating cap material layer 1010 and at the top portions of second sub-channel holes 1002, and depositing a doped semiconductor material (e.g., doped polysilicon) in the recess region. The fabrication processes of second semiconductor sub-channels 1007, drain regions 1005, and insulating cap material layer 1010 can be referred to the fabrication processes of semiconductor sub-channels 805, joint insulating material layer 810, and connection layers 804.

[0119] FIG. 11 illustrates memory structure 1100 formed based on memory structure 1000, according to some embodiments. Memory structure 1100 can be formed by performing a staircase-forming patterning process on dielectric stack 1003 to form staircase structure 1104. By performing the staircase-forming patterning process, first dielectric stack 803 can be etched to form first staircase structure 1103, and second dielectric stack 1006 can be etched to form second staircase structure 1106. First staircase structure 1103 and second staircase structure 1106 can stack along the z axis to form staircase structure 1104. In some embodiments, joint insulating material layer 810 and insulating cap material layer 1010 can be etched to form joint insulating layer 1111 and insulating cap layer1110, respectively. The staircase-forming patterning process can include forming a photoresist layer over dielectric stack 1003. In some embodiments, the photoresist layer can be patterned (e.g., using a photolithography process) to cover the core region. The photoresist layer can have a sufficient thickness along the z axis so that it can be trimmed and used as an etching mask for forming staircases from dielectric stack 1003. During the staircase-forming patterning process, the photoresist layer is repeatedly trimmed (e.g., etched by a suitable dry etch and/wet etch) along various directions (e.g., the x axis, the y axis, and the z axis) so dielectric pairs of dielectric stack 1003 can be repeatedly exposed. Same or different etchant (e.g., wet etchant and/or dry etchant) can be used to etch the sacrificial material layer (e.g., 701 or 901) and the insulating material layer (e.g., 702 or 902). In some embodiments, the trimming time

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of the photoresist layer is controlled so that the trimming/etching rate of the photoresist layer can be controlled. Accordingly, the dimension of the staircase along the x direction can be controlled. In some embodiments, the sacrificial material layers can be etched to form the sacrificial layers, and the insulating material layers can be etched to form the insulating layers. One sacrificial layer can be pairing with one insulating layer. Depending on different memory device structures, the sacrificial layer can be on top of the pairing insulating layer, or vice versa.

[0120] For illustrative purposes, as shown in FIG. 11, memory structure 1100 is divided into core array region 1120, first staircase region 1121, and second staircase region 1122. First staircase region 1121 and second staircase region 1122 can each surround memory structure 1100 along the x-y plane. First staircase region 1121 can represent the region where staircases of first dielectric stack 703 are formed, and second staircase region 1122 can represent the region where staircases of second dielectric stack 906 are formed. In some embodiments, the photoresist layer (e.g., etch mask) can be trimmed to expose dielectric stack 1003 along, e.g., the x direction - from first staircase region 1121 towards core array region 1120, and staircases of staircase structure 1104 can be formed along the same direction the photoresist layer is trimmed. In some embodiments, staircases of first staircase structure 1103 (e.g., lower/bottom staircase structure) are formed in first staircase region 1121, and staircases of second staircase structure 1106 (e.g., upper/top staircase structure) are formed in second staircase region 1122. In some embodiments, the trimming of the photoresist layer can stop when the staircases in first staircase region 1121 and second staircase region 1122 are formed. The trimmed photoresist layer can cover the top surface of core array region 1120 so that semiconductor channels 1001 can remain intact. Photoresist layer can then be removed, and memory structure 1100 can be formed.

[0121] In various embodiments, semiconductor channels 1001 can be formed before or after the formation of staircase structure 1104. That is, the second semiconductor sub-channels (e.g., formed in second dielectric stack 1006) can also be formed after staircase structure 1104 is formed. The different orders to form semiconductor channels 1001 and staircase structure 1104 should still be within the scope of the present disclosure.

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[0122] FIG. 12 illustrates memory structure 1200 formed based on memory structure 1100, according to some embodiments. Memory structure 1200 can be formed by forming dielectric filling structure 1201 to fill in the space formed by the removal of portions of dielectric stack 1003. Dielectric filling structure 1201 can be retro-stepped (not shown in FIG. 12). In some embodiments, dielectric filling structure 1201 is formed by depositing a suitable dielectric filling structure to fill in the space and performing a suitable planarization process (e.g., CMP and/or recess etch) to remove any excessive dielectric filling structure over the top surface of memory structure. In some embodiments, dielectric filling structure 1201 is similar to or as same as dielectric filling structure 311. Description of structure and formation methods of dielectric filling structure 1201 can be referred to the description of dielectric filling structure 311.

[0123] Further, the sacrificial layers can be removed by a suitable isotropic etching process, and space formed by the removal of the sacrificial layers can be filled with a suitable metal, e.g., one or more of copper, tungsten, and aluminum. Optionally, a recess etch can be performed to remove excessive metal over staircase structure 1104. The deposited metal can then form the word lines of the 3D memory device. In some embodiments, each word line is insulated from adjacent word lines by the insulating layers in between.

[0124] Method illustrated by FIGs. 7-12 can be employed to form the staircase structure in FIGs. 1-6 and semiconductor channels embedded in the staircase structure. By using the disclosed method, one staircase-forming pattern can be used to form the staircase structure that contains at least two sub-staircase structures stacked along the z axis. No staircase-forming pattern is needed to separately form the sub-staircase structures. The fabrication process of the 3D memory device can be simplified.

[0125] Further, supporting pillars through the multiple-stack staircase structure can be formed by one etching process that forms pillar holes through the multiple-stack staircase structure and subsequent filling process. In some embodiments, the pillar holes are formed at the same time or by same fabrication operations as a part of the semiconductor channels. In some embodiments, the pillar holes are formed after the formation of the semiconductor channels. Compared to existing technology, the number of operations to form supporting pillars is reduced. The fabrication of the 3D memory device is thus simpler and less costly.

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[0126] FIG. 13 is an illustration of an exemplary method 1300 for forming three-dimensional memory structure, according to some embodiments. For explanation purposes, the operations shown in method 1300 are described in the context of FIGs. 1-12. In various embodiments of the present disclosure, the operations of method 1300 can be performed in a different order and/or vary.

[0127] At operation 1301, a first dielectric stack can be formed over a substrate. In some embodiments, the substrate can include any suitable materials such as silicon. In some embodiments, the first dielectric stack includes a plurality of alternatingly arranged sacrificial material layers and insulating materials. The sacrificial material layers and the insulating material layers can include different dielectric materials. In some embodiments, a gate dielectric layer is formed between the first dielectric stack and the substrate. Details of the first dielectric stack, the gate dielectric layer, and the substrate can be referred to the description of FIG. 1.

[0128] At operation 1302, a plurality of first sub-channel holes can be formed in the first dielectric stack and the first sub-channel holes can be filled with suitable materials. In some embodiments, the first sub-channel holes can be formed with suitable patterning and etching processes so that the bottoms of the first sub-channel holes contact or expose the substrate. The first sub-channel holes can be through the first dielectric stack. Optionally, a channel epitaxial region can be formed at the bottom of each first sub-channel hole. A sacrificial filling structure can be formed in the first sub-channel holes by depositing a sacrificial filling material, as e.g., place holders, to provide support for the formation of subsequent second dielectric stack over the first dielectric stack. A planarization process can be performed to remove any excessive sacrificial filling material over the first dielectric stack.

[0129] When the 3D memory device is a double-channel memory device, a series of channel-forming layers for forming a semiconductor channel can be sequentially deposited into the plurality of first sub-channel holes so that first semiconductor sub-channels can be formed. The series of layers can include a charge trapping film, a semiconductor channel film, and a dielectric core, being deposited from the sidewall to the center of the channel hole. A connection layer (e.g., a doped semiconductor layer) can be formed over each semiconductor sub-channel. Details of the first sub-channel holes, the sacrificial filling

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structure, the semiconductor sub-channels, and the channel epitaxial region can be referred to the description of FIGs. 2 and 6.

[0130] At operation 1303, a second dielectric stack can be formed over the first dielectric stack. Similar to the first dielectric stack, the second dielectric stack can include a plurality of alternatingly arranged sacrificial material layers and insulating materials. Details of the second dielectric stack can be referred to the description of FIG. 2.

[0131] At operation 1304, a multiple-stack staircase structure can be formed. The multiple-stack (e.g., two-stack) staircase structure can include a first staircase structure (e.g., formed based on the first dielectric stack) and a second staircase structure (e.g., formed based on the second dielectric stack). The multiple-stack staircase structure can be formed by a staircase-forming patterning process so that dielectric pairs of the first dielectric stack and the second dielectric stack can be etched to form staircases. A dielectric filling structure can be formed to fill up the space formed by the removal of portions of the dielectric pairs. Details of the process to form the multiple-stack staircase structure can be referred to the description of FIGs. 7-12.

[0132] At operation 1305, a plurality of second sub-channel holes can be formed in the second staircase structure. The second sub-channel holes can adjoin the first sub-channel holes along a direction perpendicular to the top surface of the substrate. In some embodiments, a second sub-channel hole and the adjoined first sub-channel hole form a channel hole through the multiple-stack staircase structure. When the 3D memory device is a double-channel memory device, the second sub-channel holes can also be referred to as sub-channel holes of the second staircase structure. The formation of second sub-channel holes can be similar to the formation of first sub-channel holes described in operation 1302.

[0133] At operation 1306, a plurality of pillar holes can be formed in the multiple-stack staircase structure. The pillar holes can be formed by any suitable patterning/etching process. In some embodiments, the pillar holes can be through the multiple-stack staircase structure and can contact the substrate. Details of the process to form the pillar holes can be referred to the description of FIGs. 3 and 5.

[0134] At operation 1307, a plurality of supporting pillars and semiconductor channels can be formed in the multiple-stack staircase structure. The semiconductor channels can be

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formed by removing the sacrificial filling structures in the first sub-channel holes and filling the first sub-channel holes and the adjoined second sub-channel holes with a series of layers (e.g., a charge trapping film, a semiconductor channel film, and a dielectric core). When the 3D memory device is a double-channel memory device, the series of layers can be deposited in the second sub-channel holes (e.g., sub-channel holes) to form semiconductor sub-channels in the second staircase structure.

[0135] The supporting pillars can be formed by filling the same series of layers of the semiconductor channels in the pillar holes. The filling of the supporting pillars can be performed at the same time and/or through the same fabrication processes when the semiconductor channels (or semiconductor sub-channels of the second/upper staircase structure) are being formed. The supporting pillars can also be formed using any other suitable pillar-forming material such as a dielectric material with or without other support materials (such like metal). In some embodiments, the dielectric material is deposited into a pillar hole to form an insulating liner/spacer layer over the sidewall of the pillar hole, and the metal material is deposited to fill up the pillar hole. The insulating liner/spacer layer can insulate the metal material from the rest of memory structure 1200, and the metal material can provide further support to the supporting pillar. In some embodiments, the dielectric material includes silicon oxide, and the metal material includes copper. The insulating liner/spacer layer can include a single layer or a multiple layer. In an example, the insulating liner/spacer layer can include a single layer of silicon oxide or multiple layers of silicon oxide/silicon oxynitride/silicon oxide. The silicon oxide can be pure or doped with suitable impurities such as tungsten, copper, cobalt, nickel, and/or aluminum. The dielectric material can be deposited using any suitable process such as ALD, CVD, and/or spin-on-coating. The metal material can be deposited by, e.g., sputtering, spin-on-coating, and/or CVD.

[0136] In various embodiments, the order of operations 1304-1306 can vary. For example, the second sub-channel holes can be formed before or after the formation of multiple-stack staircase structure, and the pillar holes can be formed before or after the formation of second sub-channel holes. In some embodiments, the pillar holes can be formed at the same time with the second sub-channel holes by a same etching/patterning process. The filling of pillar holes can also be at the same time as or a different time than the filling of

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the second sub-channel holes. The specific orders of operations can be dependent on different fabrication requirements and should not be limited by the embodiments of the present disclosure. Details of the formation of supporting pillars and semiconductor channels can be referred to the description of FIGs. 4-6.

[0137] The foregoing description of the specific embodiments will so fully reveal the general nature of the present disclosure that others can, by applying knowledge within the skill of the art, readily modify and/or adapt for various applications such specific embodiments, without undue experimentation, without departing from the general concept of the present disclosure. Therefore, such adaptations and modifications are intended to be within the meaning and range of equivalents of the disclosed embodiments, based on the teaching and guidance presented herein. It is to be understood that the phraseology or terminology herein is for the purpose of description and not of limitation, such that the terminology or phraseology of the present specification is to be interpreted by the skilled artisan in light of the teachings and guidance.

[0138] Embodiments of the present disclosure have been described above with the aid of functional building blocks illustrating the implementation of specified functions and relationships thereof. The boundaries of these functional building blocks have been arbitrarily defined herein for the convenience of the description. Alternate boundaries can be defined so long as the specified functions and relationships thereof are appropriately performed.

[0139] The Summary and Abstract sections may set forth one or more but not all exemplary embodiments of the present disclosure as contemplated by the inventor(s), and thus, are not intended to limit the present disclosure and the appended claims in any way.

[0140] The breadth and scope of the present disclosure should not be limited by any of the above-described exemplary embodiments, but should be defined only in accordance with the following claims and their equivalents.

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WHAT IS CLAIMED IS:

1. A memory device comprising:

a substrate;

a multiple-stack staircase structure comprising a plurality of staircase structures stacked over the substrate, wherein each of the plurality of staircase structures comprises a plurality of conductor layers, wherein each of the plurality of conductor layers is located between two insulating layers;

a filling structure surrounding the multiple-stack staircase structure;

a semiconductor channel extending through the multiple-stack staircase structure, wherein the semiconductor channel comprises unaligned sidewall surfaces; and

a supporting pillar extending through at least one of the multiple-stack staircase structure and the filling structure, wherein the supporting pillar comprises aligned sidewall surfaces.

2. The memory device of claim 1, wherein:

the multi-stack staircase structure comprises a first staircase structure over the substrate and a second staircase structure over the first staircase structure; and

the supporting pillar extends from a top surface of the second staircase structure to a bottom surface of the first staircase structure.

3. The memory device of claim 2, wherein:

the supporting pillar and the semiconductor channel comprise same filling layers; and

the supporting pillar and the semiconductor channel is each filled with at least one of a charge trapping film, a semiconductor channel film, and a dielectric core.

4. The memory device of claim 2, wherein:

the supporting pillar and the semiconductor channel are filled with different filling layers; and

the supporting pillar is filled with at least one of an insulating material and a pillar-support material surrounded by the insulating material, and the semiconductor channel is filled with at least one of a charge trapping film, a semiconductor channel film, and a dielectric core.

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5. The memory device of claim 4, wherein the insulating material comprises silicon oxide and the pillar-support material comprises at least one of copper, cobalt, nickel, and aluminum.

6. The memory device of claim 5, further comprising a connection layer in the semiconductor channel between two adjacent staircase structures, wherein the connection layer comprises a doped semiconductor material, and portions of the semiconductor channel separated by the connection layer each forms a semiconductor sub-channel.

7. A method for forming a memory device, comprising:

forming a plurality of dielectric stacks stacked on one another over a substrate to create a multiple-stack staircase structure, wherein each one of the plurality of dielectric stacks comprises a plurality of dielectric pairs arranged along a direction perpendicular to a top surface of the substrate;

forming a filling structure that surrounds the multiple-stack staircase structure;

forming a semiconductor channel extending through the multiple-staircase structure, wherein the semiconductor channel comprises unaligned sidewall surfaces; and

forming a supporting pillar extending through at least one of the multiple-staircase structure and the filling structure, wherein the supporting pillar comprises aligned sidewall surfaces.

8. The method of claim 7, wherein forming the supporting pillar comprises:

forming a photoresist layer over the at least one of the filling structure and the multiple-stack staircase structure;

patterning the photoresist layer to form a patterned photoresist layer with an opening that exposes a portion of the filling structure, wherein a location of the opening corresponds to a location of the supporting pillar;

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using the patterned photoresist layer as an etch mask to etch through at least one of the filling structure and the multiple-stack staircase structure to form a pillar hole, wherein a bottom of the pillar hole contacts the substrate; and

filling the pillar hole with a first material.

9. The method of claim 8, wherein forming the semiconductor channel comprises:

forming a first sub-channel hole in a first dielectric stack of the plurality of dielectric stacks;

filling the first sub-channel hole with a sacrificial filling material to form a sacrificial filling structure;

forming a second dielectric stack over the first dielectric stack;

forming a second sub-channel hole in the second dielectric stack, wherein:

the second sub-channel hole aligns with the sacrificial filling structure along the direction perpendicular to the top surface of the substrate, and

the second sub-channel hole adjoins the first sub-channel hole to form a channel hole through the plurality of dielectric stacks and into the substrate;

removing the sacrificial filling structure in the first sub-channel hole; and

filling the channel hole with a second material.

10. The method of claim 9, wherein:

the first material is same as the second material and are formed by same fabrication operations; and

the same fabrication operations comprises depositing at least one of a charge trapping film, a semiconductor channel film, and a dielectric core into the channel hole and the pillar hole.

11. The method of claim 10, wherein the pillar hole is formed before a formation of the second sub-channel hole.

12. The method of claim 10, wherein the pillar hole is formed after a formation of the first sub-channel hole and a formation of the second sub-channel hole .

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13. The method of claim 9, wherein the first material is different from the second material and is formed by a different deposition operation than the second material.

14. The method of claim 13, wherein the first material comprises at least one of an insulating material and a pillar-support material surrounded by the insulating material; and the second material comprises at least one of a charge trapping film, a semiconductor channel film, and a dielectric core.

15. The method of claim 8, wherein forming the semiconductor channel comprises:

forming a first semiconductor sub-channel in the first dielectric stack;

forming a connection layer over the first semiconductor sub-channel, wherein the connection layer comprises a doped semiconductor material; and

forming a second dielectric stack and a second semiconductor sub-channel in the second dielectric stack, wherein the second semiconductor sub-channel aligns with and adjoins the first semiconductor sub-channel to form a semiconductor channel extending through the plurality of dielectric stacks and into the substrate.

16. The method of claim 15, wherein:

the first material is same as the second material and are formed by same fabrication operations; and

the same fabrication operations comprises depositing at least one of a charge trapping film, a semiconductor channel film, and a dielectric core into the channel hole and the pillar hole.

17. A method for forming a memory device, comprising:

depositing a plurality of dielectric stacks over one another over a substrate to form a multiple-dielectric-stack structure, wherein each one of the plurality of dielectric stacks comprises a plurality of first material layer and second material layer alternatingly arranged along a direction perpendicular to a top surface of the substrate;

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forming a first semiconductor sub-channel in a first dielectric stack of the plurality of dielectric stacks;

forming a second dielectric stack of the plurality of dielectric stacks over the first dielectric stack;

forming a second semiconductor sub-channel in the second dielectric stack, wherein the second semiconductor sub-channel aligns with the first semiconductor sub-channel along the direction perpendicular to the top surface of the substrate; and

patterning the multiple-dielectric-stack structure to form a multiple-stack staircase structure.

18. The method of claim 17, wherein patterning the multiple-dielectric-stack structure comprises a single staircase-forming patterning process.

19. The method of claim 18, wherein the staircase-forming patterning process comprises:

forming a photoresist layer over the multiple-dielectric-stack structure;

trimming the photoresist layer along a first direction parallel to a top surface of the substrate; and

etching the multiple-dielectric-stack structure, using the trimmed photoresist layer as an etch mask to form a staircase.

20. The method of claim 19, wherein forming the first semiconductor sub-channel and the second semiconductor sub-channel comprise:

forming a first sub-channel hole in the first dielectric stack and a second sub-channel hole in the second dielectric stack; and

filling the first sub-channel hole and the second sub-channel hole each with channel-forming layers, wherein the channel-forming layers comprise at least one of a charge trapping film, a semiconductor channel film, and a dielectric core.

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ABSTRACT OF THE DISCLOSURE

Methods and structures of a three-dimensional memory device are disclosed. In an example, the memory device includes a substrate and a multiple-stack staircase structure. The multiple-stack staircase structure can include a plurality of staircase structures stacked over the substrate. Each one of the plurality of staircase structures can include a plurality of conductor layers each between two insulating layers. The memory device can also include a filling structure over the multiple-stack staircase structure, a semiconductor channel extending through the multiple-stack staircase structure, and a supporting pillar extending through the multiple-stack staircase structure and the filling structure. The semiconductor channel can include unaligned sidewall surfaces, and the supporting pillar can include aligned sidewall surfaces.

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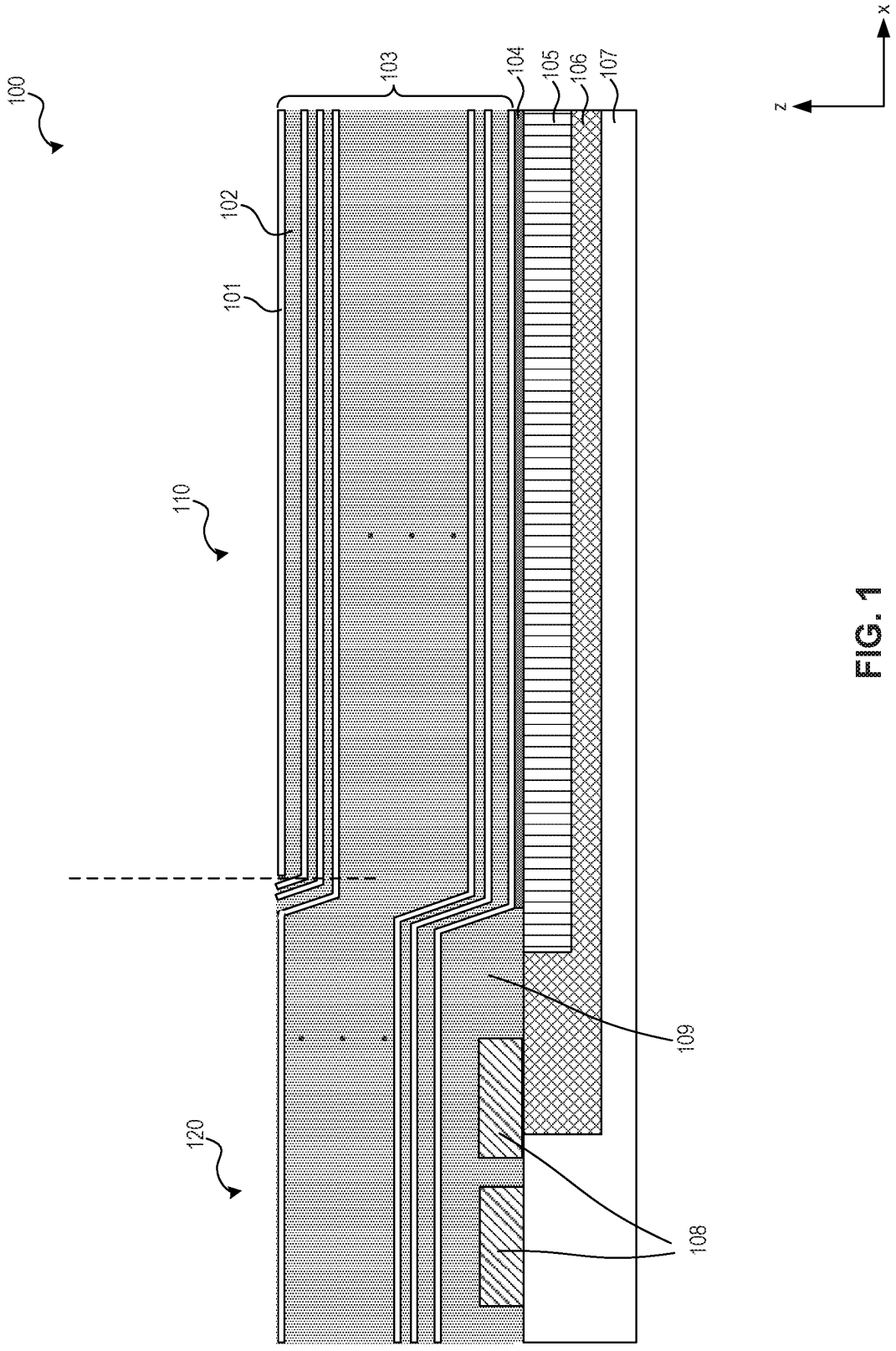


FIG. 1

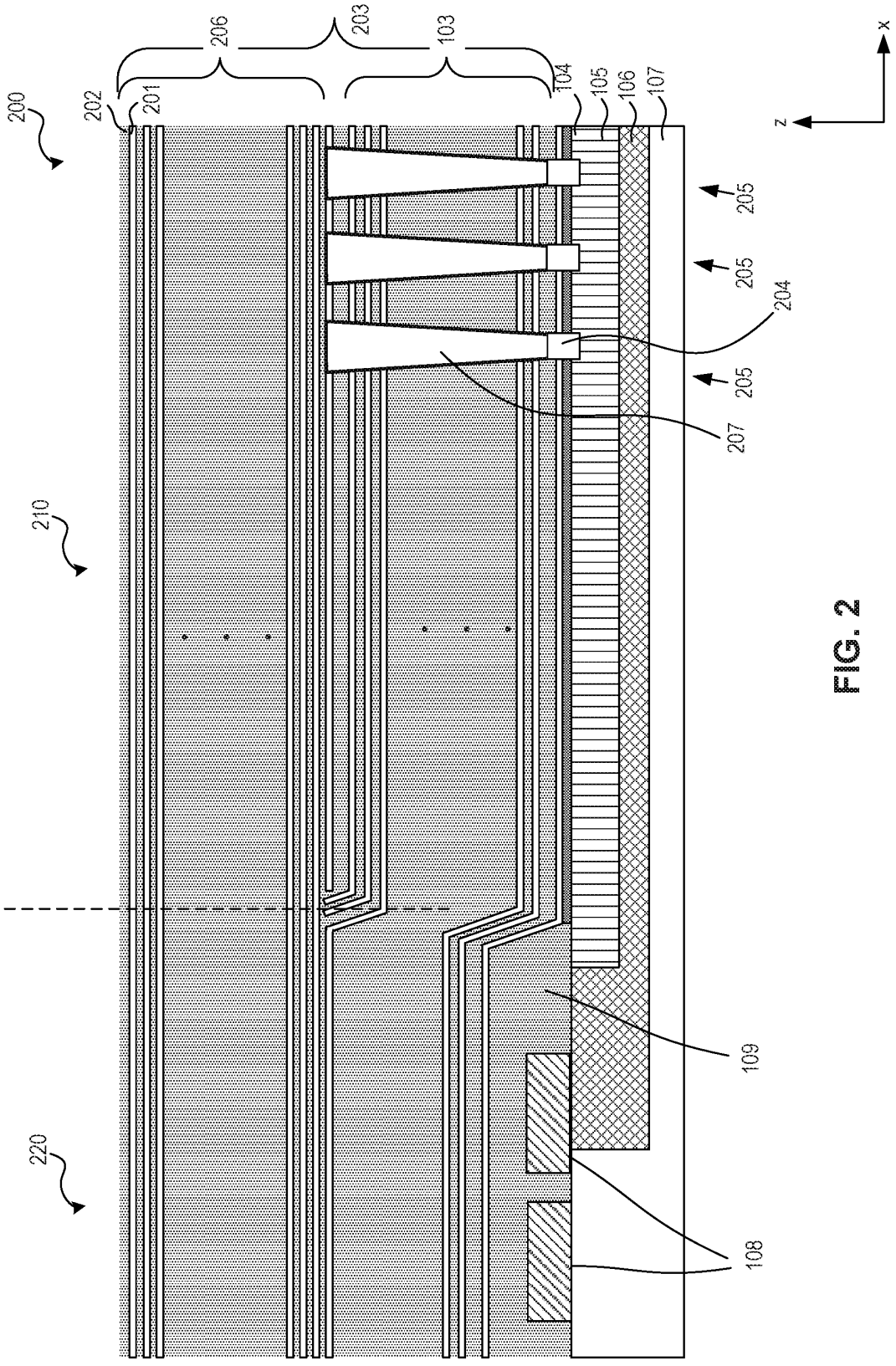

200
202
201
206
203
103
104
105
106
107
x
z
205
205
205
204
207
210
220
109
108

FIG. 2

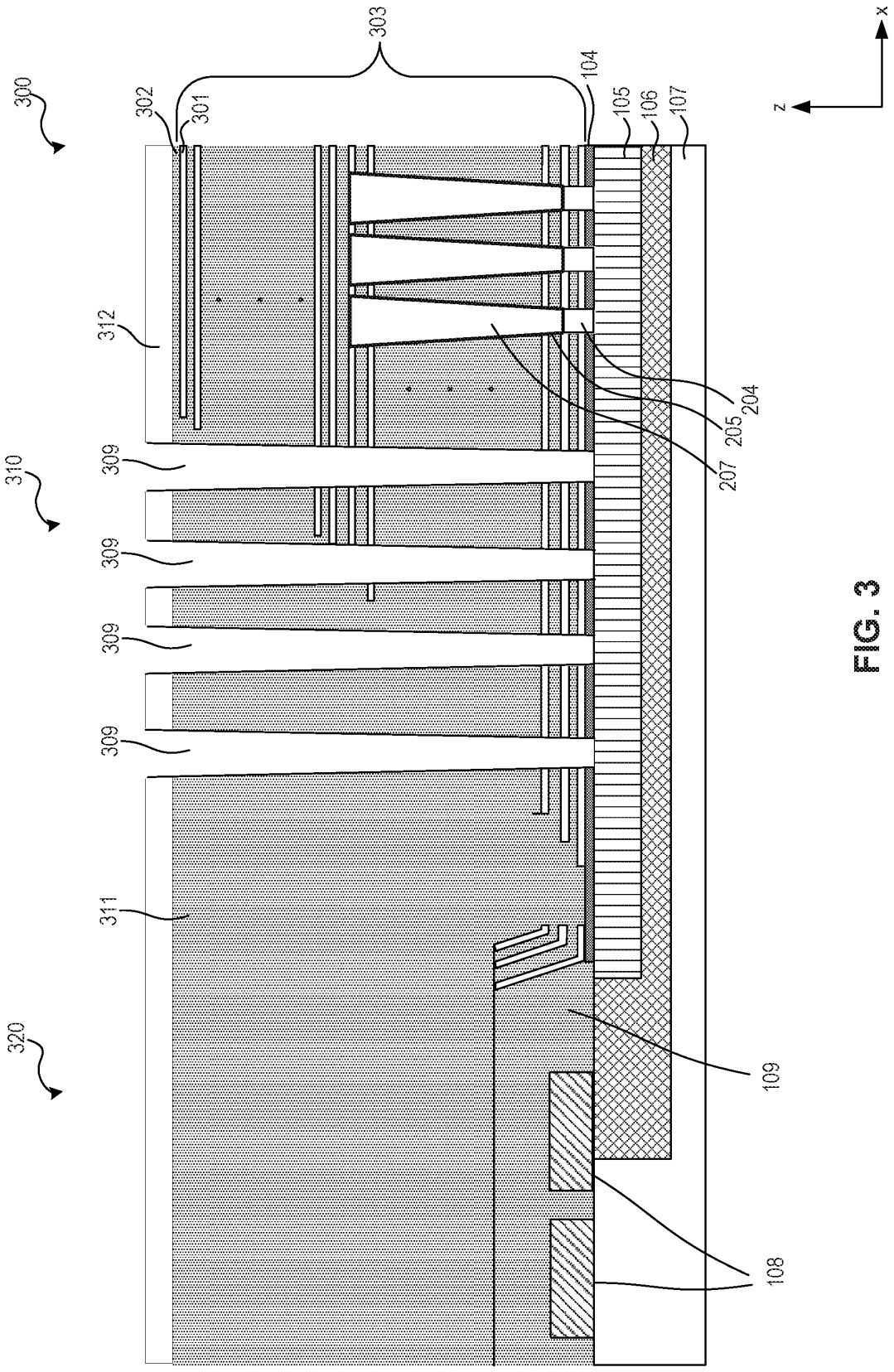

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FIG. 3

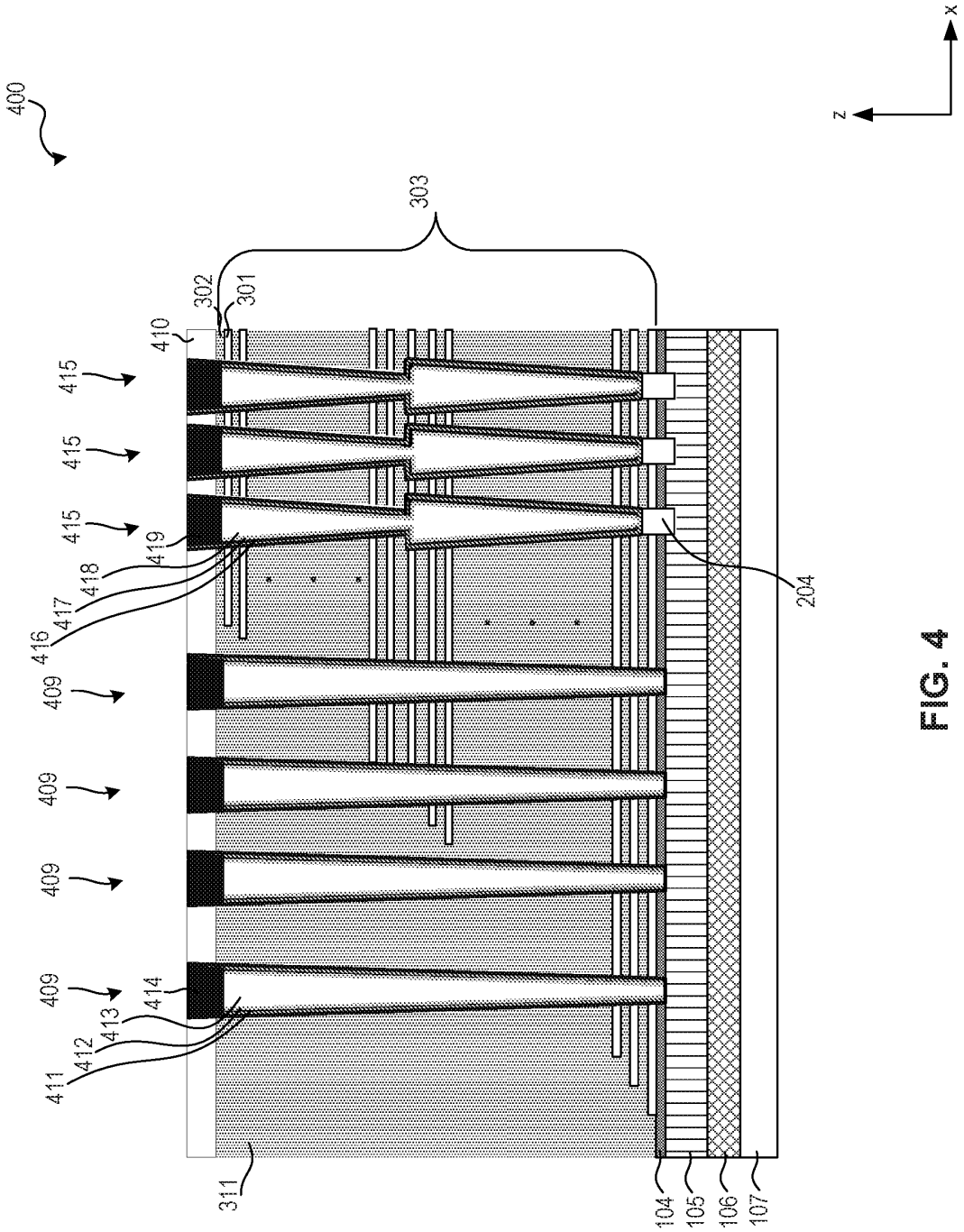

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FIG. 4

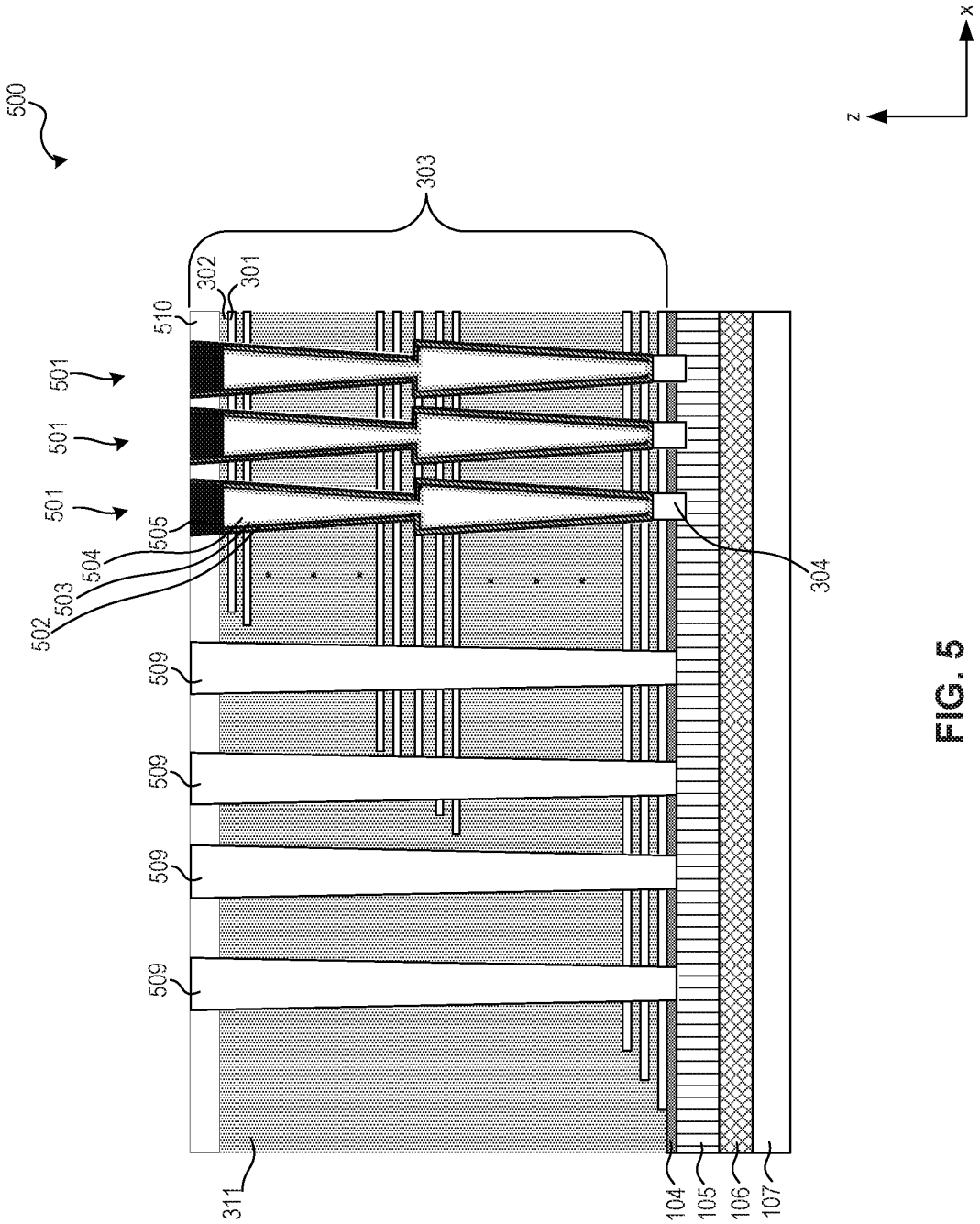

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FIG. 5

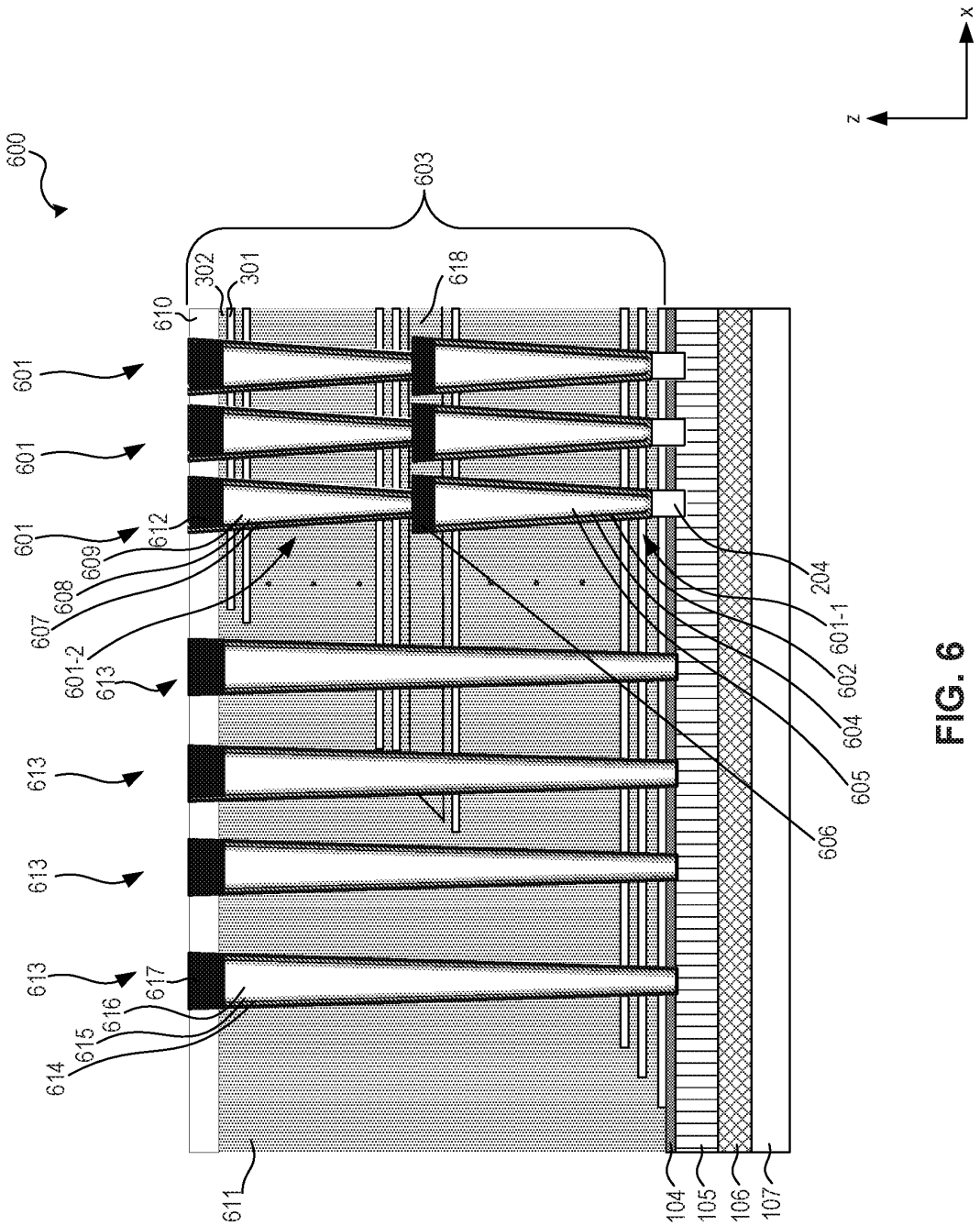

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FIG. 6

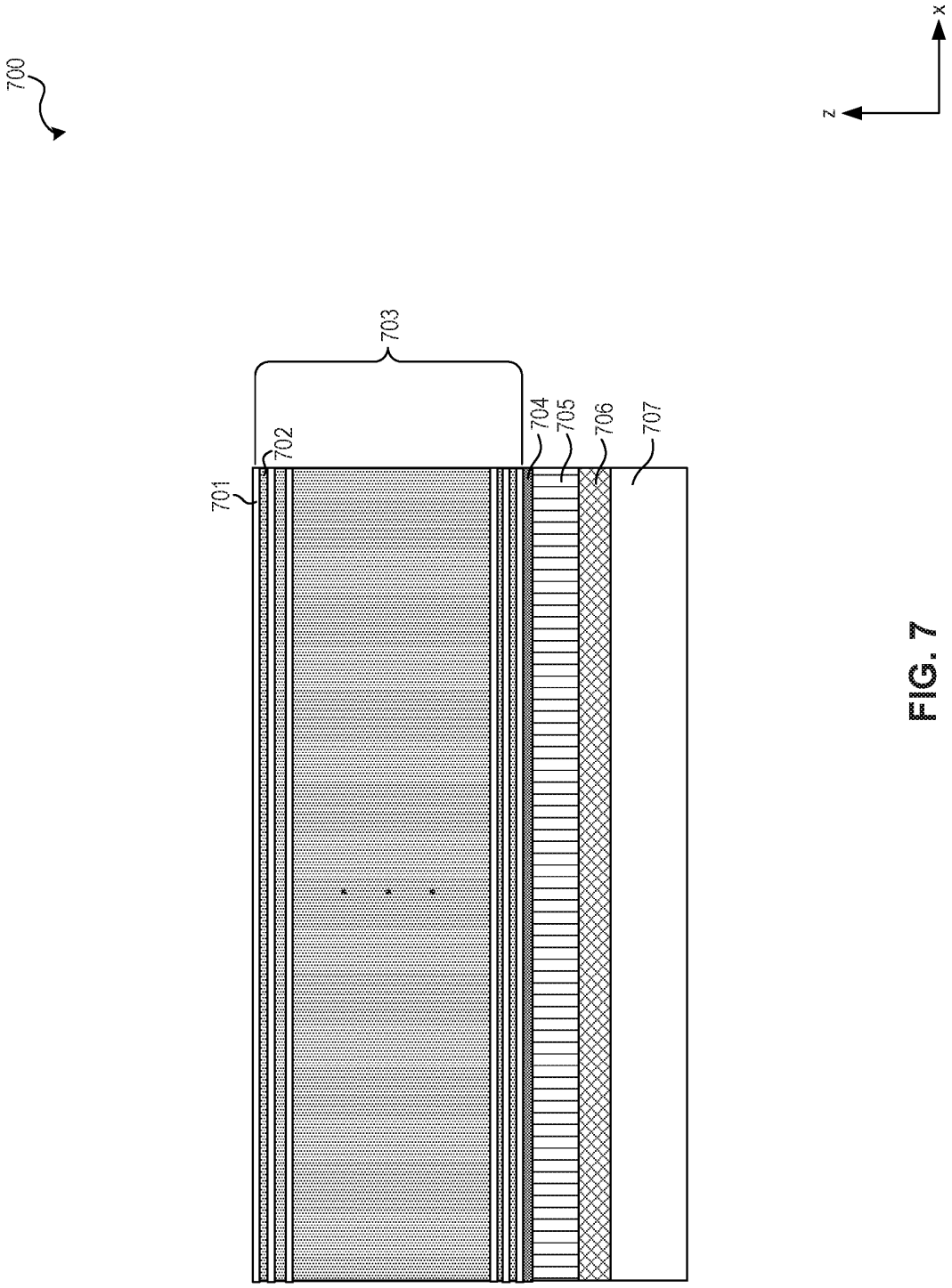


FIG. 7

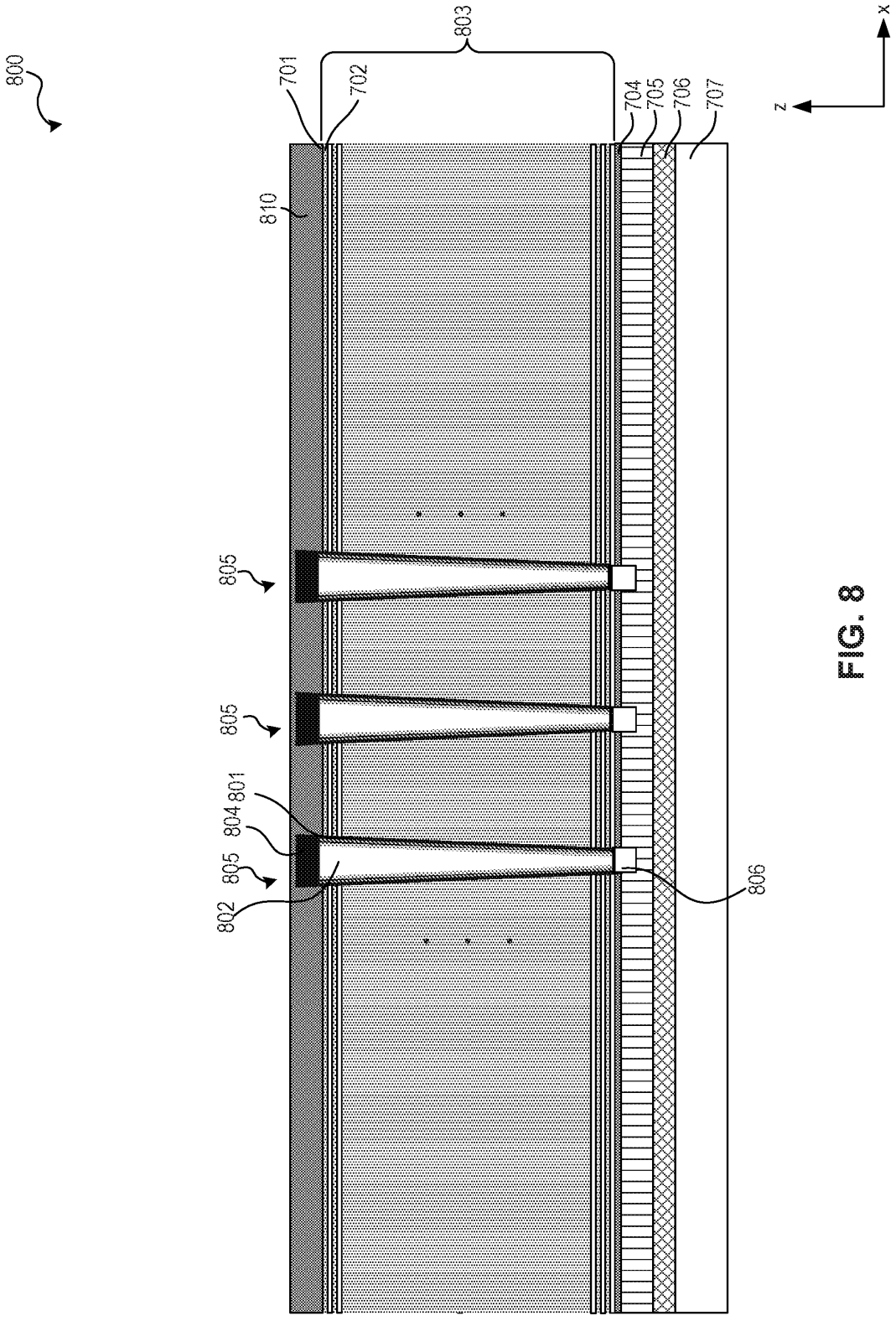

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FIG. 8

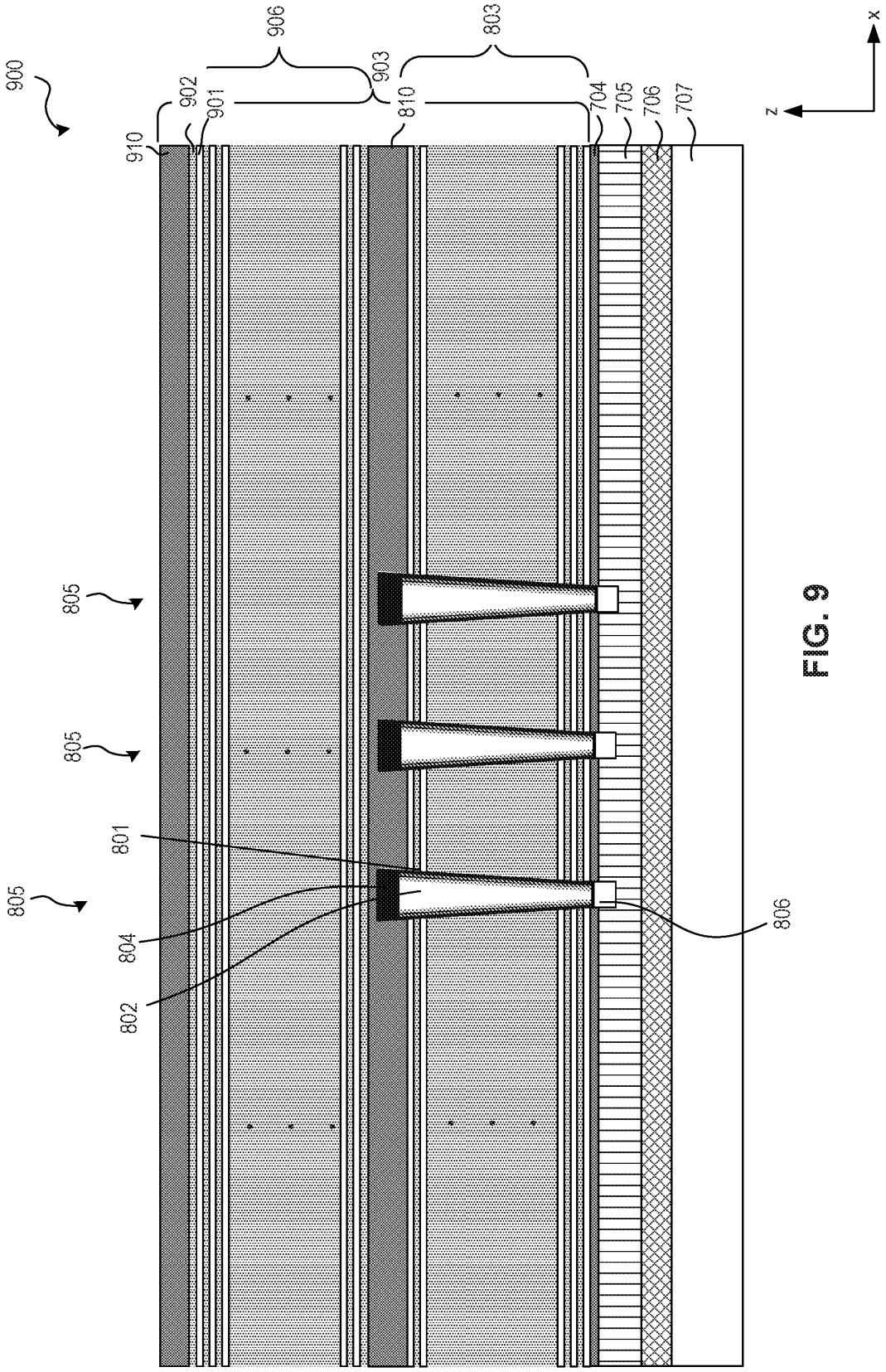

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FIG. 9

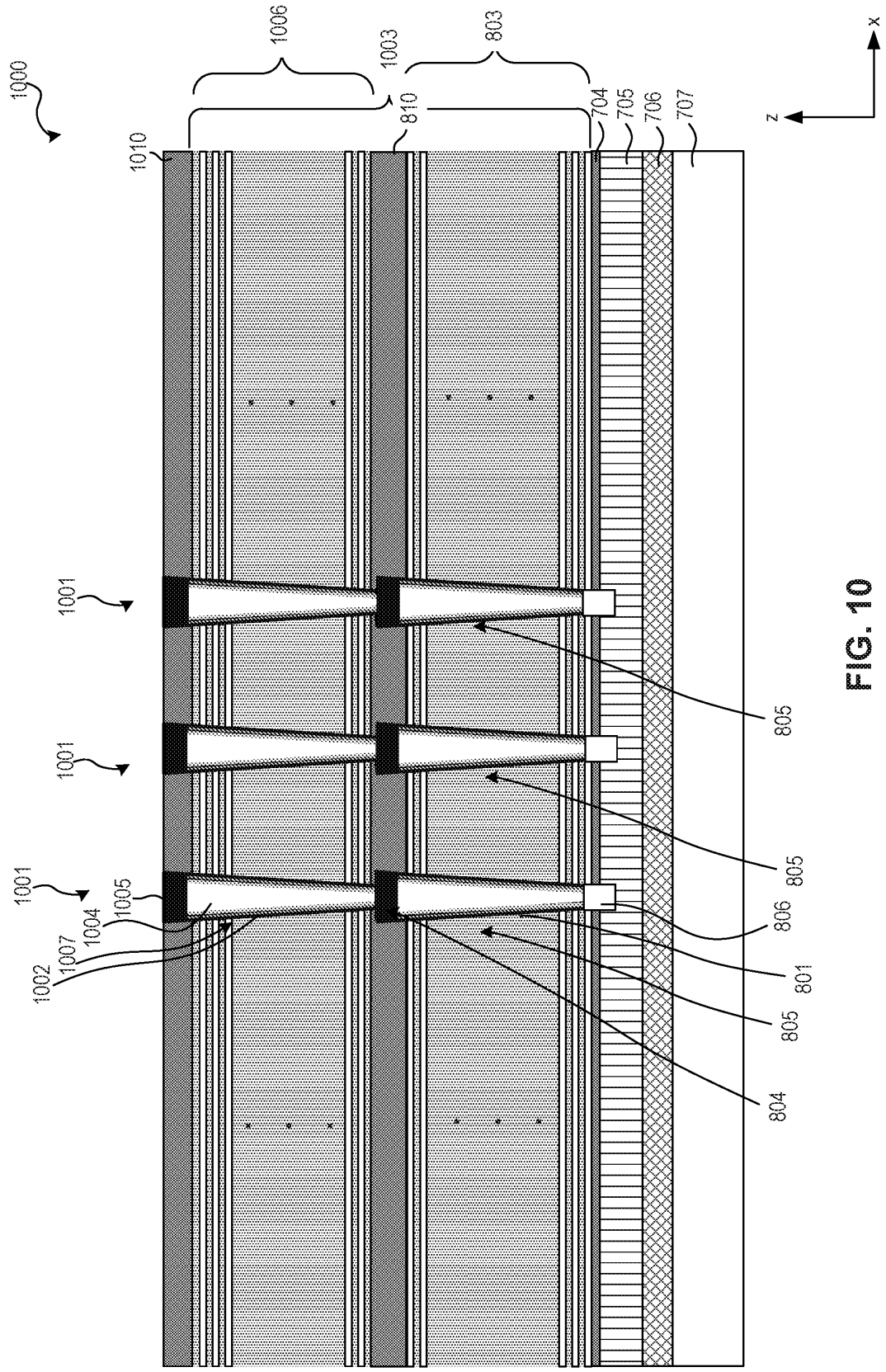

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FIG. 10

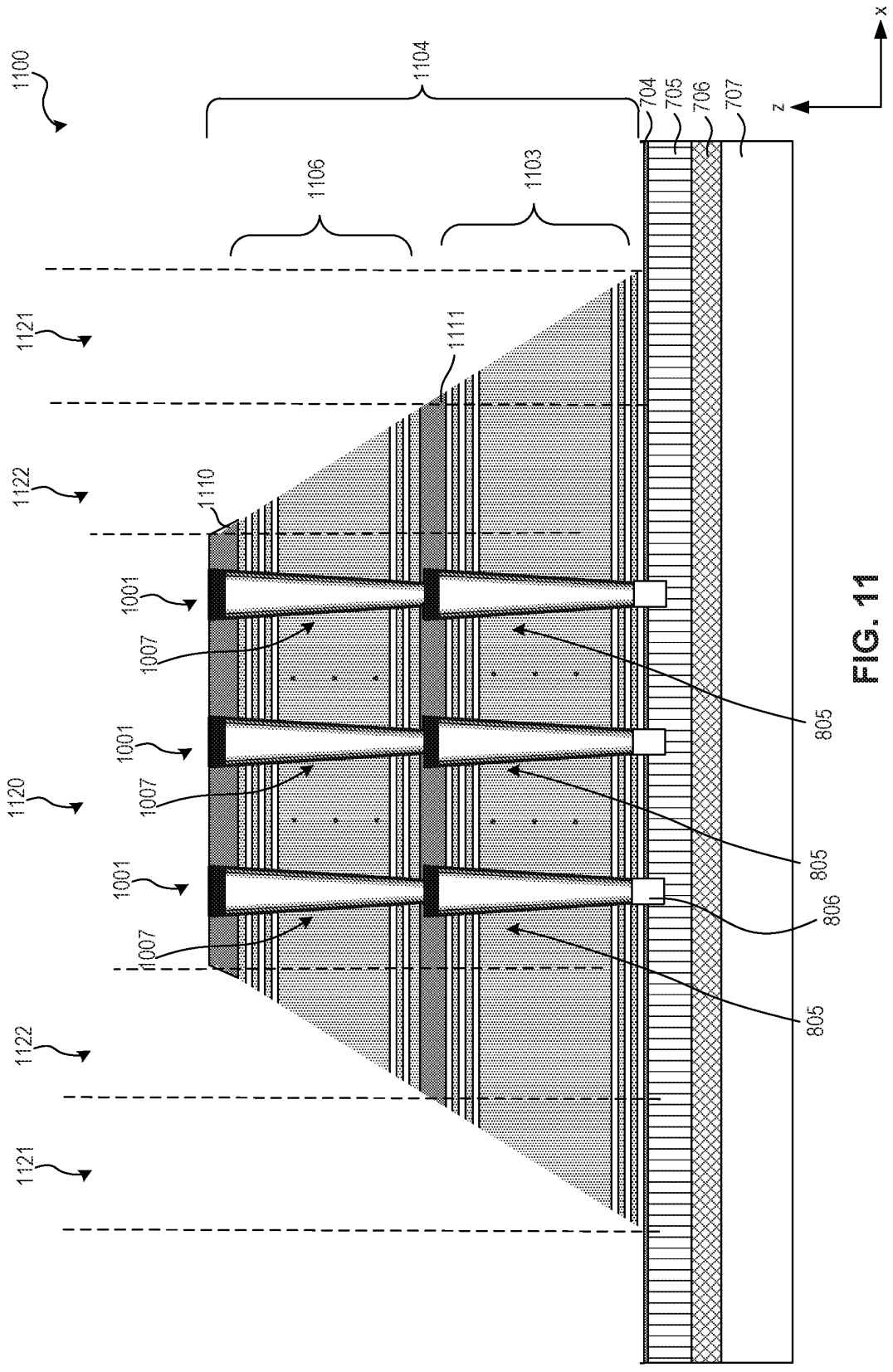

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FIG. 11

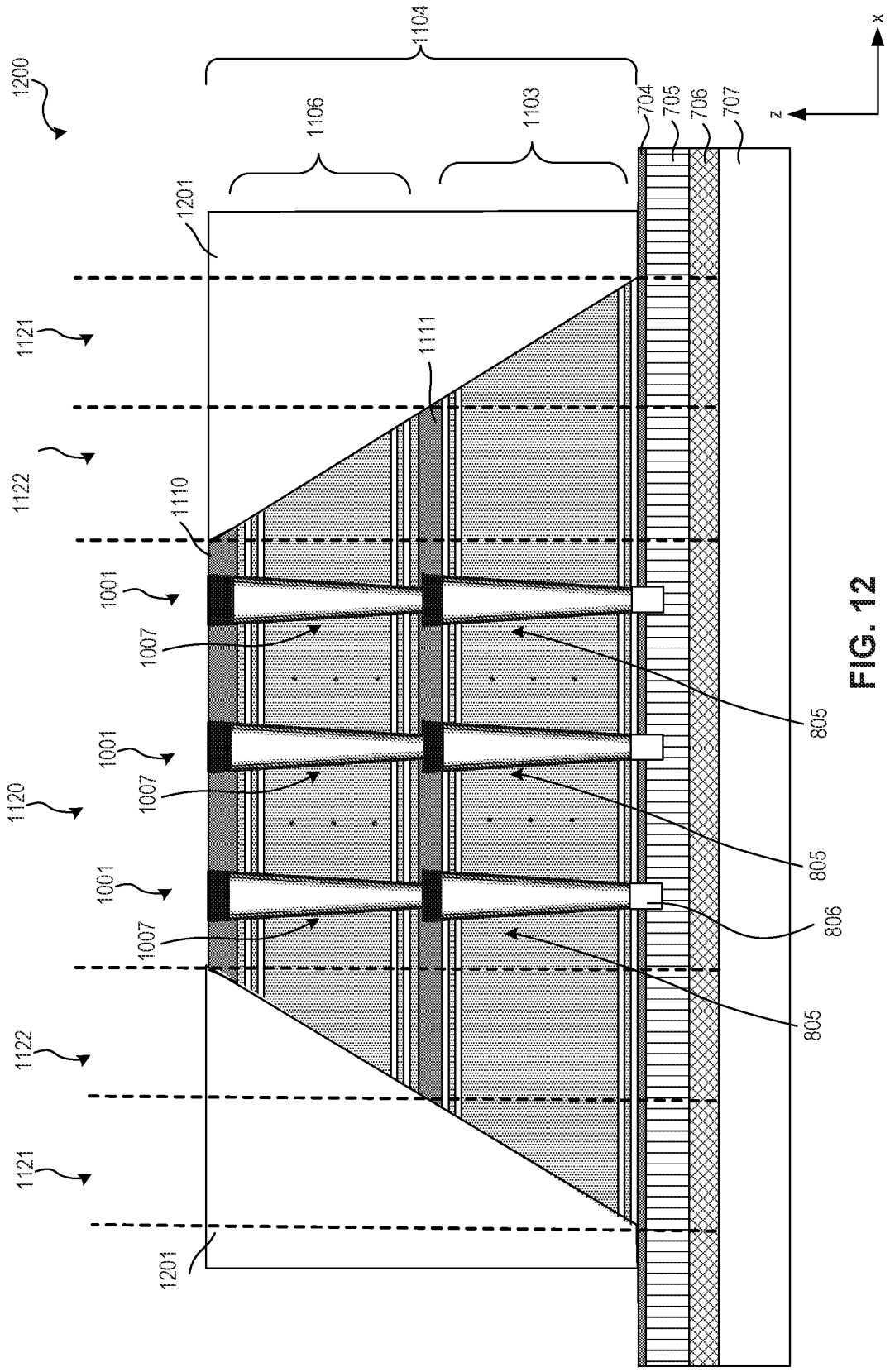

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FIG. 12

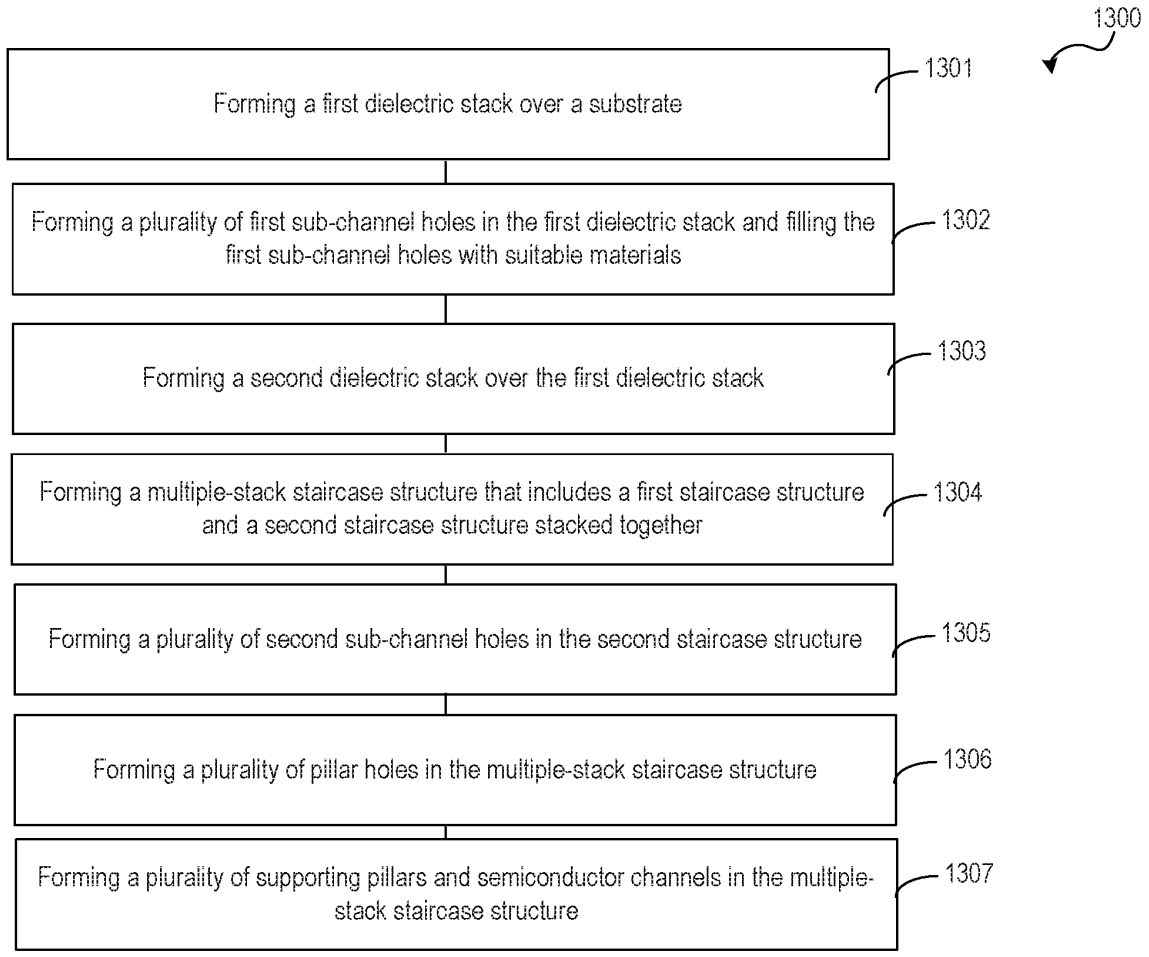


FIG. 13

Micron Ex. 1002, p. 72
Micron v. YMTC
IPR2024-00790

Doc Code: PA..
Document Description: Power of Attorney

PTO/AIA/82A (07-13)
Approved for use through 11/30/2014. OMB 0651-0051
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Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

TRANSMITTAL FOR POWER OF ATTORNEY TO ONE OR MORE REGISTERED PRACTITIONERS

NOTE: This form is to be submitted with the Power of Attorney by Applicant form (PTO/AIA/82B) to identify the application to which the Power of Attorney is directed, in accordance with 37 CFR 1.5, unless the application number and filing date are identified in the Power of Attorney by Applicant form. If neither form PTO/AIA/82A nor form PTO/AIA82B identifies the application to which the Power of Attorney is directed, the Power of Attorney will not be recognized in the application.

Application Number	To Be Assigned
Filing Date	Herewith
First Named Inventor	Jun LIU
Title	MULTIPLE-STACK THREE-DIMENSIONAL MEMORY DEVICE AND FABRICATION METHOD THEREOF
Art Unit	To Be Assigned
Examiner Name	To Be Assigned
Attorney Docket Number	4123.0350001

SIGNATURE of Applicant or Patent Practitioner

Signature	/Donald J. Featherstone/	Date (Optional)	9/10/18
Name	Donald J. Featherstone	Registration Number	33,876
Title (if Applicant is a juristic entity)	Attorney for Applicant		
Applicant Name (if Applicant is a juristic entity)	Yangtze Memory Technologies Co., Ltd.		

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4(d) for signature requirements and certifications. If more than one applicant, use multiple forms.

☑ *Total of one (1) forms are submitted.

This collection of information is required by 37 CFR 1.131, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Doc Code: PA..
Document Description: Power of Attorney

PTO/AIA/82B (07-13)
Approved for use through 01/31/2018. OMB 0651-0035
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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POWER OF ATTORNEY BY APPLICANT

I hereby revoke all previous powers of attorney given in the application identified in either the attached transmittal letter or the boxes below.

Application Number	Filing Date

(Note: The boxes above may be left blank if information is provided on form PTO/AIA/82A.)

☑ I hereby appoint the Patent Practitioner(s) associated with the following Customer Number as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above: 26111

OR

☐ I hereby appoint Practitioner(s) named in the attached list (form PTO/AIA/82C) as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the patent application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above. (Note: Complete form PTO/AIA/82C.)

Please recognize or change the correspondence address for the application identified in the attached transmittal letter or the boxes above to:

☑ The address associated with the above-mentioned Customer Number

OR

☐ The address associated with Customer Number: 26111

OR

☐ Firm or Individual Name					
Address					
City		State		Zip	
Country					
Telephone		Email			

I am the Applicant (if the Applicant is a juristic entity, list the Applicant name in the box):

Yangtze Memory Technologies Co., Ltd.

☐ Inventor or Joint Inventor (title not required below)

☐ Legal Representative of a Deceased or Legally Incapacitated Inventor (title not required below)

☑ Assignee or Person to Whom the Inventor is Under an Obligation to Assign (provide signer's title if applicant is a juristic entity)

☐ Person Who Otherwise Shows Sufficient Proprietary Interest (e.g., a petition under 37 CFR 1.46(b)(2) was granted in the application or is concurrently being filed with this document) (provide signer's title if applicant is a juristic entity)

✓ 1 **SIGNATURE of Applicant for Patent**

The undersigned (whose title is supplied below) is authorized to act on behalf of the applicant (e.g., where the applicant is a juristic entity).

Signature		Date (Optional)	
Name	Simon Shi-Ning Yang		
Title	CEO		

NOTE: Signature - This form must be signed by the applicant in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. If more than one applicant, use multiple forms.

☐ Total of forms are submitted.

This collection of information is required by 37 CFR 1.131, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Electronic Acknowledgement Receipt

EFS ID:	33675716
Application Number:	16126919
International Application Number:	
Confirmation Number:	4582
Title of Invention:	MULTIPLE-STACK THREE-DIMENSIONAL MEMORY DEVICE AND FABRICATION METHOD THEREOF
First Named Inventor/Applicant Name:	Jun LIU
Customer Number:	26111
Filer:	Donald J. Featherstone/Tonyia Skinner
Filer Authorized By:	Donald J. Featherstone
Attorney Docket Number:	4123.0350001
Receipt Date:	10-SEP-2018
Filing Date:	
Time Stamp:	18:23:34
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		41230350001ContinuationApplication.pdf	2079004 f4c84a5291dab91985f0bc1050fb8978a8748c4b	yes	75

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Transmittal Letter	1	2
	Transmittal of New Application	3	4
	Authorization for Extension of Time all replies	5	5
	Application Data Sheet	6	16
	Specification	17	54
	Claims	55	59
	Abstract	60	60
	Drawings-only black and white line drawings	61	73
	Power of Attorney	74	75
Warnings:			
Information:			
	Total Files Size (in bytes):	2079004	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

<u>New Applications Under 35 U.S.C. 111</u>
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
<u>National Stage of an International Application under 35 U.S.C. 371</u>
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
<u>New International Application Filed with the USPTO as a Receiving Office</u>
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

DONALD J. FEATHERSTONE
DIRECTOR
(202) 772-8629
DONF@STERNEKESSLER.COM

September 10, 2018

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Re: U.S. Non-Provisional Patent Application under 37 C.F.R. § 1.53(b)
(*Continuation of Appl. No. PCT/CN2018/097432; Filed: July 27, 2018*)
Appl. No. *To Be Assigned*; Filed: *Herewith*
For: **MULTIPLE-STACK THREE-DIMENSIONAL MEMORY DEVICE AND FABRICATION METHOD THEREOF**
Inventors: LIU *et al.*
Our Ref: 4123.0350001

Commissioner:

The following documents are transmitted herewith for appropriate action by the U.S. Patent and Trademark Office:

1. Utility Patent Application Transmittal Form (PTO/AIA/15);

2. Authorization to Treat a Reply As Incorporating An Extension of Time Under 37 C.F.R. § 1.136(a)(3);

3. U.S. Utility Patent Application entitled:

   MULTIPLE-STACK THREE-DIMENSIONAL MEMORY DEVICE AND FABRICATION METHOD THEREOF

   and naming as inventors:

   Jun LIU
   Zongliang HUO
   Li Hong XIAO
   Zhenyu LU
   Qian TAO
   Yushi HU
   Sizhe LI
   Zhao Hui TANG
   Yu Ting ZHOU
   Zhaosong LI

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IPR2024-00790

the application consisting of:

a. An Application Data Sheet (37 C.F.R. § 1.76) (PTO/AIA/14);

b. A specification containing:

i. 38 pages of description prior to the claims;

ii. 5 pages of claims (20 claims);

iii. a one (1) page abstract; and

c. 13 sheets of drawings: (*Figures 1-13*).

4. An executed Power of Attorney by Applicant form (PTO/AIA/82B) and the Transmittal for Power of Attorney form (PTO/AIA/82A).

The above-listed documents are filed electronically.

Correspondence should be sent to Customer Number 26111.

This patent application is being submitted under 37 C.F.R. § 1.53(b) without Declaration and without the required fees.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

/Donald J. Featherstone/

Donald J. Featherstone
Attorney for Applicant
Registration No. 33,876

DJF/Y-G/tas
Enclosures

9960904_1.docx

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Micron v. YMTC
IPR2024-00790

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 16/126,919

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	300
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	660
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	760
TOTAL CLAIMS (37 CFR 1.16(i))	20 minus 20 =	*			OR	x 100 =	0.00
INDEPENDENT CLAIMS (37 CFR 1.16(h))	3 minus 3 =	*				x 460 =	0.00
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	1720

APPLICATION AS AMENDED - PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT A	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
16/126,919	09/10/2018	Jun LIU	4123.0350001

CONFIRMATION NO. 4582

26111
STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
1100 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

FORMALITIES LETTER

OC000000102630263

Date Mailed: 09/28/2018

NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION

FILED UNDER 37 CFR 1.53(b)

Filing Date Granted

Items Required To Avoid Abandonment:

An application number and filing date have been accorded to this application. The item(s) indicated below, however, are missing. Applicant is given **TWO MONTHS** from the date of this Notice within which to file all required items below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

- The statutory basic filing fee is missing.
- The application search fee must be submitted.
- The application examination fee must be submitted.
- Surcharge as set forth in 37 CFR 1.16(f) must be submitted.
  The surcharge is due for any one of:
  - late submission of the basic filing fee, search fee, or examination fee,
  - late submission of inventor's oath or declaration,
  - filing an application that does not contain at least one claim on filing, or
  - submission of an application filed by reference to a previously filed application.

SUMMARY OF FEES DUE:

The fee(s) required within **TWO MONTHS** from the date of this Notice to avoid abandonment is/are itemized below. No entity status discount is in effect. If applicant is qualified for small entity status, a written assertion of small entity status must be submitted to establish small entity status. (See 37 CFR 1.27). If applicant is qualified for micro entity status, an acceptable Certification of Micro Entity Status must be submitted to establish micro entity status. (See 37 CFR 1.29 and forms PTO/SB/15A and 15B.)

- $ **300** basic filing fee.
- $ **160** surcharge.
- $ **660** search fee.
- $ **760** examination fee.
- $(**0**) previous unapplied payment amount.
- $ **1880** TOTAL FEE BALANCE DUE.

Items Required To Avoid Processing Delays:

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Micron v. YMTC
IPR2024-00790

Applicant is notified that the above-identified application contains the deficiencies noted below. No period for reply is set forth in this notice for correction of these deficiencies. However, if a deficiency relates to the inventor's oath or declaration, the applicant must file an oath or declaration in compliance with 37 CFR 1.63, or a substitute statement in compliance with 37 CFR 1.64, executed by or with respect to each actual inventor no later than the expiration of the time period set in the "Notice of Allowability" to avoid abandonment. See 37 CFR 1.53(f).

- A properly executed inventor's oath or declaration has not been received for the following inventor(s):
  Jun LIU
  Zongliang Huo
  Li Hong Xiao
  Zhenyu Lu
  Qian Tao
  Yushi Hu
  Sizhe Li
  Zhao Hui Tang
  Yu Ting Zhou
  Zhaosong Li

Replies must be received in the USPTO within the set time period or must include a proper Certificate of Mailing or Transmission under 37 CFR 1.8 with a mailing or transmission date within the set time period. For more information and a suggested format, see Form PTO/SB/92 and MPEP 512.

Replies should be mailed to:

Mail Stop Missing Parts
Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

Registered users of EFS-Web may alternatively submit their reply to this notice via EFS-Web, including a copy of this Notice and selecting the document description "Applicant response to Pre-Exam Formalities Notice". https://sportal.uspto.gov/authenticate/AuthenticateUserLocalEPF.html

For more information about EFS-Web please call the USPTO Electronic Business Center at 1-866-217-9197 or visit our website at http://www.uspto.gov/ebc.

If you are not using EFS-Web to submit your reply, you must include a copy of this notice.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/tgebre/

Micron Ex. 1002, p. 81
Micron v. YMTC
IPR2024-00790

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
16/126,919	09/10/2018		0.00	4123.0350001	20	3

CONFIRMATION NO. 4582

26111
STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
1100 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

FILING RECEIPT

OC000000102830282

Date Mailed: 09/28/2018

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Inventor(s)

Jun LIU, Wuhan, CHINA;
Zongliang Huo, Wuhan, CHINA;
Li Hong Xiao, Wuhan, CHINA;
Zhenyu Lu, Wuhan, CHINA;
Qian Tao, Wuhan, CHINA;
Yushi Hu, Wuhan, CHINA;
Sizhe Li, Wuhan, CHINA;
Zhao Hui Tang, Wuhan, CHINA;
Yu Ting Zhou, Wuhan, CHINA;
Zhaosong Li, Wuhan, CHINA;

Applicant(s)

Yangtze Memory Technologies Co., Ltd., Wuhan, CHINA

Assignment For Published Patent Application

Yangtze Memory Technologies Co., Ltd., Wuhan, CHINA

Power of Attorney: The patent practitioners associated with Customer Number 26111

Domestic Priority data as claimed by applicant

This application is a CON of PCT/CN2018/097432 07/27/2018

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.) - None.
Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

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Permission to Access Application via Priority Document Exchange: Yes

Permission to Access Search Results: Yes

Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

If Required, Foreign Filing License Granted: 09/26/2018

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 16/126,919**

Projected Publication Date: To Be Determined - pending completion of Missing Parts

Non-Publication Request: No

Early Publication Request: No

Title

MULTIPLE-STACK THREE-DIMENSIONAL MEMORY DEVICE AND FABRICATION METHOD THEREOF

Preliminary Class

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

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For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

SelectUSA

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The U.S. offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to promote and facilitate business investment. SelectUSA provides information assistance to the international investor

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community; serves as an ombudsman for existing and potential investors; advocates on behalf of U.S. cities, states, and regions competing for global investment; and counsels U.S. economic development organizations on investment attraction best practices. To learn more about why the United States is the best country in the world to develop technology, manufacture products, deliver services, and grow your business, visit http://www.SelectUSA.gov or call +1-202-482-6800.

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DONALD J. FEATHERSTONE
DIRECTOR
(202) 772-8629
DONF@STERNEKESSLER.COM

November 28, 2018

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Confirmation No. 4582
Mail Stop Missing Parts

Re: U.S. Patent Application
Appl. No. 16/126,919; Filed: September 10, 2018
For: **MULTIPLE-STACK THREE-DIMENSIONAL MEMORY DEVICE AND FABRICATION METHOD THEREOF**
Inventors: LIU *et al.*
Our Ref: 4123.0350001

Commissioner:

In reply to the "Notice to File Missing Parts of Non-Provisional Application," dated September 28, 2018, Applicant transmit the following documents for appropriate action by the U.S. Patent and Trademark Office:

1. Online Credit Card Payment Authorization for **$1,880.00** to cover:

   $ 1,720.00 Patent Application fee (including basic filing, search and examination fees)
   $ 160.00 Surcharge for late filing fee or late Oath or Declaration;

2. Original Combined Declaration and Assignment, executed by the inventors; and

3. Copy of Notice to File Missing Parts of Nonprovisional Application.

The above-listed documents are filed electronically.

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Fee payment is provided through online credit card payment. The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036. If extensions of time under 37 C.F.R. § 1.136 other than those otherwise provided for herewith are required to prevent abandonment of the present patent application, then such extensions of time are hereby petitioned, and any fees therefor are hereby authorized to be charged to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

/Donald J. Featherstone/

Donald J. Featherstone
Attorney for Applicant
Registration No. 33,876

DJF/Y-G/cms
Enclosures

10372934_1.docx

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Atty. Docket No. 4123.0350001

COMBINED DECLARATION AND ASSIGNMENT

DECLARATION

As the below named inventors, I hereby declare that:

This declaration is directed to:

☐ The attached application, or

☒ United States application or PCT international application number 16/126,919

filed on September 10, 2018

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. § 1001 by fine or imprisonment of not more than five (5) years, or both.

ASSIGNMENT

In consideration of the sum of One Dollar ($1.00) or equivalent and other good and valuable consideration paid to each of the below named inventors, each of the below named inventors, hereby sell and assign to **Yangtze Memory Technologies Co., Ltd.**, a corporation formed under the laws of China, whose mailing address is 18 Gaoxin 4th Road, East Lake High-Tech Development Zone, Wuhan, Hubei, China (hereafter referred to as the Assignee), his/her entire right, title and interest, including the right to sue for past infringement and to collect for all past, present and future damages, for the United States of America (as defined in 35 U.S.C. § 100) and throughout the world,

(a) in the invention(s) known as **MULTIPLE-STACK THREE-DIMENSIONAL MEMORY DEVICE AND FABRICATION METHOD THEREOF** for which application(s) for patent in the United States of America is identified above, in any and all applications thereon, in any and all Letters Patent(s) therefor, and

(b) in any and all applications that claim the benefit of the patent application identified above in part (a), including non-provisional applications, continuing (continuation, divisional, or continuation-in-part) applications, reissues, extensions, renewals and reexaminations of the patent application or Letters Patent therefor listed above in part (a), to the full extent of the term or terms for which Letters Patents issue, and

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(c) in any and all inventions described in the patent application identified above in part (a), and in any and all forms of intellectual and industrial property protection derivable from such patent application, and that are derivable from any and all continuing applications, reissues, extensions, renewals and reexaminations of such patent application, including, without limitation, patents, applications, utility models, inventor's certificates, and designs together with the right to file applications therefor; and including the right to claim the same priority rights from any previously filed applications under the International Agreement for the Protection of Industrial Property, or any other international agreement, or the domestic laws of the country in which any such application is filed, as may be applicable;

all such rights, title and interest to be held and enjoyed by the above-named Assignee, its successors, legal representatives and assigns to the same extent as all such rights, title and interest would have been held and enjoyed by the Assignor had this assignment and sale not been made.

The below named inventors agree to execute all papers necessary in connection with the application(s) and any non-provisional, continuing (continuation, divisional, or continuation-in-part), reissue, reexamination or corresponding application(s) thereof and also to execute separate assignments in connection with such application(s) as the Assignee may deem necessary or expedient.

The below named inventors agree to execute all papers necessary in connection with any patent enforcement action (judicial or otherwise) related to the application(s) or any non-provisional, continuing (continuation, divisional, or continuation-in-part), reissue or reexamination application(s) thereof and to cooperate with the Assignee in every way possible in obtaining evidence and going forward with such patent enforcement action.

The below named inventors hereby represent that he/she has full right to convey the entire interest herein assigned, and that he/she has not executed, and will not execute, any agreement in conflict therewith.

The below named inventors hereby represent that he/she understands that the patent practitioners associated with **CUSTOMER NUMBER 26111** are the legal representatives of, and attorneys for, the assignee, and are NOT the legal representatives of, and attorneys for, the inventors.

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IN WITNESS WHEREOF, executed by the below named inventors on the date opposite his/her name.

LEGAL NAME OF INVENTOR

Inventor: **Jun LIU** Date: 2018.10.23

Signature of Inventor: Jun Liu

LEGAL NAME OF INVENTOR

Inventor: **Zongliang HUO** Date: 2018.11.1

Signature of Inventor: Zongliang Huo

LEGAL NAME OF INVENTOR

Inventor: **Li Hong XIAO** Date: 2018.10.16

Signature of Inventor: Lihong Xiao

LEGAL NAME OF INVENTOR

Inventor: **Zhenyu LU** Date: 2018.10.16

Signature of Inventor: Zhenyu Lu

LEGAL NAME OF INVENTOR

Inventor: **Qian TAO** Date: 2018.10.16

Signature of Inventor: Qian Tao

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IPR2024-00790

LEGAL NAME OF INVENTOR

Inventor: **Yushi HU** Date: 2018. 10. 16

Signature of Inventor: _____

LEGAL NAME OF INVENTOR

Inventor: **Sizhe LI** Date: 2018-10-16

Signature of Inventor: 李思哲 Sizhe LI

LEGAL NAME OF INVENTOR

Inventor: **Zhao Hui TANG** Date: _____

Signature of Inventor: Zhao Hui TANG 2018-10-16

LEGAL NAME OF INVENTOR

Inventor: **Yu Ting ZHOU** Date: _____

Signature of Inventor: Yu Ting ZHOU 2018-10-16

LEGAL NAME OF INVENTOR

Inventor: **Zhaosong LI** Date: 2018-10-16

Signature of Inventor: Zhaosong Li -

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UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
16/126,919	09/10/2018	Jun LIU	4123.0350001

CONFIRMATION NO. 4582

26111
STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
1100 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

FORMALITIES LETTER

OC000000102630263

Date Mailed: 09/28/2018

NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION

FILED UNDER 37 CFR 1.53(b)

Filing Date Granted

Items Required To Avoid Abandonment:

An application number and filing date have been accorded to this application. The item(s) indicated below, however, are missing. Applicant is given **TWO MONTHS** from the date of this Notice within which to file all required items below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

- The statutory basic filing fee is missing.
- The application search fee must be submitted.
- The application examination fee must be submitted.
- Surcharge as set forth in 37 CFR 1.16(f) must be submitted.
  The surcharge is due for any one of:
  - late submission of the basic filing fee, search fee, or examination fee,
  - late submission of inventor's oath or declaration,
  - filing an application that does not contain at least one claim on filing, or
  - submission of an application filed by reference to a previously filed application.

SUMMARY OF FEES DUE:

The fee(s) required within **TWO MONTHS** from the date of this Notice to avoid abandonment is/are itemized below. No entity status discount is in effect. If applicant is qualified for small entity status, a written assertion of small entity status must be submitted to establish small entity status. (See 37 CFR 1.27). If applicant is qualified for micro entity status, an acceptable Certification of Micro Entity Status must be submitted to establish micro entity status. (See 37 CFR 1.29 and forms PTO/SB/15A and 15B.)

- $ **300** basic filing fee.
- $ **160** surcharge.
- $ **660** search fee.
- $ **760** examination fee.
- $(**0**) previous unapplied payment amount.
- $ **1880** TOTAL FEE BALANCE DUE.

Items Required To Avoid Processing Delays:

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Applicant is notified that the above-identified application contains the deficiencies noted below. No period for reply is set forth in this notice for correction of these deficiencies. However, if a deficiency relates to the inventor's oath or declaration, the applicant must file an oath or declaration in compliance with 37 CFR 1.63, or a substitute statement in compliance with 37 CFR 1.64, executed by or with respect to each actual inventor no later than the expiration of the time period set in the "Notice of Allowability" to avoid abandonment. See 37 CFR 1.53(f).

- A properly executed inventor's oath or declaration has not been received for the following inventor(s):
  Jun LIU
  Zongliang Huo
  Li Hong Xiao
  Zhenyu Lu
  Qian Tao
  Yushi Hu
  Sizhe Li
  Zhao Hui Tang
  Yu Ting Zhou
  Zhaosong Li

Replies must be received in the USPTO within the set time period or must include a proper Certificate of Mailing or Transmission under 37 CFR 1.8 with a mailing or transmission date within the set time period. For more information and a suggested format, see Form PTO/SB/92 and MPEP 512.

Replies should be mailed to:

Mail Stop Missing Parts
Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

Registered users of EFS-Web may alternatively submit their reply to this notice via EFS-Web, including a copy of this Notice and selecting the document description "Applicant response to Pre-Exam Formalities Notice". https://sportal.uspto.gov/authenticate/AuthenticateUserLocalEPF.html

For more information about EFS-Web please call the USPTO Electronic Business Center at 1-866-217-9197 or visit our website at http://www.uspto.gov/ebc.

If you are not using EFS-Web to submit your reply, you must include a copy of this notice.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/tgebre/

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Electronic Patent Application Fee Transmittal

Application Number:	16126919
Filing Date:	10-Sep-2018
Title of Invention:	MULTIPLE-STACK THREE-DIMENSIONAL MEMORY DEVICE AND FABRICATION METHOD THEREOF
First Named Inventor/Applicant Name:	Jun LIU
Filer:	Donald J. Featherstone/Catherine Saunders
Attorney Docket Number:	4123.0350001

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
UTILITY APPLICATION FILING	1011	1	300	300
UTILITY SEARCH FEE	1111	1	660	660
UTILITY EXAMINATION FEE	1311	1	760	760
Pages:				
Claims:				
Miscellaneous-Filing:				
LATE FILING FEE FOR OATH OR DECLARATION	1051	1	160	160
Petition:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	1880

Electronic Acknowledgement Receipt

EFS ID:	34417045
Application Number:	16126919
International Application Number:	
Confirmation Number:	4582
Title of Invention:	MULTIPLE-STACK THREE-DIMENSIONAL MEMORY DEVICE AND FABRICATION METHOD THEREOF
First Named Inventor/Applicant Name:	Jun LIU
Customer Number:	26111
Filer:	Donald J. Featherstone/Catherine Saunders
Filer Authorized By:	Donald J. Featherstone
Attorney Docket Number:	4123.0350001
Receipt Date:	28-NOV-2018
Filing Date:	10-SEP-2018
Time Stamp:	12:02:56
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$1880
RAM confirmation Number	112818INTEFSW12035701
Deposit Account	
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Applicant Response to Pre-Exam Formalities Notice	Cover-Letter-4123-0350001.PDF	246891 1e8552070c72c2b9437f87581318f1900a362174	no	2
Warnings:					
Information:					
2	Oath or Declaration filed	Declaration-4123-0350001.PDF	139125 ecb4b304ea843ee159b4a96c5dd31d36be27d02e	no	4
Warnings:					
Information:					
3	Miscellaneous Incoming Letter	Notice-Missing-Parts-4123-0350001.PDF	1984863 e4118209ee1ded3c237dedc259b8b4e2f22c4ef5	no	2
Warnings:					
Information:					
4	Fee Worksheet (SB06)	fee-info.pdf	37166 97d5e3056a89c80a0a4c005e4bdb8322e85b8494	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	2408045		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PATENT ASSIGNMENT COVER SHEET

Electronic Version v1.1
Stylesheet Version v1.2

EPAS ID: PAT5256341

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNMENT

CONVEYING PARTY DATA

Name	Execution Date
JUN LIU	10/23/2018
ZONGLIANG HUO	11/01/2018
LI HONG XIAO	10/16/2018
ZHENYU LU	10/16/2018
QIAN TAO	10/16/2018
YUSHI HU	10/16/2018
SIZHE LI	10/16/2018
ZHAO HUI TANG	10/16/2018
YU TING ZHOU	10/16/2018
ZHAOSONG LI	10/16/2018

RECEIVING PARTY DATA

Name:	YANGTZE MEMORY TECHNOLOGIES CO., LTD.
Street Address:	18 GAOXIN 4TH ROAD
City:	WUHAN, HUBEI
State/Country:	CHINA

PROPERTY NUMBERS Total: 1

Property Type	Number
Application Number:	16126919

CORRESPONDENCE DATA

Fax Number: (202)371-2540

Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent using a fax number, if provided; if that is unsuccessful, it will be sent via US Mail.

Phone: 202/371-2600
Email: ygao@sternekessler.com, ttopssecretary1@sternekessler.com
Correspondent Name: STERNE KESSLER GOLDSTEIN & FOX P.L.L.C
Address Line 1: 1100 NEW YORK AVENUE, N.W.
Address Line 4: WASHINGTON, D.C. 20005

ATTORNEY DOCKET NUMBER:	4123.0350001
NAME OF SUBMITTER:	DONALD J. FEATHERSTONE

SIGNATURE:	/Donald J. Featherstone/
DATE SIGNED:	11/28/2018
	This document serves as an Oath/Declaration (37 CFR 1.63).

Total Attachments: 4
source=Assignment-4123-0350001#page1.tif
source=Assignment-4123-0350001#page2.tif
source=Assignment-4123-0350001#page3.tif
source=Assignment-4123-0350001#page4.tif

Atty. Docket No. 4123.0350001

COMBINED DECLARATION AND ASSIGNMENT

DECLARATION

As the below named inventors, I hereby declare that:

This declaration is directed to:

☐ The attached application, or

☒ United States application or PCT international application number 16/126,919

filed on September 10, 2018

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. § 1001 by fine or imprisonment of not more than five (5) years, or both.

ASSIGNMENT

In consideration of the sum of One Dollar ($1.00) or equivalent and other good and valuable consideration paid to each of the below named inventors, each of the below named inventors, hereby sell and assign to **Yangtze Memory Technologies Co., Ltd.**, a corporation formed under the laws of China, whose mailing address is 18 Gaoxin 4th Road, East Lake High-Tech Development Zone, Wuhan, Hubei, China (hereafter referred to as the Assignee), his/her entire right, title and interest, including the right to sue for past infringement and to collect for all past, present and future damages, for the United States of America (as defined in 35 U.S.C. § 100) and throughout the world,

(a) in the invention(s) known as **MULTIPLE-STACK THREE-DIMENSIONAL MEMORY DEVICE AND FABRICATION METHOD THEREOF** for which application(s) for patent in the United States of America is identified above, in any and all applications thereon, in any and all Letters Patent(s) therefor, and

(b) in any and all applications that claim the benefit of the patent application identified above in part (a), including non-provisional applications, continuing (continuation, divisional, or continuation-in-part) applications, reissues, extensions, renewals and reexaminations of the patent application or Letters Patent therefor listed above in part (a), to the full extent of the term or terms for which Letters Patents issue, and

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(c) in any and all inventions described in the patent application identified above in part (a), and in any and all forms of intellectual and industrial property protection derivable from such patent application, and that are derivable from any and all continuing applications, reissues, extensions, renewals and reexaminations of such patent application, including, without limitation, patents, applications, utility models, inventor's certificates, and designs together with the right to file applications therefor; and including the right to claim the same priority rights from any previously filed applications under the International Agreement for the Protection of Industrial Property, or any other international agreement, or the domestic laws of the country in which any such application is filed, as may be applicable;

all such rights, title and interest to be held and enjoyed by the above-named Assignee, its successors, legal representatives and assigns to the same extent as all such rights, title and interest would have been held and enjoyed by the Assignor had this assignment and sale not been made.

The below named inventors agree to execute all papers necessary in connection with the application(s) and any non-provisional, continuing (continuation, divisional, or continuation-in-part), reissue, reexamination or corresponding application(s) thereof and also to execute separate assignments in connection with such application(s) as the Assignee may deem necessary or expedient.

The below named inventors agree to execute all papers necessary in connection with any patent enforcement action (judicial or otherwise) related to the application(s) or any non-provisional, continuing (continuation, divisional, or continuation-in-part), reissue or reexamination application(s) thereof and to cooperate with the Assignee in every way possible in obtaining evidence and going forward with such patent enforcement action.

The below named inventors hereby represent that he/she has full right to convey the entire interest herein assigned, and that he/she has not executed, and will not execute, any agreement in conflict therewith.

The below named inventors hereby represent that he/she understands that the patent practitioners associated with **CUSTOMER NUMBER 26111** are the legal representatives of, and attorneys for, the assignee, and are NOT the legal representatives of, and attorneys for, the inventors.

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IN WITNESS WHEREOF, executed by the below named inventors on the date opposite his/her name.

LEGAL NAME OF INVENTOR

Inventor: **Jun LIU** Date: 2018.10.23

Signature of Inventor: Jun Liu

LEGAL NAME OF INVENTOR

Inventor: **Zongliang HUO** Date: 2018.11.1

Signature of Inventor: Zongliang Huo

LEGAL NAME OF INVENTOR

Inventor: **Li Hong XIAO** Date: 2018.10.16

Signature of Inventor: Lihong Xiao

LEGAL NAME OF INVENTOR

Inventor: **Zhenyu LU** Date: 2018.10.16

Signature of Inventor: Zhenyu Lu

LEGAL NAME OF INVENTOR

Inventor: **Qian TAO** Date: 2018.10.16

Signature of Inventor: Qian Tao

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Micron v. YMTC
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LEGAL NAME OF INVENTOR

Inventor: **Yushi HU** Date: 2018.10.16

Signature of Inventor: _____

LEGAL NAME OF INVENTOR

Inventor: **Sizhe LI** Date: 2018-10-16

Signature of Inventor: 李思哲 Sizhe LI

LEGAL NAME OF INVENTOR

Inventor: **Zhao Hui TANG** Date: _____

Signature of Inventor: Zhao Hui TANG 2018-10-16

LEGAL NAME OF INVENTOR

Inventor: **Yu Ting ZHOU** Date: _____

Signature of Inventor: Yu Ting ZHOU 2018-10-16

LEGAL NAME OF INVENTOR

Inventor: **Zhaosong LI** Date: 2018-10-16

Signature of Inventor: Zhaosong Li -

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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
16/126,919	09/10/2018		1880	4123.0350001	20	3

CONFIRMATION NO. 4582

UPDATED FILING RECEIPT

26111
STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
1100 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

OC000000104197302

Date Mailed: 11/30/2018

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Inventor(s)

Jun LIU, Wuhan, CHINA;
Zongliang Huo, Wuhan, CHINA;
Li Hong Xiao, Wuhan, CHINA;
Zhenyu Lu, Wuhan, CHINA;
Qian Tao, Wuhan, CHINA;
Yushi Hu, Wuhan, CHINA;
Sizhe Li, Wuhan, CHINA;
Zhao Hui Tang, Wuhan, CHINA;
Yu Ting Zhou, Wuhan, CHINA;
Zhaosong Li, Wuhan, CHINA;

Applicant(s)

Yangtze Memory Technologies Co., Ltd., Wuhan, CHINA

Assignment For Published Patent Application

Yangtze Memory Technologies Co., Ltd., Wuhan, CHINA

Power of Attorney: The patent practitioners associated with Customer Number 26111

Domestic Priority data as claimed by applicant

This application is a CON of PCT/CN2018/097432 07/27/2018

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.) - None.
Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

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Permission to Access Application via Priority Document Exchange: Yes

Permission to Access Search Results: Yes

Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

If Required, Foreign Filing License Granted: 09/26/2018

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 16/126,919**

Projected Publication Date: 01/30/2020

Non-Publication Request: No

Early Publication Request: No

Title

MULTIPLE-STACK THREE-DIMENSIONAL MEMORY DEVICE AND FABRICATION METHOD THEREOF

Preliminary Class

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

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Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

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For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

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PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 16/126,919

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	300
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	660
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	760
TOTAL CLAIMS (37 CFR 1.16(i))	20 minus 20 =	*			OR	x 100 =	0.00
INDEPENDENT CLAIMS (37 CFR 1.16(h))	3 minus 3 =	*				x 460 =	0.00
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	1720

APPLICATION AS AMENDED - PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT A	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

Equivalent of Form PTO/SB/08a (07-09)

Substitute for form 1449/PTO				*Complete if Known*	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*				Application Number	16/126,919
				Filing Date	September 10, 2018
				First Named Inventor	Jun LIU
				Art Unit	2811
				Examiner Name	GURLEY, Lynne Ann
Sheet	1	of	1	Attorney Docket Number	4123.0350001

U.S. PATENT DOCUMENTS

Examiner initials*	Cite No.[1]	Document Number Number-Kind Code [2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	US1	2016/0268263 A1	09-15-2016	Lee et al.	
	US2	2018/0166329 A1	06-14-2018	Huang et al.	
	US3	2018/0174044 A1	06-21-2018	Na	
	US4	2018/0233512 A1	08-16-2018	Van Houdt et al.	
	US5	9,570,463 B1	02-14-2017	Zhang et al.	
	US6	9,576,967 B1	02-21-2017	Kimura et al.	

FOREIGN PATENT DOCUMENTS

Examiner initials*	Cite No.[1]	Foreign Patent Document Country Code[3]-Number[4]-Kind Code[5] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]
	FP1	CN 105977257 A	09-28-2016	SK HYNIX INC		
	FP2	WO 2016/205078 A2	12-22-2016	SANDISK TECHNOLOGIES LLC		
	FP3	CN 107431063 A	12-01-2017	SANDISK TECHNOLOGIES LLC		
	FP4	CN 107680972 A	02-09-2018	CHANGJIANG STORAGE TECH CO LTD		X
	FP5	CN 108093656 A	05-29-2018	SANDISK TECHNOLOGIES INC		
	FP6	KR 20180076298 A	07-05-2018	IMEC VZW		
	FP7	CN 108615701 A	10-02-2018	TAIWAN SEMICONDUCTOR MFG CO LTD		

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Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1] Applicant's unique citation designation number (optional). [2] See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. [3] Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [6] Applicant is to place a check mark here if English language Translation is attached.

Equivalent of Form PTO/SB/08b (7-09)

Substitute for form 1449/PTO				*Complete if Known*	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*				Application Number	16/126,919
				Filing Date	September 10, 2018
				First Named Inventor	LIU, Jun
				Art Unit	2811
				Examiner Name	GURLEY, Lynne Ann
Sheet	1	of	1	Attorney Docket Number	4123.0350001

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	T[2]
	NPL1	International Search Report and Written Opinion of the International Searching Authority directed to related International Patent Application No. PCT/CN2018/097432, mailed April 16, 2019; 8 pages.	

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Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.
[1] Applicant's unique citation designation number (optional). [2] Applicant is to place a check mark here if English language Translation is attached.

(19)中华人民共和国国家知识产权局

(12)发明专利申请

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(43)申请公布日 2016.09.28

(21)申请号 201510398142.2

(22)申请日 2015.07.08

(30)优先权数据
10-2015-0033817 2015.03.11 KR
10-2015-0054732 2015.04.17 KR

(71)申请人 爱思开海力士有限公司
地址 韩国京畿道

(72)发明人 李起洪 皮昇浩

(74)专利代理机构 北京弘权知识产权代理事务所（普通合伙） 11363
代理人 俞波 许伟群

(51)Int.Cl.
H01L 27/115(2006.01)
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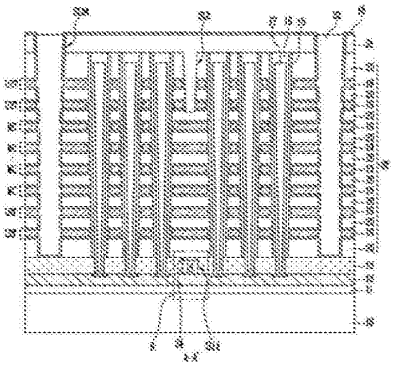
权利要求书2页 说明书21页 附图42页

(54)发明名称

半导体器件及其制造方法

(57)摘要

一种半导体器件包括：衬底，在衬底中定义了单元区和位于单元区两侧的接触区；第一源极层，形成在衬底之上；第二源极层，形成在第一源极层之上；加固图案，形成在第二源极层中；层叠结构，包括在第二源极层和加固图案之上相互交替层叠的导电层和绝缘层；沟道层，穿过层叠结构和第二源极层且电耦接至第二源极层；以及隔离绝缘图案，穿过导电层的至少一个顶部导电层。



CN 105977257 A

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1. 一种半导体器件，包括：

衬底，在所述衬底中定义了单元区和位于所述单元区两侧的接触区；

第一源极层，形成在所述衬底之上；

第二源极层，形成在所述第一源极层之上；

加固图案，形成在所述第二源极层中；

层叠结构，包括在所述第二源极层和所述加固图案之上交替地层叠的导电层和绝缘层；

沟道层，穿过所述层叠结构和所述第二源极层且电耦接至所述第二源极层；以及

隔离绝缘图案，穿过所述导电层的至少一个顶部导电层。

2. 如权利要求 1 所述的半导体器件，其中，所述隔离绝缘图案位于所述加固图案之上且与所述加固图案重叠。

3. 如权利要求 1 所述的半导体器件，其中，所述加固图案包括位于所述单元区和所述接触区的边界的线形图案。

4. 如权利要求 1 所述的半导体器件，其中，所述加固图案包括位于所述单元区或所述接触区中的线形图案。

5. 如权利要求 4 所述的半导体器件，其中，所述隔离绝缘图案与位于所述单元区中的所述线形图案重叠。

6. 如权利要求 1 所述的半导体器件，其中，所述加固图案包括与相邻存储块之间的边界邻近的岛形图案。

7. 如权利要求 1 所述的半导体器件，其中，所述加固图案包括绝缘材料。

8. 如权利要求 1 所述的半导体器件，还包括：

狭缝绝缘层，所述狭缝绝缘层穿过所述层叠结构而与所述第二源极层接触，并且不与所述加固图案重叠。

9. 一种制造半导体器件的方法，所述方法包括：

形成第一牺牲层；

形成包括交替地层叠在所述第一牺牲之上的第二牺牲层和绝缘层的层叠结构；

形成穿过所述层叠结构和所述第一牺牲层的沟道层、以及围绕所述沟道层的存储层；

形成穿过所述层叠结构的狭缝；

在所述狭缝的内壁上形成保护层；

利用所述保护层作为刻蚀阻挡物来去除所述第一牺牲层，据此形成暴露所述存储层的开口；

去除由所述开口暴露的存储层；以及

在所述开口中形成与所述沟道层接触的源极层。

10. 一种制造半导体器件的方法，所述方法包括：

形成牺牲层；

在所述牺牲层中形成加固图案；

在所述牺牲层和所述加固图案之上形成层叠结构；

形成穿过所述层叠结构和所述牺牲层的沟道层；

形成穿过所述层叠结构且暴露所述牺牲层的狭缝；

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经由所述狭缝去除所述牺牲层来形成开口，其中，所述开口由所述加固图案支撑；以及形成源极层且在所述开口中与所述沟道层接触。

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半导体器件及其制造方法

[0001] 相关申请的交叉引用

[0002] 本申请要求2015年3月11日提交的申请号为10-2015-0033817的韩国专利申请以及2015年4月17日提交的申请号为10-2015-0054732的韩国专利申请的优先权，其全部内容通过引用合并于此。

技术领域

[0003] 各种实施例总体而言涉及一种电子器件及其制造方法，具体而言涉及一种具有三维结构的半导体器件及其制造方法。

背景技术

[0004] 非易失性存储器件在缺乏电源时保持所储存的数据。就提高集成度而言，具有制造于硅衬底之上的单层中的存储器单元的二维存储器已经达到其极限。相应地，已经提出具有在垂直方向层叠于硅衬底之上的存储器单元的三维非易失性存储器件。

[0005] 三维非易失性存储器件可以包括具有相互层叠的存储器单元的存储器串。三维非易失性存储器件的存储器串可以通过相互交替层叠导电层和绝缘层来形成层叠结构并且形成穿过层叠结构的沟道层而形成。

发明内容

[0006] 然而，随着层叠结构的高度的增加，难以执行刻蚀过程以及形成耦接至存储器串的源极层。另外，由于处理的局限性，相互层叠的存储器单元可以具有非均匀特性。

[0007] 根据一个实施例的一种半导体器件可以包括定义了单元区和位于单元区两侧的接触区的衬底。所述半导体器件还可以包括形成在衬底之上的第一源极层。所述半导体器件还可以包括形成在第一源极层之上的第二源极层。所述半导体器件还可以包括形成在第二源极层中的加固图案。所述半导体器件还可以包括层叠结构，层叠结构包括在第二源极层和加固图案之上相互交替层叠的导电层和绝缘层。所述半导体器件还可以包括穿过层叠结构和第二源极层且电耦接至第二源极层的沟道层。此外，所述半导体器件还可以包括穿过导电层的至少一个顶部导电层的隔离绝缘图案。

[0008] 在一个实施例中，一种制造半导体器件的方法可以包括形成第一牺牲层。所述方法还可以包括形成层叠结构，层叠结构包括交替层叠于第一牺牲之上的第二牺牲层和绝缘层。所述方法还可以包括形成穿过层叠结构和第一牺牲层的沟道层、以及围绕沟道层的存储层。所述方法还可以包括形成穿过层叠结构的狭缝。所述方法还可以包括在狭缝的内壁上形成保护层。所述方法还可以包括利用保护层作为刻蚀阻挡物来去除第一牺牲层而形成暴露存储层的开口。所述方法还可以包括去除由开口暴露的存储层。此外，所述方法还可以包括在开口中形成接触沟道层的源极层。

[0009] 在一个实施例中，一种制造半导体器件的方法可以包括形成牺牲层。所述方法还可以包括在牺牲层中形成加固图案。所述方法还可以包括在牺牲层和加固图案之上形成层

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叠结构。所述方法还可以包括形成穿过层叠结构和牺牲层的沟道层。所述方法还可以包括形成穿过层叠结构且暴露牺牲层的狭缝。所述方法还可以包括经由狭缝去除牺牲层来形成开口，其中开口由加固图案支撑。此外，所述方法还可以包括形成源极层且在开口中与沟道层接触。

附图说明

[0010] 图 1 是根据一个实施例的半导体器件的结构的布局视图；

[0011] 图 2 是根据一个实施例的半导体器件结构的剖视图；

[0012] 图 3 是根据一个实施例的半导体器件的结构的布局视图；

[0013] 图 4 是根据一个实施例的半导体器件的结构的剖视图；

[0014] 图 5 是根据一个实施例的半导体器件的结构的剖视图；

[0015] 图 6 是根据一个实施例的半导体器件的结构的剖视图；

[0016] 图 7 是根据一个实施例的半导体器件的结构的剖视图；

[0017] 图 8 是根据一个实施例的半导体器件的结构的剖视图；

[0018] 图 9A 至 12A，图 9B 至图 12B 以及图 13 至图 16 是说明根据一个实施例的半导体器件的制造方法的剖视图；

[0019] 图 17A 至图 17D 是说明根据一个实施例的半导体器件的制造方法的局部放大图；

[0020] 图 18 至图 21 是说明根据一个实施例的半导体器件的制造方法的剖视图；

[0021] 图 22 至图 25 是说明根据一个实施例的半导体器件的制造方法的剖视图；

[0022] 图 26 至图 28 是说明根据一个实施例的半导体器件的制造方法的剖视图；

[0023] 图 29 至图 31 是说明根据一个实施例的半导体器件的制造方法的剖视图；

[0024] 图 32 至图 33 是说明根据一个实施例的半导体器件的制造方法的剖视图；

[0025] 图 34 和图 35 是说明根据一个实施例的存储器系统的配置的框图；

[0026] 图 36 和图 37 是说明根据一个实施例的计算系统的配置的框图。

具体实施方式

[0027] 在下文中，将参考附图详细描述各种实施例。在附图中，可能对组件的厚度和长度进行放大，以便于说明。在以下描述中，为了简单和简明可以省略相关功能和构成的详细描述。贯穿说明书和附图，相同的附图标记指代相同的元件。各种实施例针对一种容易制造且具有改善特性的半导体器件及其制造方法。

[0028] 参考图 1 和图 2，分别图示了根据一个实施例的半导体器件的结构的布局视图和剖视图。图 2 是沿图 1 的 A-A’ 线截取的剖视图。

[0029] 在图 1 和图 2 中，根据一个实施例的半导体器件可以包括衬底 10、第一源极层 12、第二源极层 13、加固图案 14、层叠结构 ST、沟道层 16 和隔离绝缘图案 21。

[0030] 可以在衬底 10 上定义单元区 R1 和位于单元区 R1 两边的接触区 R2。存储器串可以布置在单元区 R1 中。每个存储器串可以包括以串联方式电耦接的至少一个下选择晶体管 LST、多个存储器单元 MC 和至少一个上选择晶体管 UST。每个存储器串可以布置在与衬底 10 垂直的方向上。存储器单元 MC 可以在至少一个下选择晶体管 LST 和至少一个上选择晶体管 UST 之间相互层叠和分离。至少一个下选择晶体管 LST 可以布置在存储器单元 MC 和

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衬底 10 之间。电耦接至存储器单元 MC 的栅电极可以延伸至接触区 R2。另外，偏压可以施加至在接触区 R2 中的相互层叠的每个栅电极。栅电极可以在接触区 R2 以阶梯方式层叠，且电耦接至接触区 R2 的接触插塞。

[0031] 第一源极层 12 可以位于衬底之上且包括导电材料，诸如掺杂多晶硅或金属。例如，可以通过在衬底 10 上层叠导电层来形成第一源极层 12。在这个例子中，第一绝缘层 11 可以被插入衬底 10 与第一源极层 12 之间。在一个例子中，可以通过向衬底 10 表面掺杂杂质至预定深度而形成第一源极层 12。在一个例子中，可以不形成第一绝缘层 11。

[0032] 第二源极层 13 可以形成在第一源极层 12 上，且与第一源极层 12 电耦接。例如，第二源极层 13 可以包括金属材料，诸如钨或多晶硅层。

[0033] 第一狭缝 SL1A 和 SL1B 可以穿透第二源极层 13。第二源极层 13 的形状可以由第一狭缝 SL1A 和 SL1B 来定义。第一狭缝 SL1A 和 SL1B 可以包括 A 型第一狭缝 SL1A 和 B 型第一狭缝 SL1B。所述 A 型第一狭缝 SL1A 可以包括位于单元区 R1 和接触区 R2 的边界的第一直线部、位于单元区 R1 且将第一直线部相互连接的至少一个第二直线部以及从第一直线部延伸至接触区 R2 的至少一个第三直线部。B 型第一狭缝 SL1B 可以布置在单元区 R1 和接触区 R2 中的相邻存储块 MB 之间的边界。

[0034] 可以在第一狭缝 SL1A 和 SL1B 中形成加固图案 14。每个加固图案 14 可以是包括氧化物或氮化物的绝缘层。例如，每个加固图案 14 可以包括位于单元区 R1 和接触区 R2 的边界的第一线形图案。每个加固图案 14 还可以包括位于单元区 R1 的第二线形图案以及位于接触区 R2 的至少一个第三线形图案。每个第一线形图案可以形成在 A 型第一狭缝 SL1A 的每个第一直线部。第二线形图案可以形成在 A 型第一狭缝 SL1A 的第二直线部。第三线形图案可以形成在 A 型第一狭缝 SL1A 的每个第三直线部。另外，加固图案 14 可以包括位于单元区 R1 或接触区 R2 的岛形图案。岛形图案可以邻近相邻存储块之间的边界。每个岛形图案可以形成在 B 型第一狭缝 SL1B。然而，加固图案 14 的形状和位置可以改变。另外，刻蚀阻挡层 24 可以位于加固图案 14 上。刻蚀阻挡层 24 可以包括氧化物或氮化物。刻蚀阻挡层 24 相比下述的每个第一存储层 15 的数据储存层可以具有较大厚度。更明确地，刻蚀阻挡层 24 可以是储存层厚度的 2.5 倍。

[0035] 层叠结构 ST 可以位于第二源极层 13 和加固图案 14 之上。层叠结构 ST 可以包括相互交替层叠的导电层 19 和第二绝缘层 20。导电层 19 可以是电耦接至上选择晶体管 UST、下选择晶体管 LST 和存储器单元 MC 的栅电极。可以形成第二绝缘层 20 以使层叠的导电层 19 绝缘。例如，导电层 19 可以包括掺杂多晶硅、钨 (W)、氮化钨 (WNx)、钛 (Ti)、氮化钛 (TiN)、钽 (Ta)、氮化钽 (TaN) 等。每个第二绝缘层 20 可以包括氧化物、氮化物等。

[0036] 沟道层 16 可以位于单元区 R1，沟道层 16 穿过层叠结构 ST 和第二源极层 13，并且电耦接至第二源极层 13。沟道层 16 可以部分地穿过第二源极层 13。沟道层 16 可以交替地完全穿过第二源极层 13 以直接电耦接至第一源极层 12。每个沟道层 16 可以具有开放的中心部。此外，可以用间隙填充绝缘层 17 填充开放的中心部。

[0037] 每个第一存储层 15 可以插入至每个沟道层 16 与导电层 19 之间。第一存储层 15 可以围绕每个沟道层 16 的侧壁。第一存储层 15 可以包括至少一个沟道绝缘层、数据储存层和电荷阻挡层。数据储存层可以包括硅化物、氮化物、相变材料、纳米点等。可以进一步形成第二存储层 18 以围绕每个导电层 19。第二存储层 18 还可以包括至少一个沟道绝缘

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层、数据储存层和电荷阻挡层。数据储存层可以包括硅化物、氮化物、相变材料、纳米点等。图中的第二存储层 18 可以发挥电荷阻挡层的作用并且包括氧化物。

[0038] 分离上选择晶体管 UST 的栅电极的第二狭缝 SL2 可以被隔离绝缘图案 21 所填充。例如，第二狭缝 SL2 可以穿过至少一个导电层 19 并且被隔离绝缘图案 21 所填充。隔离绝缘图案 21 可以从第二狭缝 SL2 的内部延伸来覆盖层叠结构 ST 的顶面。例如，隔离绝缘图案 21 可以包括氧化物、氮化物等。

[0039] 第二狭缝 SL2 和第二狭缝 SL2 中的隔离绝缘图案 21 可以位于加固图案 14 之上。例如，第二狭缝 SL2 中的隔离绝缘图案 21 可以位于加固图案 14 的第二线形图案之上，所述加固图案 14 位于单元区 R1 中。隔离绝缘图案 21 可以与加固图案 14 重叠。在图 1 的布局视图中，只显示了形成在第二狭缝 SL2 中的隔离绝缘层 21 的位置。邻近接触区 R2 的第二狭缝 SL2 的边缘与形成上选择晶体管 UST 的栅电极的导电层 19 的边缘相比可以向接触区 R2 进一步延伸。

[0040] 半导体器件可以进一步包括穿过层叠结构 ST 的第三狭缝 SL3A、SL3B 和第三狭缝 SL3A、SL3B 中的狭缝绝缘层 22。第三狭缝 SL3A、SL3B 可以在半导体器件的制造过程期间用作去除牺牲层的路径和形成第二源极层 13 的路径。第三狭缝 SL3A、SL3B 可以足够深以暴露第二源极层 13，或足够深以延伸至第一源极层 12。第三狭缝 SL3A、SL3B 包括 A 型第三狭缝 SL3A 和 B 型第三狭缝 SL3B。A 型第三狭缝 SL3A 可以形成在相邻存储块 MB 之间的边界。B 型第三狭缝 SL3B 可以布置在每个接触区 R2 中。

[0041] 另外，半导体器件可以进一步包括虚设图案 23。当去除牺牲层以形成导电层 19 时，虚设图案 23 可以用作支撑。虚设图案 23 可以位于接触区 R2 或在加固图案 14 之上。虚设图案 23 可以穿过层叠结构 ST 且具有与沟道层 16 相同的形状。

[0042] 参考图 3，图示了根据一个实施例的半导体器件的结构的布局视图。图 3 是图 1 的改进例子。在下文中，省略了有关参考图 1 和图 2 针对上述的实施例描述的通用内容的描述。

[0043] 在图 3 中，由于可以不形成如图 1 所示的 B 型第一狭缝 SL1B，因此可以获得芯片尺寸的减小。

[0044] 参考图 4，示出了根据一个实施例的半导体器件的结构的剖面图。图 4 是图 2 的改进例子且显示了与图 2 中的区域 B 相应的改进例子的结构。在下文中，省略了有关参考图 1 和图 2 针对上述的实施例描述的通用内容的描述。

[0045] 在图 4 中，加固图案 14 和第一狭缝 SL1A 可以穿过第二源极层 13 和第一源极层 12 而延伸至第一绝缘层 11 的顶面。

[0046] 参考图 5，图示了根据显示了图 2 的改进例子的一个实施例的半导体器件的结构的剖视图。在下文中，省略了有关参考图 1 和图 2 针对上述的实施例描述的通用内容的描述。

[0047] 在图 5 中，第二狭缝 SL2 可以足够深以完全穿过层叠结构 ST。第二狭缝 SL2 和第三狭缝 SL3A 可以同时形成且具有基本上相同的深度。狭缝绝缘层 22 可以形成在第二狭缝 SL2 和第三狭缝 SL3A 中。另外，加固图案可以位于加固图案可以不与第二狭缝 SL2 和第三狭缝 SL3A 重叠的位置。

[0048] 布置在第二狭缝 SL2 与第三狭缝 SL3A 之间的沟道层 16 的数量可以改变。另外，

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沟道层 16 可以被布置成各种配置，诸如矩阵或交错结构。

[0049] 参考图 6，图示了根据一个实施例的半导体器件的结构的剖视图。图 6 显示了图 2 的改进例子。在下文中，省略了有关参考图 1 和图 2 针对上述的实施例描述的通用内容的描述。

[0050] 在图 6 中，可以在第一源极层 12 的部分顶面上形成第二源极层 13，所述第一源极层 12 布置在沟道层 16 与邻近第一源极层 12 的沟道层 16 的底部表面之间。凹部可以形成在第二源极层 13 的表面。第二源极层 13 中的凹部可以形成在第三狭缝 SL3A 下面且具有比第三狭缝 SL3A 更大的宽度。第二源极层 13 中的凹部可以电耦接至第一狭缝 SL1A。第二存储层 18 可以在第二源极层 13 的凹部表面之上延伸。填充第三狭缝 SL3A 的狭缝绝缘层 22 可以延伸至第二源极层 13 的凹部来完全填充第二源极层 13 的凹部。

[0051] 参考图 7，图示了根据一个实施例的半导体器件的结构的剖面图。图 7 是图 6 的改进例子且显示了与图 6 的区域 C 相应的改进例子的结构。在下文中，省略了有关参考图 1 和图 2 针对上述的实施例描述的通用内容的描述。

[0052] 在图 7 中，填充第三狭缝 SL3A 的狭缝绝缘层 22 可以延伸至第二源极层 13 的凹部并且包括间隙 AG。所述间隙 AG 可以是空气隙。间隙 AG 可以配置在相邻沟道层 16 之间的狭窄空间中。间隙 AG 可以配置在加固图案 14 与沟道层 16 之间的狭窄空间中。间隙 AG 可以在第三狭缝 SL3A 在水平方向上延伸的方向上延伸。第三狭缝 SL3A 在水平方向延伸的方向可以定义为与衬底 10 的表面平行的方向。

[0053] 参考图 8，图示了根据一个实施例的半导体器件的结构的剖视图。图 8 是图 6 的改进例子。在下文中，省略了有关参考图 1 和图 2 针对上述的实施例描述的通用内容的描述。

[0054] 在图 8 中，可以在第三狭缝 SL3A 的侧壁上形成狭缝绝缘层 22 来开放穿过层叠结构 ST 的第三狭缝 SL3A 的中心部。狭缝绝缘层 22 可以在第二源极层 13 的凹部表面之上延伸。位于第三狭缝 SL3A 外面的狭缝绝缘层 22 可以基本上平行于层叠结构 ST 的顶面延伸。由狭缝绝缘层 22 开放的第三狭缝 SL3A 的中心部可以由共源极线 29 填充。所述共源极线 29 可以延伸以接触第二源极层 13。共源极线 29 可以在第三狭缝 SL3A 在水平方向上延伸的方向上延伸。共源极线 29 可以将外部施加的源电压传递至第二源极层 13。共源极线 29 可以包括多晶硅或具有比多晶硅低的电阻的金属材料。

[0055] 在参考图 1 至图 8 的上述实施例中，在加固图案 14 与层叠结构 ST 之间未形成任何层，甚至未形成刻蚀阻挡层 24。可替代地，加固图案 14 可以直接接触层叠结构 ST 的第二绝缘层 20 的底层。

[0056] 参考图 9A 至图 12A、图 9B 至图 12B 以及图 13 至图 16，图示了制造根据一个实施例的半导体器件的方法的剖视图。图 9A、图 10A、图 11A 和图 12A 是布局视图，图 9B、图 10B、图 11B 和图 12B 是分别从图 9A、图 10A、图 11A 和图 12A 的 A-A’ 线截取的剖视图。

[0057] 在图 9A 和图 9B 中，可以在衬底 30 上形成第一绝缘层 31。此外，可以在第一绝缘层上 31 形成第一源极层 32。第一源极层 32 可以是包括掺杂多晶硅层、金属层等的导电层。

[0058] 接下来，可以在第一源极层 32 上形成第一牺牲层 34。在第一牺牲层 34 形成之前，可以在第一源极层 32 上形成第二牺牲层 33。第一牺牲层 34 可以包括相对于第二牺牲层 33 具有高刻蚀选择性的材料。例如，第一牺牲层 34 可以包括无掺杂多晶硅层或掺杂多晶硅层。此外，第二牺牲层 33 可以包括氧化物或氮化物。

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[0059] 接下来，第一狭缝 SL1A 和 SL1B 可以穿过第一牺牲层 34 而形成。另外，可以在每个第一狭缝 SL1A 和 SL1B 中形成加固图案 35。第一狭缝 SL1A 和 SL1B 可以足够深以穿过第一牺牲层 34 来暴露第二牺牲层 33、第一源极层 32 或第一绝缘层 31。在形成第一狭缝 SL1A 和 SL1B 之后，可以在第一源极层 32 上形成加固层以填充第一狭缝 SL1A 和 SL1B。接下来，可以使加固层平坦化直到暴露第一牺牲层 34 的表面，以便可以形成加固图案。如以上参考图 1 和图 2 的描述，第一狭缝 SL1A 和 SL1B 可以包括 A 型第一狭缝 SL1A 和 B 型第一狭缝 SL1B。如以上参考图 3 的描述，可以不形成 B 型第一狭缝 SL1B。加固图案 35 可以是包括氧化物、氮化物等的绝缘层。如图 9A 和图 9B 所示，加固图案 35 可以包括线形图案和岛形图案。然而，加固图案 35 的位置和形状可以改变。

[0060] 在图 10A 和图 10B 中，可以在加固图案 35 穿过的第一牺牲层 34 之上形成层叠结构 ST。层叠结构 ST 可以包括相互交替层叠的第三牺牲层 36 和第二绝缘层 37。第三牺牲层 36 可以具有相对于第二牺牲层 37 的高刻蚀选择性。例如，第三牺牲层 36 可以包括氮化物。此外，第二绝缘层 37 可以包括氧化物。

[0061] 第三牺牲层 36 和第二绝缘层 37 可以具有相同或不同的厚度。另外，在第二绝缘层 37 之中的离衬底 30 最远的顶层和第二绝缘层 37 的离衬底 30 最近的底层可以具有与插入于其间的其他绝缘层相比更大的厚度。第二绝缘层 37 的底层可以布置为与第三牺牲层 36 的底层相比更靠近衬底 30。换句话说，第二绝缘层 37 的底层可以定义层叠结构 ST 的底层。

[0062] 在形成层叠结构 ST 之前，可以形成刻蚀阻挡层 EBL。可以形成刻蚀阻挡层 EBL 来防止层叠结构 ST 的底层（即第二绝缘层 37 的底层）在随后的刻蚀过程期间被刻蚀和变薄。刻蚀阻挡层 EBL 可以包括相对于第二绝缘层 37 具有高刻蚀选择性的材料。例如，刻蚀阻挡层 EBL 可以包括与第三牺牲层 36 相同的材料。

[0063] 接下来，第一开口 OP1 可以穿过层叠结构 ST、刻蚀阻挡层 EBL 和第一牺牲层 34 而形成。第一开口 OP1 可以完全穿过第一牺牲层 34 以延伸至第二牺牲层 33 或第一源极层 32。另外，第一开口 OP1 可以位于单元区或接触区。位于单元区的第一开口 OP1 可以是沟道孔。另外，位于接触区的第一开口 OP1 可以是虚设孔。沟道孔可以不与加固图案 35 重叠，而虚设孔可以不与加固图案 35 重叠，或可以与加固图案 35 重叠。

[0064] 在第一存储层 38 可以在第一开口 OP1 中形成之后，可以在其中形成沟道层 39。当沟道层 39 具有中心开放部时，可以在沟道层 39 中形成间隙填充绝缘层 40。

[0065] 在图 11A 和图 11B 中，第二狭缝 SL2 可以从第三牺牲层 36 之中的最远离衬底 30 的顶层穿过层叠结构 ST 到至少一个剩余的第三牺牲层 36 而形成。第二狭缝 SL2 可以形成在位于单元区的加固图案 35 之上。第二狭缝 SL2 可以与加固图案 35 重叠。

[0066] 接下来，可以在第二狭缝 SL2 中形成隔离绝缘图案 41。形成在第二狭缝 SL2 中的隔离绝缘层 41 可以穿过层叠结构 ST 的上部并且与位于单元区的加固图案重叠。形成第二狭缝 SL2 之后，可以形成绝缘层以填充第二狭缝 SL2。接下来，可以使绝缘层平坦化来形成隔离绝缘图案 41。隔离绝缘图案 41 可以与第二狭缝 SL2 一样形成在层叠结构 ST 之上。

[0067] 在图 12A 和图 12B 中，第三狭缝 SL3A 和 SL3B 可以穿过层叠结构 ST 和刻蚀阻挡层 EBL 而形成。每个第三狭缝 SL3A 和 SL3B 的上部和下部可以具有相等的宽度。在替选方案中，其上部可以比其下部宽。如以上参考图 1 和图 2 的描述，第三狭缝 SL3A 和 SL3B 可以包

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括 A 型第三狭缝 SL3A 和 B 型第三狭缝 SL3B。第三狭缝 SL3A 和 SL3B 可以用作去除第一牺牲层 34 的路径和用于形成第二源极层的路径。第三狭缝 SL3A 和 SL3B 可以足够深以完全穿过层叠结构 ST 和刻蚀阻挡层 EBL 来暴露第一牺牲层 34。另外，第三狭缝 SL3A 和 SL3B 可以位于相邻存储块 MB 之间的边界或接触区中。

[0068] 图 13 中，第一牺牲层 34 可以经由第三狭缝 SL3A（图 12A 中的 SL3B）选择性地去除来形成第二开口 OP2，以便围绕沟道层 39 的部分第一存储层 38 可以由第二开口 OP2 暴露。可以不去除而是保留形成在第一牺牲层 34 中的加固图案 35，加固图案 35 支撑层叠结构 ST 来保持第二开口 OP2。换句话说，第二开口 OP2 可以由加固图案 35 稳定地保持。此外，加固图案 35 可以防止形成在第二开口 OP2 之上的层叠结构 ST 的倾斜或倒塌。图 13 还图示了区域 D。将参考与区域 D 有关的图 17A 至图 17D 详细描述在区域 D 中执行的过程。

[0069] 接下来，可以在第三狭缝 SL3A（图 12A 的 SL3B）中形成保护层 42。保护层 42 可以形成在第三狭缝 SL3A（图 12A 的 SL3B）的侧壁上来保持第二开口 O P2 与第三狭缝 SL3A（图 12A 的 SL3B）之间的连接。然而，第三狭缝 SL3A（图 12A 的 SL3B）的底面可以不完全由保护层 42 堵塞。保护层 42 可以是锥形的以使得其厚度可以从第三狭缝 SL3A（图 12A 的 SL3B）上部至邻近衬底 30 的其下部逐渐减少。另外，保护层 42 可以与第三狭缝 SL3A（图 12A 的 SL3B）一样形成在层叠结构 ST 之上。例如，可以利用具有较差的台阶覆盖性的沉积方法，诸如等离子体增强化学气相沉积（PE-CVD）形成保护层 42。如上所述，通过在第三狭缝 SL3A（图 12A 的 SL3B）的侧壁上形成锥形的保护层 42，可以减小每个第三狭缝 SL3A（图 12A 的 SL3B）上部和下部之间的宽度差。保护层 42 可以包括相对于第一牺牲层 34 具有高刻蚀选择性的材料，并且包括氮化物。在第三狭缝 SL3A（图 12A 的 SL3B）中形成保护层 42 之后，可以去除第一牺牲层 34。

[0070] 在图 14 中，可以去除由第二开口 OP2 暴露的第一存储层 38，以便可以通过第二开口 OP2 部分地暴露沟道层 39。当第一存储层 38 延伸至第一源极层 32 时，部分第一存储层 38 可以保留在第一源极层 32 中。

[0071] 当去除第一存储层 38 时，还可以去除第二牺牲层 33 和通过第二开口 OP2 暴露的刻蚀阻挡层 EBL。另外，可以刻蚀未被保护层 42 覆盖且通过第三狭缝 SL3A（图 12A 的 SL3B）下部暴露的第三牺牲层 36 和第二绝缘层 37。当刻蚀包括在第一存储层 38 中的多个层时，可以选择性地刻蚀第三牺牲层 36 或第二绝缘层 37。因此，非平坦性可以形成在每个第三狭缝 SL3A（图 12A 的 SL3B）的下部。例如，未被保护层 42 阻挡的第二绝缘层 37 可以比第三牺牲层 36 被刻蚀得更深。在一个例子中，可以保留被刻蚀的第三牺牲层 36 以便被刻蚀的第三牺牲层 36 相比第二绝缘层 37 可以向第三狭缝 SL3A（图 12A 的 SL3B）的内部更凸出。将参考图 17A 至图 17D 详细描述去除第一存储层 38 的过程。

[0072] 在图 15 中，可以在第二开口 OP2 中形成电耦接至沟道层 39 的第二源极层 43。例如，利用由第二开口 OP2 暴露的沟道层 39 作为种子，第二源极层 43 可以从沟道层 39 选择地生长。第二源极层 43 可以包括多晶硅层。

[0073] 在图 16 中，去除剩余的保护层 42 之后，可以经由第三狭缝 SL3A（图 12A 的 SL3B）来选择性地去除第三牺牲层 36 来形成第三开口 OP3。由于第二绝缘层 37 可以由沟道层 39 和隔离绝缘图案 41 支撑，因此可以增加结构稳定性。

[0074] 另外，根据上述非平坦结构，由于选择性地刻蚀位于层叠结构 ST 下部的一些第二

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绝缘层 37，因此可以增加每个第三狭缝 SL3A（图 12A 的 SL3B）的下宽度。因此，与如图 12B 所示的第三狭缝 SL3A（图 12A 的 SL3B）的初始结构相比，可以减小第三狭缝 SL3A 的最终结构的上部和下部之间的宽度差。

[0075] 接下来，可以在第三开口 OP3 中形成导电层 44。例如，在第三狭缝 SL3A（图 12A 的 SL3B）的内壁上和第三开口 OP3 中形成导电材料。此外，通过去除形成在第三狭缝 SL3A（图 12A 的 SL3B）的内壁中的导电材料，可以形成导电层 44。导电层 44 可以被第三狭缝 SL3A（图 12A 的 SL3B）隔离。由于第三狭缝 SL3A（图 12A 的 SL3B）的下宽度的增加，可以容易地去除形成在第三狭缝 SL3A（图 12A 的 SL3B）内壁上的导电材料，以便导电层 44 可以容易地被第三狭缝 SL3A 隔离。

[0076] 导电层 44 可以包括钨（W）。另外，在第三开口 OP3 中形成导电层 44 之前，可以在第三开口 OP3 中进一步形成第二存储层 45 或阻挡层。阻挡层可以包括钛（Ti）、氮化钛（TiN）、钽（Ta）、氮化钽（TaN）、氮化钨（WNx）等。

[0077] 接下来，可以在每个第三狭缝 SL3A（图 12A 的 SL3B）中形成狭缝绝缘层 46。狭缝绝缘层 46 可以包括氧化物。

[0078] 根据上述制造方法，可以在第一牺牲层 34 中形成加固图案 35。因此，可以在由加固图案 35 支撑的稳定结构中执行形成第二开口 OP2 的过程、去除第一存储层 38 的过程以及形成第二源极层 43 的过程。另外，通过形成隔离绝缘层 41，可以简单地使上选择栅电极绝缘。此外，可以在由隔离绝缘图案 41 支撑的稳定结构中执行去除第三牺牲层 36 的过程。另外，通过利用保护层 42，可以选择性地去除由第二开口 OP2 暴露的第一存储层 38。另外，同时，可以增加每个第三狭缝 SL3A（图 12A 的 SL3B）的下宽度。

[0079] 参考图 17A 至图 17D，图示了说明根据一个实施例的制造半导体器件的方法的部分放大图。图 17A 是图 13 的区域 D 的放大图。图 17B 至图 17D 是图 14 的区域 D 的放大图。去除第一存储层的顺序过程参考图 17A 至图 17D 被描述如下。

[0080] 在图 17A 中，第一存储层 38 可以包括围绕沟道层 39 的沟道绝缘层 38C、围绕沟道绝缘层 38C 的数据储存层 38B 和围绕数据储存层 38B 的电荷阻挡层 38A。沟道绝缘层 38C 和电荷阻挡层 38A 可以包括氧化物。此外，数据储存层 38B 可以包括氮化物。另外，第三牺牲层 36 可以包括氮化物，第二绝缘层 37 可以包括氧化物，第二牺牲层 33 可以包括氧化物，另外，如图 13 至图 15 所示，保护层 42 可以包括氮化物。

[0081] 当形成第二开口 OP2 时，电荷阻挡层 38A、刻蚀阻挡层 EBL 和第二牺牲层 33 的一部分可以由第二开 OP2 暴露。刻蚀阻挡层 EBL 可以形成为具有与数据储存层 38B 相比更大的厚度，以便在数据储存层 38B 的刻蚀过程期间不被去除。更具体地，刻蚀阻挡层 EBL 的厚度可以是数据储存层 38B 的 2.5 倍。

[0082] 在图 17B 中，通过执行刻蚀过程去除由第二开口 OP2 暴露的电荷阻挡层 38A 来暴露数据储存层 38B。可以刻蚀由第二开口 OP2 暴露的第二牺牲层 33 和暴露在第三狭缝下部的第二绝缘层 37。另外，可以保留形成在第一源极层 32 或第二牺牲层 33 中的部分电荷阻挡层 38A。

[0083] 参考图 17C，通过执行刻蚀过程来去除由第二开口 OP2 暴露的数据储存层 38B，可以暴露沟道绝缘层 38C。也可以对刻蚀阻挡层 EBL 进行刻蚀。当刻蚀阻挡层 EBL 的厚度与数据储存层 38B 的厚度相近时，在数据储存层 38B 的刻蚀过程期间可以去除刻蚀阻挡层 EBL

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以暴露第二绝缘层 37 的底层。如以上参考图 17A 的描述，当刻蚀阻挡层 EBL 的厚度大于数据储存层 38B 的厚度时，可以在数据储存层 38B 的刻蚀过程期间减少刻蚀阻挡层 EBL 的厚度。即使当执行数据储存层 38B 的刻蚀过程直到暴露沟道绝缘层 38C 时，也可以不完全去除而保留具有相当大厚度的刻蚀阻挡层 EBL 以保护第二绝缘层 37 的底层。

[0084] 另外，当刻蚀数据储存层 38B 时，也可以刻蚀保护层 42 至预定厚度。结果，可以通过刻蚀的保护层 42 由每个第三狭缝的底部暴露一些第三牺牲层 36 和第二绝缘层 37。保护层 42 的厚度可以在从每个第三狭缝顶部至其底部、朝着衬底 30 的向下方向上逐渐减少。因此，当刻蚀保护层 42 时，可以在从邻近衬底 30 排列的下层方向上依次地暴露第三牺牲层 36 和第二绝缘层 37。结果，邻近衬底 30 的第三牺牲层 36 的下层可以被刻蚀得比其上层深，从而在每个第三狭缝的下部形成为非平坦。

[0085] 参考图 17D，可以通过执行刻蚀过程来去除由第二开口 OP2 暴露的沟道绝缘层 38C 而暴露沟道层 39。当刻蚀沟道绝缘层 38C 时，如图 17C 所示的剩余的刻蚀阻挡层 EBL 可以保护第二绝缘层 37 的底层。因此，可以避免第二绝缘层 37 的底层的厚度损失以保持目标厚度。当刻蚀沟道绝缘层 38C 时，可以去除如图 17C 所示、由第二开口 OP2 暴露的第二牺牲层 33 以暴露第一源极层 32。另外，当刻蚀沟道绝缘层 38C 时，可以去除部分电荷阻挡层 38A。

[0086] 另外，当刻蚀沟道绝缘层 38C 时，可以将未被保护层 42 覆盖的、且由第三狭缝下部暴露的一些第二绝缘层 37 刻蚀至预定厚度。可以去除如图 17C 所示、在刻蚀沟道绝缘层 38C 以暴露沟道层 39 之后剩余的刻蚀阻挡层 EBL。结果，可以暴露第二绝缘层 37 的底层的底面。

[0087] 当刻蚀上述第一存储层 38 时，可以刻蚀具有不同的刻蚀选择性的第二绝缘层 37 和第三牺牲层 36 至不同厚度。因此，在刻蚀第一存储层 38 之后，保留在第三狭缝下部的第二绝缘层 37 和第三牺牲层 36 可以定义非平坦度。第三牺牲层 36 的刻蚀的侧壁与第二绝缘层 37 的刻蚀的侧壁相比可以向每个第三狭缝的内部进一步凸出。

[0088] 参考图 18 至图 21，图示了说明根据实施例的半导体器件的制造方法并且显示了形成保护层的改进的例子的剖视图。在下文中，省略了上述已描述的实施例的通用内容的描述。

[0089] 在图 18 中，可以在衬底 50 上形成第一绝缘层 51、第一源极层 52、第二牺牲层 53、第一牺牲层 54 和加固图案 55。可以在其上形成包括相互交替层叠的第三牺牲层 56 和第二绝缘层 57 的层叠结构 ST。在形成层叠结构 ST 之前，可以进一步形成刻蚀阻挡层 EBL。接下来，可以在其上形成存储层 58、沟道层 59 和间隙填充绝缘层 60。此外，可以从距离衬底 50 最远的第三牺牲层 56 的顶层穿过层叠结构 ST 至至少一个剩余的层来形成第二狭缝 SL2。第二狭缝 SL2 可以用隔离绝缘图案 61 填充。

[0090] 接下来，可以穿过层叠结构 ST 和刻蚀阻挡层 EBL 形成第三狭缝 SL3A 以暴露第一牺牲层 54。可以在第三狭缝 SL3A 中形成保护层 62、63、64。例如，可以在第三狭缝 SL3A 和层叠结构 ST 的表面上形成具有均匀厚度的第一保护层 62。第一保护层 62 可以是由具有优良台阶覆盖的沉积法诸如低压化学气相沉积 (LP-CVD) 形成的氮化物层。相应地，可以在第一保护层 62 上形成锥形的、以便其厚度从顶部至底部向着衬底 50 逐渐减小的第二保护层 63。第二保护层 63 可以是由具有较差的台阶覆盖性的沉积法诸如等离子增强化学气相沉积 (PE-CVD) 形成的氮化物层。接下来，可以在第二保护层 63 上形成相对于第一保护层

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62 和第二保护层 63 具有高刻蚀选择性的第三保护层 64。第三保护层 64 可以是通过物理气相沉积 (PVD) 法形成的氮化钛 (TiN) 层。通过 PVD 法，可以形成第三保护层 64 以在层叠结构 ST 上具有悬垂形状，并且包括开口，第三狭缝 SL3A 经由此开口开放。

[0091] 参考图 19，可以去除形成在第三狭缝 SL3A 底面的第一保护层 62 以暴露第一牺牲层 54。可以暴露形成在第三狭缝 SL3A 的底面的、且未被第三保护层 64 覆盖的部分第一保护层 62。此外，由第三保护层 64 来保护形成在第三狭缝 SL3A 侧壁的部分第一保护层 62。因此，当执行刻蚀过程以去除第一保护层 62 时，可以去除未被第三保护层 64 覆盖的部分第一保护层 62。可以由第三保护层 64 来保护形成在第三狭缝 SL3A 侧壁和层叠结构 ST 上部的第一保护层 62 和第二保护层 63。结果，可以在第三狭缝 SL3A 的侧壁上形成具有间隔层 (spacer) 形状的第一保护层图案 62A。

[0092] 接下来，可以利用第一保护层图案 62A、第二保护层 63 和第三保护层 64 作为刻蚀阻挡层，通过刻蚀过程去除第一牺牲层 54，以便可以形成第二开口 OP2，且可以由第二开口 OP2 来暴露部分存储层 58。

[0093] 参考图 20，可以去除由第二开口 OP2 暴露的第一存储层 58 以暴露沟道层 59。

[0094] 例如，当第一存储层 58 包括沟道绝缘层、数据储存层和电荷阻挡层时，可以首先除去由第二开口 OP2 暴露的电荷阻挡层。可以部分地去除由第二开口 OP2 暴露的第二牺牲层 53。此外，可以去除第三保护层 64。接下来，可以去除由第二开口 OP2 暴露的数据储存层。也可以去除由第二开口 OP2 暴露的刻蚀阻挡层 EBL。另外，可以部分地去除第一保护层图案 62A 和第二保护层 63。因此，可以由邻近衬底 50 的第三狭缝 SL3A 的下部来暴露第三牺牲层 56 和第二绝缘层 57。可以部分地去除暴露的第三牺牲层 56。接下来，可以去除由第二开口 OP2 暴露的沟道绝缘层。可以去除由第二开口 OP2 暴露的第二牺牲层 53 以暴露第一源极层 52。另外，可以部分地去除由第三狭缝 SL3A 下部暴露的第二绝缘层 57 以在第三狭缝 SL3A 的下部形成非平坦性。

[0095] 参考图 21，可以形成电耦接至由第二开口 OP2 暴露的部分沟道层 59 的第二源极层 65。可以按照与以上参考图 16 描述的方式基本相同的方式来执行随后的过程。

[0096] 根据上述过程，可以通过结合各种沉积法来形成多个保护层 62 至 64，而且所述保护层被用作刻蚀阻挡物以刻蚀第一存储层 58。因此，可以选择性地去除第一存储层 58。此外，可以增加第三狭缝 SL3A 的下宽度。

[0097] 参考图 22 至图 25，图示了说明根据一个实施例的制造半导体器件的方法的、且显示了形成保护层的改进的例子的剖视图。在下文中，省略了上述已描述的实施例的通用内容的描述。

[0098] 在图 22 中，可以在衬底 70 之上形成第一绝缘层 71、第一源极层 72、第二牺牲层 73、第一牺牲层 74 和加固图案 75。可以在其上形成包括相互交替层叠的第三牺牲层 76 和第二绝缘层 77 的层叠结构 ST。在形成层叠结构 ST 之前，可以进一步形成刻蚀阻挡层 EBL。接下来，在形成第一存储层 78、沟道层 79 和间隙填充绝缘层 80 之后，可以形成第二狭缝 SL2 和隔离绝缘图案 81。

[0099] 可以穿过层叠结构 ST 和刻蚀阻挡层 EBL 形成第三狭缝 SL3A 以暴露第一牺牲层 74。可以在第三狭缝 SL3A 中形成保护层 82、84。例如，可以在第三狭缝 SL3A 和层叠结构 ST 的表面上形成具有均匀厚度的第一保护层 82。第一保护层 82 可以是由具有优良台阶覆

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盖性的沉积法诸如低压化学气相沉积 (LP-CVD) 形成的氮化物层。另外，第一保护层 82 与参考图 18 的上述第一保护层 62 相比可以具有较大厚度。接下来，可以在第一保护层 82 上形成相对于第一保护层 82 具有高刻蚀选择性的第二保护层 84。第二保护层 84 可以是通过物理气相沉积 (PVD) 法形成的氮化钛 (TiN) 层。通过 PVD 法，可以形成第二保护层 84 以在层叠结构 ST 上具有悬垂形状，并且包括开口，第三狭缝 SL3A 经由此开口开放。

[0100] 在图 23 中，可以去除形成在第三狭缝 SL3A 底面的第一保护层 82 以暴露第一牺牲层 74，以便可以在第三狭缝 SL3A 的侧壁上形成具有间隔层形状的第一保护层图案 82A。

[0101] 接下来，可以利用第一保护层图案 82A 和第二保护层 84 作为刻蚀阻挡物，通过刻蚀过程去除第一牺牲层 74，以便可以形成第二开口 OP2，且可以由第二开口 OP2 来暴露部分第一存储层 78。

[0102] 图 24 中，可以去除由第二开口 OP2 暴露的第一存储层 78 来暴露沟道层 79。

[0103] 例如，当第一存储层 78 包括沟道绝缘层、数据储存层和电荷阻挡层时，可以首先除去由第二开口 OP2 暴露的电荷阻挡层。此时，可以部分地去除由第二开口 OP2 暴露的第二牺牲层 73。此外，可以去除第二保护层 84。接下来，可以通过刻蚀过程去除由第二开口 OP2 暴露的数据储存层。也可以经由第二开口 OP2 去除部分刻蚀阻挡层 EBL。当刻蚀阻挡层 EBL 与数据储存层相比具有较大厚度时，当刻蚀数据储存层以暴露沟道绝缘层时，刻蚀阻挡层 EBL 可以不被完全去除而是保护离衬底 70 最近的第二绝缘层 77 的底层。

[0104] 另外，可以部分地去除第一保护层图案 82A。第一保护层图案 82A 可以如此厚以致于第一保护层图案 82A 可以以减少的厚度保留。因此，第三牺牲层 76 和第二绝缘层 77 可以不被第三狭缝 SL3A 暴露且由第一保护层图案 84A 来保护。接下来，可以去除由第二开口 OP2 暴露的沟道绝缘层。可以去除由第二开口 OP2 暴露的第二牺牲层 73 以暴露第一源极层 72。另外，当刻蚀沟道绝缘层时，剩余的刻蚀阻挡层 EBL 可以保护第二绝缘层 77 的底层。因此，可以保持第二绝缘层 77 的底层的厚度。在刻蚀沟道绝缘层以暴露沟道层 79 之后，可以经由第二开口 OP2 去除剩余的刻蚀阻挡层 EBL。

[0105] 图 25 中，可以形成电连接由第二开口 OP2 暴露的部分沟道层 79 的第二源极层 85。可以按照与以上参考图 16 描述的方式基本相同的方式来执行随后的过程。

[0106] 根据上述过程，可以通过结合各种沉积法来形成多层保护层 82 和 84，而且所述保护层被用作刻蚀阻挡物以形成第一存储层 78。因此，可以选择性地去除第一存储层 78。

[0107] 参考图 26 至图 28，图示了说明根据一个实施例制造半导体器件的方法的、且显示了形成第二源极层的改进的例子的剖视图。在下文中，省略了上述已描述的实施例的通用内容的描述。

[0108] 在图 26 中，可以在衬底 90 之上形成第一绝缘层 91、第一源极层 92 和层叠结构 ST。层叠结构 ST 包括相互交替层叠的第三牺牲层 96 和第二绝缘层 97。可以在第一源极层 92 和层叠结构 ST 之间形成加固图案 95。可以在加固图案 95 和层叠结构 ST 之间进一步形成刻蚀阻挡层 EBL。

[0109] 包括第一存储层 98、沟道层 99 和间隙填充绝缘层 100 的穿通结构可以穿过层叠结构 ST。穿通结构可以延伸至第一源极层 92。第二狭缝 SL2 可以穿过层叠结构 ST 的上部。第二狭缝 SL2 可以完全被隔离绝缘图案 101 填充。此外，隔离绝缘图案 101 可以延伸以覆盖层叠结构 ST 的顶面。第三狭缝 SL3A 可以穿过隔离绝缘图案 101 和层叠结构 ST。第三狭

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缝 SL3A 的侧壁可以由第一保护层图案 102A 来保护。

[0110] 第一保护层图案 102A 可以在隔离绝缘图案 101 的顶面上延伸。第三狭缝 SL3A 可以连接至第二开口 OP2。第二开口 OP2 可以配置在层叠结构 ST 和第一源极层 92 之间。第二开口 OP2 的形状可以由加固图案 95 保持。

[0111] 可以经由第二开口 OP2 去除刻蚀阻挡层 EBL，以便刻蚀阻挡层 EBL 仅保留在加固图案 95 上。可以经由第二开口 OP2 去除部分第一存储层 98。此外，可以由第二开口 OP2 暴露沟道层 99 的下部。

[0112] 可以通过依次执行参考图 22 至图 24 的上述过程来形成上述结构。形成上述结构之后，可以通过从由第二开口 OP2 暴露沟道层 99 和第一源极层 92 生长硅来形成第二源极层 103。通过控制第二源极层 103 被生长成的厚度，第二源极层 103 可以延伸至预定厚度并且可以不完全填充第二开口 OP2。可以在由第二开口 OP2 暴露的沟道层 99 和第一源极层 92 的暴露的表面上形成第二源极层 103，以便在第二源极层 103 的表面上形成凹部 CA。凹部 CA 的深度可以大于每个第三牺牲层 96 的厚度。

[0113] 参考图 27，可以通过去除第一保护层图案 102A 由第三狭缝 SL3A 暴露第三牺牲层 96。

[0114] 参考图 28，可以经由第三狭缝 SL3A 去除第三牺牲层 96，以便可以在第二绝缘层 97 之间形成第三开口 OP3。接下来，可以用导电材料填充第三开口 OP3。导电材料可以包括低电阻金属材料，诸如钨 (W)。在第三狭缝 SL3A 的侧壁上和第二源极层 103 的凹部 CA 表面形成所述导电材料。形成导电材料之前，可以进一步形成第二存储层 105 或阻挡层。阻挡层可以包括钛 (Ti)、氮化钛 (TiN)、钽 (Ta)、氮化钽 (TaN)、氮化钨 (WNx) 等。

[0115] 接下来，可以通过去除形成在第三狭缝 SL3A 侧壁上的导电材料来形成导电层 104。导电层 104 可以由第三狭缝 SL3A 分离并且填充第三开口 OP3。导电材料可以保留在凹部 CA 中，或可以从凹部 CA 完全去除，这取决于凹部 CA 的区域。例如，当凹部 CA 的深度大于第三牺牲层 96 的每个厚度和第三开口 OP3 的厚度时，凹部 CA 可以不完全由导电材料填充。另外，非常薄层的导电材料可以形成在凹部 CA 的表面。在这个例子中，通过执行刻蚀过程来去除导电材料，可以完全去除形成在凹部 CA 中的导电材料。即使当导电材料保留在凹部 CA 中时，剩余的导电材料也可以与填充第三开口 OP3 的导电层 104 分离。因此，剩余的导电材料可以不影响驱动。

[0116] 接下来，可以在第三狭缝 SL3A 中形成狭缝绝缘层 106。狭缝绝缘层 106 可以包括氧化物。狭缝绝缘层 106 可以延伸至第二源极层 103 的凹部 CA。凹部 CA 可以完全由狭缝绝缘层 106 填充，或者包括参考图 7 描述的间隙。

[0117] 参考图 29 至图 31，图示了说明根据一个实施例的半导体器件的制造方法且显示了形成狭缝绝缘层的改进例子的剖视图。在下文中，省略了上述已描述的实施例的通用内容的描述。

[0118] 在图 29 中，可以在衬底 110 之上形成第一绝缘层 111、第一源极层 112 和层叠结构 ST。层叠结构 ST 包括相互交替层叠的第二绝缘层 117 和导电层 119。可以在第一源极层 112 和层叠结构 ST 之间形成加固图案 115。可以在加固图案 115 上形成刻蚀阻挡层 EBL。可以由加固图案 115 来保持层叠结构 ST 和第一源极层 112 之间的间隙。

[0119] 包括第一存储层 118、沟道层 119 和间隙填充绝缘层 120 的穿通结构可以穿过层

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叠结构 ST。穿通结构可以延伸至第一源极层 112。第一存储层 118 可以划分为保留在第一源极层 112 和沟道层 119 之间的第一部分和保留在层叠结构 ST 和沟道层 119 之间的第二部分。当插入由加固图案 115 保持的间隙时，第一部分和第二部分可以相互分离。沟道层 119 的下部可以暴露在第一部分和第二部分之间。

[0120] 第二狭缝 SL2 可以穿过层叠结构 ST 的上部。隔离绝缘图案 121 可以完全填充第二狭缝 SL2。此外，隔离绝缘图案 121 可以延伸以覆盖层叠结构 ST 的顶面。第三狭缝 SL3A 可以穿过隔离绝缘图案 121 和层叠结构 ST。

[0121] 可以在每个沟道层 119 的下部表面上形成第二源极层 113，所述沟道层 119 暴露在第一存储层 118 的第一部分和第二部分与第一源极层 112 表面之间。在第二源极层 113 的表面形成凹部 CA。

[0122] 第二存储层 125 可以围绕导电层 124。第二存储层 125 可以从导电层 124 的表面延伸至第三狭缝 SL3A 的侧壁。第二存储层 125 可以从第三狭缝 SL3A 的侧壁延伸至第二源极层 113 的凹部 CA 的表面。第二存储层 125 可以从第三狭缝 SL3A 的侧壁延伸至隔离绝缘图案 121 的顶部。

[0123] 可以利用以上参考图 26 至图 28 的上述过程形成上述结构。在形成上述结构之后，可以在第三狭缝 SL3A 的表面和凹部 CA 的表面上形成狭缝绝缘层 126。根据一个实施例，狭缝绝缘层 126 相比以上参考图 28 的所述狭缝绝缘层可以具有较小厚度，以便可以开放第三狭缝 SL3A 的中心部。换句话说，第三狭缝 SL3A 可以不完全由狭缝绝缘层 126 来填充并且具有开放的中心部。

[0124] 接下来，可以在狭缝绝缘层 126 上形成相对于狭缝绝缘层 126 具有高刻蚀选择性的保护层 128。保护层 128 可以包括通过物理气相沉积 (PVD) 法形成的氮化钛 (TiN) 层。通过 PVD 法，可以形成保护层 128 以具有悬垂结构。保护层 128 还可以包括开口，第三狭缝 SL3A 经由此开口而开放。

[0125] 参考图 30，可以去除形成在第三狭缝 SL3A 底面的部分狭缝绝缘层 126 和部分第二存储层 125 以暴露第二源极层 113。可以去除未被保护层 128 覆盖且暴露在第三狭缝 SL3A 底面的部分狭缝绝缘层 126 和部分第二存储层 125。形成在第三狭缝 SL3A 侧壁和隔离绝缘图案 121 顶部上的狭缝绝缘层 126 和第二存储层 125 可以由保护层 128 来保护。因此，可以在第三狭缝 SL3A 的侧壁上形成具有间隔层形状的狭缝绝缘层 126A。狭缝绝缘层 126A 可以保留在层叠结构 ST 之下。另外，第二存储层 125 可以由第二存储层图案 125A 分离。

[0126] 参考图 31，可以去除保护层 128。接下来，第三狭缝 SL3A 开放的中心部可以由导电材料诸如金属来填充。此外，可以通过平坦化处理、诸如化学机械抛光 (CMP) 处理使导电材料的表面平坦化。可以执行平坦化处理直至暴露狭缝绝缘层图案 126A。结果，可以在第三狭缝 SL3A 中形成接触第二源极层 113 的共源极线 129。第二存储层图案 125A 可以由共源极线 129 分离。另外，狭缝绝缘图案 126A 也可以由共源极线 129 分离。

[0127] 参考图 32 和图 33，图示了说明根据一个实施例的半导体器件的制造方法且显示了形成刻蚀阻挡层和加固图案的过程的改进例子的剖面图。在下文中，省略了上述已描述的实施例的通用内容的描述。

[0128] 在图 32 中，可以在衬底 130 上形成第一绝缘层 131。此外，可以在第一绝缘层 131 上形成第一源极层 132。第一源极层 132 可以包括导电层，上述导电层包括掺杂多晶硅层、

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金属层等。

[0129] 接下来，可以在第一源极层 132 上形成第一牺牲层 134。在形成第一牺牲层 134 之前，可以进一步形成第二牺牲层 133。第一牺牲层 134 可以包括相对于第二牺牲层 133 具有高刻蚀选择性的材料。例如，第一牺牲层 134 可以包括无掺杂多晶硅层、掺杂多晶硅层等，第二牺牲层 133 可以包括氧化物或氮化物。

[0130] 可以在第一牺牲层 134 上形成刻蚀阻挡层 EBL。刻蚀阻挡层 EBL 可以包括相对于以下将描述的第二绝缘层 137 具有高刻蚀选择性的材料，以便保护第二绝缘层 137。例如，刻蚀阻挡层 EBL 可以包括氮化物。刻蚀阻挡层 EBL 可以具有与第一存储层 138 的数据储存层相比较大的厚度。例如，刻蚀阻挡层 EBL 可以是数据储存层厚度的 2.5 倍。

[0131] 接下来，第一狭缝 SL1A 可以穿过第一牺牲层 34 和刻蚀阻挡层 EBL 而形成。可以在第一狭缝 SL1A 中形成加固图案 135。第一狭缝 SL1A 可以足够深以穿过第一牺牲层 134 和刻蚀阻挡层 EBL 而暴露第二牺牲层 133、第一源极层 132 或第一绝缘层 131。为了形成加固图案 135，可以以依序方式来执行用加固层填充第一狭缝 SL1A 的过程以及使加固层平坦化直至暴露刻蚀阻挡层 EBL 的过程。加固图案 135 可以是绝缘层。当刻蚀阻挡层 EBL 具有相对于加固层的刻蚀选择性时，刻蚀阻挡层 EBL 可以在加固层的平坦化处理期间发挥平坦化截止层的作用。加固层可以包括相对于刻蚀阻挡层 EBL 具有高刻蚀选择性的氧化物。

[0132] 接下来，可以在加固图案 135 穿过的刻蚀阻挡层 EBL 之上形成层叠结构 ST。如以上参考图 10A 和图 10B 的描述，层叠结构 ST 可以包括相互交替层叠的第三牺牲层 136 和第二绝缘层 137。

[0133] 接下来，第一开口 OP1 可以穿过层叠结构 ST、刻蚀阻挡层 EBL 和第一牺牲层 134 而形成。可以利用如以上参考图 10A 和图 10B 所述的基本上相同的过程来形成第一开口 OP1。

[0134] 接下来，通过执行以上参考图 10A 和 10B 的过程，可以在第一开口 OP1 中形成第一存储层 138、沟道层 139 和间隙填充绝缘层 140。如以上参考图 17A 的描述，每个第一存储层 138 可以包括沟道绝缘层、数据储存层和电荷阻挡层。

[0135] 在图 33 中，可以利用以上参考图 11A 和图 11B 的过程来形成第二狭缝 SL2 和隔离绝缘层 141。接下来，通过利用以上参考图 12A 和图 12B 的所述过程，第三狭缝 SL3A 可以穿过层叠结构 ST 而形成。接下来，可以通过经由第三狭缝 SL3A 去除如图 32 所示的第一牺牲层 134 来形成第二开口 OP2。

[0136] 接下来，可以在第三狭缝 SL3A 的侧壁上形成保护层 142。可以利用以上参考图 13 的所述过程、以上参考图 18 和图 19 的所述过程或以上参考图 22 至图 24 的所述过程来形成保护层 142。

[0137] 在形成保护层 142 之后，可以通过利用以上参考图 17A 至 17D 的所述过程来去除由第二开口 OP2 暴露的每个第一存储层 138 的一部分以暴露沟道层 139。如图 32 所示的刻蚀阻挡层 EBL 可以保留来避免层叠结构 ST 的底部第二绝缘层 137 的厚度损失。在暴露沟道层 139 之后，可以去除如图 32 所示的刻蚀阻挡层 EBL。

[0138] 接下来，可以以依序方式执行形成第二源极层的过程、形成第二存储层的过程、形成导电层的过程、去除保护层 142 的过程以及形成狭缝绝缘层的过程。可以根据上述实施例中的一个来执行这些过程。

[0139] 例如，可以利用以上参考图 15 和图 16 的上述过程来执行形成第二源极层的过程、

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形成第二存储层的过程、形成导电层的过程、去除保护层 142 的过程以及形成狭缝绝缘层的过程。

[0140] 在一个例子中，可以利用以上参考图 21 的上述过程来执行形成第二源极层的过程、形成第二存储层的过程、形成导电层的过程、去除保护层 142 的过程以及形成狭缝绝缘层的过程。

[0141] 在一个例子中，可以利用以上参考图 25 的上述过程来执行形成第二源极层的过程、形成第二存储层的过程、形成导电层的过程、去除保护层 142 的过程以及形成狭缝绝缘层的过程。

[0142] 在一个例子中，可以利用以上参考图 26 至图 28 的上述过程来执行形成第二源极层的过程、形成第二存储层的过程、形成导电层的过程、去除保护层 142 的过程以及形成狭缝绝缘层的过程。

[0143] 在一个例子中，可以利用以上参考图 29 至图 31 的上述过程来执行形成第二源极层的过程、形成第二存储层的过程、形成导电层的过程、去除保护层 142 的过程以及形成狭缝绝缘层的过程。在这个例子中，在去除保护层 142 之后，可以进一步执行以上参考图 31 的所述形成共源极线的过程。

[0144] 参考图 34，图示了说明根据一个实施例的存储器系统的配置的框图。

[0145] 如图 34 所示，根据一个实施例的存储器系统 1000 可以包括存储器件 1200 和控制器 1100。

[0146] 存储器件 1200 可以用作储存各种类型的数据，诸如文本、图像和软件代码。存储器件 1200 可以是非易失性存储器并且包括图 1 至图 33 所示的所述结构。存储器件 1200 可以包括定义了单元区和位于单元区两侧的接触区的衬底。存储器 1200 还可以包括第一源极层，形成在衬底之上；第二源极层，形成在第一源极层之上；加固图案，形成在第二源极层中；层叠结构，包括在第二源极层和加固图案之上相互交替层叠的导电层和绝缘层；沟道层，穿过层叠结构和第二源极层且电耦接至源极层；以及隔离绝缘图案，穿过至少一个顶部导电层。由于存储器件 1200 以上述方式配置和制造，因此将省略详细描述。

[0147] 控制器 1100 可以电耦接至主机和存储器件 1200。控制器 1100 可以响应于主机的请求而访问存储器件 1200。例如，控制器 1100 可以控制存储器件 1200 的读取、写入、擦除和后台操作。

[0148] 控制器 1100 可以包括随机存取存储器 (RAM) 1110、中央处理单元 (CPU) 1120、主机接口 1130、错误校正码 (ECC) 电路 1140 和存储器接口 1150。

[0149] RAM 1110 可以用作 CPU 1120 的操作存储器、存储器件 1200 与主机之间的高速缓冲存储器、以及存储器件 1200 与主机之间的缓冲存储器。RAM 1110 可以由静态随机存取存储器 (SRAM) 或只读存储器 (RAM) 替代。

[0150] CPU 1120 可以配置成用于控制控制器 1100 的整体操作。例如，CPU 1120 可以配置成操作固件、诸如存储在 RAM 1110 中的闪存转换层 (FTL)。

[0151] 主机接口 1130 可以与主机连接。例如，控制器 1100 可以通过各种接口协议与主机通信，上述各种接口协议包括通用串行总线 (USB) 协议、多媒体卡 (MMC) 协议、外设组件互连 (PCI) 协议、PCI-express(PCI-E) 协议、高级技术附件 (ATA) 协议、串行 ATA 协议、并行 ATA 协议、小型计算机系统接口 (SCSI) 协议、增强小型磁盘接口 (ESDI) 协议、集成驱动

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电路（IDE）协议、私有协议、或它们的组合等

[0152] ECC 电路 1140 可以利用错误校正码（ECCs）检测和校正从存储器件 1200 读取的数据中所包含的错误。

[0153] 存储器接口 1150 可以与存储器件 1200 连接。例如，存储器接口 1150 可以包括 NAND 接口或 NOR 接口。

[0154] 例如，控制器 1100 还可以包括配置为暂时储存数据的缓冲存储器。所述缓冲存储器可以暂时储存通过主机接口 1130 从外部传输的数据。在可替选方案中，缓冲存储器可以暂时储存通过存储器接口 1150 从存储器件 1200 传输的数据。控制器 1100 还可以包括储存代码数据以与主机连接的只读存储器（ROM）。

[0155] 由于根据一个实施例的存储器系统 1000 包括考虑到容易制造且具有改善的特性的存储器件 1200，因此存储器系统 1000 的特性也可以得到改善。

[0156] 参考图 35，图示了说明根据一个实施例的存储系统的结构的框图。在下文中，省略了上述组件的重复性描述。

[0157] 如图 35 所示，根据一个实施例的存储系统 1000’可以包括存储器件 1200’和控制器 1100。控制器 1100 可以包括 RAM 1110、CPU 1120、主机接口 1130、ECC 电路 1140 和存储器接口 1150 等。

[0158] 存储器件 1200’可以是非易失性存储器。存储器件 1200’可以包括以上如图 1 至图 31 所述的存储串。另外，存储器件 1200’可以包括：单元区；衬底，定义了单元区和位于单元区两侧的接触区；第一源极层，形成在衬底之上；第二源极层，形成在第一源极层之上；加固图案，形成在第二源极层中；层叠结构，包括在第二源极层和加固图案之上相互交替层叠的导电层和绝缘层；沟道层，穿过层叠体和第二源极层且电耦接至第二源极层；以及隔离绝缘图案，穿过至少一个顶部导电层。由于存储器件 1200’以与存储器件 1200 相同的方式配置和制造，因此将省略其详细描述。

[0159] 存储器件 1200’可以是由多个存储芯片组成的多芯片封装体。所述多个存储芯片被划分为多个组。所述多个组可以通过第一至第 k 信道 CH1 至 CHk 与控制器 1100 通信。另外，包括在一个组中的存储芯片可以适用于通过公共信道与控制器 1100 通信。存储系统 1000’可改变成使得一个存储芯片可以电耦接至单个信道。

[0160] 如上所述，根据一个实施例，由于存储系统 1000’包括存储器件 1200’，所述存储器件 1200’具有改善的集成度、容易制造、且具有改善的特性，因此，存储系统 1000’的集成度和特性也可以得到改善。另外，由于存储器件 1200’可以利用多芯片封装体而形成，因此存储系统 1000’的数据存储容量和驱动速度可以进一步提高。

[0161] 参考图 36，图示了说明根据一个实施例的计算系统的结构的框图。在下文中，省略了上述组件的重复性描述。

[0162] 如图 36 所示，根据一个实施例的计算系统 2000 可以包括存储器件 2100、CPU 2200、随机存取存储器（RAM）2300、用户接口 2400、电源 2500 和系统总线 2600。

[0163] 存储器件 2100 可以储存经由用户接口 2400 输入的数据以及由 CPU 2200 处理的数据。存储器件 2100 可以电耦接至 CPU 2200、RAM 2300、用户接口 2400 和电源 2500。例如，存储器件 2100 可以通过控制器电耦接至系统总线 2600，或直接电耦接至系统总线 2600。当存储器件 2100 直接电耦接至系统总线 2600 时，控制器的功能可以由 CPU 2200 和 RAM 2300

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来执行。

[0164] 存储器件 2100 可以是非易失性存储器。存储器 2100 可以包括以上参考图 1 至图 33 的所述存储串。存储器件 2100 可以包括：衬底，其上定义了单元区和位于单元区两侧的接触区；第一源极层，形成在衬底之上；第二源极层，形成在第一源极层之上；加固图案，形成在第二源极层中；层叠体，包括在第二源极层和加固图案之上相互交替层叠的导电层和绝缘层；沟道层，穿过层叠结构和第二源极层、且电耦接至第二源极层；以及隔离绝缘图案，穿过至少一个顶部导电层。由于存储器件 2100 以与存储器件 1200 或 1200' 相同的方式配置和制造，因此将省略其详细描述。

[0165] 另外，如以上参考图 35 所述，存储器件 2100 可以是由多个存储芯片组成的多芯片封装体。

[0166] 具有上述结构的计算系统 2000 可以是诸如计算机、超级移动 PC(UMPC)、工作站、上网本、个人数字助理 (PDAs)、便携式计算机、网络本、无线电话、移动电话、智能电话、电子书、便携式多媒体播放器 (PMP)、便携式游戏机、导航仪、黑匣子、数字照相机、三维 (3D) 电视、数字录音机、数字音频播放器、数字图像记录仪、数字图像播放器、数字录像机、数字视频播放器、无线环境中的信息收发设备等电子设备的各种组件中的一种、用于家庭网络的各种电子设备中的一种、用于计算机网络的各种电子设备中的一种、用于远程信息处理网络中的各种电子设备中的一种、RFID 设备、和 / 或用于计算系统的各种设备中的一种等等。

[0167] 如上所述，由于根据一个实施例的计算系统 2000 包括具有改善的集成度、容易制造以及具有改善的特性的存储器件 2100，因此计算系统 2000 的数据存储容量和特性可以得到改善。

[0168] 参考图 37，描述了示出根据一个实施例的计算系统的框图。

[0169] 如图 37 所示，根据一个实施例的计算系统 3000 可以包括具有操作系统 3200、应用程序 3100、文件系统 3300 和转换层 3400 的软件层。计算系统 3000 可以包括诸如存储器件 3500 的硬件层。

[0170] 操作系统 3200 可以管理计算系统 3000 的软件、硬件资源。操作系统 3200 可以控制中央处理单元的程序运行。应用程序 3100 可以包括由计算系统 3000 运行的各种应用程序。应用程序 3100 可以是由操作系统 3200 运行的实用程序。

[0171] 文件系统 3300 可以表示逻辑结构，所述逻辑结构配置为管理存在于计算系统 3000 中的数据、文件。文件系统 3300 可以整理文件和数据，且根据给定规则将他们储存在存储器件 3500 中。文件系统 3300 可以基于计算系统 3000 中所使用的操作系统 3200 来确定。例如，当操作系统 3200 是基于 Microsoft Windows 的系统时，文件系统 3300 可以是文件分配表 (FAT) 或 NT 文件系统 (NTFS)。另外，当操作系统 3200 是基于 Unix/Linux 的系统时，文件系统 3300 可以是扩展文件系统 (EXT)、Unix 文件系统 (UFS) 或日志文件系统 (JFS)。

[0172] 参考图 37，操作系统 3200、应用程序 3100 和文件系统 3300 用单独的模块来描述。然而，应用程序 3100 和文件系统 3300 可以包括在操作系统 3200 中。

[0173] 转换层 3400 可以响应于文件系统 3300 的请求来转换适合存储器件 3500 的地址。例如，转换层 3400 可以将由文件系统 3300 产生的逻辑地址转换为存储器件 3500 的物理地址。逻辑地址和物理地址的映射信息可以储存在地址转换表中。例如，转换层 3400 可以是

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闪存转换层 (FTL)、通用快闪存储链路层 (ULL) 等。

[0174] 存储器件 3500 可以是非易失性存储器，且可以包括以上参考图 1 至图 33 的所述存储串。存储器件 3500 可以包括：衬底，其上定义了单元区和位于单元区两侧的接触区；第一源极层，形成在衬底之上；第二源极层，形成在第一源极层之上；加固图案，形成在第二源极层中；层叠体，包括在第二源极层和加固图案之上相互交替层叠的导电层和绝缘层；沟道层，穿过层叠结构和第二源极层且电耦接至第二源极层；以及隔离绝缘图案，穿过至少一个顶部导电层。由于存储器件 3500 以与存储器件 1200、1200' 或 2100 相同的方式配置和制造，因此将省略其详细描述。

[0175] 具有上述结构的计算系统 3000 可以分为在上层区域中执行的操作系统层和在下层区域中执行的控制器层。应用程序 3100、操作系统 3200 和文件系统 3300 可以包括在操作系统层中，且由操作存储器来驱动。转换层 3400 可以包括在操作系统层或控制器层中。

[0176] 如上所述，由于根据一个实施例的计算系统 3000 包括具有改善的集成度、容易制造以及具有改善的特性的存储器件 3500，因此，进而计算系统 3000 的数据存储容量和特性可以得到改善。

[0177] 根据一个实施例，半导体器件可以包括形成在源极层上的加固图案。因此，在制造半导体器件过程期间，可以增加结构稳定性，改善制造产量。另外，可以利用保护层容易地形成电耦接至沟道层的源极层。

[0178] 通过以上实施例可以看出，本申请提供了以下的技术方案。

[0179] 技术方案 1. 一种半导体器件，包括：

[0180] 衬底，在所述衬底中定义了单元区和位于所述单元区两侧的接触区；

[0181] 第一源极层，形成在所述衬底之上；

[0182] 第二源极层，形成在所述第一源极层之上；

[0183] 加固图案，形成在所述第二源极层中；

[0184] 层叠结构，包括在所述第二源极层和所述加固图案之上交替地层叠的导电层和绝缘层；

[0185] 沟道层，穿过所述层叠结构和所述第二源极层且电耦接至所述第二源极层；以及

[0186] 隔离绝缘图案，穿过所述导电层的至少一个顶部导电层。

[0187] 技术方案 2. 如权利要求 1 所述的半导体器件，其中，所述隔离绝缘图案位于所述加固图案之上且与所述加固图案重叠。

[0188] 技术方案 3. 如权利要求 1 所述的半导体器件，其中，所述加固图案包括位于所述单元区和所述接触区的边界的线形图案。

[0189] 技术方案 4. 如权利要求 1 所述的半导体器件，其中，所述加固图案包括位于所述单元区或所述接触区中的线形图案。

[0190] 技术方案 5. 如权利要求 4 所述的半导体器件，其中，所述隔离绝缘图案与位于所述单元区中的所述线形图案重叠。

[0191] 技术方案 6. 如权利要求 1 所述的半导体器件，其中，所述加固图案包括与相邻存储块之间的边界邻近的岛形图案。

[0192] 技术方案 7. 如权利要求 1 所述的半导体器件，其中，所述加固图案包括绝缘材料。

[0193] 技术方案 8. 如权利要求 1 所述的半导体器件，还包括：

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[0194] 狭缝绝缘层，所述狭缝绝缘层穿过所述层叠结构而与所述第二源极层接触，并且不与所述加固图案重叠。

[0195] 技术方案 9. 如权利要求 1 所述的半导体器件，还包括：插入至所述沟道层与所述层叠结构之间的存储层。

[0196] 技术方案 10. 如权利要求 1 所述的半导体器件，其中，在所述沟道层的表面和所述第一源极层的表面上形成所述第二源极层以在所述第二源极层的表面定义凹部。

[0197] 技术方案 11. 如权利要求 10 所述的半导体器件，还包括：填充所述第二源极层的所述凹部的狭缝绝缘层。

[0198] 技术方案 12. 如权利要求 11 所述的半导体器件，还包括：形成在所述狭缝绝缘层中的间隙。

[0199] 技术方案 13. 如权利要求 1 所述的半导体器件，还包括：

[0200] 狭缝，穿过所述层叠结构；

[0201] 狭缝绝缘层，形成在所述狭缝的侧壁上，其中，所述狭缝的中心部由所述狭缝绝缘层开放；以及

[0202] 共源极线，填充所述狭缝的所述中心部且与所述第二源极层接触。

[0203] 技术方案 14. 如权利要求 1 所述的半导体器件，还包括：

[0204] 数据储存层，布置在每个沟道层与所述层叠结构之间；以及

[0205] 刻蚀阻挡层，形成在所述加固图案与所述层叠结构之间。

[0206] 技术方案 15. 如权利要求 14 所述的半导体器件，其中，所述刻蚀阻挡层具有比所述数据储存层厚的厚度。

[0207] 技术方案 16. 一种制造半导体器件的方法，所述方法包括：

[0208] 形成第一牺牲层；

[0209] 形成包括交替地层叠在所述第一牺牲之上的第二牺牲层和绝缘层的层叠结构；

[0210] 形成穿过所述层叠结构和所述第一牺牲层的沟道层、以及围绕所述沟道层的存储层；

[0211] 形成穿过所述层叠结构的狭缝；

[0212] 在所述狭缝的内壁上形成保护层；

[0213] 利用所述保护层作为刻蚀阻挡物来去除所述第一牺牲层，据此形成暴露所述存储层的开口；

[0214] 去除由所述开口暴露的存储层；以及

[0215] 在所述开口中形成与所述沟道层接触的源极层。

[0216] 技术方案 17. 如权利要求 16 所述的方法，还包括：

[0217] 当去除所述存储层时，通过部分地去除未被形成在所述狭缝的侧壁上部的保护层覆盖的绝缘层而在狭缝的下部形成非平坦结构。

[0218] 技术方案 18. 如权利要求 16 所述的方法，其中，形成所述保护层包括：形成锥形的保护层以使所述保护层的厚度从所述狭缝的顶部至底部逐渐减小。

[0219] 技术方案 19. 如权利要求 16 所述的方法，其中，形成所述保护层包括：

[0220] 在去除所述第一牺牲层之前，在所述狭缝中形成具有均匀厚度的第一保护层；

[0221] 在所述第一保护层之上形成第二保护层，其中，所述第二保护层包括相对于所述

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第一保护层具有刻蚀选择性的材料并且具有悬垂形状；以及

[0222] 去除形成在所述狭缝的底面的所述第一保护层来暴露所述第一牺牲层。

[0223] 技术方案 20. 如权利要求 19 所述的方法，其中，所述第一保护层包括利用低压化学气相沉积 LP-CVD 法形成的氮化物层，所述第二保护层包括利用物理气相沉积 PVD 法形成的氮化钛层。

[0224] 技术方案 21. 如权利要求 19 所述的方法，还包括：

[0225] 在形成所述第二保护层之前，在所述第一保护层之上形成第三保护层，其中，所述第三保护层呈锥形，以使所述第三保护层的厚度从所述狭缝的顶部至底部逐渐减小。

[0226] 技术方案 22. 如权利要求 21 所述的方法，其中，所述第三保护层包括利用等离子体增强化学气相沉积 PE-CVD 法形成的氮化物层。

[0227] 技术方案 23. 如权利要求 16 所述的方法，还包括：在所述第一牺牲层中形成加固图案。

[0228] 技术方案 24. 如权利要求 16 所述的方法，还包括：穿过所述第二牺牲层的至少一个顶部第二牺牲层的隔离绝缘图案。

[0229] 技术方案 25. 一种制造半导体器件的方法，所述方法包括：

[0230] 形成牺牲层；

[0231] 在所述牺牲层中形成加固图案；

[0232] 在所述牺牲层和所述加固图案之上形成层叠结构；

[0233] 形成穿过所述层叠结构和所述牺牲层的沟道层；

[0234] 形成穿过所述层叠结构且暴露所述牺牲层的狭缝；

[0235] 经由所述狭缝去除所述牺牲层来形成开口，其中，所述开口由所述加固图案支撑；以及

[0236] 形成源极层且在所述开口中与所述沟道层接触。

[0237] 技术方案 26. 如权利要求 25 所述的方法，还包括：

[0238] 形成穿过所述层叠结构上部且与所述加固图案重叠的隔离绝缘图案。

[0239] 技术方案 27. 如权利要求 25 所述的方法，其中，所述牺牲层形成在另一源极层之上，所述源极层与所述另一源极层接触。

[0240] 技术方案 28. 如权利要求 27 所述的方法，其中，形成所述源极层包括：从所述沟道层和所述另一源极层选择性地生长所述源极层。

[0241] 技术方案 29. 如权利要求 28 所述的方法，其中，所述源极层形成在所述沟道层的表面和所述另一源极层的表面，以便在所述源极层的表面定义凹部。

[0242] 技术方案 30. 如权利要求 29 所述的方法，还包括：

[0243] 在形成所述源极层之后，在所述狭缝和所述源极层的所述凹部中形成狭缝绝缘层。

[0244] 技术方案 31. 如权利要求 30 所述的方法，其中，在布置于所述凹部中的所述狭缝绝缘层中形成间隙。

[0245] 技术方案 32. 如权利要求 30 所述的方法，其中，在所述狭缝的侧壁和所述凹部的表面上形成所述狭缝绝缘层来开放所述狭缝的中心部。

[0246] 技术方案 33. 如权利要求 32 所述的方法，还包括：

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[0247] 在开放所述狭缝的所述中心部的所述狭缝绝缘层之上形成保护层；

[0248] 利用所述保护层作为刻蚀阻挡物来刻蚀所述狭缝绝缘层的底面来暴露所述源极层；

[0249] 去除所述保护层；以及

[0250] 形成填充所述狭缝的所述中心部且与所述源极层接触的共源极线。

[0251] 技术方案 34. 如权利要求 33 所述的方法，其中，所述保护层包括相对于所述狭缝绝缘层具有刻蚀选择性的材料，并且具有悬垂结构。

[0252] 技术方案 35. 如权利要求 25 所述的方法，其中，每个沟道层被包括数据储存层的存储层围绕，

[0253] 在形成所述牺牲层与形成所述加固图案之间或者在形成加固图案与形成所述层叠结构之间，还包括形成具有比所述数据储存层厚的厚度的刻蚀阻挡层，以及

[0254] 在经由开口去除存储层的一部分之后、在形成所述源极层之前，还包括去除所述刻蚀阻挡层。

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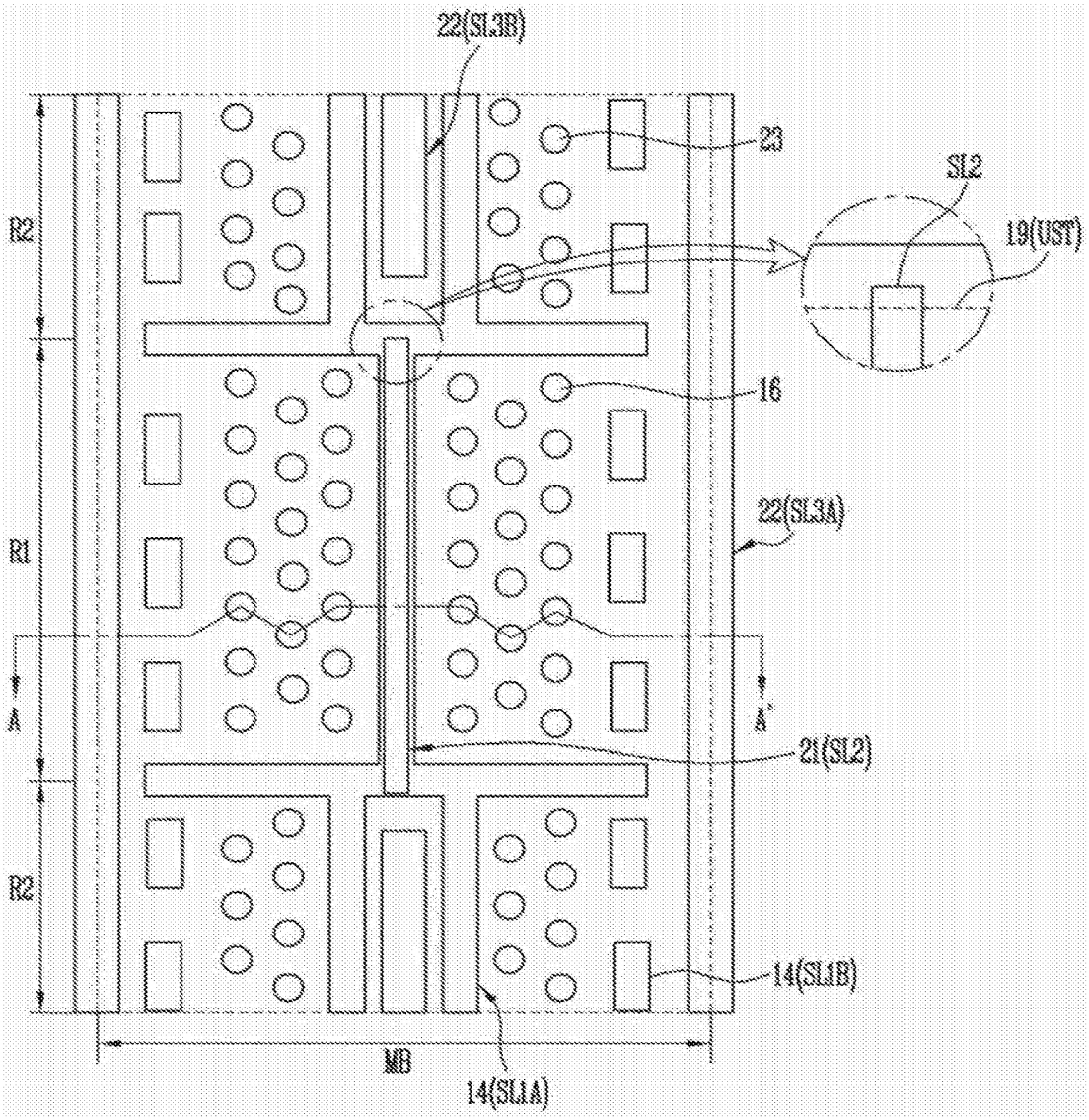


图 1

Micron Ex. 1002, p. 136
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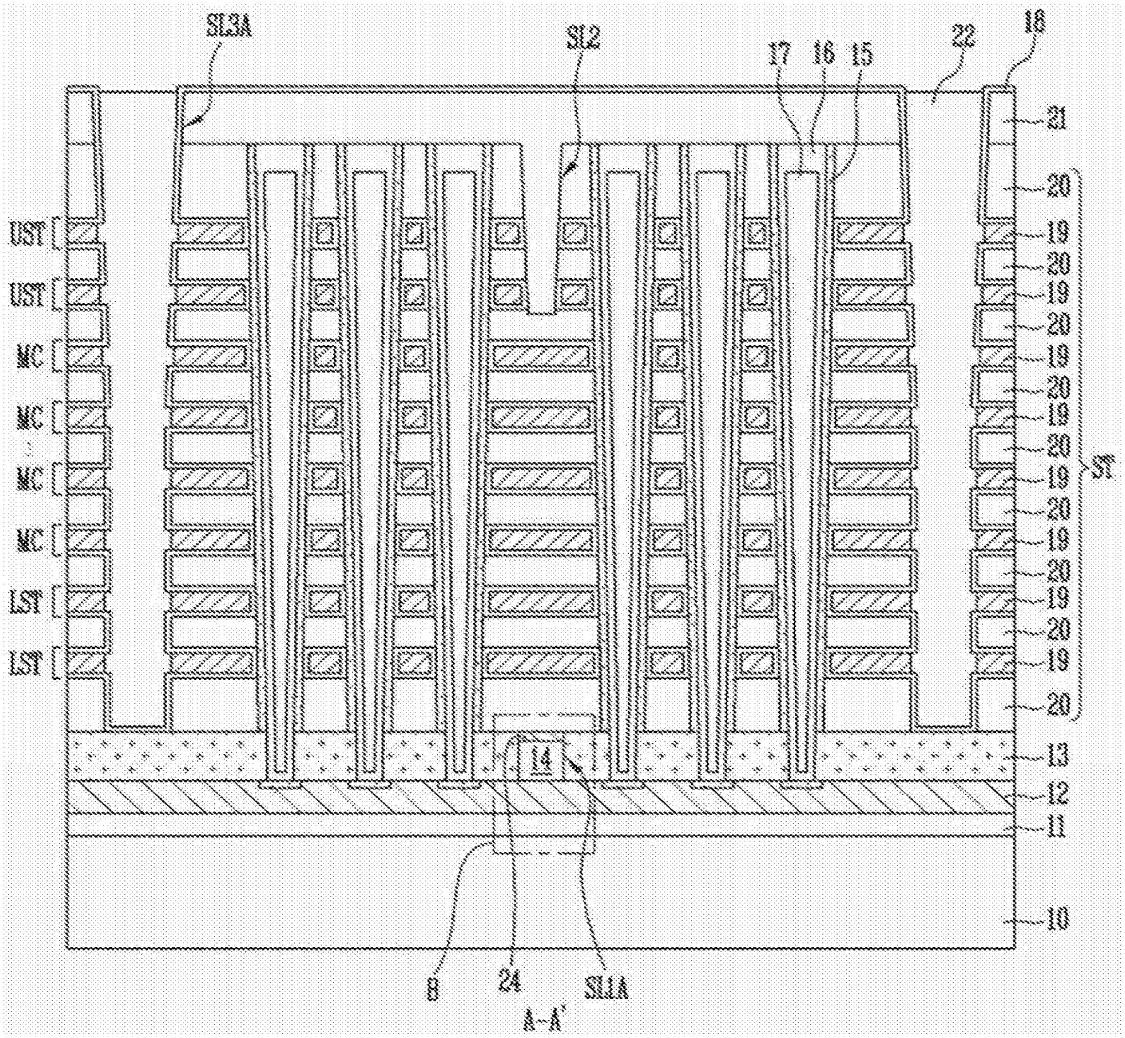


图 2

Micron Ex. 1002, p. 137
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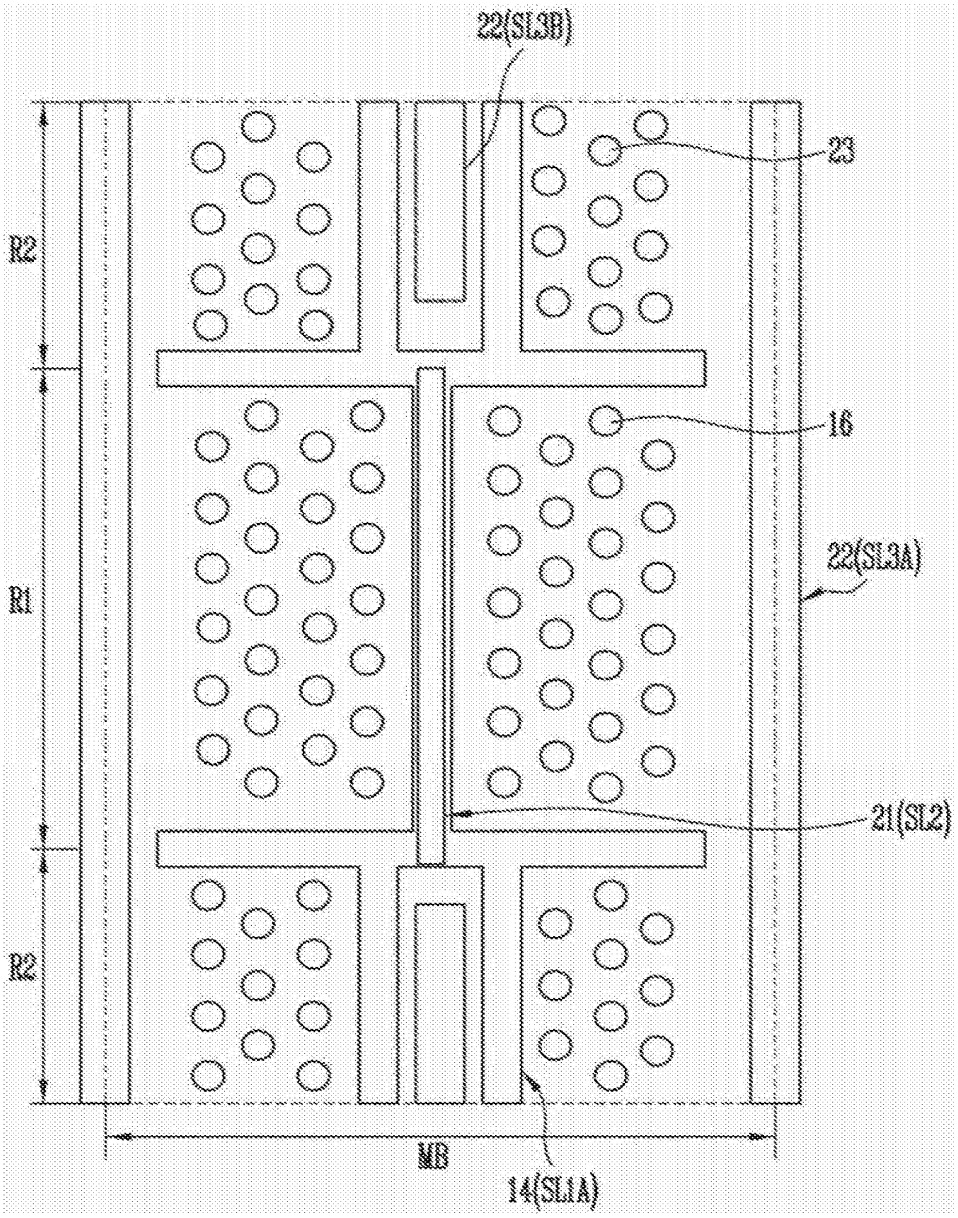


图 3

Micron Ex. 1002, p. 138
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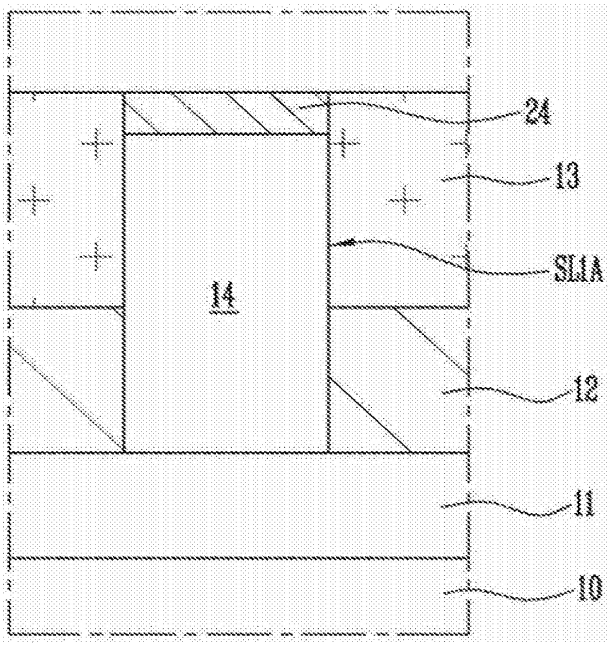


图 4

Micron Ex. 1002, p. 139
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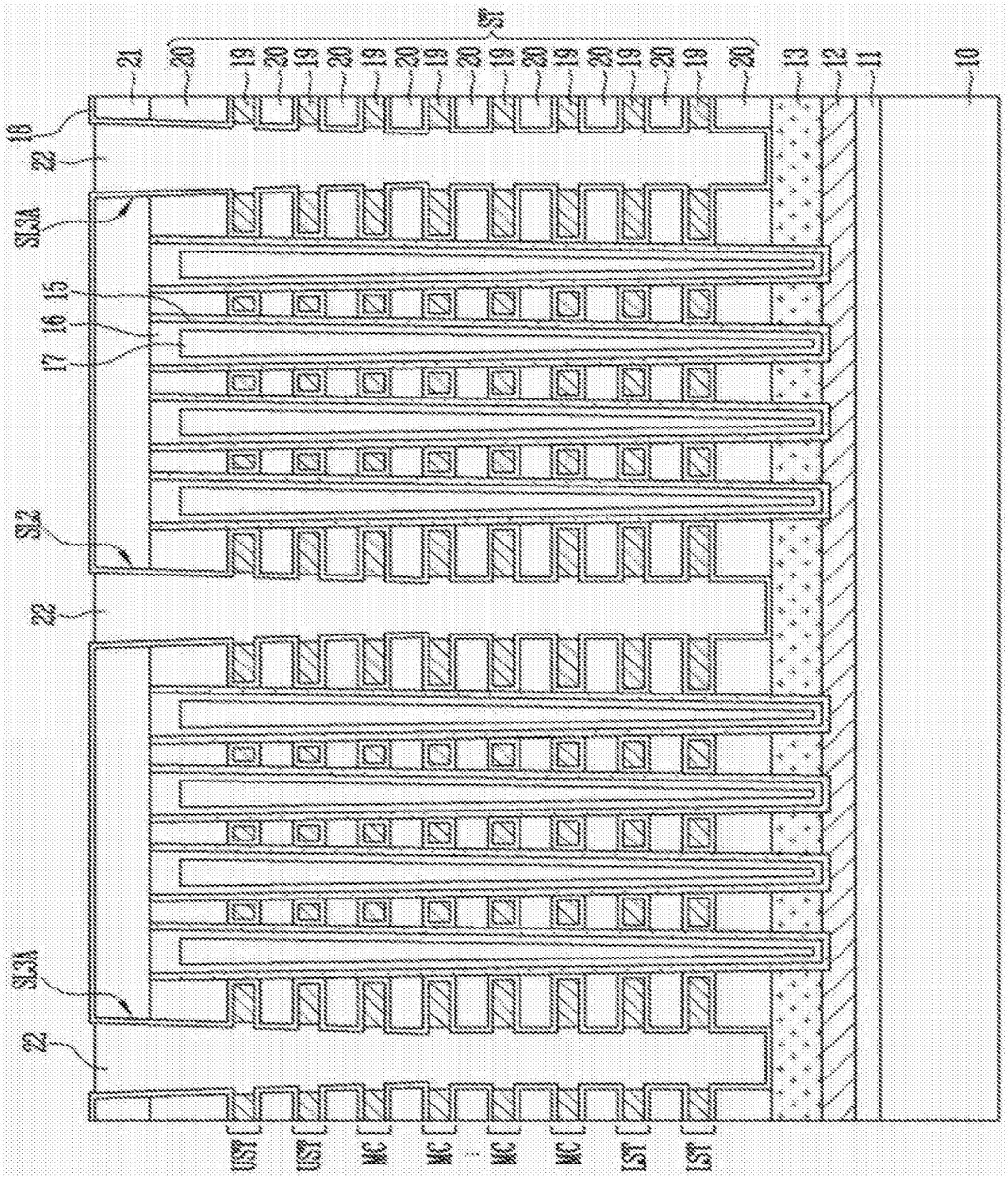


图 5

Micron Ex. 1002, p. 140
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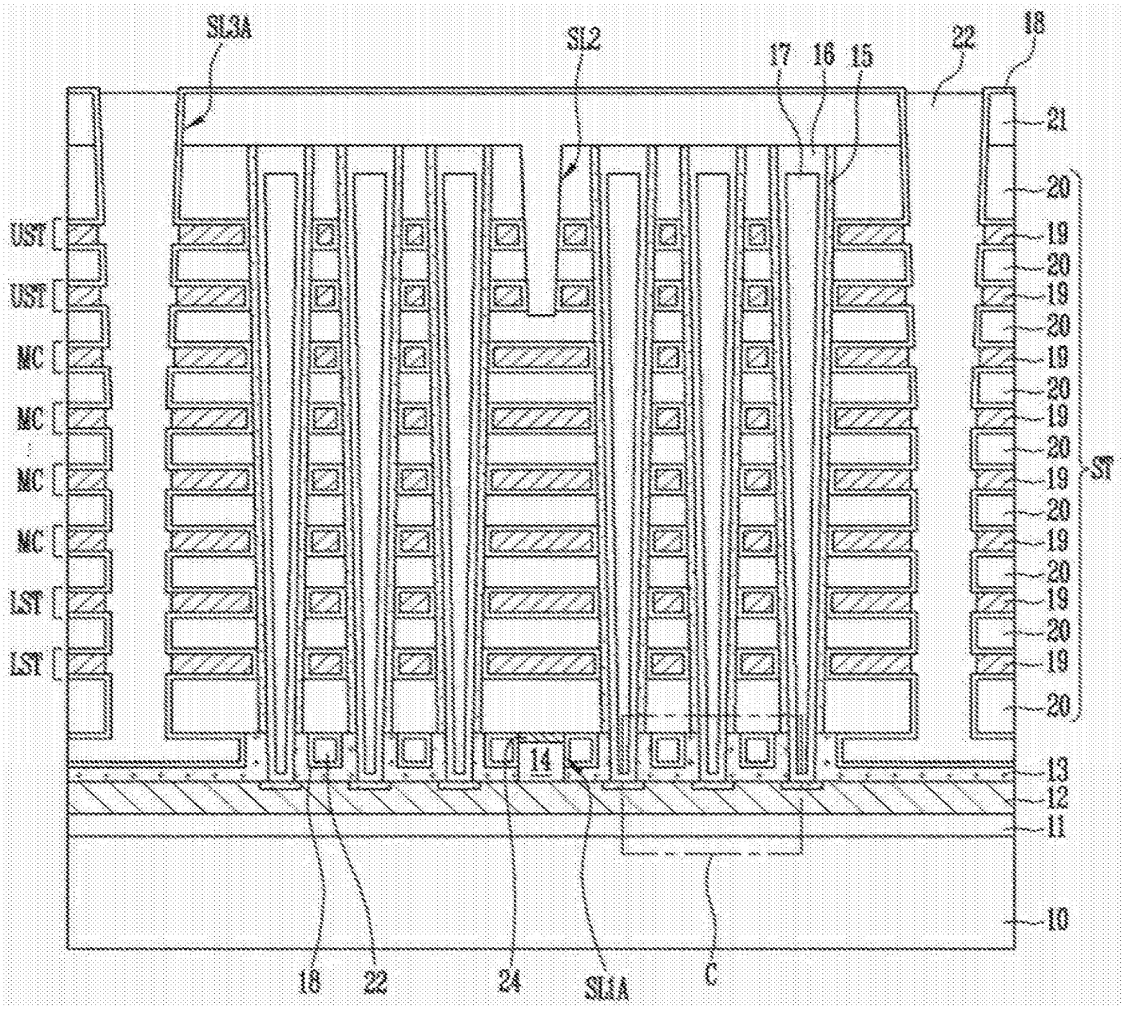


图 6

Micron Ex. 1002, p. 141
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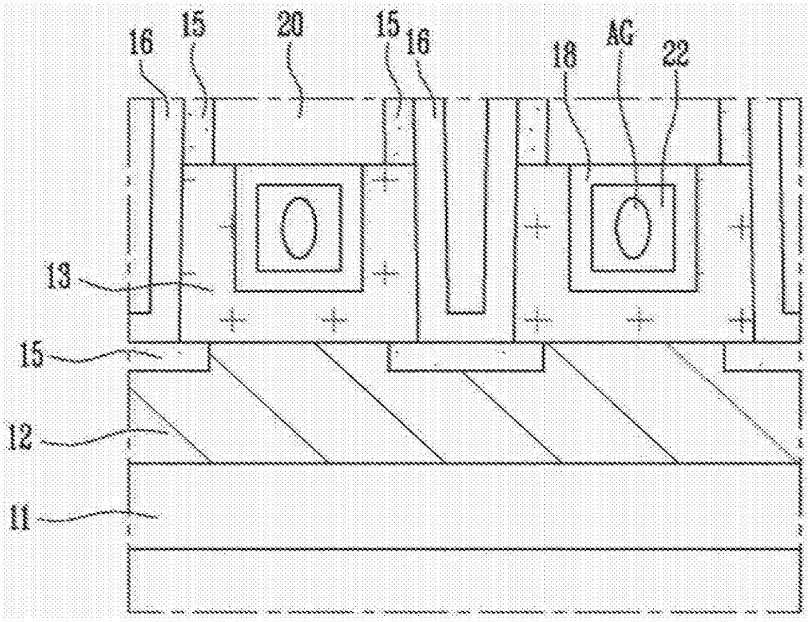


图 7

Micron Ex. 1002, p. 142
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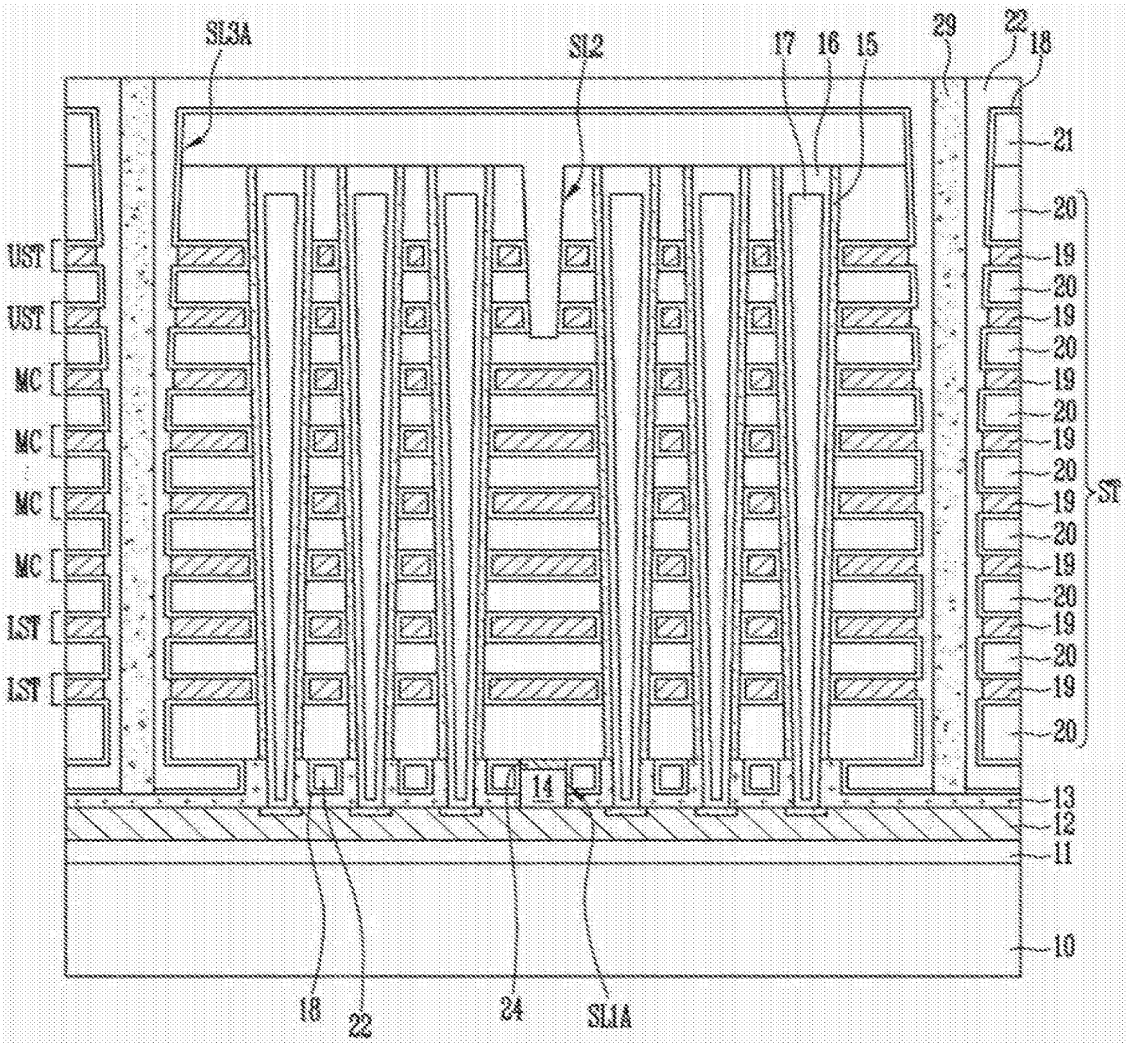


图 8

Micron Ex. 1002, p. 143
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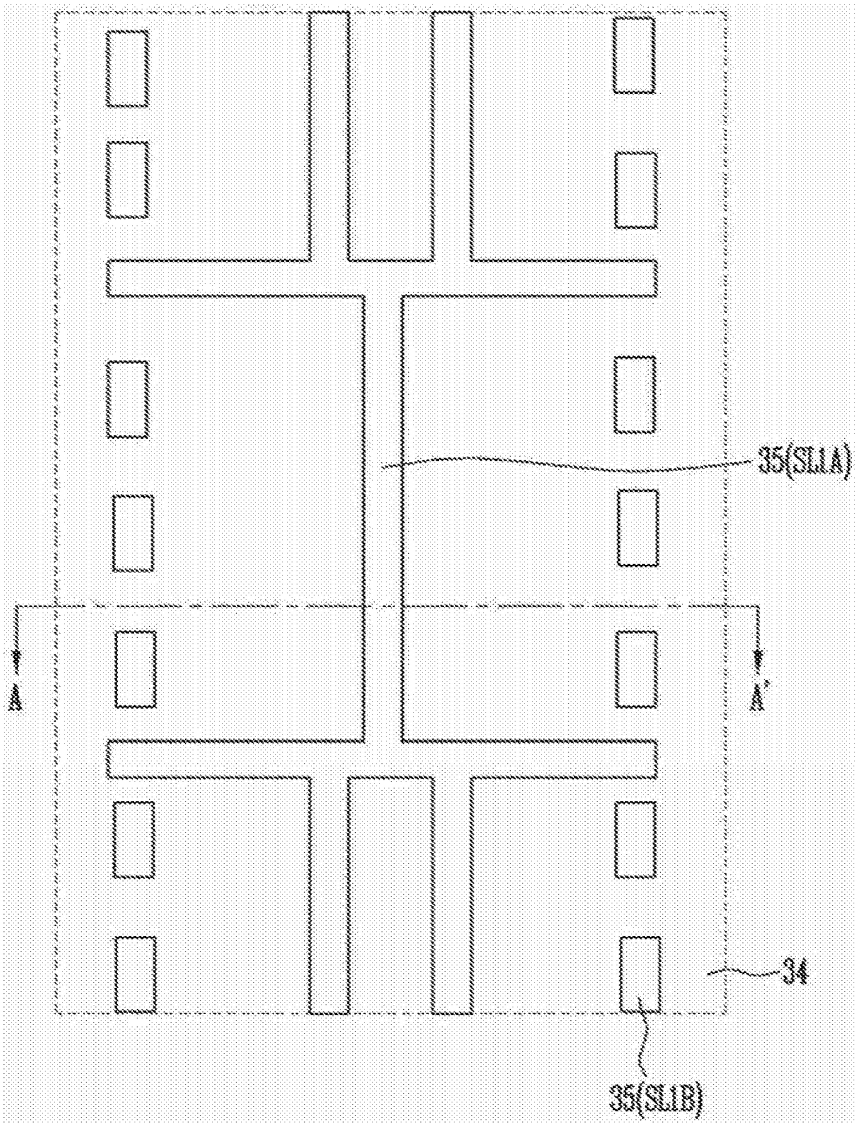


图 9A

Micron Ex. 1002, p. 144
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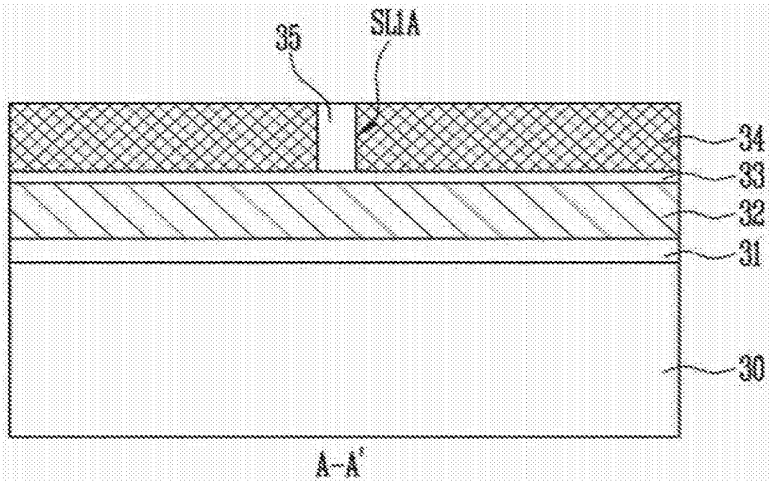


图 9B

Micron Ex. 1002, p. 145
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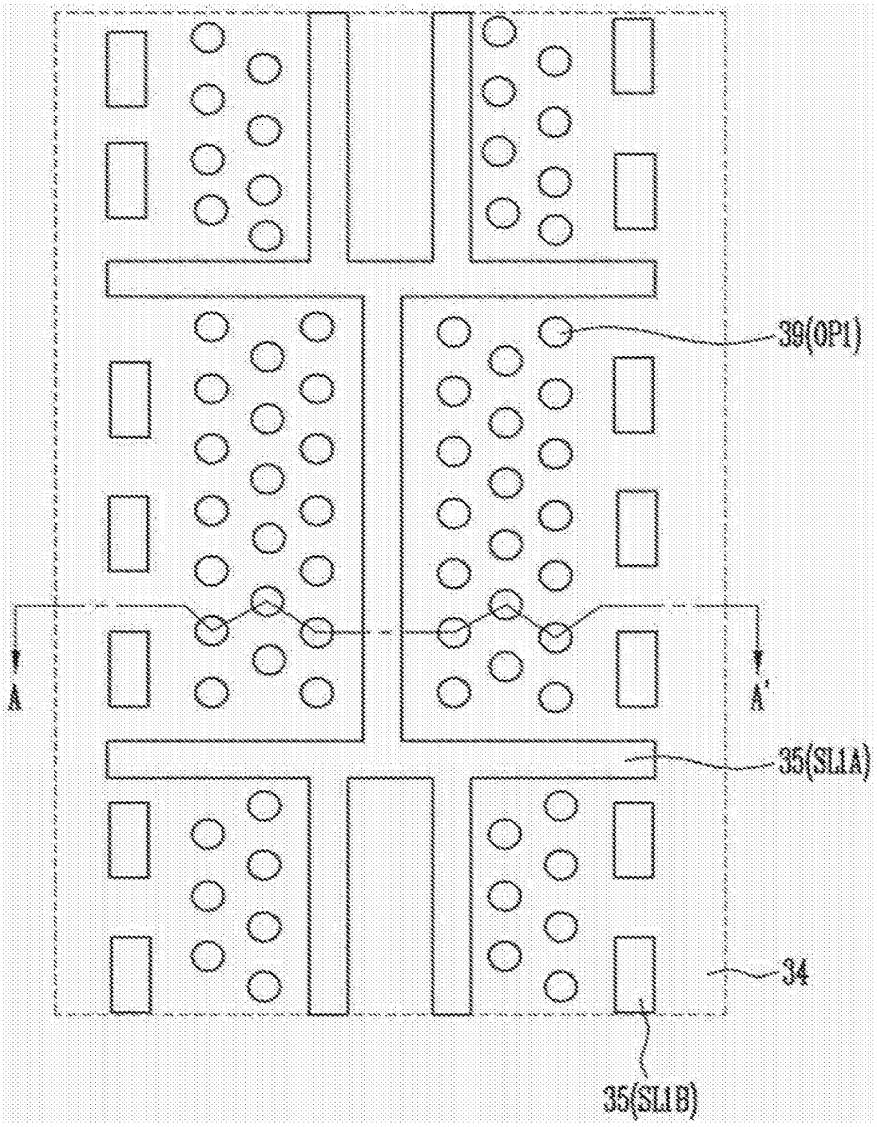


图 10A

Micron Ex. 1002, p. 146
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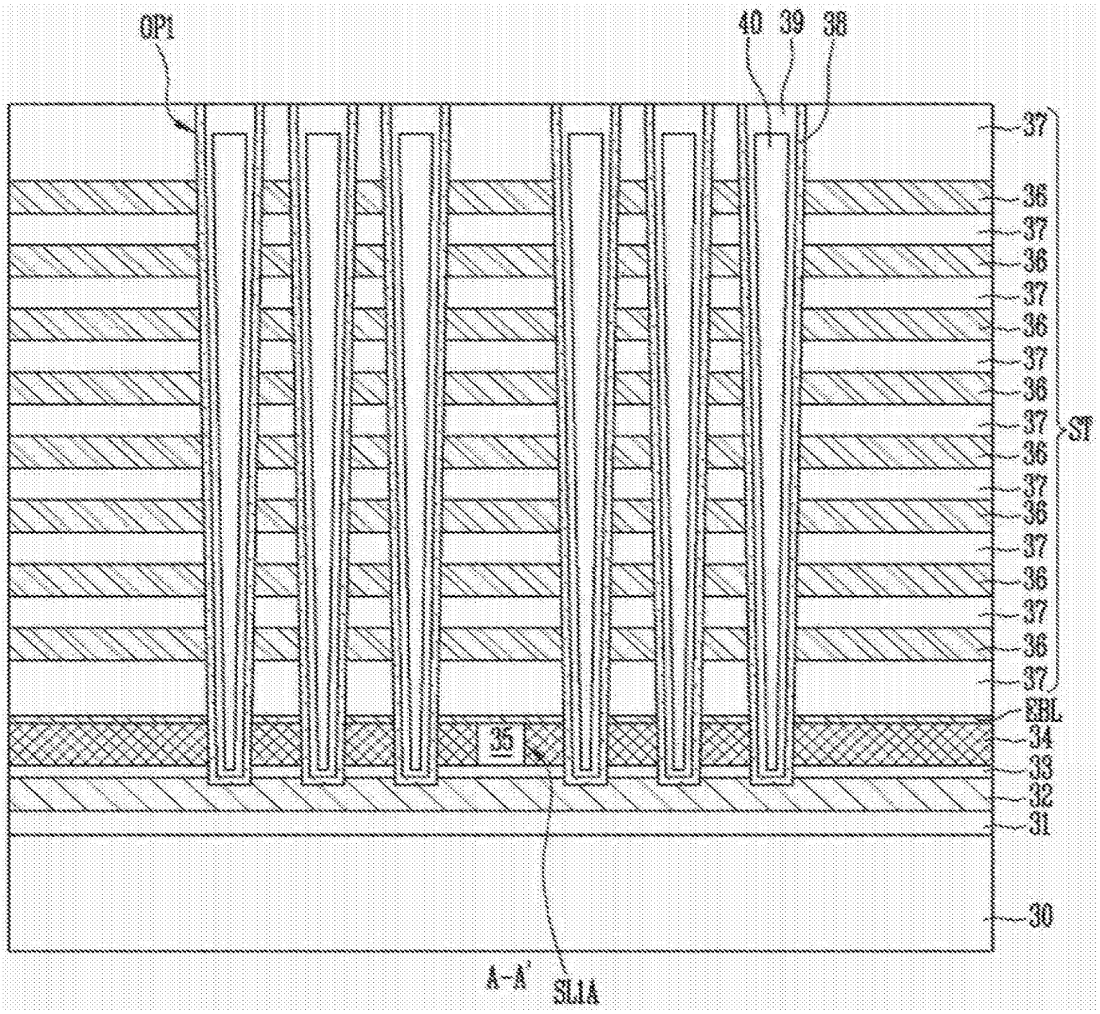


图 10B

Micron Ex. 1002, p. 147
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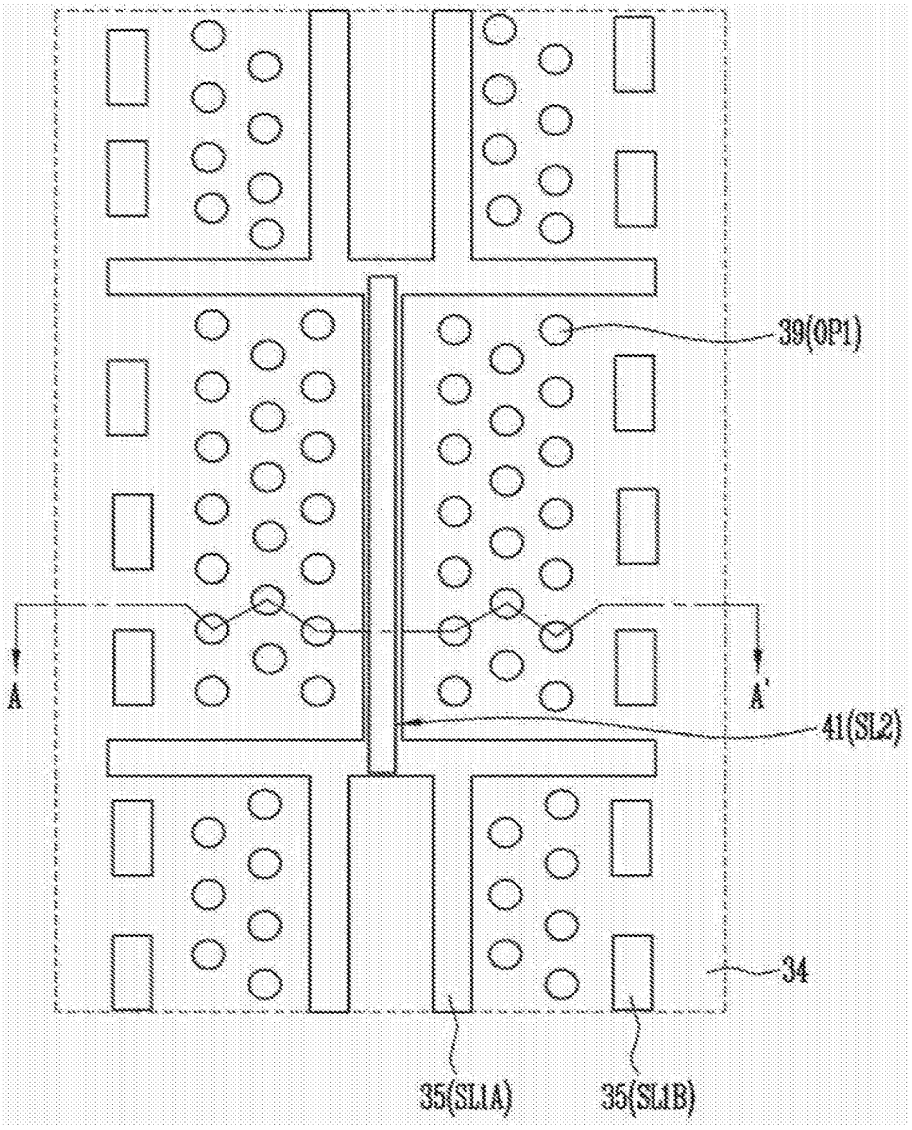


图 11A

Micron Ex. 1002, p. 148
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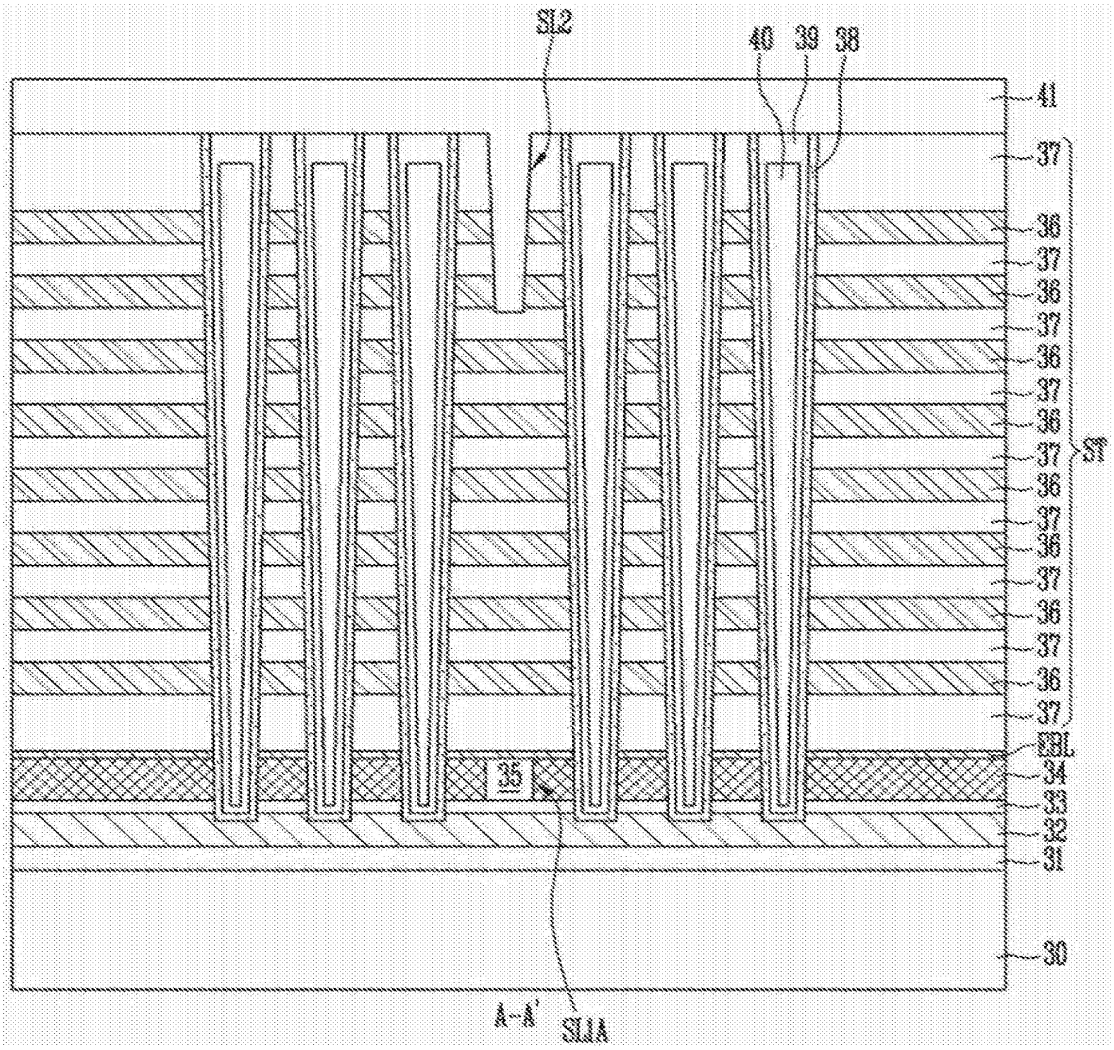


图 11B

Micron Ex. 1002, p. 149
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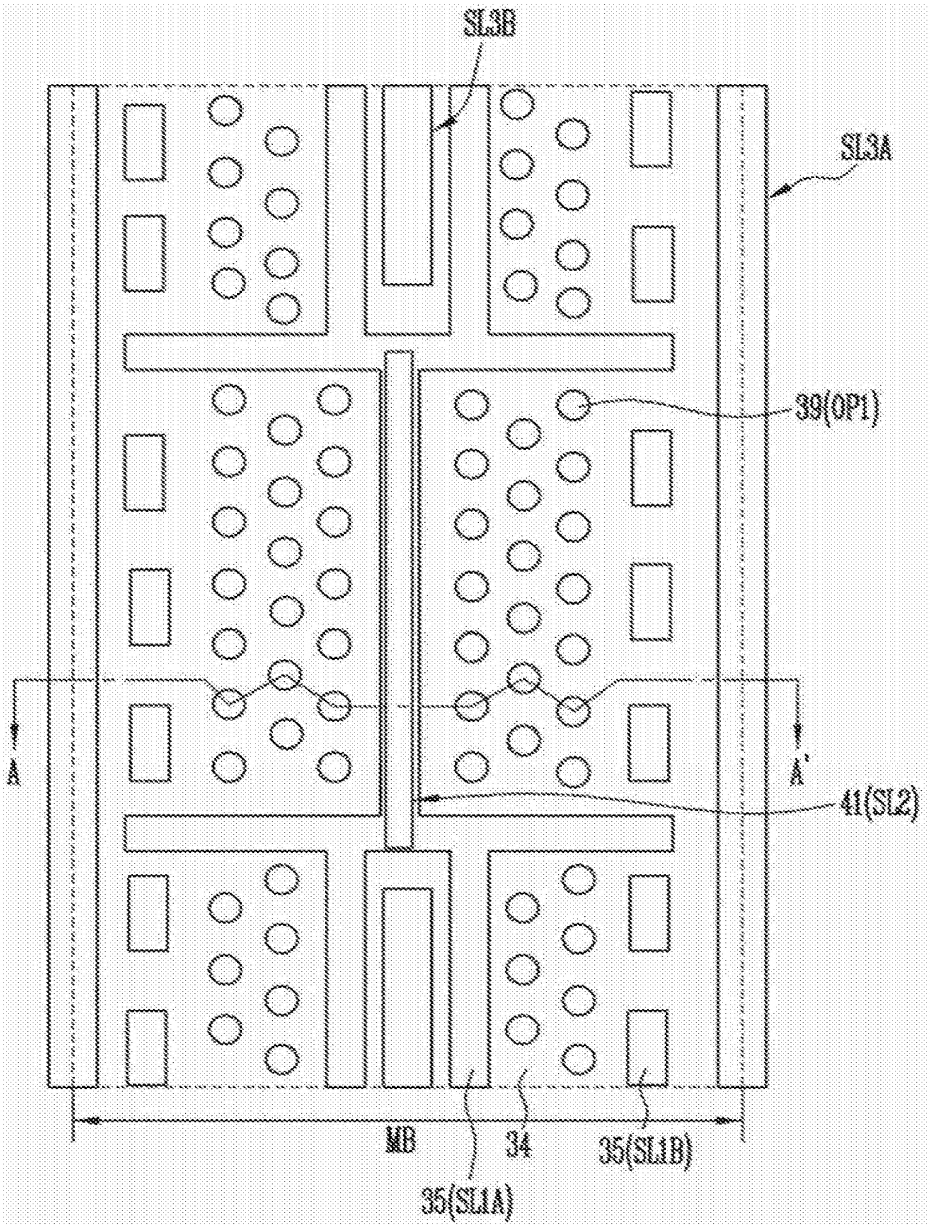


图 12A

Micron Ex. 1002, p. 150
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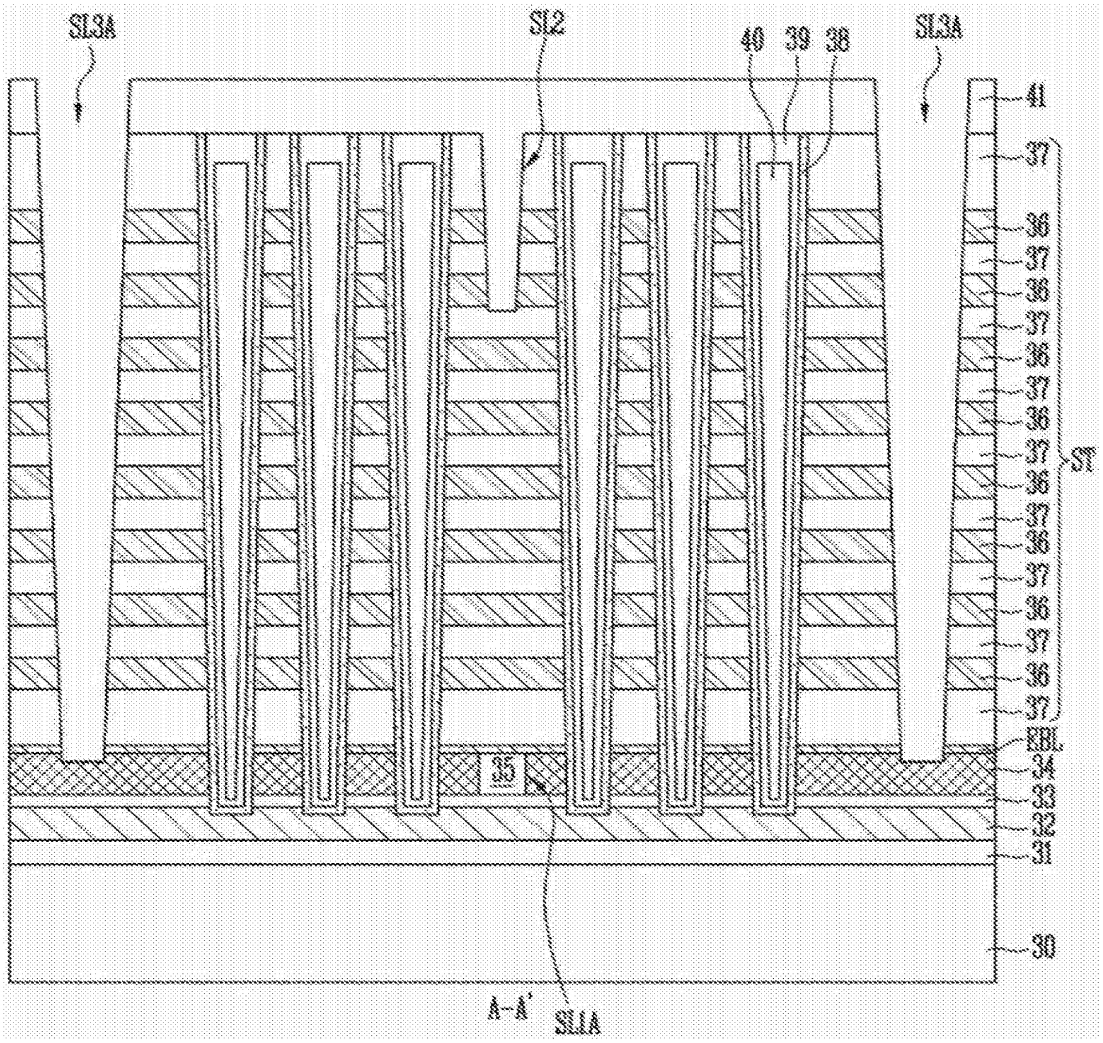


图 12B

Micron Ex. 1002, p. 151
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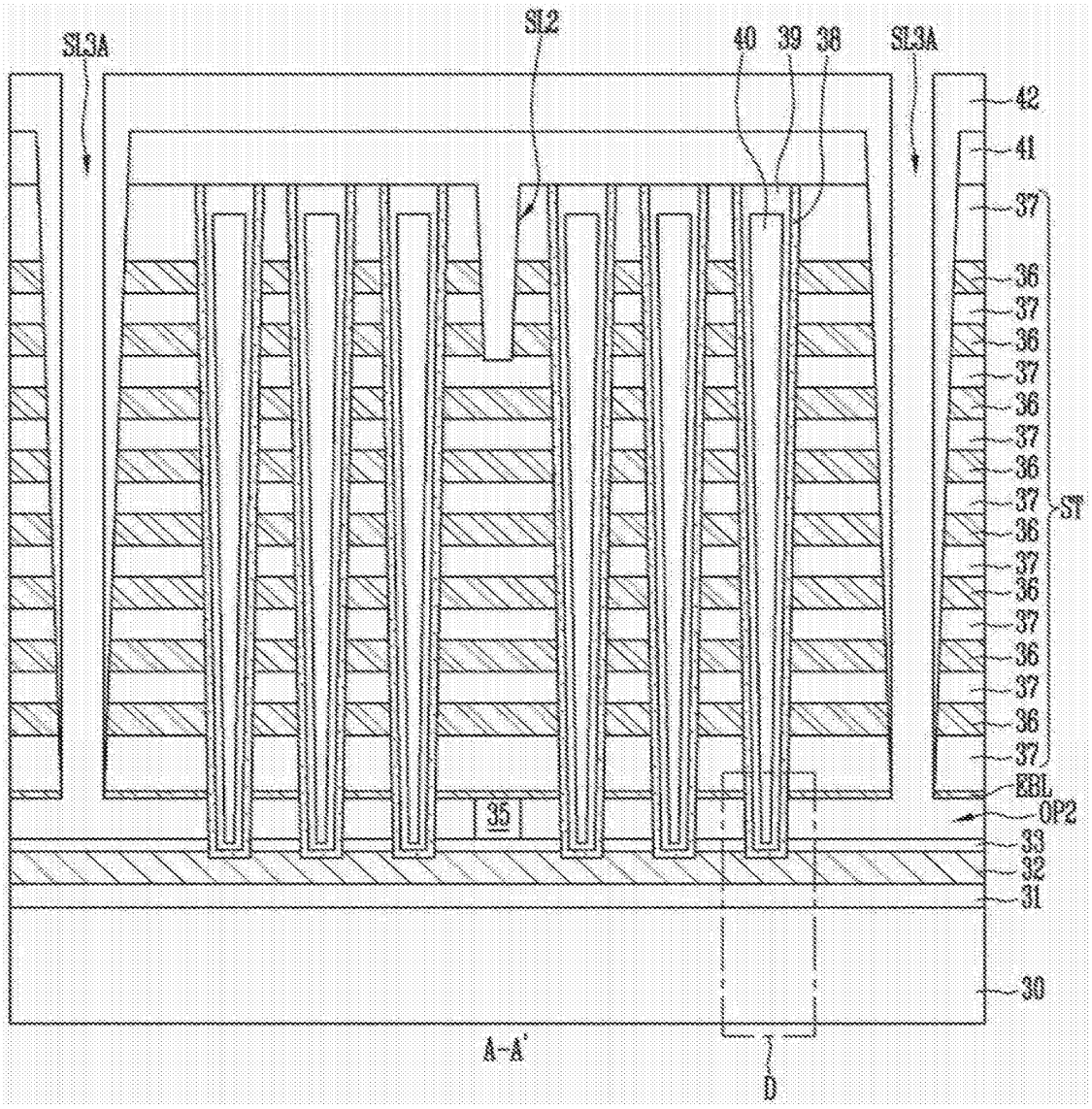


图 13

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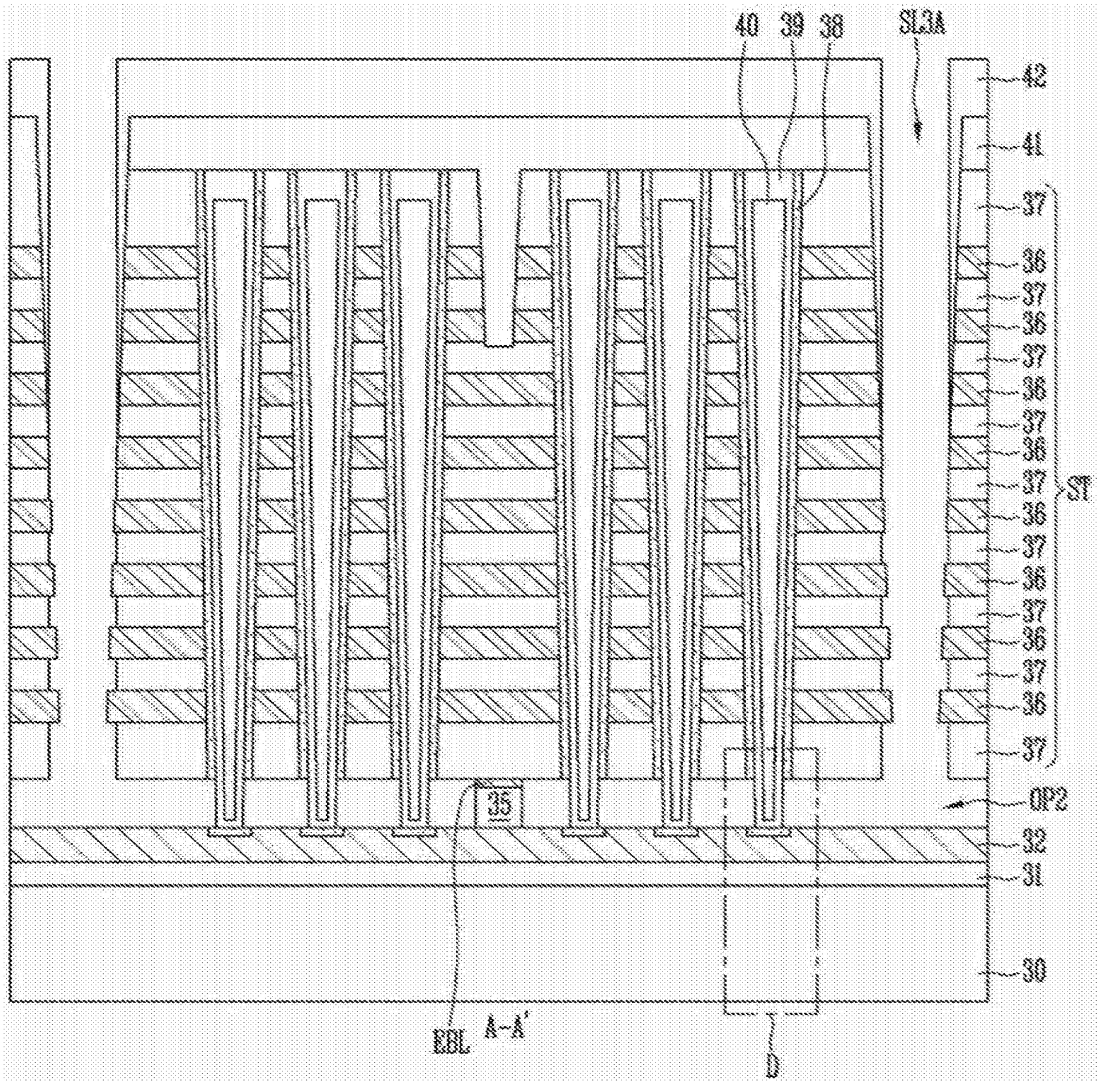


图 14

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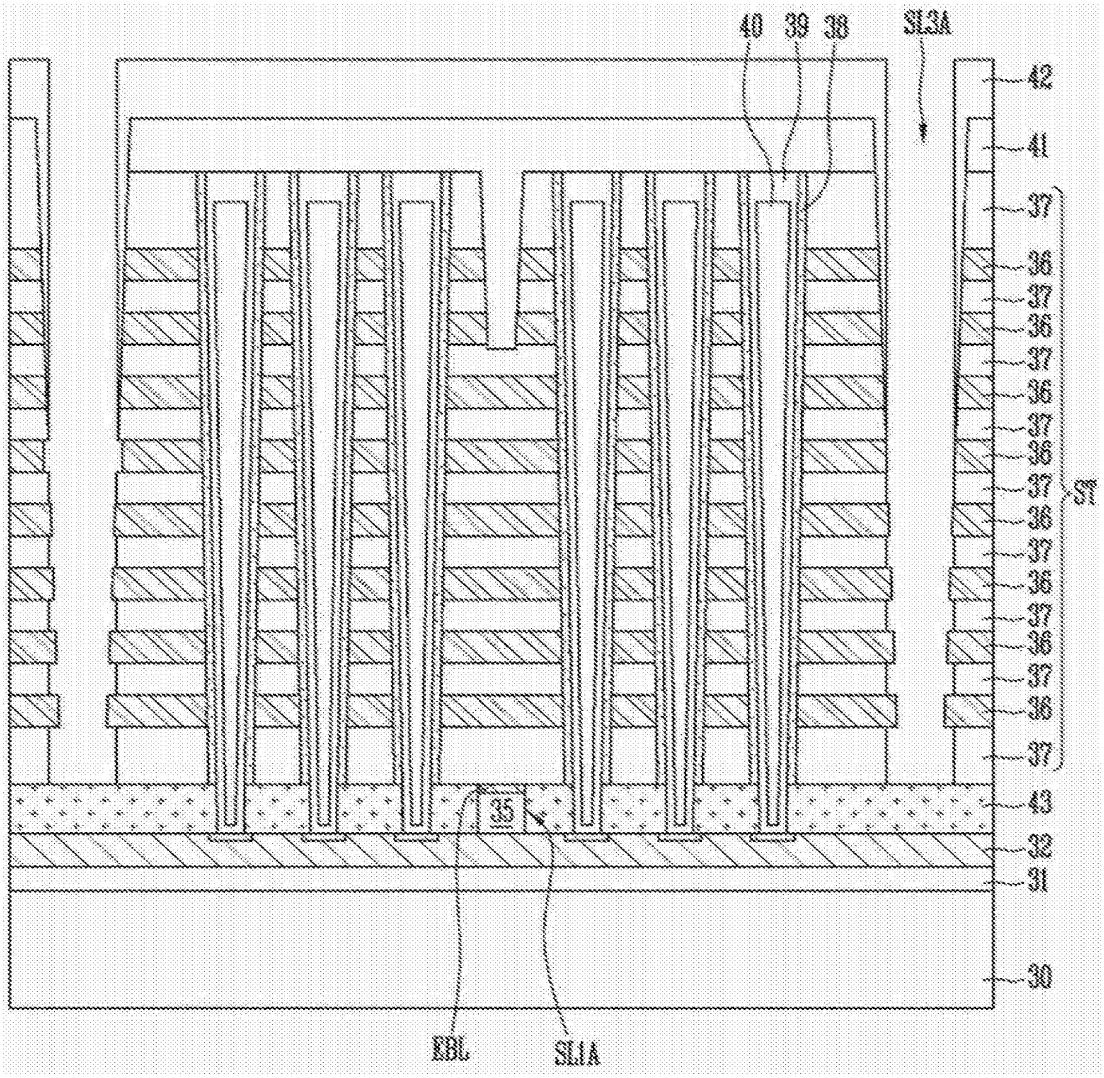


图 15

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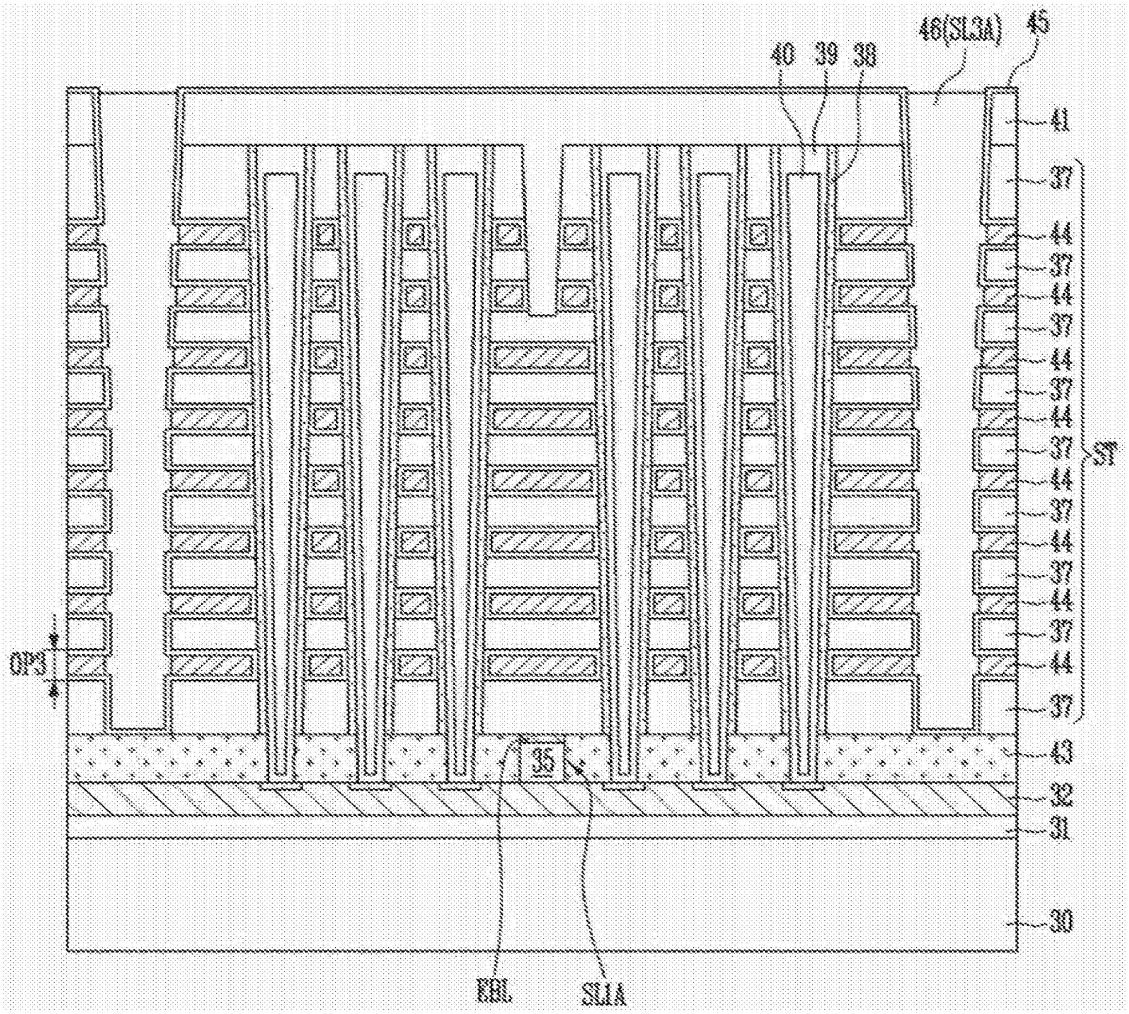


图 16

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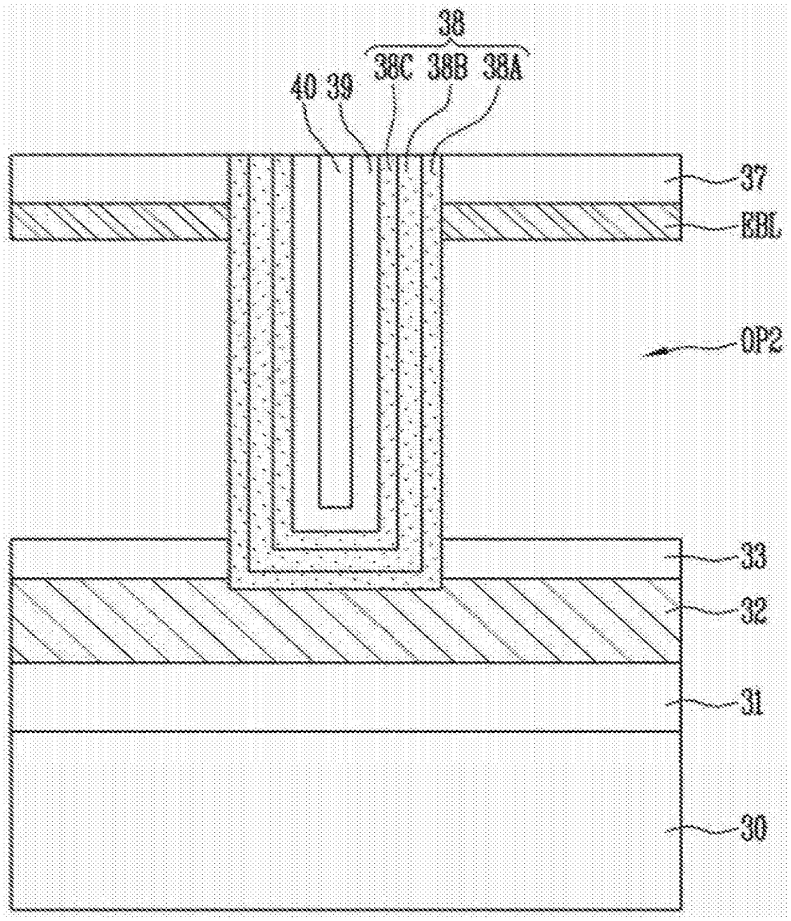


图 17A

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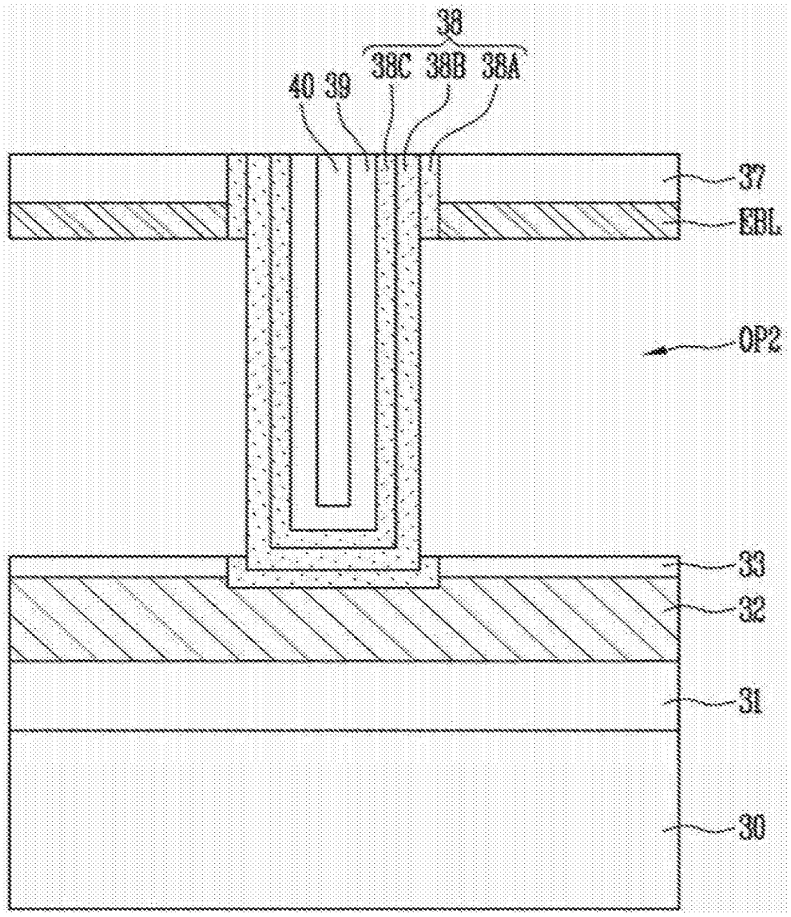


图 17B

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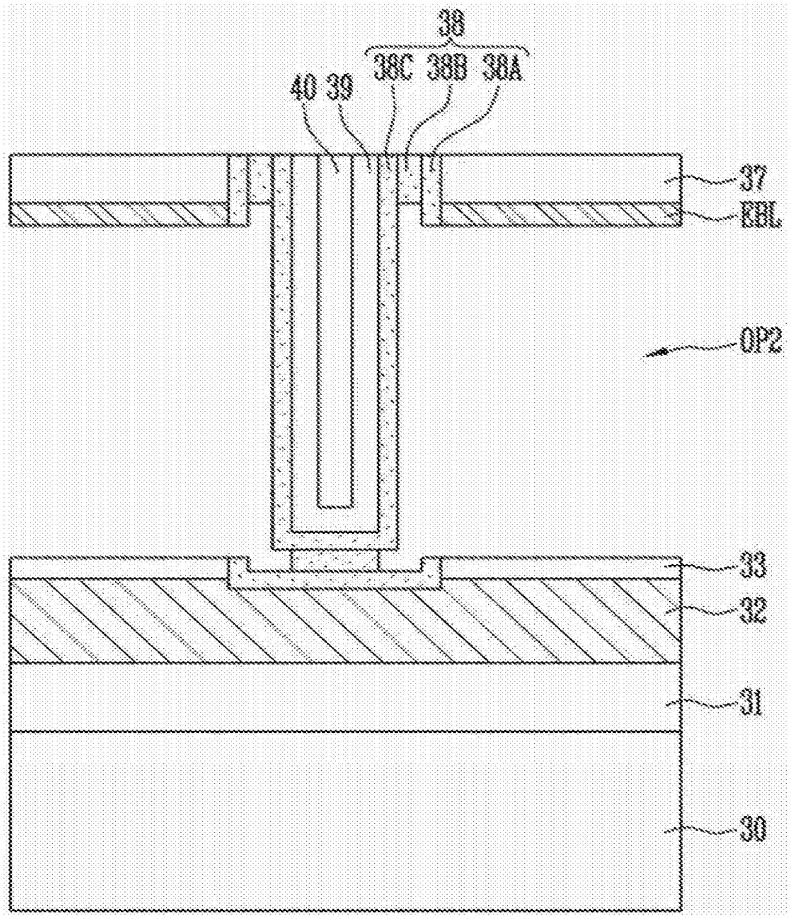


图 17C

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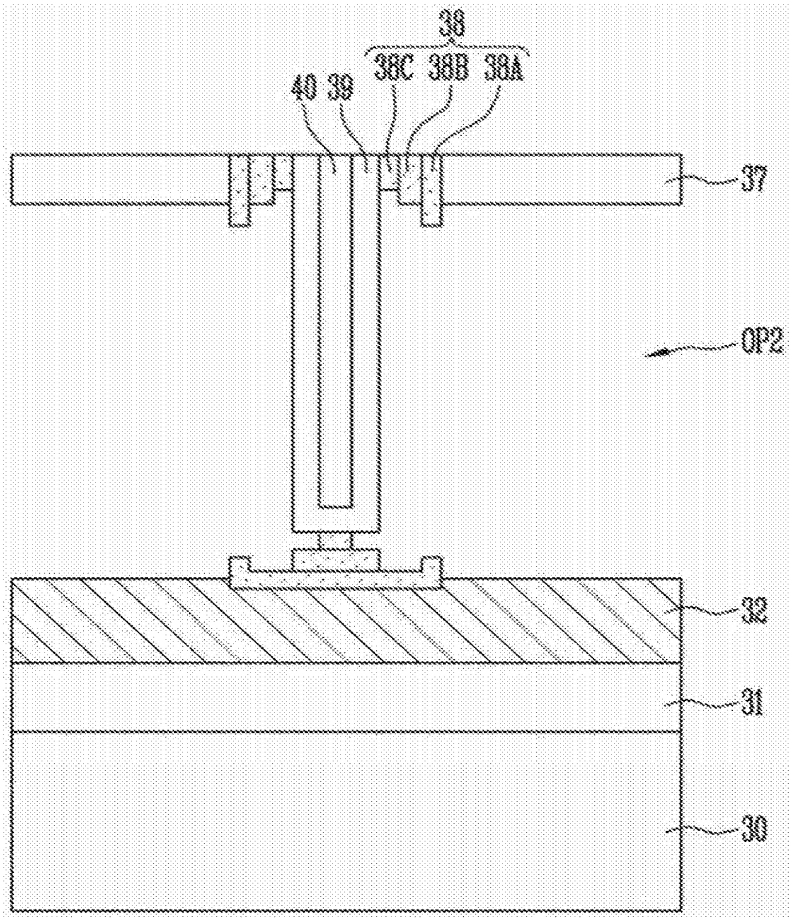


图 17D

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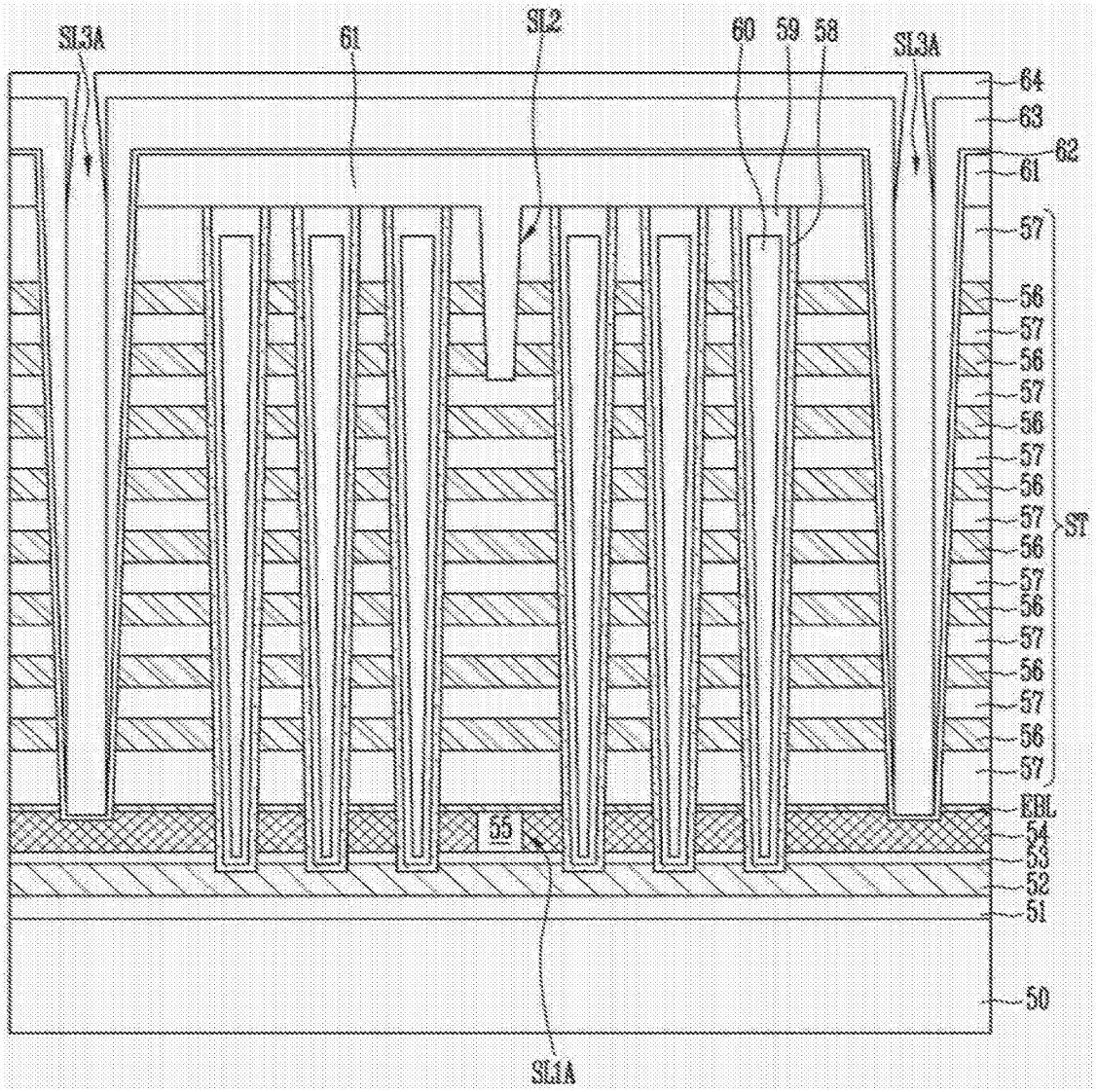


图 18

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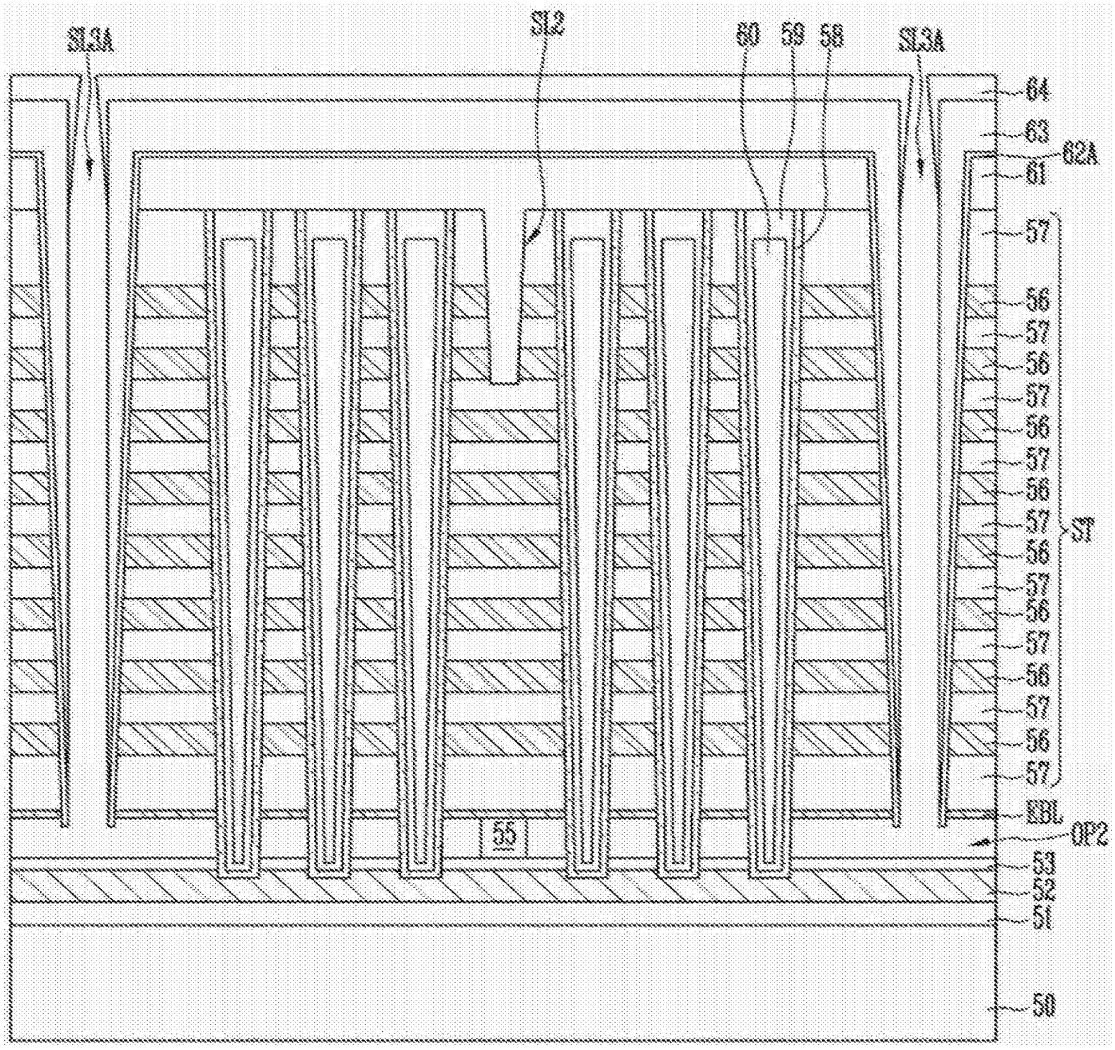


图 19

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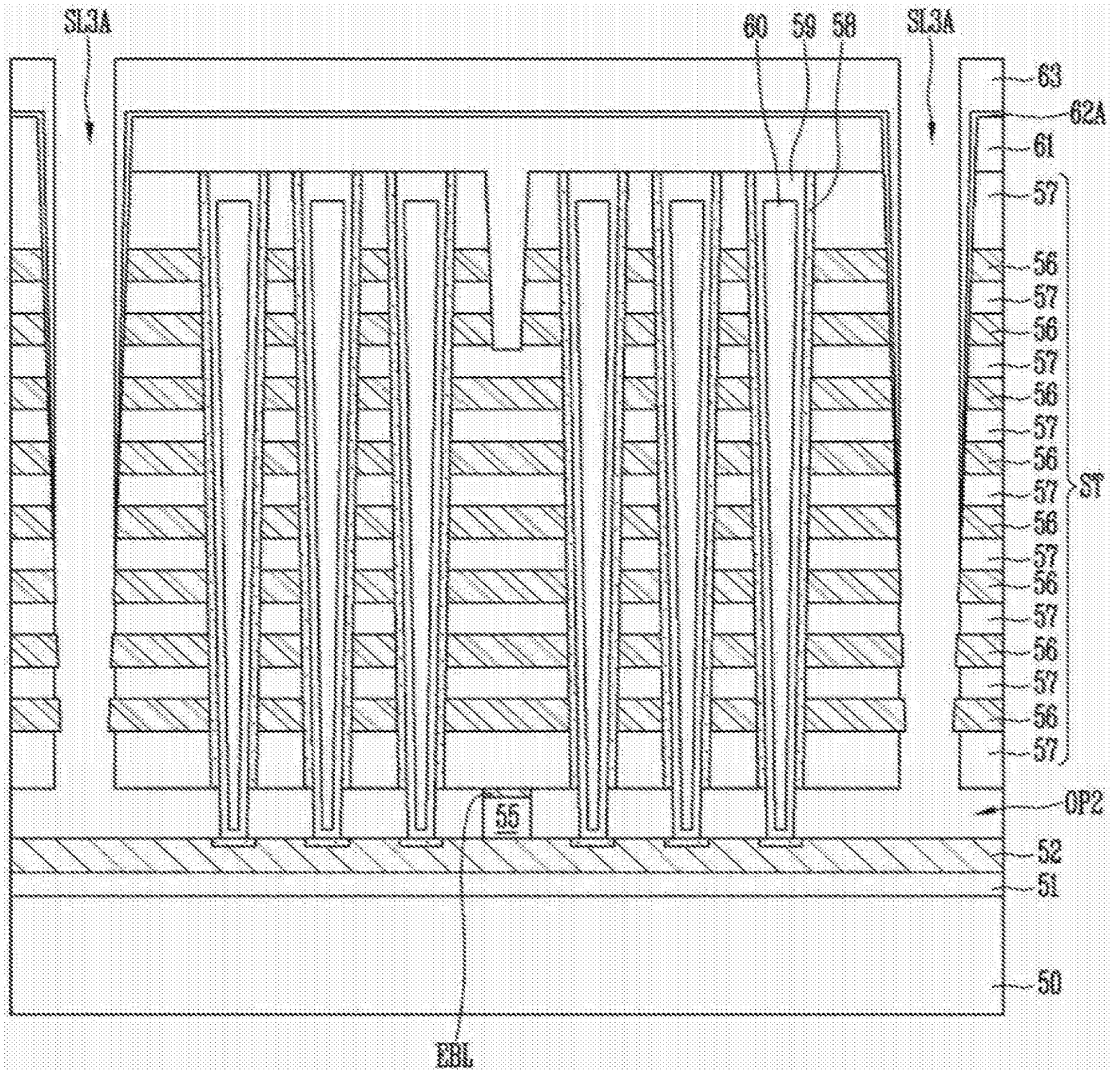


图 20

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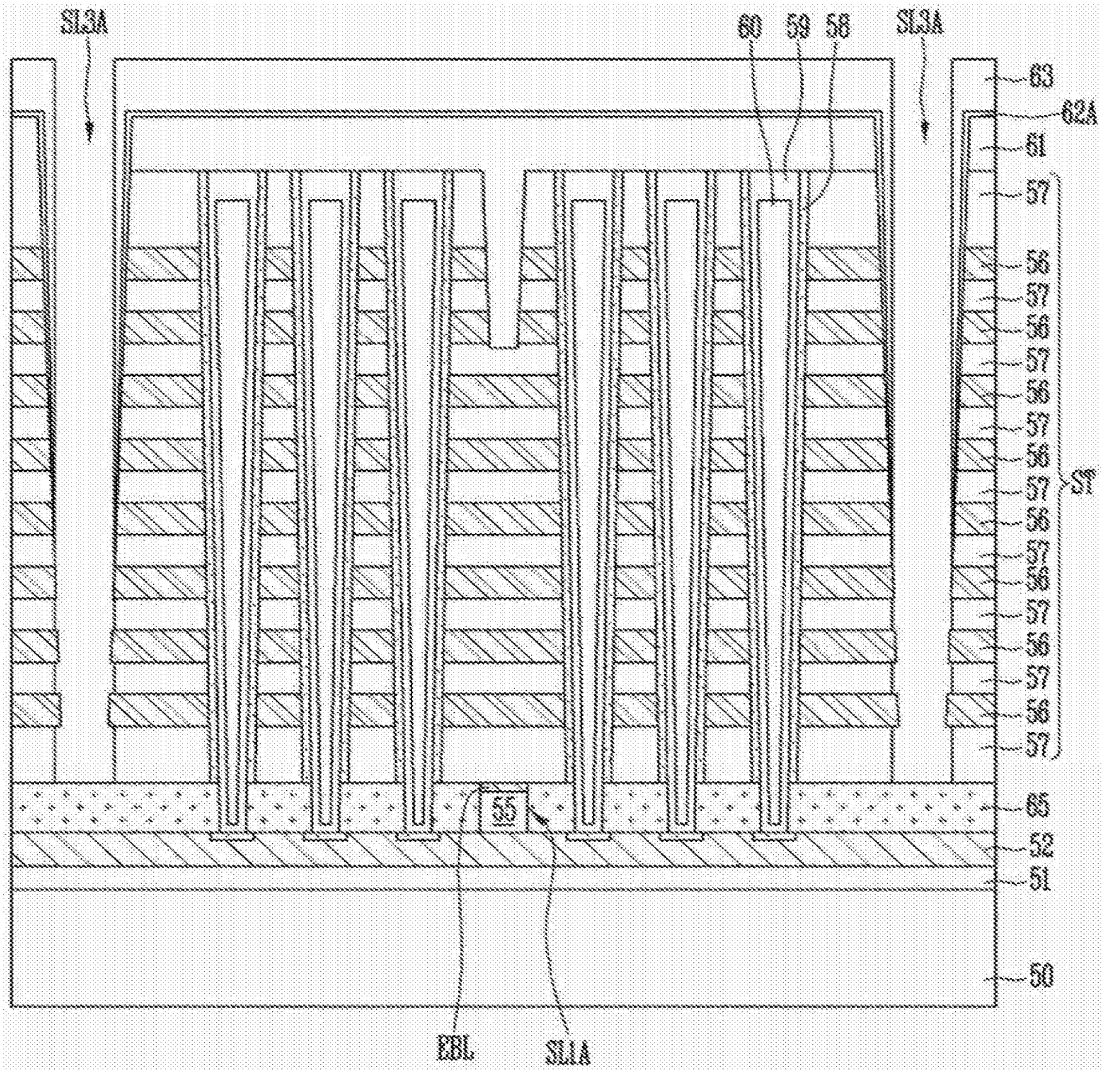


图 21

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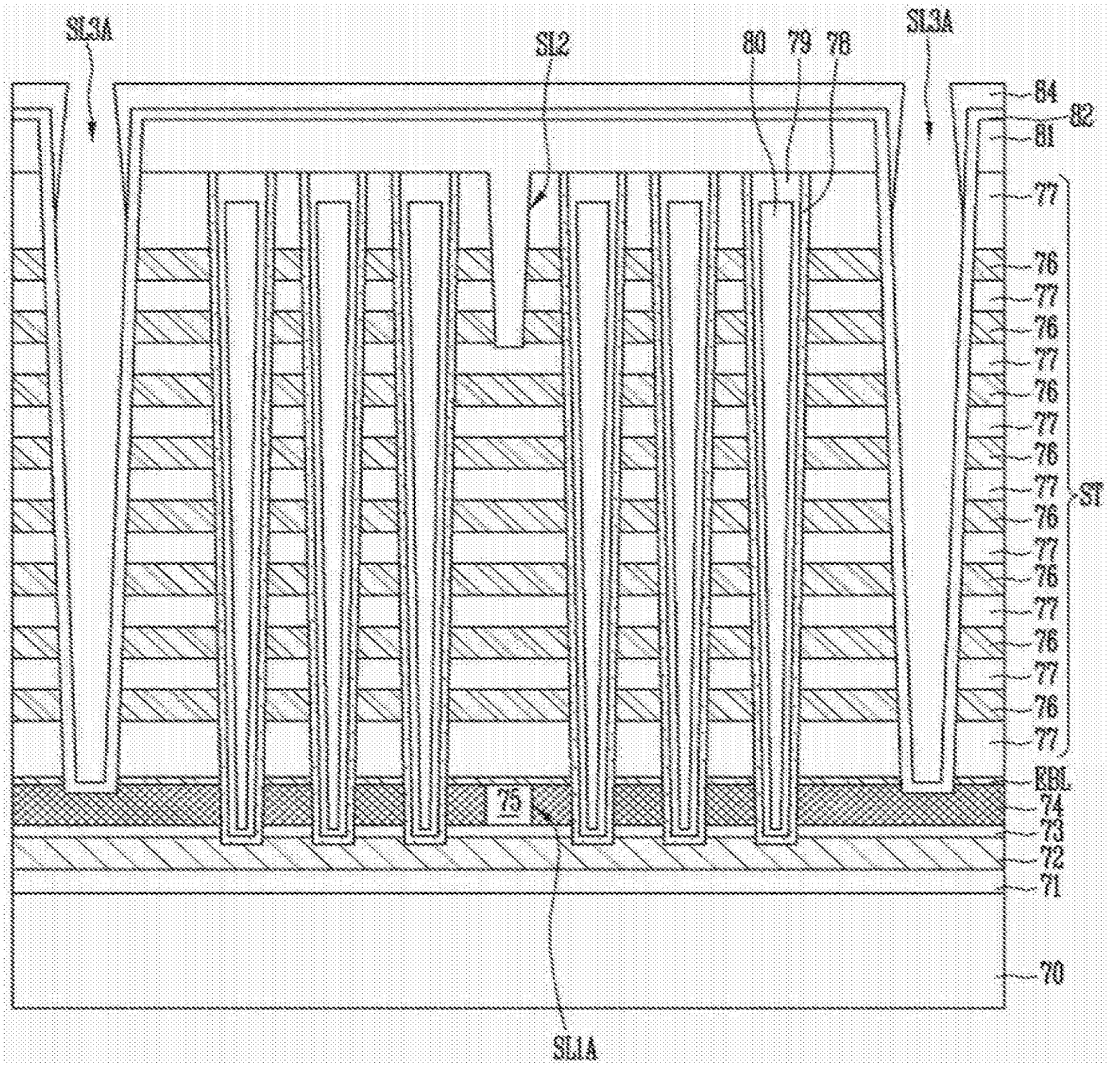


图 22

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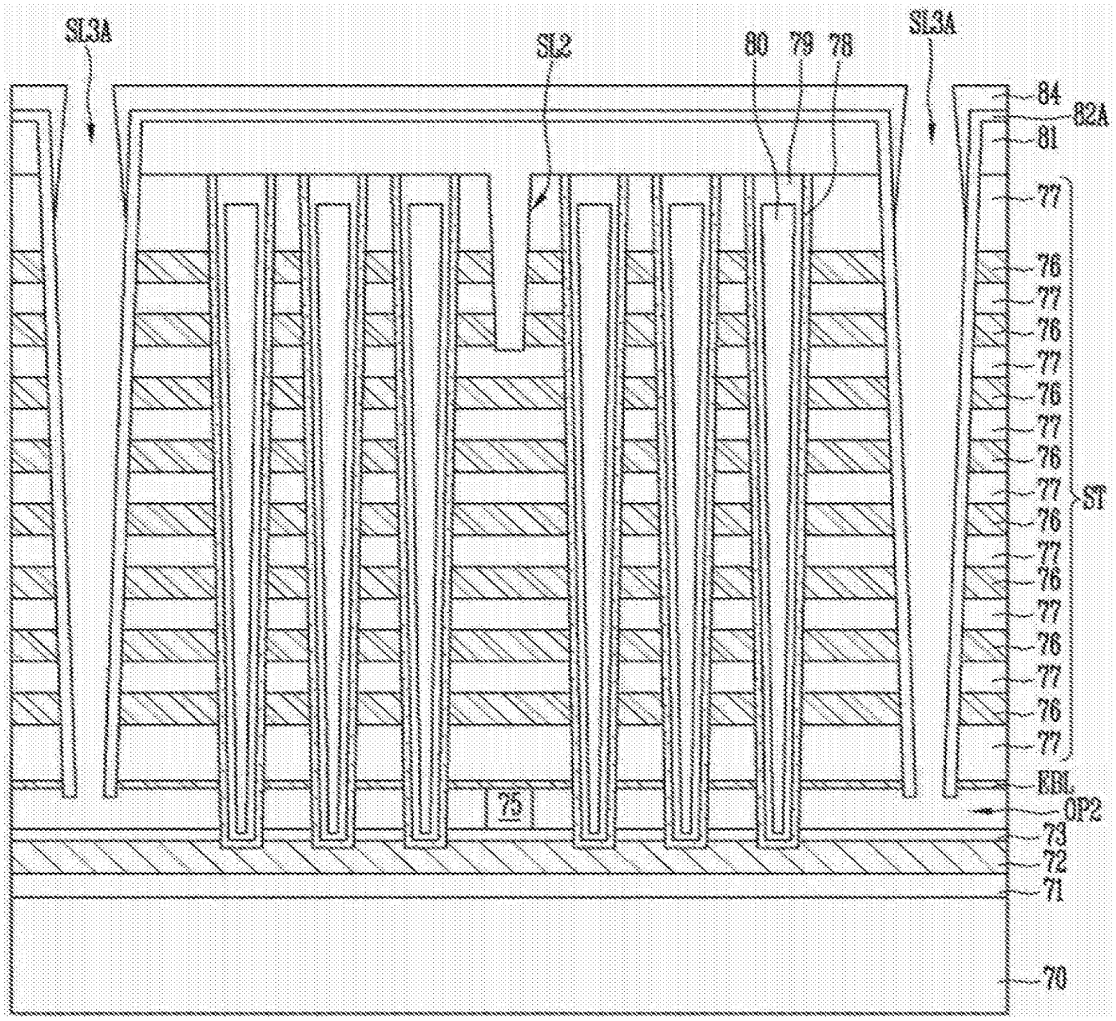


图 23

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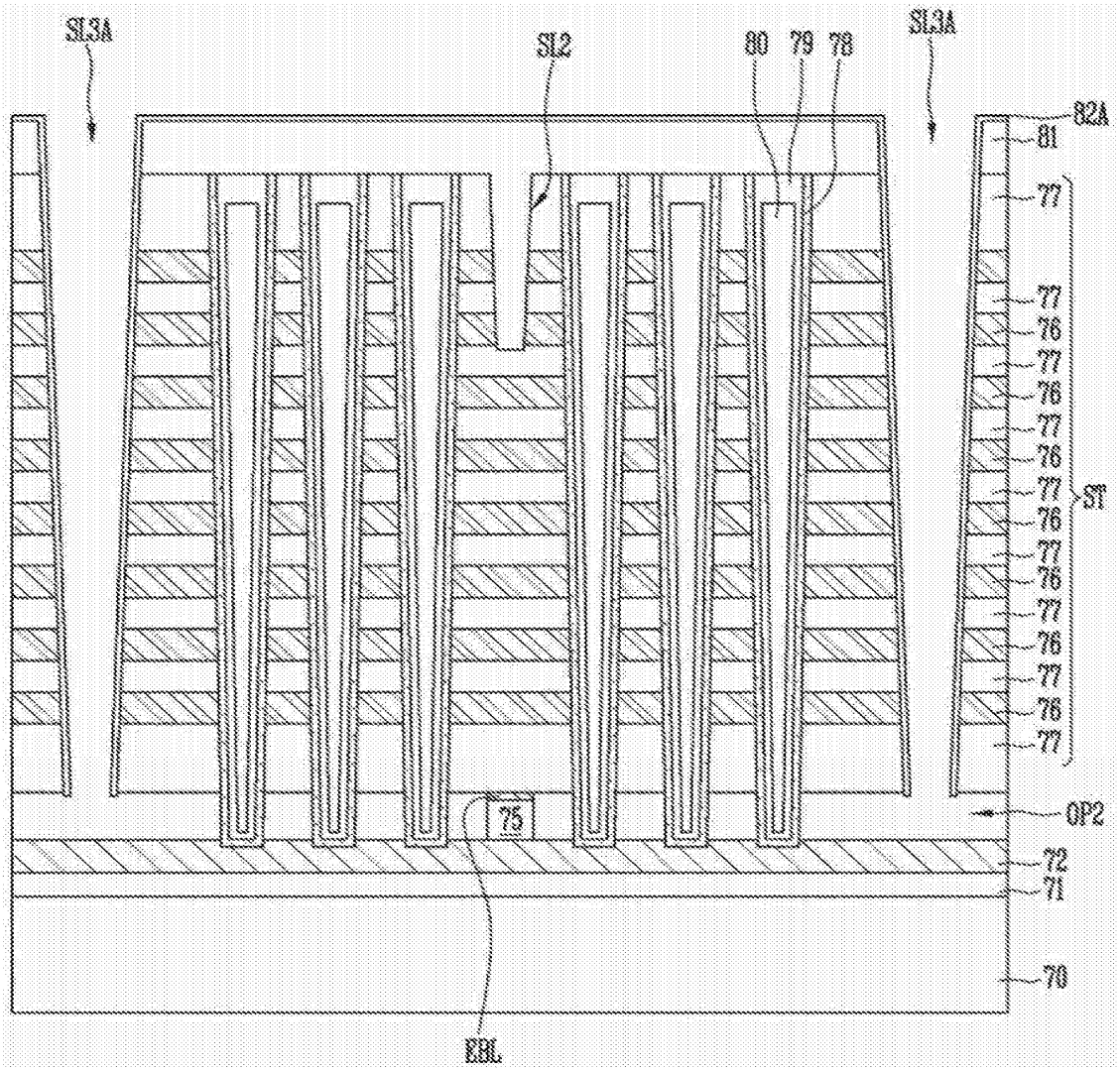


图 24

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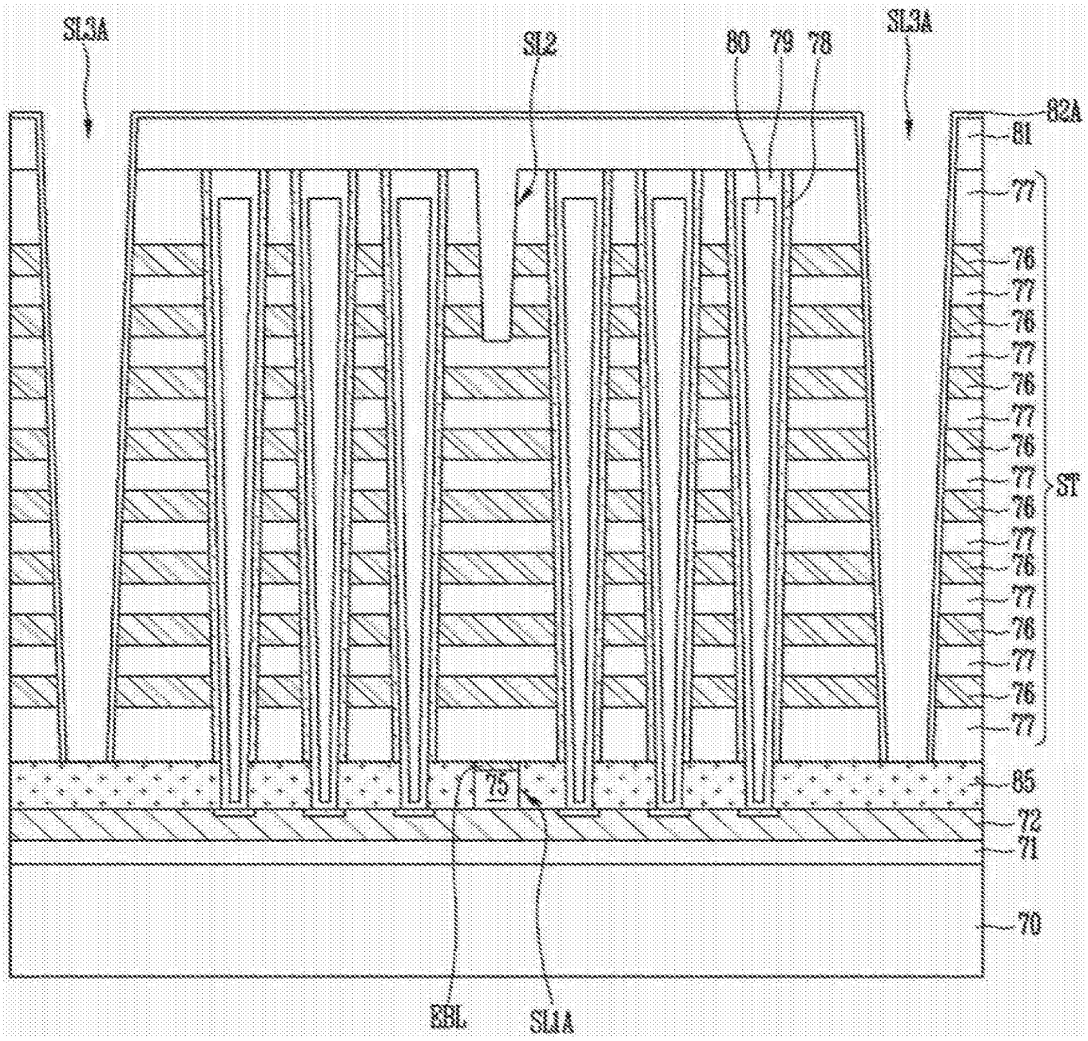


图 25

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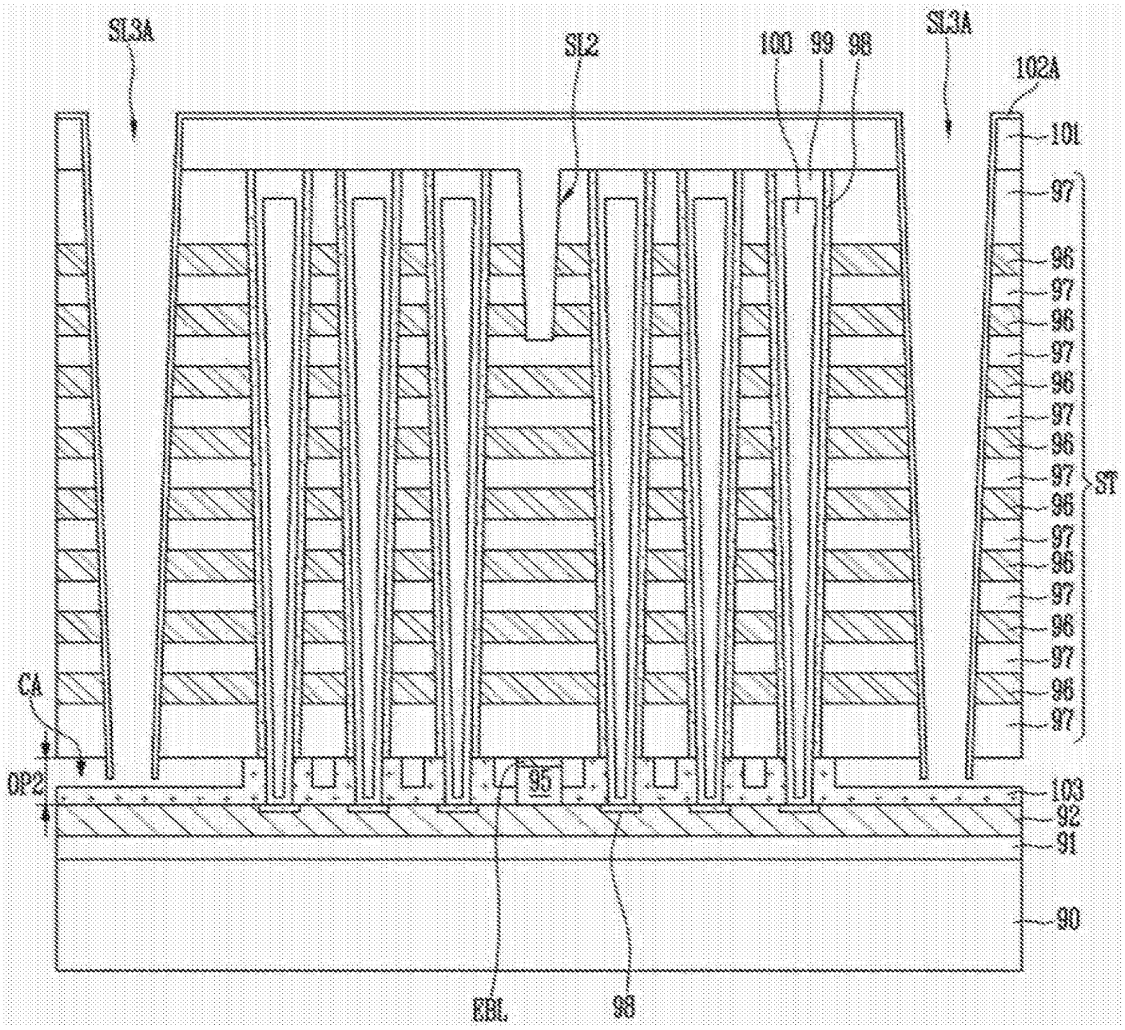


图 26

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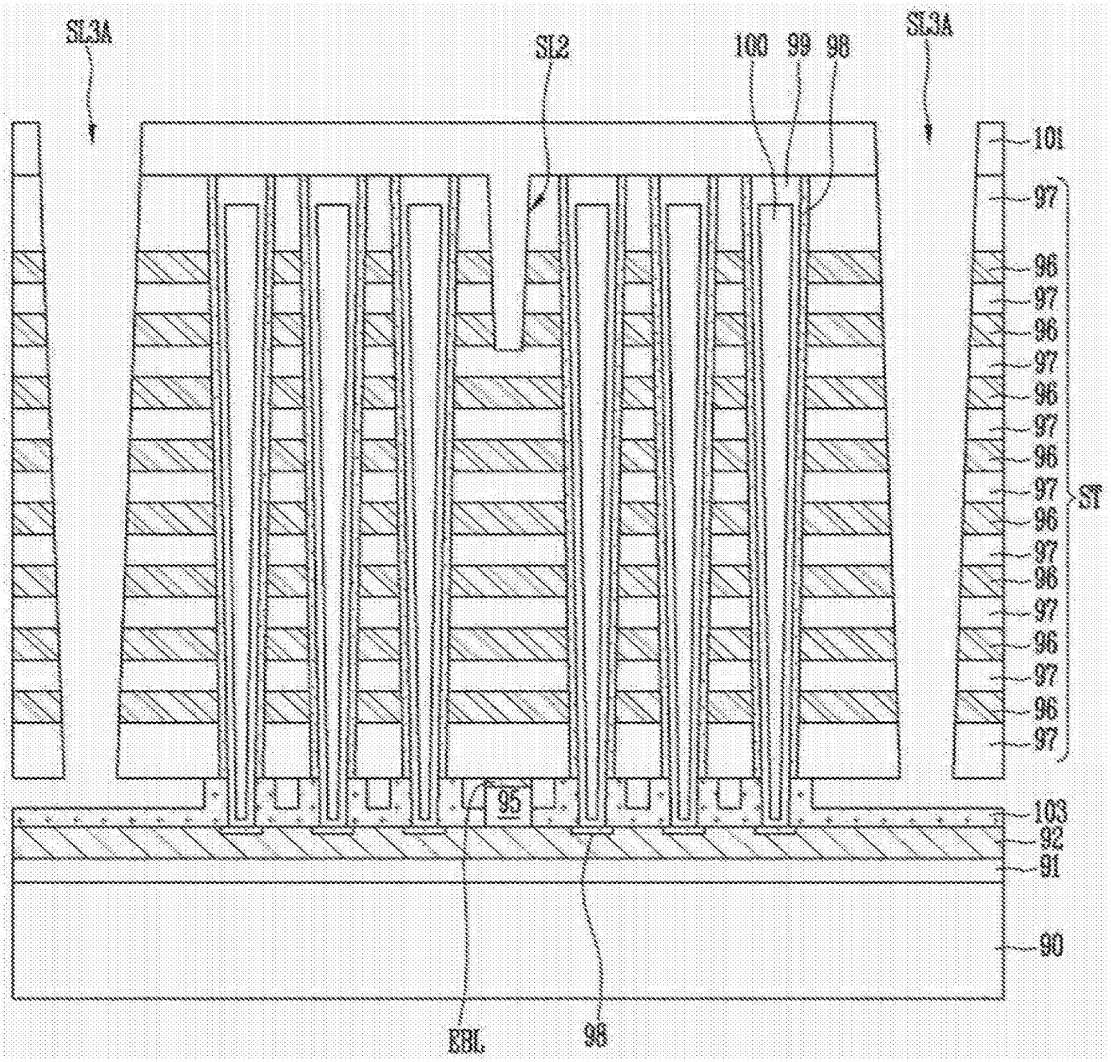


图 27

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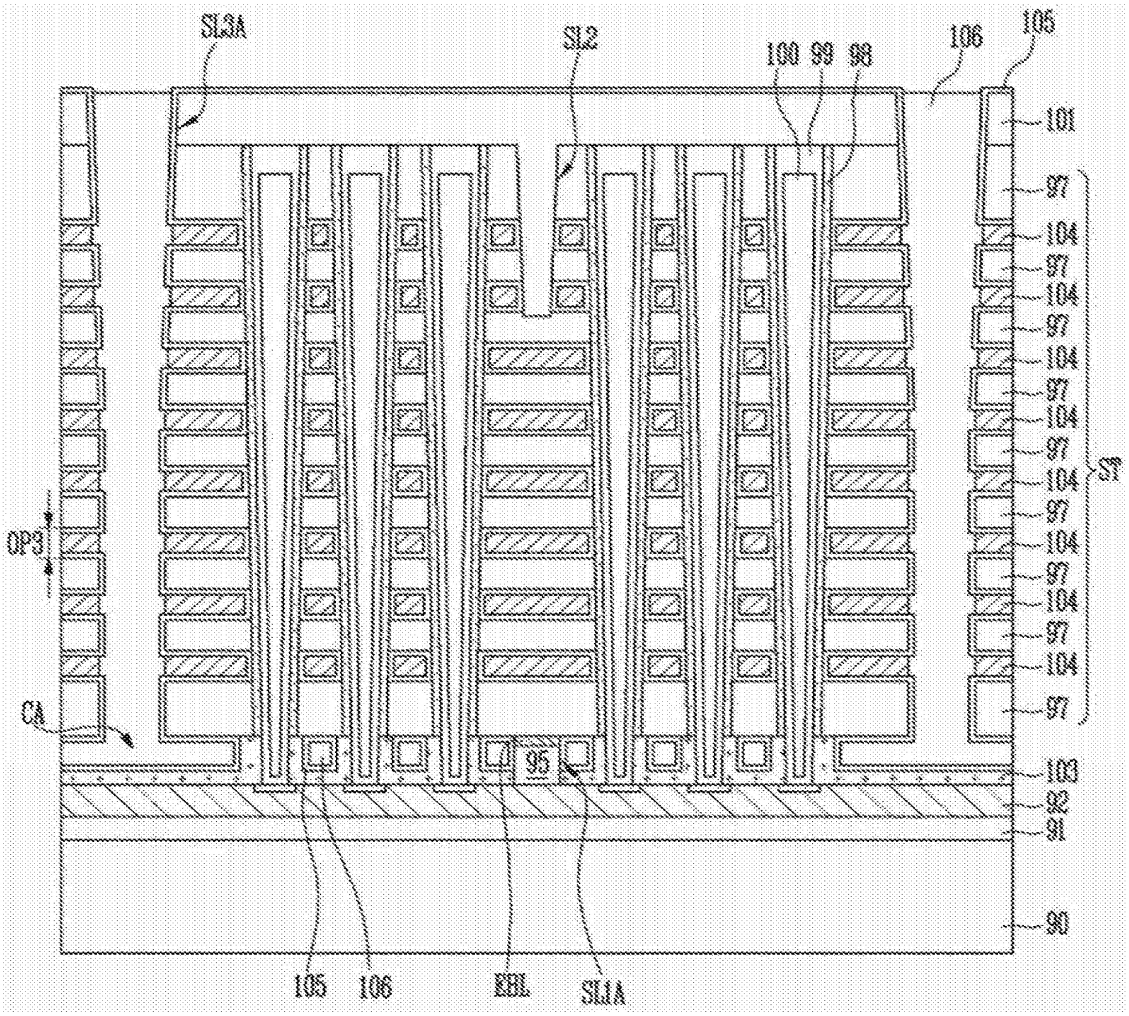


图 28

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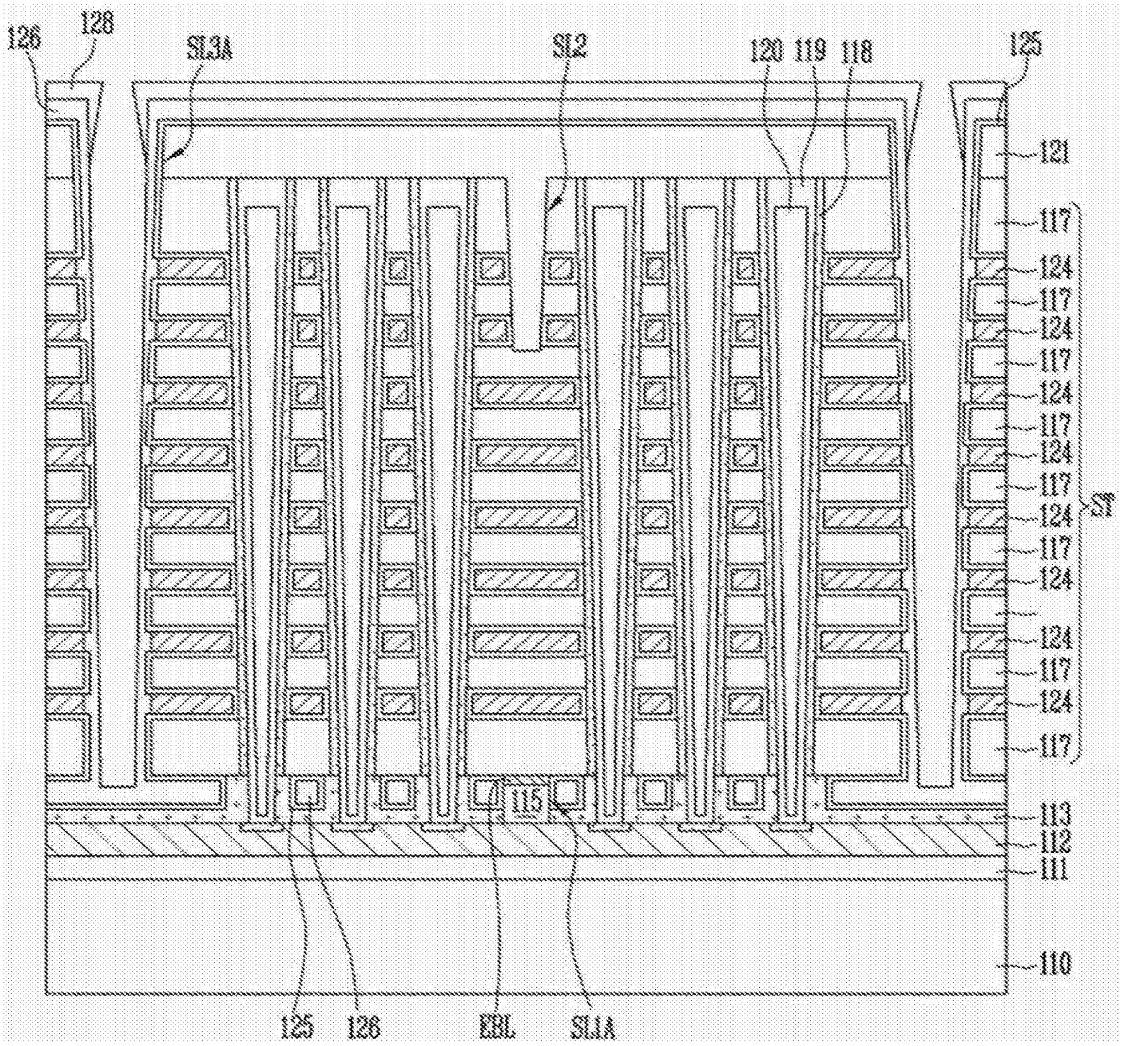


图 29

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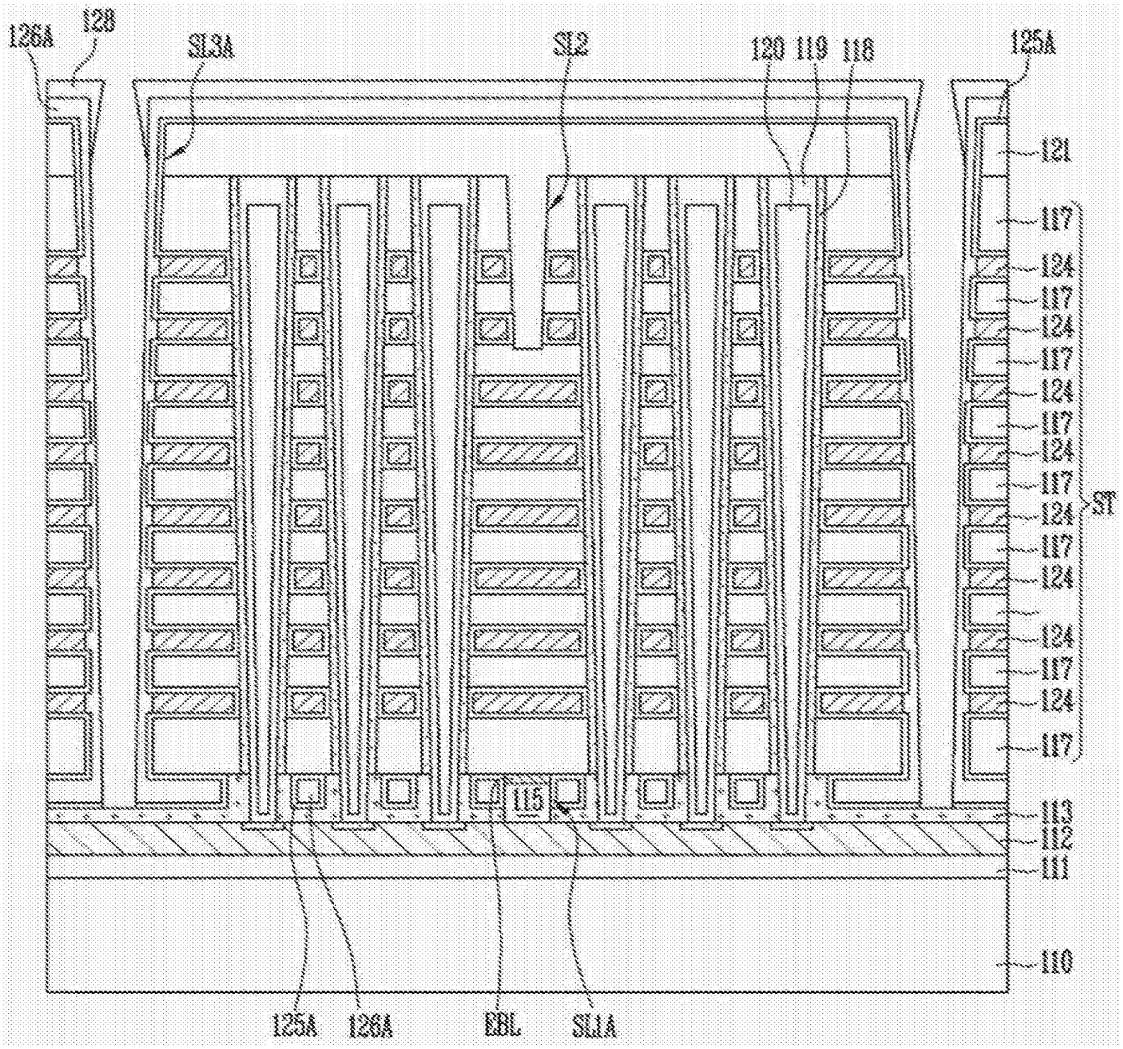


图 30

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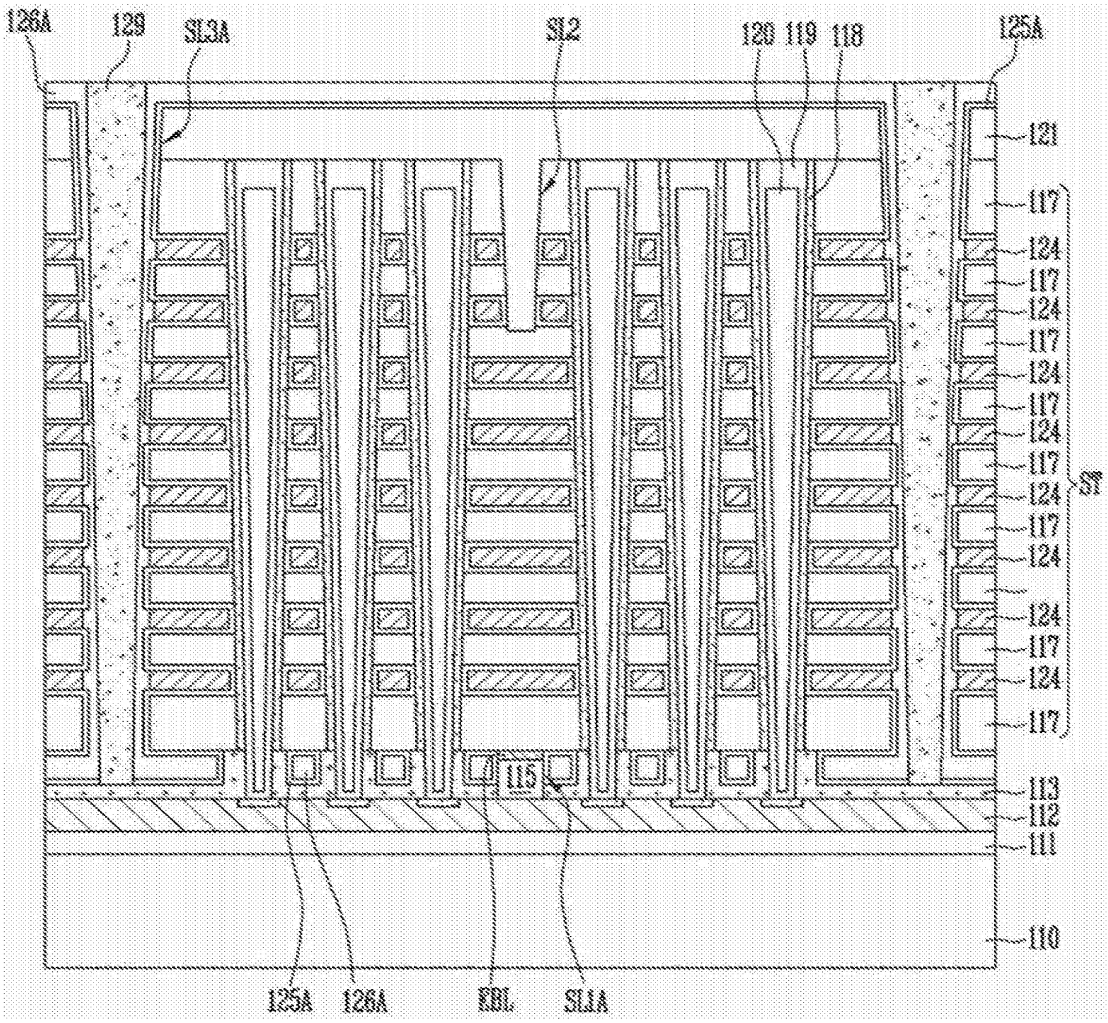


图 31

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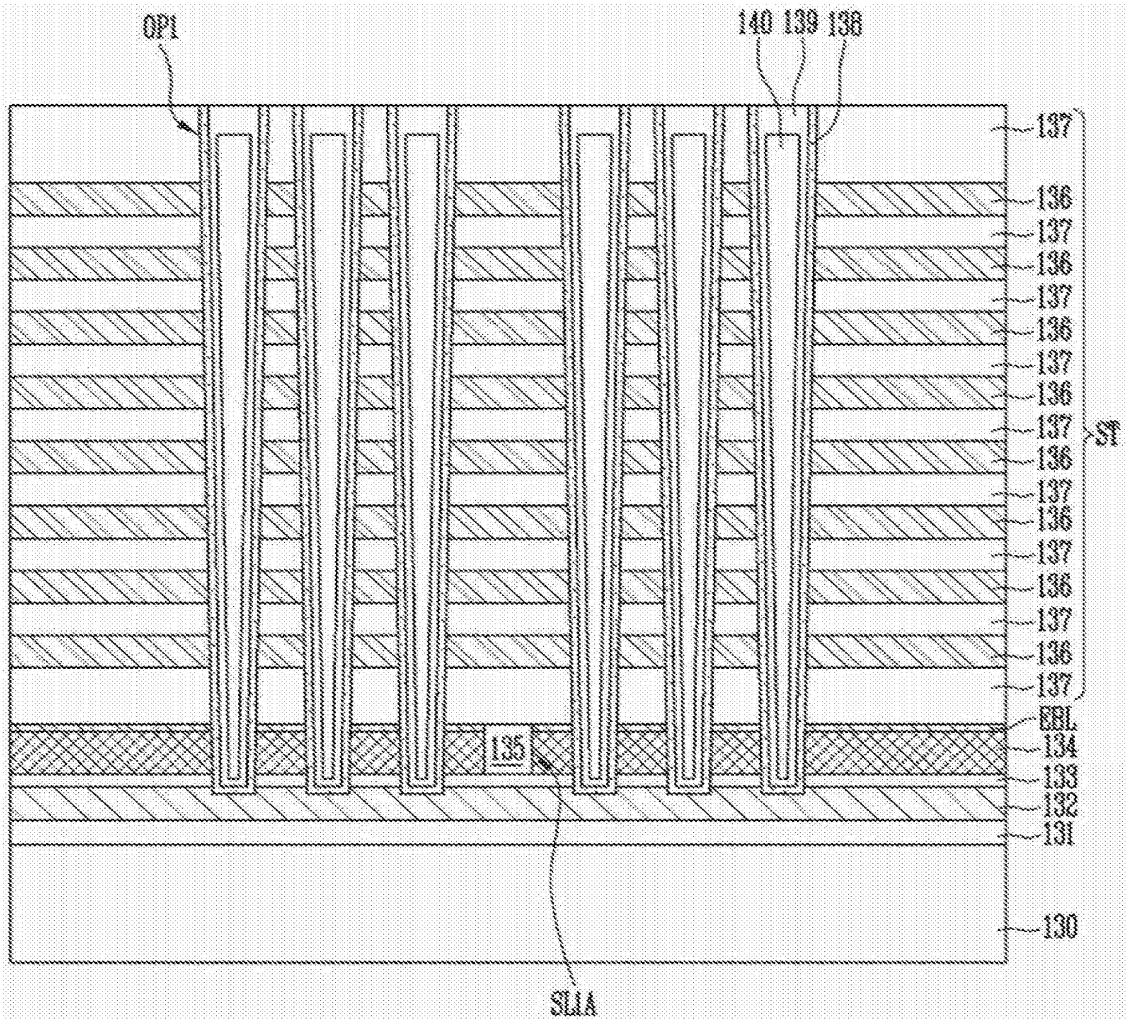


图 32

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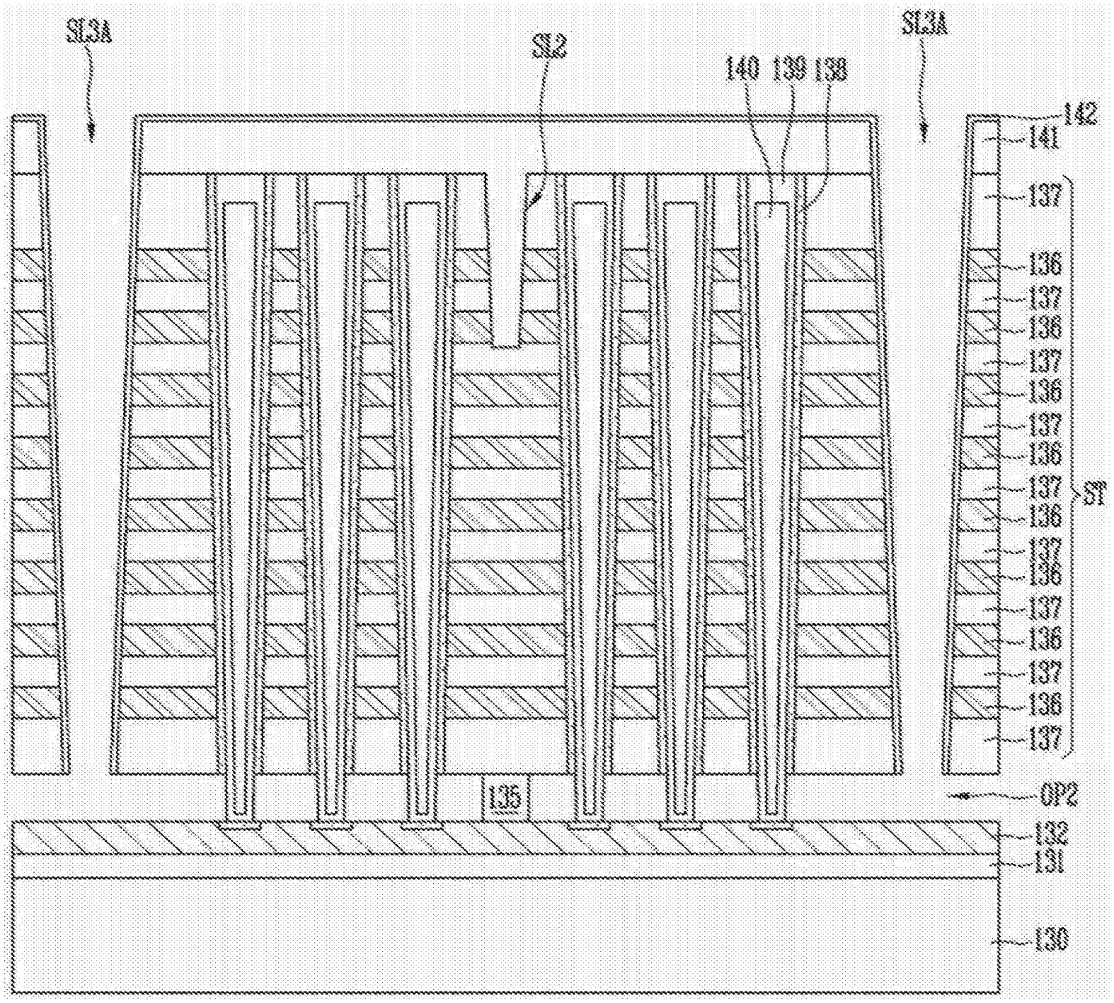


图 33

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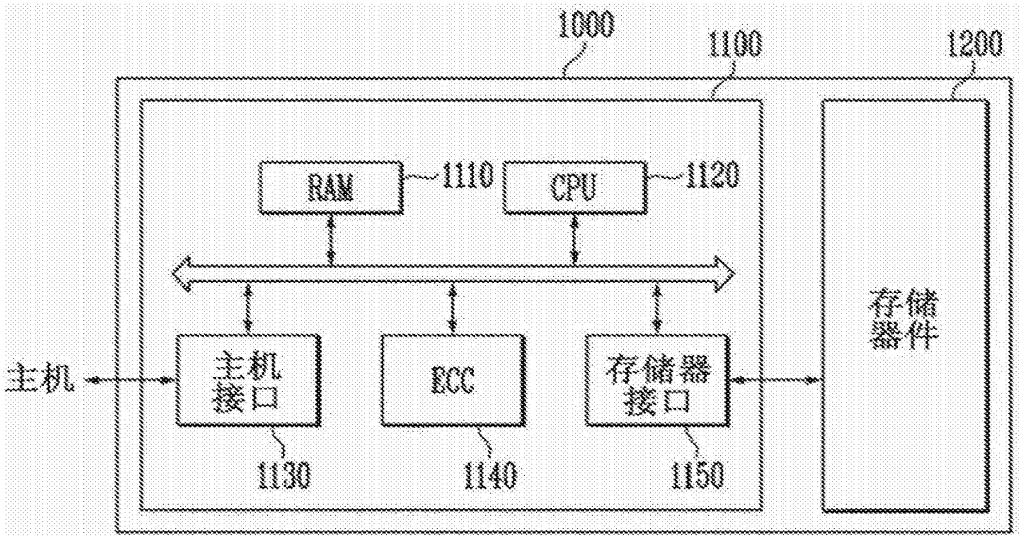


图 34

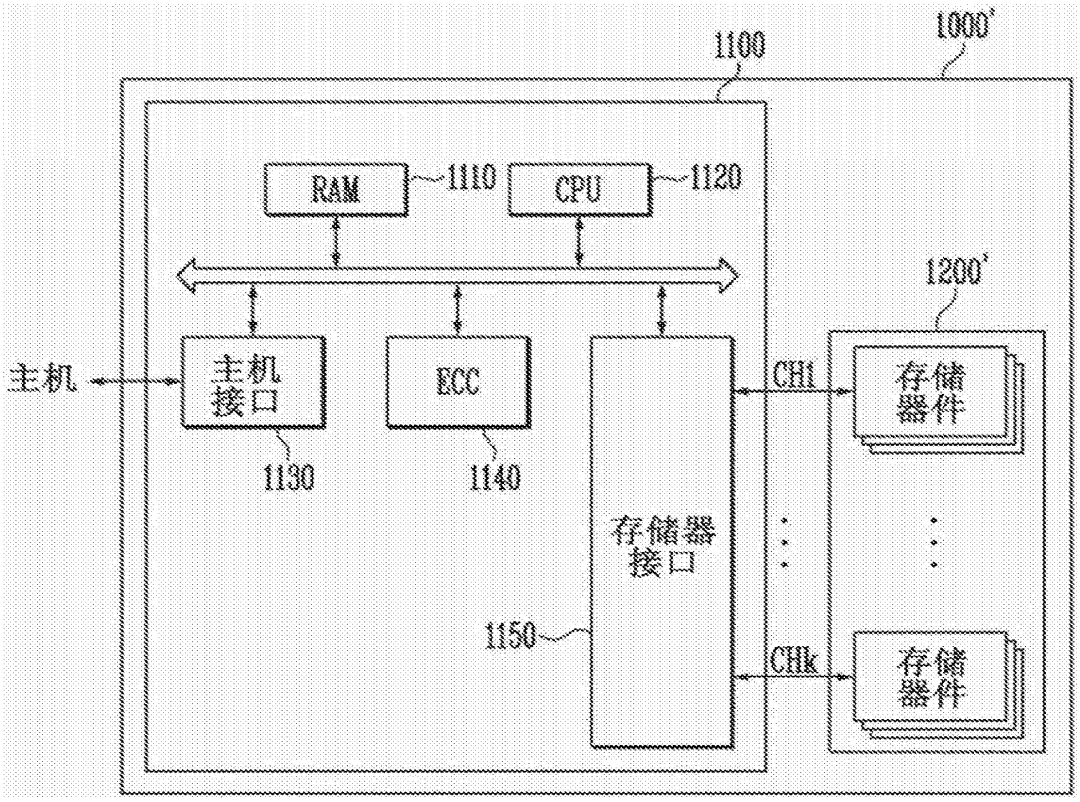


图 35

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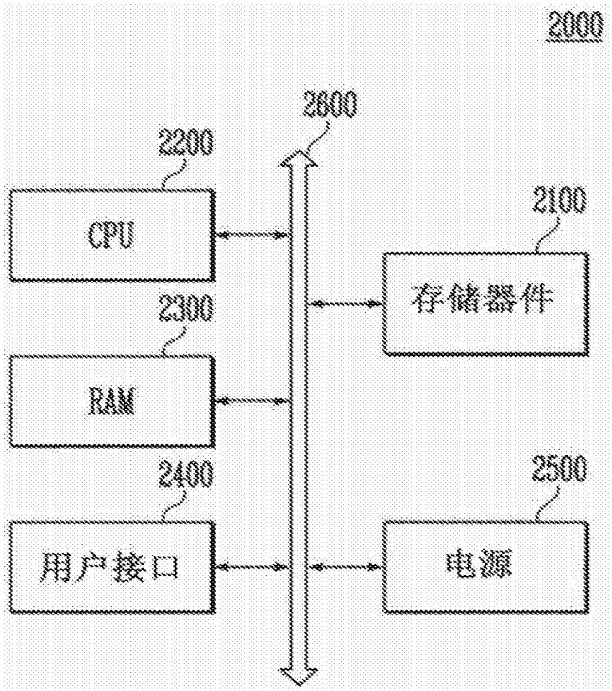


图 36

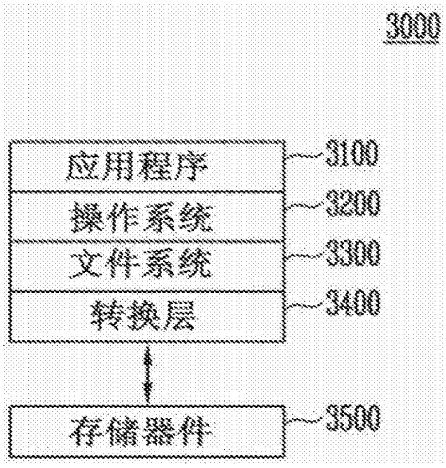


图 37

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(71) Applicant: **SANDISK TECHNOLOGIES LLC** [US/US]; Two Legacy Town Center, 6900 North Dallas Parkway, Plano, Texas 75024 (US).

(72) Inventors: **NISHIKAWA, Masatoshi**; c/o SanDisk Corporation, 951 SanDisk Drive, Milpitas, California 95035 (US). **HONMA, Ryoichi**; c/o SanDisk Corporation, 951 SanDisk Drive, Milpitas, 95035 (US). **MIWA, Toru**; c/o SanDisk Corporation, 951 SanDisk Drive, Milpitas, California 95035 (US). **MATSUMOTO, Masahide**; c/o SanDisk Corporation, 951 SanDisk Drive, Milpitas, California 95035 (US). **MIZUTANI, Yuki**; c/o SanDisk Corporation, 951 SanDisk Drive, Milpitas, California 95035 (US). **KOKETSU, Hiroaki**; c/o SanDisk Corporation, 951 SanDisk Drive, Milpitas, California 95035 (US). **ALSMEIER, Johann**; c/o SanDisk Corporation, 951 SanDisk Drive, Milpitas, California 95035 (US).

(74) Agents: **RADOMSKY, Leon** et al.; 11800 Sunrise Valley Drive, Suite 1500, Reston, Virginia 20191 (US).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

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[Continued on next page]

(54) Title: PASSIVE DEVICES FOR INTEGRATION WITH THREE-DIMENSIONAL MEMORY DEVICES

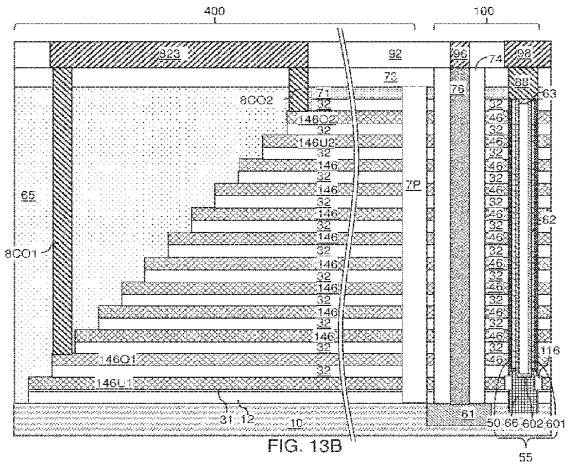


FIG. 13B

(57) Abstract: A three dimensional memory device includes a memory device region containing a plurality of non-volatile memory devices, a peripheral device region containing active driver circuit devices, and a stepped surface region between the peripheral device region and the memory device region containing a plurality of passive driver circuit devices.

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— *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))*

Published:

— *without international search report and to be republished upon receipt of that report (Rule 48.2(g))*

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PASSIVE DEVICES FOR INTEGRATION WITH THREE-DIMENSIONAL MEMORY DEVICES

CROSS REFERENCE TO RELATED APPLICATION

[0001] This application claims the benefit of priority to U.S. Non-Provisional Application Serial Nos. 14/739,284, filed June 15, 2015 and 14/739,354, filed June 15, 2015, the entire content of the foregoing applications are incorporated herein by reference.

FIELD

[0002] The present disclosure relates generally to the field of semiconductor devices and specifically to passive devices that are compatible with three-dimensional memory devices and methods of making thereof.

BACKGROUND

[0003] Passive devices refer to devices that provide an output with, or without, a phase change in linear proportion to a sinusoidal electrical input. Passive devices do not have the ability to switch on, or off, the output. Passive devices include, for example, resistors, capacitors, and inductors. Semiconductor circuits routinely employ passive devices in addition to active devices such as transistors.

SUMMARY

[0004] According to an aspect of the present disclosure a three dimensional memory device is provided, comprising a memory device region containing a plurality of non-volatile memory devices, a peripheral device region containing active driver circuit devices, and a first stepped surface region between the peripheral device region and the memory device region containing a plurality of passive driver circuit devices. According to another aspect of

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the present disclosure, a device comprising a set of capacitors is provided, the device comprising a stack of alternating layers including electrically insulating layers and electrically conductive layers located over a substrate, wherein each underlying electrically conductive layer that is located within the stack and has at least one overlying electrically conductive layer that laterally extends farther than the underlying electrically conductive layer to form a stepped surface region on a side of the stack, and a dielectric material portion located over the stepped surface region of the stack, wherein an interface between the dielectric material portion and the stack includes a contiguous set of horizontal surfaces and vertical surfaces to provide the stepped surface region. The device further comprises a set of dielectric fill material portions located within trenches that vertically extend through the stack of alternating layers and laterally contact sidewalls of the stack of alternating layers in the stepped surface region and a plurality of contact via structures in contact with respective electrically conductive layers within the stack of alternating layers. The electrically conductive layers constitute conductive components of a set of capacitors and a subset of the electrically insulating layers constitutes node dielectrics of the set of capacitors, Each capacitor in the set comprises a first node that includes an underlying electrically conductive layer of a respective vertically neighboring pair and a respective contact via structure that extends upward from the underlying electrically conductive layer and through the dielectric material portion, and a second node that includes an overlying electrically conductive layer of the respective vertically neighboring pair and a respective contact via structure that extends upward from the overlying electrically conductive layer and through the dielectric material portion.

[0005] According to another aspect of the present disclosure a method of forming a memory device comprises forming a plurality of memory devices in a memory device region;

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forming a plurality of passive devices outside the memory device region, and forming a conductive layer in one deposition step such that a first portion of the conductive layer comprises a portion of at least one of the passive device and a second portion of the conductive layer forms a portion of at least one memory device.

[0006] According to yet another aspect of the present disclosure, a semiconductor device is provided, comprising an alternating stack of first material layers and second material layers located over a substrate, at least one pillar structure extending from a first horizontal plane including a top surface of the alternating stack through at least a portion of the alternating stack, a laterally-extending semiconductor or conductive structure contacting a bottom surface of the at least one pillar structure, and a contact via structure contacting a top surface of the laterally-extending semiconductor or conductive structure and laterally spaced from the at least one pillar structure. Each of the at least one pillar structure comprises at least one doped semiconductor material portion therein, and each semiconductor material portion within the at least one pillar structure has a doping of a same second conductivity type.

[0007] According to still another aspect of the present disclosure a method of forming at least one resistor structure comprises forming an alternating stack of first material layers and second material layers over a substrate, and forming at least one vertically-extending cavity from a first horizontal plane including a top surface of the alternating stack to a laterally-extending semiconductor or conductive structure. A physically exposed portion of a top surface of the laterally-extending semiconductor or conductive structure is present within a second horizontal plane located in the alternating stack below the first horizontal plane. The method further comprises forming a resistor comprising a pillar structure within each of the at least one vertically-extending cavity, wherein each pillar structure comprises at least one doped semiconductor material portion, and wherein each semiconductor material within the

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pillar structure has a doping of a same second conductivity type, and forming a contact via structure contacting another portion of the top surface of the laterally-extending semiconductor or conductive structure.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] FIG. 1 is a vertical cross-sectional view of a first exemplary structure after formation of a stack of an alternating plurality of first material layers and second material layers according to a first embodiment of the present disclosure.

[0009] FIG. 2 is a vertical cross-sectional view of the first exemplary structure after formation of memory stack structures and an insulating cap layer according to the first embodiment of the present disclosure.

[0010] FIG. 3 is a vertical cross-sectional view of the first exemplary structure after formation of an optional dielectric material portion according to the first embodiment of the present disclosure.

[0011] FIG. 4 is a vertical cross-sectional view of the first exemplary structure during formation of stepped surfaces according to the first embodiment of the present disclosure.

[0012] FIG. 5A is a vertical cross-sectional view of the first exemplary structure after formation of stepped surfaces according to the first embodiment of the present disclosure.

[0013] FIG. 5B is a top-down view of the first exemplary structure of FIG. 5A.

[0014] FIG. 6A is a vertical cross-sectional view of the first exemplary structure after formation of a retro-stepped dielectric material portion and dielectric pillar structures according to the first embodiment of the present disclosure.

[0015] FIG. 6B is a horizontal cross-sectional view of the first exemplary structure of FIG. 6A along the horizontal plane B – B'.

[0016] FIG. 7A is a vertical cross-sectional view of the first exemplary structure after

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formation of a backside contact trench according to the first embodiment of the present disclosure.

[0017] FIG. 7B is a horizontal cross-sectional view of the first exemplary structure of FIG. 7A along the plane B – B'. The vertical plane A – A' is the plane of vertical cross-sectional view of FIG. 7A.

[0018] FIG. 7C is a vertical cross-sectional view of the first exemplary structure of FIG. 8B along the vertical plane C – C'.

[0019] FIG. 7D is a top-down view of the first exemplary structure of FIGS. 7A – 7C.

[0020] FIG. 8A is a vertical cross-sectional view of the first exemplary structure after formation of lateral recesses according to the first embodiment of the present disclosure.

[0021] FIG. 8B is a horizontal cross-sectional view of the first exemplary structure of FIG. 8A along the plane B – B'. The vertical plane A – A' is the plane of vertical cross-sectional view of FIG. 8A.

[0022] FIG. 8C is a vertical cross-sectional view of the first exemplary structure of FIG. 7B along the vertical plane C – C'.

[0023] FIG. 9A is a vertical cross-sectional view of the first exemplary structure after formation of electrically conductive layers according to the first embodiment of the present disclosure.

[0024] FIG. 9B is a horizontal cross-sectional view of the first exemplary structure of FIG. 9A along the plane B – B'. The vertical plane A – A' is the plane of vertical cross-sectional view of FIG. 9A.

[0025] FIG. 10A is a vertical cross-sectional view of the first exemplary structure after removal of a metallic material from trenches according to the first embodiment of the present disclosure.

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[0026] FIG. 10B is a horizontal cross-sectional view of the first exemplary structure of FIG. 10A along the plane B – B'. The vertical plane A – A' is the plane of vertical cross-sectional view of FIG. 10A.

[0027] FIG. 11A is a vertical cross-sectional view of the first exemplary structure after formation of dielectric fill material portions and a backside contact via structure according to the first embodiment of the present disclosure.

[0028] FIG. 11B is a horizontal cross-sectional view of the first exemplary structure of FIG. 11A along the plane B – B'. The vertical plane A – A' is the plane of vertical cross-sectional view of FIG. 11A.

[0029] FIG. 12A is a vertical cross-sectional view of the first exemplary structure after formation of capacitor plate contact via structures and drain contact via structures according to the first embodiment of the present disclosure.

[0030] FIG. 12B is a horizontal cross-sectional view of the first exemplary structure of FIG. 12A along the plane B – B'. The vertical plane A – A' is the plane of vertical cross-sectional view of FIG. 12A.

[0031] FIG. 12C is a vertical cross-sectional view of the first exemplary structure of FIG. 12B along the vertical plane C – C'.

[0032] FIG. 12D is a top-down view of the first exemplary structure of FIGS. 12A – 12C.

[0033] FIG. 13A is a top-down view of the first exemplary structure after formation of a line level dielectric material layer and interconnect line structures according to the first embodiment of the present disclosure.

[0034] FIG. 13B is a vertical cross-sectional view of the first exemplary structure of FIG. 13A along the vertical plane B – B'.

[0035] FIG. 13C is a vertical cross-sectional view of the first exemplary structure of FIG.

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13A along the vertical plane C – C'.

[0036] FIG. 13D is a vertical cross-sectional view of the first exemplary structure of FIG. 13A along the vertical plane D – D'.

[0037] FIG. 13E is a vertical cross-sectional view of the first exemplary structure of FIG. 13A along the vertical plane E – E'.

[0038] FIGS. 14A and 14X are schematic top down views of devices of embodiments of the invention. FIGS. 14B, 14E, 14H, 14K, 14N, 14Q and 14T are top-down views of the alternative exemplary structures during fabrication steps of the device of FIG. 14X. FIGS. 14C, 14F, 14I, 14L, 14O, 14R and 14U are vertical cross-sectional views along respective lines C-C', F-F', I-I', L-L', O-O', R-R' and U-U' in FIGS. 14B, 14E, 14H, 14K, 14N, 14Q and 14T, respectively. FIGS. 14D, 14G, 14J, 14M, 14P, 14S and 14V are vertical cross-sectional views along respective lines D-D', G-G', J-J', M-M', P-P', S-S' and V-V' in FIGS. 14B, 14E, 14H, 14K, 14N, 14Q and 14T, respectively.

[0039] FIG. 14W is a resulting capacitor that includes adjacent electrode plates separated by an insulating layer, and respective electrical contacts (e.g., capacitor contact via structures) to the electrode plates.

[0040] FIGS. 14Y and 14Z are schematic top down views of capacitor interconnection schemes of embodiments of the invention.

[0041] FIG. 15A is a vertical cross-sectional view of a second exemplary structure after formation of a doped semiconductor well and an optional doped contact region according to a second embodiment of the present disclosure.

[0042] FIG. 15B is a vertical cross-sectional view of the second exemplary structure after formation of an alternating stack of first material layers and second material layers according to the second embodiment of the present disclosure.

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[0043] FIG. 16 is a vertical cross-sectional view of the second exemplary structure after formation of memory openings and vertically-extending cavities according to the second embodiment of the present disclosure.

[0044] FIG. 17 is a vertical cross-sectional view of the second exemplary structure after formation of memory stack structures and pillar structures according to the second embodiment of the present disclosure.

[0045] FIG. 18 is a vertical cross-sectional view of the second exemplary structure after implantation of dopants of a second conductivity type into the pillar structures according to the second embodiment of the present disclosure.

[0046] FIG. 19 is a vertical cross-sectional view of the second exemplary structure after formation of an optional insulating cap layer according to the second embodiment of the present disclosure.

[0047] FIG. 20 is a vertical cross-sectional view of the second exemplary structure after formation of a resistor contact trench according to the second embodiment of the present disclosure.

[0048] FIG. 21 is a vertical cross-sectional view of the second exemplary structure after formation of an insulating spacer and a substrate contact via structure according to the second embodiment of the present disclosure.

[0049] FIG. 22 is a vertical cross-sectional view of the second exemplary structure after formation of drain contact via structures, pillar contact via structures, and interconnect line structures according to the second embodiment of the present disclosure.

[0050] FIG. 23 is a vertical cross-sectional view of an alternate embodiment of the second exemplary structure according to the second embodiment of the present disclosure.

[0051] FIG. 24 is a vertical cross-sectional view of a third exemplary structure after

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replacement of first portions of second material layers with electrically conductive layers while maintaining second portions of the second material layers intact according to a third embodiment of the present disclosure.

[0052] FIG. 25 is a vertical cross-sectional view of the third exemplary structure after formation of drain contact via structures and a pillar contact line structure according to the third embodiment of the present disclosure.

[0053] FIG. 26 is a vertical cross-sectional view of the third exemplary structure after formation of a resistor contact trench according to the third embodiment of the present disclosure.

[0054] FIG. 27 is a vertical cross-sectional view of the third exemplary structure after formation of a substrate contact via structure according to the third embodiment of the present disclosure.

[0055] FIG. 28 is a vertical cross-sectional view of a fourth exemplary structure after formation of a dielectric material layer according to a fourth embodiment of the present disclosure.

[0056] FIG. 29A is a vertical cross-sectional view of the fourth exemplary structure after formation of a backside contact trench according to the fourth embodiment of the present disclosure.

[0057] FIG. 29B is a horizontal cross-sectional view of the fourth exemplary structure along the horizontal plane B – B' of FIG. 29A. The vertical plane A – A' is the plane of vertical cross-sectional view of FIG. 29A.

[0058] FIG. 29C is a vertical cross-sectional view of the first exemplary structure of FIG. 29B along the vertical plane C – C'.

[0059] FIG. 29D is a top-down view of the first exemplary structure of FIGS. 29A – 29C.

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[0060] FIG. 30A is a vertical cross-sectional view of the fourth exemplary structure after formation of electrically conductive layers according to the fourth embodiment of the present disclosure.

[0061] FIG. 30B is a horizontal cross-sectional view of the fourth exemplary structure of FIG. 30A along the plane B – B'. The vertical plane A – A' is the plane of vertical cross-sectional view of FIG. 30A.

[0062] FIG. 31A is a vertical cross-sectional view of the fourth exemplary structure after removal of a metallic material from trenches according to the fourth embodiment of the present disclosure.

[0063] FIG. 31B is a horizontal cross-sectional view of the fourth exemplary structure of FIG. 31A along the plane B – B'. The vertical plane A – A' is the plane of vertical cross-sectional view of FIG. 31A.

[0064] FIG. 32A is a vertical cross-sectional view of the fourth exemplary structure after formation of a backside insulating spacer and a backside contact via structure according to the fourth embodiment of the present disclosure.

[0065] FIG. 32B is a horizontal cross-sectional view of the fourth exemplary structure of FIG. 32A along the plane B – B'. The vertical plane A – A' is the plane of vertical cross-sectional view of FIG. 32A.

[0066] FIG. 33A is a vertical cross-sectional view of the fourth exemplary structure after formation of substrate contact via structures and drain contact via structures according to the fourth embodiment of the present disclosure.

[0067] FIG. 33B is a horizontal cross-sectional view of the fourth exemplary structure of FIG. 33A along the plane B – B'. The vertical plane A – A' is the plane of vertical cross-sectional view of FIG. 33A.

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[0068] FIG. 33C is a vertical cross-sectional view of the fourth exemplary structure of FIG. 33B along the vertical plane C – C'.

[0069] FIG. 33D is a top-down view of the fourth exemplary structure of FIGS. 33A – 33C.

[0070] FIG. 34A is a vertical cross-sectional view of the fourth exemplary structure after formation of vertically-extending cavities according to the fourth embodiment of the present disclosure.

[0071] FIG. 34B is a horizontal cross-sectional view of the fourth exemplary structure of FIG. 34A along the plane B – B'. The vertical plane A – A' is the plane of vertical cross-sectional view of FIG. 34A.

[0072] FIG. 34C is a vertical cross-sectional view of the fourth exemplary structure of FIG. 34B along the vertical plane C – C'.

[0073] FIG. 34D is a top-down view of the fourth exemplary structure of FIGS. 34A – 34C.

[0074] FIG. 35A is a vertical cross-sectional view of the fourth exemplary structure after formation of resistor pillar structures according to the fourth embodiment of the present disclosure.

[0075] FIG. 35B is a horizontal cross-sectional view of the fourth exemplary structure of FIG. 35A along the plane B – B'. The vertical plane A – A' is the plane of vertical cross-sectional view of FIG. 35A.

[0076] FIG. 35C is a vertical cross-sectional view of the fourth exemplary structure of FIG. 35B along the vertical plane C – C'.

[0077] FIG. 35D is a top-down view of the fourth exemplary structure of FIGS. 35A – 35C.

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[0078] FIG. 36A is a vertical cross-sectional view of the fourth exemplary structure after formation of interconnect line structures according to the fourth embodiment of the present disclosure.

[0079] FIG. 36B is a horizontal cross-sectional view of the fourth exemplary structure of FIG. 36A along the plane B – B'. The vertical plane A – A' is the plane of vertical cross-sectional view of FIG. 36A.

[0080] FIG. 36C is a vertical cross-sectional view of the fourth exemplary structure of FIG. 36B along the vertical plane C – C'. FIG. 36D is a top-down view of the fourth exemplary structure of FIGS. 36A – 36C.

[0081] FIG. 37 is a schematic top down view of devices of embodiments of the invention.

DETAILED DESCRIPTION

[0082] As discussed above, the present disclosure is directed to passive devices that are compatible with three-dimensional memory devices and methods of making thereof, the various aspects of which are described below. The embodiments of the disclosure can be employed to form various structures including a device structure, a non-limiting example of which includes capacitors and/or resistors that can be formed on a same substrate as additional semiconductor devices such as three-dimensional monolithic memory array devices comprising a plurality of NAND memory strings. The drawings are not drawn to scale. Multiple instances of an element may be duplicated where a single instance of the element is illustrated, unless absence of duplication of elements is expressly described or clearly indicated otherwise. Ordinals such as "first," "second," and "third" are employed merely to identify similar elements, and different ordinals may be employed across the specification and the claims of the instant disclosure. As used herein, a first element located "on" a second element can be located on the exterior side of a surface of the second element

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or on the interior side of the second element. As used herein, a first element is located "directly on" a second element if there exist a physical contact between a surface of the first element and a surface of the second element.

[0083] As used herein, a "layer" refers to a material portion including a region having a substantially uniform thickness. A layer may extend over the entirety of an underlying or overlying structure, or may have an extent less than the extent of an underlying or overlying structure. Further, a layer may be a region of a homogeneous or inhomogeneous contiguous structure that has a thickness less than the thickness of the contiguous structure. For example, a layer may be located between any pair of horizontal planes between, or at, a top surface and a bottom surface of the contiguous structure. A plane is horizontal when it is parallel to a flat portion of the top surface of the substrate. However, it should be understood that the substrate may be positioned at any angle with respect to the direction of gravity and that the term "horizontal" does not imply that a horizontal direction must be perpendicular to the direction of gravity. A layer may extend horizontally, vertically, and/or along a tapered surface. A substrate may be a layer, may include one or more layers therein, and/or may have one or more layer thereupon, thereabove, and/or therebelow.

[0084] A monolithic three dimensional memory array is one in which multiple memory levels are formed above a single substrate, such as a semiconductor wafer, with no intervening substrates. The term "monolithic" means that layers of each level of the array are directly deposited on the layers of each underlying level of the array. In contrast, two dimensional arrays may be formed separately and then packaged together to form a non-monolithic memory device. For example, non-monolithic stacked memories have been constructed by forming memory levels on separate substrates and vertically stacking the memory levels, as described in U.S. Patent No. 5,915,167 titled "Three Dimensional

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Structure Memory." The substrates may be thinned or removed from the memory levels before bonding, but as the memory levels are initially formed over separate substrates, such memories are not true monolithic three dimensional memory arrays. The various three dimensional memory devices of the present disclosure include a monolithic three-dimensional NAND string memory device, and can be fabricated employing the various embodiments described herein.

[0085] Referring to FIG. 1, a first exemplary structure according to a first embodiment of the present disclosure is illustrated, which can be employed, for example, to fabricate a device structure containing vertical NAND memory devices. The first exemplary structure includes a substrate, which can be a semiconductor substrate. The substrate can include a semiconductor material layer 10. The semiconductor material layer 10 can include at least one elemental semiconductor material, at least one III-V compound semiconductor material, at least one II-VI compound semiconductor material, at least one organic semiconductor material, or other semiconductor materials known in the art. The substrate can have a major surface 7, which can be, for example, a topmost surface of the semiconductor material layer 10. The major surface 7 can be a semiconductor surface. In one embodiment, the major surface 7 can be a single crystalline semiconductor surface.

[0086] As used herein, a "semiconductor material" refers to a material having electrical conductivity in the range from 1.0×10^{-6} S/cm to 1.0×10^{5} S/cm, and is capable of producing a doped material having electrical resistivity in a range from 1.0 S/cm to 1.0×10^{5} S/cm upon suitable doping with an electrical dopant. As used herein, an "electrical dopant" refers to a p-type dopant that adds a hole to a valence band within a band structure, or an n-type dopant that adds an electron to a conduction band within a band structure. As used herein, a "conductive material" refers to a material having electrical conductivity greater than 1.0×10^{5}

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S/cm. As used herein, an "insulator material" or a "dielectric material" refers to a material having electrical conductivity less than 1.0×10^{-6} S/cm. All measurements for electrical conductivities are made at the standard condition. Optionally, at least one doped well (not expressly shown) can be formed within the semiconductor material layer 10.

[0087] At least one semiconductor device (not shown) for a peripheral circuitry can be formed on a portion of the semiconductor material layer 10. The region in which the at least one semiconductor device for the peripheral circuitry is herein referred to as a peripheral device region. The at least one semiconductor device can include, for example, field effect transistors. The least one semiconductor device for the peripheral circuitry can contain a driver circuit for memory devices to be subsequently formed, which can include at least one NAND device.

[0088] Optionally, a dielectric pad layer 12 can be formed above the semiconductor material layer 10. The dielectric pad layer 12 can be, for example, silicon oxide layer. The thickness of the dielectric pad layer 12 can be in a range from 3 nm to 30 nm, although lesser and greater thicknesses can also be employed. A dielectric cap layer 31 can be optionally formed. The dielectric cap layer 31 includes a dielectric material such as silicon oxide, a dielectric metal oxide, and silicon nitride (in case the material of second material layers to be subsequently formed is not silicon nitride).

[0089] A stack of an alternating plurality of first material layers (which can be insulating layers 32) and second material layers (which can be sacrificial material layer 42) is formed over the top surface of the substrate, which can be, for example, on the top surface of the dielectric cap layer 31. As used herein, an alternating plurality of first elements and second elements refers to a structure in which instances of the first elements and instances of the second elements alternate. Each instance of the first elements that is not an end element of

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the alternating plurality is adjoined by two instances of the second elements on both sides, and each instance of the second elements that is not an end element of the alternating plurality is adjoined by two instances of the first elements on both ends. The first elements may have the same thickness thereamongst, or may have different thicknesses. The second elements may have the same thickness thereamongst, or may have different thicknesses. The alternating plurality of first material layers and second material layers may begin with an instance of the first material layers or with an instance of the second material layers, and may end with an instance of the first material layers or with an instance of the second material layers. In one embodiment, an instance of the first elements and an instance of the second elements may form a unit that is repeated with periodicity within the alternating plurality.

[0090] Each first material layer includes a first material, and each second material layer includes a second material that is different from the first material. In one embodiment, each first material layer can be an insulator layer 32, and each second material layer can be a sacrificial material layer 42. In this case, the stack can include an alternating plurality of insulator layers 32 and sacrificial material layers 42.

[0091] The stack of the alternating plurality is herein referred to as an alternating stack (32, 42). In one embodiment, the alternating stack (32, 42) can include insulator layers 32 composed of the first material, and sacrificial material layers 42 composed of a second material different from that of insulator layers 32. The first material of the insulator layers 32 can be at least one electrically insulating material. As such, each insulator layer 32 can be an electrically insulating material layer. Electrically insulating materials that can be employed for the insulator layers 32 include, but are not limited to silicon oxide (including doped or undoped silicate glass), silicon nitride, silicon oxynitride, organosilicate glass (OSG), spin-on dielectric materials, dielectric metal oxides that are commonly known as high

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dielectric constant (high-k) dielectric oxides (e.g., aluminum oxide, hafnium oxide, etc.) and silicates thereof, dielectric metal oxynitrides and silicates thereof, and organic insulating materials. In one embodiment, the first material of the insulator layers 32 can be silicon oxide.

[0092] The second material of the sacrificial material layers 42 is a sacrificial material that can be removed selective to the first material of the insulator layers 32. As used herein, a removal of a first material is "selective to" a second material if the removal process removes the first material at a rate that is at least twice the rate of removal of the second material. The ratio of the rate of removal of the first material to the rate of removal of the second material is herein referred to as a "selectivity" of the removal process for the first material with respect to the second material.

[0093] The sacrificial material layers 42 may comprise an electrically insulating material, a semiconductor material, or a conductive material. The second material of the sacrificial material layers 42 can be subsequently replaced with electrically conductive electrodes which can function, for example, as control gate electrodes of a vertical NAND device. Non-limiting examples of the second material include silicon nitride, an amorphous semiconductor material (such as amorphous silicon), and a polycrystalline semiconductor material (such as polysilicon). In one embodiment, the sacrificial material layers 42 can be material layers that comprise silicon nitride or a semiconductor material including at least one of silicon and germanium.

[0094] In one embodiment, the insulator layers 32 can include silicon oxide, and sacrificial material layers can include silicon nitride sacrificial material layers. The first material of the insulator layers 32 can be deposited, for example, by chemical vapor deposition (CVD). For example, if silicon oxide is employed for the insulator layers 32,

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tetraethyl orthosilicate (TEOS) can be employed as the precursor material for the CVD process. The second material of the sacrificial material layers 42 can be formed, for example, CVD or atomic layer deposition (ALD).

[0095] The sacrificial material layers 42 can be suitably patterned so that conductive material portions to be subsequently formed by replacement of the sacrificial material layers 42 can function as electrically conductive electrodes, such as the control gate electrodes of the monolithic three-dimensional NAND string memory devices to be subsequently formed. The sacrificial material layers 42 may comprise a portion having a strip shape extending substantially parallel to the major surface 7 of the substrate.

[0096] The thicknesses of the insulator layers 32 and the sacrificial material layers 42 can be in a range from 20 nm to 50 nm, although lesser and greater thicknesses can be employed for each insulator layer 32 and for each sacrificial material layer 42. The number of repetitions of the pairs of an insulator layer 32 and a sacrificial material layer (e.g., a control gate electrode or a sacrificial material layer) 42 can be in a range from 2 to 1,024, and typically from 8 to 256, although a greater number of repetitions can also be employed. The top and bottom gate electrodes in the stack may function as the select gate electrodes. In one embodiment, each sacrificial material layer 42 in the alternating stack (32, 42) can have a uniform thickness that is substantially invariant within each respective sacrificial material layer 42. The first exemplary structure may include a memory device region 100 in which an array of memory devices can be subsequently formed, and a capacitor region 400 in which at least one passive device can be subsequently formed.

[0097] Referring to FIG. 2, a lithographic material stack (not shown) including at least a photoresist layer can be formed over the alternating stack (32, 42), and can be lithographically patterned to form openings therein. The pattern in the lithographic material

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stack can be transferred through the entirety of the alternating stack (32, 42) by at least one anisotropic etch that employs the patterned lithographic material stack as an etch mask. Portions of the alternating stack (32, 42) underlying the openings in the patterned lithographic material stack are etched to form memory openings. In other words, the transfer of the pattern in the patterned lithographic material stack through the alternating stack (32, 42) forms the memory openings that extend through the alternating stack (32, 42). The chemistry of the anisotropic etch process employed to etch through the materials of the alternating stack (32, 42) can alternate to optimize etching of the first and second materials in the alternating stack (32, 42). The anisotropic etch can be, for example, a series of reactive ion etches. Optionally, the dielectric cap layer 31 may be used as an etch stop layer between the alternating stack (32, 42) and the substrate. The sidewalls of the memory openings can be substantially vertical, or can be tapered. The patterned lithographic material stack can be subsequently removed, for example, by ashing. The memory openings can be formed in the memory device region 100.

[0098] The memory openings are formed through the dielectric cap layer 31 and the dielectric pad layer 12 so that the memory openings extend from the top surface of the alternating stack (32, 42) to the top surface of the semiconductor material layer 10. In one embodiment, an overetch into the semiconductor material layer 10 may be optionally performed after the top surface of the semiconductor material layer 10 is physically exposed at a bottom of each memory openings. The overetch may be performed prior to, or after, removal of the lithographic material stack. In other words, the recessed surfaces of the semiconductor material layer 10 may be vertically offset from the undressed top surfaces of the semiconductor material layer 10 by a recess depth. The recess depth can be, for example, in a range from 1 nm to 50 nm, although lesser and greater recess depths can also be

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employed. The overetch is optional, and may be omitted. If the overetch is not performed, the bottom surface of each memory openings can be coplanar with the topmost surface of the semiconductor material layer 10. Each of the memory openings can include a sidewall (or a plurality of sidewalls) that extends substantially perpendicular to the topmost surface of the substrate. The region in which the array of memory openings is formed is herein referred to as a device region.

[0099] A memory stack structure 55 can be formed within each memory opening through the alternating stack (32, 42). The memory stack structures 55 can be formed, for example, by forming an optional epitaxial channel portion 66 at a bottom portion of each memory opening by selectively depositing a semiconductor material that is intrinsic or has a doping of a same conductivity type as the semiconductor material layer 10. Alternatively, portion 66 may be omitted or replaced by a trench in layer 10. A memory film layer is deposited in the memory openings over the alternating stack (32, 42) by a series of conformal deposition processes. The memory film layer can be a stack of contiguous material layers that overlie the entirety of the alternating stack (31, 42,). The memory film layer contacts all sidewall surface(s) and all bottom surface(s) of the memory openings. The memory film layer is a contiguous film stack that provides the functionality of charge storage in the absence of an external electrical bias voltage, while enabling charge transfer in the presence of a suitable external electrical bias voltage.

[00100] In one embodiment, the memory film layer can be a stack, in the order of formation, of a blocking dielectric layer, a charge storage layer, and a tunnel dielectric layer. In one embodiment, a plurality of floating gates or a charge storage dielectric can be located between the tunneling dielectric layer and the blocking dielectric layer.

[0100] The blocking dielectric layer contacts the sidewalls of the memory openings.

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Specifically, the blocking dielectric layer can contact the sidewalls of the sacrificial layers 42. The blocking dielectric layer may include one or more dielectric material layers that can function as the control gate dielectrics for control gate electrodes to be subsequently formed. The blocking dielectric layer can include silicon oxide, a dielectric metal oxide, a dielectric metal oxynitride, or a combination thereof. In one embodiment, the blocking dielectric layer can include a stack of at least one silicon oxide layer and at least one dielectric metal oxide layer. The blocking dielectric layer can be formed by a conformal deposition process such as chemical vapor deposition (CVD) and/or atomic layer deposition (ALD), and/or by deposition of a conformal material layer (such as an amorphous silicon layer) and subsequent conversion of the conformal material layer into a dielectric material layer (such as a silicon oxide layer). The thickness of the blocking dielectric layer can be in a range from 6 nm to 24 nm, although lesser and greater thicknesses can also be employed. Alternatively, the blocking dielectric layer may be omitted from the memory opening, and instead be formed through the backside contact trench in recesses formed by removal of the sacrificial layers 42 prior to forming the metal control gate electrodes through a backside contact trench.

[0101] The charge storage layer includes a dielectric charge trapping material, which can be, for example, silicon nitride, or a conductive material such as doped polysilicon or a metallic material. In one embodiment, the charge storage layer includes silicon nitride. The charge storage layer can be formed as a single charge storage layer of homogeneous composition, or can include a stack of multiple charge storage material layers. The multiple charge storage material layers, if employed, can comprise a plurality of spaced-apart floating gate material layers that contain conductive materials (e.g., metal such as tungsten, molybdenum, tantalum, titanium, platinum, ruthenium, and alloys thereof, or a metal silicide such as tungsten silicide, molybdenum silicide, tantalum silicide, titanium silicide, nickel

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silicide, cobalt silicide, or a combination thereof) and/or semiconductor materials (e.g., polycrystalline or amorphous semiconductor material including at least one elemental semiconductor element or at least one compound semiconductor material). Alternatively or additionally, the charge storage layer may comprise an insulating charge trapping material, such as one or more silicon nitride segments. Alternatively, the charge storage layer may comprise conductive nanoparticles such as metal nanoparticles, which can be, for example, ruthenium nanoparticles. The charge storage layer can be formed, for example, by chemical vapor deposition (CVD), atomic layer deposition (ALD), physical vapor deposition (PVD), or any suitable deposition technique for the selected material(s) for the charge storage layer. The thickness of the charge storage layer can be in a range from 2 nm to 20 nm, although lesser and greater thicknesses can also be employed.

[0102] The tunnel dielectric layer includes a dielectric material through which charge tunneling can be performed under suitable electrical bias conditions. The charge tunneling may be performed through hot-carrier injection or by Fowler-Nordheim tunneling induced charge transfer depending on the mode of operation of the monolithic three-dimensional NAND string memory device to be formed. The tunneling dielectric layer can include silicon oxide, silicon nitride, silicon oxynitride, dielectric metal oxides (such as aluminum oxide and hafnium oxide), dielectric metal oxynitride, dielectric metal silicates, alloys thereof, and/or combinations thereof. In one embodiment, the tunneling dielectric layer can include a stack of a first silicon oxide layer, a silicon oxynitride layer, and a second silicon oxide layer, which is commonly known as an ONO stack. In one embodiment, the tunneling dielectric layer can include a silicon oxide layer that is substantially free of carbon or a silicon oxynitride layer that is substantially free of carbon. The thickness of the tunnel dielectric layer can be in a range from 2 nm to 20 nm, although lesser and greater thicknesses can also

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be employed.

[0103] Optionally, a permanent channel material layer (such as a polysilicon layer) and/or a sacrificial layer (such as a dielectric material layer) may be formed on the memory film layer. The memory film layer (and any additional layer such as a permanent channel material layer or a sacrificial layer) can be anisotropically etched so that horizontal portions of the memory film layer (and any additional layer) are removed from above the top surface of the alternating stack (32, 42) and at the bottom of each memory opening. Each remaining vertical portion of the memory film layer that remains within a memory opening after the anisotropic etch constitutes a memory film 50. Each memory film 50 can be homeomorphic to a torus. As used herein, an element is homeomorphic to a geometrical shape if the shape of the element can be mapped to the geometrical shape by continuous deformation without creation or destruction of any hole. If an electrode underlies the memory openings, a top surface of the electrode can be physically exposed within the cavity defined by the inner sidewalls of an overlying memory film 50.

[0104] In one embodiment, a first semiconductor channel layer can be deposited directly on the surfaces of the tunnel dielectric layer as a permanent channel material layer by a conformal deposition method such as chemical vapor deposition (CVD). The first semiconductor channel layer and the memory films can be anisotropically etched to form an opening at a bottom portion of each memory opening. A top surface of the substrate semiconductor layer 10 is physically exposed at the bottom of each memory opening. Each remaining portion of the first semiconductor channel layer within a memory opening constitutes a first semiconductor channel portion 601.

[0105] After formation of a memory film 50 and a first semiconductor channel portion 601 within each memory opening, a second semiconductor channel layer can be deposited on

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the sidewalls of the first semiconductor channel portions 601, physically exposed surfaces of the substrate semiconductor layer 10 within the memory openings, and over the alternating stack (32, 42). The semiconductor material of the second semiconductor channel layer can include a doped polycrystalline semiconductor material (such as doped polysilicon), or can include a doped amorphous semiconductor material (such as amorphous silicon) that can be subsequently converted into a doped polycrystalline semiconductor material after a suitable anneal at an elevated temperature.

[0106] Optionally, a dielectric core 62 can be formed within a cavity inside each semiconductor channel 60, for example, by deposition of a dielectric material such as silicon oxide, and subsequent planarization of the dielectric material. The planarization of the dielectric material removes the portion of the deposited dielectric material from above the top surface of the horizontal plane including the top surface of the topmost layer of the alternating stack (32, 42), which can be, for example, the top surface of the topmost insulator layer 32. The planarization of the dielectric material can be performed, for example, by chemical mechanical planarization. Each remaining portion of the dielectric material inside a memory opening constitutes a dielectric core 62. The dielectric core 62 is an optional component, and a combination of a memory film 50 and a semiconductor channel 60 may completely fill a memory opening

[0107] The horizontal portion of the second semiconductor channel layer above the top surface of the topmost layer of the alternating stack (32, 42) can be removed, for example, by a recess etch. Each remaining portion of the second semiconductor channel layer constitutes a second semiconductor channel 602. Each adjoined pair of a first semiconductor channel 601 and a second semiconductor channel 602 vertically extend through the alternating stack (32, 42), and optional pillar collectively constitutes a portion of a semiconductor channel 60

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for a memory stack structure 55. A set of a memory film 50 and a semiconductor channel 60 within a same memory opening constitutes a memory stack structure 55.

[0108] Drain regions 63 can be formed by recessing a top portion of each dielectric core and depositing a doped semiconductor material. The doped semiconductor material can be, for example, doped polysilicon. The drain regions 63 can have a doping of a second conductivity type, which is the opposite of the first conductivity type (that is the conductivity type of the semiconductor material layer 10). Excess portions of the deposited semiconductor material can be removed from above the top surface of the alternating stack (32, 42), for example, by chemical mechanical planarization (CMP) or a recess etch.

[0109] Optionally, an insulating cap layer 71 can be formed over the alternating stack (32, 42) and the array of memory stack structures 55. The insulating cap layer 71 can include a dielectric material such as silicon oxide, a dielectric metal oxide, and/or a nitrogen-doped organosilicate glass. The thickness of the insulating cap layer 71 can be in a range from 5 nm to 100 nm, although lesser and greater thicknesses can also be employed.

[0110] Referring to FIG. 3, a portion of the alternating stack (32, 42) can be removed, for example, by applying and patterning a photoresist layer (not shown), and by transferring the pattern of the photoresist layer through the alternating stack (32, 42) employing an etch such as an anisotropic etch. A trench extending through the entire thickness of the alternating stack (32, 42) can be formed. Subsequently, the trench can be filled with an optional dielectric material such as silicon oxide to form a dielectric material portion 64. Excess portions of the dielectric material can be removed from above the top surface of the insulating cap layer 71 by a planarization process such as chemical mechanical planarization and/or a recess etch. The top surfaces of the insulating cap layer 71 can be employed as a stopping surface during the planarization. A top surface of the dielectric material portion 64

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can be coplanar with a top surface of the insulating cap layer 71.

[0111] Referring to FIG. 4, a trimming material layer 67 is formed and patterned over the insulating cap layer 71. The trimming material layer 67 comprises a material that can be continually trimmed, i.e., a material that can be gradually removed over a time duration from outside to inside at a controlled removal rate. For example, the trimming material layer 67 can be selected from a photoresist material, an organic polymer material, and an inorganic polymer material. Organic polymer materials that can be employed for the trimming material layer 67 can be an organic material made of cross-linked carbon-containing monomers, and can be carbon-based self-planarizing material known in the art. Inorganic polymer material that can be employed for the trimming material layer 67 include silicon-based polymer materials such as silicon-based antireflective coating materials as known in the art. A portion of the trimming material layer 67 remains after repeated trimming that shifts an outer sidewall of the trimming material layer 67 to a periphery of the capacitor region 400 adjoining the memory device region 100.

[0112] Portions of the insulating cap layer 71 and a topmost insulator layer 32 within the area of an opening in the trimming material layer 67 can be removed by an anisotropic etch. The last step of the anisotropic etch can be selective to the material of the sacrificial material layer 42 to minimize an overetch into the topmost sacrificial material layer 42. A recess cavity is formed at the levels of the insulating cap layer 71 and the topmost insulator layer 32 within the area of the opening in the trimming material layer 67.

[0113] Subsequently, a set of process steps is repeatedly performed to form stepped surfaces in the capacitor region 400. Each set of processing steps can include a first processing step of trimming the trimming material layer 67 to widen the opening in the trimming material layer 67, a second processing step of anisotropically etching the material

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of the sacrificial material layers 42 (with or without collateral etching of the material of the insulating cap layer 71) within the opening in the trimming material layer 67, a third step of anisotropically etching any remaining portion of the insulating cap layer 71 and the material of the insulator layers 32 within the opening in the trimming material layer 67. In one embodiment, an anisotropic etch process employed in the second processing step can be selective to the material of the insulator layers 32, and the anisotropic etch employed in the third processing step can be selective to the material of the sacrificial material layers 42.

[0114] Referring to FIGS. 5A and 5B, the set of processing steps is repeated performed until the bottommost sacrificial material layer 42 is patterned. Optionally, the dielectric cap layer 31 and the dielectric pad layer 12 may be patterned with the same pattern as the bottommost sacrificial material layer 42. The trimming material layer 67 can be subsequently removed, for example, by ashing.

[0115] A stepped surface region is formed in the capacitor region 400. As used herein, a "stepped surface region" refers to a region in which stepped surfaces are present. As used herein, "stepped surfaces" refer to a set of surfaces that include at least two horizontal surfaces and at least two vertical surfaces such that each horizontal surface is adjoined to a first vertical surface that extends upward from a first edge of the horizontal surface, and is adjoined to a second vertical surface that extends downward from a second edge of the horizontal surface.

[0116] The cavity overlying the steppes surfaces is a stepped cavity. As used herein, a "stepped cavity" refers to a cavity having stepped surfaces. The stepped cavity 69 can straddle a remaining portion of the dielectric material portion 64 (not shown) and a remaining patterned portion of the alternating stack (32, 42). Within the stepped surface region, each underlying second material layer (such as a sacrificial material layer 42) laterally extends

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farther than any overlying second material layer, and each underlying first material layer (such as an insulator layer 32) laterally extends farther than any overlying first material layer. A vertically adjoining pair of a first material layer (such as an insulator layer 32) and a second material layer (such as a sacrificial material layer 42) can have vertically coincident sidewalls. As used herein, a first surface and a second surface are vertically coincident with each other if there exists a vertical plane including both the first surface and the second surface.

[0117] Referring to FIGS. 6A and 6B, a dielectric material portion (i.e., insulating fill material portion) can be formed in the stepped cavity 69 by deposition of a dielectric material such as silicon oxide. Excess portions of the deposited dielectric material can be removed from above the top surface of the insulating cap layer 71, for example, by chemical mechanical planarization (CMP). The remaining portion of the deposited dielectric material filling the stepped cavity 69 constitutes the dielectric material portion.

[0118] The dielectric material portion is retro-stepped, and is herein referred to as a retro-stepped dielectric material portion 65. As used herein, a "retro-stepped" element refers to an element that has stepped surfaces and a horizontal cross-sectional area that increases monotonically as a function of a vertical distance from a top surface of a substrate on which the element is present. The retro-stepped dielectric material portion 65 is formed over the stepped structure of the alternating stack (32, 42), and can have a planar top surface. If silicon oxide is employed for the retro-stepped dielectric material portion 65, the silicon oxide of the retro-stepped dielectric material portion 65 may, or may not, be doped with dopants such as B, P, and/or F. The horizontal cross-sectional area of the retro-stepped dielectric material portion 65 at a horizontal plane is not less than the horizontal cross-sectional area of the retro-stepped dielectric material portion 65 at any horizontal plane that is

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more proximal to the substrate (i.e., the semiconductor material layer 10).

[0119] At least one dielectric pillar structure 7P may be optionally formed through the retro-stepped dielectric material portion 65 and/or through the alternating stack (32, 42). Further, dielectric support pillar structures 7Q may be formed in the contact region, which provide support for the insulator layers 32 in subsequent processing steps, and especially, during replacement of sacrificial material layers with conductive material layers. The at least one dielectric pillar structure 7P and the dielectric support pillar structures 7Q can be formed, for example, by forming openings extending through the retro-stepped dielectric material portion 65 and/or through the alternating stack (32, 42) and at least to the top surface of the substrate 10, and by filling the openings with a dielectric fill material that is resistant to the etch chemistry to be employed to remove the sacrificial material layers 42. In one embodiment, the at least one dielectric pillar structure can include silicon oxide and/or a dielectric metal oxide such as aluminum oxide. In one embodiment, the portion of the dielectric material that is deposited over the insulating cap layer 71 concurrently with deposition of the at least one dielectric pillar structure 7P and the dielectric support pillar structures 7Q can be present over insulating cap layer 71 as a dielectric material layer 73. The dielectric material layer 73 and the at least one dielectric pillar structure 7P and the dielectric support pillar structures 7Q can be formed as a single contiguous structure of integral construction, i.e., without any material interface therebetween. In another embodiment, the portion of the dielectric material that is deposited over insulating cap layer 71 concurrently with deposition of the at least one dielectric pillar structure 7P and the dielectric support pillar structures 7Q can be removed, for example, by chemical mechanical planarization or a recess etch. In this case, the dielectric material layer 73 is not present, and the top surface of insulating cap layer 71 can be physically exposed.

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[0120] In this embodiment, the shape of the at least one dielectric pillar structure 7P can be such that the at least one dielectric pillar structure 7P physically isolates a first portion of the alternating stack (32, 42) located within the memory device region 100 from a second portion of the alternating stack (32, 42) located within the capacitor region 400. In one embodiment, a dielectric pillar structure 7P can be formed at a boundary between the memory device region 100 and the capacitor region 400. However, other pillar 7P shapes, such as cylindrical pillar shapes may be used as described below with respect to FIG. 14A of the alternative embodiment. The dielectric support pillar structures 7Q can be formed as an array of discrete dielectric support pillar structures so as to provide mechanical support to the structures in the contact region during subsequent processing steps.

[0121] FIGS. 7A – 7D, a photoresist layer (not shown) can be applied over the alternating stack (32, 42) and the retro-stepped dielectric material portion 65 and the optional dielectric material layer 73, and lithographically patterned to form openings therein. The pattern of the openings includes an opening in the memory device region 100 and a plurality of openings in the capacitor region 400. The pattern of the opening in the memory device region 100 is selected such that a lateral distance from the opening in the memory device region 100 to a group of memory stack structures 55 does not exceed a predefined distance, which is the distance of a lateral etch to be subsequently employed to form lateral recesses. The pattern of the openings in the capacitor region 400 is selected such that trenches to be subsequently formed within the area of the openings within the capacitor region 400 can divide the second portion of the alternating stack (32, 42) located within the capacitor region 400 into a plurality of physically disjoined alternating stacks (32, 42).

[0122] An anisotropic etch can be performed to etch through portions of the optional dielectric material layer 73, the optional insulating cap layer 71, the retro-stepped dielectric

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material portion 65, and the alternating stack (32, 42) that underlie the openings within the photoresist layer. A backside contact trench 79 is formed directly underneath the opening in the photoresist layer within the memory device region 100. A lateral separation trench 89 is formed directly underneath each opening in the photoresist layer within the capacitor region 400. The backside contact trench 79 and the lateral separation trenches 89 can extend from the top surface of the dielectric material layer 73 (or the material layer contacting the bottom surface of the photoresist layer in case a dielectric material layer 73 is not employed) at least to the top surface of the semiconductor material layer 10 in the substrate. The lateral separation trenches 89 divides the second portion of the alternating stack (32, 42) in the capacitor region 400 into a plurality of physically disjoined alternating stacks (32, 42) that are laterally spaced apart by the lateral separation trenches 89.

[0123] Each of the backside contact trench 79 and the lateral separation trenches 89 can be a line trench, i.e., a trench having a uniform width and extending along a lengthwise direction. The sidewalls of the backside contact trench 79 and the lateral separation trenches 89 may be vertical, or may be tapered. In one embodiment, the backside contact trench 79 may have a first trench width tw1, and the lateral separation trenches 89 may have a second trench width tw2 that is less than the first trench width tw1. In one embodiment, the first trench width tw1 can be in a range from 30 nm to 1,000 nm, and the second trench width w2 can be in a range from 20 nm to 500 nm, although lesser and greater trench widths can be employed for each of the backside contact trench 79 and the lateral separation trenches 89.

[0124] In one embodiment, a dielectric pillar structure 7P can extend along a first horizontal direction hd1, and the backside contact trench 79 can extend along the first horizontal direction hd1. The lateral separation trenches 89 can adjoin the dielectric pillar structure 7P such that a sidewall of each lateral separation trench 89 is a sidewall of the

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dielectric pillar structure 7P. The lateral separation trenches 89 can extend along a horizontal direction that is different from the first horizontal direction hd1, which is herein referred to as a second horizontal direction hd2. In one embodiment, the second horizontal direction hd2 can be perpendicular to the first horizontal direction hd1. In one embodiment, the lateral separation trenches 89 can laterally extend along a lateral direction that is perpendicular to the stepped surfaces within the stepped surface region. As used herein, a lateral direction that is perpendicular to the stepped surfaces refers to the lateral direction that is perpendicular to vertical surfaces within the stepped surfaces. In other words, the second horizontal direction hd2 can be perpendicular to the vertical surfaces (i.e., the sidewalls of the insulator layers 32 and the sacrificial material layers 42) of the stepped surfaces.

[0125] Each lateral separation trench 89 extends through the stack of alternating layers (32, 42) as embodied in multiple physically disjoined portions. Sidewalls of patterned portions of the stack of alternating layers (32, 42) are physically exposed within each lateral separation trench 89. The photoresist layer can be removed, for example, by ashing.

[0126] Referring to FIGS. 8A – 8C, an etchant that selectively etches the second material of the sacrificial material layers 42 with respect to the first material of the insulator layers 32 can be introduced into the backside contact trench 79 and the lateral separation trenches 89, for example, employing an isotropic etch process. Backside recesses (43, 143) are formed in volumes from which the sacrificial material layers 42 are removed. The removal of the second material of the sacrificial material layers 42 can be selective to the first material of the insulator layers 32, the material of the at least one dielectric support pillar 7P, the material of the retro-stepped dielectric material portion 65, the semiconductor material of the semiconductor material layer 10, and the material of the outermost layer of the memory films 50. In one embodiment, the sacrificial material layers 42 can include silicon nitride, and the

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materials of the insulator layers 32, the at least one dielectric support pillar 7P, and the retro-stepped dielectric material portion 65 can be selected from silicon oxide and dielectric metal oxides. In another embodiment, the sacrificial material layers 42 can include a semiconductor material such as polysilicon, and the materials of the insulator layers 32, the at least one dielectric support pillar 7P, and the retro-stepped dielectric material portion 65 can be selected from silicon oxide, silicon nitride, and dielectric metal oxides. In this case, the depth of the backside contact trench 79 can be modified so that the bottommost surface of the backside contact trench 79 is located within the dielectric pad layer 12, i.e., to avoid physical exposure of the top surface of the semiconductor substrate layer 10.

[0127] The etch process that removes the second material selective to the first material and the outermost layer of the memory films 50 can be a wet etch process employing a wet etch solution, or can be a gas phase (dry) etch process in which the etchant is introduced in a vapor phase into the backside contact trench 79. For example, if the sacrificial material layers 42 include silicon nitride, the etch process can be a wet etch process in which the exemplary structure is immersed within a wet etch tank including phosphoric acid, which etches silicon nitride selective to silicon oxide, silicon, and various other materials employed in the art. The at least one dielectric support pillar 7P, the retro-stepped dielectric material portion 65, and the memory stack structures 55 provide structural support while the backside recesses (43, 143) are present within volumes previously occupied by the sacrificial material layers 42.

[0128] Each backside recess (43, 143) can be a laterally-extending cavity having a lateral dimension that is greater than the vertical extent of the cavity. In other words, the lateral dimension of each backside recess (43, 143) can be greater than the height of the backside recess (43, 143). A plurality of backside recesses (43, 143) can be formed in the volumes

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from which the second material of the sacrificial material layers 42 is removed. The plurality of backside recesses (43, 143) include first backside recesses 43 that are formed within the memory device region 100 by introduction of the etchant through the backside contact trench 79, and second backside recesses that are formed within the capacitor region 400 by introduction of the etchant through the lateral separation trenches 89.

[0129] Each of the plurality of first backside recesses (43, 143) can extend substantially parallel to the top surface of the substrate 10. A backside recess (43, 143) can be vertically bounded by a top surface of an underlying insulator layer 32 and a bottom surface of an overlying insulator layer 32. In one embodiment, each backside recess (43, 143) can have a uniform height throughout.

[0130] The memory openings in which the memory stack structures 55 are formed are herein referred to as front side recesses or front side cavities in contrast with the first backside recesses 43. In one embodiment, the memory device region 100 comprises an array of monolithic three-dimensional NAND strings having a plurality of device levels disposed above the substrate 10. In this case, each first backside recess 43 can define a space for receiving a respective word line of the array of monolithic three-dimensional NAND strings.

[0131] The second lateral recesses 143 can be formed at each level of the sacrificial material layers 42 in the capacitor region 400. Each second lateral recess 143 can be adjoined to at least one of the lateral separation trenches 89. At least one set of second lateral recesses 143 can be laterally adjoined to a neighboring pair of lateral separation trenches 89. Thus, a stacked cavity structure is formed between each neighboring pair of lateral separation trenches 89 such that a set of second backside recesses 143 is interlaced with a set of insulator layers 32. In one embodiment, the lateral separation trenches 89 can be formed with a periodicity p. The lateral distance between neighboring pairs of the lateral separation

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trenches 89 can be uniform. In this case, the second backside recesses 143 within a stacked cavity structure (143, 32) between a neighboring pair of lateral separation trenches 89 can have the same lateral extent along the first horizontal direction hd1, and can have different lateral extents along the second horizontal direction hd2.

[0132] Physically exposed surface portions of epitaxial channel portions 66 and the semiconductor material layer 10 can be converted into dielectric material portions by thermal conversion and/or plasma conversion of the semiconductor materials into dielectric materials. For example, thermal conversion and/or plasma conversion can be employed to convert a surface portion of each epitaxial channel portion 66 into a dielectric spacer 116, and to convert a surface portion of the semiconductor material layer 10 underneath each backside contact trench 79 and trenches 89 into a sacrificial dielectric portion 616. In one embodiment, each dielectric spacer 116 can be topologically homeomorphic to a torus, i.e., generally ring-shaped. As used herein, an element is topologically homeomorphic to a torus if the shape of the element can be continuously stretched without destroying a hole or forming a new hole into the shape of a torus.

[0133] The dielectric spacers 116 include a dielectric material that includes the same semiconductor element as the epitaxial channel portions 66 and additionally includes at least one non-metallic element such as oxygen and/or nitrogen such that the material of the dielectric spacers 116 is a dielectric material. In one embodiment, the dielectric spacers 116 can include a dielectric oxide, a dielectric nitride, or a dielectric oxynitride of the semiconductor material of the epitaxial channel portions 66. Likewise, each sacrificial dielectric portion 616 includes a dielectric material that includes the same semiconductor element as the semiconductor material layer 10 and additionally includes at least one non-metallic element such as oxygen and/or nitrogen such that the material of the sacrificial

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dielectric portions 616 is a dielectric material. In one embodiment, the sacrificial dielectric portions 616 can include a dielectric oxide, a dielectric nitride, or a dielectric oxynitride of the semiconductor material of the semiconductor material layer 10.

[0134] Referring to FIGS. 9A and 9B, a backside blocking dielectric layer (not shown) including a dielectric material (such as aluminum oxide) can be formed in the backside recesses (43, 143) by a conformal deposition. At least one conductive material can be deposited in the plurality of backside recesses (43, 143), on the sidewalls of the backside contact trench 79 and trenches 89, and over the topmost layer of the first exemplary structure. The conductive material can be deposited by a conformal deposition method, which can be, for example, chemical vapor deposition (CVD), atomic layer deposition (ALD), electroless plating, electroplating, or a combination thereof. The conductive material can be an elemental metal, an intermetallic alloy of at least two elemental metals, a conductive nitride of at least one elemental metal, a conductive metal oxide, a conductive doped semiconductor material, a conductive metal-semiconductor alloy such as a metal silicide, alloys thereof, and combinations or stacks thereof. Non-limiting exemplary conductive materials that can be deposited in the plurality of backside recesses (43, 143) include tungsten, tungsten nitride, titanium, titanium nitride, tantalum, and tantalum nitride. In one embodiment, the conductive material can comprise a metal such as tungsten and/or metal nitride. In one embodiment, the conductive material for filling the plurality of backside recesses (43, 143) can be a combination of titanium nitride and tungsten. In one embodiment, the conductive material can be deposited by chemical vapor deposition. The second material layers 42 are replaced with conductive material portions.

[0135] A plurality of first electrically conductive layers 46 can be formed in the plurality of first backside recesses 43 in the memory device region. A plurality of second electrically

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conductive layers 146 can be formed in the plurality of second backside recesses 143. A contiguous conductive material layer 46L can be formed on the sidewalls of the backside contact trench 79 and over the topmost layer of the first exemplary structure. Thus, each sacrificial material layer 42 can be replaced with a first electrically conductive layer 46 in the memory device region 100 and a second electrically conductive layer 146 in the capacitor region 400. A backside cavity 79' is present in the portion of each backside contact trench 79 that is not filled with the contiguous conductive material layer 46L. A lateral separation cavity 89' is present in the portion of each lateral separation trench 89 that is not filled with the contiguous conductive material layer 46L.

[0136] In one embodiment, the thickness of the deposited conductive material can be selected that the lateral separation trenches 89 and the backside contact trench 79 are not completely filled with the contiguous conductive material layer 46L. In this case, a cavity (79', 89') is present within each of the lateral separation trenches 89 and the backside contact trench 79 after deposition of the conductive material. The contiguous conductive material layer 46L, the first electrically conductive layers 46, and the second electrically conductive layers 146 are formed as a single contiguous structure.

[0137] Referring to FIGS. 10A and 10B, the deposited conductive material of the contiguous conductive material layer 46L is etched back from the sidewalls of each backside contact trench 79, from the sidewalls of each lateral separation trench 89, and from the dielectric material layer 73, for example, by an isotropic etch. Each remaining portion of the deposited conductive material in the first backside recesses 43 constitutes a first electrically conductive layer 46. Each remaining portion of the deposited conductive material in the second backside recesses 143 constitutes a second electrically conductive layer 146. Each electrically conductive layer (46, 146) can be a conductive line structure.

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[0138] Each first electrically conductive layer 46 can function as a combination of a plurality of control gate electrodes and a word line electrically connecting, i.e., electrically shorting, the plurality of control gate electrodes. The plurality of control gate electrodes within each first electrically conductive layer 46 can include control gate electrodes located at the same level for the vertical memory devices including the memory stack structures 55. In other words, each first electrically conductive layer 46 can be a word line that functions as a common control gate electrode for the plurality of vertical memory devices.

[0139] A patterned stack comprising an alternating plurality of the first material layers (i.e., the insulator layers 32) and second electrically conductive layers 146 is formed in the capacitor region 400. The second electrically conductive layers 146 in the patterned stack (32, 146) are formed at each level of the second material layers (i.e., the sacrificial material layers 42).

[0140] Referring to FIGS. 11A – 11B, a dielectric material can be conformally deposited within the backside contact trench 79 and the lateral separation trenches 89. The dielectric material can include, for example, silicon oxide, silicon nitride, a dielectric metal oxide, or a combination thereof. In one embodiment, the dielectric material can comprise silicon oxide.

[0141] In one embodiment, the lateral separation trenches 89 can be completely filled with the dielectric material to form trench fill dielectric material portions 84, while the backside contact trench 79 is not completely filled with the dielectric material. In other words, a backside cavity can be present within the portions of the deposited dielectric material within the backside contact trench 79.

[0142] An anisotropic etch can be performed to remove horizontal portions of the deposited dielectric material from above the dielectric material layer 73. A contiguous remaining vertical portion of the deposited dielectric material within the backside contact

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trench 79 constitutes an insulating spacer 74. The insulating spacer 74 comprises the same dielectric material as the form trench fill dielectric material portions 84. In one embodiment, the trench fill dielectric material portions 84 can have a same width throughout, and the insulating spacer 74 has a lateral thickness, as measured on the sidewalls of the backside contact trench 79, that is greater than one half of the width of the trench fill dielectric material portions 84. A remaining annular portion of the sacrificial dielectric portions 616 can be incorporated into a bottom portion of the insulating spacer 74.

[0143] Electrical dopants (p-type dopants or n-type dopants) can be implanted into portions of the semiconductor material layer 10 that underlies the backside cavity within the backside contact trench 79. In one embodiment, the conductivity type of the implanted dopants can be the opposite of the conductivity type of the semiconductor material layer 10. The implanted portion of the semiconductor material layer 10 can function as a source region 61 for the memory stack structures 55, and a surface portion of the semiconductor material layer 10 between the source region 61 and the epitaxial channel portions 66 can be a horizontal channel portion. In one embodiment, the semiconductor material layer 10 can have a doping of a first conductivity type, and the source region 61 can have a doping of a second conductivity type that is the opposite of the first conductivity type.

[0144] The backside cavity surrounded by an insulating spacer 74 can be filled with a conductive material to form a backside contact via structure 76. The backside contact via structure 76 can be electrically shorted to a portion of the substrate (10, 61), which can be the source region 61. The backside contact via strcuture76 extends through, and is laterally surrounded by, the insulating spacer 74.

[0145] The patterned stack comprising an alternating plurality of the first material layers (i.e., the insulator layers 32) and second electrically conductive layers 146 in the capacitor

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region 400 is laterally contacted by dielectric material fill portions on all sides. Specifically, the patterned stack (32, 146) is laterally contacted by a set of dielectric fill material portions (7P, 84, 65) formed within trenches. In one embodiment, each trench laterally surrounding an alternating stack of insulator layers 32 and the second electrically conductive layers 146 can be filled with a dielectric fill material. The trench including a dielectric pillar structure 7P and contacting a sidewall of the alternating stack (32, 146) can be filled with a first dielectric fill material. Two lateral separation trenches 89 including the trench fill dielectric material portions 84 and contacting a pair of sidewalls of the alternating stack (32, 146) can be filled with a second dielectric material. The pair of sidewalls of the alternating stack (32, 146) can be substantially parallel to each other. The retro-stepped cavity including the retro-stepped dielectric material portion 65 and contacting stepped surfaces of the alternating stack (32, 146) includes another dielectric fill material.

[0146] Referring to FIGS. 12A – 12D, a photoresist layer (not shown) is applied over the dielectric material layer 73, and is lithographically patterned to form openings in regions in which formation of additional contact via structures is desired. The pattern in the photoresist layer is transferred through the dielectric material layer 73, the insulating cap layer 71, and the retro-stepped dielectric material portion 65 to form various vertically-extending cavities. The anisotropic etch can be selective to the materials of the electrically conductive layers (46, 146) and the drain region 63, and optionally to additional materials within the memory stack structures 55. A first subset of the vertically-extending cavities (not shown) can extend to stepped surfaces (not shown) of the first electrically conductive layers 46 adjacent to the memory device region 100. A second subset of the vertically-extending cavities (subsequently filled with capacitor contact via structures 8C) can extend to stepped surfaces of the second electrically conductive layers 146 in the capacitor region 400. Another subset

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of the vertically-extending cavities (subsequently filled with drain contact via structures 88) can extend to top surfaces of the drain regions 63. The photoresist layer can be removed, for example, by ashing.

[0147] At least one conductive material is deposited in the vertically-extending cavities to fill each of the vertically-extending cavities. Excess portions of the at least one conductive material can be removed from above a horizontal plane including a top surface of the dielectric material layer 73, for example, by chemical mechanical planarization (CMP). Each remaining portion of the at least one conductive material constitutes a contact via structure (8C, 88), which include capacitor contact via structures 8C formed in the capacitor region 400, drain contact via structures 88 formed in the memory device region 100, and control gate contact via structures (not shown) that are formed in a stepped surface region (not shown) adjacent to the memory device region 100.

[0148] A plurality of contact via structures (i.e., the capacitor contact via structures 8C) is formed on the second electrically conductive layers 146 in the capacitor region 400. An additional plurality of contact via structures (i.e., the control gate contact via structures) is formed on the first electrically conductive layers 46 adjacent to the memory device region 100, as will be described below with respect to FIG. 14X.

[0149] In one embodiment, the capacitor contact via structures 8C can be arranged to facilitate pairwise connection between upper second electrically conductive layers 146 (i.e., second electrically conductive layers 146 located within an upper half of the alternating stack (32, 146)) and lower second electrically conductive layers 146 (i.e., second electrically conductive layers 146 located within a lower half of the alternating stack (32, 146)) through line level interconnect structures to be subsequently formed over the dielectric material layer 73. For example, capacitor contact via structures 8C to be electrically shorted by overlying

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interconnect line structures (such as metal line structures) can be formed along the second horizontal direction hd2, which is parallel to the lengthwise direction of the trench fill dielectric material portions 84.

[0150] As shown in FIGS. 13A – 13E, a line level dielectric material layer 92 including a dielectric material can be formed over the top surface of the dielectric material layer 73. The dielectric material of the line level dielectric material layer 92 can be, for example, silicon oxide, silicon nitride, organosilicate glass, or a combination thereof. Interconnect line structures can be formed in the line level dielectric material layer 92, for example, by forming line trenches in the line level dielectric material layer 92 and filling the line trenches with at least one conductive material. Excess portions of the at least one conductive material can be removed from above the top surface of the line level dielectric material layer 92, for example, by chemical mechanical planarization.

[0151] Node-tying metal lines (821, 822, 823, 831, 832, 833), source metal line 96, and bit lines 98 (only portions of the word lines are shown for clarity) can be formed in the line level dielectric material layer 92. The node-tying metal lines (821, 822, 823, 831, 832, 833) tie, i.e., electrically short, the same node of capacitor structures. The node-tying metal lines (821, 822, 823, 831, 832, 833) can include first node-tying metal lines (821, 822, 823) that tie the first node of a respective capacitor, and second node-tying metal lines (831, 832, 833) that tie the second node of a respective capacitor. The source metal line 96 provides electrical connection to the backside contact via structure 76 and the source region 61. The bit lines 98 provide electrical connection to the drain contact via structures 88 and the drain regions 63.

[0152] The second electrically conductive layers 146 constitute capacitor electrodes (e.g., plates) of a set of capacitors. Each capacitor plate is a conductive component of the set of capacitors. A subset of the electrically insulating layers 32 within the capacitor region 400

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constitutes node dielectrics of the set of capacitors. Each capacitor in the set comprises a first node that includes an underlying second electrically conductive layer (146U1 or 146U2) (which is one of the second electrically conductive layers 146) of a respective vertically neighboring pair and a respective contact via structure (8CU1 or 8CU2) that extends upward from the underlying second electrically conductive layer (146U1 or 146U2) and through the retro-stepped dielectric material portion 65. Each capacitor in the set further comprises a second node that includes an overlying second electrically conductive layer (146O1 or 146O2) (which is one of the second electrically conductive layers 146) of the respective vertically neighboring pair and a respective contact via structure (8CO1 or 8CO2) that extends upward from the overlying electrically conductive layer (146O1 or 146O2) and through the retro-stepped dielectric material portion 65.

[0153] In one embodiment, each capacitor within the set of capacitors can comprises two pairs of vertically neighboring electrically conductive layers (146U1, 146O1) and (146U2, 146O2) such that the first node of the capacitor includes an underlying electrically conductive layer 146U1 of a first vertically neighboring pair (146U1, 146O1) and an electrically conductive layer 146U2 of a second vertically neighboring pair (146U2, 146O2); and the second node of the capacitor includes an overlying electrically conductive layer 146O1 of the vertically neighboring pair (146U1, 146O1) and another electrically conductive layer 146O2 of the second vertically neighboring pair (146U2, 146O2).

[0154] In case the horizontal steps (i.e., the horizontal surface portions) of the stepped surfaces of the alternating stack (32, 146) has a uniform width, upper vertically neighboring pairs of second electrically conductive layers 146 (located in the upper half of the alternating stack (32, 146)) and lower vertically neighboring pairs (located in the lower half of the alternating stack (32, 146)) of second electrically conductive layers 146 can be matches such

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that each set of an upper vertically neighboring pair of second electrically conductive layers 146 and a lower vertically neighboring pair of the second electrically conductive layers 146 has a same total overlap area between neighboring pairs of second electrically conductive layers 146. If the insulator layers 32 have the same thickness throughout, the capacitance of each capacitor can be the same. If the alternating stack (32, 146) in the capacitor region includes a total of N second electrically conductive layers 146, the total number of capacitors including an upper vertically neighboring pair of second electrically conductive layers 146 and a lower vertically neighboring pair of the second electrically conductive layers 146 can be a positive integer that does not exceed N/4.

[0155] Alternatively, tying of the nodes of two pairs of vertically neighboring second electrically conductive layers 146 can be omitted. In this case, each capacitor can consist of a single vertically neighboring pair of second electrically conductive layers 146.

[0156] The first exemplary structure can include a device comprising a set of capacitors. The set of capacitors can comprise: a stack of alternating layers (32, 146) including electrically insulating layers 32 and electrically conductive layers 146 and located over a substrate 10. Each electrically conductive layer 146 that is located within the stack (32, 146), and has at least one overlying electrically conductive layer 146 which laterally extends farther than any overlying electrically conductive layer 146. The set of capacitors includes a dielectric material portion 65 located over the stepped surface region of the stack (32, 146). An interface between the dielectric material portion 65 and the stack (32, 146) includes a contiguous set of horizontal surfaces and vertical surfaces to provide the stepped surface region. The device comprises a set of dielectric fill material portions (84, 7P) are located within trenches that vertically extend through the stack (32, 146) of alternating layers and laterally contacts sidewalls of the stack (32, 146) of alternating layers. The device comprises

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a plurality of capacitor contact via structures 8C in contact with respective electrically conductive layers 146 within the stack (32, 146) of alternating layers. The electrically conductive layers 146 constitute conductive components of a set of capacitors and a subset of the electrically insulating layers 32 constitutes node dielectrics of the set of capacitors. Only the electrically insulating layers 32 located between a first node and a second node of a capacitor constitutes the node dielectrics. Each capacitor in the set comprises: a first node that includes an underlying electrically conductive layer 146U1 (or alternatively 146U2) of a respective vertically neighboring pair and a respective capacitor contact via structure 8CU1 (or alternatively 8CU2) that extends upward from the underlying electrically conductive layer 146U1 and through the dielectric material portion 65; and a second node that includes an overlying electrically conductive layer 146O1 (or alternatively 146O2) of the respective vertically neighboring pair and a respective capacitor contact via structure 8CO1 (or alternatively 8CO2) that extends upward from the overlying electrically conductive layer 146O1 and through the dielectric material portion 65.

[0157] In one embodiment, each of the trenches (i.e., the lateral separation trenches 89 and optionally the trench in which the dielectric pillar structure 7P is present, or trenches 89A, 89B described below with respect to FIGS. 14A-14X) can be entirely filled with a dielectric material of a respective dielectric fill material portion (84, and optionally 7P). In one embodiment, all sidewall surfaces of the electrically conductive layers 146 within the stack of alternating layers (32, 146) can be in contact with a surface selected from sidewall surfaces of the set of dielectric fill material portions (84, and optionally 7P) and sidewall surfaces of the dielectric material portion 65.

[0158] In one embodiment, the entire interface between an electrically conductive layer 146 within the stack (32, 146) of alternating layers and the set of dielectric fill material

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portions (84, and optionally 7P) can be a contiguous interface, and can be vertical or tapered. In one embodiment, the contiguous interface can be substantially vertical throughout an entirety thereof. As used herein, a surface is substantially vertical if the surface is vertical or a taper angle of the surface with respect to a vertical direction does not exceed 3 degrees. In one embodiment, the interface between the electrically conductive layer 146 and the set of dielectric fill material portions (84, and optionally 7P) adjoins an interface between the electrically conductive layer 146 and the dielectric material portion 65 (which is located within a subset of the stepped surfaces in the stepped surface region). In one embodiment, the combination of the interface between the electrically conductive layer 146 and the set of dielectric fill material portions (84, and optionally 7P) and the interface between the electrically conductive layer 146 and the dielectric material portion 65 includes all sidewall surfaces of the electrically conductive layer 146.

[0159] In one embodiment, the set of dielectric fill material portions (84, and optionally 7P) can be a contiguous (i.e., physically adjoined) set of material portions and contact the dielectric material portion 65. In one embodiment, the dielectric material portion 65 can be a retro-stepped dielectric material portion in which a horizontal cross-sectional area of the dielectric material portion 65 at a horizontal plane is not less than a horizontal cross-sectional area of the dielectric material portion at any horizontal plane that is more proximal to the substrate 10.

[0160] In one embodiment, each capacitor within the set of capacitors comprises two pairs of vertically neighboring electrically conductive layers (146U1, 146O1) and (146U2, 146O2). The first node of the capacitor includes an underlying electrically conductive layer 146U1 of a first vertically neighboring pair (146U1, 146O1) and an electrically conductive layer (146U2 or 146O2) of a second vertically neighboring pair (146U2, 146O2). The second

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node of the capacitor includes an overlying electrically conductive layer 146O1 of the first vertically neighboring pair (146U1, 146O1) and another electrically conductive layer (146U2 or 146O2) of the second vertically neighboring pair (146U2, 146O2).

[0161] In one embodiment, the underlying electrically conductive layer 146U1 of the first vertically neighboring pair (146U1, 146O1) and the electrically conductive layer (146U2 or 146O2) of the second vertically neighboring pair (146U2, 146O2) are electrically shorted through two contact via structures (for example, 8CU1 and 8CU2) and a first conductive line structure (for example, 833). The overlying electrically conductive layer 146O1 of the first vertically neighboring pair (146U1, 146O1) and the other electrically conductive layer of the second vertically neighboring pair (146U2, 146O2) are electrically shorted through two additional contact via structures (for example, 8CO1 and 8CO2) and a second conductive line structure (for example, 823).

[0162] In one embodiment, the set of capacitors comprise at least a first capacitor and a second capacitor. In this case, the first capacitor can comprise a first upper pair of vertically neighboring electrically conductive layers (e.g., 146U2 and 146O2) and a first lower pair of vertically neighboring electrically conductive layers (e.g., 146U1 and 146O1). The second capacitor can comprise a second upper pair of vertically neighboring electrically conductive layers (located within an upper half of the alternating stack and at different levels than the first upper pair of vertically neighboring electrically conductive layers) and a second lower pair of vertically neighboring electrically conductive layers (located within a lower half of the alternating stack and at different levels than the first lower pair of vertically neighboring electrically conductive layers). In one embodiment, the second upper pair of vertically neighboring electrically conductive layers 146 overlies the first upper pair of vertically neighboring electrically conductive layers 146; the first upper pair of vertically neighboring

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electrically conductive layers 146 overlies the first lower pair of vertically neighboring electrically conductive layers 146; and the first lower pair of vertically neighboring electrically conductive layers 146 overlies the second lower pair of vertically neighboring electrically conductive layers 146.

[0163] In one embodiment, the capacitors can be configured to provide the same capacitance for each capacitor. Such a configuration can be obtained by forming pairs of vertically neighboring electrically conductive layers 146, and providing parallel connection for a pair of component capacitors. The first component capacitor is formed by a node dielectric employing an insulator layer 32 within the lower half of the alternating stack (32, 146) and two neighboring electrically conductive layers 146. The second component capacitor is formed by a node dielectric employing an insulator layer within the upper half of the alternating stack (32, 146) and two neighboring electrically conductive layers 146. The two component capacitors are connected in parallel such that the total capacitance is the same as the target capacitance for the capacitor formed by the parallel connection of the two component capacitors. By selecting the pairs of component capacitors for parallel connection, multiple capacitors having the same total capacitance can be formed.

[0164] In one embodiment, the thickness of the insulator layers 32 can be the same throughout, and the sum of an upper overlap area between the vertically neighboring electrically conductive layers (146U2, 146O2) within the first upper pair (of a first capacitor) and a lower overlap area between the vertically neighboring electrically conductive layers (146U1, 146O2) within the first lower pair (of the first capacitor) can be substantially the same as the sum of an upper overlap area between the vertically neighboring electrically conductive layers within the second upper pair (of the second capacitor) and a lower overlap area between the vertically neighboring electrically conductive layers within the second

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lower pair (of the second capacitor). In this case, the first capacitor and the second capacitor can have the same total capacitance. In one embodiment, each capacitor within the set of capacitors can have a substantially same total overlap area between vertically neighboring electrically conductive layers contained therein.

[0165] In one embodiment, the device can further comprise a monolithic three-dimensional memory device located on the substrate 10 and in the memory device region 100. The monolithic three-dimensional memory device can comprise a memory opening 49 extending through the stack (32, 46); a memory film 55 located within the memory opening 49; and a semiconductor channel (601, 602 and optionally 66) located within the memory film 55.

[0166] In one embodiment, the set of capacitors can be a component of a peripheral device of the monolithic three-dimensional memory device; the monolithic three-dimensional memory device can be a vertical NAND memory device; the electrically conductive layers 46 comprise, or are electrically connected to, a respective word line of the vertical NAND memory device; and the substrate comprises a silicon substrate. In one embodiment, the vertical NAND memory device can comprise an array of monolithic three-dimensional NAND strings over the silicon substrate; at least one memory cell in the first device level of the three-dimensional array of NAND strings can be located over another memory cell in the second device level of the three-dimensional array of NAND strings; and the silicon substrate can contain an integrated circuit comprising a driver circuit for the memory device located thereon. The three-dimensional array of NAND strings can comprise: a plurality of semiconductor channels (601, 602, and optionally 66, and portions of 10), wherein at least one end portion of each of the plurality of semiconductor channels extends substantially perpendicular to a top surface of the silicon substrate; a plurality of charge storage elements,

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each charge storage element located adjacent to a respective one of the plurality of semiconductor channels; and a plurality of control gate electrodes having a strip shape extending substantially parallel to the top surface of the silicon substrate. The plurality of control gate electrodes comprise at least a first control gate electrode located in the first device level and a second control gate electrode located in the second device level.

[0167] FIG. 14A illustrates a schematic top down view of a device of embodiments of the invention. As shown in FIG. 14A, the capacitor region 400 is located in the stepped surface region of the stack between the sense amplifiers 402 and other bit line peripheral devices 404 (e.g., devices of the driver circuit, such as charge pump circuit devices, reference voltage and current circuit, and/pr power-on circuit, etc.) and the memory device region 100 (also referred to as the cell array) in direction hd2 (i.e., the bit line direction). The capacitor region 400 is also referred to as a dummy staircase region because it includes the stepped surface without word line contact vias (i.e., control gate interconnects). The dummy staircase region is formed at the same time during the same etching steps as the word line stepped surface regions 300 (labeled WLHU staircase) in which the word line contact vias (i.e., control gate interconnects) will be formed during a subsequent step. In other words, the stepped surface regions are formed on plural (e.g., all) sides of the elevated memory device region. For a rectangular memory device region 100, the word line stepped surface regions 300 are formed on two opposing sides of the memory device region 100 such that word lines will eventually extend in the word line direction hd1 between opposing regions 300. The word line and select gate switching transistors are located in row decoder regions 302 (labeled WL/SG SW) adjacent to regions 300 in direction hd1.

[0168] The remaining two sides of the memory device region 100 contain the dummy staircase regions. The capacitors are formed in the dummy staircase capacitor region 400

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located adjacent to the sense amplifier region 402. Thus, the size of the sense amplifier region 402 may be reduced by over 10%, such as about 20% by omitting the capacitors from region 402 and instead forming the capacitors in region 400 which is an unused dummy region in prior art devices.

[0169] The memory device region 100 contains the memory stack structures 55 and the support pillars (e.g., dielectric pillar structures) 7P, similar to that shown in FIG. 5A. However, in the embodiment of FIG. 14A, the support pillars 7P comprise cylindrical pillars instead of or in addition to the elongated dielectric pillar structures 7P shown in FIG. 6B. It should be understood that only a few of the memory stack structures 55 and the support pillars 7P are shown for clarity. If desired, the dielectric support pillar structures 7Q (not shown for clarity) as described and illustrated above may also be present in the device of the embodiment of Fig. 14A.

[0170] The periphery of the device (e.g., the periphery of the substrate, such as portion of a semiconductor wafer or a diced chip) contains a dummy staircase track 406 and a kerf region 501 (e.g., having half width of the original dicing region if the substrate is diced into chips). The dummy staircase track 406 surrounds the device and contains a stepped surface region which is a mirror image of the stepped surface region of the dummy staircases 400. The track 406 is formed during the same patterning (e.g., etching) steps as the other stepped regions 300 and 400 in the device.

[0171] FIGS. 14B-14D illustrate an exemplary structure according to an alternative of the first embodiment. The structure is similar to the structure shown in FIGS. 6A-6B, except that the support pillars 7P comprise cylindrical pillars (shown in FIG. 14A) located in region 100. The structure of FIGS. 14B-14D contains the alternating stack (32, 42), the dielectric material layer 73 and the retro-stepped dielectric material portion 65 described above with respect to

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FIG. 6A.

[0172] FIGS. 14E-14G illustrate the next step in the process in which the lateral separation trenches 89A, 89B are formed in the stack (32, 42) at the same time as the backside contact trenches 79, similar to that shown in FIGS. 7A-7D (the backside contact trenches are not shown in FIGS 14E-14G for compactness). As shown in FIG. 14E, the lateral separation trenches include first trenches 89A which extends in the bit line direction hd2, similar to trenches 89 shown in FIG. 7B. However, in this embodiment, the lateral separation trenches also include at least one second trench 89B which extend in the word line direction hd1, similar to the pillar 7P shown in FIG. 7B. The second trench 89B connects the end portions of the first trenches 89A near the end of the capacitor region 400 closest to the memory device region 100 and farthest from the stepped surface in region 400.

[0173] As shown in FIGS. 14H-14J, portions of sacrificial material layers 42 are selectively removed from the alternating stack in regions 100, 300 and 400 through the trenches 89A, 89B and the backside contact trenches 79, similar to that shown in FIGS. 8A-8C. However, unlike the prior embodiment shown in FIGS. 8A-8C, portions 42A of the sacrificial material layers 42 remain in the alternating stack near the end of the capacitor region 400 closest to the memory device region 100 and farthest from the stepped surface in region 400. Thus, each backside recess 143 abuts a portion 42A of the sacrificial material layers 42. These portions 42A (instead of the elongated pillar 7P in the prior embodiment) electrically insulate region 400 from region 100.

[0174] A plurality of first electrically conductive layers 46 (e.g., word lines / control gates which extend in the word line direction hd1) can be formed in the plurality of first backside recesses 43 in the memory device region 100 and in region 300, as described above with respect to FIGS. 9A-9B. As shown in FIGS. 14K-14M, a plurality of second electrically

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conductive layers 146 can be formed in the plurality of second backside recesses 143 at the same time as layers 46. A contiguous conductive material layer 46L can be formed on the sidewalls of the trenches 89A, 89B, the backside contact trenches 79 (as described above) and over the topmost layer of the structure. The layer 46L partially fills the trenches 89A, 89B to leave remaining trenches 89'.

[0175] Referring to FIGS. 14N-14P, the deposited conductive material of the contiguous conductive material layer 46L is etched back from the sidewalls of each backside contact trench 79, from the sidewalls of each lateral separation trenches 89', and from the dielectric material layer 73, similar to that described above with respect to FIGS. 10A-10B. This leaves electrically conductive layers 146 which function as capacitor electrodes in region 400 separated from each other by trenches 89A and 89B. The electrically conductive layers 146 between trench 89B in region 400 and region 100 are separated from electrically conductive layers 46 in region 100 by the remaining portions 42A (e.g., silicon nitride or other insulating material layer portions) of layers 42.

[0176] Referring to FIGS. 14Q-14S, the lateral separation trenches 89A, 89B can be completely filled with the dielectric material to form trench fill dielectric material portions 84, while the backside contact trenches 79 are not completely filled with the dielectric material, as described above with respect to FIGS. 11A-11B. The insulating spacer 74 can be formed in the backside contact trenches and filled with a conductive material to form a backside contact via structure 76 which extends in the word line direction hd1, as shown in FIG. 14X and as described above with respect to FIGS. 11A-11B.

[0177] As described above with respect to FIGS. 12A-12D, first subset of the vertically-extending cavities can extend to stepped surfaces of the first electrically conductive layers 46 in region 300 adjacent to the memory device region 100. A second subset of the vertically-

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extending cavities (subsequently filled with capacitor contact via structures 8C) can extend to stepped surfaces of the second electrically conductive layers 146 in the capacitor region 400. Another subset of the vertically-extending cavities (subsequently filled with drain contact via structures 88) can extend to top surfaces of the drain regions 63.

[0178] Referring to FIGS. 14T-14X, at least one conductive material is deposited in the vertically-extending cavities to fill each of the vertically-extending cavities with capacitor contact via structures 8C formed in the capacitor region 400, drain contact via structures 88 formed in the memory device region 100, and control gate contact via structures 304 that are formed in a stepped surface region 300 adjacent to the memory device region 100.

[0179] The portions 146A of the electrically conductive layers 146 that are electrically insulated from layers 46 by the trench fill dielectric material portions 84 and which are contacted by via structures 8C comprise capacitor electrodes. The portions 32A of the electrically insulating layers 32 in region 400 located between the capacitor electrodes 146A comprise capacitor dielectrics.

[0180] As shown in FIGS. 14U and 14W, a resulting capacitor 410 includes adjacent electrode plates 146A separated by an insulating layer 32A, and respective electrical contacts (e.g., capacitor contact via structures 8C) to the electrode plates 146A.

[0181] Thus, as shown in FIG. 14X, in the first embodiment and in the alternative embodiment described above, a three dimensional memory device (e.g., such as the NAND device) includes the memory device region 100 containing a plurality of non-volatile memory devices (e.g., the NAND strings), a peripheral device region 402/404 containing active driver circuit devices (e.g., transistors), and first stepped surface region 400 located between the peripheral device region 402/404 and the memory device region 100, and containing a plurality of passive driver circuit devices, such as capacitors 410 or resistors as will be

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described with respect to additional embodiments below. In should be noted that the peripheral device region 402/404, the dummy staircase track 406 and the kerf region 501 may also contain additional passive devices (e.g., capacitors or resistors) or it may contain no passive devices. Thus, the capacitors 410 may be located in dummy staircase track 406 if desired. Likewise, region 400 may also contain additional active devices (e.g., transistors) or it may contain no active devices.

[0182] As described above, the stack of alternating layers including electrically insulating layers 32 and electrically conductive layers (46, 146) located over the substrate 10. The first stepped surface region 400 contains first portions of the electrically insulating layers 32 and first portions of the electrically conductive layers 146, and the first stepped region 400 is located on a first side of the stack facing the peripheral region. The second stepped surface region 300 contains second portions of the electrically insulating layers 32 and second portions of the electrically conductive layers 46 located on a second side of the stack (e.g. at a side perpendicular to the first side).

[0183] As described above, a plurality of semiconductor channels 60 are located in the memory device region 100 in the stack, such that at least one end portion of each of the plurality of semiconductor channels extends substantially perpendicular to a top surface of the substrate 10. A plurality of charge storage elements (i.e., portions of the memory films 50) are located adjacent to a respective one of the plurality of semiconductor channels 60. A plurality of passive device contact via structures (e.g., capacitor via structures 8C) extend extending substantially perpendicular to the top surface 7 of the substrate 10 to the respective first portions of the electrically conductive layers 146 in the first stepped surface region 400. A plurality of control gate contact via structures 304 extend substantially perpendicular to the top surface 7 of the substrate 10 to the respective second portions of the electrically

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conductive layers 46 in the second stepped surface region 300.

[0184] The peripheral device region contains sense amplifiers in region 402. The second stepped surface region 300 comprises a word line stepped surface region 300. The second portions of the electrically conductive layers 46 comprise a plurality of control gate electrodes extending substantially parallel to the top surface of the substrate, and the plurality of control gate electrodes comprise at least a first control gate electrode located in the first device level and a second control gate electrode located in the second device level.

[0185] In the above embodiments, the passive driver circuit devices comprise capacitors 410, and the first portions 146A of the electrically conductive layers 146 comprise a plurality of capacitor electrodes. The first portions of the electrically insulating layers 32 in region 400 comprise capacitor dielectrics located between the capacitor electrodes 146A. The respective first 146A and second 46 portions of each of the electrically conductive layer are located at the same level above the substrate and are electrically insulated from each other (e.g., by material 84 and/or optionally by pillar 7P).

[0186] As shown in FIG. 14Y, N/2 capacitors 410 may be formed from N layers 146 in the stack, where N is any integer greater than 1. However, as described above with respect to FIGS. 13A-13D, layers 146 at the top of the stack are shorter than layers 146 at the bottom of the stack. This causes the capacitors to be of unequal size.

[0187] FIG. 14Z illustrates a capacitor interconnection configuration similar to that of FIGS. 13A-13D, where the longest layer 146 is electrically connected by interconnect (e.g., metal line) 833 to the second shortest layer 146 in the stack to form one capacitor electrode. The next longest layer 146 in the stack is electrically connected by interconnect (e.g., metal line 823) to the shortest layer 146 in the stack to form another capacitor electrode. The remaining layers 146 in the stack may be connected in a similar way. This results in a

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capacitor 410A having two overlying layers 146 of different length connected to each other to form an overlying electrode and two underlying layers 146 of different length connected to each other to form an underlying electrode, where the average electrode length of all capacitors in the stack is about the same. This results in N/4 capacitors in a stack containing N layers 146.

[0188] In a second exemplary structure according to a second embodiment of the present disclosure the passive device of the driver circuit comprises a pillar shaped resistor. Referring to FIG. 15A, a substrate includes a semiconductor material layer 10 having a major surface 7. A doped semiconductor well 110 can be formed in a device region, which is herein referred to as a resistor region 500. The resistor region 500 may be located in a portion of the memory device region 100, as shown in FIG. 37. A memory device region 100 and a capacitor region 400 can be provided for formation of the devices illustrated in the first embodiment. The semiconductor material layer 10 can have a doping of a first conductivity type (which can be p-type or n-type), and the doped semiconductor well 110 can have a doping of a second conductivity type which is the opposite of the first conductivity type. In one embodiment, the concentration of electrical dopants (which can be p-type dopants or n-type dopants) in the doped semiconductor well 110 can be in a range from $1.0 \times 10^{17}/cm^3$ to $2.0 \times 10^{21}/cm^3$, although lesser and greater dopant concentrations can also be employed. In one embodiment, the doped semiconductor well 110 can include a conductive (e.g., degenerately doped semiconductor or metallic) material rather than a semiconductor material, i.e., a material having electrical conductivity greater than 1.0×10^5 S/cm. The doped semiconductor well 110 is a laterally-extending semiconductor or conductive structure, and can consist of at least one single crystalline semiconductor material portion having a doping of the second conductivity type (e.g., n-type well) and located in the substrate 10 (e.g., p-type

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substrate or substrate well). Optionally, a doped contact region 112 can be formed, which has a doping of the same conductivity type (e.g., n-type) as the doped semiconductor well 110 and has a greater dopant concentration than the doped semiconductor well 110 (e.g., N+ well). Optionally, shallow trench isolation structures 120 including at least one dielectric material can be formed at a periphery of the doped semiconductor well 110 for device isolation.

[0189] Referring to FIG. 15B, the processing steps of FIG. 1 are performed to form a stack (32, 42) of alternating layers including the first material layers 32 and the second material layers 42.

[0190] Referring to FIG. 16, memory openings 49 are formed in the memory device region 100 and at least one resistor opening 249 can be formed in the resistor region 500. The memory openings 49 and the at least one resistor opening 249 can be formed simultaneously employing the same processing steps employed to form the memory openings of the first embodiment. The size of each resistor opening 249 may be the same as, or may be different from, the size of the memory openings 49. If a plurality of resistor openings 249 is formed, the resistor openings 249 can have the same size, or can have different size. The size of the resistor openings 249 can be adjusted depending on the target resistance of a resistor to be subsequently formed. In one embodiment, the resistance of a resistor to be formed in a resistor opening 249 is generally inversely proportional to the diameter (or a lateral dimension if a non-circular cross-sectional shape is employed) of the resistor opening 249. The bottom of each resistor opening 249 can extend to a top surface of the doped semiconductor well 110.

[0191] Each resistor opening 249 is a vertically-extending cavity that extends from a first horizontal plane including a top surface of the alternating stack (32, 42) to the laterally-

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extending semiconductor or conductive structure of the combination of the doped semiconductor well 110 and the doped contact region 112. A physically exposed portion of the top surface of the laterally-extending semiconductor or conductive structure (i.e., the doped semiconductor well 110) is present within a second horizontal plane located underneath, and vertically spaced by a plurality of layers within the alternating stack (32, 42) from, the top surface of the alternating stack (32, 42). The second horizontal plane is the plane including the bottom surface of each resistor opening 249, which is the recessed, or non-recessed, top surface of the doped semiconductor well 110.

[0192] Referring to FIG. 17, the processing steps of FIG. 2 of the first embodiment can be performed to form memory stack structures 55 and at least one pillar structure 155 simultaneously. The memory stack structures 55 are formed in the memory openings 49 in the memory device region 100, and a pillar structure 155 is formed in each resistor opening 249 in the resistor region 500. Each pillar structure 155 can have the same set of components as a memory stack structure 55 and which are formed during the same formation (e.g., deposition) steps. Each component within a pillar structure 155 can have the same composition as the corresponding component (having the same reference numeral) within a memory stack structure 155. Each component within a pillar structure 155 can have the same height as the corresponding component within a memory stack structure 155. Except for an epitaxial channel portion 66 and a dielectric core 62, each component within a pillar structure 155 can have the same lateral dimension (such as a lateral thickness) as the corresponding component within a memory stack structure 155. If a horizontal cross-sectional shape of a pillar structure 155 is different from a horizontal cross-sectional shape of a memory stack structure 55 taken at a same vertical distance from the top surface of the substrate (10, 110, 112, 12), the epitaxial channel portion 155 and the dielectric core 62 within the pillar

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structure 155 can have different dimensions than the corresponding dimensions of a memory stack structure 55. If a horizontal cross-sectional shape of a pillar structure 155 is the same a horizontal cross-sectional shape of a memory stack structure 55 taken at a same vertical distance from the top surface of the substrate (10, 110, 112, 12), the epitaxial channel portion 66 and the dielectric core 62 within the pillar structure 155 can have the same dimensions as the epitaxial channel portion 66 and the dielectric core 62 within the memory stack structure 55.

[0193] A pillar structure 155 is formed within each resistor opening 249. A semiconductor channel (601, 602) is formed on each optional epitaxial channel portion 66, which is a single crystalline semiconductor material portion and is intrinsic or has a doping of the first conductivity type. The single crystalline semiconductor material portion in the resistor opening 249 (as embodied as an epitaxial channel portion 66 in the resistor opening 249) is formed simultaneously with formation of the epitaxial channel portions 66 in the memory openings 49. The first conductivity type is the conductivity type of the semiconductor material layer 10, and is the opposite of the conductivity type of the doped semiconductor well 110 (which has a doping of the second conductivity type). The memory films 50 in the memory stack structures 55 and the at least one pillar structure 155 can be a layer stack of dielectric material layers as described above, i.e., a stack of a blocking dielectric layer, a memory material layer, and a tunneling dielectric layer.

[0194] Each semiconductor channel (610, 602) in the memory openings 49 and the at least one resistor opening 249 can be formed by deposition of an intrinsic semiconductor material or a semiconductor material of the first conductivity type. The semiconductor channels (601, 602) can include a polycrystalline semiconductor material or an amorphous semiconductor material. A vertically-extending semiconductor material portion in each

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resistor opening 249 (as embodied in a semiconductor channel (601, 602) in the resistor opening 249) is formed simultaneously with formation of the semiconductor channels (601, 602) in the memory openings 49.

[0195] Each drain region 63 formed in the at least one resistor opening 249 is a doped semiconductor material portion, and is formed with a doping of the second conductivity type. The drain regions 63 of the memory stack structures 55 and each drain region 63 of the pillar structure 155 can be formed simultaneously.

[0196] Referring to FIG. 18, a photoresist layer 67 is applied over the second exemplary structure, and is lithographically patterned to form openings in the resistor region 500. Specifically, an opening in the photoresist layer 67 is formed in an area including the at least one pillar structure 155 by patterning the photoresist layer 67. In one embodiment, the thickness of the photoresist layer 67 can be selected such that electrical dopants to be subsequently implanted into the at least one pillar structure 155 can be implanted to the bottommost portion of the at least one pillar structure 155, while the electrical dopants are not implanted into any portion of the memory stack structures 55 in the memory device region 100. In one embodiment, the thickness of the photoresist layer 67 can be greater than the thickness of the alternating stack (32, 42).

[0197] Electrical dopants of the second conductivity type (e.g., n-type) can be implanted into the vertically-extending semiconductor material portion (embodied as a semiconductor channel (601, 602)) in each pillar structure 155, while implantation of the electrical dopants of the second conductivity type into the semiconductor channels (601, 602) of the memory stack structures 55 is prevented by the presence of the patterned photoresist layer 67. All semiconductor material portions in the pillar structure 155 can be doped with the implanted dopants of the second conductivity type. The dose of the implanted dopants of the second

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conductivity type is selected such that all semiconductor material portions are doped in the pillar structure 155.

[0198] The implantation of the electrical dopants of the second conductivity type converts each epitaxial semiconductor channel 66 (which is intrinsic or has a doping of the first conductivity type as formed) in the at least one pillar structure 155 into a epitaxial doped semiconductor portion 166 having a doping of the second conductivity type. Further, the implantation of the electrical dopants of the second conductivity type converts each semiconductor channel (601, 601) in the at least one resistor opening 249 into a vertically-extending doped semiconductor portion, which is herein referred to as a first doped semiconductor portion 160. Each epitaxial doped semiconductor portion 166 and each first doped semiconductor portion 160 are doped semiconductor material portions, and are formed by ion implantation of electrical dopants of the second conductivity type such that an atomic concentration of the dopants of the second conductivity type in a range from 1.0×10^{17} /cm^3 to 1.0×10^{20}/cm^3 therein. In one embodiment, all semiconductor material within each pillar structure 155 can have a doping of a same conductivity type, which is the second conductivity type.

[0199] An epitaxial doped semiconductor portion 166 is located at a bottom portion of each vertically-extending cavity (i.e., a resistor opening 249), and comprises the same semiconductor material as the epitaxial channel portions 66 of the memory stack structures 55. In one embodiment, each first doped semiconductor portion 160 can comprise a doped polycrystalline semiconductor material portion that is formed directly on inner surfaces of at least one electrically insulating material (i.e., the dielectric material of the memory film 50) within a respective resistor opening 249. Each drain region 63 within the at least one pillar structure 155 is herein referred to as a second doped semiconductor portion 163.

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[01100] Referring to FIG. 19, the patterned photoresist layer 67 can be removed, for example, by ashing. A dielectric cap layer 71 can be formed employing the same method as in the first embodiment (as illustrated in FIG. 2).

[0200] Referring to FIG. 20, the processing steps of FIGS. 3, 4, 5A and 5B, 6A and 6B, and 7A – 7C can be performed. Concurrently with formation of the backside contact trench 79 and optional formation of the lateral separation trenches 89 (See FIGS. 7B and 7C), a resistor contact trench 279 can be formed in an area overlying the doped contact region 112. The lateral separation trenches 89 may be omitted if the capacitor structures of the first embodiment are not to be formed.

[0201] The processing steps of FIGS. 8A – 8C, 9A and 9B, and 10A and 10B can be subsequently performed to form first electrically conductive layers 46 in the memory device region 100, second electrically conductive layers 146 in the capacitor region 400, and third electrically conductive layers 246 in the resistor region 500. During the processing steps of FIGS. 8A – 8C, portions of the sacrificial material layers 42 in the resistor region 500 can be removed by introduction of the etchant through the resistor contact trench 279 to form third backside recesses in each space from which the sacrificial material layers 42 are removed from the resistor region 500. The third electrically conductive layers 246 are formed in the third backside recesses by deposition of the same material as the first and second electrically conductive layers (46, 146) in the same processing step. The contiguous conductive material layer 46L can be deposited on the sidewalls of the resistor contact trench 279, and is subsequently removed from the sidewalls of the resistor contact trench 279 during the processing steps of FIGS. 10A and 10B.

[0202] Referring to FIG. 21, the processing steps of FIGS. 11A and 11B can be performed to form an insulating spacer 274 in each resistor contact trench 279 concurrently

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with formation of the insulating spacer 74 in the backside contact trench 79. The insulating spacer 274 in the resistor region 500 can have the same composition as, and the same lateral thickness as, the insulating spacer 74 in the memory device region 100. A substrate contact via structure 276 can be formed in the cavity extending through the insulating spacer 274 in the resistor region 500. The substrate contact via structure 276 in the resistor region 500 can be formed concurrently with formation of the backside contact via structure 76 in the memory device region 100. The substrate contact via structure 276 is a contact via structure that contacts a top surface of a laterally-extending semiconductor or conductive structure (which is a combination of the doped semiconductor well 110 and the doped contact region 112). In one embodiment, the backside contact via structure 76 and the substrate contact via structure 276 can be formed by deposition of a metallic material.

[0203] Referring to FIG. 22, the processing steps of FIGS. 12A – 12D can be sequentially performed to form various contact via structures (8C, 88), which can include the capacitor contact via structures 8C, the control gate contact via structures 304, and the drain contact via structures 88. A pillar contact via structure 850 can be formed on a top surface of each pillar structure 155 concurrently with formation of other via contact structures such as the drain contact via structures 88. In one embodiment, as many pillar contact via structures 850 can be formed as the number of pillar structures 155. The pillar structures 850 can be formed in the same processing step as, and can have the same composition as, the drain contact vial structures 88. Optionally, the pillar contact via structures 850, the capacitor contact via structures 8C, the control gate contact via structures 304, and the drain contact via structures 88 can be formed employing a same set of processing steps, and can comprise a same set of conductive materials.

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[0204] Subsequently, the processing steps of FIGS. 13A – 13E can be performed to form a line level dielectric material layer 92 and various interconnect line structures therein. The interconnect line structures formed in the line level dielectric material layer 92 can include, for example, node-tying metal lines (821, 822, 823, 831, 832, 833), source metal line 96, and bit lines 98 as illustrated in FIGS. 13A – 13E, and additionally include a first resistor node metal line 851 contacting the pillar contact structures 850 and a second resistor node metal liner 852 contacting the substrate contact via structure 276.

[0205] The second exemplary structure can comprise a semiconductor device. The semiconductor device can comprise an alternating stack (32, 246) of first material layers 32 and second material layers 246 located over a substrate (10, 110, 112, 120). The semiconductor device can further comprise at least one pillar structure 155 extending from a first horizontal plane including a top surface of the alternating stack (32, 246) to a second horizontal plane located underneath, and vertically spaced by a plurality of layers (such as the first material layers 32 and the second material layers 246) within the alternating stack (32, 246) from, the top surface of the alternating stack (32, 246). The semiconductor device further comprises a laterally-extending semiconductor or conductive structure (110, 112) contacting a bottom surface of the at least one pillar structure 155; and a contact via structure 276 contacting a top surface of the laterally-extending semiconductor or conductive structure (110, 112) and laterally spaced from the at least one pillar structure 155. Each of the at least one pillar structure 155 comprises a set of at least one doped semiconductor material portion (160, 166, 63) therein. All semiconductor material within each of the at least one pillar structure 155 has a doping of a same conductivity type, which can be the second conductivity type. The contact via structure (as embodied in the substrate contact via structure 276) can comprise a metallic via structure.

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[0206] In one embodiment, the at least one doped semiconductor material portion (160, 166, 63) comprises a doped polycrystalline semiconductor material portion 160 contacting inner surfaces of at least one electrically insulating material, which can be a memory film 50.

[0207] The semiconductor device can further include a memory opening extending between the first horizontal plane and another horizontal plane including a bottom surface of the alternating stack (32, 46), and a memory stack structure 55 that comprises a memory film 50 located within the memory opening, and a semiconductor channel (601, 602) located within the memory film 50. Each of the at least one pillar structure 155 comprises a layer stack of at least two dielectric material layers (i.e., a memory film 50) located on an outer sidewall of a respective set of at least one doped semiconductor material portion (160, 166, 63). The memory film 50 in a memory stack structure 55 and the layer stack 50 of at least two dielectric material layers in the pillar structure 155 comprise an identical set of dielectric materials.

[0208] A first doped semiconductor material portion (as embodied in a doped polycrystalline semiconductor material portion 160) within each set of at least one doped semiconductor material portion (160, 166, 63) comprises the same semiconductor material as the semiconductor channel (601, 602), and further includes electrical dopants of the second conductivity type.

[0209] In one embodiment, the semiconductor channel (601, 602) can be intrinsic, or can have a doping of an opposite conductivity type from the set of at least one doped semiconductor material portion (160, 166, 63), which has a doping of the second conductivity type.

[0210] In one embodiment, the memory stack structure 55 further comprises a drain region 63 having a doping of the second conductivity type. A second doped semiconductor

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material portion, as embodied as a drain region 63, can be present within each set of at least one doped semiconductor material portion (160, 166, 63). The second doped semiconductor material portion 63 in each pillar structure 155 can comprise the same semiconductor material as the drain region 63 in the memory stack structure 55.

[0211] In one embodiment, the memory stack structure 55 further comprises an epitaxial channel portion 66 having a doping of the first conductivity type, and an epitaxial doped semiconductor portion 166 can be present within each set of at least one doped semiconductor material portion (160, 166, 63). The epitaxial doped semiconductor portion 166 comprises the same semiconductor material as the epitaxial channel portion 66, and further includes electrical dopants of the second conductivity type.

[0212] In one embodiment, the laterally-extending semiconductor or conductive structure (110, 112) consists of at least one single crystalline semiconductor material portion located in the substrate. In one embodiment, the laterally-extending semiconductor or conductive structure (110, 112) can consist of the doped semiconductor well 110 and the doped contact region 112, which have a doping of the second conductivity type.

[0213] In one embodiment, the first material layers 32 can be electrically insulating layers 32, and the second material layers (246, 46) can be electrically conductive layers. In one embodiment, the first material layers 32 comprise a first electrically insulating material, the second material layers (246, 46) comprise a second electrically insulating material, and the memory stack structure 55 extends through another alternating stack (32, 46) of the first material layers 32 and electrically conductive layers 46 located at each level of the second material layers (246, 46). In one embodiment, the set of at least one doped semiconductor material portion (160, 166, 163) comprises electrical dopants of the second conductivity type at an atomic concentration in a range from 1.0×10^{17} /cm^3 to 1.0×10^{20}/cm^3.

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[0214] In one embodiment, the semiconductor structure can further include the vertical NAND memory device of the first embodiment.

[0215] Referring to FIG. 23, an alternate embodiment of the second exemplary structure can be derived from the second exemplary structure by forming a pillar contact via structure 850 that contacts a plurality of pillar structures 155 at the processing steps of FIG. 22.

[0216] In a third exemplary structure according to a third embodiment of the present disclosure the original insulating layers 42 are retained in the stack and are not replaced by the electrically conducting layers 246. Referring to FIG. 24, this structure can be derived from the second exemplary structure of FIG. 19 by performing the processing steps of FIGS. 3, 4, 5A and 5B, and by forming the dielectric pillar structure(s) 7P and the dielectric material layer 73 employing the processing methods of FIGS. 6A and 6B. If desired, the dielectric support pillar structures 7Q (not shown for clarity) as described and illustrated above may also be present in the device of this embodiment. At least one pillar structure 155 can be formed in a resistor region 600, which can be a region that replaces the resistor region 500 of the second embodiment, or can be provided in addition to the resistor region 500 of the second embodiment. Regions 500 or 600 may be located in part of the memory device region 100 and/or in the kerf region 501, as shown in FIG. 37.

[0217] Subsequently, the processing steps of FIGS. 7A – 7D, 8A – 8C, 9A and 9B, 10A and 10B, and 11A and 11B are performed without forming the resistor contact trench 279 in the resistor region 600. If another resistor region 500 of the second embodiment is provided, a resistor contact trench 279 can be formed in such a resistor contact region 500.

[0218] In the third embodiment, first portions of second material layers 42 in the memory device region 100, an optional capacitor region 400, and an optional additional resistor region 500 are replaced with electrically conductive layers (46, 146, 246), while second portions of

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the second material layers 42 in the resistor region 600 remain intact. In this case, the second material layers 42 comprise a dielectric material, and are not removed within a region (i.e., the resistor region 600) including at least one vertically-extending cavity that is filled with a pillar structure 155.

[0219] Referring FIG. 25, at least one pillar contact via structure 850, drain contact via structures 88, and capacitor contact via structures 8C can be formed in the same manner as in the processing steps of FIG. 22.

[0220] Referring to FIG. 26, a resistor contact trench 279 can be formed through the alternating stack of first material layers 32 and second material layers 42 over the area of the doped contact region 112, for example, by application of a photoresist layer, lithographic patterning of the photoresist layer, and transfer of the pattern in the photoresist layer through the alternating stack (32, 42) by an anisotropic etch. In this case, the resistor contact trench 279 can be formed after formation of the backside contact trench 79 employed to replace portions of the second material layers 42 in the memory device region 100 and the capacitor region 400 with a conductive material. In one embodiment, the first material layers 32 can include a first insulating material (such as silicon oxide) and the second material layers 42 can include a second insulating material (such as silicon nitride).

[0221] Referring to FIG. 27, a substrate contact via structure 276 can be formed by filling the resistor contact trench 279 with at least one conductive material. An insulating spacer is not necessary in the resistor contact trench 279. Thus, the substrate contact via structure 276 can contact sidewalls of the first material layer 32 and the second material layer 42 in the resistor region 600. The at least one pillar contact via structure 850 can be a first resistor node via structure, and the substrate contact via structure 276 can be a second resistor node via structure.

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[0222] In a fourth exemplary structure according to a fourth embodiment of the present disclosure, the resistors are formed in one or more of the stepped regions 700, which may be located in the word line stepped surface region(s) 300, the dummy staircase region(s) 400, and/or in the dummy staircase track 406, as shown in FIG. 37. Referring to FIG. 28, this structure can be derived from the first exemplary structure of FIGS. 6A and 6B, or the second exemplary structure of FIG. 19 by forming the optional dielectric pillar structure 7P and the dielectric support pillar structures 7Q and the dielectric material layer 73. The capacitor region 400 of the first embodiment may, or may not, be present in the fourth exemplary structure. The resistor region 500 of the second embodiment may, or may not, be present in the fourth exemplary structure. The resistor region 600 of the third embodiment may, or may not, be present in the fourth exemplary structure. A resistor region 700 is provided adjacent to a memory device region 100 (e.g., in stepped regions 300, 400 and/or 406). The optional dielectric pillar structure 7P can be formed at, or in proximity to, a boundary between the memory device region 100 and the resistor region 700 in a pattern same as, or similar to, the pattern of the dielectric pillar structure 7P of the first embodiment.

[0223] Referring to FIGS. 29A – 29D, the processing steps of FIGS. 7A – 7D are performed to form a backside contact trench 79 in the memory device region 100 and optional lateral separation trenches 89 in the resistor region 700.

[0224] Referring to FIGS. 30A and 30B, the processing steps of FIGS. 8A – 8C and the processing steps of FIGS. 9A and 9B are performed to form an alternating stack (32, 346) of first material layers that are electrically insulating layers 32 and second material layers that are electrically conductive layers 346, which are herein referred to as fourth electrically conductive layers 346.

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[0225] Referring to FIGS. 31A and 31B, the processing steps of FIGS. 10A and 10B are performed to remove any remaining metallic material from inside the backside contact trench 79.

[0226] Referring to FIGS. 32A and 32B, the processing steps of FIGS. 11A and 11B are performed to form an insulating spacer 74 and a backside contact via structure 76.

[0227] Referring to FIGS. 33A – 33D, the processing steps of FIGS. 12A – 12D are performed with a different lithographic pattern for forming contact via structures, which are herein referred to as resistor contact via structures 8R. A photoresist layer is applied over the dielectric material layer 73, and is lithographically patterned to form openings that overlie stepped horizontal surfaces of the fourth electrically conductive layers 346. A first set of vertically-extending via cavities is formed through the optional dielectric material layer 73 and the retro-stepped dielectric material layer 65. The lithographic pattern formed in the photoresist layer can be selected such that each horizontal stepped surface of the fourth electrically conducive layers 346 is physically exposed at the bottom of the first set of vertically-extending via cavities in the resistor region 700. The photoresist layer is removed, for example, by ashing. The first set of vertically-extending via cavities can be filled in the same manner as in the processing steps of FIGS. 12A – 12D of the first embodiment to form the resistor contact via structures 8R. Each fourth electrically conductive layer 346 is a laterally-extending semiconductor or conductive structure that contacts a respective resistor contact via structure 8R.

[0228] Referring to FIGS. 34A – 34D, another photoresist layer is applied over the dielectric material layer 73, and is lithographically patterned to form openings that overlie the stepped horizontal surfaces of the fourth electrically conductive layers 346 and do not overlap with the resistor contact via structures 8R. A second set of vertically-extending via cavities

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7C is formed through the optional dielectric material layer 73 and the retro-stepped dielectric material layer 65. The lithographic pattern formed in the photoresist layer can be selected such that each horizontal stepped surface of the fourth electrically conducive layers 346 is physically exposed at the bottom of the second set of vertically-extending via cavities in the resistor region 700 without etching, or physically exposing any surface of, the resistor contact via structures 8R. The photoresist layer is removed, for example, by ashing.

[0229] Referring to FIGS. 35A – 35D, the second set of vertically-extending via cavities 7C can be filled with a suitable material that can provide a target level of resistivity. In one embodiment, the second set of vertically-extending via cavities can be filled with doped semiconductor material. The doped semiconductor material can be deposited in the second set of vertically extending via cavities by deposition of a semiconductor material with *in-situ* doping, or can be deposited as an intrinsic semiconductor material or a doped semiconductor material and implanted with electrical dopants employing an implantation mask layer (such as a photoresist layer). Excess portions of the doped semiconductor material above the top surface of the dielectric material layer 73 can be removed, for example, by chemical mechanical planarization.

[0230] Each remaining portion of the doped semiconductor material in a vertically-extending via cavity of the second constitutes a pillar structure 7R. Each pillar structure 7R can include a doped semiconductor material having a doping of at a preselected dopant level. In one embodiment, the pillar structures 7R can have a same horizontal cross-sectional area, and the resistance of each pillar structure 7R can be inversely proportional to the height of the pillar structure 346. Each fourth electrically conductive layer 346 is a laterally-extending semiconductor or conductive structure that contacts a respective resistor contact via structure 8R and a respective pillar structure 7R. In one embodiment, each of the pillar structure 7R

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can consist of a respective doped semiconductor material portion that is deposited within a respective vertically-extending cavity formed on the laterally-extending semiconductor or conductive structure (which is embodied as a fourth electrically conductive layer 346).

[0231] In one embodiment, a pillar structure 7R is formed within each vertically-extending cavity in the second set of vertically extending cavities, and each pillar structure 7P can comprises a doped semiconductor material portion. All semiconductor material within each pillar structure 7R can have a doping of the same conductivity type, which can be the first conductivity type or the second conductivity type.

[0232] Referring to FIGS. 36A – 36D and 37, a line level dielectric material layer 92 including a dielectric material can be formed over the top surface of the dielectric material layer 73 in the same manner as in the first embodiment. Interconnect line structures can be formed in the line level dielectric material layer 92, for example, by forming line trenches in the line level dielectric material layer 92 and filling the line trenches with at least one conductive material. Excess portions of the at least one conductive material can be removed from above the top surface of the line level dielectric material layer 92, for example, by chemical mechanical planarization.

[0233] First electrode metal lines 841, second electrode metal lines 842, source metal line 96, and bit lines 98, and optionally, additional metal line structures of the first, second, and third embodiments can be formed in the line level dielectric material layer 92. Each first electrode metal line 841 can contact a top surface of a pillar structure 7R, and each second electrode metal line 842 can contact a top surface of a resistor contact via structure 8R. The node-tying metal lines (821, 822, 823, 831, 832, 833) can include first node-tying metal lines (821, 822, 823) that tie the first node of a respective capacitor, and second node-tying metal lines (831, 832, 833) that tie the second node of a respective capacitor. The source metal line

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98 provides electrical connection to the backside contact via structure 76 and the source region 61. The bit lines 98 provide electrical connection to the drain contact via structures 88 and the drain regions 63.

[0234] While the present disclosure is described employing an embodiment in which a single pillar structure 7R is formed per fourth electrically conductive layer 346, embodiments are contemplated herein in which multiple pillar structures 7R are formed per fourth exemplary conductive structure 346 at one or more levels.

[0235] Each physically adjoined set of a pillar structure 7R, a laterally-extending semiconductor or conductive structure as embodied as a portion of a fourth electrically conductive layer 346, and contact via structure 8R collectively constitute a resistor structure (7R, 346, 8R). A plurality of resistor structures can be simultaneously formed.

[0236] The fourth exemplary structure comprises a semiconductor device, which comprises an alternating stack (32, 346) of first material layers 32 and second material layers 346 located over a substrate (10, 61), at least one pillar structure 7P extending from a first horizontal plane including a top surface of the alternating stack (32, 346) to a second horizontal plane located underneath, and vertically spaced by a plurality of layers within the alternating stack (32, 346) from, the top surface of the alternating stack. For each pillar structure 7P, the second horizontal plane can be the plane that includes the top surface of a fourth electrically conductive layer 346 that contacts the pillar structure 7R. The plurality of layers that separates the first horizontal plane and the second horizontal plane can be the set of first and second material layers (32, 346) located between the first horizontal plane and the second horizontal plane. The first horizontal plane is common for all pillar structures 7P, and the second horizontal plane depends on the location of the bottommost portion of the pillar structure 7R.

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[0237] A laterally-extending semiconductor or conductive structure, as embodied by a fourth electrically conductive layer 346, contacts a bottom surface of the at least one pillar structure 7P. A contact via structure 8R contacts a top surface of the laterally-extending semiconductor or conductive structure, as embodied by the fourth electrically conductive layer 346, and is laterally spaced from the at least one pillar structure 7P. Each of the at least one pillar structure 7P comprises a set of at least one doped semiconductor material portion therein (which can be a single doped semiconductor material portion). All semiconductor material within each of the at least one pillar structure has a doping of the same conductivity type, which can be the first conductivity type or the second conductivity type.

[0238] A plurality of resistor structures can be provided. Each resistor structure comprises at least one pillar structure 7R extending from the first horizontal plane to a respective electrically conductive layer 346 located at different levels. A fourth electrically conductive layer 346 can contact a bottom surface of each pillar structure 7R. A resistor contact via structure 8R can contact a top surface of each fourth electrically conductive layer 346. In one embodiment, each resistor contact via structure 8R can comprise a metallic via structure.

[0239] The doped semiconductor material portion of each pillar structure 7R can comprise a doped polycrystalline semiconductor material portion contacting inner surfaces of at least one electrically insulating material, which can be the insulating material of the retro-stepped dielectric material portion. In one embodiment, the first material layers 32 comprise electrically insulating layers, the second material layers 346 comprise electrically conductive layers, the laterally-extending semiconductor or conductive structure 346 comprises one of the electrically conductive layers. In one embodiment, each of the at least one pillar structure 7P can consist of a respective doped semiconductor material portion.

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[0240] The alternating stack (32, 346) of the insulator layers 32 and the fourth electrically conductive layers 346 can comprise a stepped surface region in which each fourth electrically conductive layer 346 having at least one overlying fourth electrically conductive layer 346 laterally extends farther than any overlying fourth electrically conductive layer 346. Horizontal surfaces of the alternating stack (32, 346) that do not underlie any other layer within the alternating stack (32, 346) (and which contact one of the retro-stepped dielectric material portion 65, a pillar structure 7R, and/or a resistor contact via structure 8R) are adjoined to vertical surfaces of the first and second material layers. The retro-stepped dielectric material portion 65 overlies the stepped surface region. A set of at least one pillar structure 7R, a laterally-extending semiconductor or conductive structure as embodied in a portion of a fourth electrically conductive layer 346, and a resistor contact via structure 8R collectively constitute a resistor structure.

[0241] The first, second, third, and fourth exemplary structures can be formed alone, or in combination with any other among the first, second, third, and fourth exemplary structures. The exemplary structures of the present disclosure can provide passive components (such as resistors and capacitors) integrated with a three-dimensional device including an alternating stack of first material layers and second material layers, which can be a three-dimensional memory device such as a vertical NAND device. Some embodiments of the present disclosure provide capacitor structures and/or resistor structures employing stepped surfaces that are formed on the alternating stack of material layers. Thus, the processing steps of forming contact via structures for control gate electrodes of a vertical memory device can be employed to form the stepped surface region for the exemplary devices of the present disclosure. In some other embodiments, pillar structures that constitute a resistive portion of a resistor structure can be formed employing the same processing steps as the processing

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steps employed to form memory stack structures and by adding the processing step of a masked ion implantation to dope the semiconductor material therein. Thus, the passive devices of the present disclosure can be formed with minimal addition and/or modification to known processing steps for manufacturing a three-dimensional memory device, thereby reducing the production cost for the passive devices. In addition, the passive devices of the present disclosure can be formed in proximity to memory stack structures by employing stepped surfaces that can be formed on an alternating stack of insulator layers and electrically conductive layers. Thus, integration of the passive devices into a peripheral circuit for a memory device can be done with minimal electrical wiring.

[0242] Although the foregoing refers to particular preferred embodiments, it will be understood that the disclosure is not so limited. It will occur to those of ordinary skill in the art that various modifications may be made to the disclosed embodiments and that such modifications are intended to be within the scope of the disclosure. All of the publications, patent applications and patents cited herein are incorporated herein by reference in their entirety.

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WHAT IS CLAIMED IS:

1. A three dimensional memory device, comprising:

a memory device region containing a plurality of non-volatile memory devices;

a peripheral device region containing active driver circuit devices; and

a first stepped surface region between the peripheral device region and the memory device region containing a plurality of passive driver circuit devices.

2. The device of Claim 1, further comprising:

a stack of alternating layers including electrically insulating layers and electrically conductive layers located over a substrate, wherein the first stepped surface region contains first portions of the electrically insulating layers and first portions of the electrically conductive layers, and the first stepped region is located on a first side of the stack;

a second stepped surface region containing second portions of the electrically insulating layers and second portions of the electrically conductive layers located on a second side of the stack;

a plurality of semiconductor channels located in the memory device region in the stack, wherein at least one end portion of each of the plurality of semiconductor channels extends substantially perpendicular to a top surface of the substrate;

a plurality of charge storage elements, each charge storage element located adjacent to a respective one of the plurality of semiconductor channels;

a plurality of passive device contact via structures extending substantially perpendicular to the top surface of the substrate to the respective first portions of the electrically conductive layers in the first stepped surface region; and

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a plurality of control gate contact via structures extending substantially perpendicular to the top surface of the substrate to the respective second portions of the electrically conductive layers in the second stepped surface region.

3. The device of Claim 2, wherein:

the peripheral device region contains sense amplifiers;

the second stepped surface region comprises a word line stepped surface region; and

the second portions of the electrically conductive layers comprise a plurality of control gate electrodes extending substantially parallel to the top surface of the substrate, and the plurality of control gate electrodes comprise at least a first control gate electrode located in the first device level and a second control gate electrode located in the second device level.

4. The device of Claim 3, wherein:

the plurality of passive driver circuit devices comprise a plurality of capacitors;

the first portions of the electrically conductive layers comprise a plurality of capacitor electrodes;

the first portions of the electrically insulating layers comprise capacitor dielectrics located between the capacitor electrodes; and

the respective first and the second portions of each of the electrically conductive layer are located at the same level above the substrate and are electrically insulated from each other.

5. The device of Claim 3, wherein the plurality of passive driver circuit devices comprises a plurality of resistors.

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6. A device comprising a set of capacitors, the device comprising:

a stack of alternating layers including electrically insulating layers and electrically conductive layers located over a substrate, wherein each underlying electrically conductive layer that is located within the stack and has at least one overlying electrically conductive layer that laterally extends farther than the underlying electrically conductive layer to form a stepped surface region on a side of the stack;

a dielectric material portion located over the stepped surface region of the stack, wherein an interface between the dielectric material portion and the stack includes a contiguous set of horizontal surfaces and vertical surfaces to provide the stepped surface region;

a set of dielectric fill material portions located within trenches that vertically extend through the stack of alternating layers and laterally contact sidewalls of the stack of alternating layers in the stepped surface region; and

a plurality of contact via structures in contact with respective electrically conductive layers within the stack of alternating layers,

wherein the electrically conductive layers constitute conductive components of a set of capacitors and a subset of the electrically insulating layers constitutes node dielectrics of the set of capacitors, wherein each capacitor in the set comprises:

a first node that includes an underlying electrically conductive layer of a respective vertically neighboring pair and a respective contact via structure that extends upward from the underlying electrically conductive layer and through the dielectric material portion; and

a second node that includes an overlying electrically conductive layer of the respective vertically neighboring pair and a respective contact via structure that extends

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upward from the overlying electrically conductive layer and through the dielectric material portion.

7. The device of Claim 6, wherein:

each of the trenches is entirely filled with a dielectric material of a respective dielectric fill material portion;

all sidewall surfaces of the electrically conductive layers within the stack of alternating layers are in contact with a surface selected from sidewall surfaces of the set of dielectric fill material portions and sidewall surfaces of the dielectric material portion;

an entire interface between an electrically conductive layer within the stack of alternating layers and the set of dielectric fill material portions is a contiguous interface; and

the contiguous interface is substantially vertical throughout an entirety thereof.

8. The device of Claim 7, wherein:

the interface between the electrically conductive layer and the set of dielectric fill material portions adjoins an interface between the electrically conductive layer and the dielectric material portion;

a combination of the interface between the electrically conductive layer and the set of dielectric fill material portions and the interface between the electrically conductive layer and the dielectric material portion includes all sidewall surfaces of the electrically conductive layer;

the set of dielectric fill material portions is a contiguous set of material portions and contact the dielectric material portion; and

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the dielectric material portion is a retro-stepped dielectric material portion in which a horizontal cross-sectional area of the dielectric material portion at a horizontal plane is not less than a horizontal cross-sectional area of the dielectric material portion at any horizontal plane that is more proximal to the substrate.

9. The device of Claim 6, wherein:

each capacitor within the set of capacitors comprises two pairs of vertically neighboring electrically conductive layers;

the first node of the capacitor includes an underlying electrically conductive layer of a first vertically neighboring pair and an electrically conductive layer of a second vertically neighboring pair; and

the second node of the capacitor includes an overlying electrically conductive layer of the first vertically neighboring pair and another electrically conductive layer of the second vertically neighboring pair.

10. The device of Claim 9, wherein:

the underlying electrically conductive layer of the first vertically neighboring pair and the electrically conductive layer of the second vertically neighboring pair are electrically shorted through two contact via structures and a first conductive line structure; and

the overlying electrically conductive layer of the first vertically neighboring pair and the other electrically conductive layer of the second vertically neighboring pair are electrically shorted through two additional contact via structures and a second conductive line structure.

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11. The device of Claim 9, wherein:

the set of capacitors comprise at least a first capacitor and a second capacitor;

the first capacitor comprises a first upper pair of vertically neighboring electrically conductive layers and a first lower pair of vertically neighboring electrically conductive layers;

the second capacitor comprises a second upper pair of vertically neighboring electrically conductive layers and a second lower pair of vertically neighboring electrically conductive layers;

the second upper pair of vertically neighboring electrically conductive layers overlies the first upper pair of vertically neighboring electrically conductive layers;

the first upper pair of vertically neighboring electrically conductive layers overlies the first lower pair of vertically neighboring electrically conductive layers; and

the first lower pair of vertically neighboring electrically conductive layers overlies the second lower pair of vertically neighboring electrically conductive layers.

12. The device of Claim 11, wherein a sum of an upper overlap area between the vertically neighboring electrically conductive layers within the first upper pair and a lower overlap area between the vertically neighboring electrically conductive layers within the first lower pair is substantially the same as the sum of an upper overlap area between the vertically neighboring electrically conductive layers within the second upper pair and a lower overlap area between the vertically neighboring electrically conductive layers within the second lower pair.

13. The device of Claim 11, wherein:

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each capacitor within the set of capacitors has a substantially same total overlap area between vertically neighboring electrically conductive layers contained therein; and

the set of capacitors is located in at least one of a kerf region, a first stepped surface region between a peripheral device region and a memory device region, and a second stepped surface region which comprises a stepped track between the kerf region and the peripheral device region.

14. The device of Claim 6, further comprising a monolithic three-dimensional memory device located over the substrate, the monolithic three-dimensional memory device comprising:

additional control gate portions of the electrically conductive layers located at the same levels as the electrically conductive layers of the stack;

a memory opening extending through the stack;

a memory film located within the memory opening; and

a semiconductor channel located within the memory film.

15. The device of Claim 14, wherein:

the set of capacitors is a component of a peripheral device of the monolithic three-dimensional memory device;

the monolithic three-dimensional memory device is a vertical NAND memory device;

the additional control gate portions of the electrically conductive layers comprise, or are electrically connected to, a respective word line of the vertical NAND memory device;

the substrate comprises a silicon substrate;

the vertical NAND memory device comprises an array of monolithic three-dimensional NAND strings over the silicon substrate;

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at least one memory cell in the first device level of the three-dimensional array of NAND strings is located over another memory cell in the second device level of the three-dimensional array of NAND strings;

the silicon substrate contains an integrated circuit comprising a driver circuit for the memory device located thereon; and

the three-dimensional array of NAND strings comprises:

a plurality of semiconductor channels, wherein at least one end portion of each of the plurality of semiconductor channels extends substantially perpendicular to a top surface of the silicon substrate;

a plurality of charge storage elements, each charge storage element located adjacent to a respective one of the plurality of semiconductor channels; and

a plurality of control gate electrodes having a strip shape extending substantially parallel to the top surface of the silicon substrate, the plurality of control gate electrodes comprise at least a first control gate electrode located in the first device level and a second control gate electrode located in the second device level.

16. A method of forming a memory device comprising:

forming a plurality of memory devices in a memory device region;

forming a plurality of passive devices outside the memory device region; and

forming a conductive layer in one deposition step such that a first portion of the conductive layer comprises a portion of at least one of the passive device and a second portion of the conductive layer forms a portion of at least one memory device.

17. The method of Claim 16, further comprising:

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forming a stack comprising an alternating plurality of electrically insulating layers and second material layers over a substrate;

forming trenches extending through the stack of alternating layers, wherein sidewalls of a patterned portion of the stack of alternating layers are physically exposed;

forming a patterned stack comprising an alternating plurality of the electrically insulating layers and electrically conductive layers, wherein the electrically conductive layers in the patterned stack are formed at each level of the second material layers, and the patterned stack is laterally contacted by a set of dielectric fill material portions formed within trenches; and

forming a plurality of contact via structures on the electrically conductive layers, wherein:

portions of the electrically conductive layers located in a first stepped surface region between a peripheral device region and a memory device region constitute at least a portion of passive devices; and

forming the conductive layer comprises forming at least one of the electrically conductive layers or at least one of the plurality of contact via structures.

18. The method of Claim 17, wherein:

the passive devices comprise capacitors;

a subset of the electrically insulating layers located in the first stepped surface region constitutes node dielectrics of the set of capacitors; and

each capacitor in the set comprises:

a first node that includes an underlying electrically conductive layer of a respective vertically neighboring pair and a respective contact via structure that

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extends upward from the underlying electrically conductive layer and through the dielectric material portion; and

a second node that includes an overlying electrically conductive layer of the respective vertically neighboring pair and a respective contact via structure that extends upward from the overlying electrically conductive layer and through the dielectric material portion.

19. The method of Claim 18, further comprising replacing the second material layers with conductive material portions;

wherein:

the electrically conductive layers in the patterned stack comprises remaining portions of the conductive material portions;

the set of dielectric fill material portions is formed within the trenches after replacement of the second material layers with the conductive material portions; and

the second material layers are replaced with the conductive material portions by:

forming lateral recesses by etching the second material layers by introducing an etchant through one or more of the trenches;

depositing the conductive material portions within the lateral recesses; and

filling the one or more of the trenches with one or more dielectric fill material portions within the set of dielectric fill material portions.

20. The method of Claim 18, further comprising:

filling each of the trenches with a dielectric material of a respective dielectric fill material portion;

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forming a stepped surface region in which each underlying second material layer laterally extends farther than any overlying second material layer thereof; and

forming a dielectric material portion over the stepped surface region.

21. The method of Claim 20, further comprising:

forming a support pillar trench through the alternating stack;

forming a dielectric pillar structure within the support pillar trench by depositing a first dielectric fill material;

forming lateral separation trenches through the alternating stack; and

forming dielectric trench fill structures by depositing a second dielectric fill material, wherein:

the set of dielectric fill material portions comprise the dielectric pillar structure and the dielectric trench fill structures;

the support pillar trench laterally extends along a same lateral direction as stepped surfaces within the stepped surface region; and

the lateral separation trenches laterally extend along a lateral direction that is perpendicular to the stepped surfaces within the stepped surface region.

22. The method of Claim 20, wherein the dielectric material portion is a retro-stepped dielectric material portion in which a horizontal cross-sectional area of the dielectric material portion at a horizontal plane is not less than a horizontal cross-sectional area of the dielectric material portion at any horizontal plane that is more proximal to the substrate.

23. The method of Claim 18, wherein:

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each capacitor within the set of capacitors comprises two pairs of vertically neighboring electrically conductive layers;

the first node of the capacitor includes an underlying electrically conductive layer of a first vertically neighboring pair and an electrically conductive layer of a second vertically neighboring pair; and

the second node of the capacitor includes an overlying electrically conductive layer of the vertically neighboring pair and another electrically conductive layer of the second vertically neighboring pair.

24. The method of Claim 16, wherein the passive devices comprise resistors.

25. The method of Claim 16, wherein:

forming the plurality of memory devices in a memory device region comprises forming a monolithic three-dimensional memory device located over the substrate; and

the monolithic three-dimensional memory device comprises:

a memory opening extending through the stack;

a memory film formed within the memory opening; and

a semiconductor channel formed within the memory film.

26. The method of Claim 25, wherein:

the passive devices are components of a peripheral device of the monolithic three-dimensional memory device;

the monolithic three-dimensional memory device is a vertical NAND memory device;

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the electrically conductive layers comprise, or are electrically connected to, a respective word line of the vertical NAND memory device;

the substrate comprises a silicon substrate;

the vertical NAND memory device comprises an array of monolithic three-dimensional NAND strings over the silicon substrate;

at least one memory cell in the first device level of the three-dimensional array of NAND strings is located over another memory cell in the second device level of the three-dimensional array of NAND strings;

the silicon substrate contains an integrated circuit comprising a driver circuit for the memory device located thereon; and

the three-dimensional array of NAND strings comprises:

a plurality of semiconductor channels, wherein at least one end portion of each of the plurality of semiconductor channels extends substantially perpendicular to a top surface of the silicon substrate;

a plurality of charge storage elements, each charge storage element located adjacent to a respective one of the plurality of semiconductor channels; and

a plurality of control gate electrodes having a strip shape extending substantially parallel to the top surface of the silicon substrate, the plurality of control gate electrodes comprise at least a first control gate electrode located in the first device level and a second control gate electrode located in the second device level.

27. The method of Claim 25, wherein the first stepped surface region contains first portions of the electrically insulating layers and first portions of the electrically conductive layers, and the first stepped region is located on a first side of the stack.

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28. The method of Claim 27, further comprising forming a second stepped surface region containing second portions of the electrically insulating layers and second portions of the electrically conductive layers located on a second side of the stack during at the same time as forming the first stepped surface region.

29. The method of Claim 28, wherein:

forming the plurality of contact via structures comprises forming a plurality of passive device contact via structures extending substantially perpendicular to the top surface of the substrate to the respective first portions of the electrically conductive layers in the first stepped surface region, and at the same time forming a plurality of control gate contact via structures extending substantially perpendicular to the top surface of the substrate to the respective second portions of the electrically conductive layers in the second stepped surface region;

the peripheral device region contains sense amplifiers;

the second stepped surface region comprises a word line stepped surface region; and

the second portions of the electrically conductive layers comprise a plurality of control gate electrodes extending substantially parallel to the top surface of the substrate, and the plurality of control gate electrodes comprise at least a first control gate electrode located in the first device level and a second control gate electrode located in the second device level.

30. A semiconductor device, comprising:

an alternating stack of first material layers and second material layers located over a substrate;

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at least one pillar structure extending from a first horizontal plane including a top surface of the alternating stack through at least a portion of the alternating stack;

a laterally-extending semiconductor or conductive structure contacting a bottom surface of the at least one pillar structure; and

a contact via structure contacting a top surface of the laterally-extending semiconductor or conductive structure and laterally spaced from the at least one pillar structure,

wherein:

each of the at least one pillar structure comprises at least one doped semiconductor material portion therein; and

each semiconductor material portion within the at least one pillar structure has a doping of a same second conductivity type.

31. The semiconductor device of Claim 30, wherein the contact via structure comprises a metallic via structure and the at least one doped semiconductor material portion comprises electrical dopants of the same second conductivity type at an atomic concentration in a range from 1.0×10^{17} /cm^3 to 1.0×10^{20}/cm^3.

32. The semiconductor device of Claim 30, wherein the at least one doped semiconductor material portion comprises a doped polycrystalline semiconductor material portion contacting inner surfaces of at least one electrically insulating material.

33. The semiconductor structure of Claim 30, further comprising:

a memory opening extending through the alternating stack; and

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a memory stack structure that comprises a memory film located within the memory opening, and a semiconductor channel located within the memory film.

34. The semiconductor device of Claim 33, wherein:

the at least one pillar structure comprises at least a portion of a resistor;

each of the at least one pillar structure comprises a layer stack of at least two dielectric material layers located on an outer sidewall of a respective set of at least one doped semiconductor material portion;

the memory film and the layer stack of at least two dielectric material layers comprise an identical set of dielectric materials; and

the laterally-extending semiconductor or conductive structure consists of at least one single crystalline semiconductor material portion located in the substrate.

35. The semiconductor structure of Claim 34, wherein:

the at least one doped semiconductor material portion comprises a same semiconductor material as the semiconductor channel, and further includes electrical dopants of the same second conductivity type; and

the semiconductor channel is intrinsic or has a doping of a first conductivity type that is the opposite of the second conductivity type.

36. The semiconductor structure of Claim 35, wherein:

the memory stack structure further comprises a drain region having a same second conductivity type of doping as the least one doped semiconductor material portion; and

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a second doped semiconductor material portion of the at least one doped semiconductor material portion comprises a same semiconductor material as the drain region.

37. The semiconductor structure of Claim 34, wherein:

the memory stack structure further comprises an epitaxial channel portion; and

a epitaxial doped semiconductor portion of the at least one doped semiconductor material portion comprises a same semiconductor material as the epitaxial channel portion, and further includes electrical dopants of the same second conductivity type.

38. The semiconductor structure of Claim 34, wherein:

the first material layers are electrically insulating layers; and

the second material layers are electrically conductive layers.

39. The semiconductor structure of Claim 34, wherein:

the first material layers comprise a first electrically insulating material;

the second material layers comprise a second electrically insulating material; and

the memory stack structure extends through another alternating stack of the first material layers and electrically conductive layers located at each level of the second material layers.

40. The semiconductor structure of Claim 30, wherein:

the first material layers comprise electrically insulating layers;

the second material layers comprise electrically conductive layers; and

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the laterally-extending semiconductor or conductive structure comprises one of the electrically conductive layers.

41. The semiconductor structure of Claim 40, wherein each of the at least one pillar structure consists of a respective doped semiconductor material portion.

42. The semiconductor structure of Claim 41, wherein:

the alternating stack comprises a stepped surface region in which each electrically conductive layer having at least one overlying electrically conductive layer laterally extends farther than any overlying electrically conductive layer;

a retro-stepped dielectric material portion overlies the stepped surface region; and

the at least one pillar structure, the laterally-extending semiconductor or conductive structure, and the contact via structure collectively constitute a resistor structure.

43. The semiconductor structure of Claim 42, further comprising additional resistor structures, each additional resistor structure comprising:

at least one additional pillar structure extending from the first horizontal plane to a respective electrically conductive layer located at a different level from the laterally-extending semiconductor or conductive structure;

a respective electrically conductive layer contacting a bottom surface of the at least one additional pillar structure; and

an additional contact via structure contacting a top surface of the respective electrically conductive layer.

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44. The semiconductor structure of Claim 30, further comprising a vertical NAND memory device located over the substrate, wherein:

the vertical NAND memory device comprises a memory stack structure extending through an alternating stack of electrically insulating layers located at each level of the first material layers and electrically conductive layers located at each level of the second material layers;

the electrically conductive layers comprise, or are electrically connected to, a respective word line of the vertical NAND memory device;

the substrate comprises a silicon substrate;

the vertical NAND memory device comprises an array of monolithic three-dimensional NAND strings over the silicon substrate;

at least one memory cell in the first device level of the three-dimensional array of NAND strings is located over another memory cell in the second device level of the three-dimensional array of NAND strings;

the silicon substrate contains an integrated circuit comprising a driver circuit for the memory device located thereon; and

the three-dimensional array of NAND strings comprises:

a plurality of semiconductor channels, wherein at least one end portion of each of the plurality of semiconductor channels extends substantially perpendicular to a top surface of the silicon substrate;

a plurality of charge storage elements, each charge storage element located adjacent to a respective one of the plurality of semiconductor channels; and

a plurality of control gate electrodes having a strip shape extending substantially parallel to the top surface of the silicon substrate, the plurality of control

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gate electrodes comprise at least a first control gate electrode located in the first device level and a second control gate electrode located in the second device level.

45. The semiconductor structure of Claim 44, wherein the at least one pillar structure comprises at least a portion of a resistor located in at least one of a kerf region, a first stepped surface region between a peripheral device region and a memory device region, a second stepped surface region which comprises a stepped track between the kerf region and the peripheral device region, and a third stepped surface region which comprises a word line contact region containing word line contact via structures.

46. A method of forming at least one resistor structure, comprising:

forming an alternating stack of first material layers and second material layers over a substrate;

forming at least one vertically-extending cavity from a first horizontal plane including a top surface of the alternating stack to a laterally-extending semiconductor or conductive structure, wherein a physically exposed portion of a top surface of the laterally-extending semiconductor or conductive structure is present within a second horizontal plane located in the alternating stack below the first horizontal plane;

forming a resistor comprising a pillar structure within each of the at least one vertically-extending cavity, wherein each pillar structure comprises at least one doped semiconductor material portion, and wherein each semiconductor material within the pillar structure has a doping of a same second conductivity type; and

forming a contact via structure contacting another portion of the top surface of the laterally-extending semiconductor or conductive structure.

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47. The method of Claim 46, wherein:

the contact via structure is formed by deposition of a metallic material; and

the at least one doped semiconductor material portion comprises a doped polycrystalline semiconductor material portion that is formed directly on inner surfaces of at least one electrically insulating material.

48. The method of Claim 46, further comprising:

forming a memory opening extending through the alternating stack;

forming a memory film located within the memory opening; and

forming a semiconductor channel on the memory film.

49. The method of Claim 48, wherein:

the vertically-extending semiconductor material portion and the semiconductor channel are formed by deposition of an intrinsic semiconductor material or a doped semiconductor material having a doping of a first conductivity type that is the opposite of the same conductivity type; and

a first doped semiconductor material portion of at the least one doped semiconductor material portion is formed by:

depositing a vertically-extending semiconductor material portion in each vertically-extending cavity simultaneously with formation of the semiconductor channel; and

implanting electrical dopants of the same second conductivity type into the vertically-extending semiconductor material portion while preventing implantation of

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the electrical dopants of the same second conductivity type into the semiconductor channel.

50. The method of Claim 49, further comprising:

forming a drain region having a doping of the same second conductivity type on the semiconductor channel;

forming a second doped semiconductor material portion on each vertically-extending semiconductor material portion simultaneously with formation of the drain region;

forming an epitaxial channel portion on the substrate, wherein the semiconductor channel is formed on the epitaxial channel portion; and

forming a epitaxial doped semiconductor portion comprising a same semiconductor material as the epitaxial channel portion at a bottom portion of each vertically-extending cavity.

51. The method of Claim 48, wherein the laterally-extending semiconductor or conductive structure consists of at least one single crystalline semiconductor material portion located in the substrate.

52. The method of Claim 48, further comprising replacing the second material layers with electrically conductive layers within a memory device region including the memory opening, wherein:

the first material layers are electrically insulating layers; and

the second material layers comprise a dielectric material and are not removed within a region including the at least one vertically-extending cavity.

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53. The method of Claim 48, further comprising replacing the second material layers with electrically conductive layers, wherein the first material layers are electrically insulating layers.

54. The method of Claim 53, wherein the laterally-extending semiconductor or conductive structure comprises one of the electrically conductive layers.

55. The method of Claim 54, wherein each of the pillar structure consists of a respective doped semiconductor material portion that is deposited within a respective vertically-extending cavity formed on the laterally-extending semiconductor or conductive structure.

56. The method of Claim 55, further comprising:

forming a stepped surface region in which each electrically conductive layer having at least one overlying electrically conductive layer laterally extends farther than any overlying electrically conductive layer; and

forming a retro-stepped dielectric material portion the stepped surface region.

57. The method of Claim 56, wherein:

the pillar structure, the laterally-extending semiconductor or conductive structure, and the contact via structure collectively constitute a resistor structure; and

the method further comprises forming additional resistor structures simultaneously with formation of the resistor structure, each additional resistor structure comprising:

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at least one additional pillar structure extending from the first horizontal plane to a respective electrically conductive layer located at a level from the laterally-extending semiconductor or conductive structure;

a respective electrically conductive layer contacting a bottom surface of a respective additional pillar structure; and

an additional contact via structure contacting a top surface of the respective electrically conductive layer.

58. The method of Claim 46, further comprising forming a vertical NAND memory device over the substrate, wherein:

the vertical NAND memory device comprises a memory stack structure extending through an alternating stack of electrically insulating layers located at each level of the first material layers and electrically conductive layers located at each level of the second material layers;

the electrically conductive layers comprise, or are electrically connected to, a respective word line of the vertical NAND memory device;

the substrate comprises a silicon substrate;

the vertical NAND memory device comprises an array of monolithic three-dimensional NAND strings over the silicon substrate;

at least one memory cell in the first device level of the three-dimensional array of NAND strings is located over another memory cell in the second device level of the three-dimensional array of NAND strings;

the silicon substrate contains an integrated circuit comprising a driver circuit for the memory device located thereon; and

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the three-dimensional array of NAND strings comprises:

a plurality of semiconductor channels, wherein at least one end portion of each of the plurality of semiconductor channels extends substantially perpendicular to a top surface of the silicon substrate;

a plurality of charge storage elements, each charge storage element located adjacent to a respective one of the plurality of semiconductor channels; and

a plurality of control gate electrodes having a strip shape extending substantially parallel to the top surface of the silicon substrate, the plurality of control gate electrodes comprise at least a first control gate electrode located in the first device level and a second control gate electrode located in the second device level.

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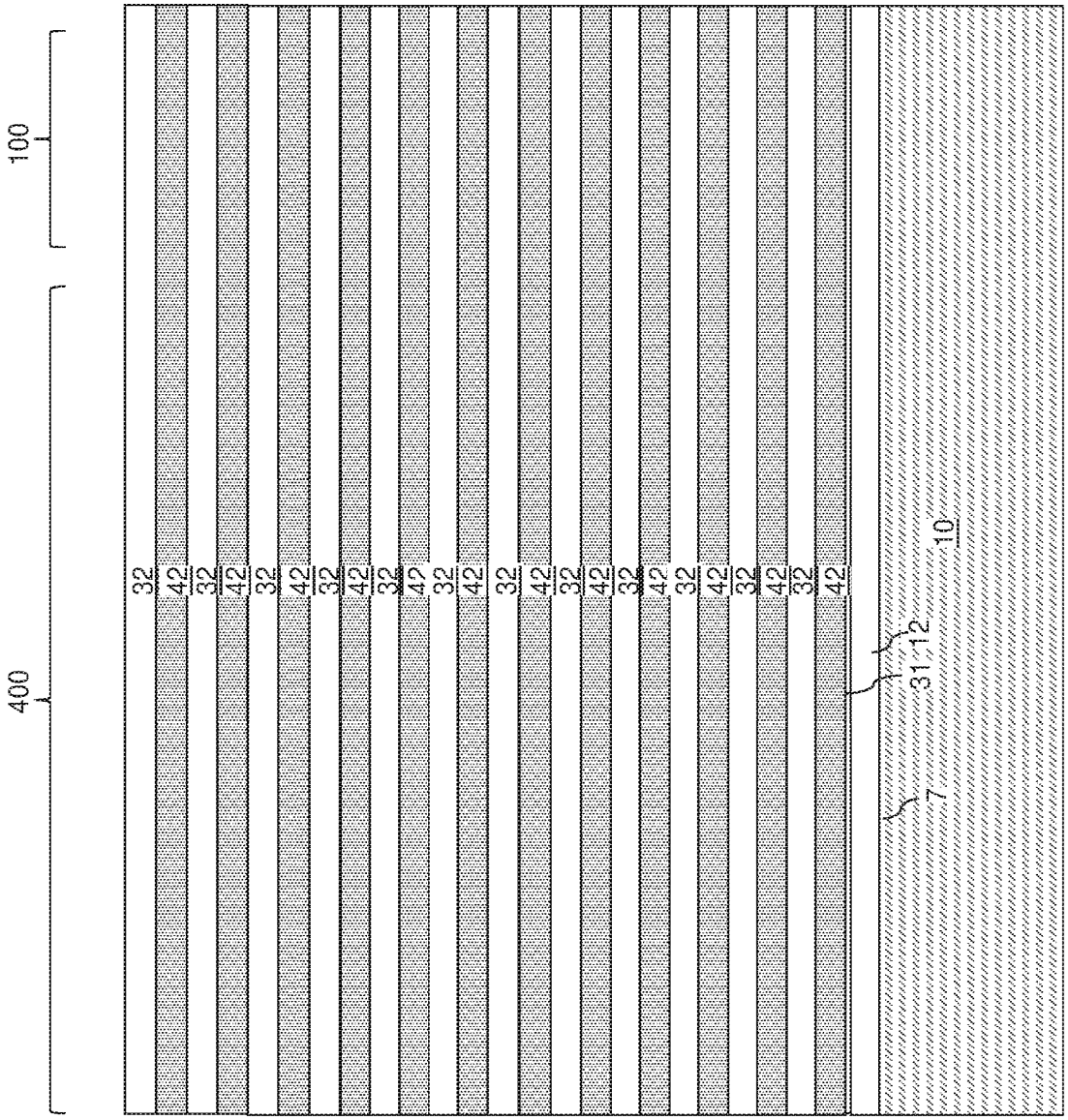


FIG. 1

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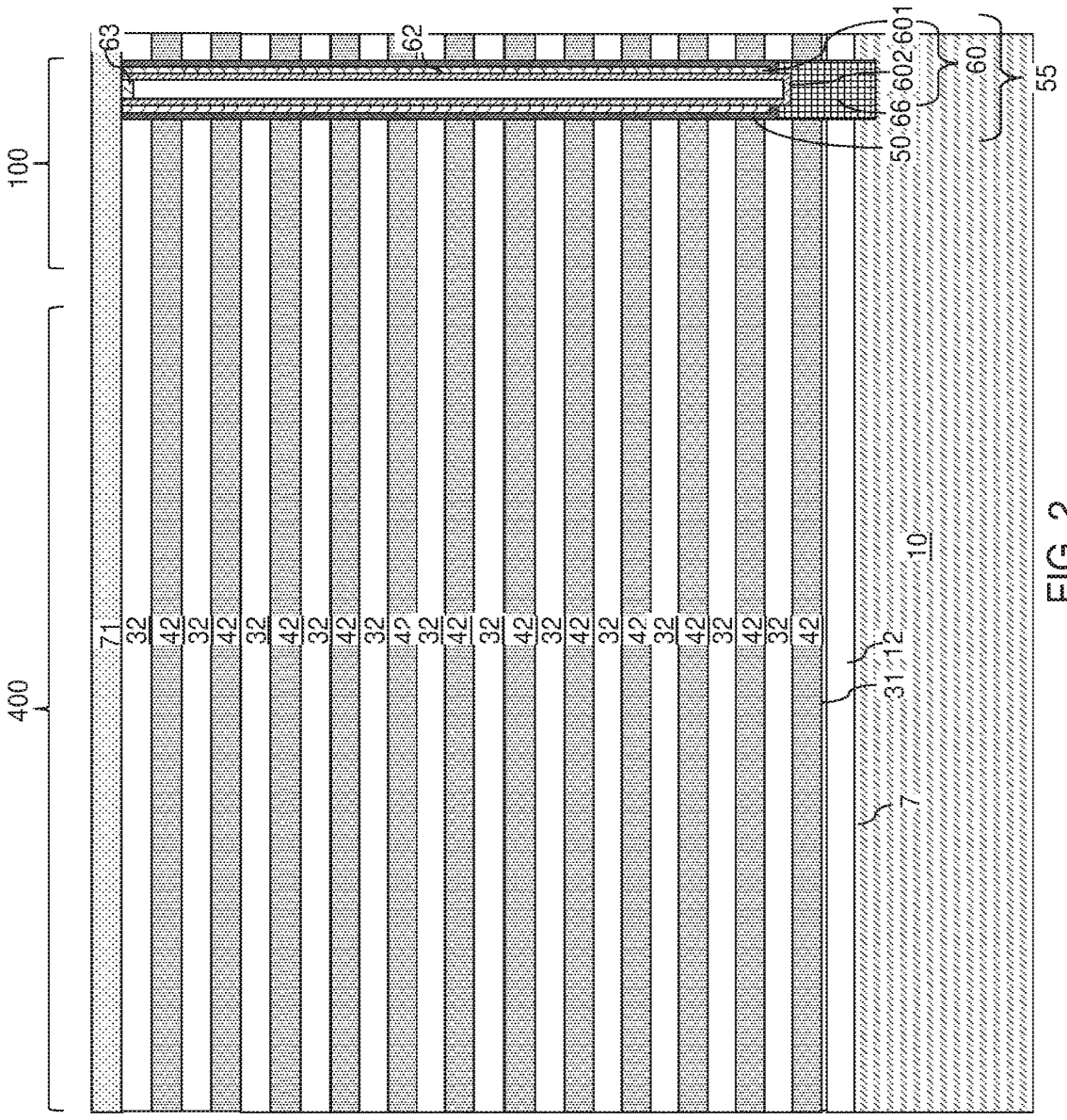


FIG. 2

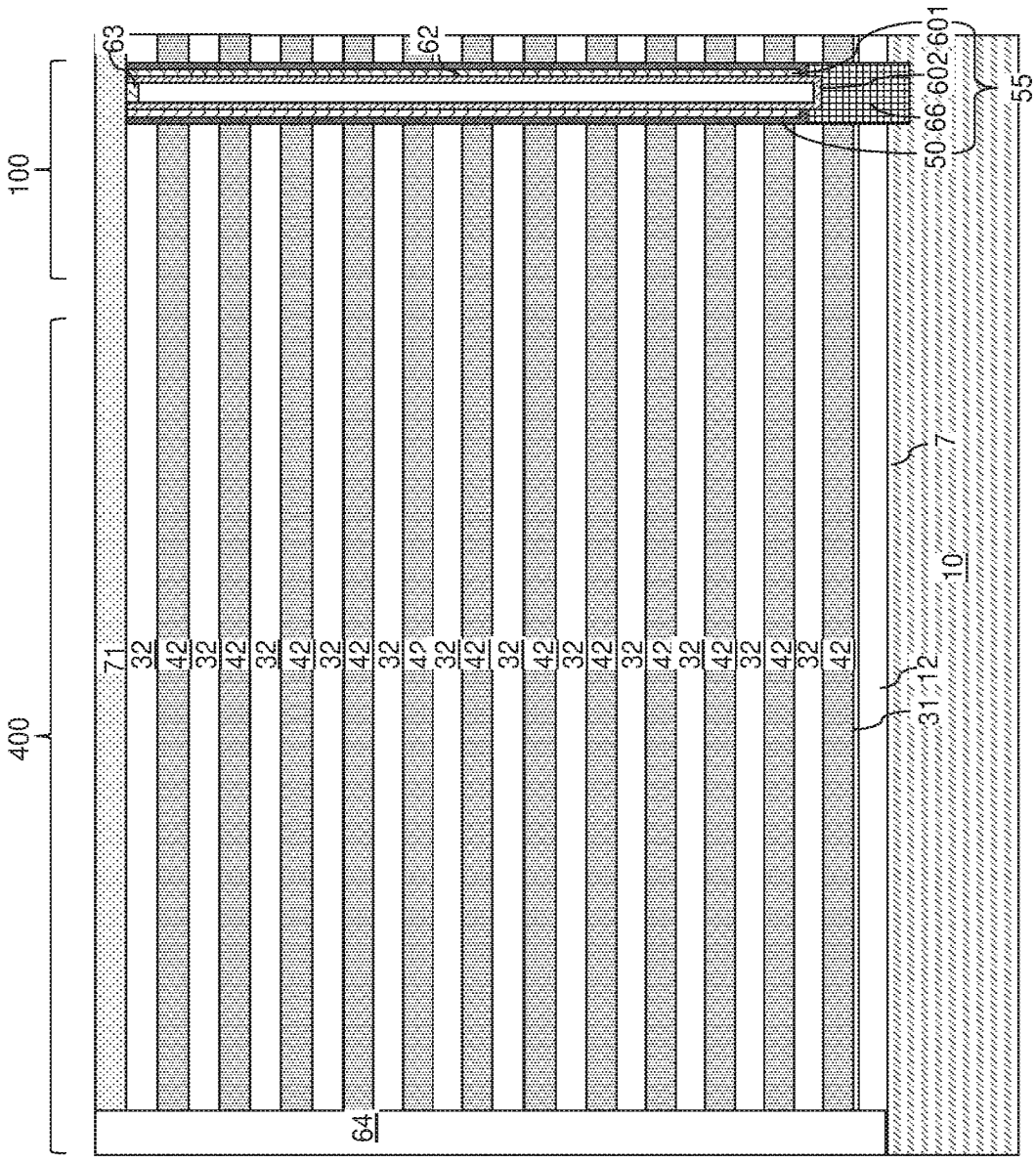


FIG. 3

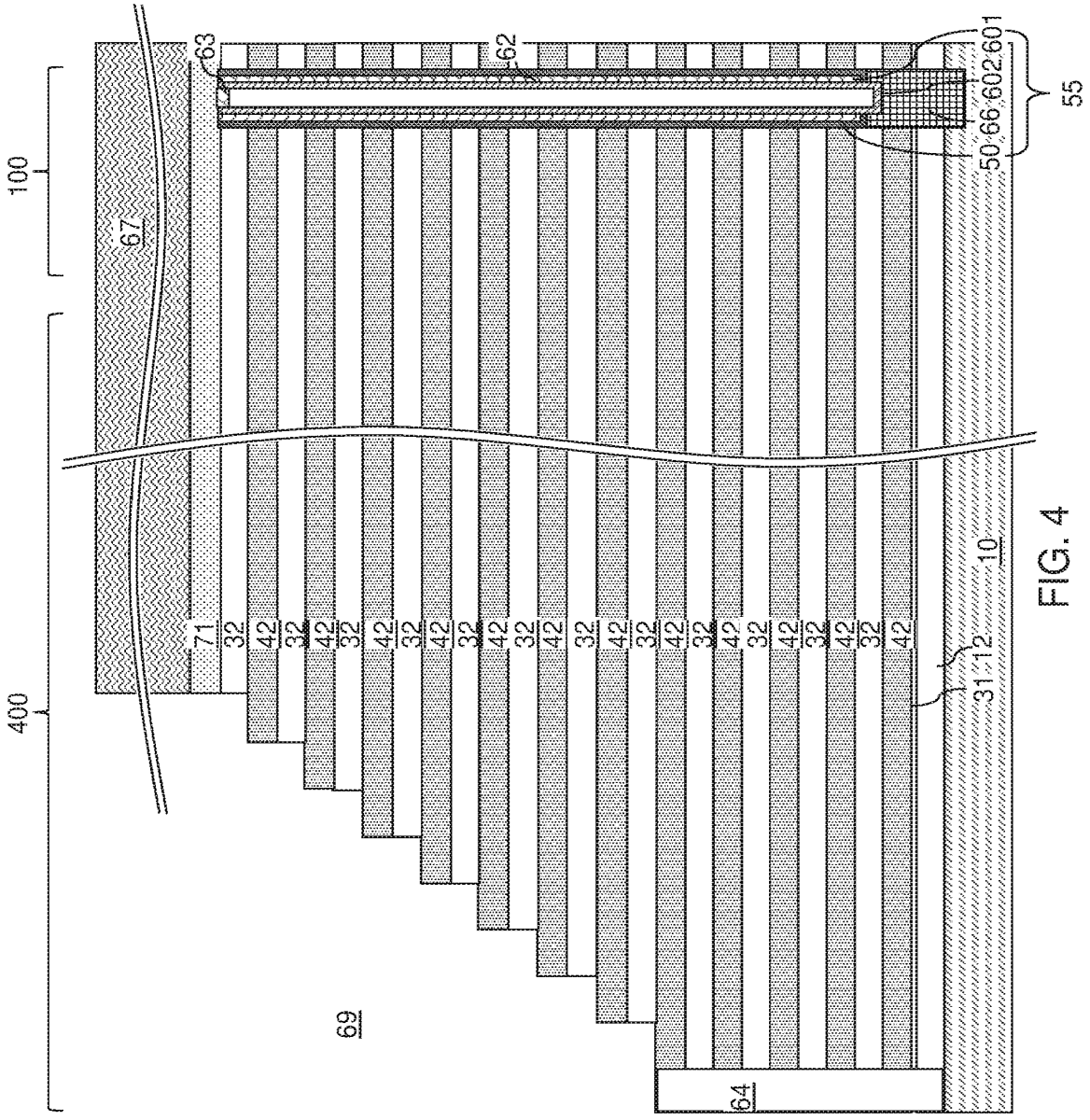


FIG. 4

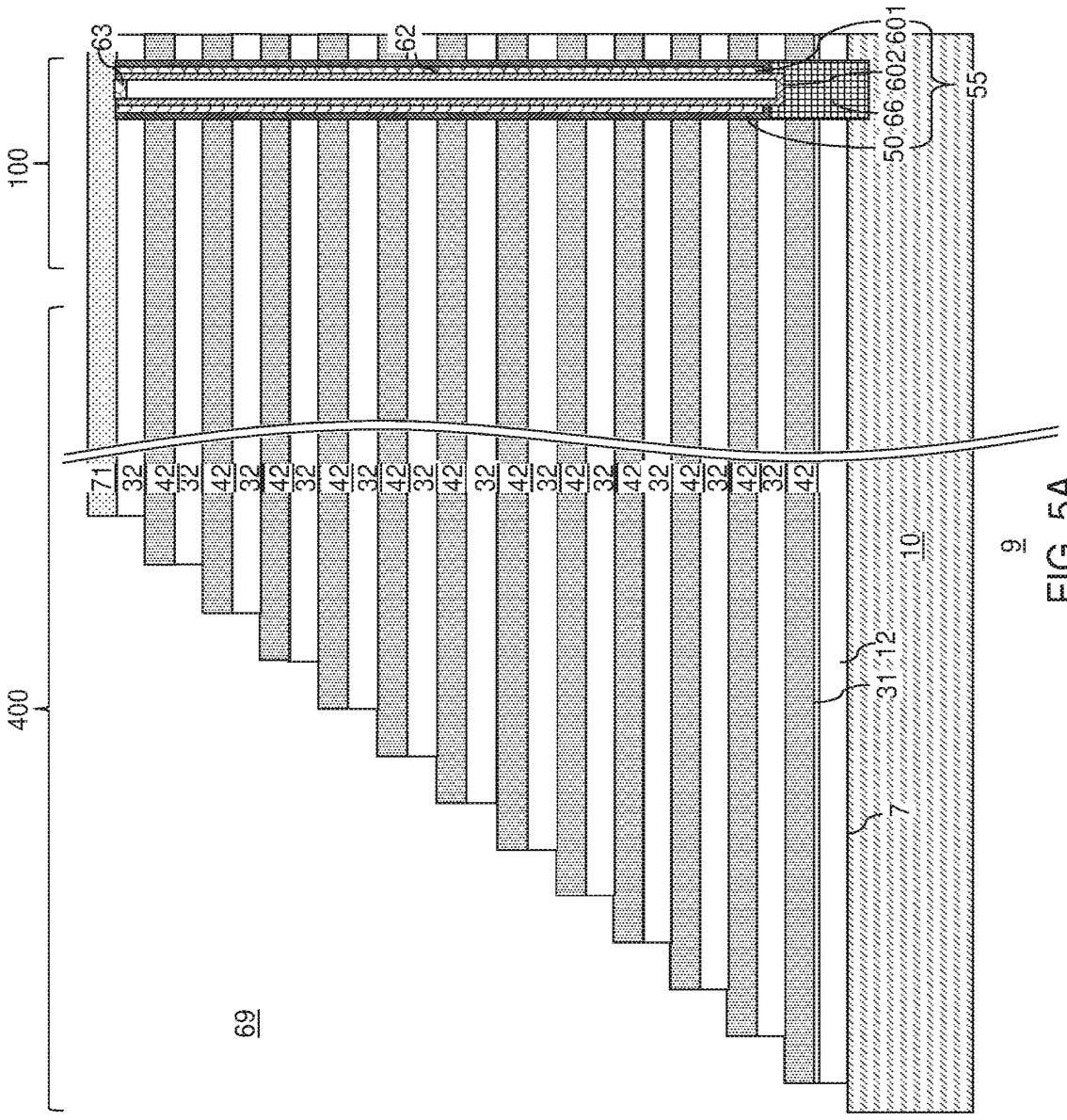


FIG. 5A

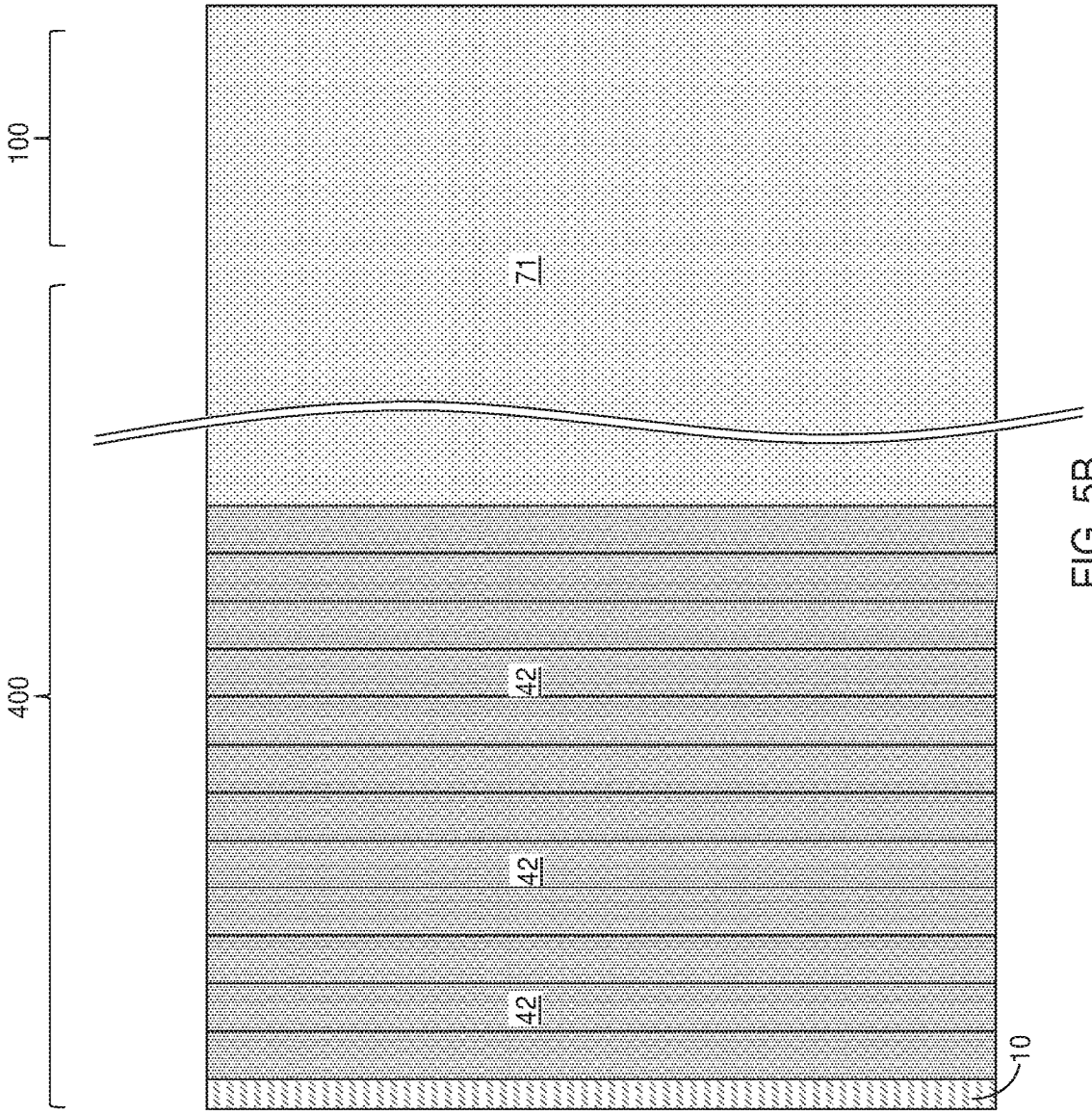


FIG. 5B

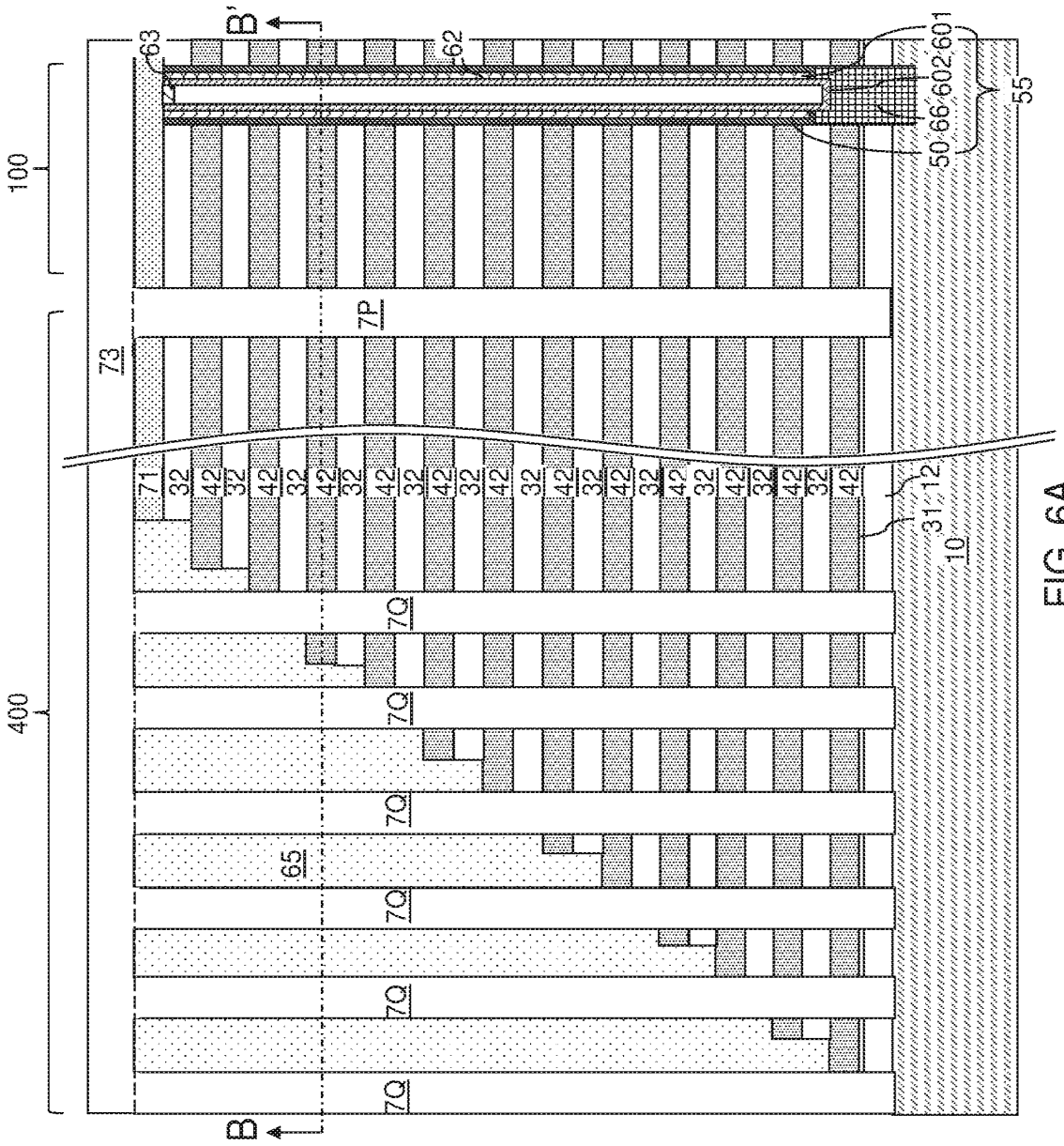


FIG. 6A

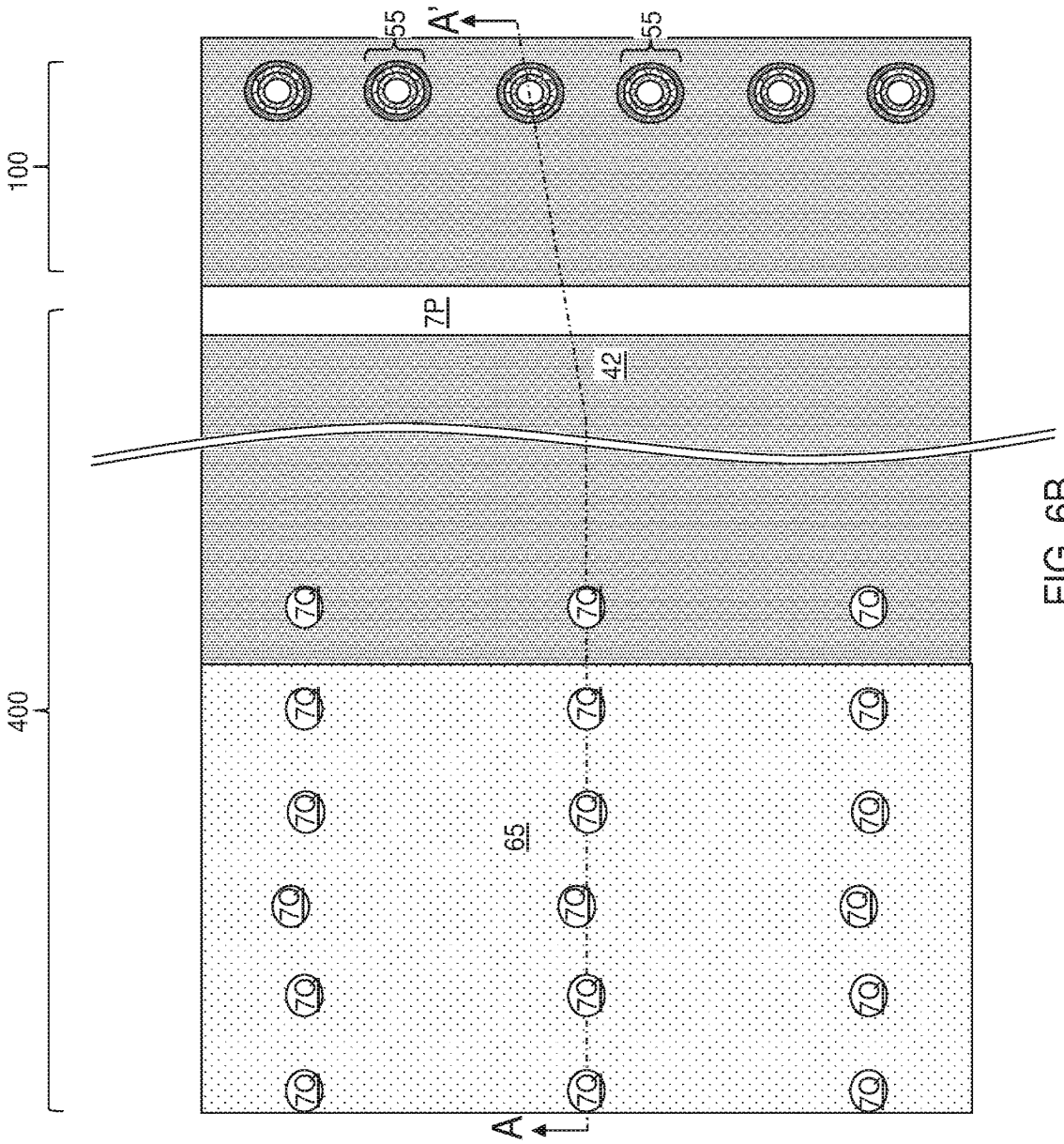


FIG. 6B

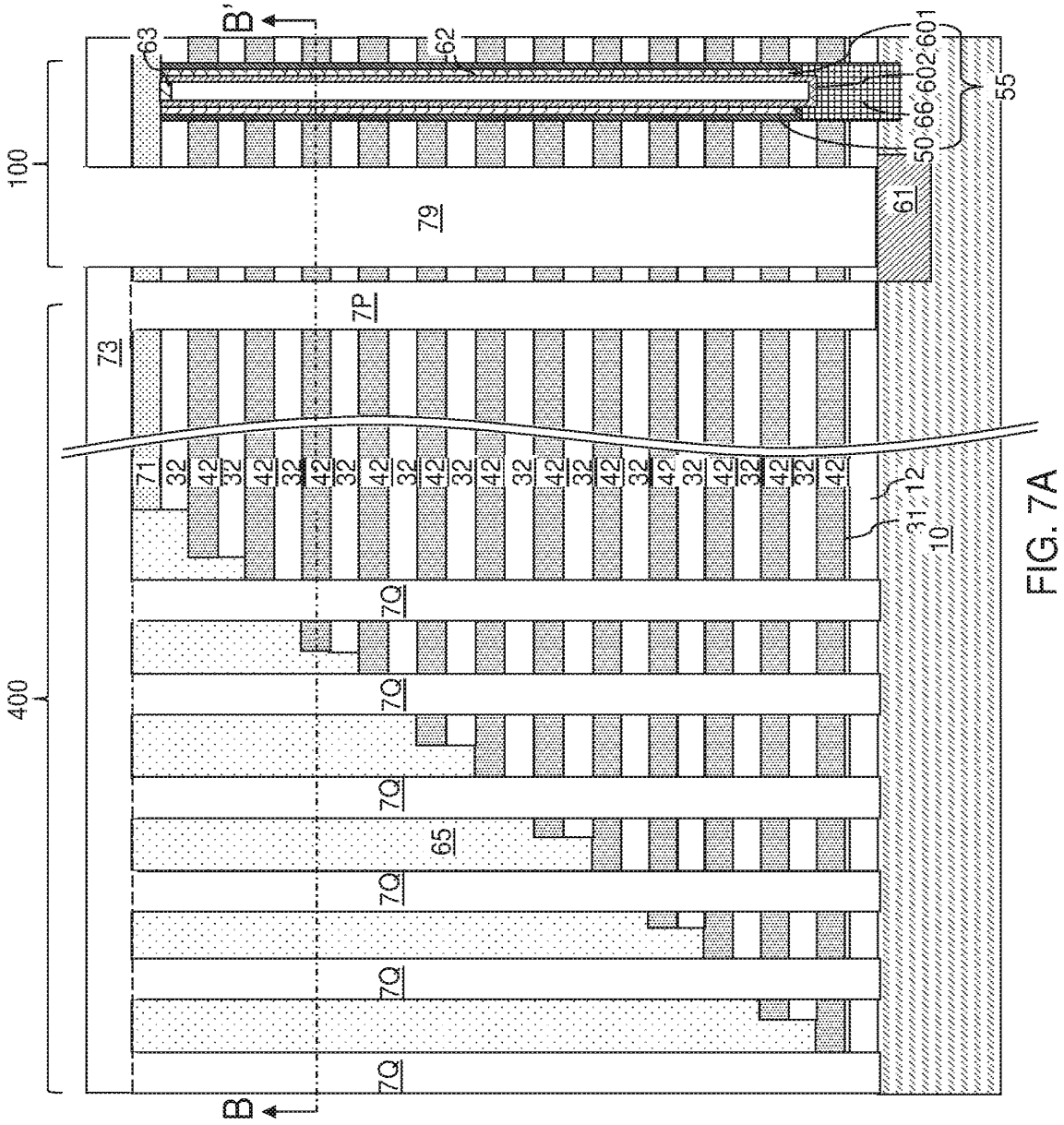


FIG. 7A

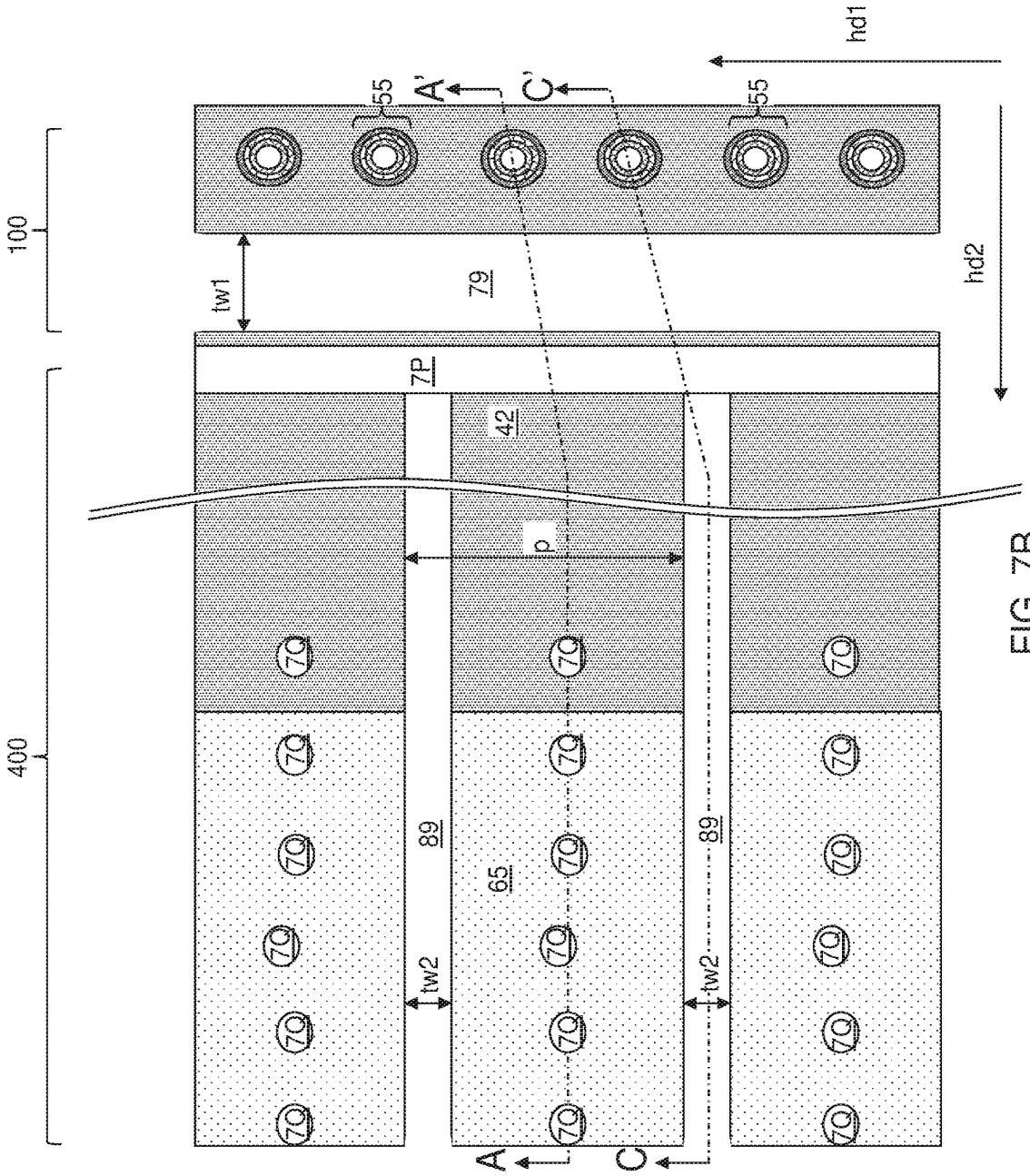


FIG. 7B

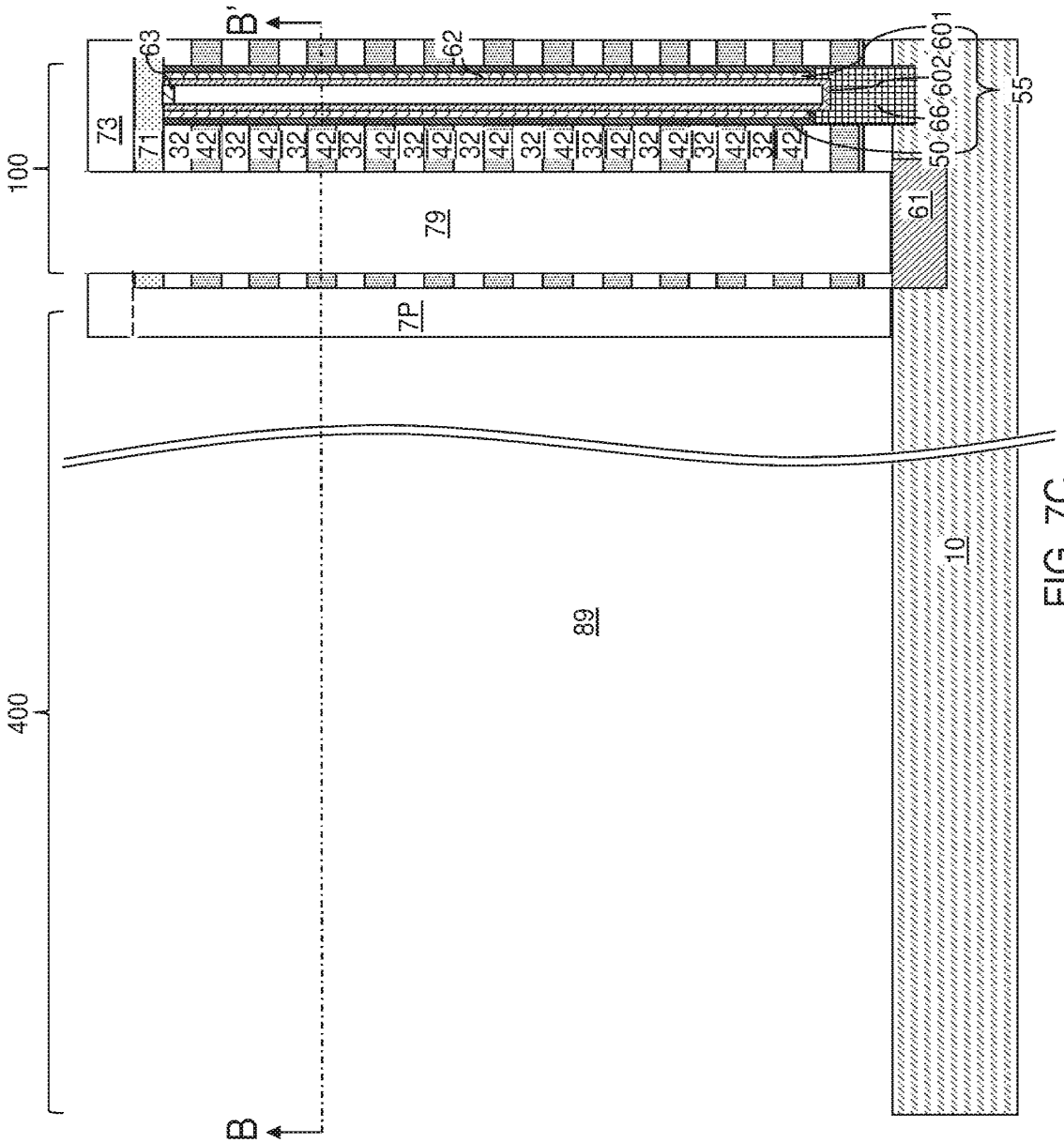


FIG. 7C

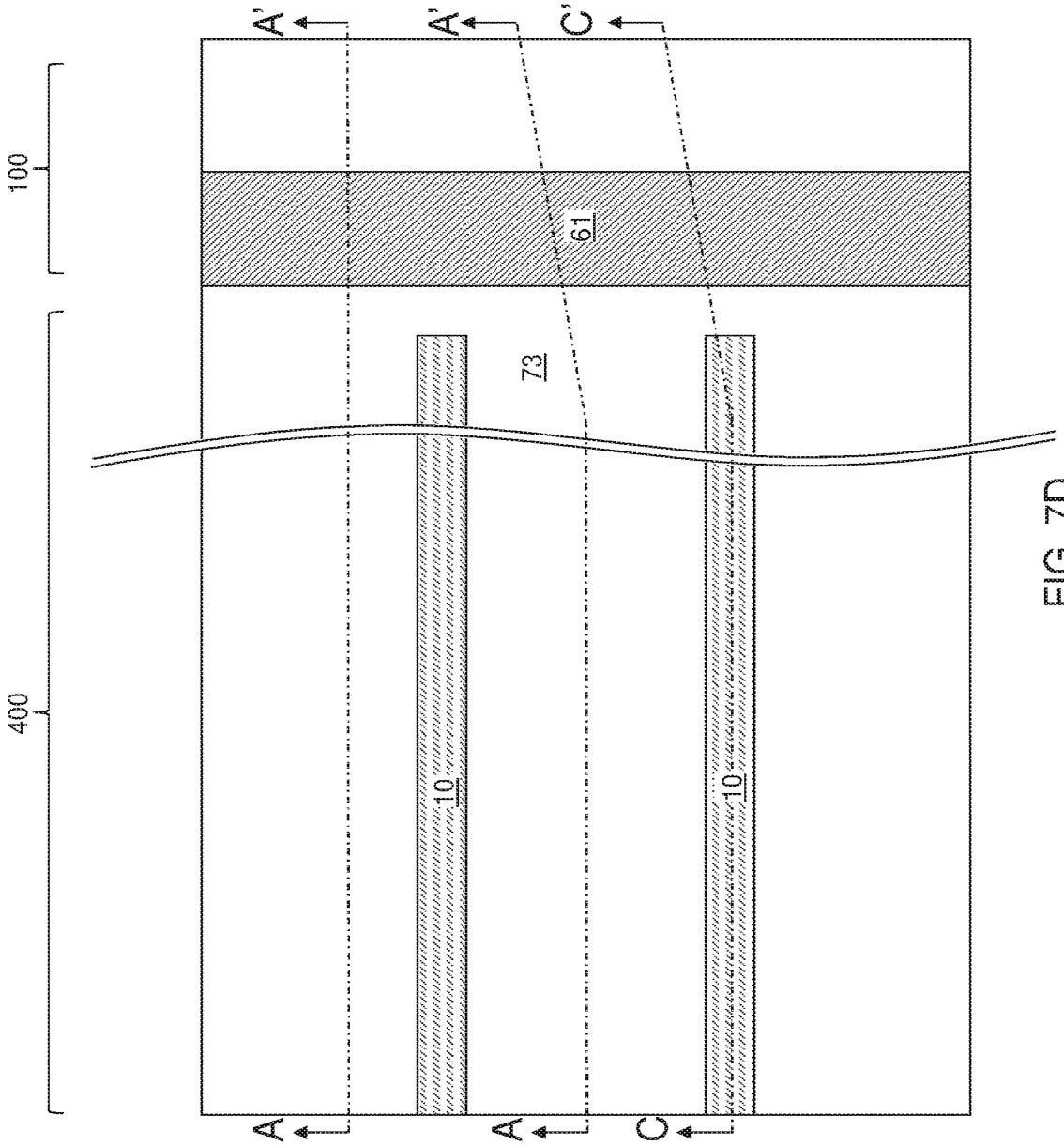


FIG. 7D

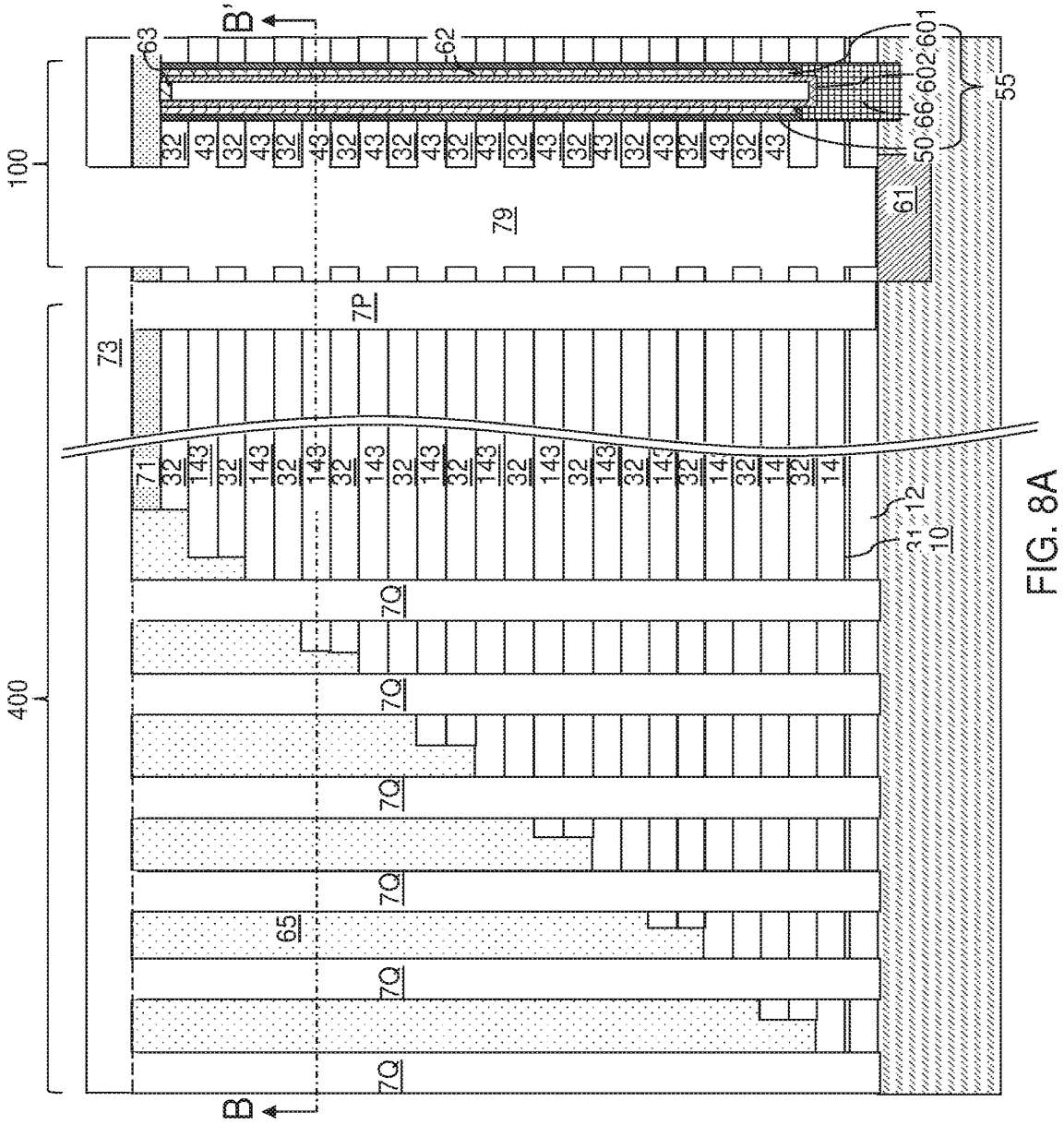

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79
100
400
73
7P
7Q
65
71
143
32
43
14
12
31
10

FIG. 8A

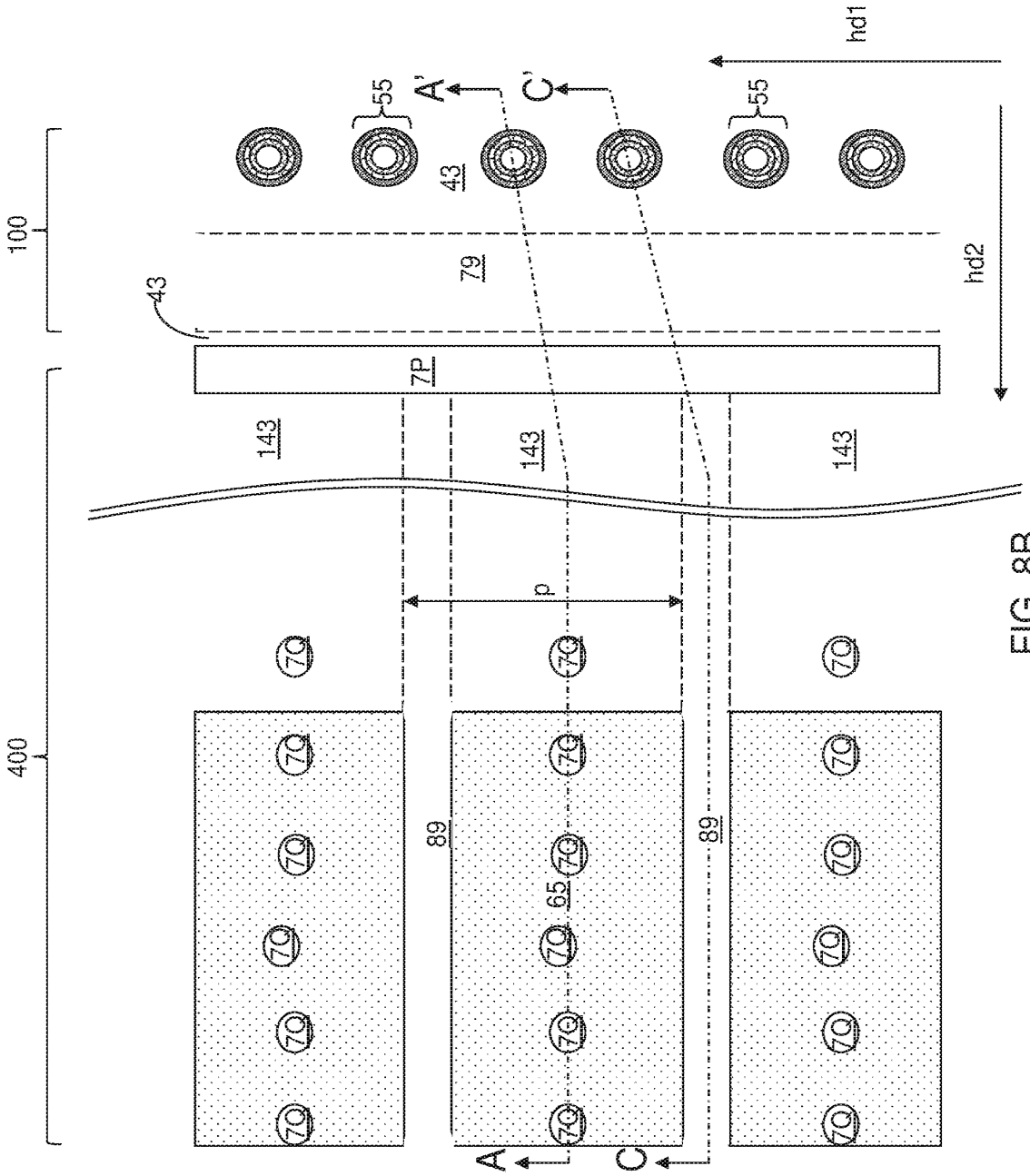


FIG. 8B

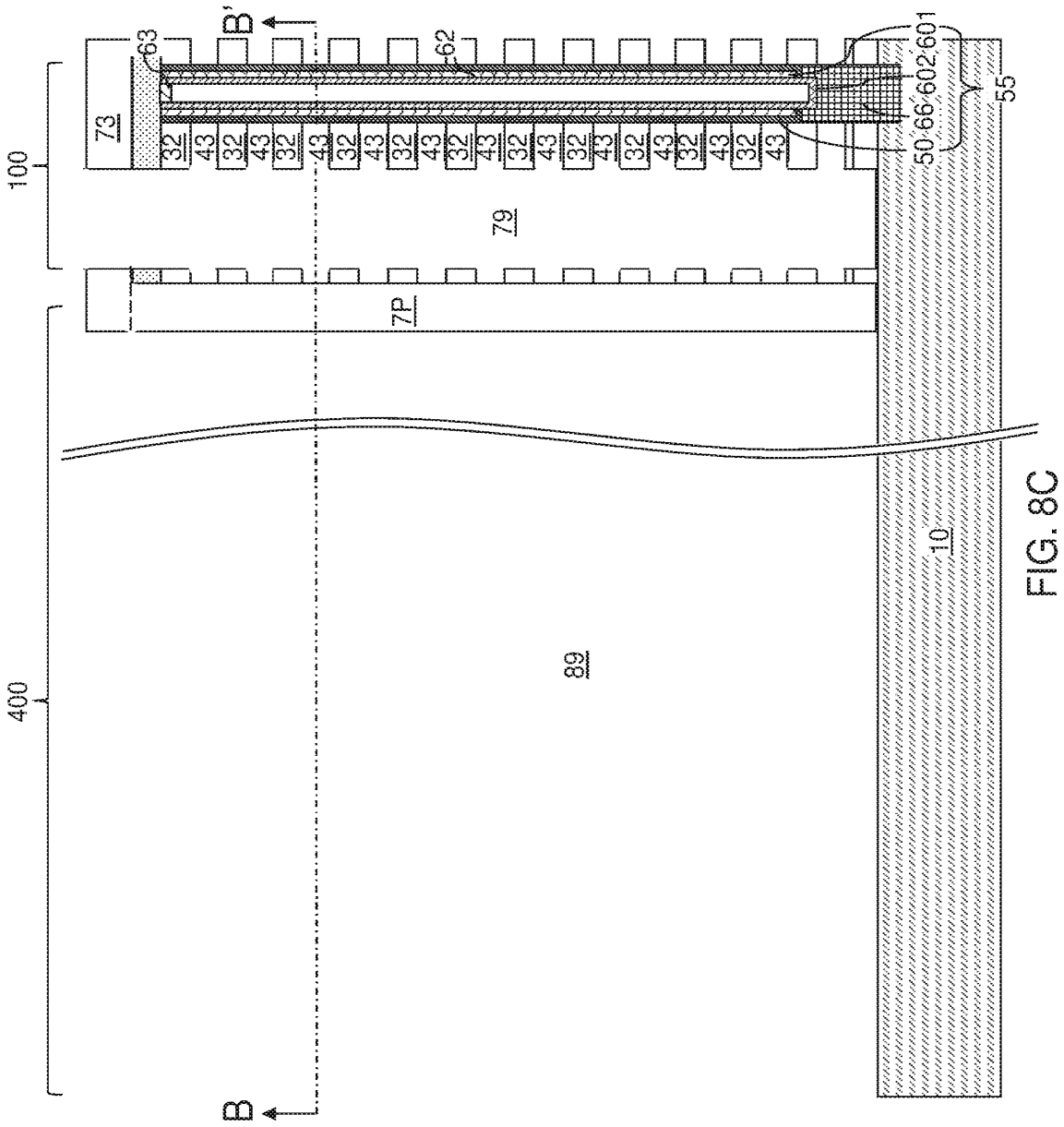


FIG. 8C

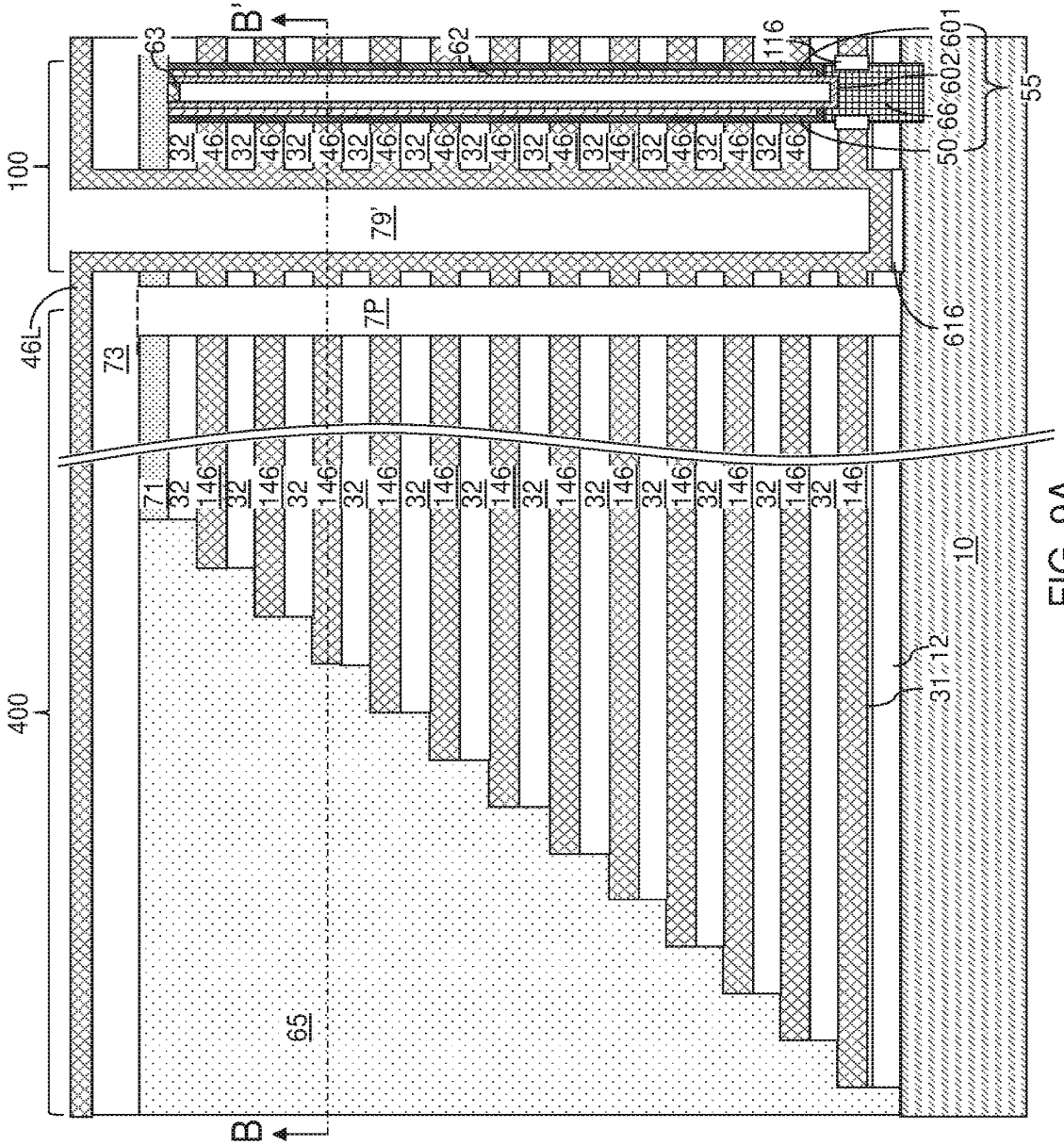

B'
B
63
62
116
55
50/66/602/601
100
79'
7P
46L
73
616
71
32
146
46
65
400
31/12
10

FIG. 9A

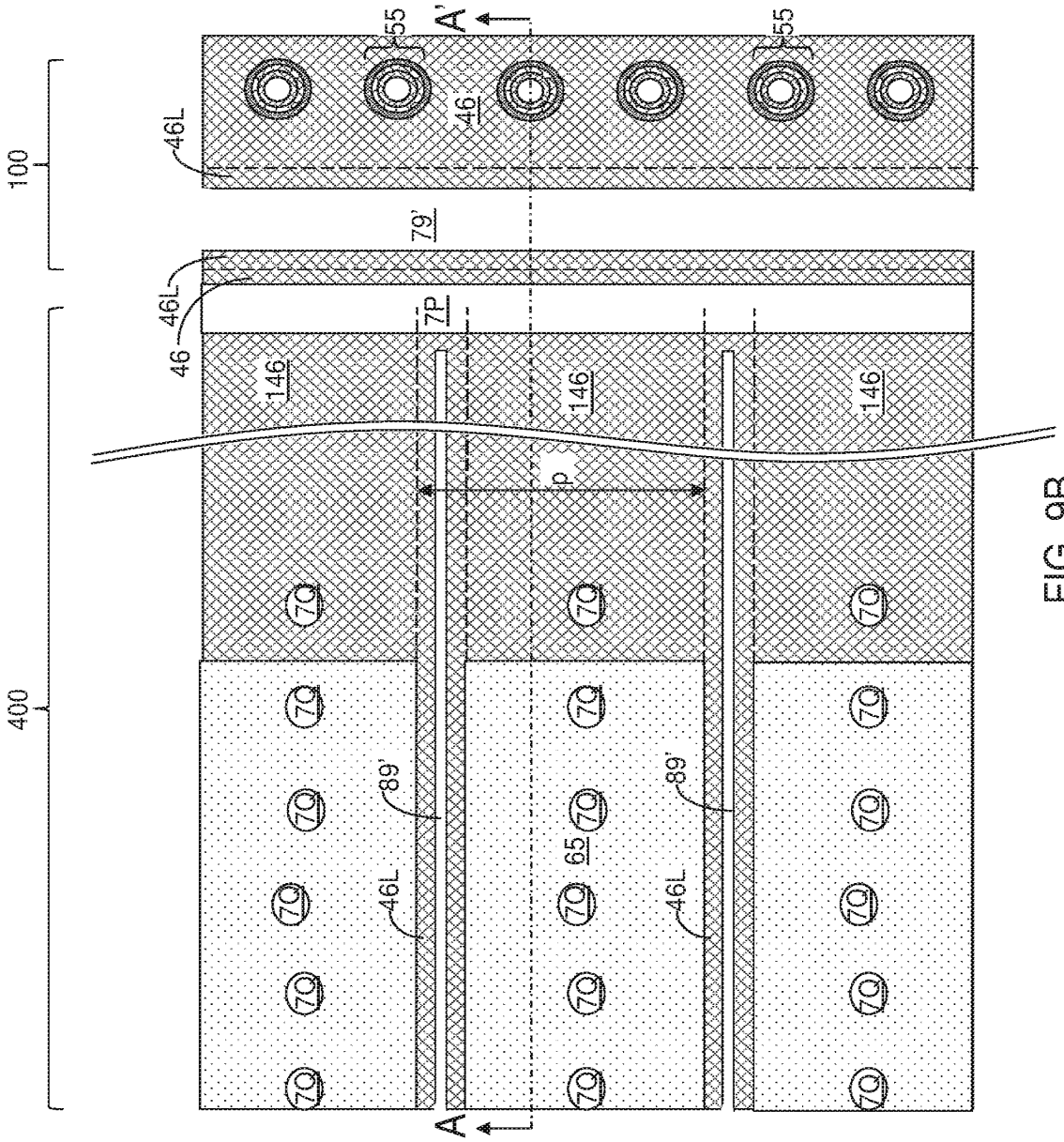

A'
55
55
46
46L
100
79'
46L
46
7P
146
146
146
p
70
89'
89'
65
46L
46L
400
A

FIG. 9B

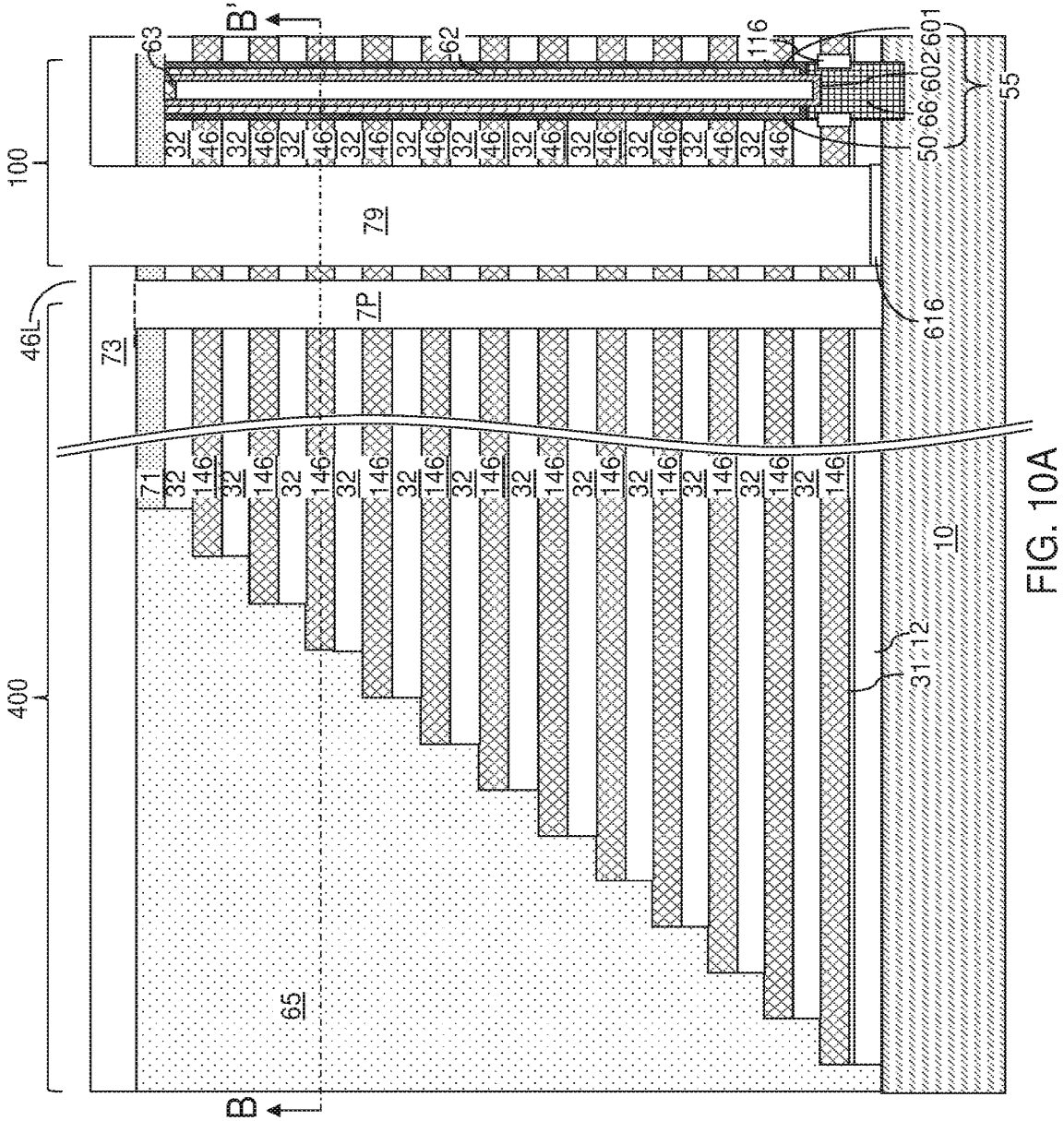

B'
B
63
62
116
55
50/66/602/601
100
79
7P
46L
73
616
71
32
146
46
65
400
31/12
10

FIG. 10A

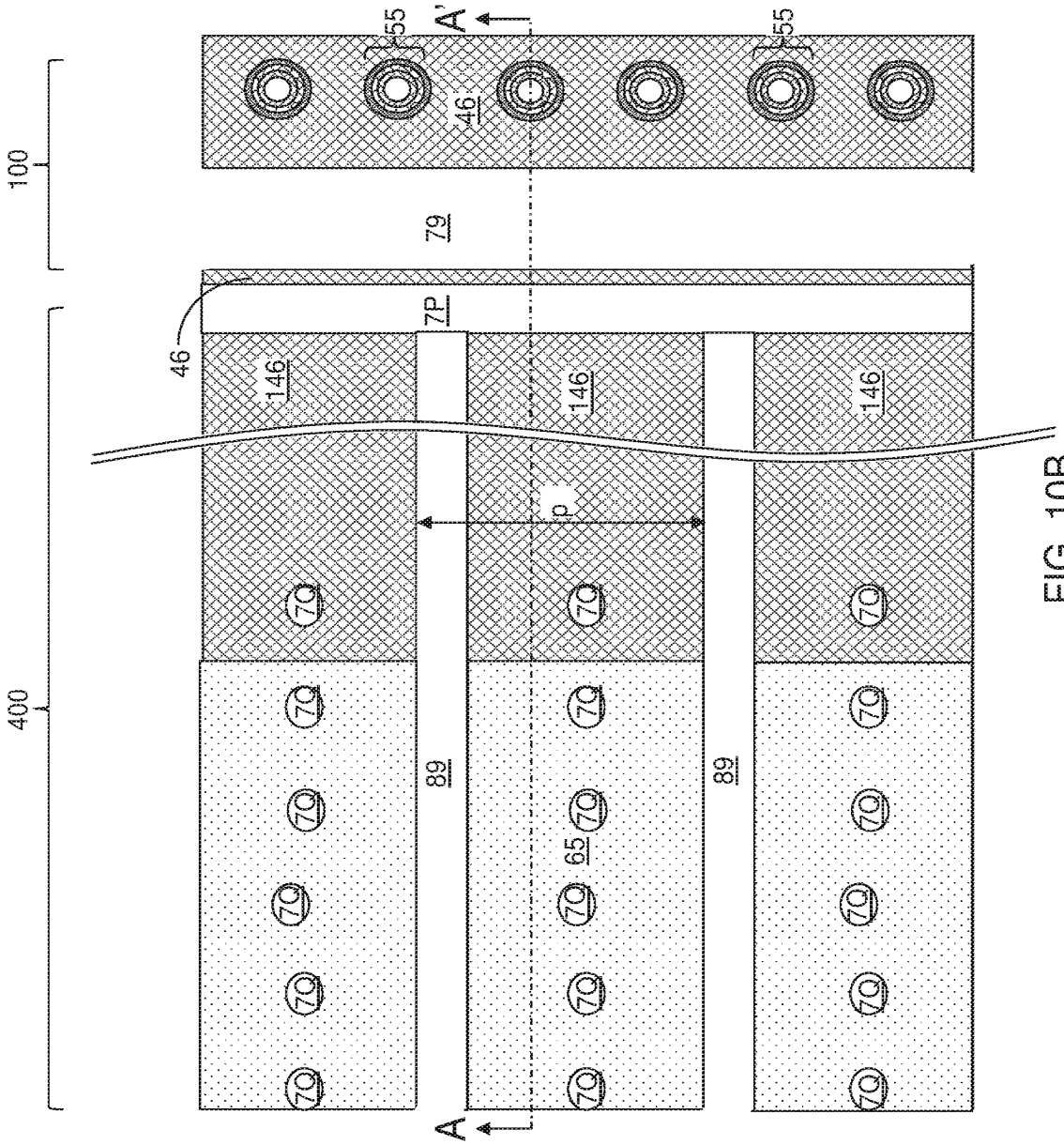


FIG. 10B

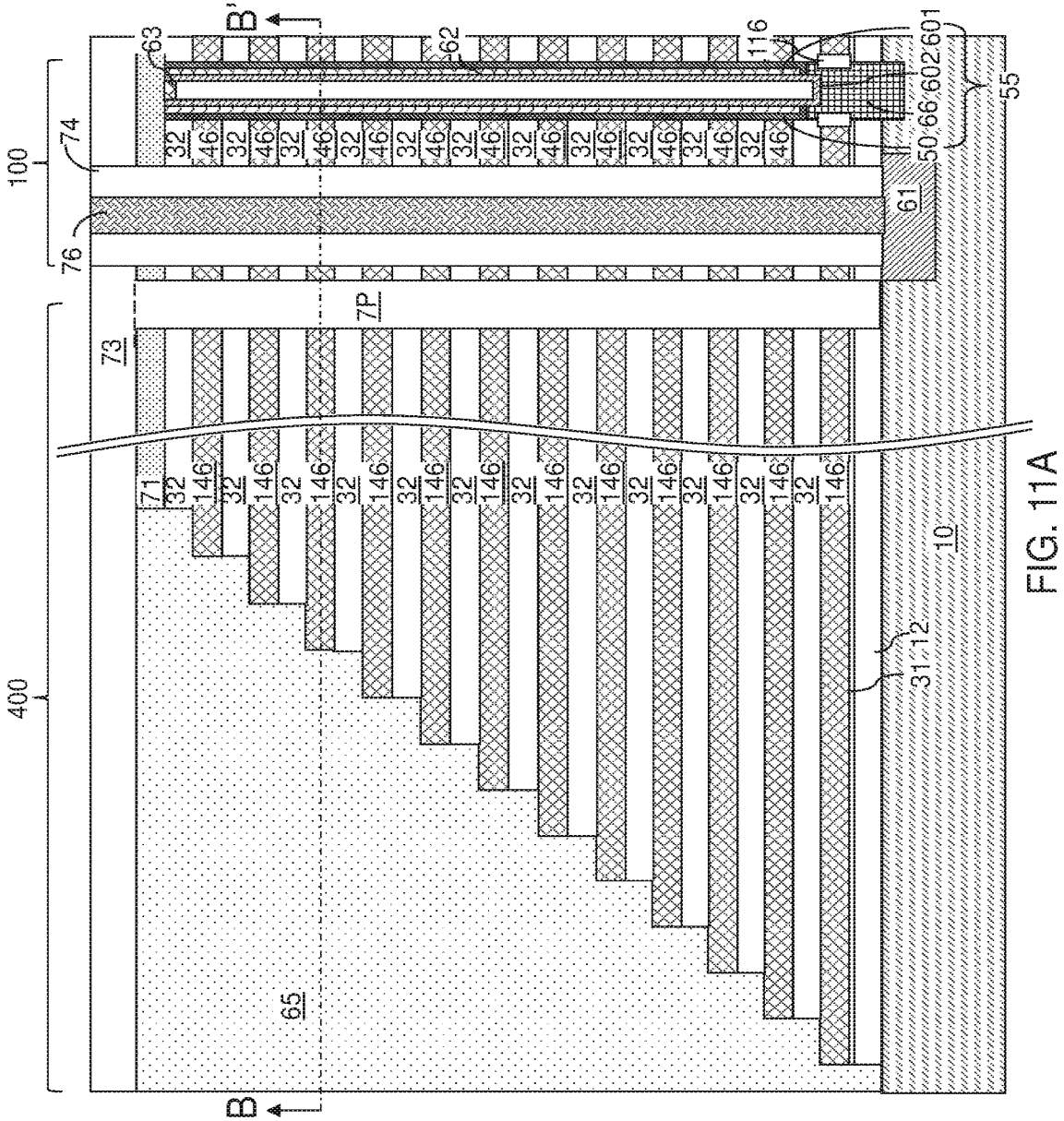

B'
B
63
62
116
55
50
66
602
601
61
74
76
100
400
7P
73
71
65
10
31
12
32
46
146

FIG. 11A

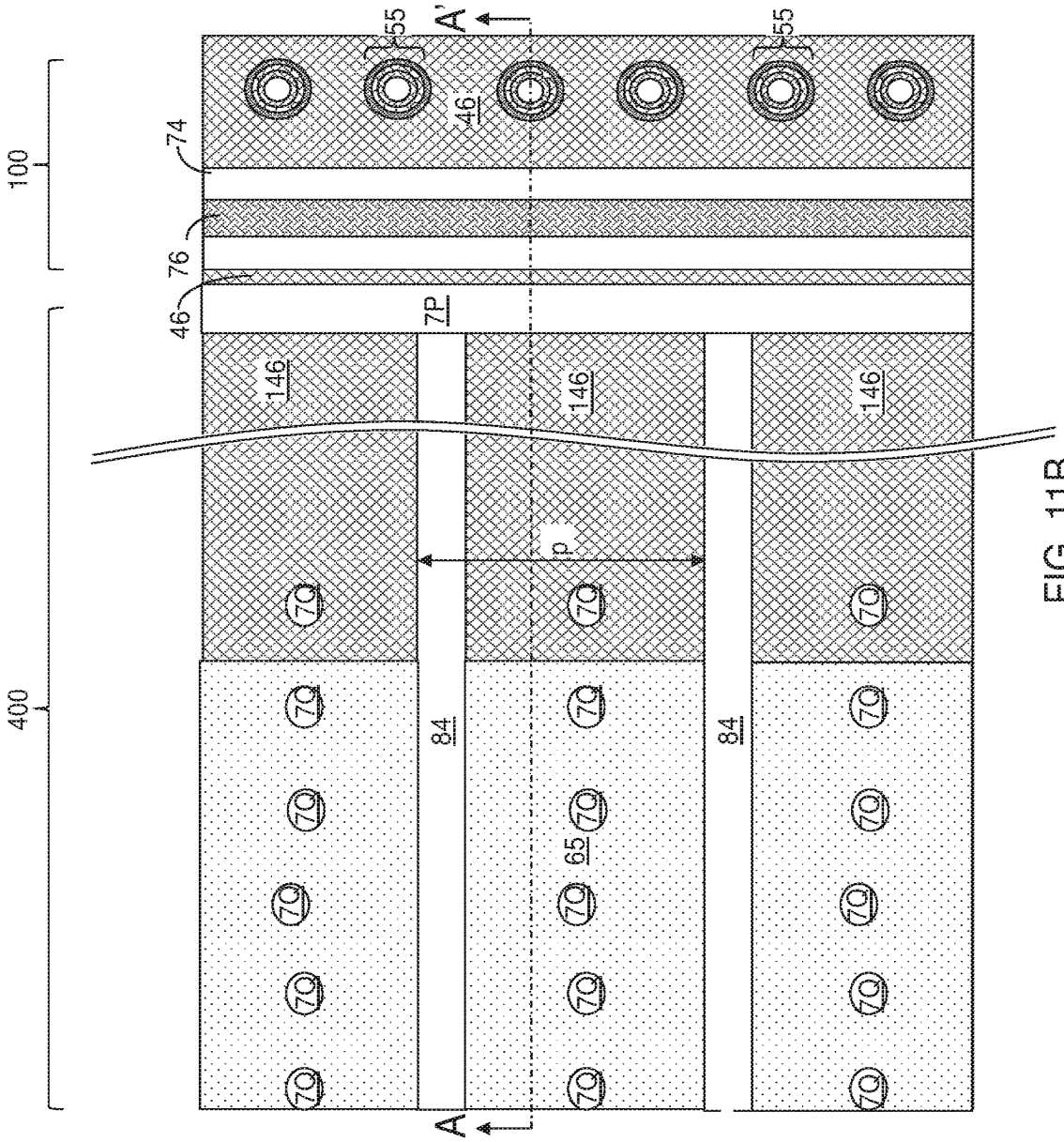


FIG. 11B

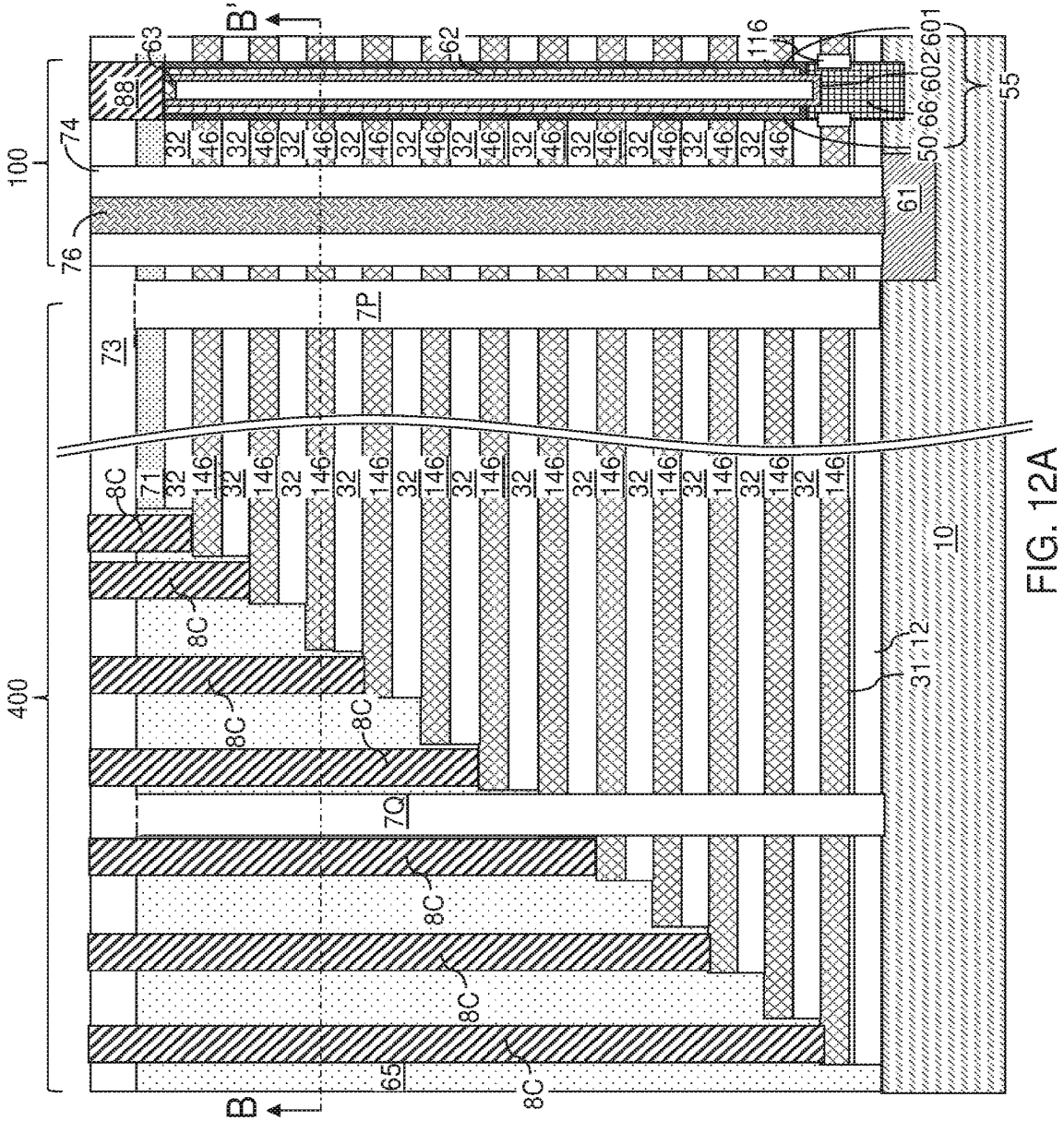

B'
B
63
62
116
55
601
602
66
50
61
88
74
100
76
7P
73
71
8C
146
32
46
31
12
10
400
7Q
65

FIG. 12A

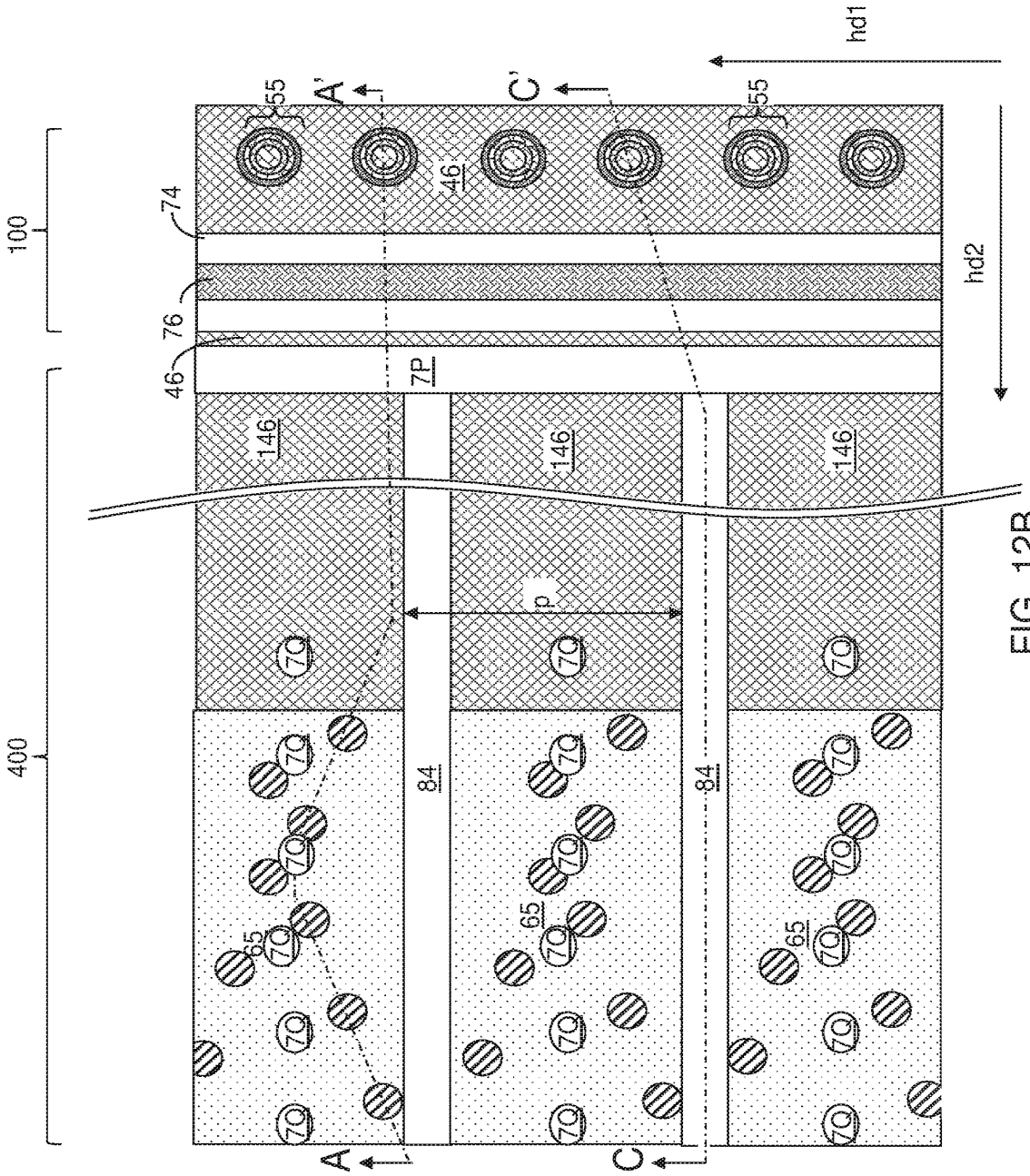


FIG. 12B

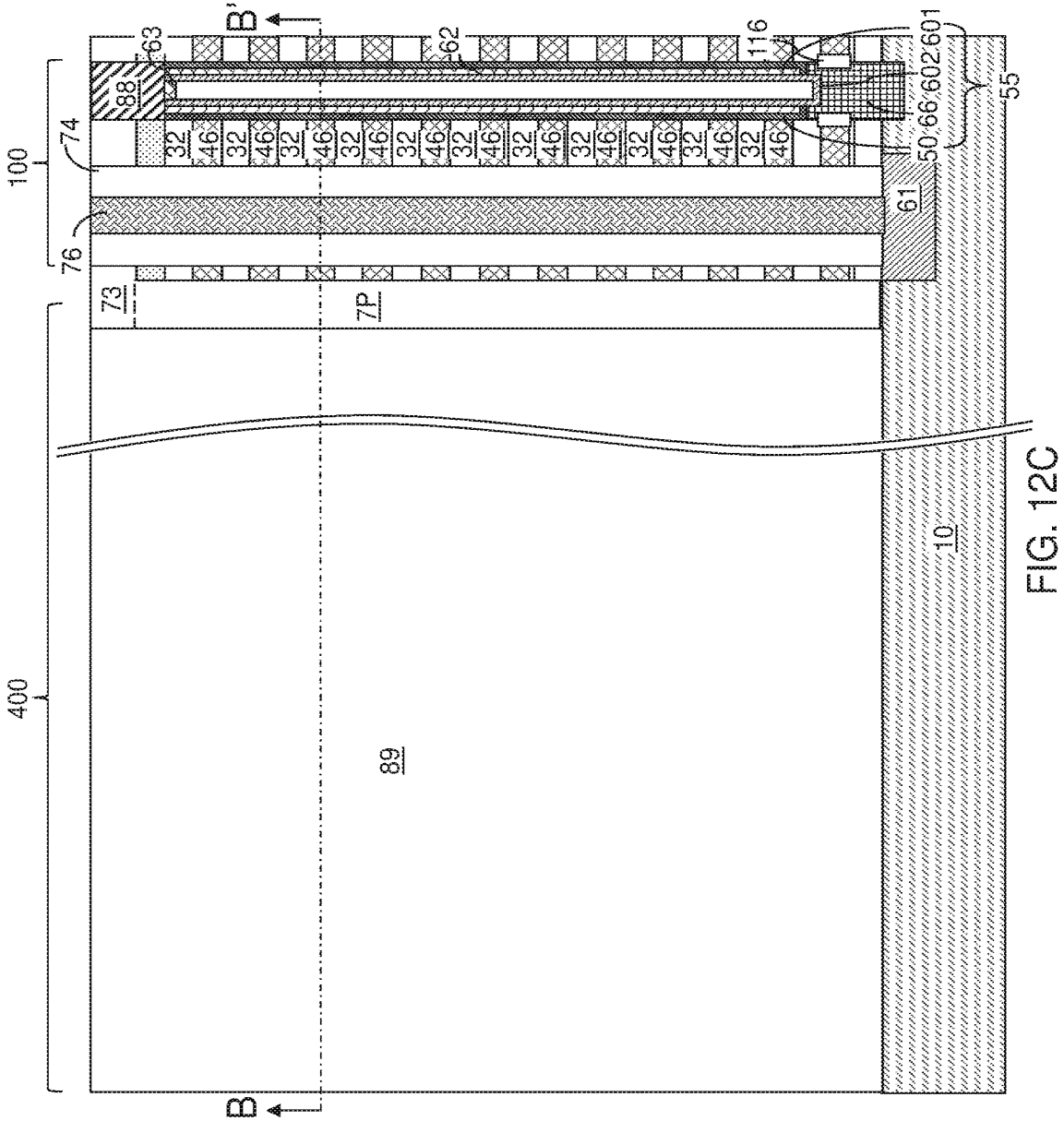


FIG. 12C

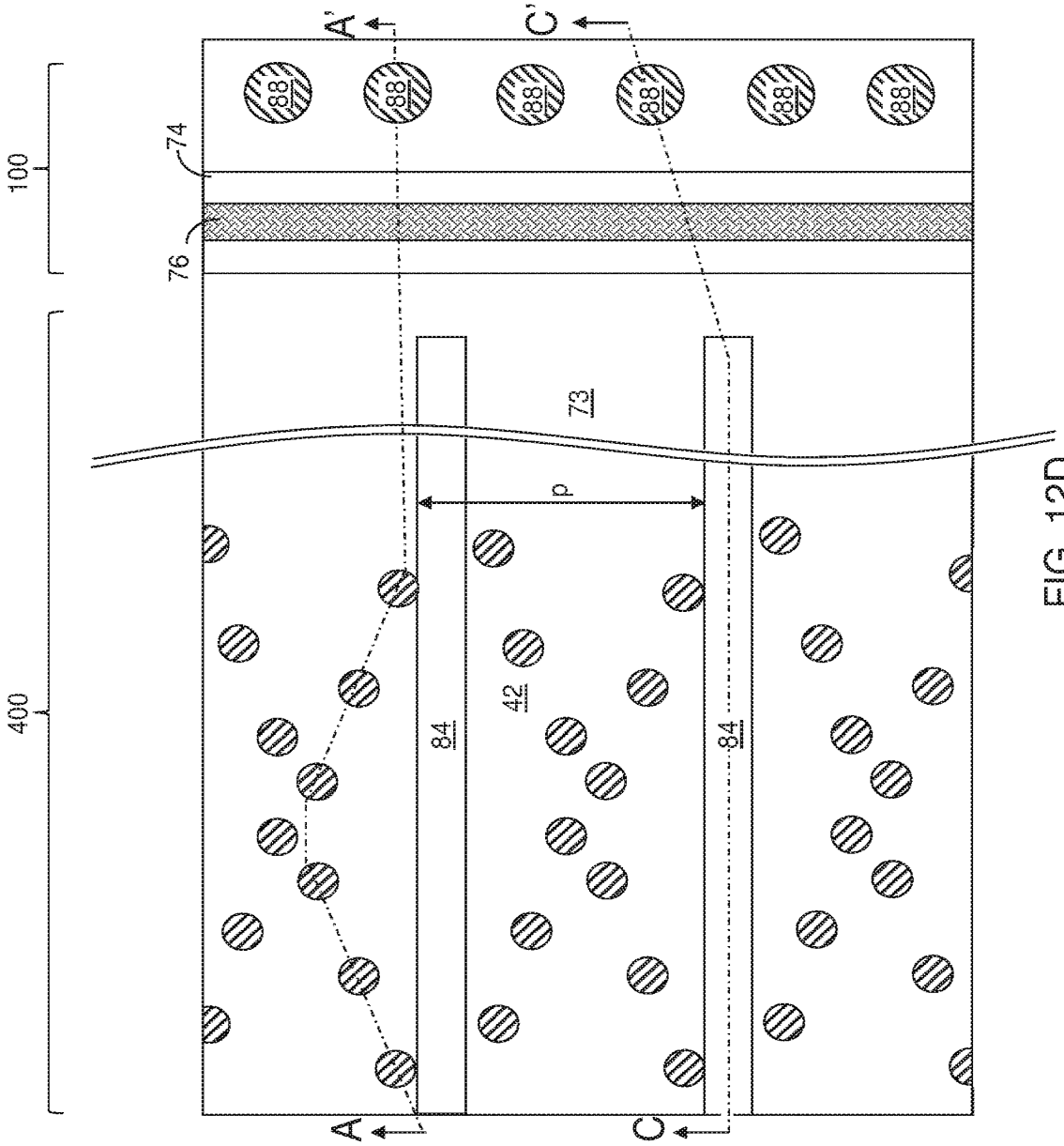


FIG. 12D

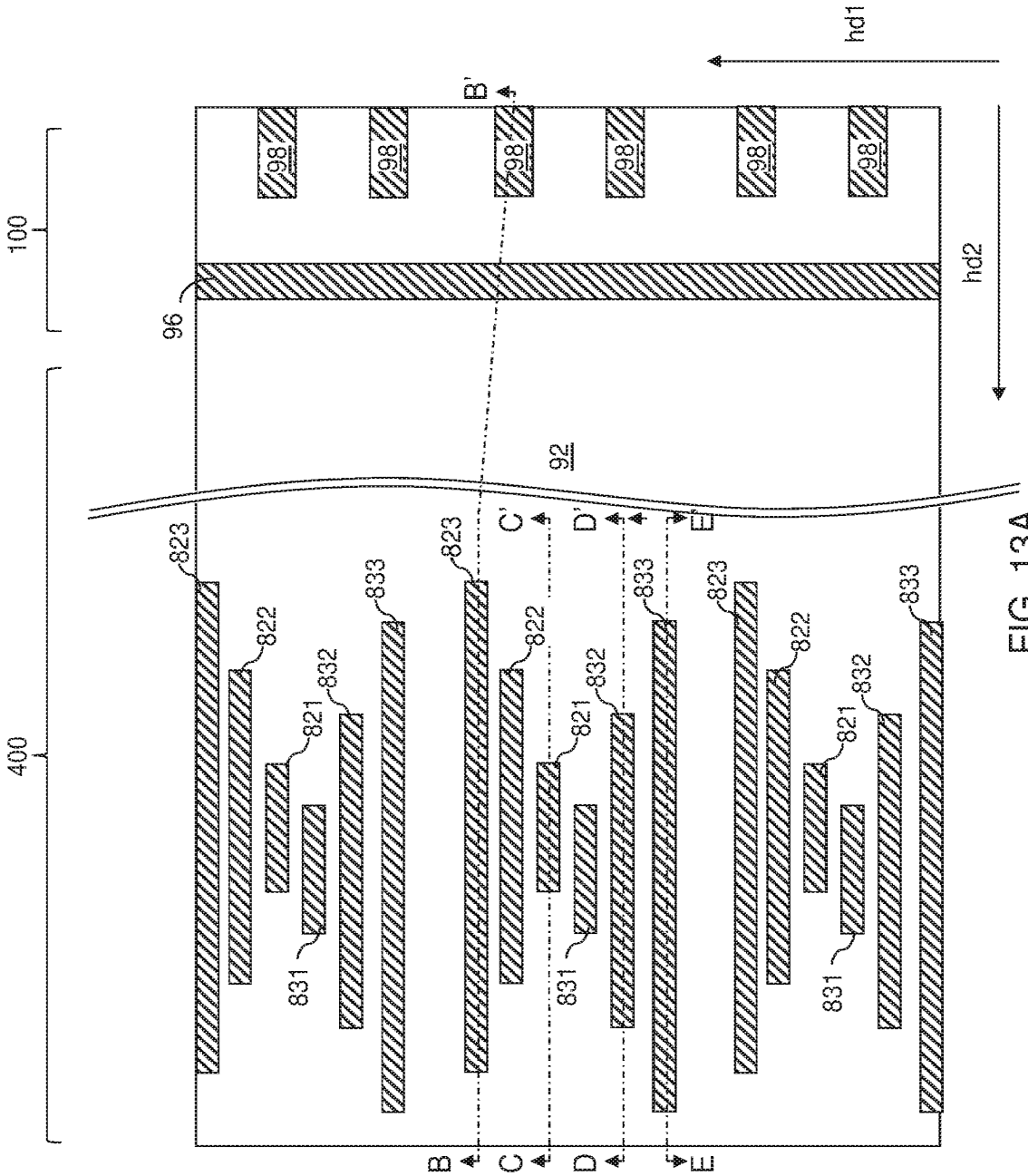


FIG. 13A

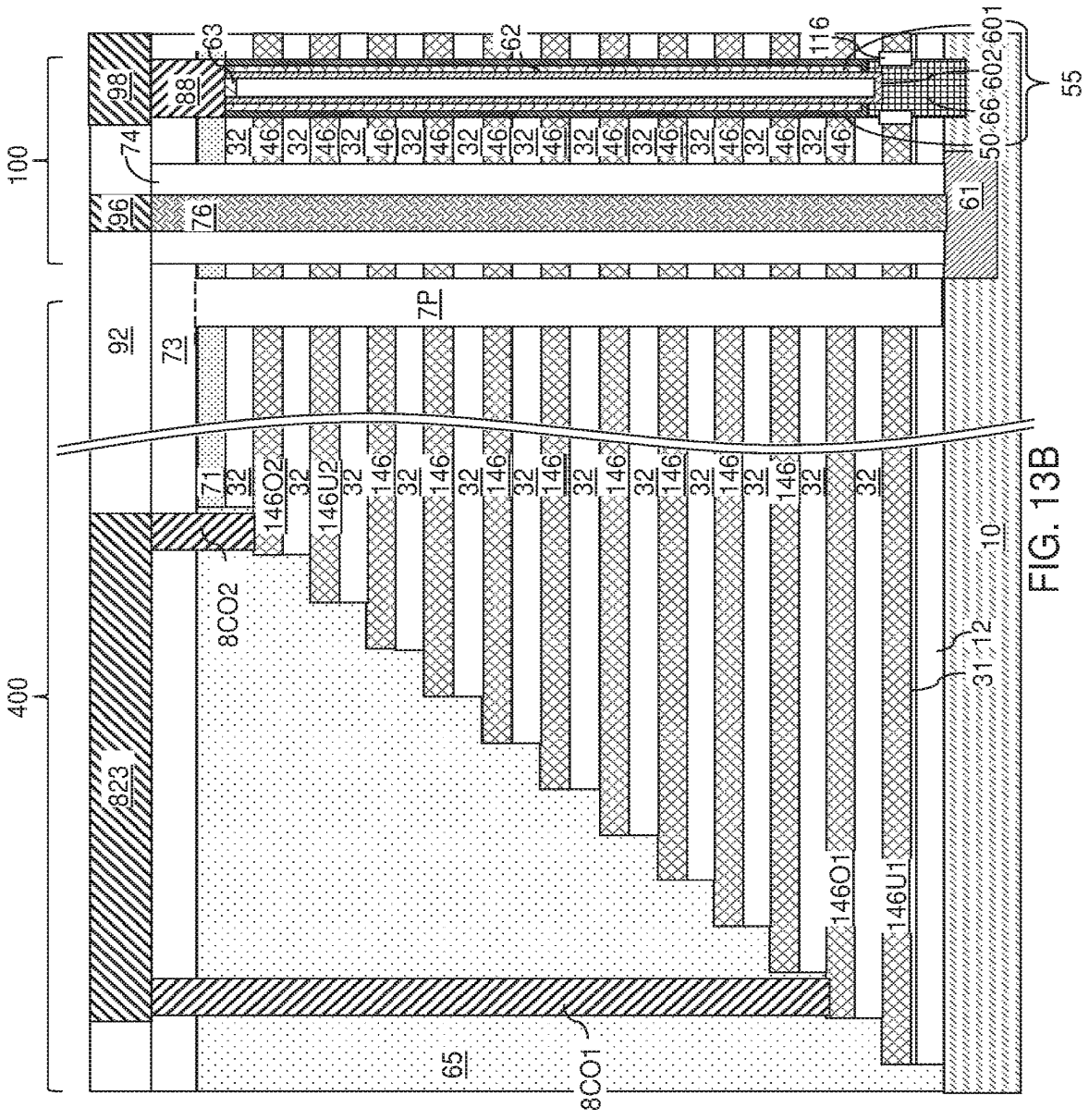

100
400
98
88
74
96
76
92
73
71
823
63
62
116
55
50
66
602
601
61
7P
32
46
146O2
146U2
146
8CO2
8CO1
65
10
31
12
146O1
146U1

FIG. 13B

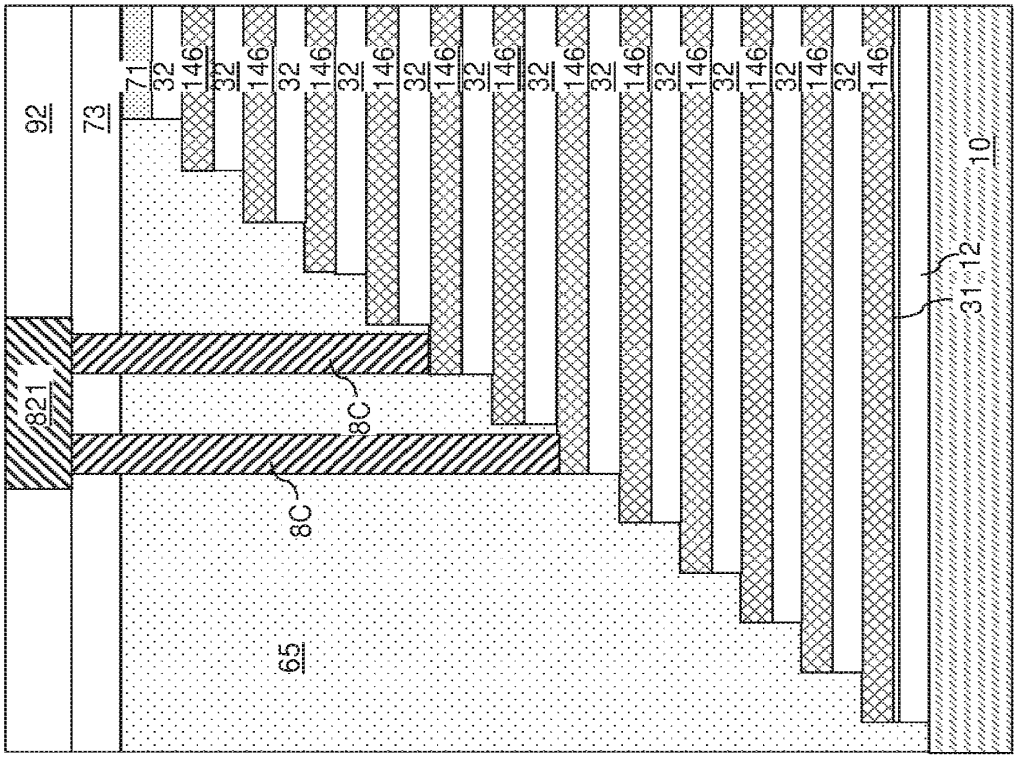


FIG. 13C

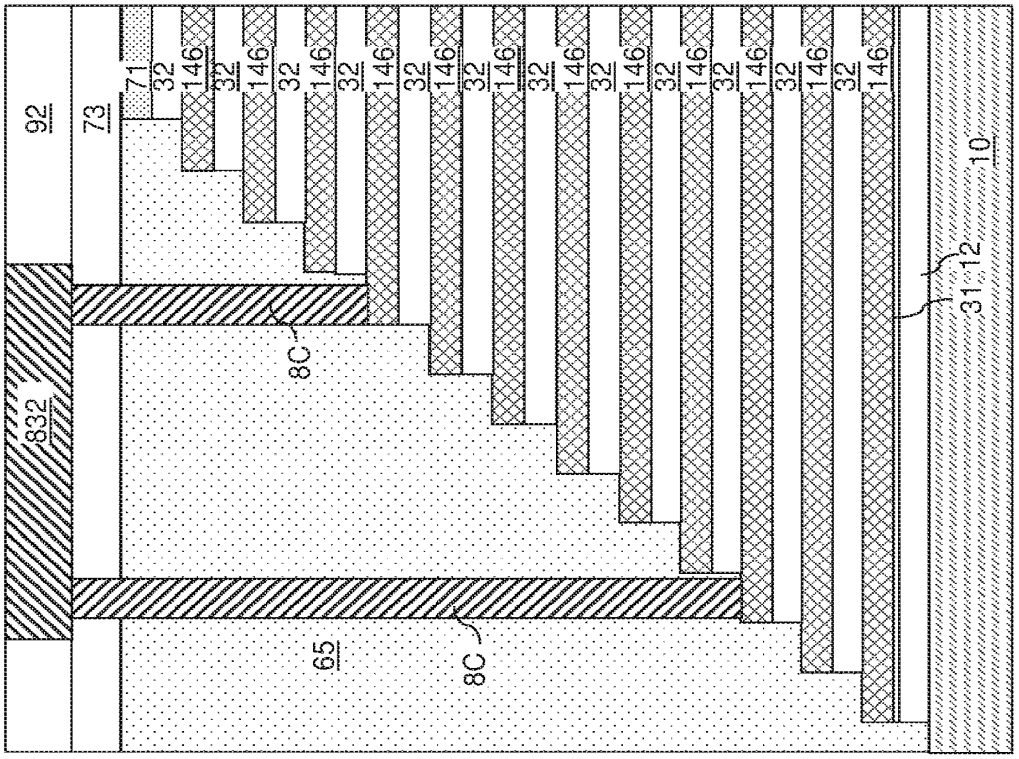


FIG. 13D

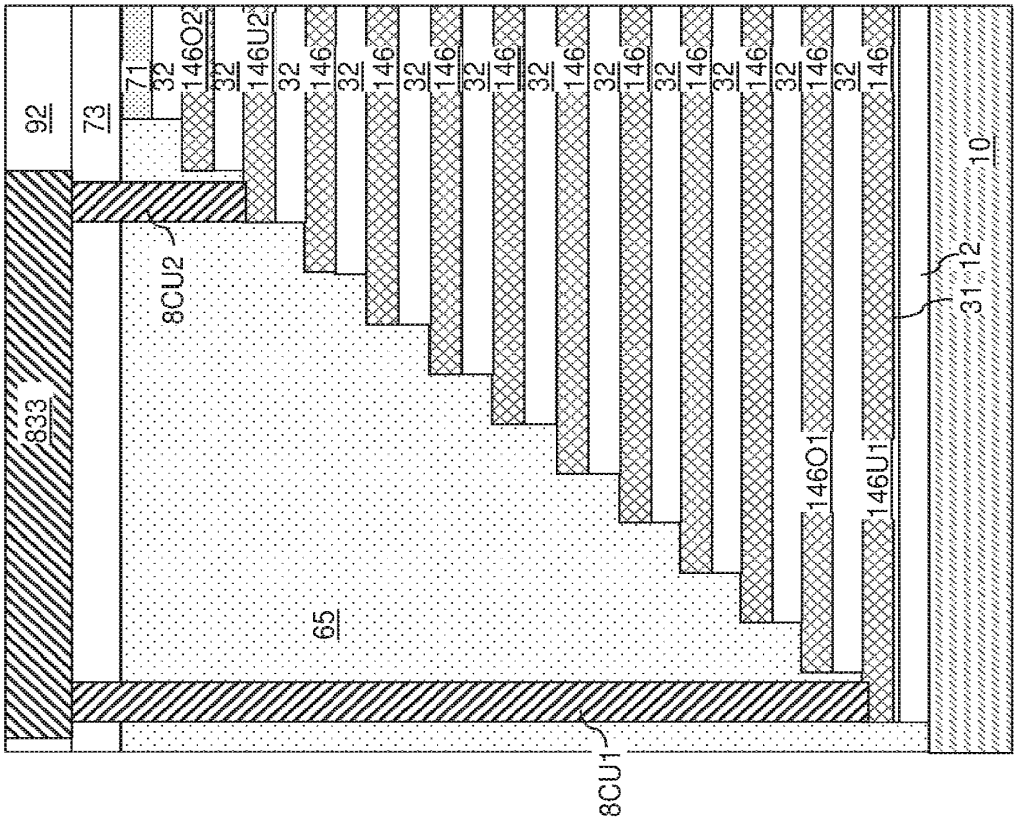

92
73
71
32
146O2
32
146U2
32
146
32
146
32
146
32
146
32
146
32
146
32
146
32
146
32
146
32
146
32
146
32
146
32
146
32
146
833
8CU2
65
146O1
146U1
31
12
10
8CU1

FIG. 13E

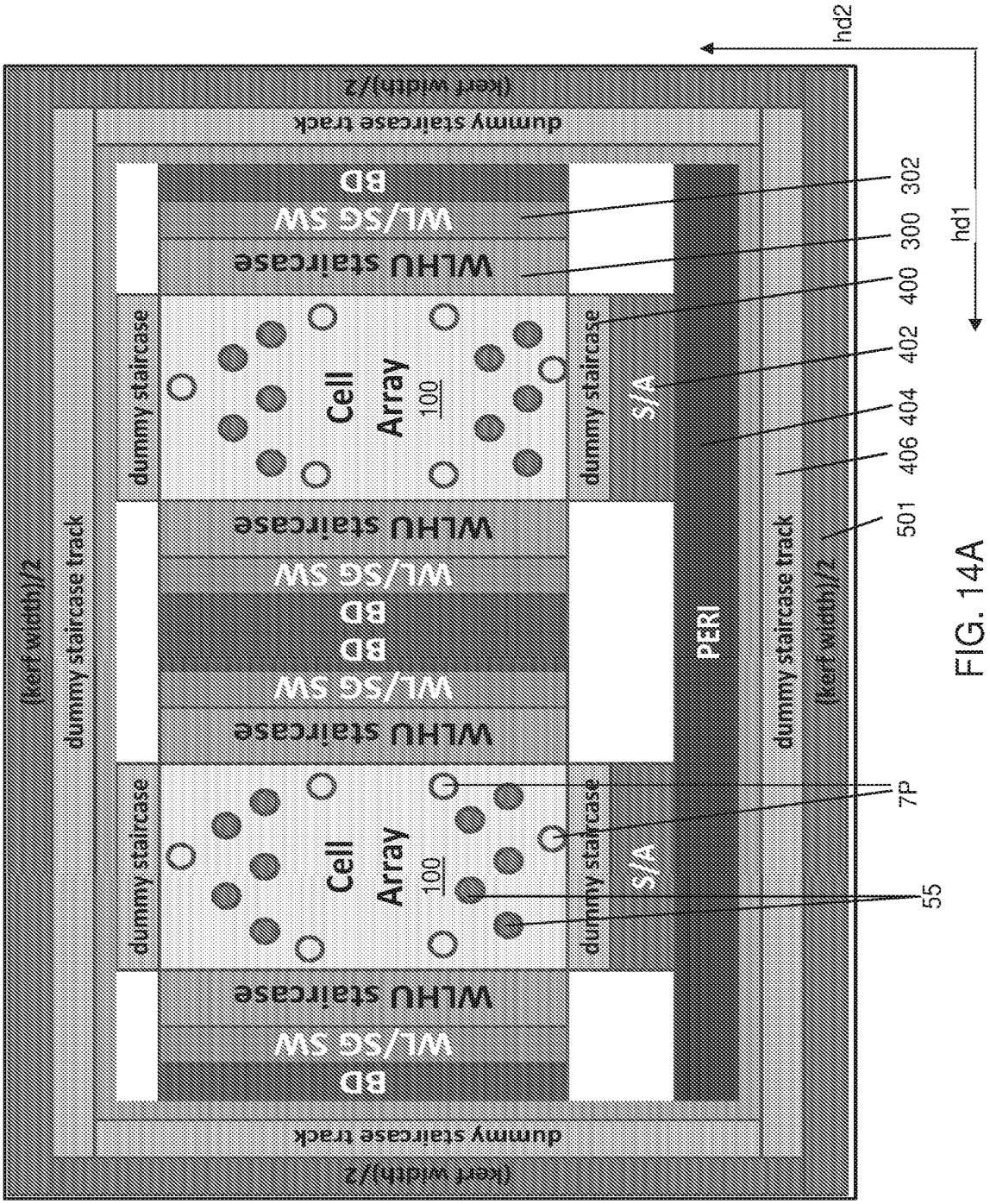

hd2
hd1
302
300
400
402
404
406
501
7P
55
(kerf width)/2
dummy staircase track
dummy staircase track
dummy staircase
dummy staircase
dummy staircase
dummy staircase
Cell Array 100
Cell Array 100
S/A
S/A
PERI
WLHU staircase
WL/SG SW
BD
WLHU staircase
WL/SG SW
BD
BD
WL/SG SW
WLHU staircase
WLHU staircase
WL/SG SW
BD

FIG. 14A

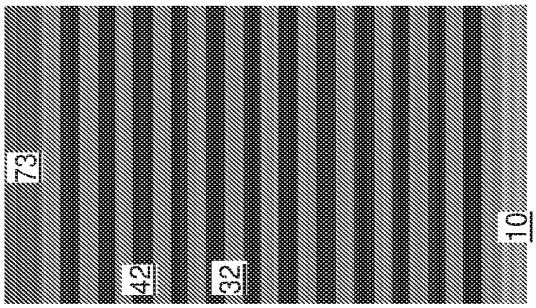


FIG. 14D

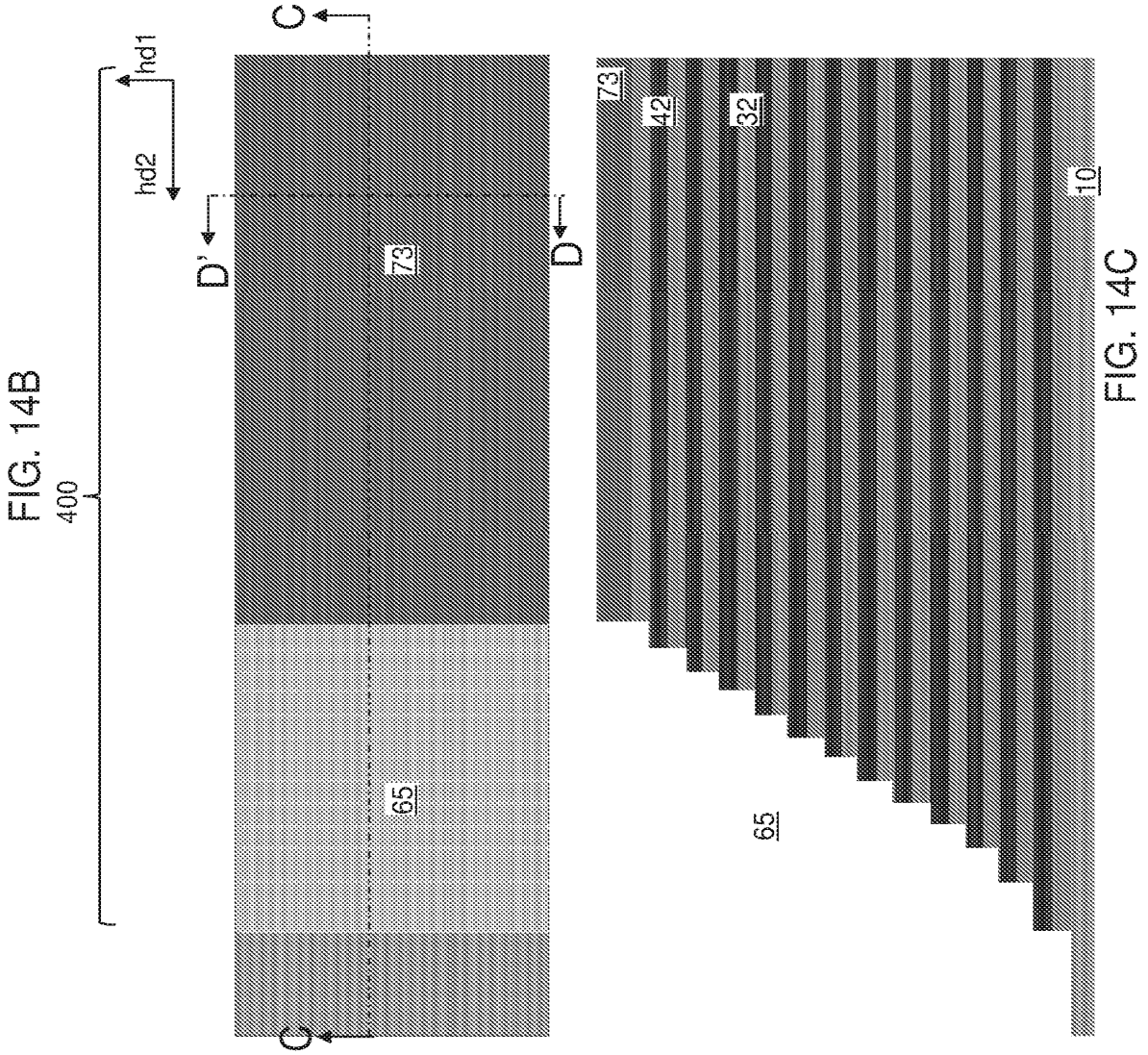


FIG. 14B

FIG. 14C

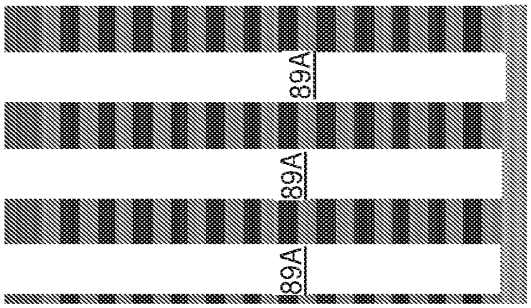


FIG. 14G

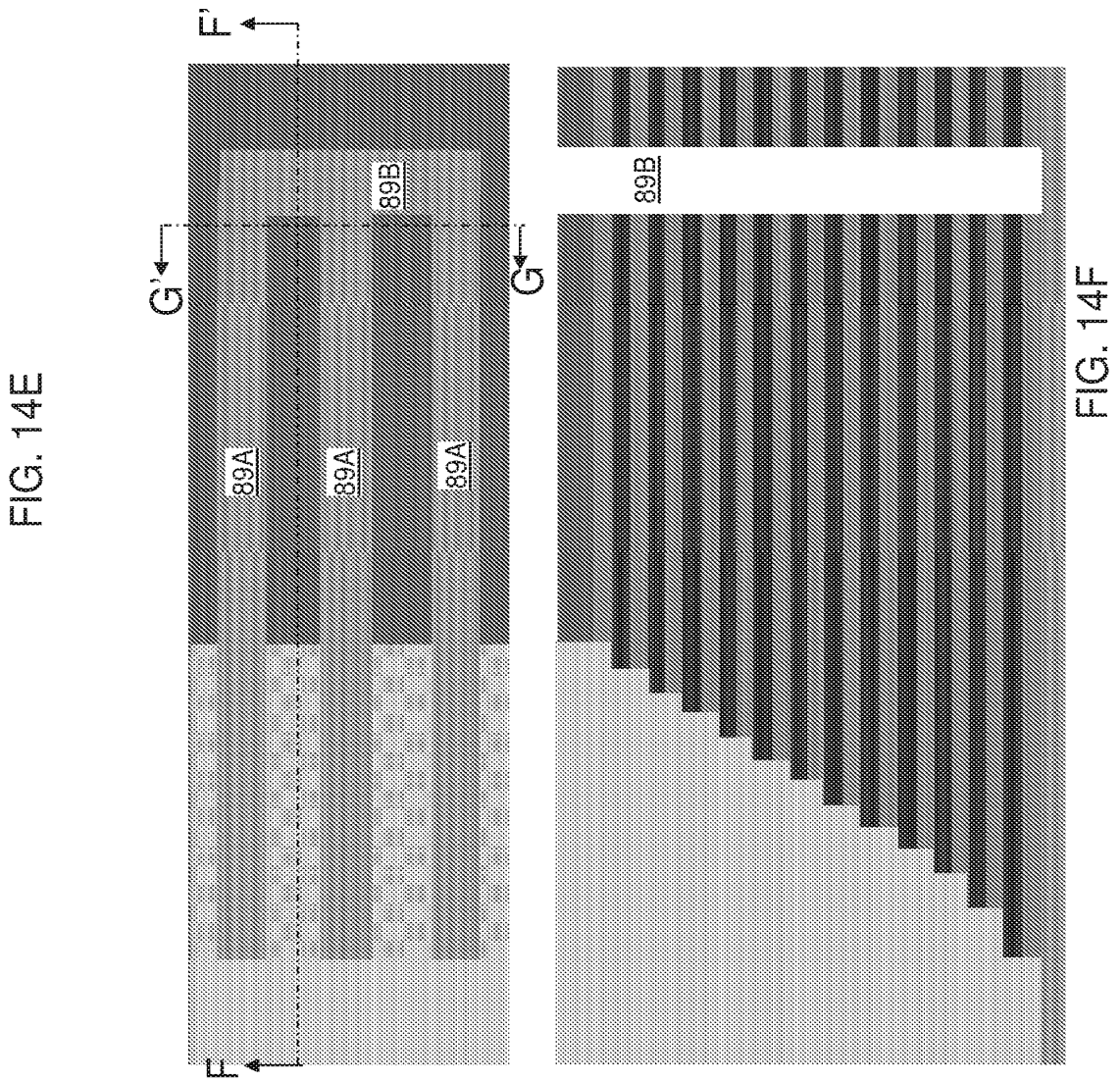


FIG. 14E

FIG. 14F

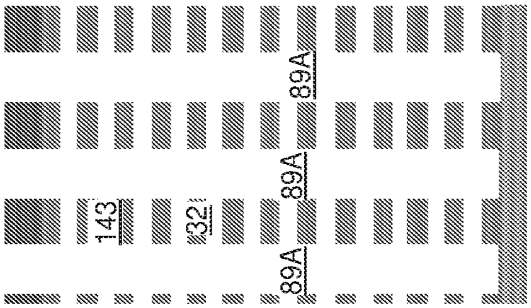


FIG. 14J

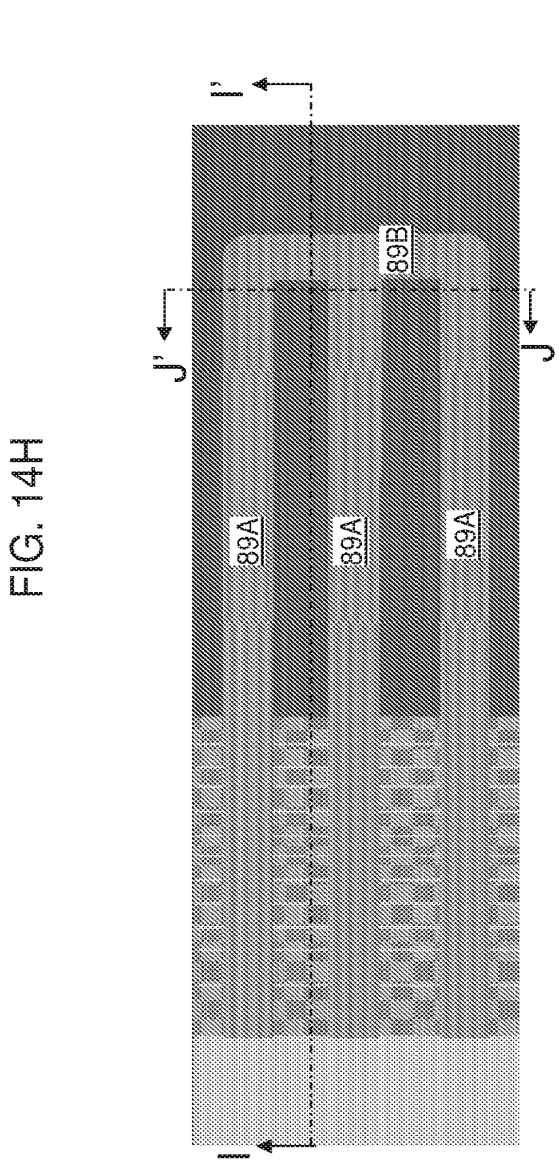


FIG. 14H

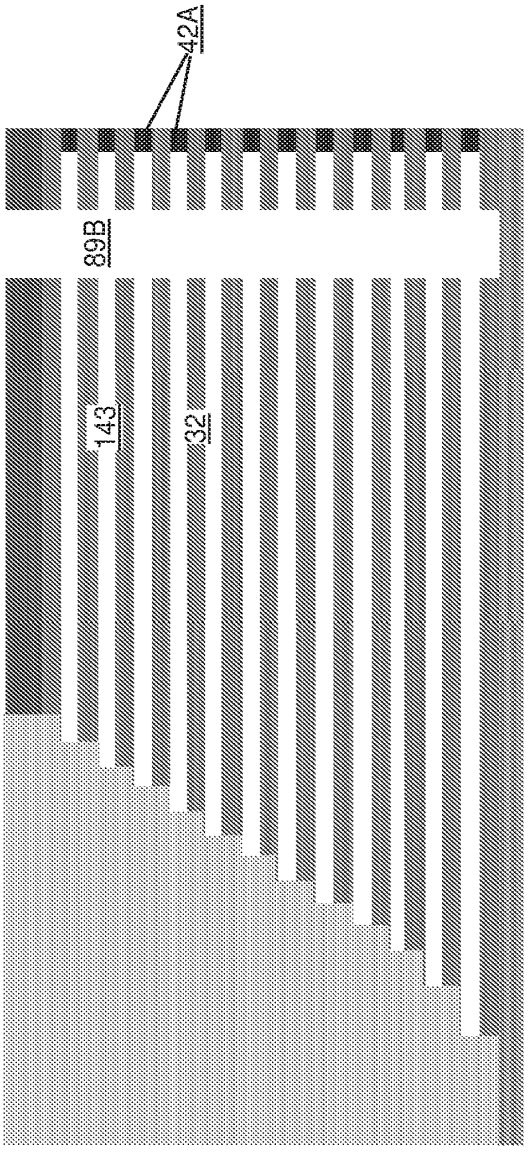


FIG. 14I

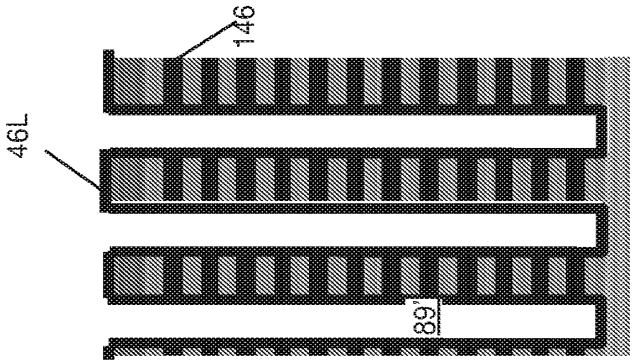


FIG. 14M

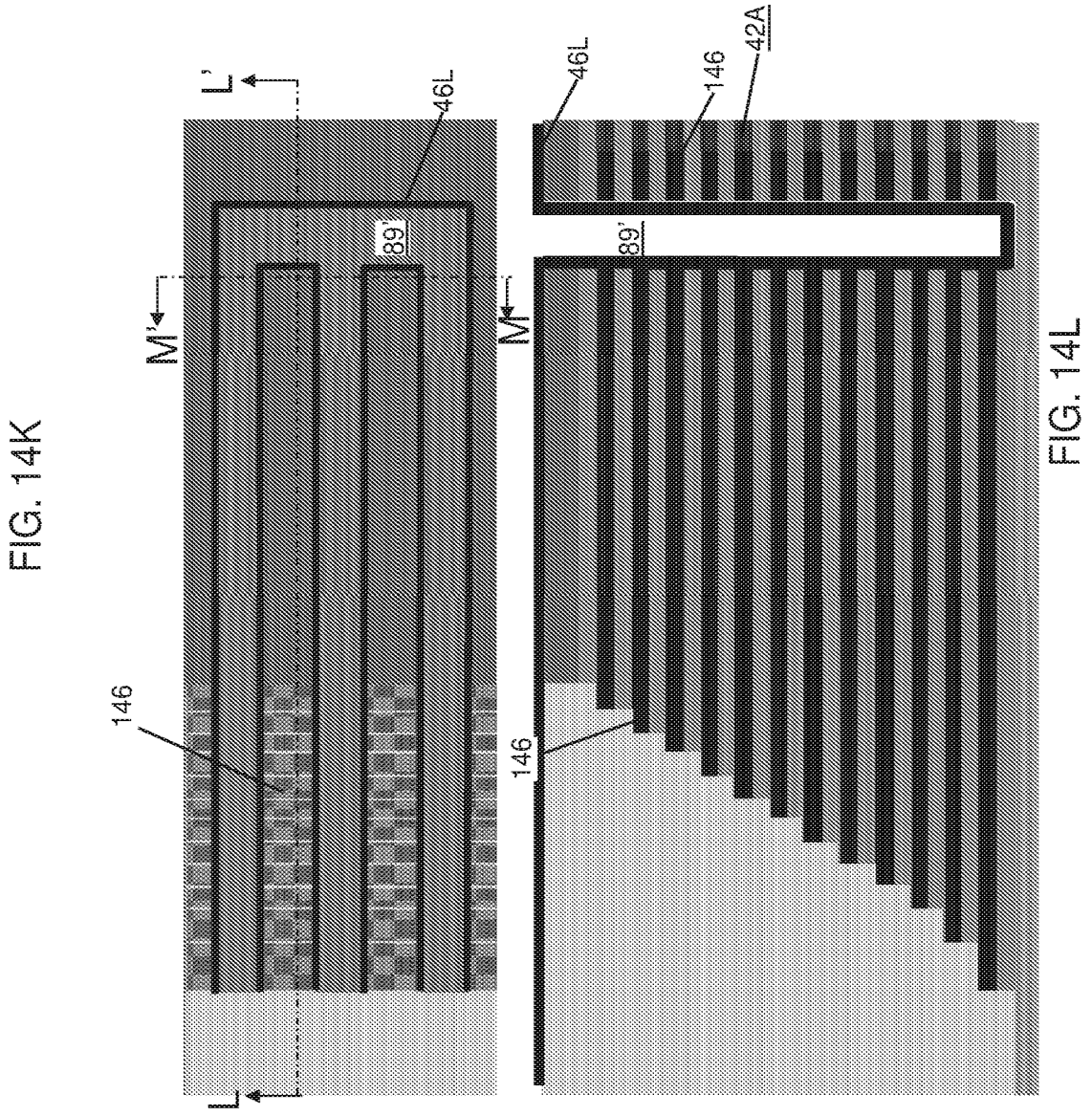


FIG. 14K

FIG. 14L

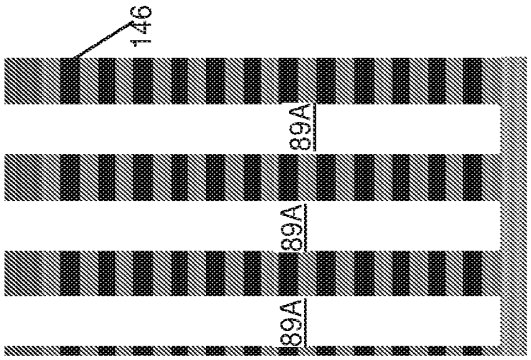


FIG. 14P

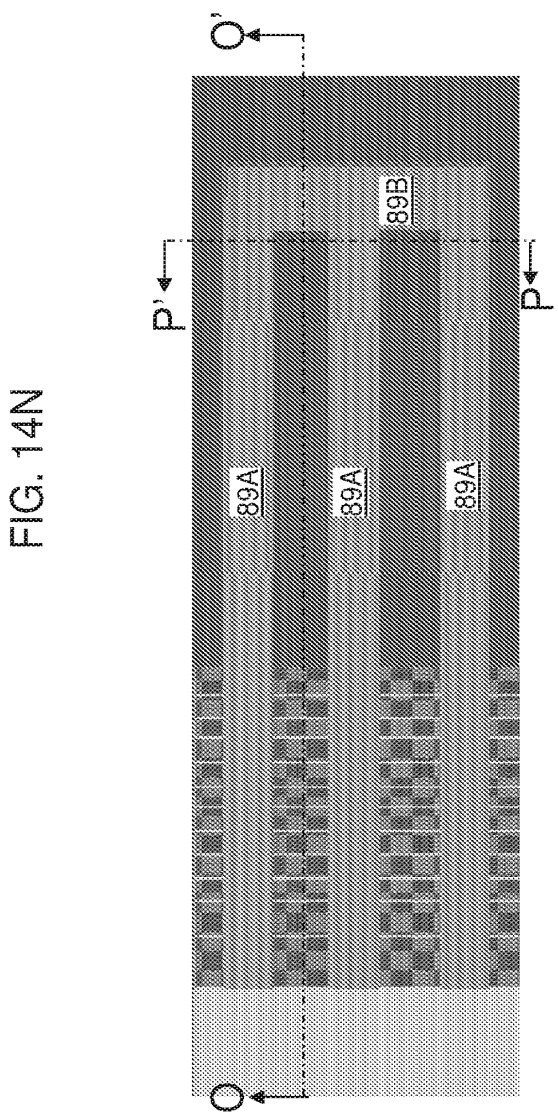


FIG. 14N

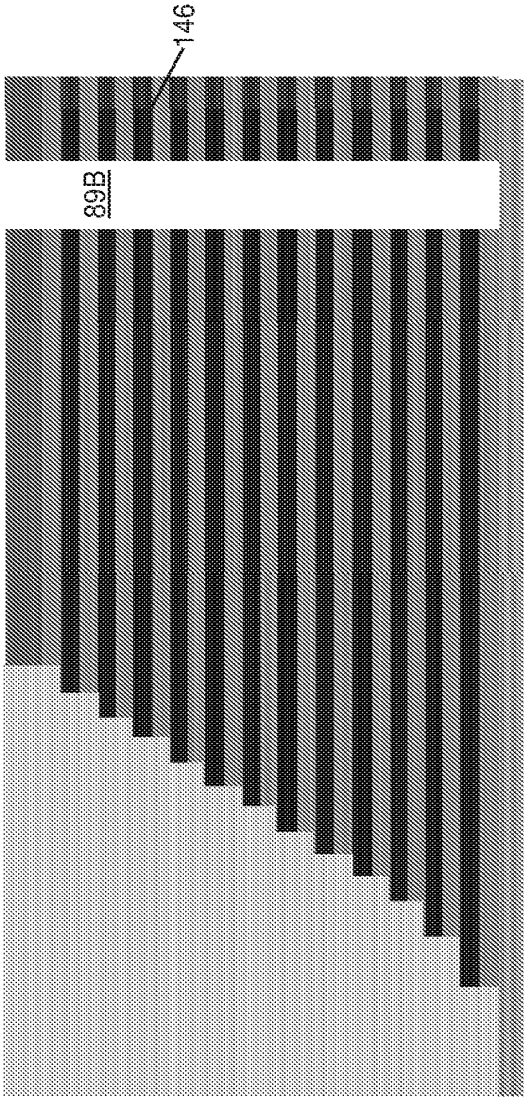


FIG. 14O

Micron Ex. 1002, p. 317
Micron v. YMTC
IPR2024-00790

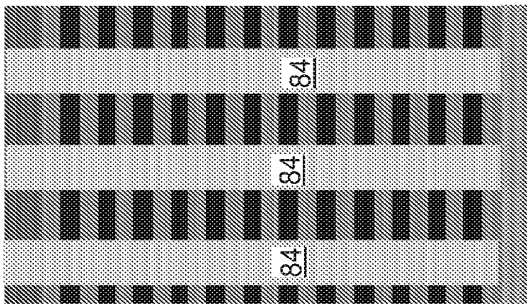


FIG. 14S

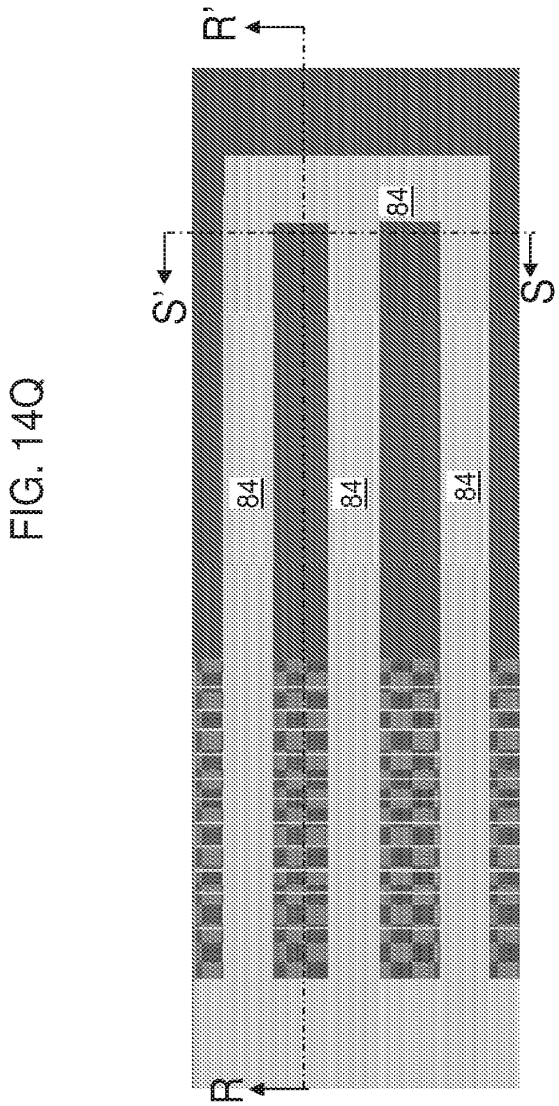


FIG. 14Q

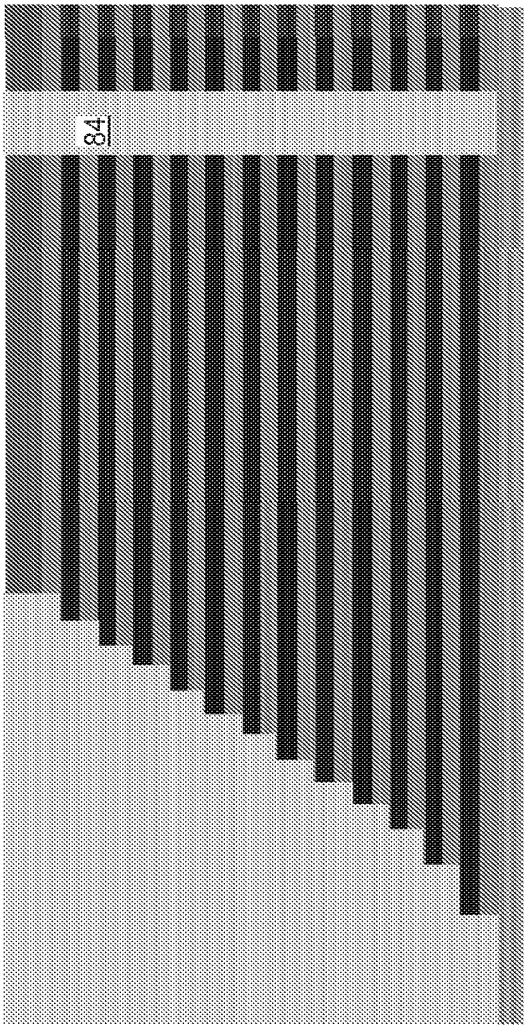


FIG. 14R

Micron Ex. 1002, p. 318
Micron v. YMTC
IPR2024-00790

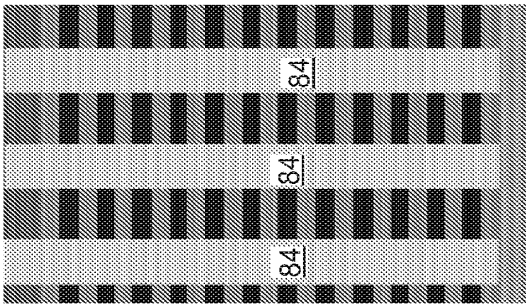


FIG. 14V

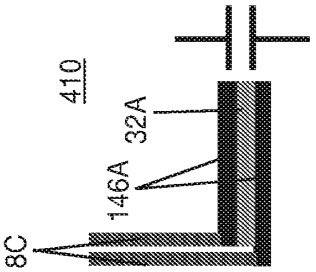


FIG. 14W

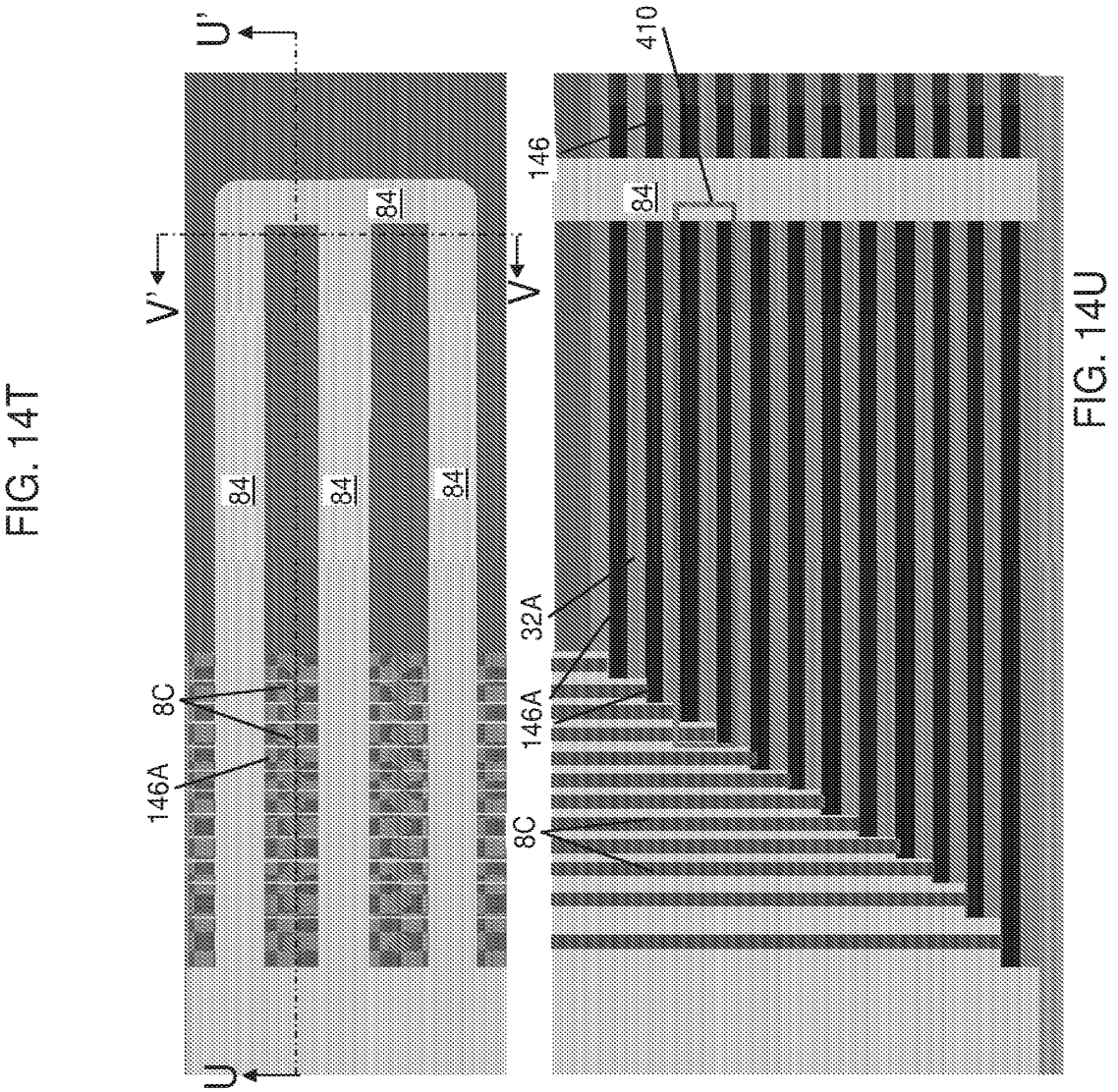


FIG. 14T

FIG. 14U

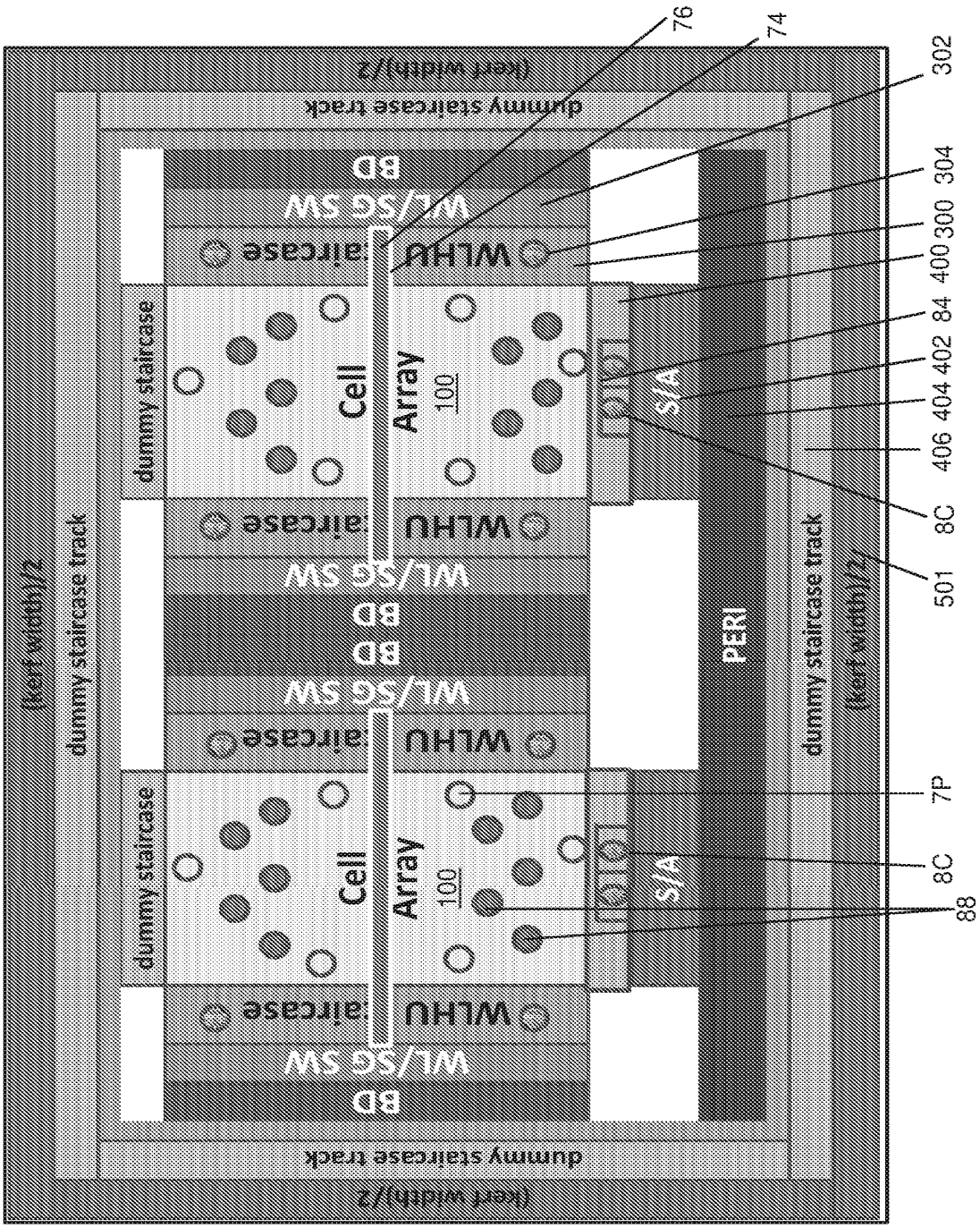

(kerf width)/2
dummy staircase track
dummy staircase
Cell Array 100
staircase
WLHU
WL/SG SW
BD
S/A
PERI
76
74
302
304
300
400
84
402
404
406
8C
501
7P
88

FIG. 14X

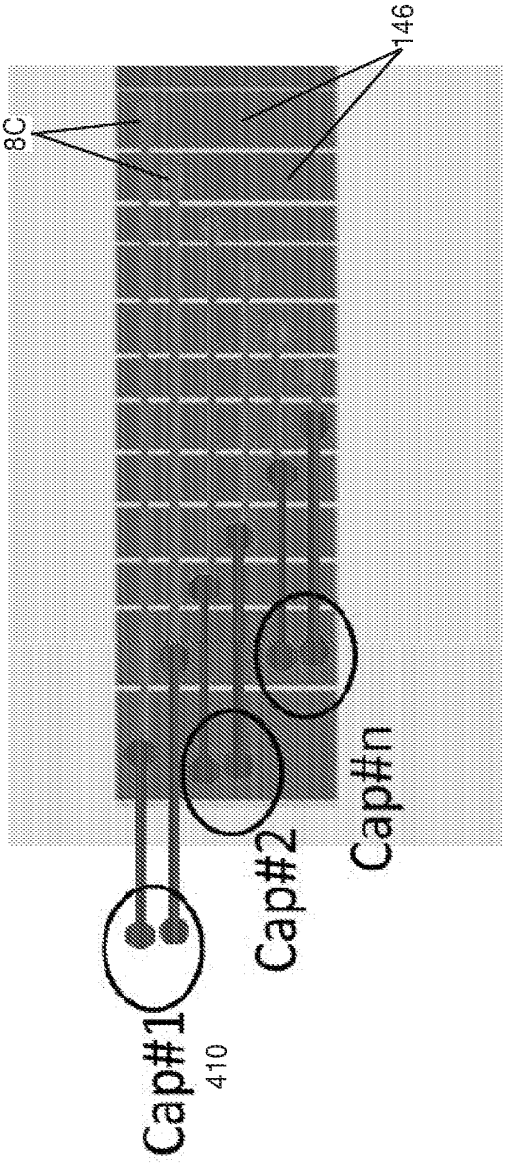


FIG. 14Y

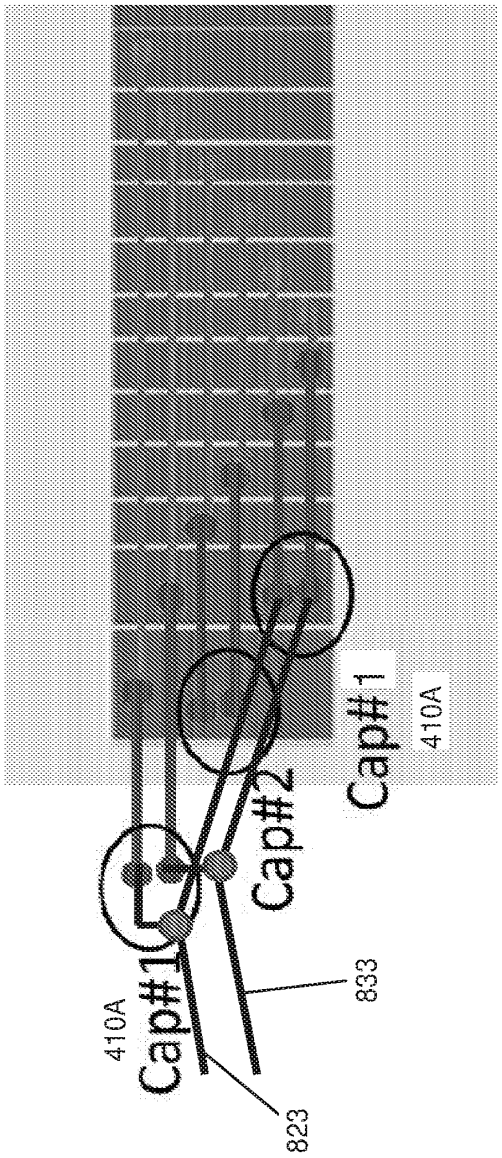


FIG. 14Z

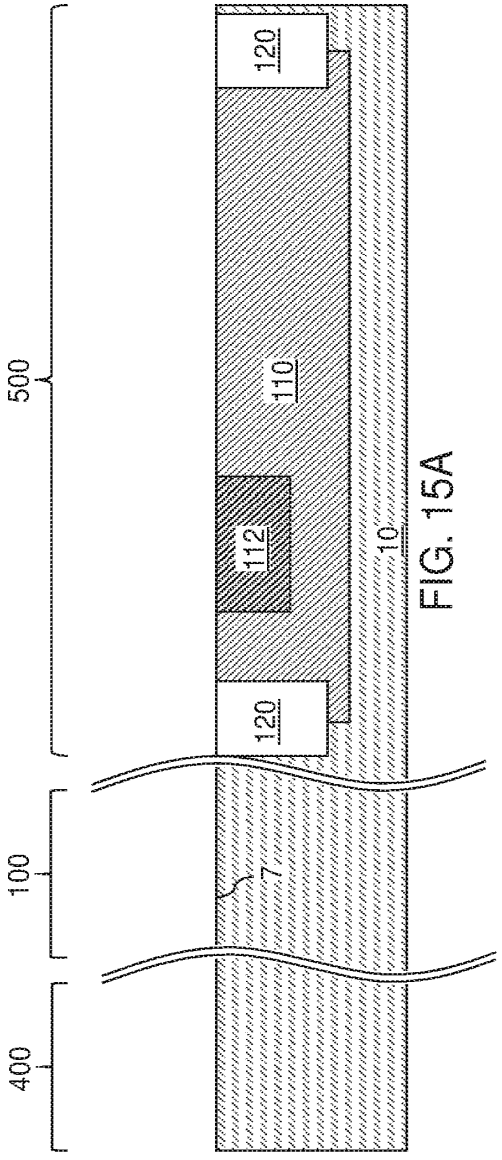


FIG. 15A

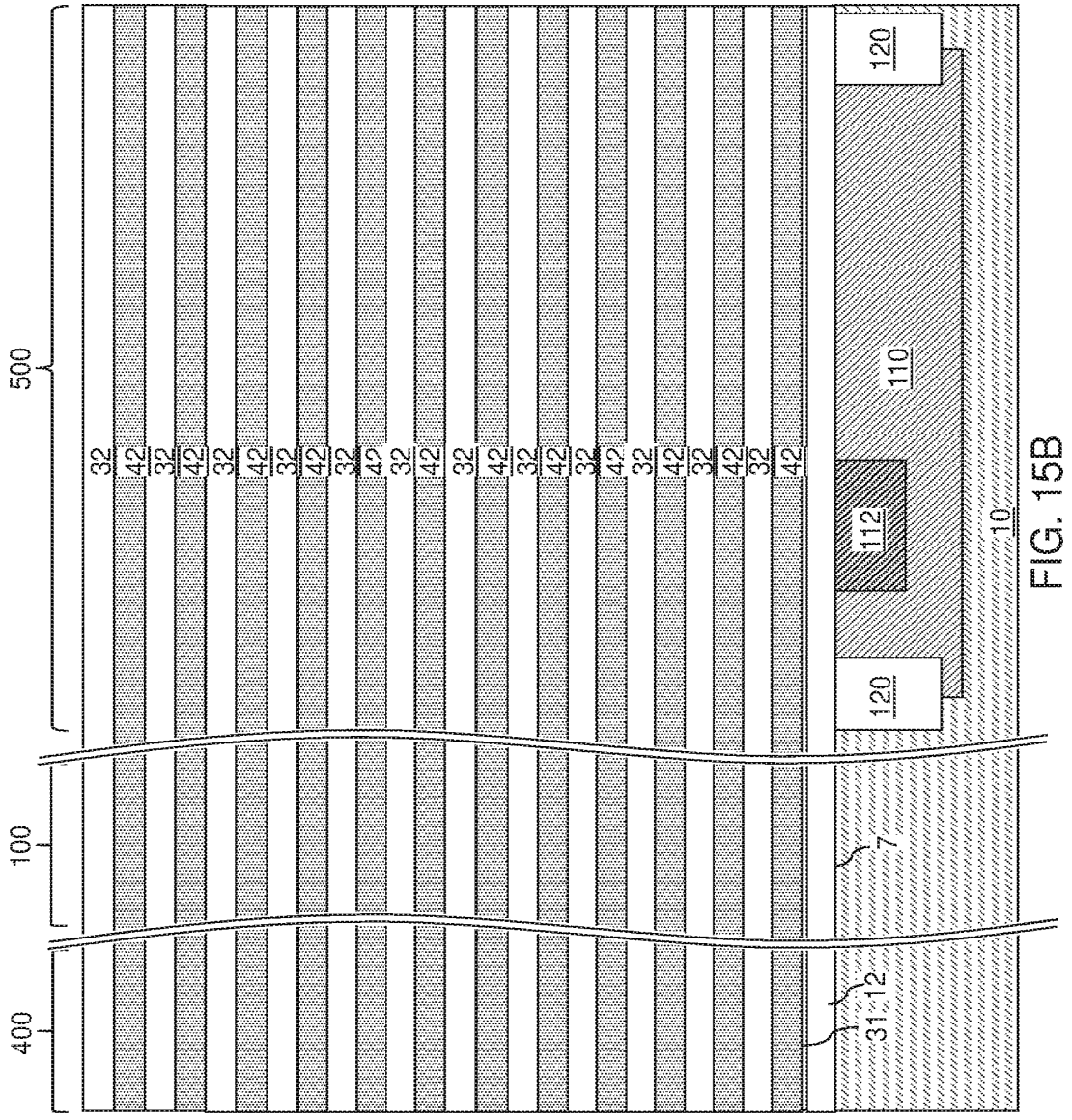


FIG. 15B

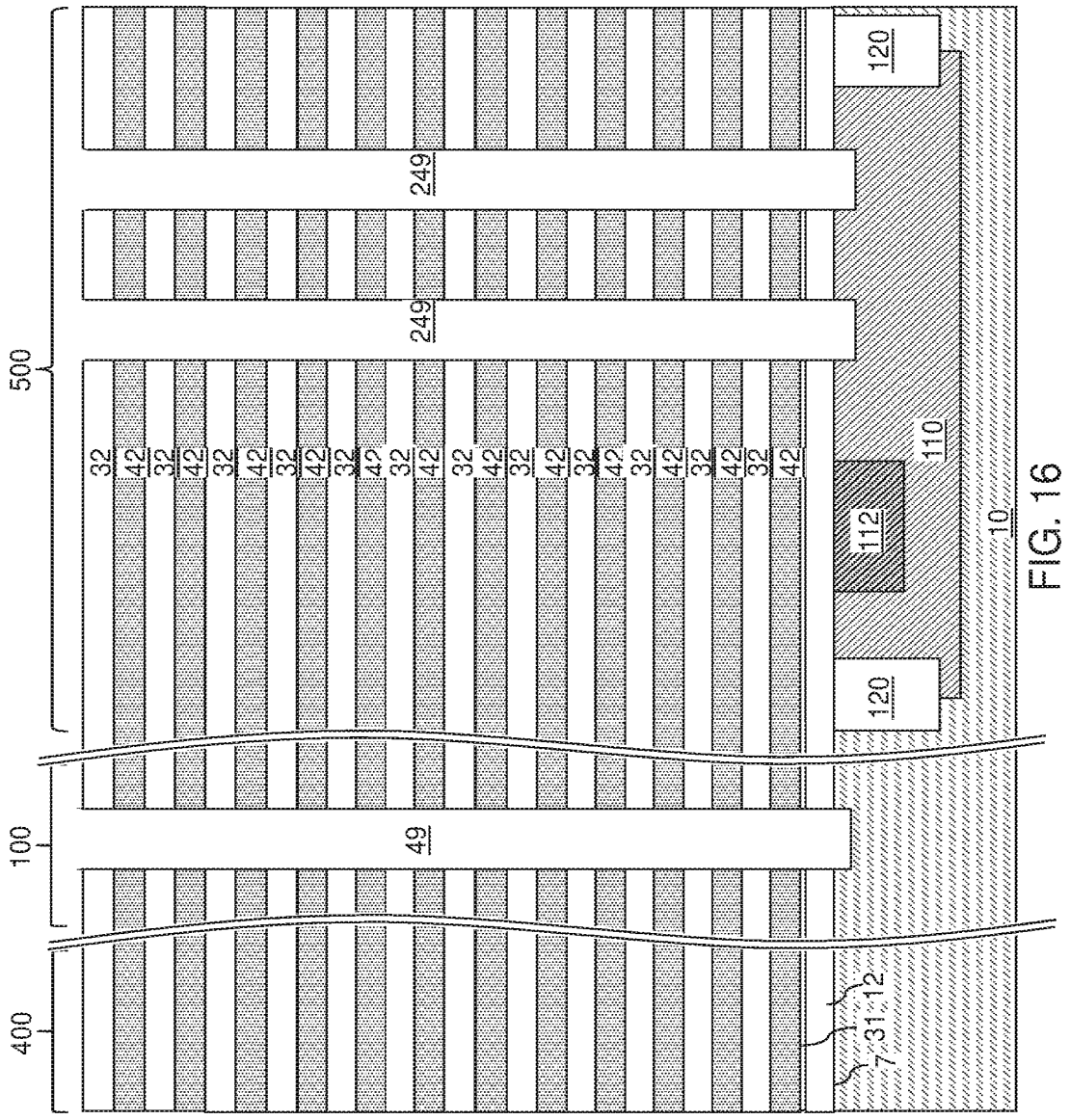


FIG. 16

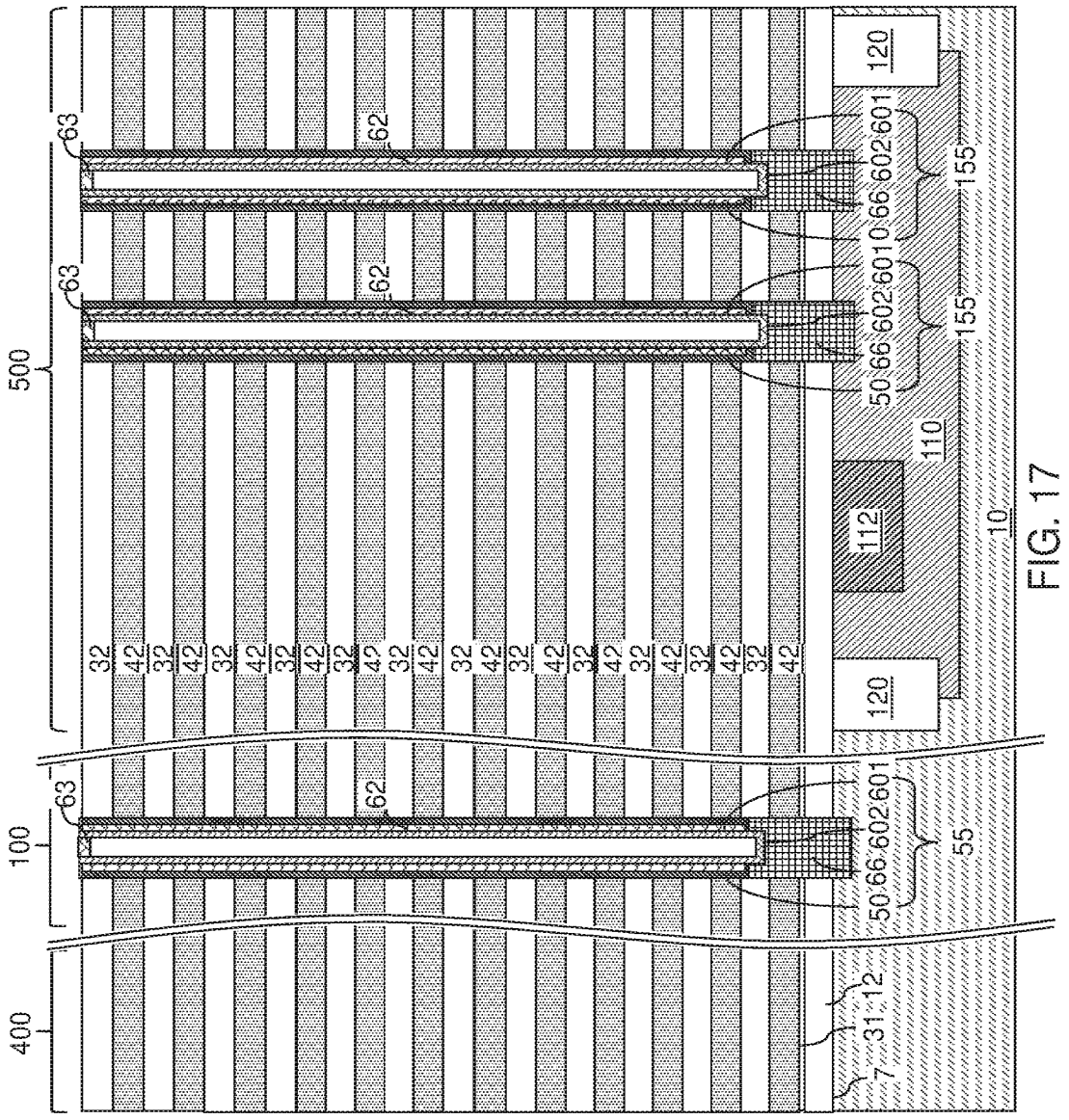


FIG. 17

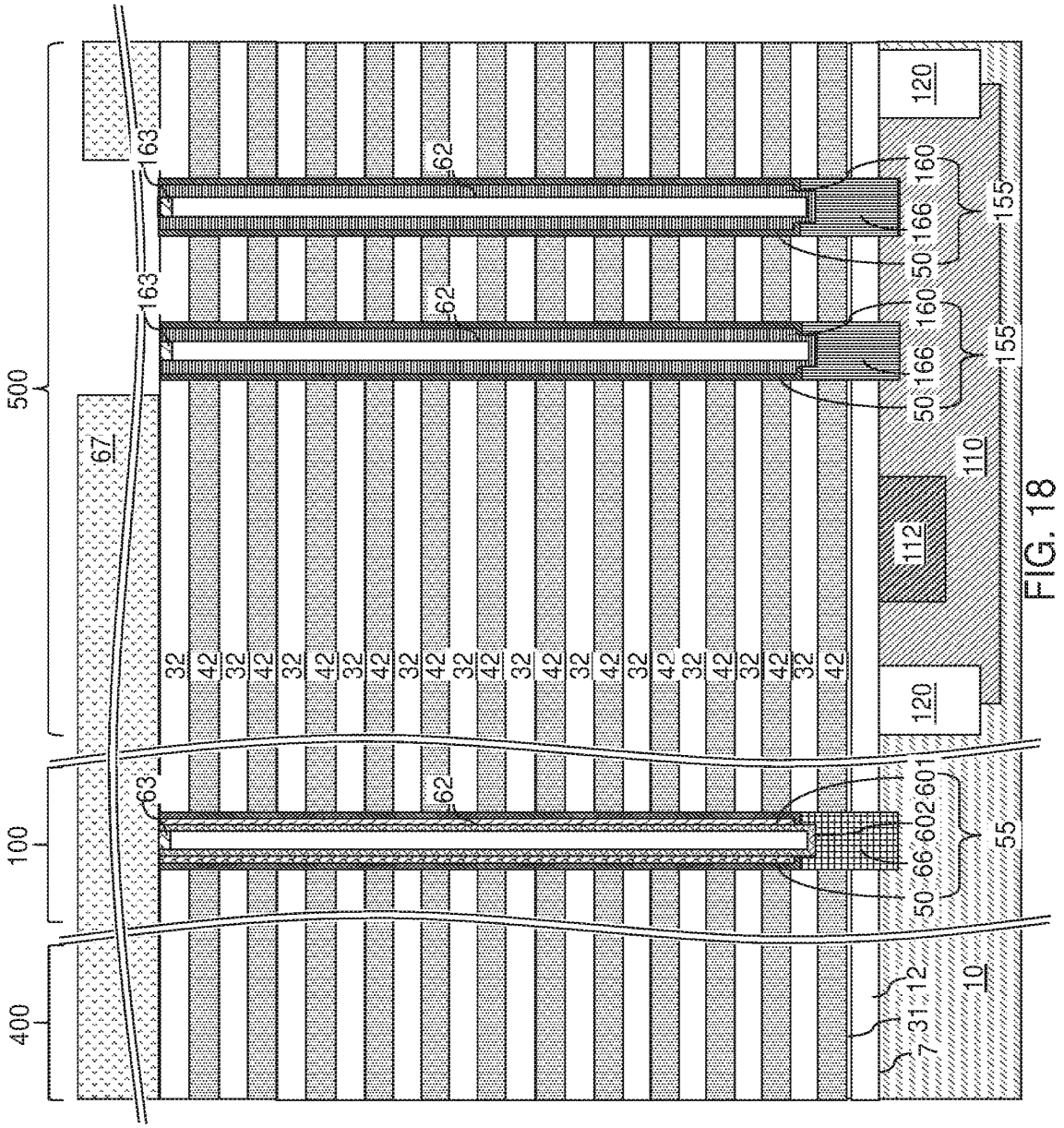

500
100
400
67
63
62
32
42
120
160
166
50
155
110
112
601
602
66
55
12
31
7
10

FIG. 18

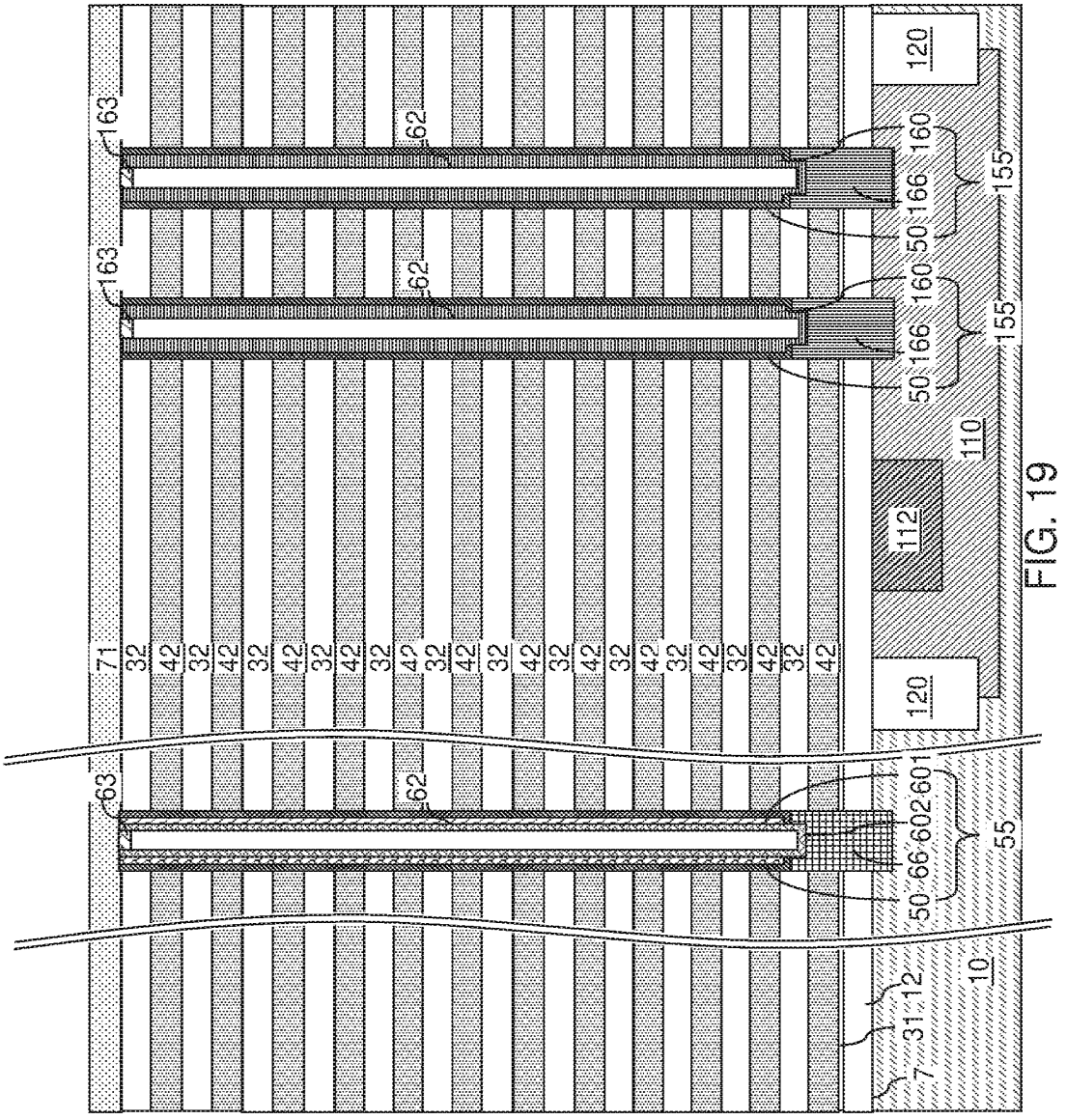


FIG. 19

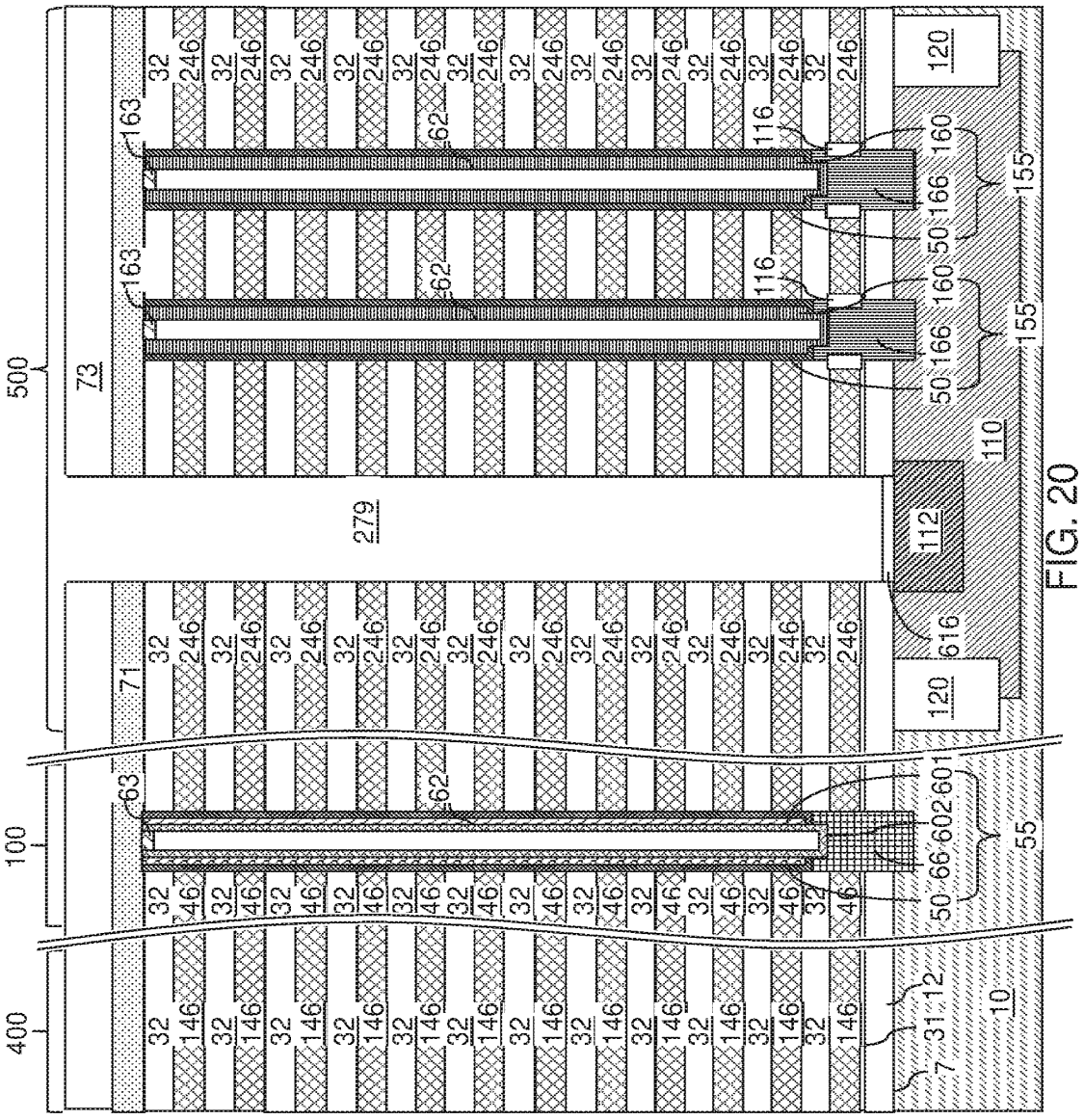

500
100
400
73
71
279
163
62
116
160
166
50
155
110
112
120
616
63
601
602
66
55
12
31
7
10
32
246
146

FIG. 20

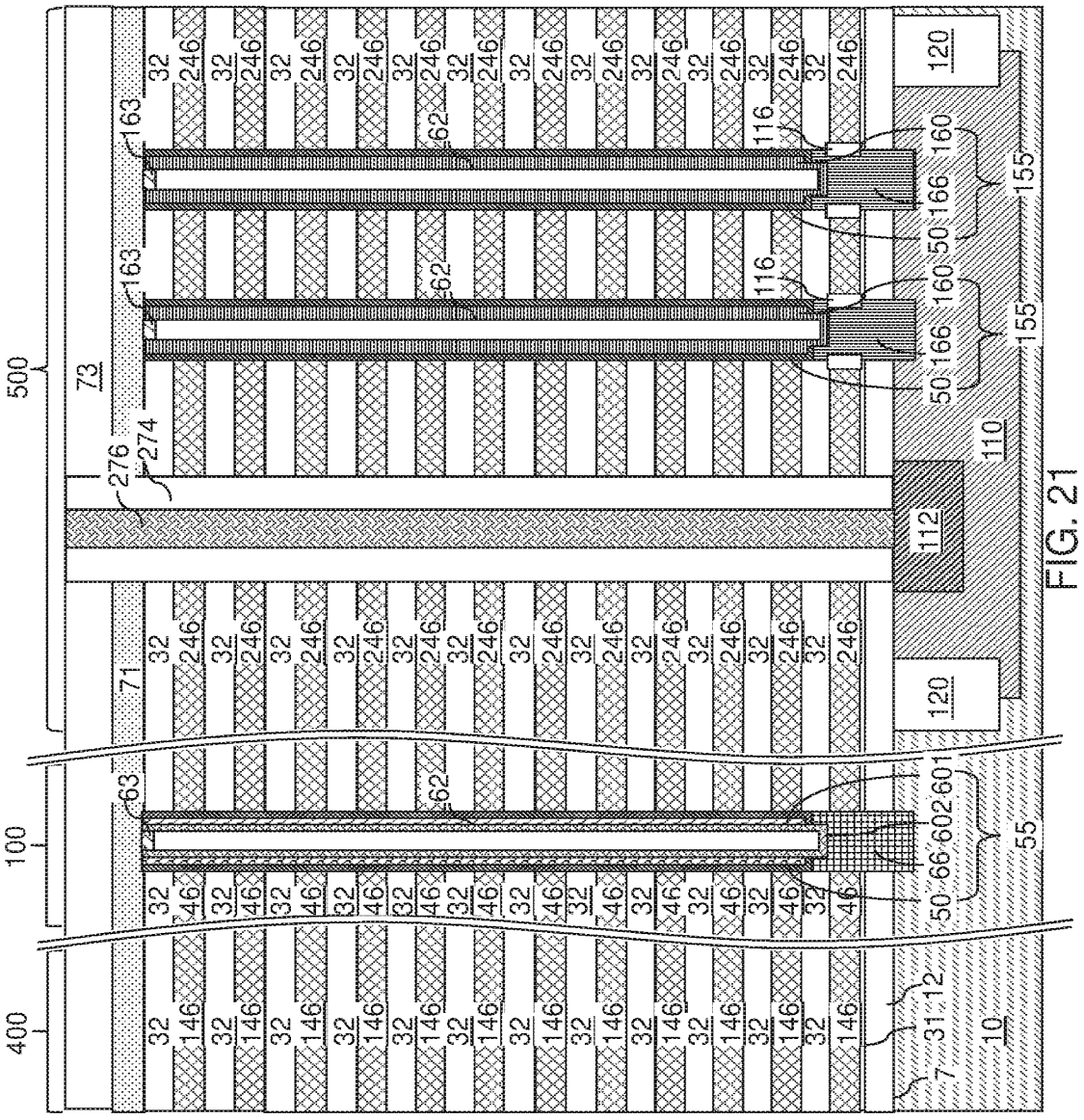

500
100
400
73
71
63
163
62
116
120
160
166
50
155
110
112
276
274
32
246
146
601
602
66
55
12
31
7
10

FIG. 21

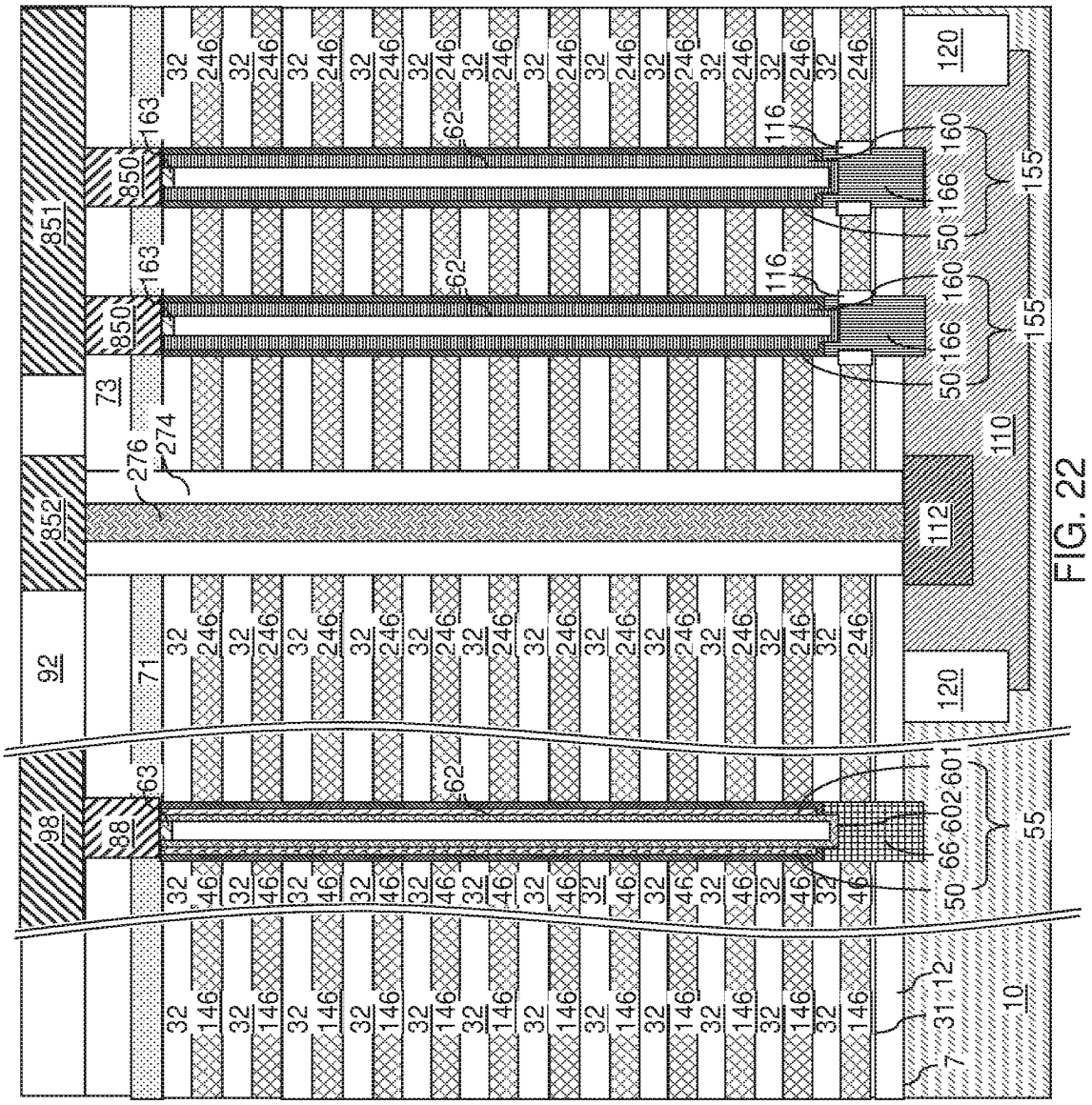

851
850
163
32
246
62
116
160
166
50
155
120
73
274
276
852
112
110
92
71
63
88
98
601
602
66
55
146
12
31
7
10

FIG. 22

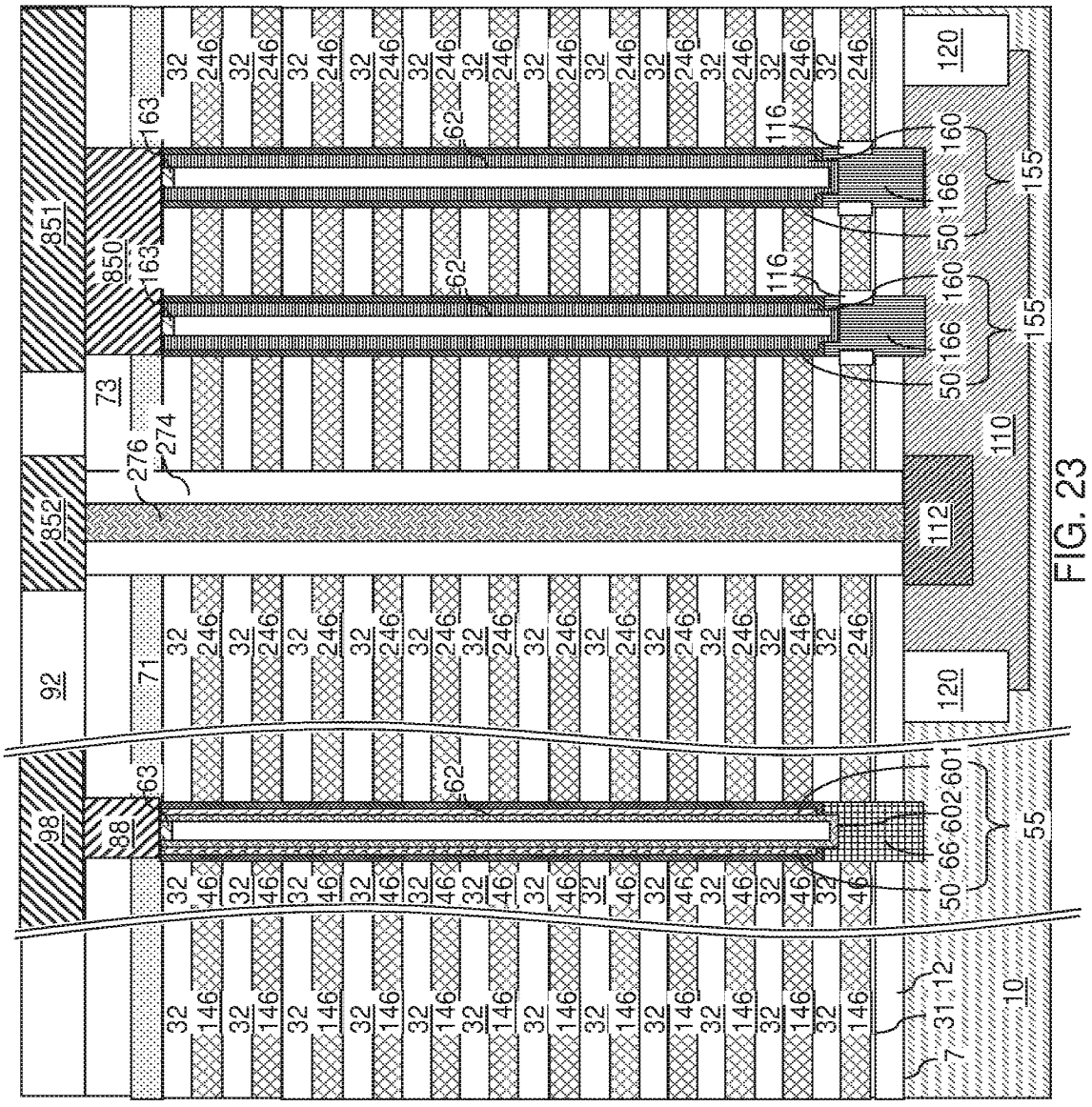

851
850
852
92
98
88
73
71
63
163
274
276
62
116
120
160
166
155
110
112
601
602
66
55
12
31
7
10
32
246
146

FIG. 23

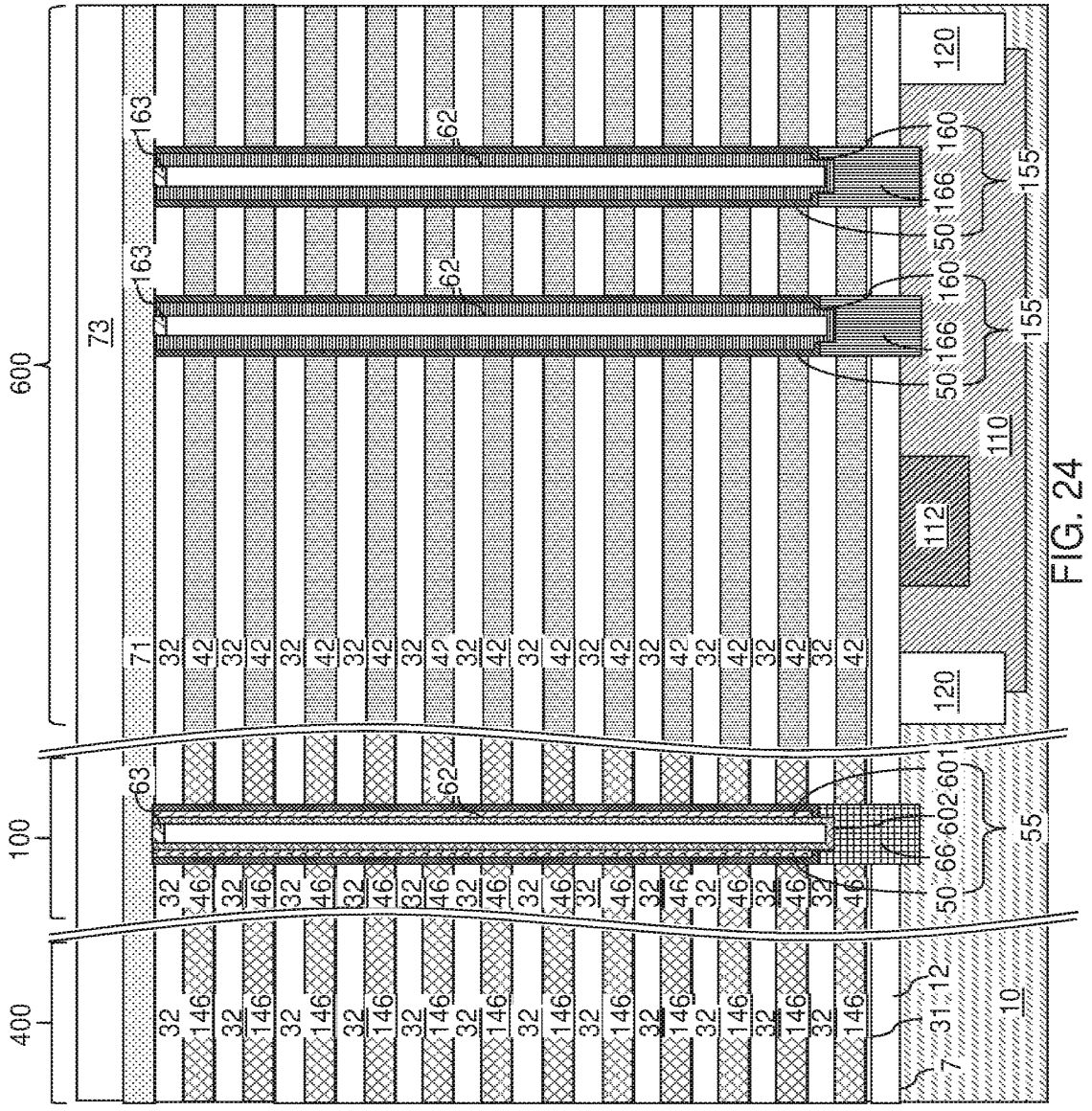

600
100
400
73
71
63
62
163
120
160
166
50
155
110
112
32
42
46
146
601
602
66
55
12
31
7
10

FIG. 24

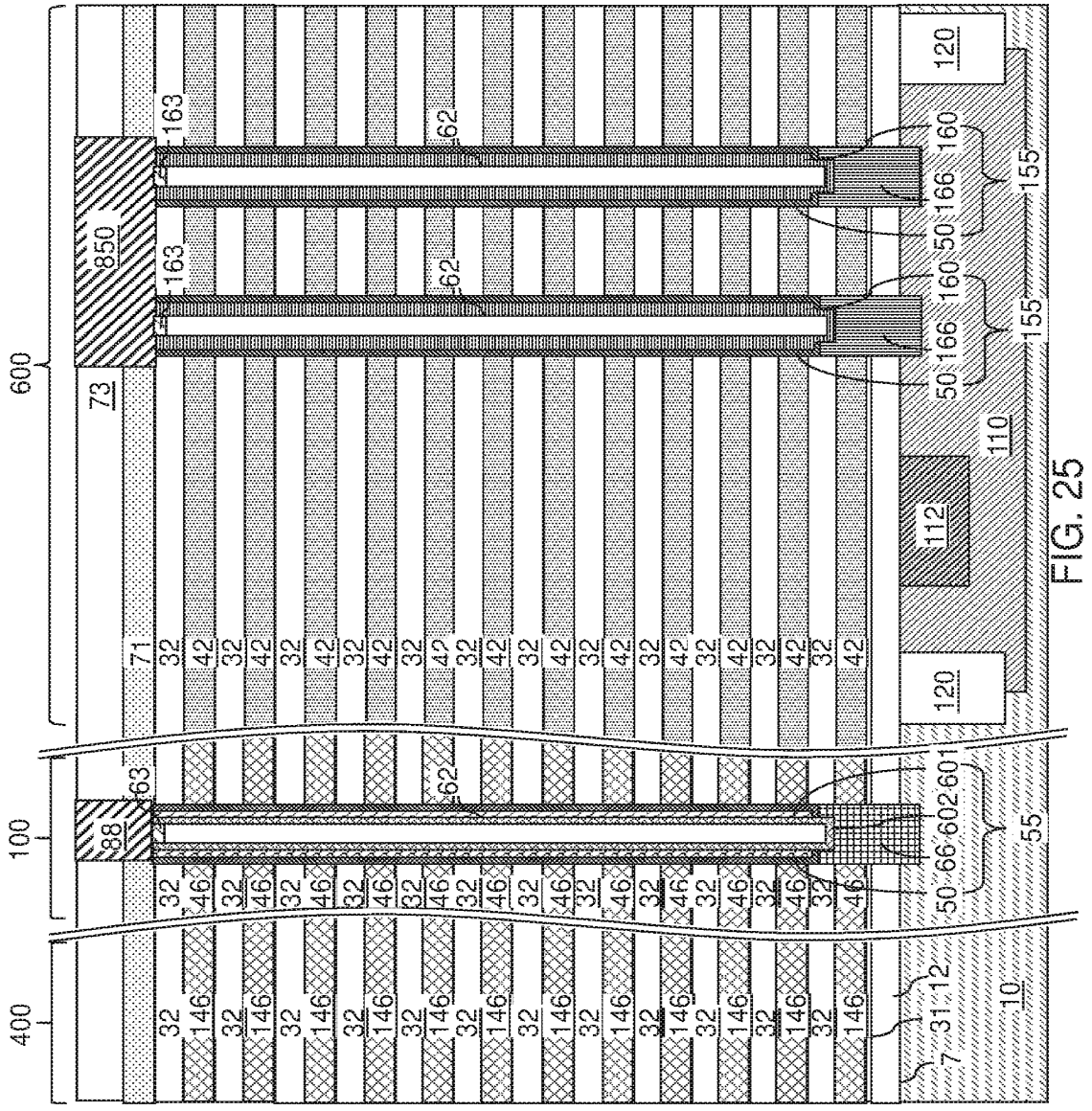


FIG. 25

Micron Ex. 1002, p. 333
Micron v. YMTC
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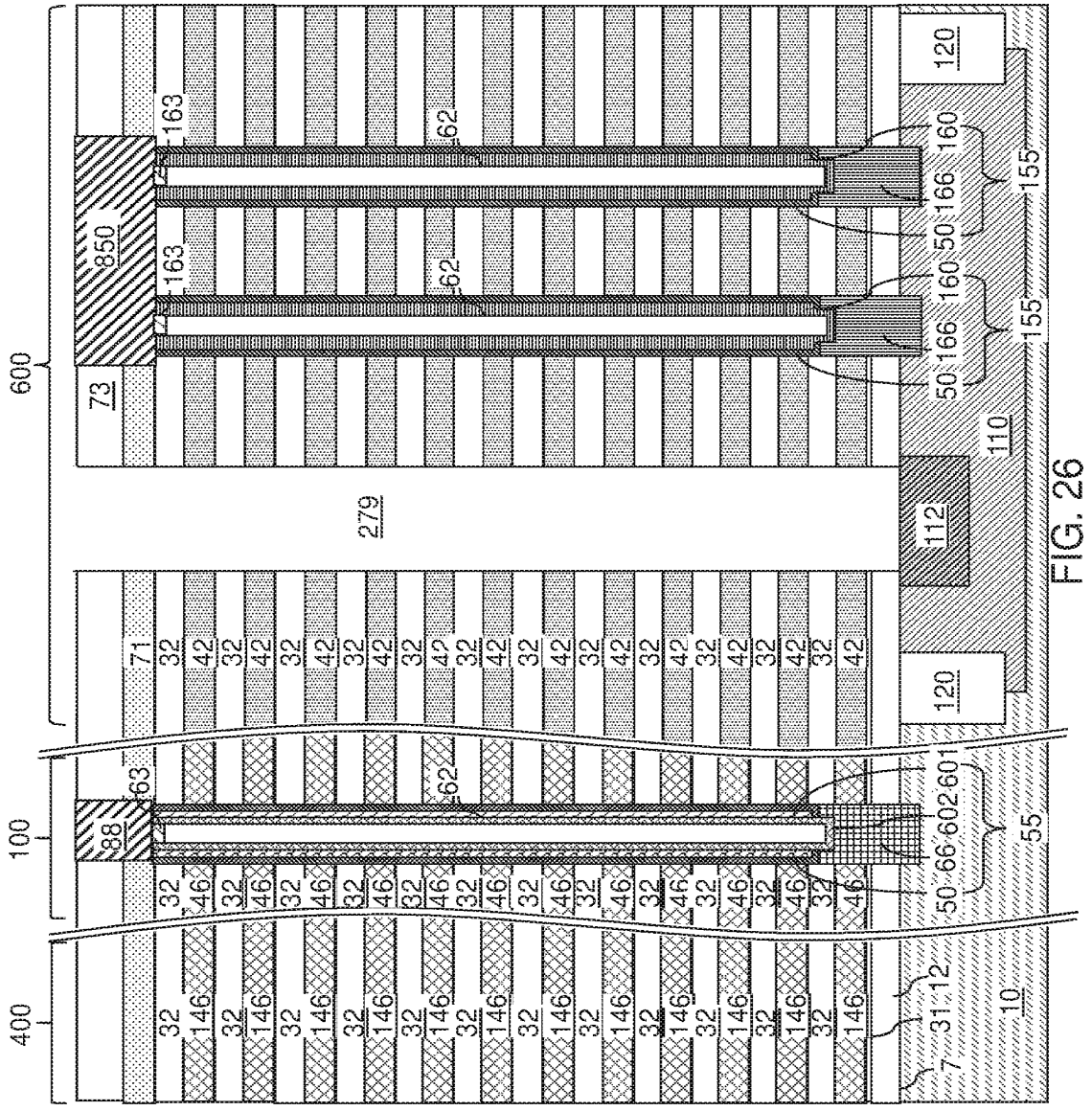

600
100
400
850
73
279
88
71
63
163
62
160
166
50
155
110
112
120
601
602
66
55
32
42
46
146
12
31
7
10

FIG. 26

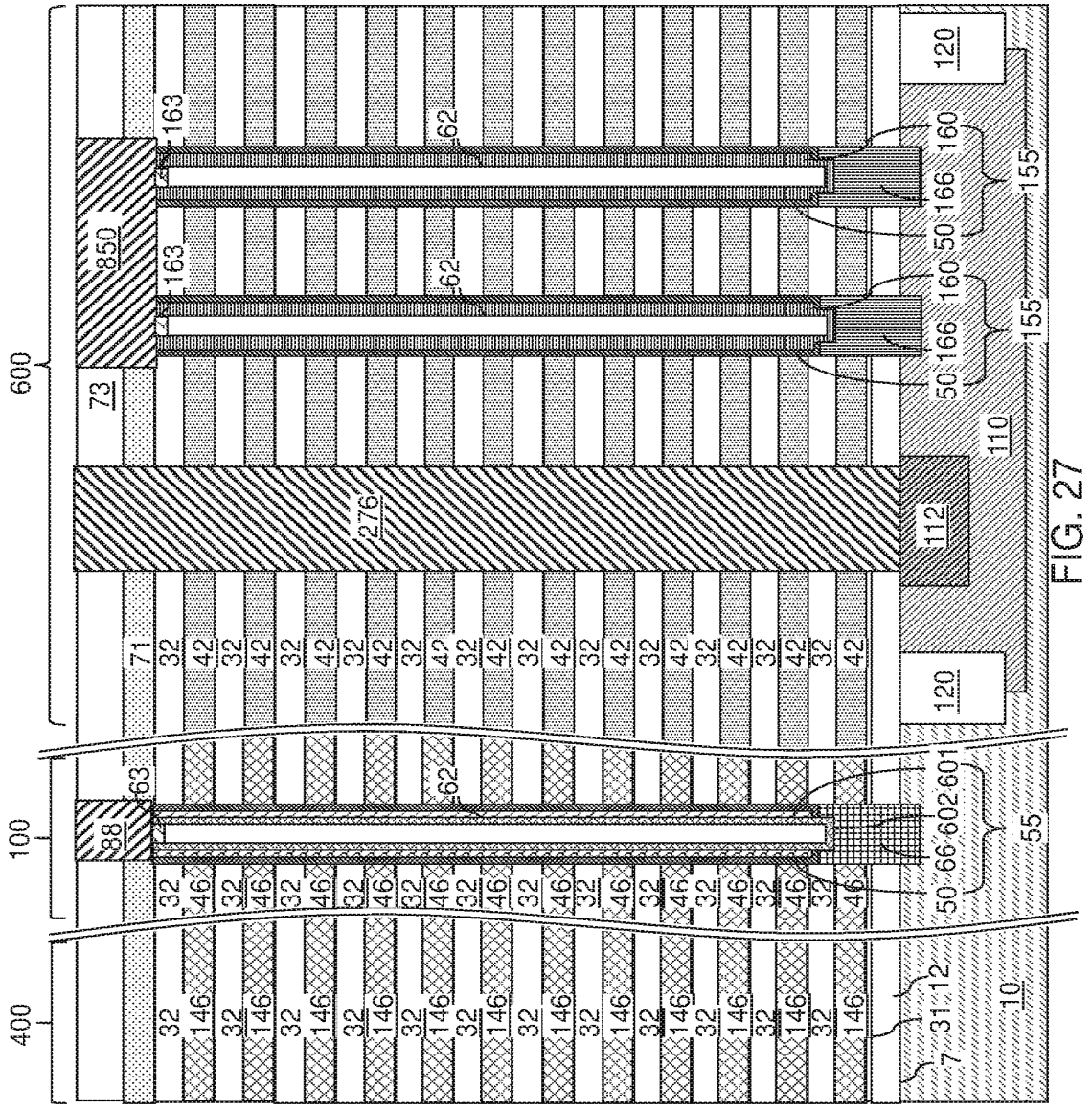


FIG. 27

Micron Ex. 1002, p. 335
Micron v. YMTC
IPR2024-00790

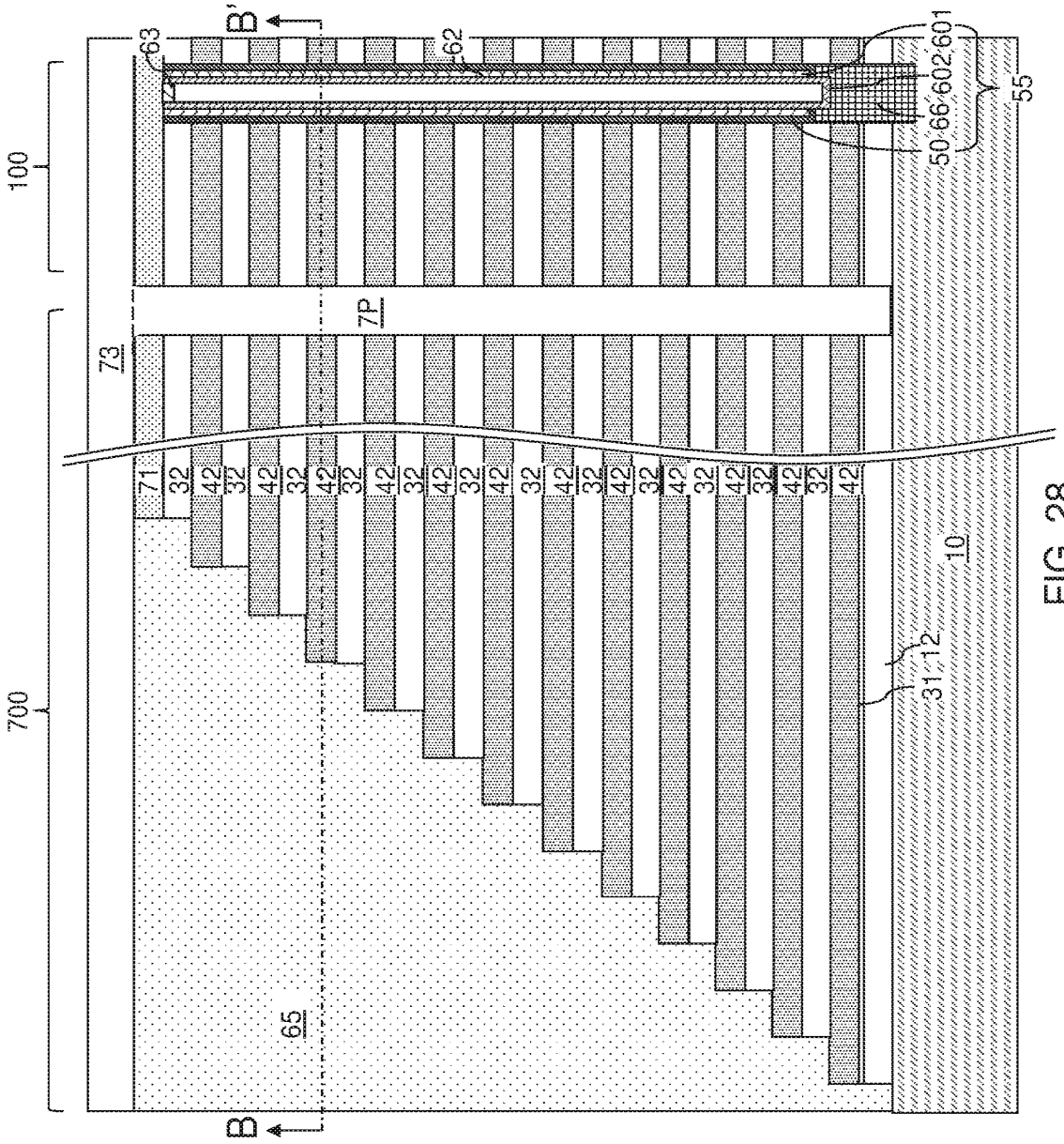


FIG. 28

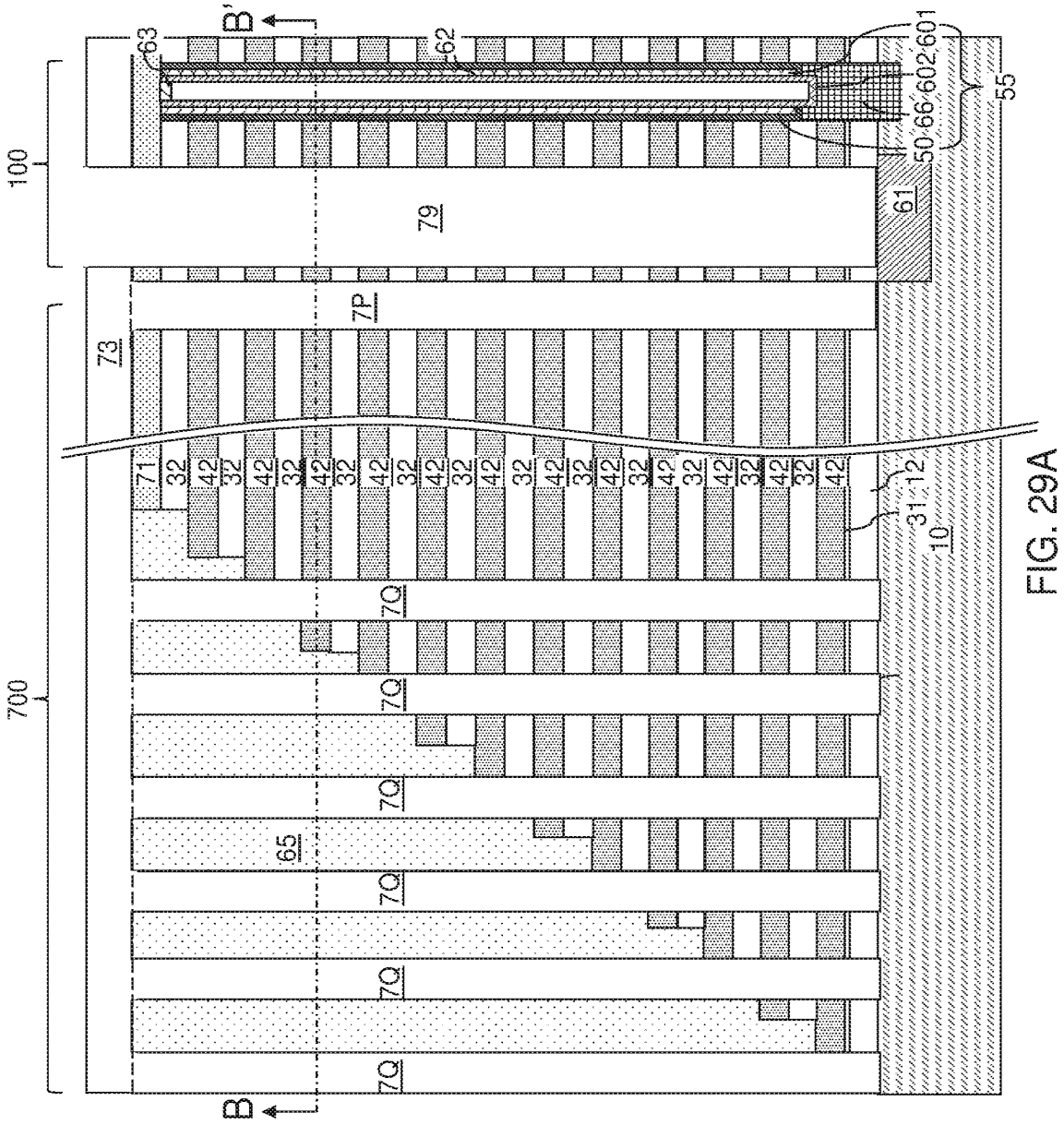


FIG. 29A

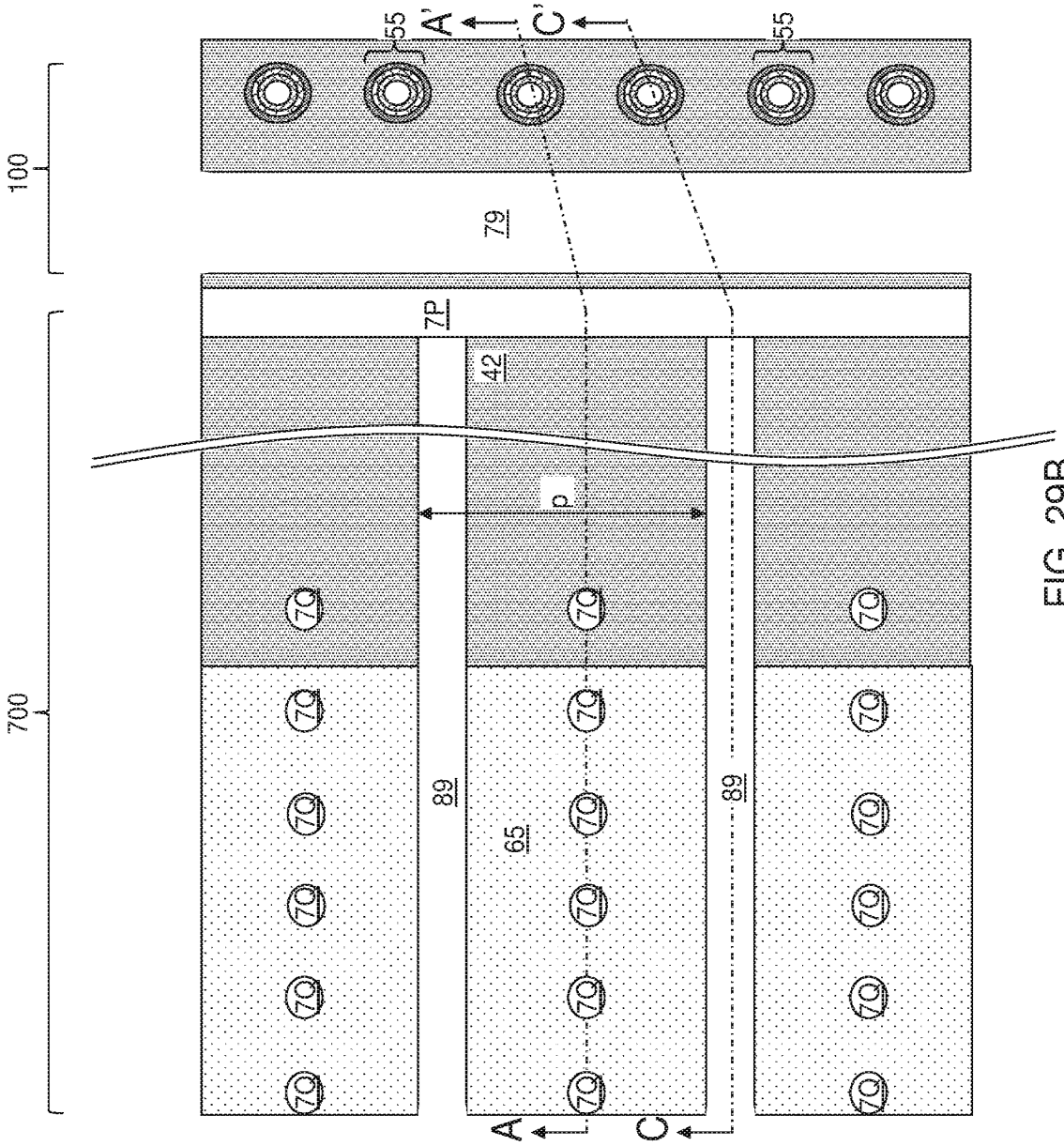


FIG. 29B

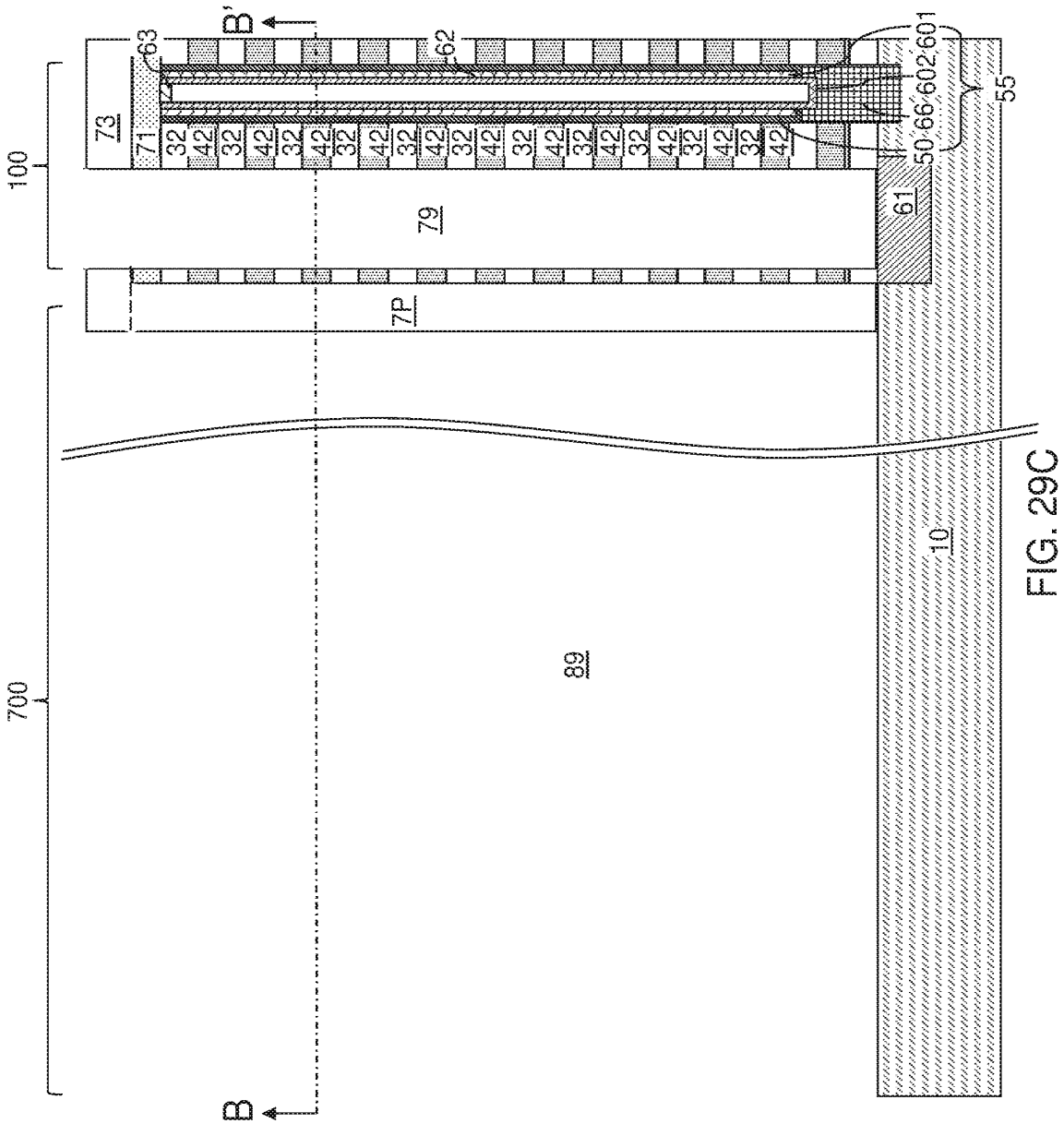


FIG. 29C

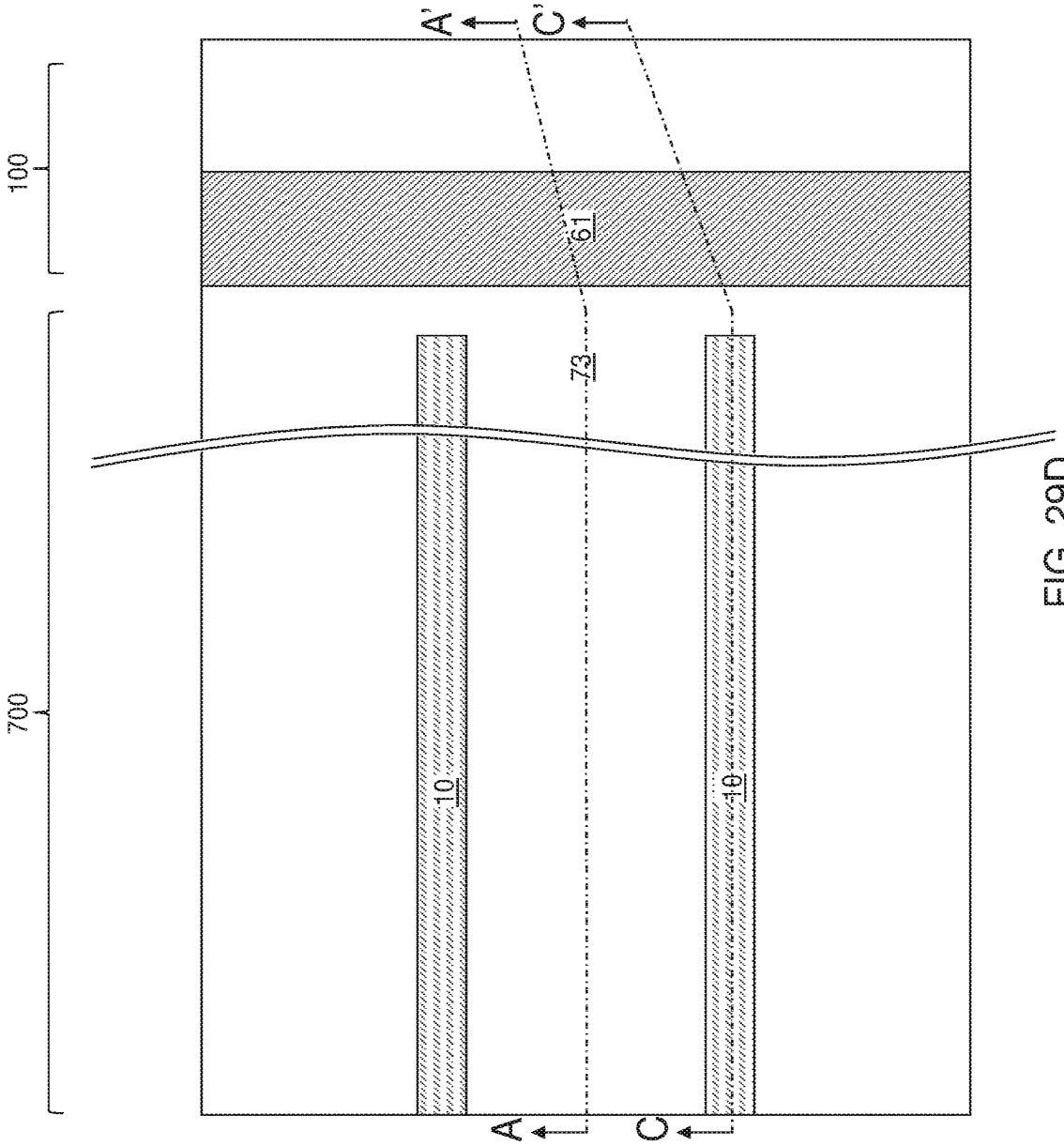


FIG. 29D

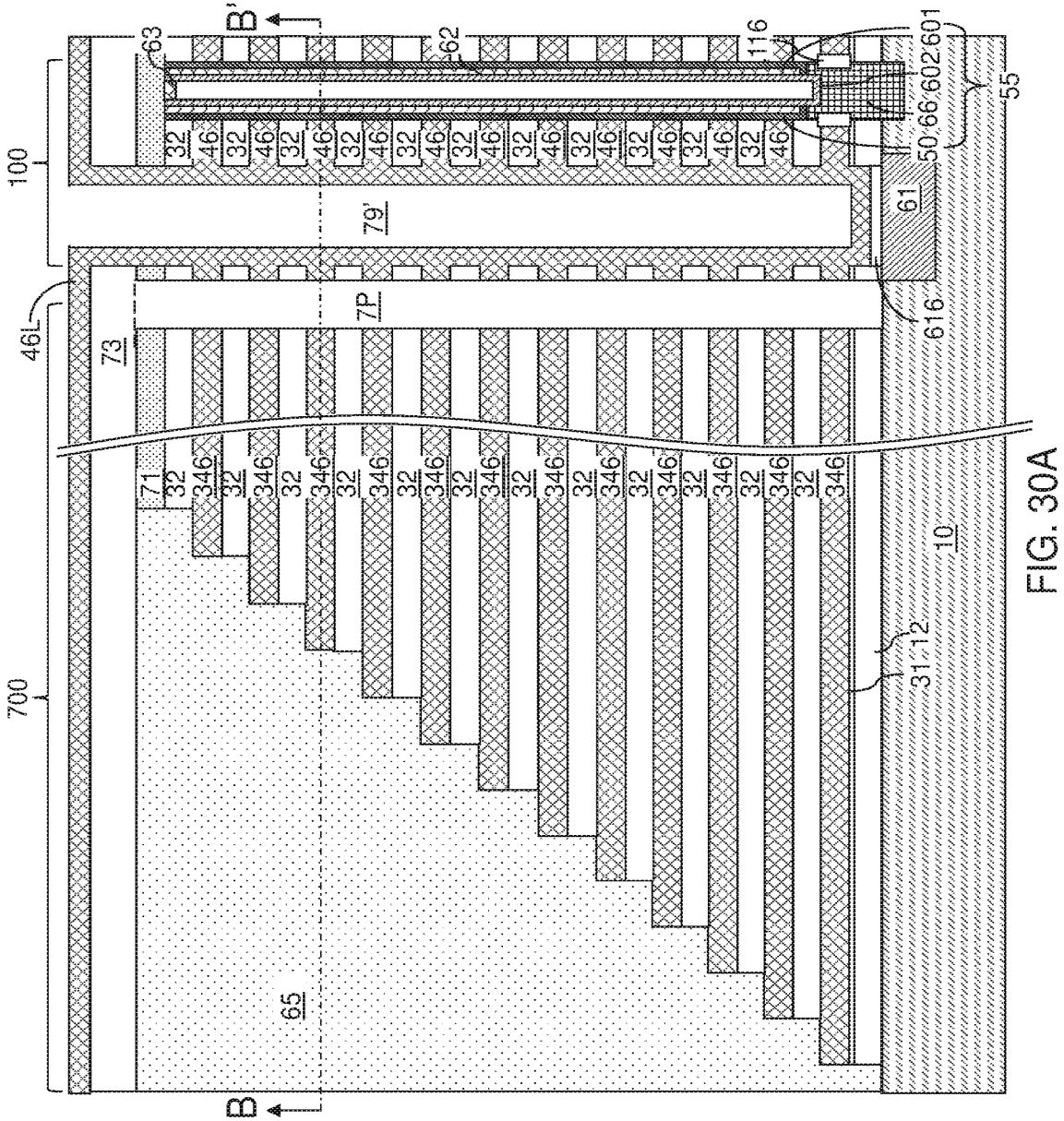

B'
B
63
62
116
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601
602
66
50
61
616
79'
7P
73
46L
100
700
71
65
10
12
31
32
46
346

FIG. 30A

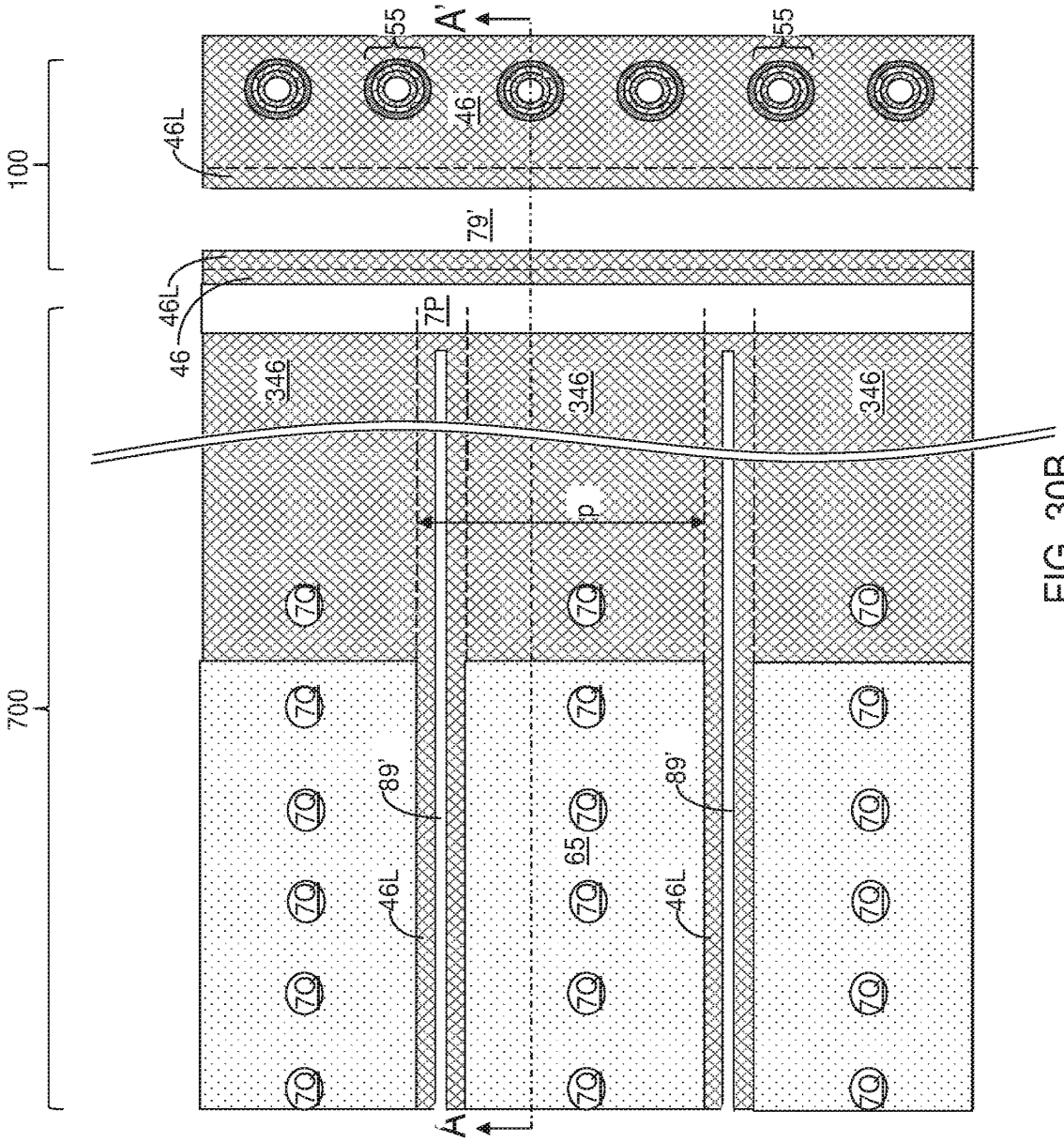

A'
55
55
46
46L
100
79'
46L
46
7P
346
346
346
p
70
89'
89'
65
46L
46L
700
A

FIG. 30B

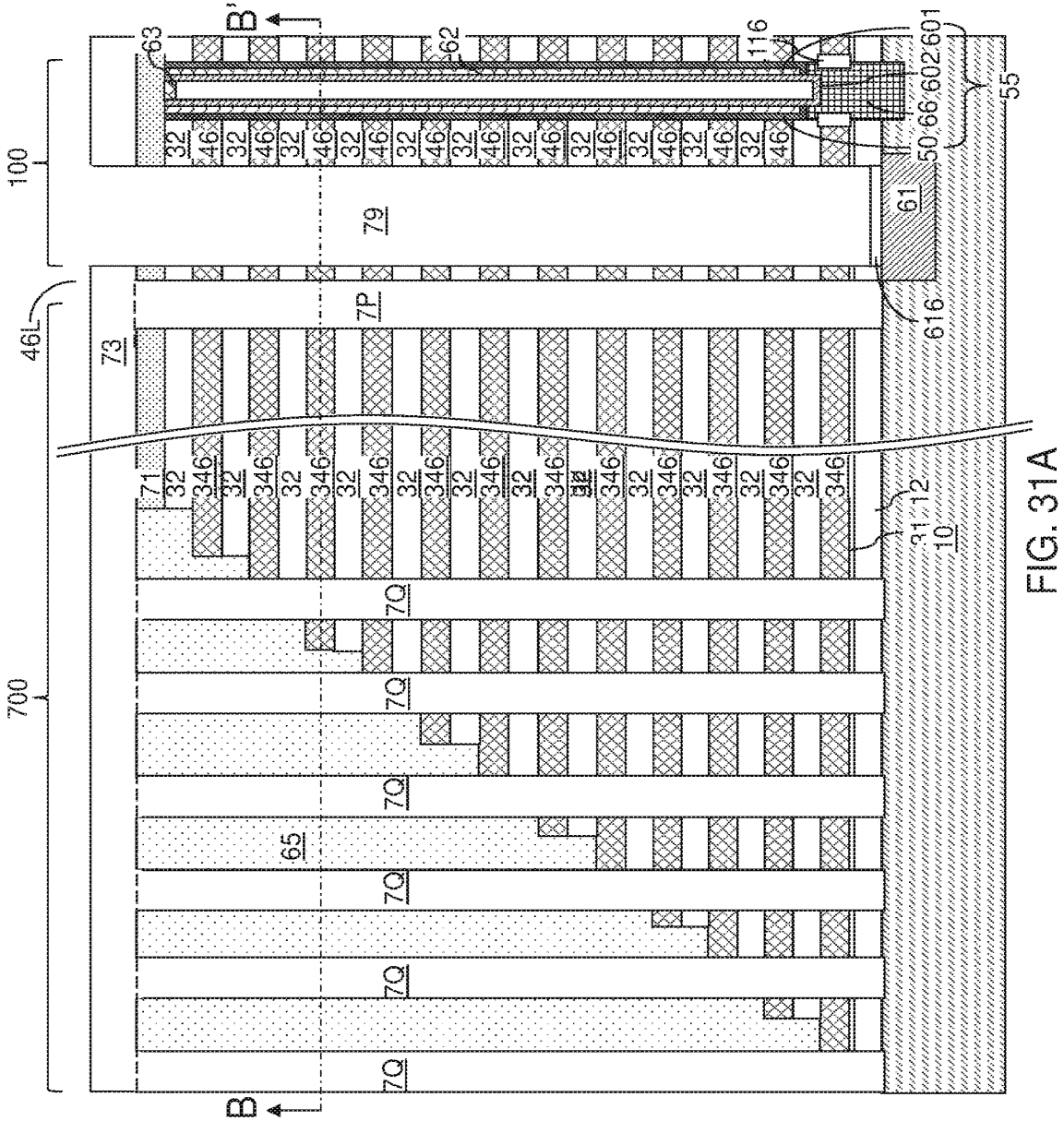

B'
B
63
62
116
601
602
66
50
55
61
616
100
79
7P
46L
73
71
32
346
46
31
12
10
7Q
700
65

FIG. 31A

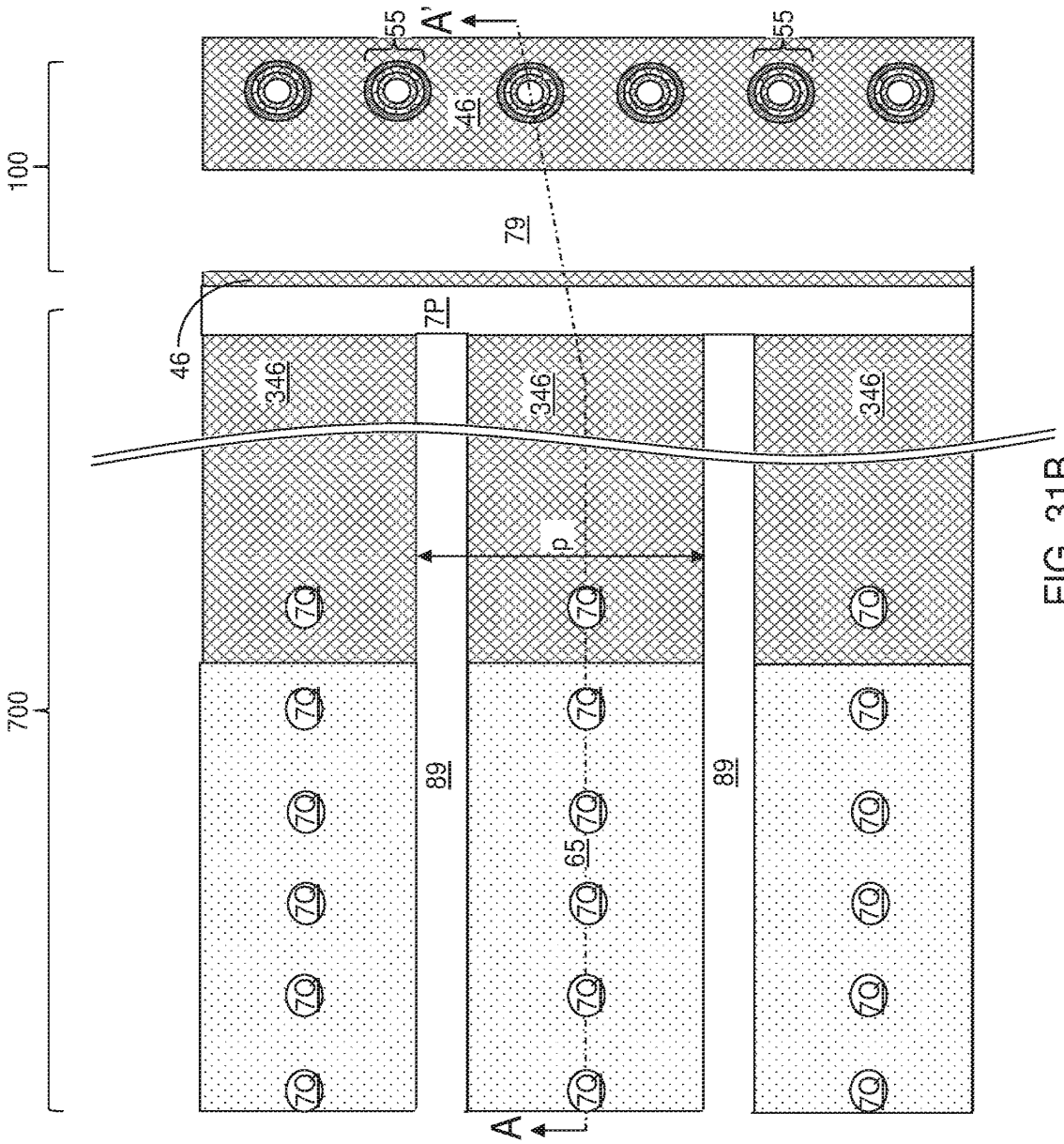


FIG. 31B

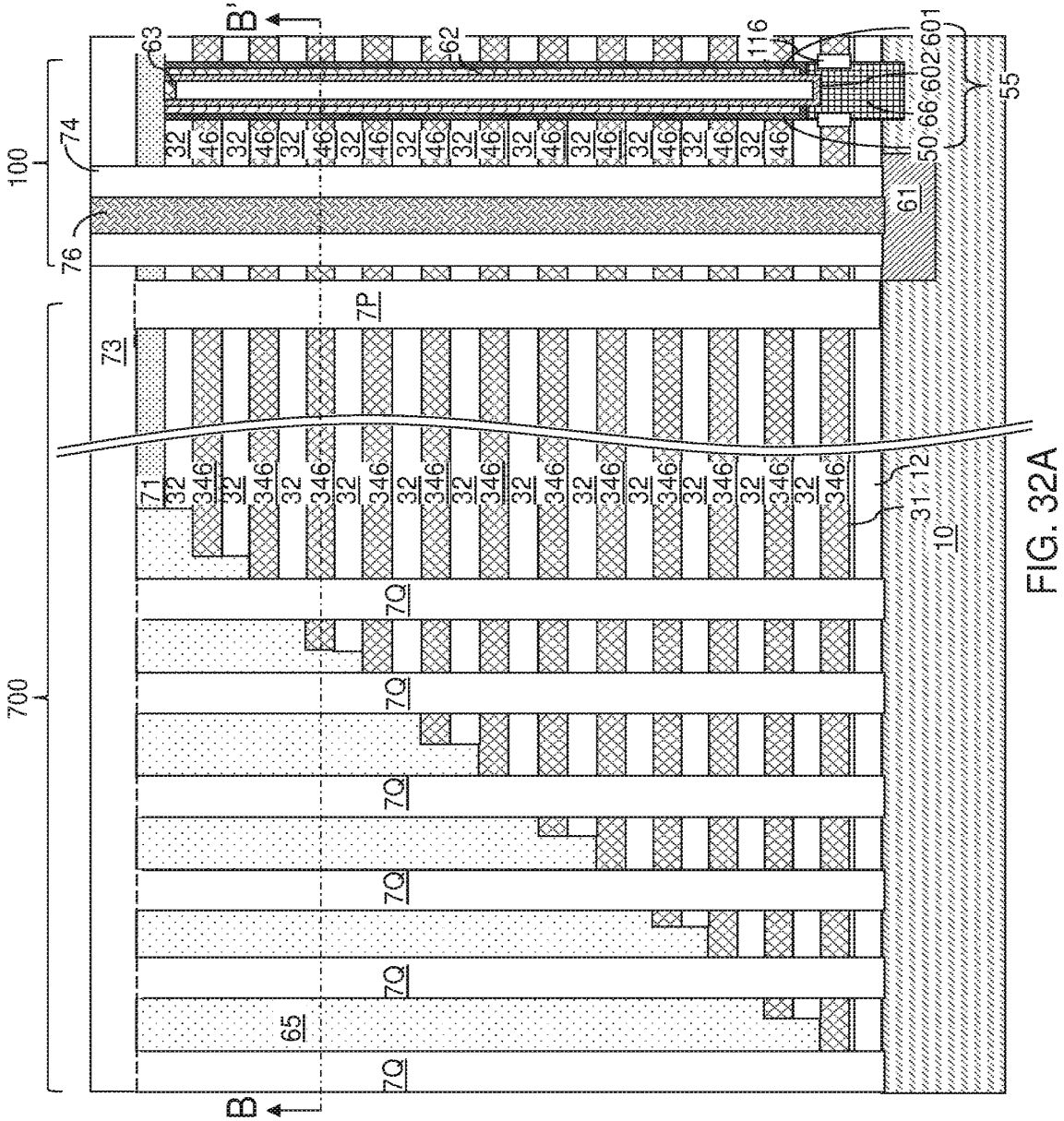

B'
B
63
62
116
55
50
66
602
601
61
100
74
76
7P
73
71
32
346
31
12
10
7Q
65
700

FIG. 32A

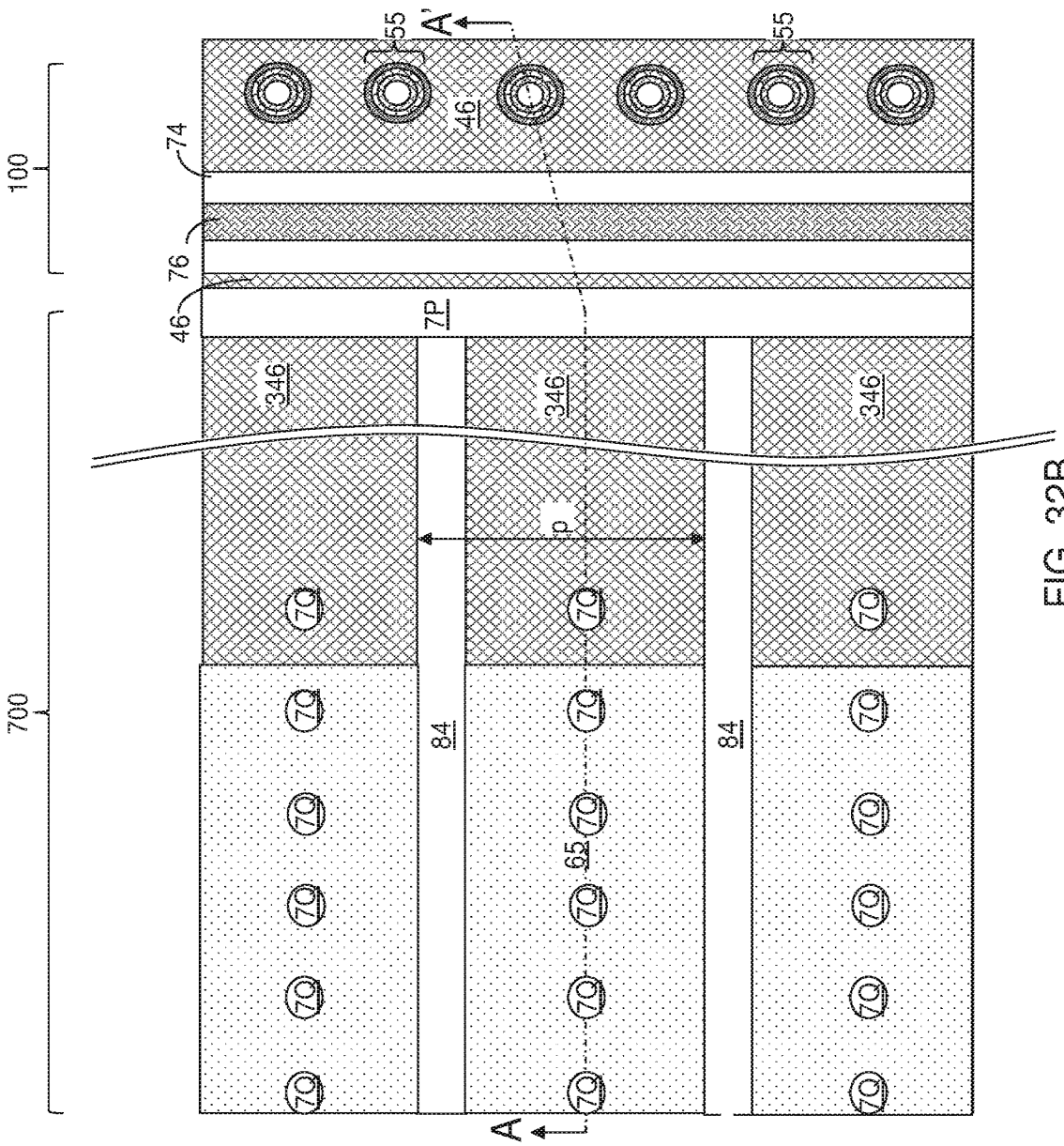


FIG. 32B

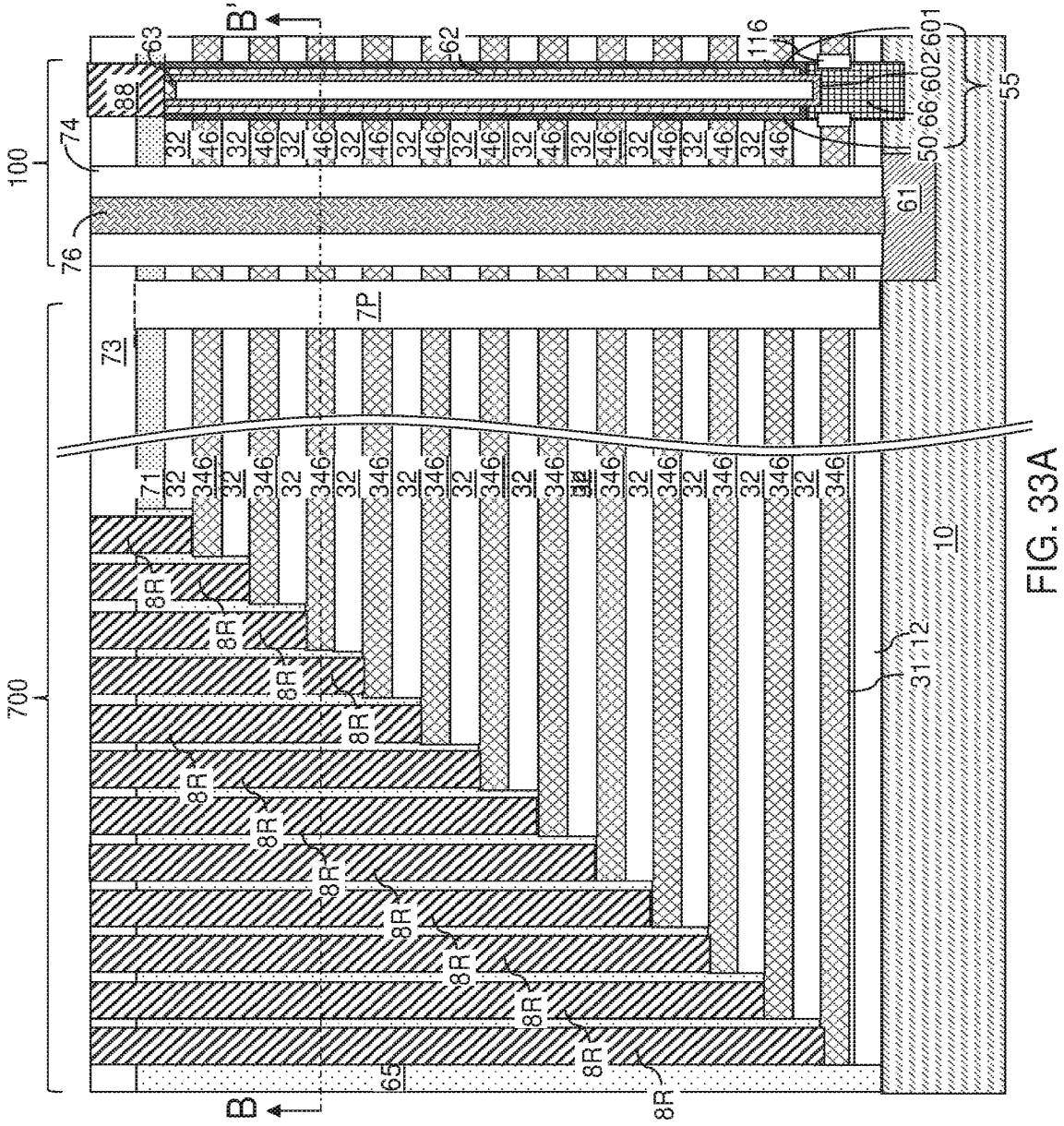

B'
B
63
62
116
55
601
602
66
50
61
100
74
76
7P
73
71
700
65
10
31
12
8R
32
46
346

FIG. 33A

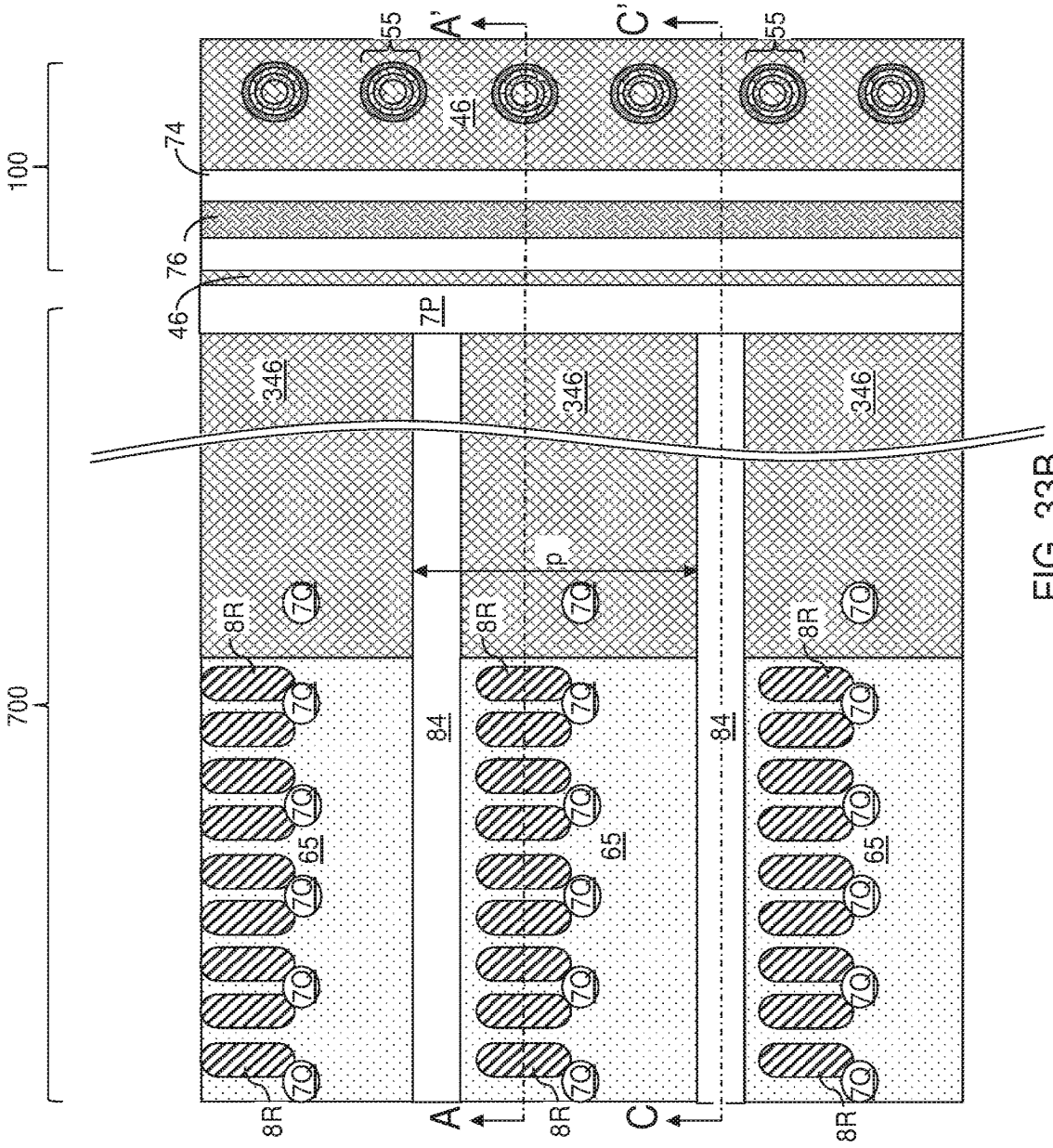


FIG. 33B

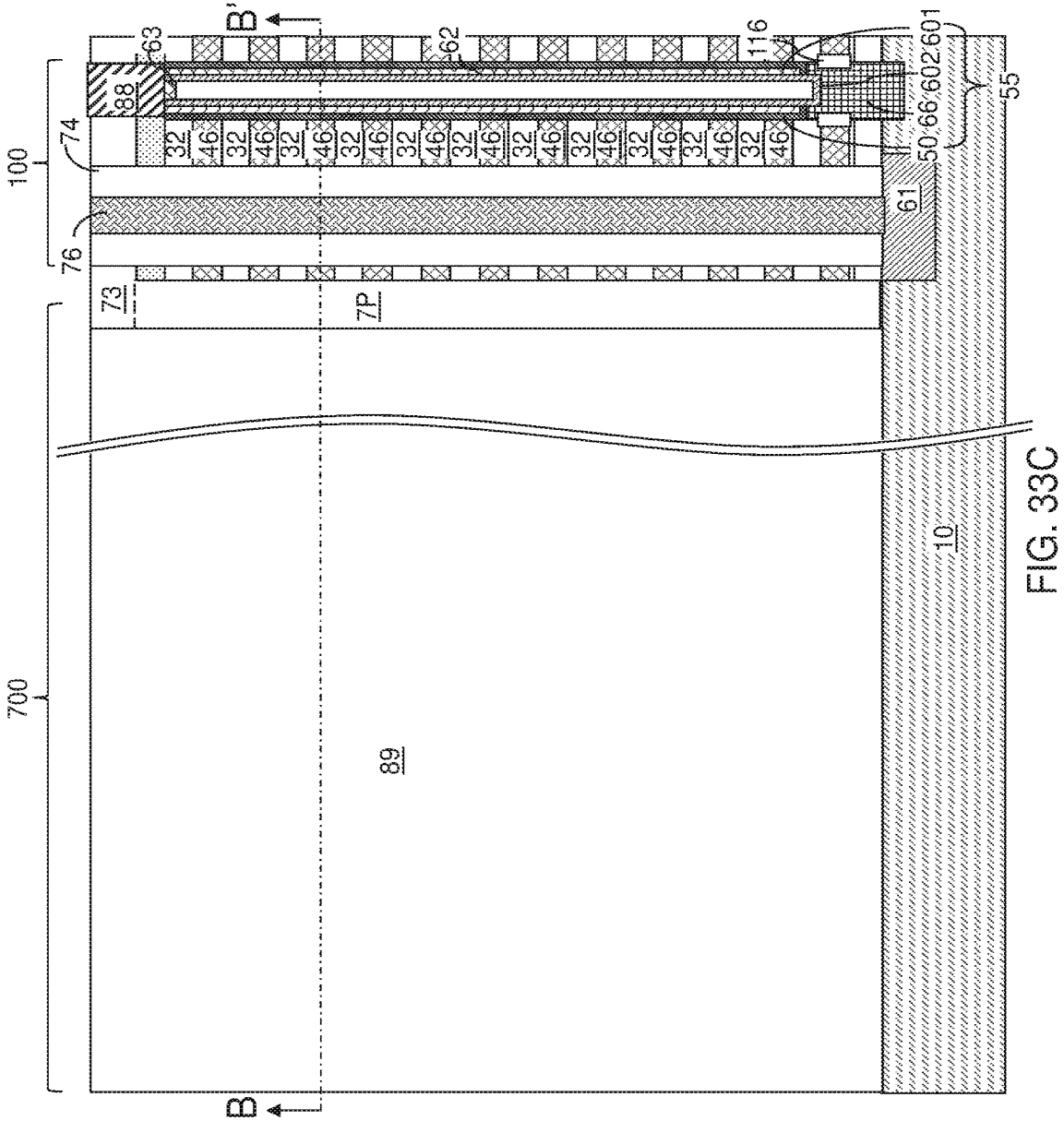


FIG. 33C

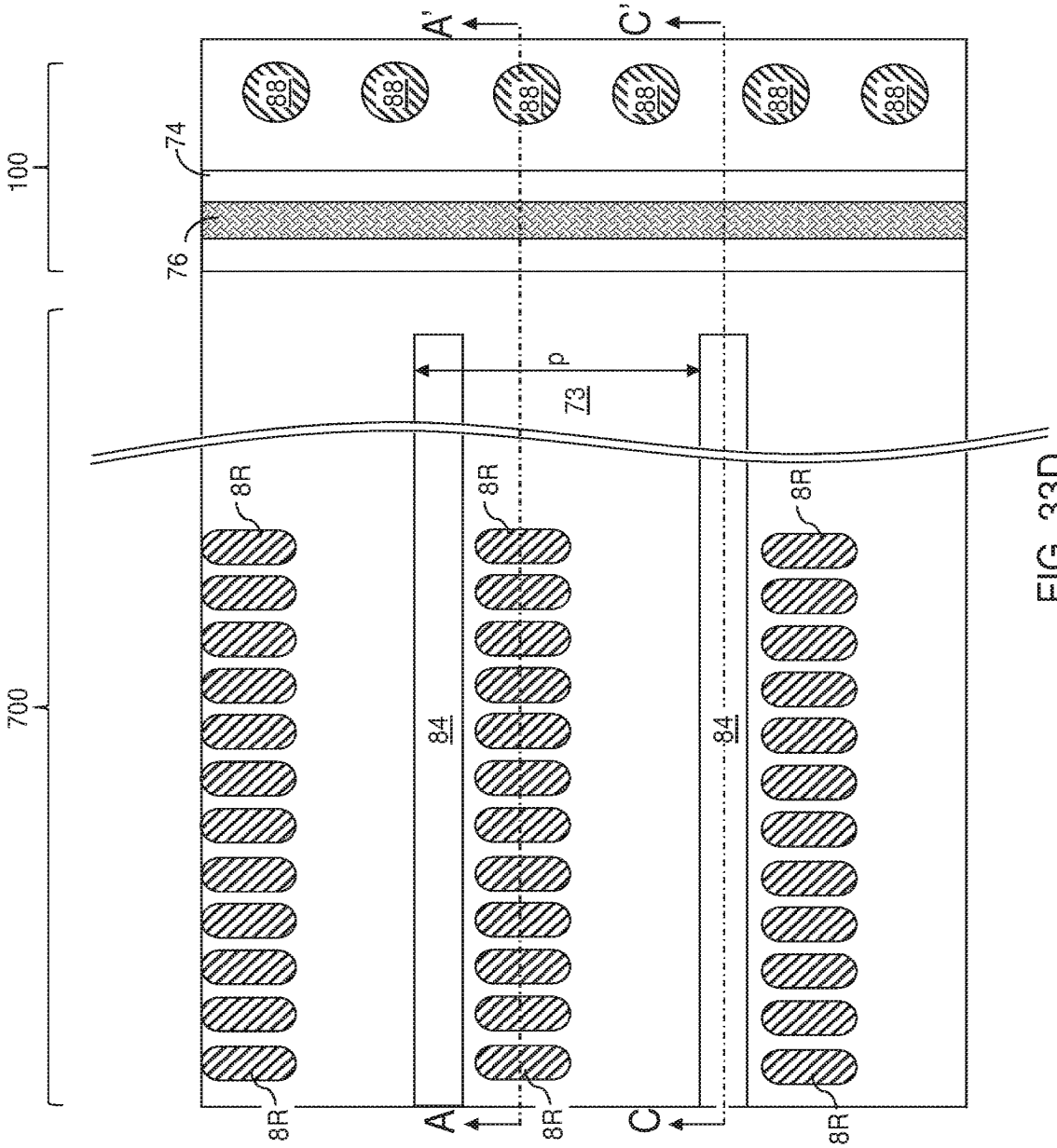


FIG. 33D

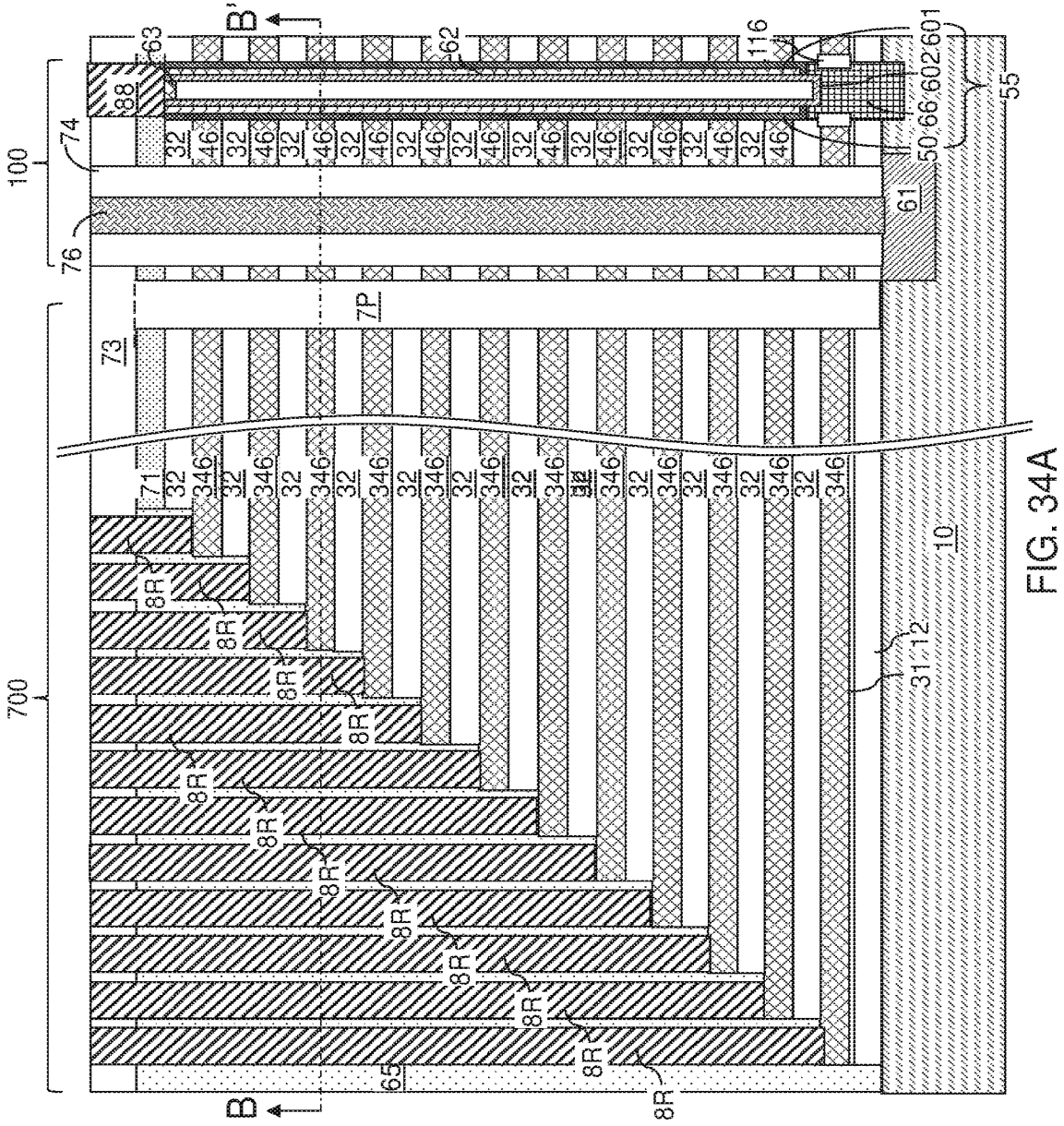

B'
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63
62
116
55
601
602
66
50
61
74
76
100
700
7P
73
71
346
32
46
8R
65
31
12
10

FIG. 34A

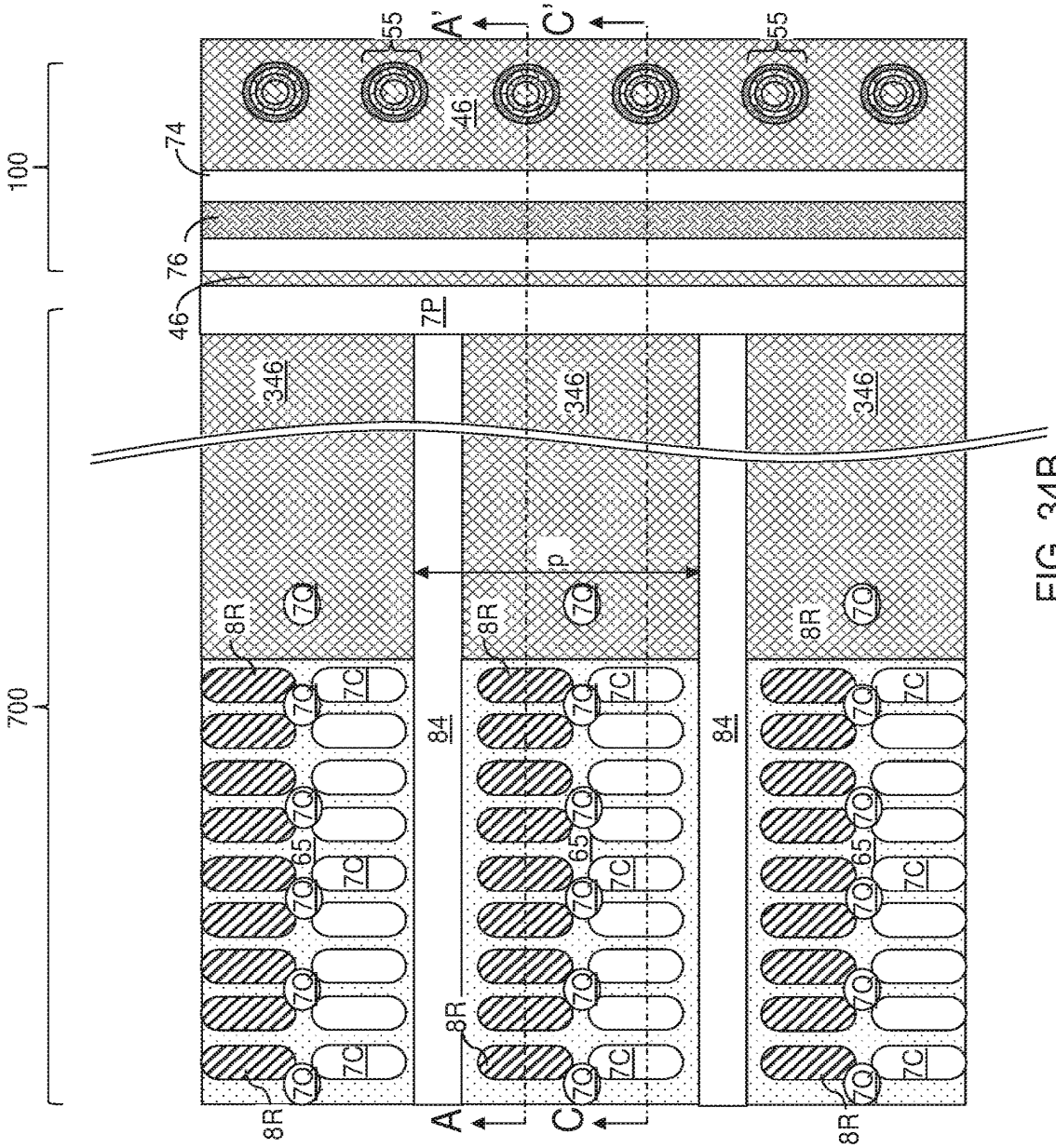


FIG. 34B

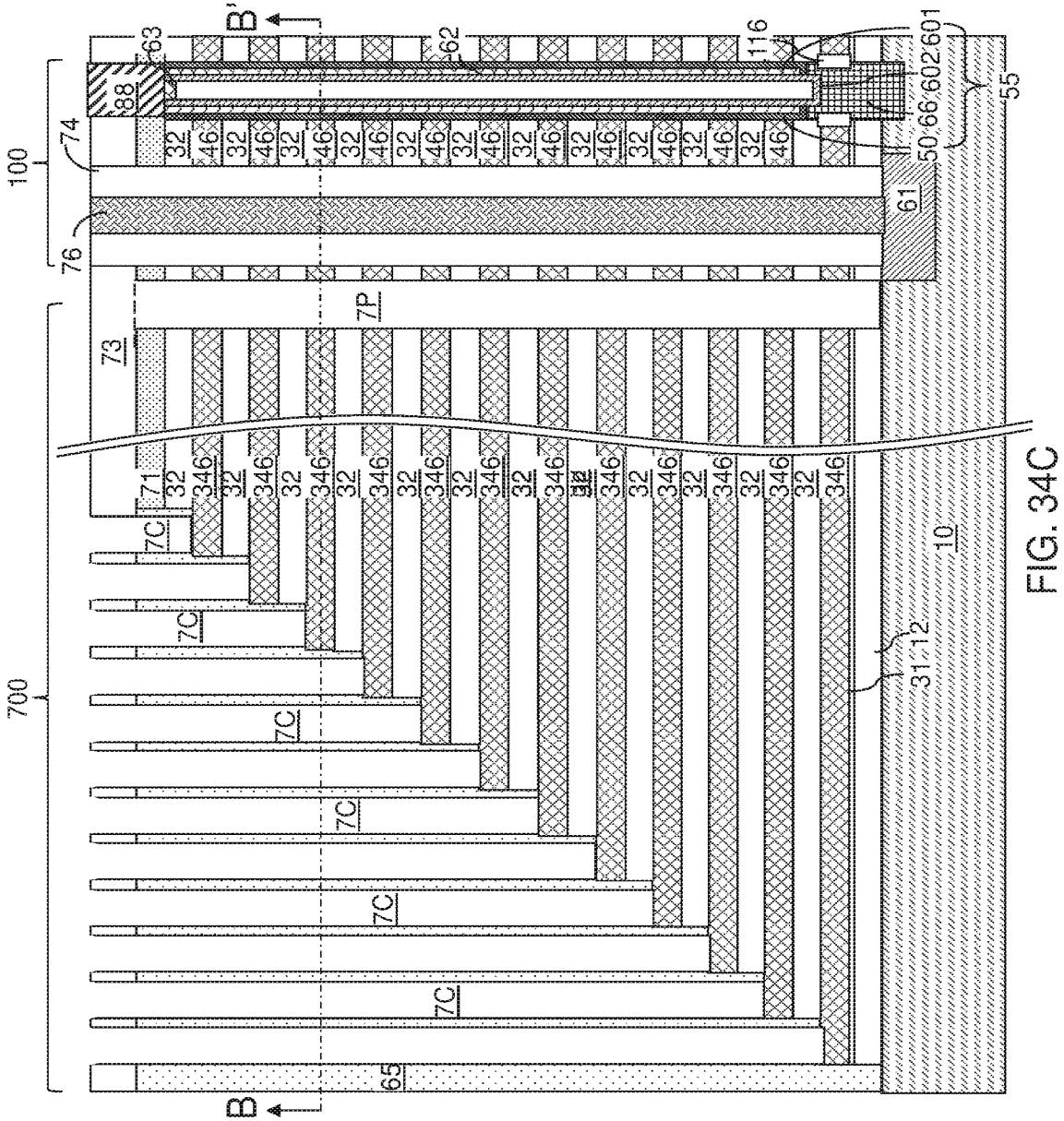

B'
B
63
62
116
55
50/66/602/601
61
100
74
76
7P
73
71
32
346
46
7C
700
10
31/12
65
88

FIG. 34C

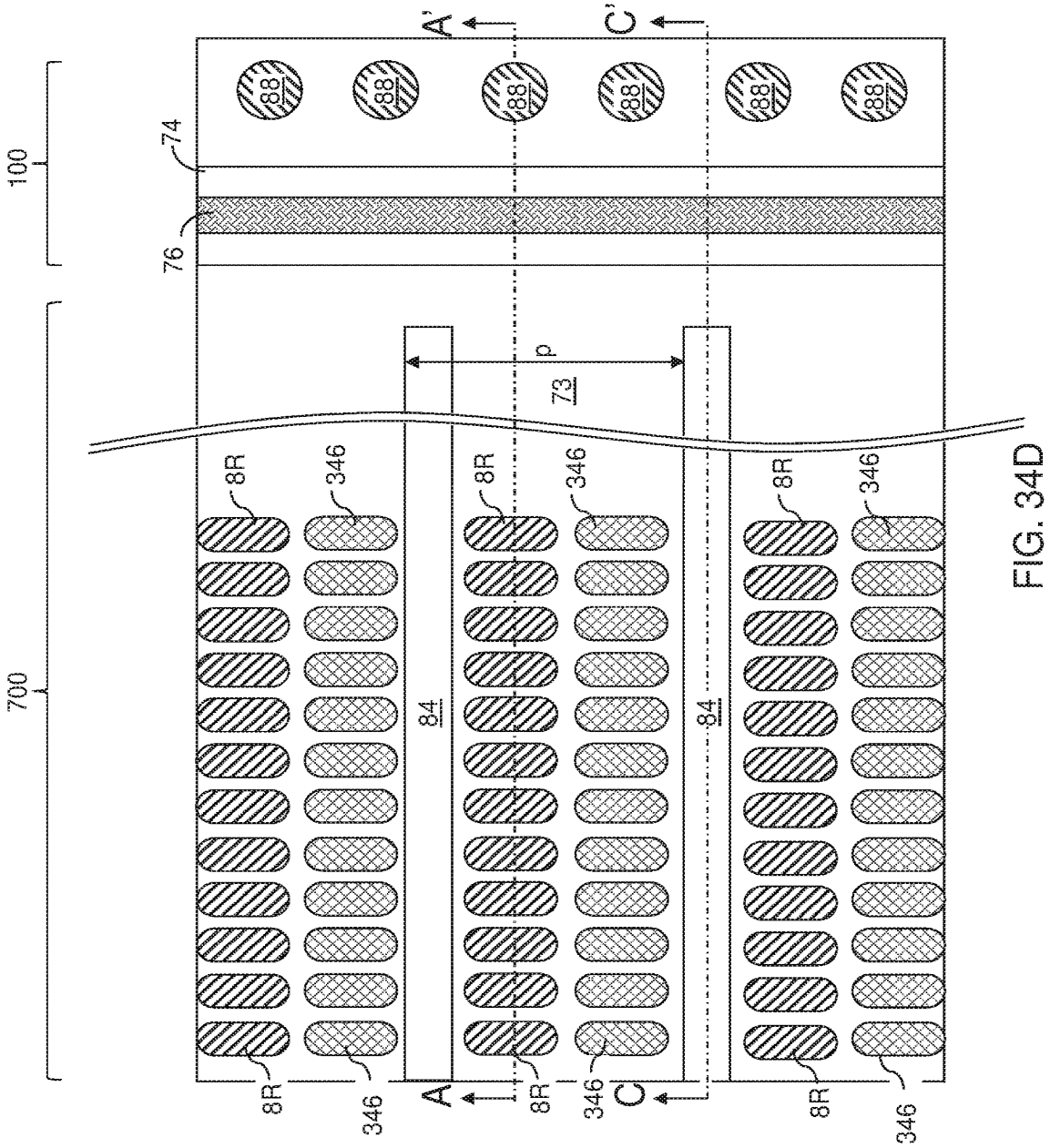


FIG. 34D

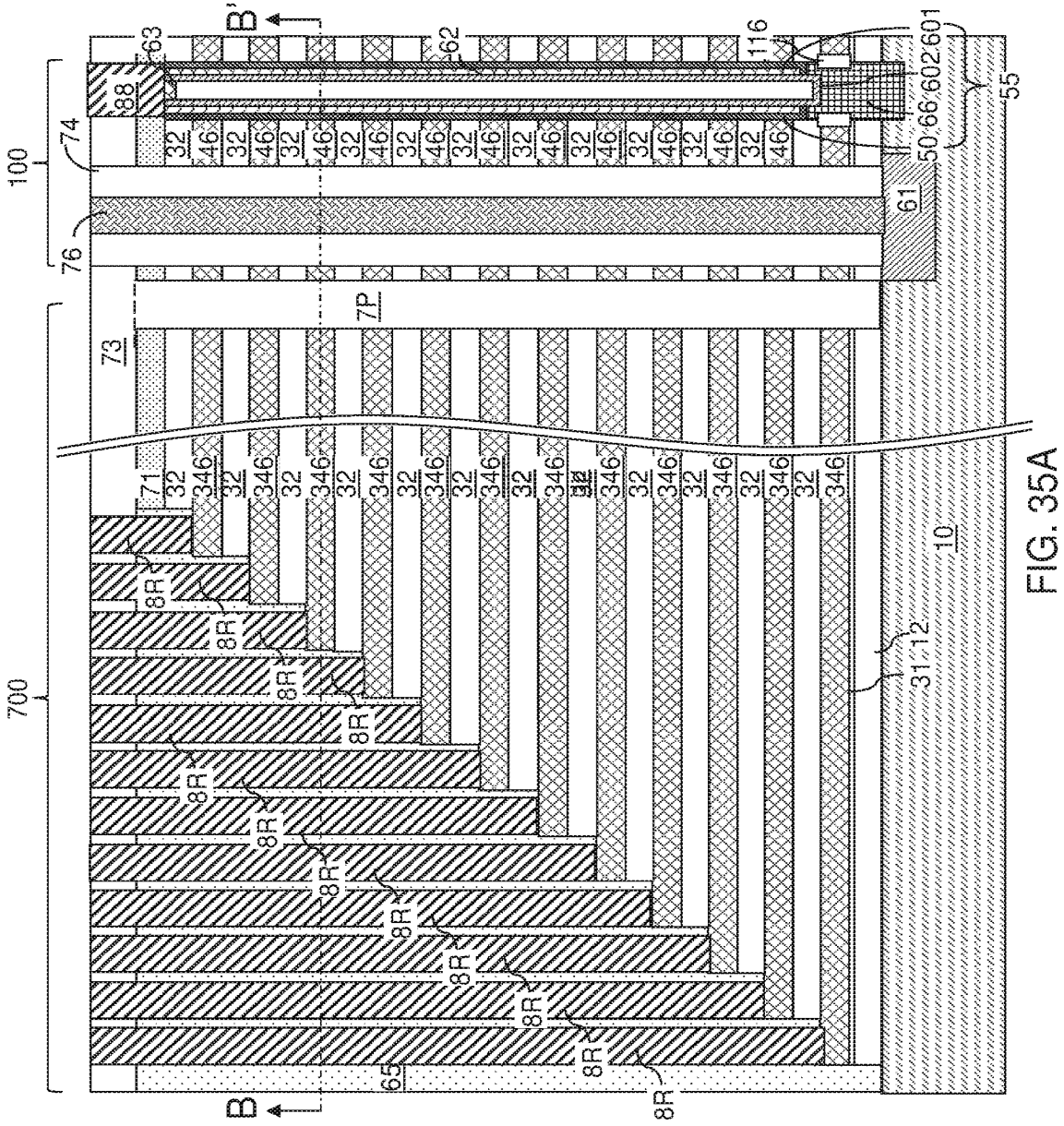

B'
B
63
62
116
601
602
66
50
55
88
74
100
76
61
7P
73
71
32
346
46
8R
700
31
12
10
65

FIG. 35A

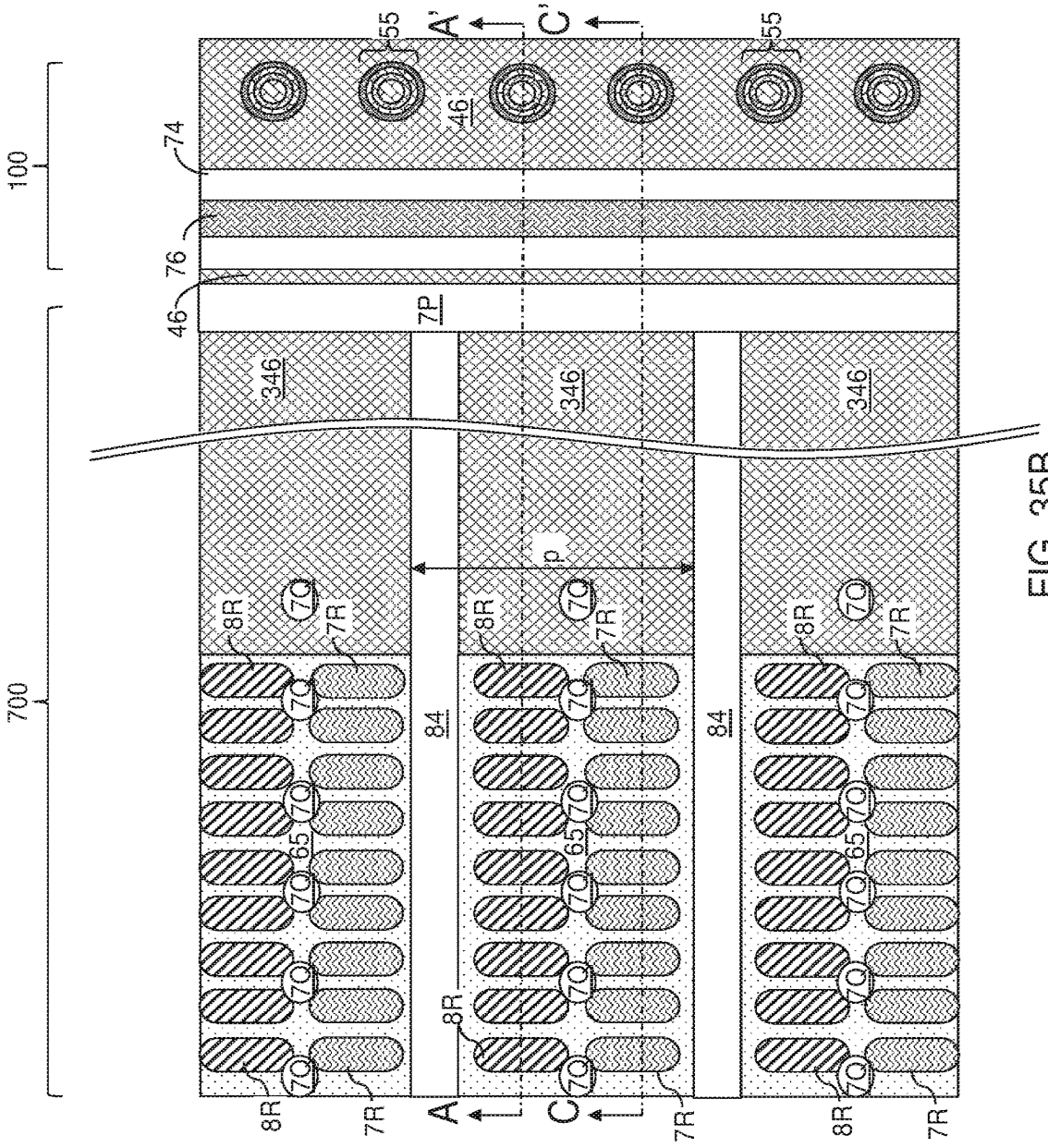

100
700
74
76
46
55
A'
C'
46
7P
346
346
346
p
8R
7Q
7R
84
84
65
A
C
7R
8R
7R
8R
7R

FIG. 35B

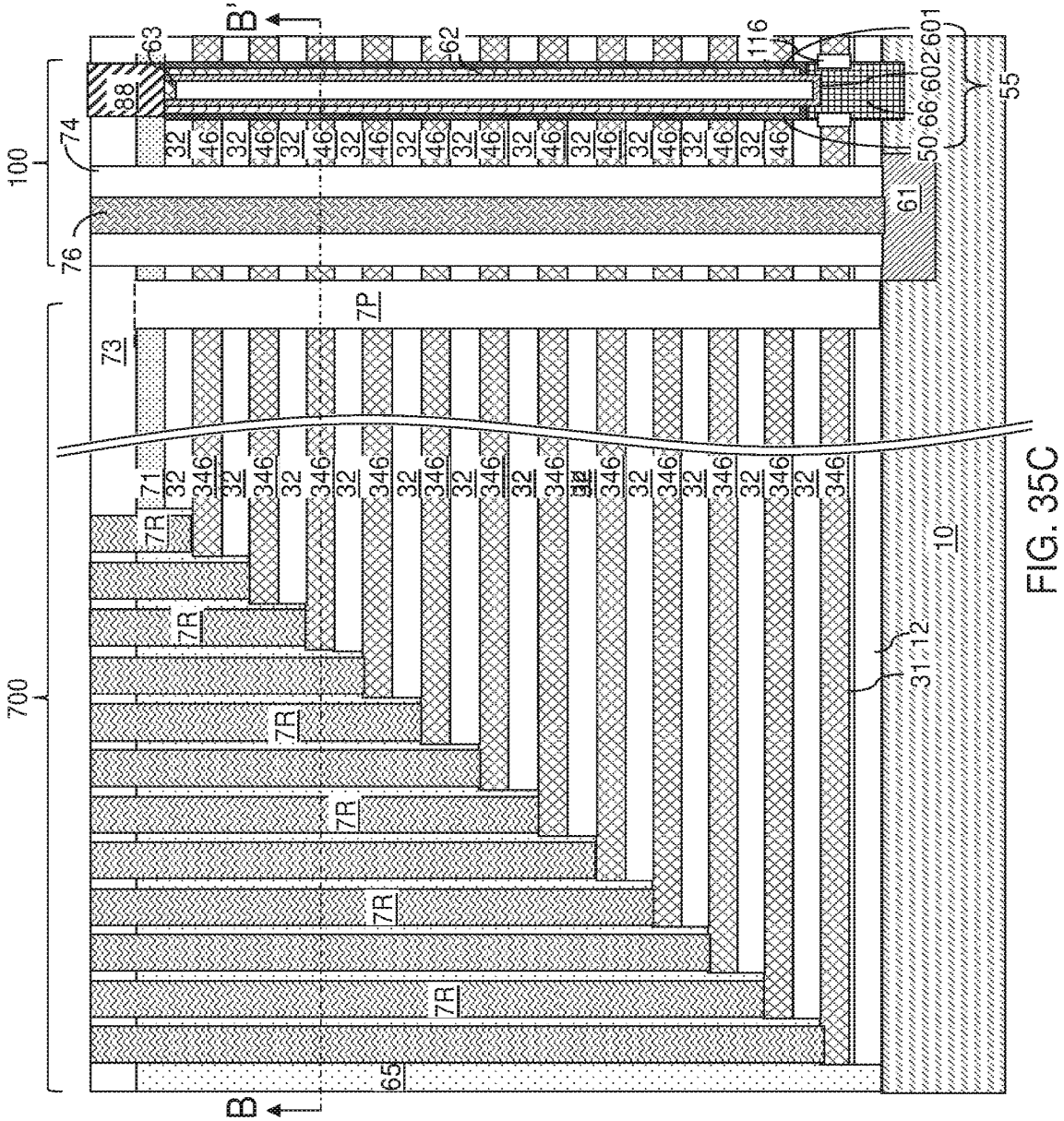

B'
B
63
62
116
601
602
66
50
55
88
74
100
76
61
7P
73
71
7R
32
46
346
700
65
10
31
12

FIG. 35C

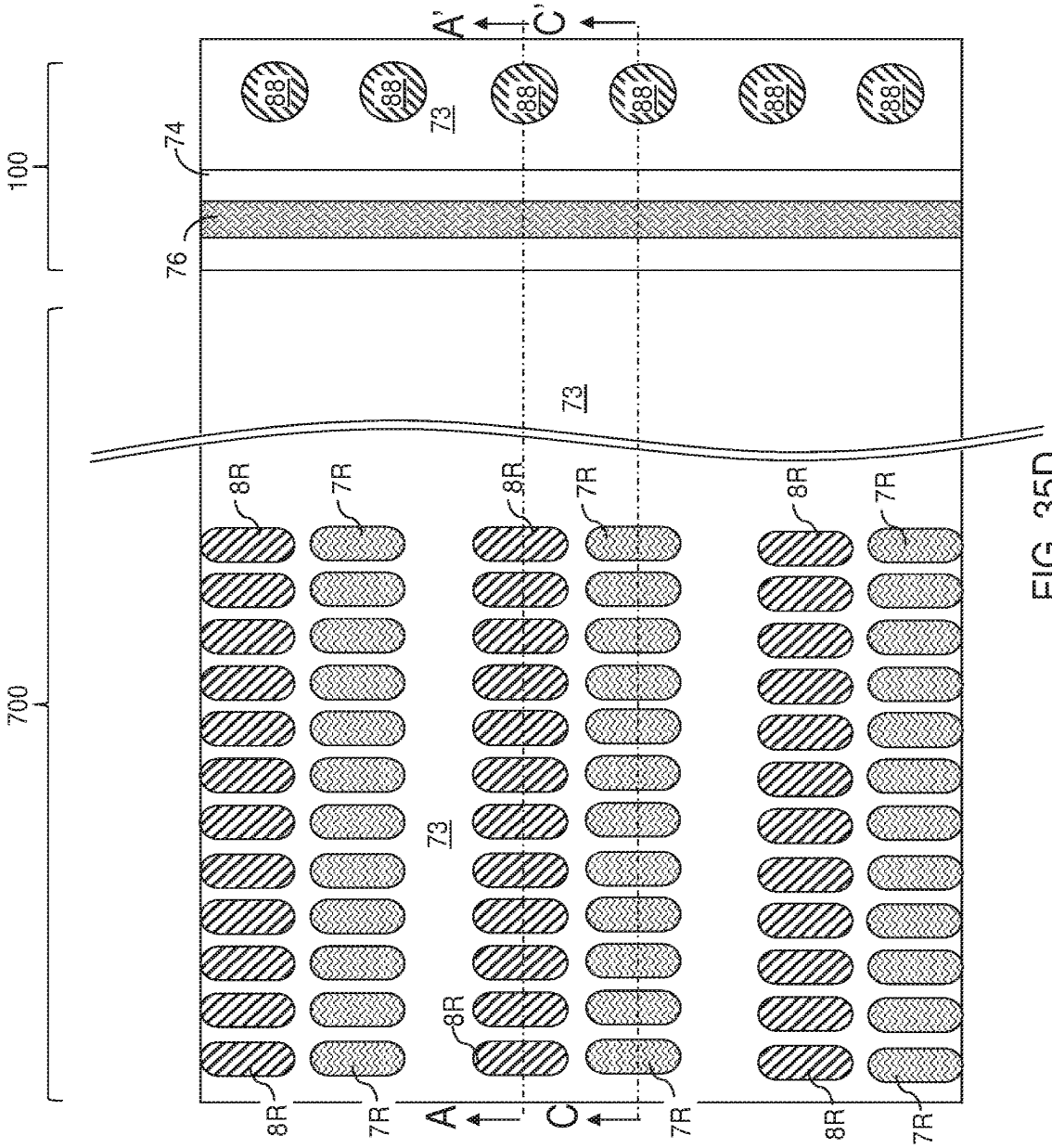


FIG. 35D

Micron Ex. 1002, p. 358
Micron v. YMTC
IPR2024-00790

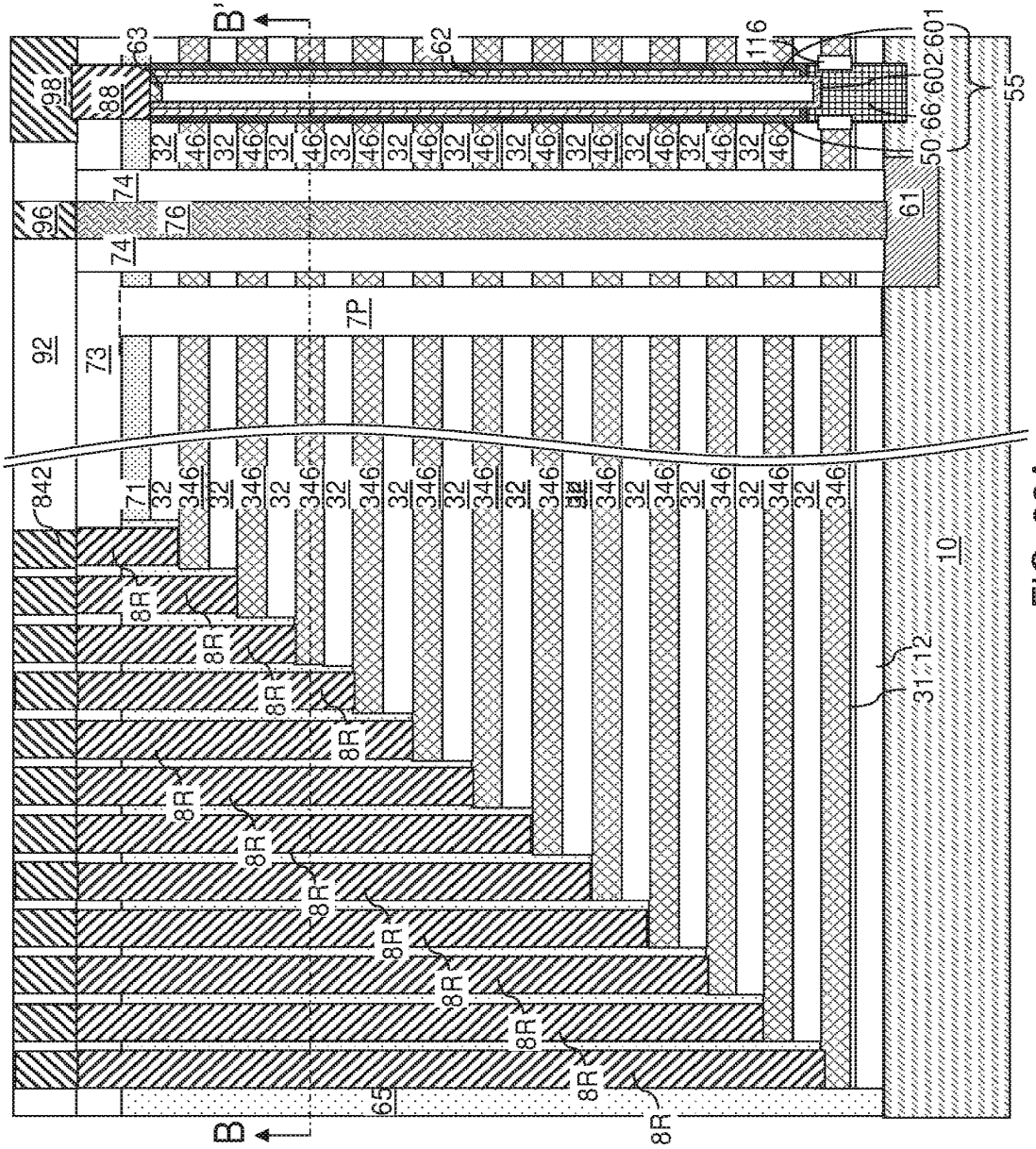

B'
B
63
62
116
601
602
66
50
55
98
88
32
46
74
96
76
61
92
73
7P
842
71
346
10
31
12
8R
65

FIG. 36A

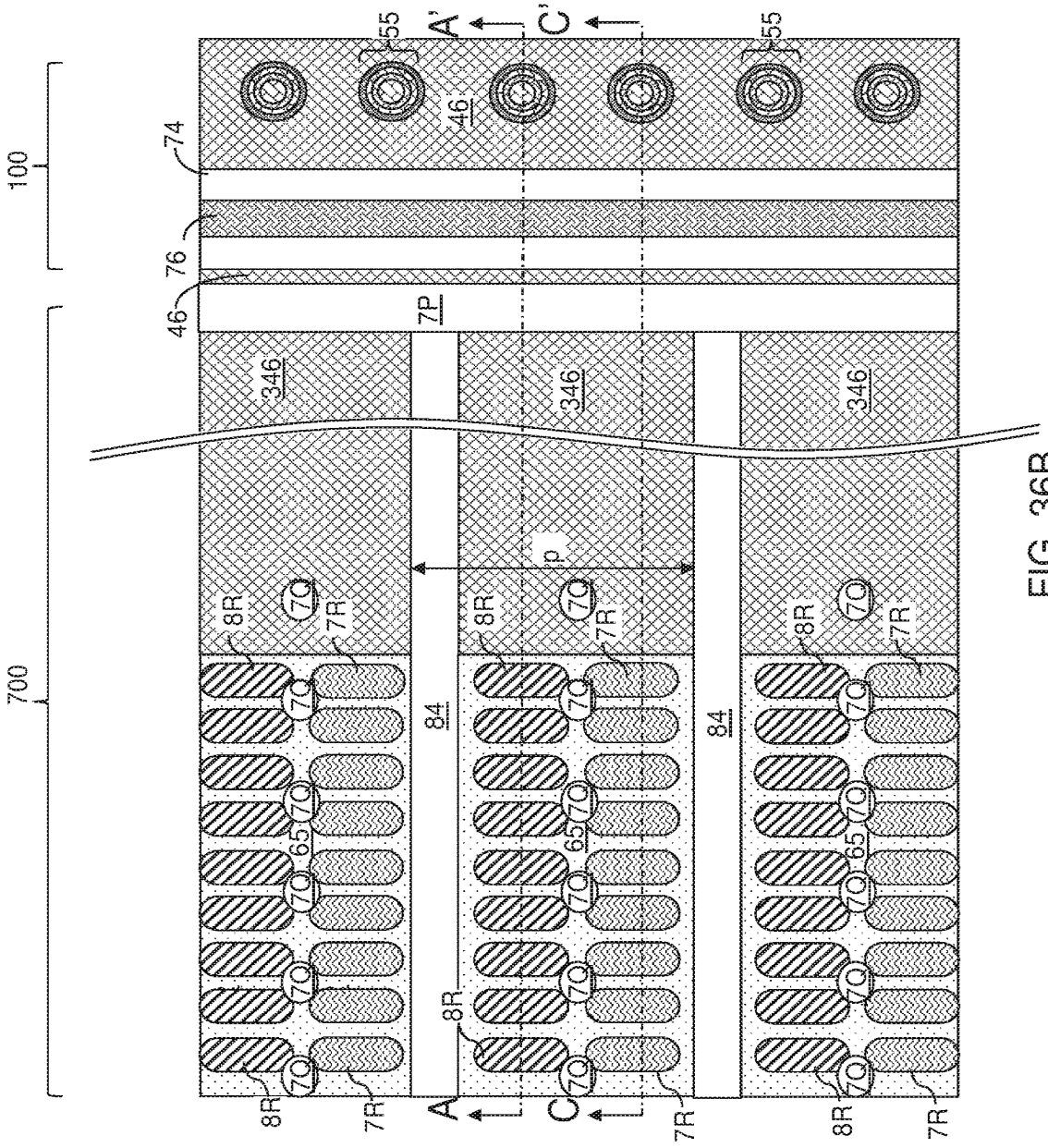


FIG. 36B

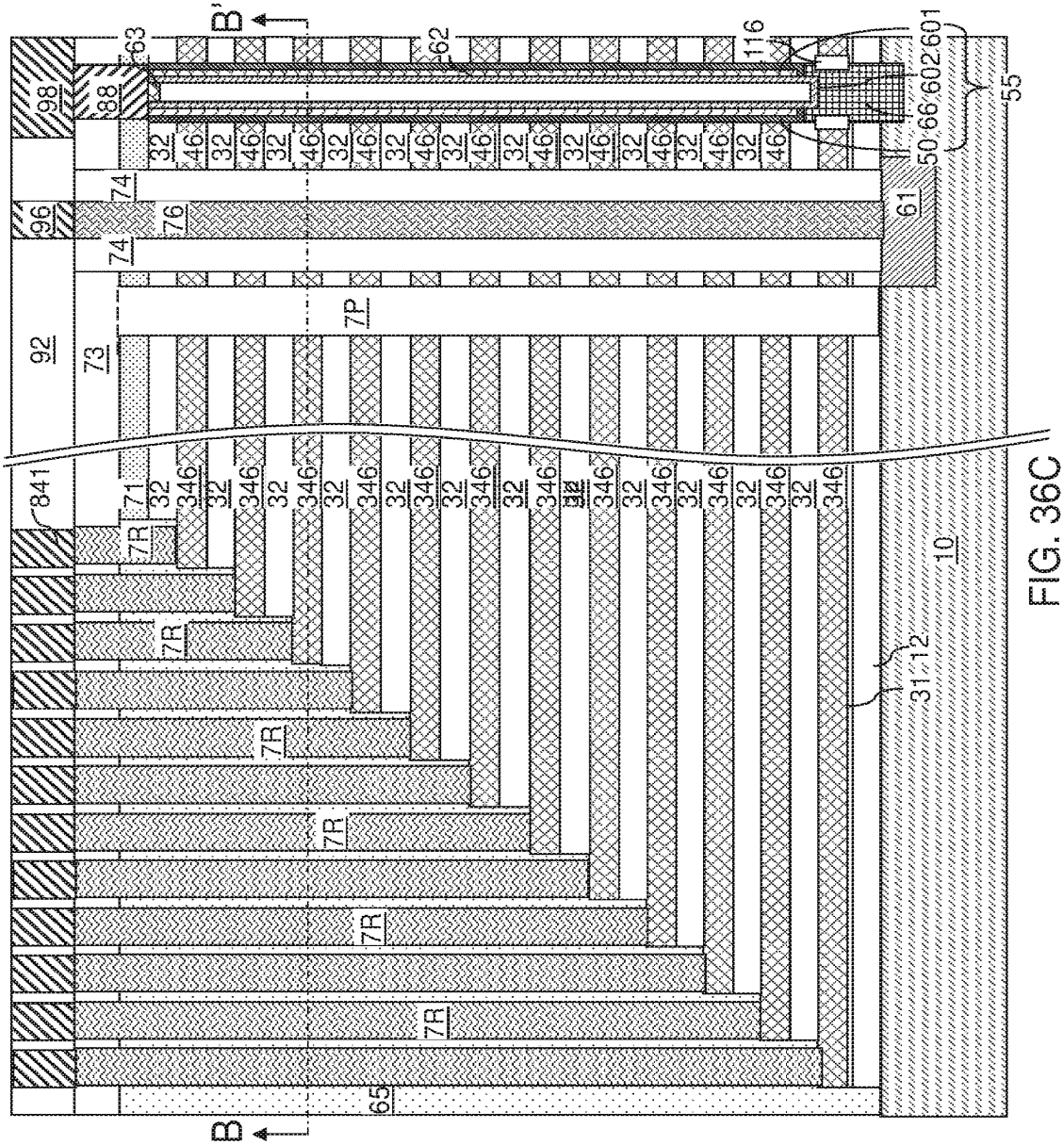

B'
B
63
62
116
55
50
66
602
601
61
98
88
96
74
76
92
73
7P
841
71
32
346
46
7R
65
31
12
10

FIG. 36C

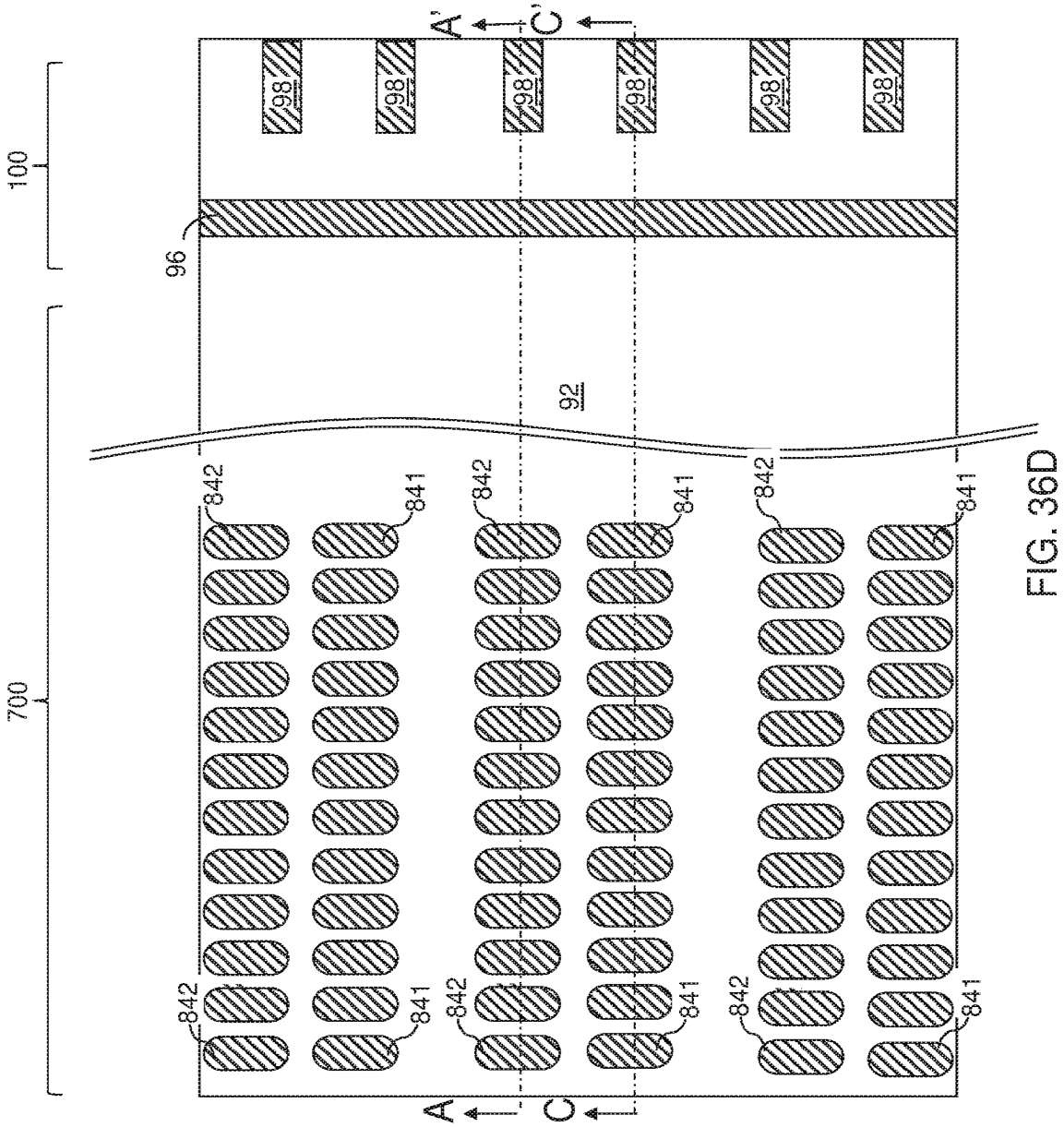


FIG. 36D

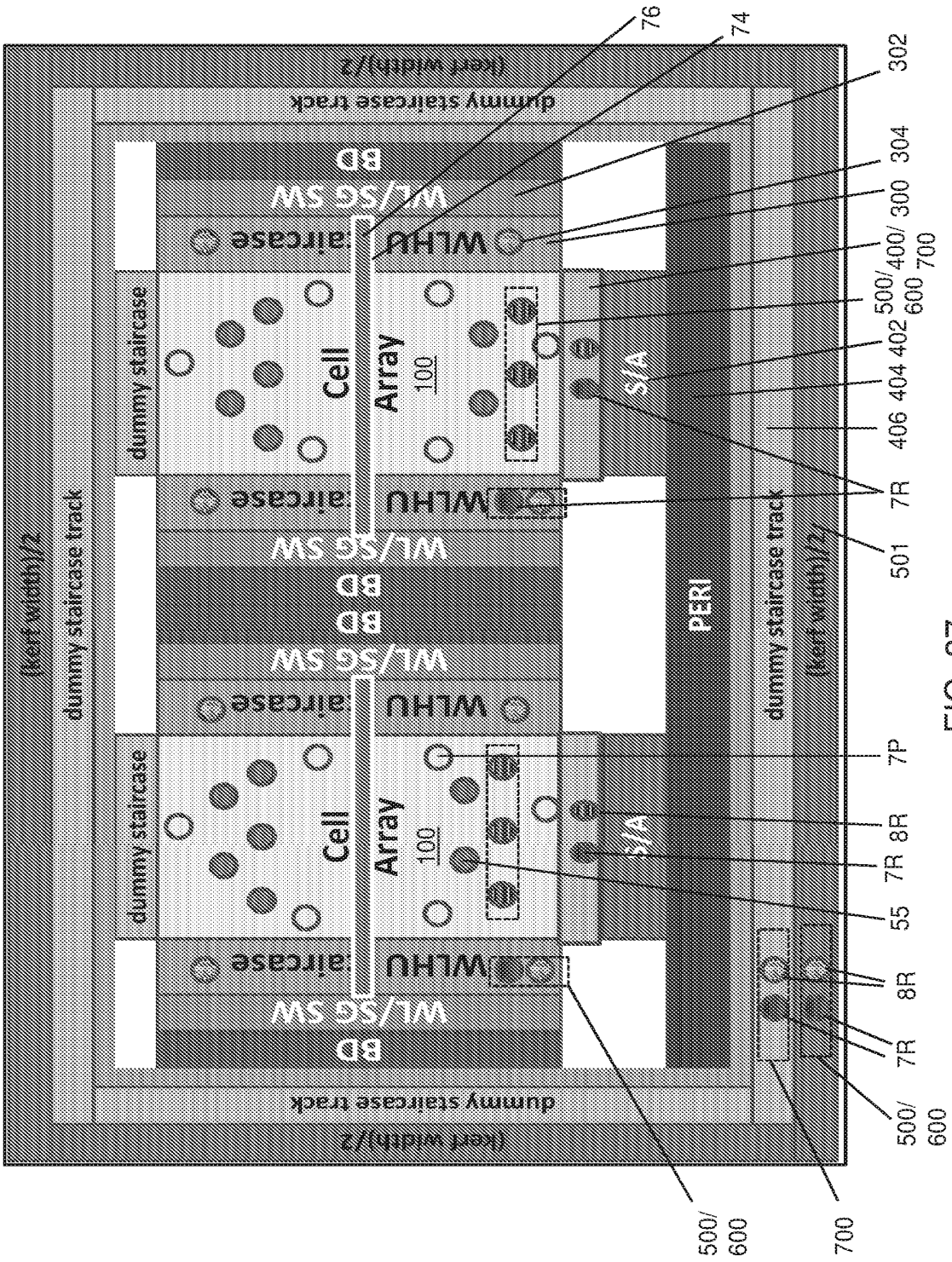


FIG. 37

Micron Ex. 1002, p. 363
Micron v. YMTC
IPR2024-00790