

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,
Patent Owner

Case No.: IPR2024-00790
U.S. Patent No. 10,868,031
Issue Date: December 15, 2020

Title: MULTIPLE-STACK THREE-DIMENSIONAL MEMORY DEVICE AND
FABRICATION METHOD THEREOF

**DECLARATION OF SANJAY BANERJEE, PH.D., IN SUPPORT OF
PETITION FOR *INTER PARTES* REVIEW OF
U.S. PATENT NO. 10,868,031**

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I, Sanjay Banerjee, hereby declare as follows:

I. INTRODUCTION

1. My name is Sanjay Banerjee. I have been retained on behalf of Petitioner Micron Technology, Inc. (“Micron”) to provide this Declaration concerning technical subject matter relevant to the *inter partes* review petition (“Petition”) concerning U.S. Patent No. 10,868,031 (Ex. 1001, the “’031 Patent”).

2. I have confined my analysis to the materials that were available when I prepared the Declaration. I reserve the right to supplement this Declaration in response to additional evidence that may come to light.

3. If requested, I am prepared to explain (in a deposition or at a trial before the Patent Trial and Appeal Board (the “Board”)) the technology disclosed and claimed in the ’031 Patent—including the state of the art in the relevant timeframe. Similarly, I am prepared to explain the technology disclosed in the Kim (Ex. 1005, U.S. Patent No. 10,381,369) and Tessariol (Ex. 1006, U.S. Patent Application Publ. No. 2019/0081061) references, and in any other prior art references cited herein. This may include, among other things, background information on 3D NAND technology.

4. I have been asked to consider whether Kim and Tessariol disclose or teach the features recited in the claims of the ’031 Patent. My opinions and the bases for my opinions are set forth below.

II. QUALIFICATIONS

5. I currently serve as the Cockrell Family Regents Chair Professor of Electrical and Computer Engineering and Director of the Microelectronics Research Center at the University of Texas at Austin (“UT”). Prior to this position, I was first an Assistant Professor (September 1987-August 1990) and later an Associate Professor (September 1990-August 1993) at UT, before being named a Professor in September 1993. Prior to starting my academic work at UT, I was a member of the technical staff at Texas Instruments (Corporate R&D) from the time I completed my doctoral studies in 1983 until August 1987. I worked on vertical 3D Dynamic Random Access Memory (DRAM) cells (*see* S. Banerjee and M. Bordelon, “A Model for the Trench Transistor,” *IEEE Trans. Elec. Dev.*, 34 (12), 2485-2493, December 1987).

6. In addition to my academic work at UT, I was also the Director of the South West Academy of Nanoelectronics, one of three centers created by the Semiconductor Research Corporation Nanoelectronics Research Initiative in 2006 to research and develop a replacement for conventional metal oxide semiconductor field effect transistors (“MOSFETs”) during the entire program.

7. I received my Ph.D. in Electrical Engineering from the University of Illinois in 1983. I also received an M.S. in Electrical Engineering from the

University of Illinois in 1981. I received a B. Tech. in Electronics from the Indian Institute of Technology at Kharagpur in 1979.

8. As described in my CV (Ex. 1004), I have more than 40 years of experience in the field of electrical engineering, including extensive experience in semiconductor development and fabrication including that of 3-Dimensional Dynamic Random Access Memory (“DRAM”) cells, MOSFETs, flash memory, and beyond-complementary metal-oxide-semiconductor (“CMOS”) transistors. My work in these fields has resulted in thirty-five United States patents related to methods of forming polysilicon and novel transistors, flash memory, and vertical DRAM cells. I have been elected a Fellow of the National Academy of Inventors.

9. Much of my research and experience has related to methods for MOSFET fabrication and design, including deposition of thin films by chemical vapor deposition (CVD), atomic layer deposition (ALD), physical vapor deposition (PVD), patterning using photolithography and etching using plasma-based Reactive Ion Etching (RIE) which are some of the processing techniques used to make 3D NAND flash. I have worked extensively on polysilicon thin film transistors similar to the ones used in the channel of NAND flash memory cells, high-k and other dielectrics used for charge storage, and for tunneling. A number of the sponsored research grants on which I have been a principal or coinvestigator have related to chemical deposition methods and/or ultra-shallow source/drain junction technology,

including “Transport in MOSFETs” (Motorola, August 1993-August 1994), “Ultra Shallow Junction Technology” (SEMATECH January 1994-December 1996), and “Vertical Si-Ge-C MOSFETS” (Semiconductor Research Corporation September 2000-August 2003). In addition, I am an author on over forty publications relating to flash memory cells, including vertical 3D memory that can be used in NAND flash (e.g., Sarkar J, Dey S, Shahrjerdi D, Banerjee SK, Vertical Flash memory cell with nanocrystal floating gate for ultradense integration and good retention IEEE ELECTRON DEVICE LETTERS 28 (5): 449-451 MAY 2007.) One of my papers on flash memory was given a Best Paper Award by the SRC.

10. I am a Fellow of the Institute of Electrical and Electronics Engineers (“IEEE”), the American Physical Society (“APS”), and the American Association for the Advancement of Science (“AAAS”). I have served on numerous professional and government committees in the electrical engineering field, including chairing multiple IEEE committees, meetings, and programs, serving on Morgan & Claypool’s editorial board, and serving as a member on the International Technology Roadmap for Semiconductors (“ITRS”).

11. I have taught courses in Semiconductor Physics, Solid State Electronic Devices, and Microelectronic and VLSI Device Fabrication at UT. In addition, I have delivered many courses to industry on Semiconductor Devices and Memory and Semiconductor Processing. I have taught courses that cover 3D memories, such

as 3D NAND (Ultra Large Scale Integration Techniques and Solid State Electronic Devices). As a principal investigator, I have been the advisor to over 80 Doctoral and Masters students.

12. I am the co-author of several books and invited book chapters covering the area of electronic and semiconductor devices, including: Dopant Diffusion, Solid State Electronic Devices (three editions), Silicon-germanium Devices, and Novel 3D CMOS. I have authored or co-authored more than 1,000 papers and presentations in the areas of semiconductor devices and electronics development over the course of my career.

13. I have been the recipient of fifty grants to fund my research from a variety of funding agencies including the National Science Foundation (“NSF”), DARPA, the Department of Energy, Semiconductor Research Corporation, the Department of Defense-Multidisciplinary University Research Initiative, and the Office of Naval Research.

14. I have received numerous awards for my work, including the NSF Presidential Young Investigator Award. The NSF Presidential Young Investigator

Award was¹ a highly competitive honor and grant bestowed annually upon recognized young academic leaders in science and engineering. I have received numerous other awards, including some the highest honors for semiconductor devices such as the Andrew Grove Award from IEEE, and the Semiconductor Industry Association/Semiconductor Research Corporation University Researcher Award, for my work in semiconductor memory and transistors, which are described in more detail in my CV (Ex. 1004).

III. COMPENSATION

15. I am being compensated for my work in this matter at an hourly rate of \$650.00 for consulting services. My compensation is not based on the outcome of this matter or on the substance of my opinions.

IV. MATERIALS CONSIDERED

16. In preparing this Declaration, I reviewed and considered the following materials, along with any other materials referenced in the body of my Declaration:

¹ The NSF Presidential Young Investigator Award was an award given out by the NSF until 1991, at which time it was replaced with the NSF Young Investigator Awards and Presidential Faculty Fellows Program.

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EXHIBIT NO.	DESCRIPTION
1001	U.S. Patent No. 10,868,031 to Liu et al. (“the ’031 Patent”)
1002	File History of U.S. Patent No. 10,868,031 (“the ’031 FH”)
1005	U.S. Patent No. 10,381,369 (“Kim”)
1006	U.S. Patent Application Publ. No. US2019/0081061 (“Tessariol”)
1007	Aritome, “NAND Flash Memory Technologies” (2016)
1008	Silvagni, “3D NAND Flash Based on Planar Cells,” Computers 2017
1009	Micheloni et al., “Inside Solid State Drives (SSDs)” (2 nd Ed. 2018)
1010	U.S. Patent No. 10,475,737 to Tang et al.
1011	U.S. Patent No. 10,559,583 to Park et al.
1012	U.S. Patent No. 9,768,186 to Shimabukuro et al.
1013	U.S. Patent No. 9,728,499 to Shimabukuro et al.
1014	U.S. Patent No. 9,299,641 to Sekar et al.
1015	U.S. Patent No. 11,244,725 to Goda et al.
1016	U.S. Patent No. 9,142,302 to Dong et al.
1020	Micheloni, “3D Flash Memories” (2016)
1021	Top Seiko Co., Ltd., Guide to Materials
1022	Sharpe, W.N., et al., “Mechanical Properties of MEMS Materials,” DARPA, AFRL-IF-RS-TR-2004-76 (March 2004)
1023	Wolf, S., et al., “Silicon Processing for the VLSI Era, Volume 1 – Process Technology, Chapter 15, Multilevel Interconnects for ULSI,” (2 nd Ed. 2000)

V. UNDERSTANDING OF THE GOVERNING LAW

17. I am not an attorney but have been instructed in and applied the law as described in this section.

A. Burden of Proof

18. I understand that the petitioner in an *inter partes* review bears the burden of establishing unpatentability by “a preponderance of the evidence.” I understand that to prove an assertion by “a preponderance of the evidence” the party with the burden of proof must demonstrate that it is more likely than not that the assertion is true.

B. Claim Construction

19. I understand that the first step in determining whether a patent claim would have been anticipated or obvious is to ascertain how a person of ordinary skill in the art (“POSITA”) would have understood the claim terms.

20. I have been instructed by counsel on the law regarding claim construction and patent claims, and I understand that a patent may include two types of claims: independent claims and dependent claims. An independent claim stands alone and includes only the limitations it recites. A dependent claim can depend from an independent claim, or it can further depend from another dependent claim. I understand that a dependent claim includes all the limitations that it recites, in addition to all the limitations recited in the claim(s) from which it depends.

21. It is my understanding that in proceedings before the USPTO, the claims of a patent are to be construed under what is referred to as the “*Phillips* standard.” I understand that this means that claim terms of a patent are given the ordinary and customary meaning they would have to a POSITA in view of the description provided in the patent itself and the patent’s file history.

22. I understand that to determine how a person of ordinary skill would understand a claim term, one should look to those sources available that show what a person of skill in the art would have understood the disputed claim language to mean. I understand that, in construing a claim term, one looks primarily to the intrinsic patent evidence, including the words of the claims themselves, the remainder of the patent specification, and the patent’s prosecution history. I understand that extrinsic evidence, which is evidence external to the patent and the prosecution history, may also be useful in interpreting patent claims when the intrinsic evidence itself is insufficient.

23. I understand that words or terms should be given their ordinary and accepted meaning unless it clearly appears that the inventors were using them to mean something else. In making this determination, the claims, the remainder of the patent, and the prosecution history are of paramount importance. Additionally, the patent and its prosecution history must be consulted to confirm whether the patentee

has acted as its own lexicographer (*i.e.*, provided its own special meaning to any claim terms) or intentionally disclaimed, disavowed, or surrendered any claim scope.

24. I further understand that in proceedings before the PTAB, claim terms need only be construed to the extent necessary to resolve any controversy that may arise.

25. In comparing the claims of the Challenged Patent to the prior art, I have considered the '031 Patent and its file history in light of the understanding of a POSITA at the time of the alleged invention. I address further how a POSITA would have understood the claims of the alleged invention in §X below.

C. Obviousness

26. I have been further instructed and understand that a patent claim is unpatentable and invalid as obvious if the subject matter of the claim as a whole would have been obvious under 35 U.S.C. §103 to a person of ordinary skill in the art of the claimed subject matter as of the time of the invention at issue. I understand that when assessing the obviousness of claimed subject matter, the following factors are evaluated: (1) the scope and content of the prior art; (2) the difference or differences between each claim of the patent and the prior art; and (3) the level of ordinary skill in the art at the time the patent was filed. I also understand that the Board considers certain objective factors if they are present, generally referred to as

“secondary considerations” or “objective indicia” of nonobviousness, as further discussed below in this section.

27. I have been informed that there are two ways to determine whether prior art is analogous and thus can be considered prior art: (1) whether the art is from the same field of endeavor, regardless of the problem addressed, and (2) if the reference is not within the field of the patentee’s endeavor, whether the reference still is reasonably pertinent to the particular problem with which the patent is concerned. I have also been informed that the field of endeavor of a patent is not limited to the specific point of novelty, the narrowest possible conception of the field, or the particular focus within a given field. I have also been informed that a reference is reasonably pertinent if, even though it may be in a different field from that of the patentee’s endeavor, it is one which, because of the matter with which it deals, logically would have commended itself to a patentee’s attention in considering his or her problem.

28. I understand that claimed subject matter may be obvious in view of a single reference or a combination of more than one item of prior art. I understand, however, that it is not enough to show simply that all the limitations of the claimed subject matter are spread throughout the prior art. Instead, for claimed subject matter to be obvious over multiple references, there generally must have been some reason

or motivation for one of ordinary skill in the art to combine the teachings of the prior art references to arrive at the claimed subject matter.

29. I have been informed that, in seeking to determine whether an invention that is a combination of known elements would have been obvious to a person of ordinary skill in the art at the time of the invention, one must consider the reference(s) in their entirety to ascertain whether the disclosures in those references render the combination obvious to such a person.

30. I have been informed and understand that, while not required, the prior art references themselves may provide a teaching, suggestion, motivation, or reason to combine, but that other times the motivation linking two or more prior art references is common sense to a POSITA at the time of the invention.

31. I understand that a particular combination may be proven obvious merely by showing that it was obvious to try the combination. I have been informed that, if a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill. I have further been informed and understand that a POSITA combines the teachings of the prior art references and does not necessarily combine the embodiments of those teachings physically.

32. I further understand that an obviousness analysis recognizes that market demand, rather than scientific literature, often drives innovation, and that a motivation to combine references also may be supplied by the direction of the marketplace. For example, when there is a design need or market pressure to solve a problem and there are a finite number of identified, predictable solutions, a person of ordinary skill has good reason to pursue the known options within his or her technical grasp because the result is likely the product not of innovation but of ordinary skill and common sense.

33. I have been informed that the combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results. Thus, where all of the elements of a claim are used in substantially the same manner in devices in the same field of endeavor, the claim is likely obvious.

34. Additionally, I understand that a patent is likely to be invalid for obviousness if a person of ordinary skill can implement a predictable variation or if there existed at the time of the invention a known problem for which there was an obvious solution encompassed by the patent's claims. Therefore, when a work is available in one field of endeavor, design incentives and other market forces can prompt variations of it, either in the same field or a different one.

35. I further understand that combining embodiments related to each other in a single prior art reference would not ordinarily require a leap of inventiveness.

36. I also understand that one of ordinary skill in the art must have had a reasonable expectation of success when combining references for claimed subject matter to be obvious.

37. I have been informed and I understand that factors referred to as “objective indicia of non-obviousness” or “secondary considerations” are also to be considered when assessing obviousness when such evidence is available. I understand that these factors can include: (1) commercial success; (2) long-felt but unresolved needs; (3) copying of the invention by others in the field; (4) initial expressions of disbelief by experts in the field; (5) failure of others to solve the problem the claimed subject matter solved; and (6) unexpected results.

38. I also understand that evidence of objective indicia of nonobviousness must be commensurate in scope with the claimed subject matter. I further understand that there must be a relationship, sometimes referred to as a “nexus,” between any such secondary indicia and the claimed invention. I also have been informed that even when they are present, secondary considerations may be unable to overcome primary evidence of obviousness (*e.g.*, motivation to combine with predictable results) that is sufficiently strong. I have also been informed that near-

simultaneous invention by others can be evidence that a claimed invention is obvious.

39. Finally, I have been informed that one cannot use hindsight to determine that an invention was obvious.

40. I provide my opinions in this Declaration based on the guidelines set forth above.

VI. LEVEL OF SKILL IN THE ART

41. I have been informed and understand that the level of ordinary skill in the relevant art at the time of the invention is relevant to inquiries such as the meaning of claim terms, the meaning of disclosures found in the prior art, and the reasons a POSITA may have for combining or modifying references.

42. I have been informed and understand that factors that may be considered in determining the level of ordinary skill include: (1) the education of the inventor; (2) the type of problems encountered in the art; (3) prior art solutions to those problems; (4) rapidity with which innovations are made; (5) sophistication of the technology; and (6) education level of active workers in the relevant field. I have been further informed and understand that a POSITA is also a person of ordinary creativity.

43. A POSITA in the field of the '031 Patent would have had a bachelor of science degree in electrical engineering or a similar discipline, along with 2-3 years

of professional experience working with (*e.g.*, researching, designing, or teaching) monolithic 3D structures and NAND flash memory devices, or an equivalent level of skill, knowledge, and experience (*e.g.*, an advanced degree may replace some of the professional experience). This POSITA would have been aware of and generally knowledgeable about semiconductor manufacturing and 3D NAND's structure, its component parts, how it operates, and how it is controlled.

44. In view of my educational background and work experience, I am a person of more than the ordinary level of skill in the art of the '031 Patent and was so by July 27, 2018. In forming my opinions, I have drawn on my academic background and professional experiences. My opinions herein, however, were formed taking into account the perspective of a POSITA.

VII. THE '031 PATENT'S EFFECTIVE FILING DATE

45. I understand that the application leading to the '031 Patent was filed on September 10, 2018. I further understand that the patent claims priority to a an earlier-filed PCT publication No. PCT/CN2018/097432, filed on July 27, 2018.

46. For purposes of this Declaration, I have been instructed to use July 27, 2018, as the priority date of the '031 Patent. My opinions in this Declaration were formed from the perspective of a POSITA as of July 27, 2018, including both the knowledge of a POSITA at that time as well as how a POSITA would have understood the prior art.

VIII. TECHNOLOGY OVERVIEW

A. 3D NAND Basics

47. The '031 Patent and the prior art discussed in this Petition relate to three-dimensional (3D) memory devices, *e.g.*, 3D NAND memory devices. The basic building block of the non-volatile semiconductor memory is the memory cell, a structure that stores one or more bits of data. These memory cells are based on the Metal Oxide Semiconductor Field Effect Transistor, or MOSFET. This overview is for N-channel MOSFET-based 3D NAND flash devices. When the proper voltage conditions are applied, (1) electrons are attracted to the surface of the semiconductor device in the channel region forming a conductive path between source and drain and (2) electrons flow through the channel from the source to the drain when a drain voltage is applied. The flow of electrons through the channel is electrically controlled by the gate. The voltage on the gate needed to cause significant conduction in the channel is known as the threshold voltage.

48. A traditional type of non-volatile semiconductor memory can store information using a MOSFET that includes an extra “floating” gate. Floating gates were historically made out of conductive electrodes that were not electrically connected to the external terminals such as source, drain and control gate of the memory cell. But charges can also be stored in charge traps in the gate dielectric, where these act as the “floating gates.” The shapes of the energy band diagrams in

the two cases are somewhat different, but the overall charge storage mechanisms have similarities. I will discuss charge-trap memories in more detail shortly. The floating gate stores the charge that is used to represent the data. A floating gate is surrounded by electrical insulators on all sides - it electrically “floats” in the insulation - and therefore has no direct electrical contact to the rest of the device. Instead, the floating gate is capacitively coupled to the various electrodes. Electrically Erasable Programmable Read Only Memory (EEPROM) can both store and *erase* data electrically. In EEPROM devices, the insulator, or dielectric, between the floating gate and the channel is known as the tunnel dielectric, while the dielectric between the floating gate and the control gate is known as the control dielectric. Flash memory is a type of EEPROM where a large number of memory cells can be erased very quickly - that is, in a “flash.” Flash memory cells are not erased individually like other EEPROMs, but rather in a group called a “block.”

49. The two most common memory cell architectures used for flash EEPROMs are NOR and NAND. The conditions that must be applied to a memory cell in a NOR or NAND architecture in order to program, erase or read the cell are discussed below. Conditions for programming, reading, and erasing memory cells in the various cell architectures were known to those of ordinary skill in the field at the time the '031 Patent was filed. The logic value associated with the “erased” and “programmed” states of a memory cell is a matter of convention. In some sources,

the logic value “1” denotes the erased state and “0” denotes the programmed state - in others, the reverse is true. Either of these conventions is appropriate. For this background discussion of NAND architecture, I will use the convention where “1” represents the logic value of the erased state and “0” represents the logic value of the programmed state. In the NOR architecture, a single memory cell exists at each intersection of a bit line (drain) and a word line (control gate). In the NAND memory cell architecture, groups of cells are connected together in series between source and drain (*i.e.*, the bit line). This group of cells, is known as a NAND string. The control gates of these cells are the word lines.

50. One generally programs the cells using tunneling of electrons from the substrate into the floating gate by applying a high positive voltage to the control gate. One gets Fowler-Nordheim tunneling through triangular barriers for thicker tunnel dielectrics, or direct tunneling through trapezoidal barriers for thinner tunneling layers. This high voltage applied to the control gate increases the electric field across the tunnel dielectric and narrows the triangular potential barrier for Fowler Nordheim tunneling, thereby making it easier for electrons to quantum mechanically tunnel through the dielectric. There is also an increase of tunneling current for direct tunneling. These tunneled electrons are stored (trapped) on the floating gate. This results in the high threshold voltage state, generally known as the “0” state. One also erases the NAND cell by tunneling, by either applying a high positive voltage

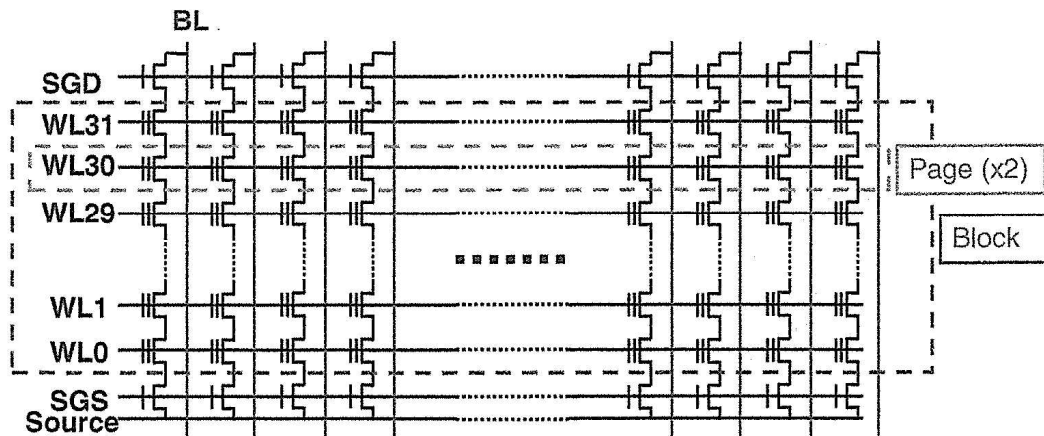
to the substrate electrode, or applying a negative voltage to the control gate. This increases the electric field across the tunnel dielectric, reduces the barrier width and thus increases the probability of tunneling (*i.e.*, removing charge from the floating gate). This results in the low threshold voltage state, generally known as the “1” state. For metallic or semiconducting floating gates, the electrons are trapped at the same energy at the Fermi level, or bottom of the conduction band, respectively, and the carriers pile up next to the tunnel dielectric interface. This also makes it necessary to pattern the conducting floating gate to isolate them between adjacent cells. On the other hand, if the charges are trapped in a charge trap layer, there is no need to pattern and etch the layer because the traps states are already isolated from each other. In this case, the electrons can be trapped at multiple trap energy levels and slightly different distances from the tunnel dielectric and channel depending on the spatial distribution of the traps, making the threshold voltage distribution wider than for conducting floating gates. The trap potentials are also different. Instead of a trapezoidal well, traps have a Coulombic well that is subject to Poole-Frenkel barrier lowering upon application of a field.

51. NAND cells are read by applying a high voltage (V_{PASS}) to all the word lines in the NAND string except the cell that is being read. This ensures that all other cells in the string will conduct current. The conduction of the cell being read will depend on whether it is in the “0” or “1” state. This conduction can be

determined through the use of a sense amplifier, which may sense either voltage or current on the bit line.

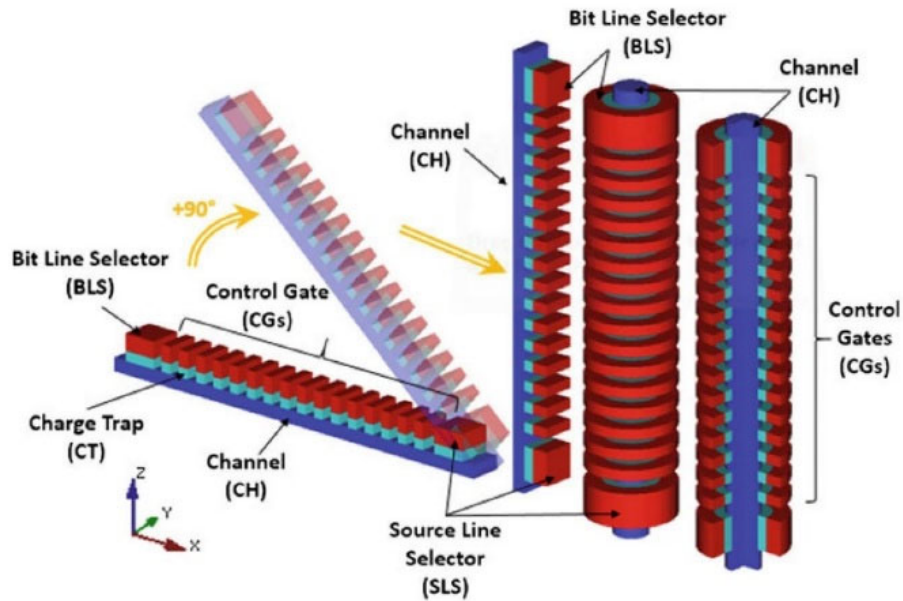
52. NAND memories are more compact than NOR memories because NAND cells are connected in a string. Adjacent NOR cells need to be isolated from each other, which is accomplished using isolation regions which consume “silicon real estate.” For NAND architectures, individual cells in a string do not need such isolation -- one only needs to isolate one string from the adjacent strings. This consumes less surface space for isolation and makes the NAND architectures more attractive for mass storage applications. Ex. 1007, 38.

53. In the early days, NAND devices were formed as two-dimensional arrays of cells on a substrate surface (*viz.*, only in the horizontal X- and Y-directions). Ex. 1007, 58. The example below from a NAND flash memory textbook is a schematic showing a 2D NAND memory architecture where cells grouped into “page[s]” and “block[s],” which are only fabricated in the X- and Y-directions.

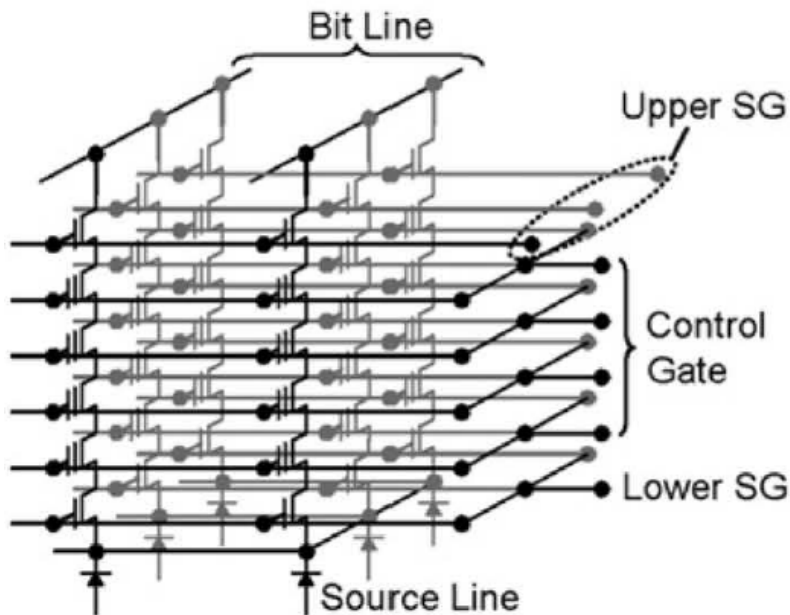


Ex. 1007, 40.

54. “[T]o further scale down the memory cell size” and achieve higher memory densities, “three-dimensional (3D) NAND flash cells” were developed. Ex. 1007, 292. “Conceptually, a modern 3D NAND structure could be conceived by starting from the 2D NAND string building block” and “turning the 2D NAND string upside,” “resulting” in a “3D structure” with a “vertical channel.” Ex. 1008, 3. The evolution of NAND architectures from 2D to 3D led to further savings of silicon real estate. The image below illustrates the concept of rotating a NAND memory string on its side (*i.e.*, placing it in the vertical dimension on the z-axis).



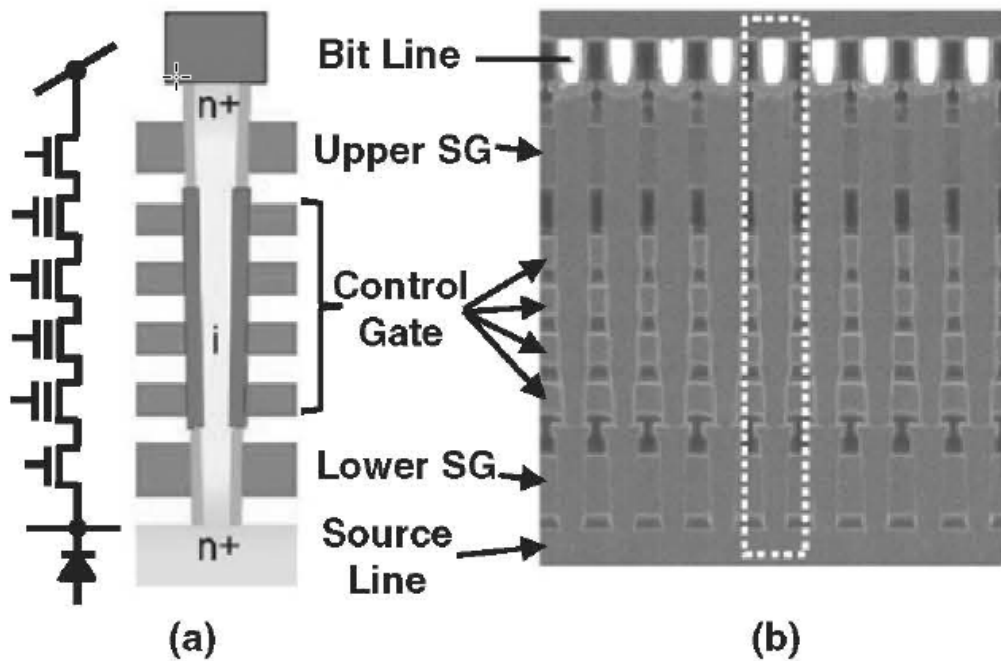
Ex. 1009, 122. The vertical memory cell strings can then be repeated numerous times to form a three-dimensional memory array:



Ex. 1007, 296. This is structurally different than simply stacking various 2D NAND memory arrays on top of one another, because the memory channels/strings in a 3D

NAND run in the vertical (not horizontal) direction which has important implications for semiconductor fabrication of the 3D NAND structures.

55. 3D NAND memory devices typically include alternating horizontal layers of conductors and dielectric in a “[s]tack.” Ex. 1007, 294. A vertically aligned “through-hole[]” channel (also known as a channel structure) “filled by memory film ... and channel poly-Si” passes through the layers to form the vertical memory cell strings. *Id.*, 295. Control gates for the memory cells are formed where the wordlines (formed by the horizontal conduction layers) intersect the vertical memory strings and act as a control gate. *Id.*, 295-296. A particular vertical memory cell “string is selected by a bit line and an upper select gate (upper SG).” *Id.*, 295-296. The lowest layer is a “select gate (lower SG)” that allows the strings to connect to a lower “common source.” *Id.*, 295, 297. An example 3D NAND vertical memory cell string is shown below.



Id., 296.

56. It was well-known to POSITAs to use so-called “staircase structures” to provide electrical access points for the various wordlines. For example, as illustrated below, each subsequent wordline (40) progressively extends further in the horizontal X-direction to provide landing pads for the contacts 60.



Ex. 1010 (U.S. Pat. No. 10,475,737), Fig. 13, 4:56-64, 8:45-56.

57. To manufacture such 3D NAND devices, it was known in the art to utilize sacrificial layers. Rather than simply depositing alternating layers of dielectric and conductor, the “sacrificial” approach entailed first creating an alternating stack of dielectric layers and interim “sacrificial layers,” which are subsequently removed and replaced with conductive control gate layers. Ex. 1010, 4:25-55. Due to the increased number of layers in 3D NAND relative to 2D NAND, there was a greater need for vertical stability, and it was known to use supporting pillars that extend through the stack to provide mechanical support during the process of replacing the sacrificial gate layers with conductive gate layers. *Id.*, 7:44-8:3.

B. Semiconductor Etching

58. Fabrication of semiconductor chips, including 3D NAND flash, is based on deposition of various types of thin films such as semiconductors, insulators and conductors (metals), patterning them using photolithography, and etching the layers using wet chemical etching or dry plasma-based etching. A plasma involves electrically exciting a mixture of gases and fragmenting the molecules into highly reactive species called radicals, electrons, and positive ions.

59. There are different types of plasma etching, including commonly used Reactive Ion Etching (RIE). Two of the important metrics of etch processes are the *selectivity* of the etch and the *anisotropy* of the etch. Selectivity refers to the ability of the process to etch one material preferentially (*i.e.* higher rate) than an adjoining material/layer. Anisotropy of an etch is the ability of the etch process to have a higher etch rate in the vertical direction compared to the lateral direction. It ranges from 0, which is a completely isotropic etch, to 1 which is perfectly anisotropic, with completely vertical sidewalls.

60. Practical RIE processes have anisotropy values close to but less than 1. Unfortunately, there is often a tradeoff between the two. Wet etches are based on chemical reactions with different materials and are often very selective, but not anisotropic. They etch as fast vertically as they do laterally, making them isotropic. (Some plasma-based etches can also be quite selective and isotropic.) In the '031

Patent, a dielectric stack of two different insulators is first deposited by CVD, and some of the layers (the sacrificial layers) are selectively etched out. These cavities are subsequently filled with a conductor (metal) by CVD, which can fill these cavities isotropically, unlike PVD. This forms the different wordlines, or control gates, of the memory cells.

61. Most plasma-based etches, on the other hand, depend both on chemical reactions with reactive radicals which tend to be selective, in combination with physical bombardment by the ions perpendicular to the wafer surface, which provides a less selective, but more anisotropic etch. RIE is a popular plasma-based etch process which provides a good compromise between selectivity and anisotropy, and is often used to etch holes with high aspect ratio. Aspect ratio refers to the geometry of the structure in terms of depth over lateral dimensions.

62. In the '031 Patent such processes are used to etch the holes for the memory cells and the support pillars. However, even RIE is not perfectly anisotropic. Hence, the holes tend to have a conical, rather than cylindrical shape, causing the bottom of the hole to have a smaller cross section than the top. This is what causes the mis-alignment of the hole sidewalls in the two dielectric stacks in the '031 Patent. A 2-step etch process, as opposed to a 1-step process, etches the channel holes in the lower stack first, and fills the holes with a sacrificial material that can be subsequently etched off selectively. The second stack is then deposited,

and the channel holes are etched in it, leading to mis-aligned channel hole sidewalls where the larger top-cross section of the lower channel hole meets the smaller bottom-cross section of the upper channel hole. The pillar holes are etched in a 1-step process through both of the stacks, leading to aligned pillar sidewalls. Sometimes an Etch Stop Layer (ESL) can be inserted between the two stacks to facilitate a two-step etch, as in Kim. The ESL will have a much lower etch rate compared to the etch rate of the other layers to provide a self-limiting etch. Subsequently, a different etch chemistry is used to remove the ESL.

IX. THE '031 PATENT

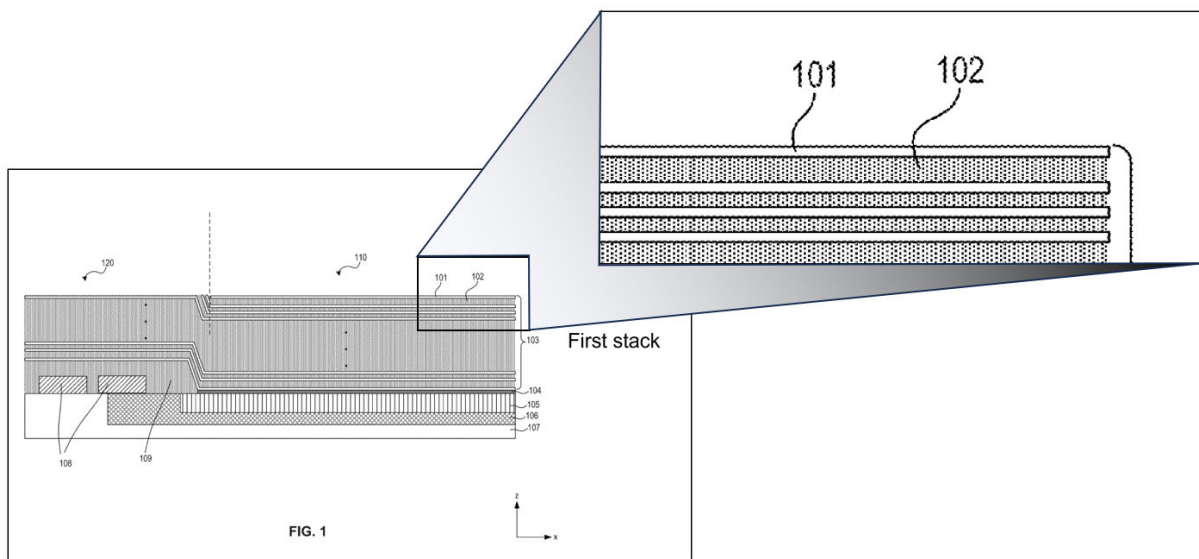
A. Summary of the Patent

63. The '031 Patent is titled “Multiple-Stack Three-Dimensional Memory Device and Fabrication Method Thereof.” The '031 Patent contains one independent claim and 5 dependent claims.

64. Consistent with its title, the '031 Patent relates to 3D memory devices, *e.g.*, 3D NAND memory. Ex. 1001, 1:15-38. The '031 Patent admits that such 3D NAND devices were known when the priority application for the '031 Patent was filed. *Id.* The specification explains that a “multiple-stack (or multiple-level) 3D NAND memory device often includes multiple stacks of word lines arranged along the direction perpendicular to the substrate.” *Id.* The specification further explains that “[c]hannel holes are respectively formed in each stack for the subsequent

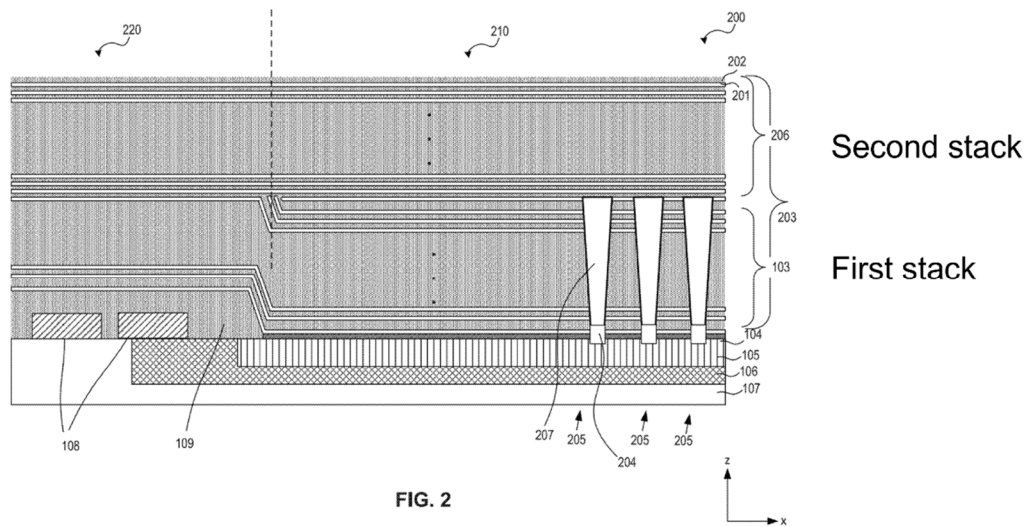
formation of semiconductor channels through the multiple-stack 3D memory device.” *Id.*

65. The '031 Patent illustrates a first stack (labelled 103) comprised of alternating dielectric (102) and sacrificial (101) layers as shown in Fig. 1 below. *See* Ex. 1001, 10:30-49.



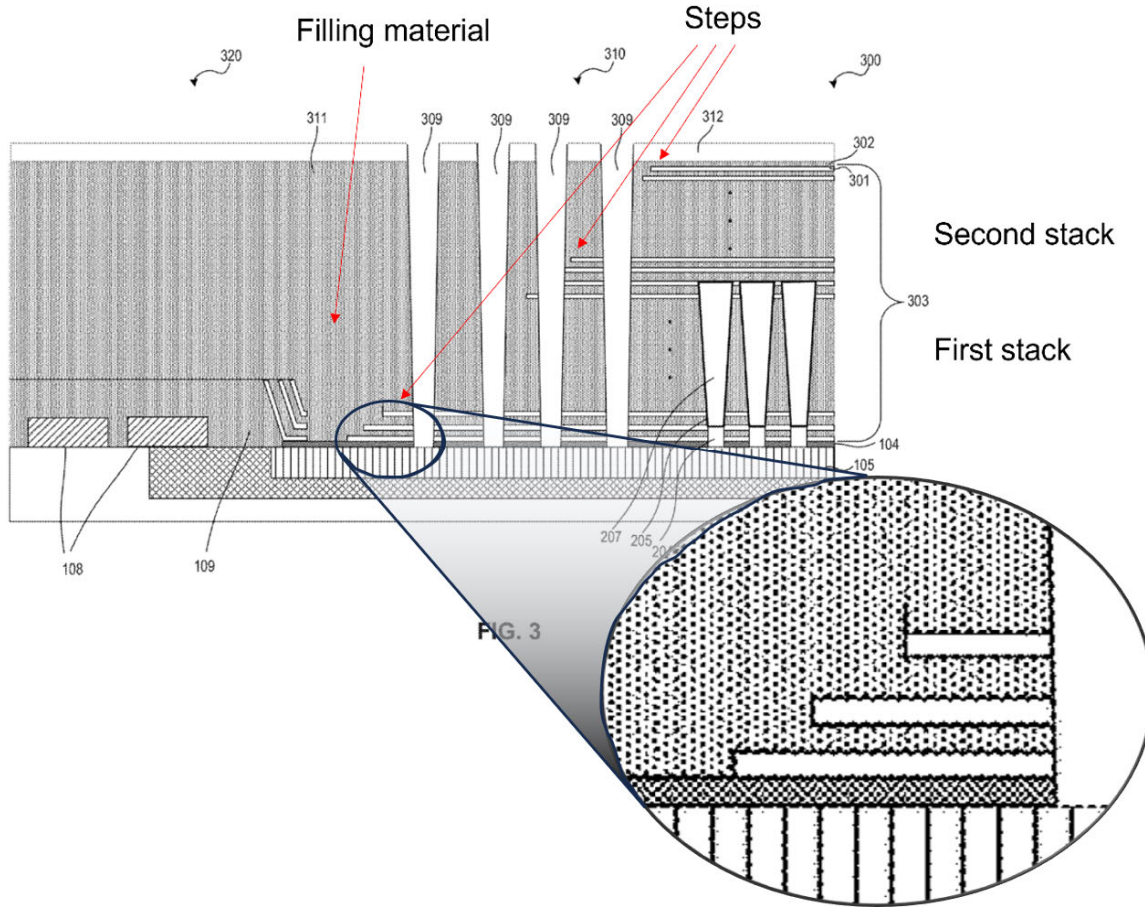
Id., Fig. 1 (annotated), 11:6-34.

66. The '031 Patent further discloses forming a second stack (labelled 206) comprised of alternating dielectric (202) and sacrificial (201) layers located above the first stack, thereby creating a multi-stack structure as shown in Fig. 2 below. *See* Ex. 1001, 12:65-13:10.



Id., Fig. 2 (annotated), 11:44-60, 12:65-13:10.

67. The '031 specification describes “staircase structure[s]” as “having stepped surfaces.” Ex. 1001, 9:39-52. This is unsurprising given the “staircase” namesake from which the term derives. The '031 specification explains that an etching process (which has long-been known and used in semiconductor manufacturing processes) can be used to create the multi-stack structure to form the steps for a staircase portion of each stack (*viz.*, “staircase structure 303,” also known as “multiple-stack staircase structure 303” or “two-stack staircase structure 303”) as shown in annotated Fig. 3 below:

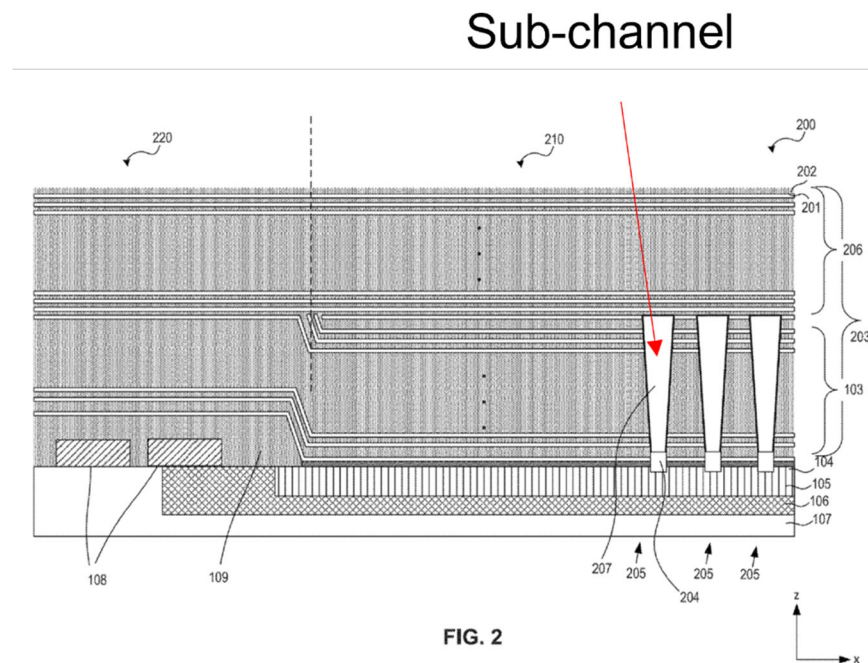


Id., Fig. 3 (annotated), 11:44-60, 12:65-13:64. As can be seen above, there is a staircase region in each stack. After the staircase has been formed, the '031 Patent describes depositing a filling material (311) (*e.g.*, dielectric) to fill the empty space that resulted from creating the steps. *Id.*, 13:36-48.

68. The '031 Patent states that in multi-stack structures, “the fabrication processes of semiconductor channels and supporting pillars are time-consuming and costly.” Ex. 1001, 1:37-38. In view of these purported problems, the '031 Patent goes on to describe creating the channel structures with a two-step etch process and

creating supporting pillars with a one-step etch process, as described in more detail below.

69. To begin, as illustrated below, the '031 Patent creates so-called “sub-channel” structures (labelled 207) that require etching the first stack (103) before depositing the second stack (206) on top the first stack:



Ex. 1001, Fig. 2 (annotated), 11:44-60.

70. Following formation of the second stack (206), the '031 Patent discloses that another etch process (*viz.*, a second etch) is performed to form a sub-channel hole in the second stack on top of where the first sub-channel structure is located, as shown in annotated Fig. 4 below. Subsequent processing fills the sub-channel to result in the creation of sub-channels that, collectively, extend vertically

through both the first and second stacks, as shown in annotated Fig. 4 below. The '031 Patent teaches that employing a “[m]ultiple-channel structure can further increase memory cell density of the 3D memory device.” Ex. 1001, 18:37-38.

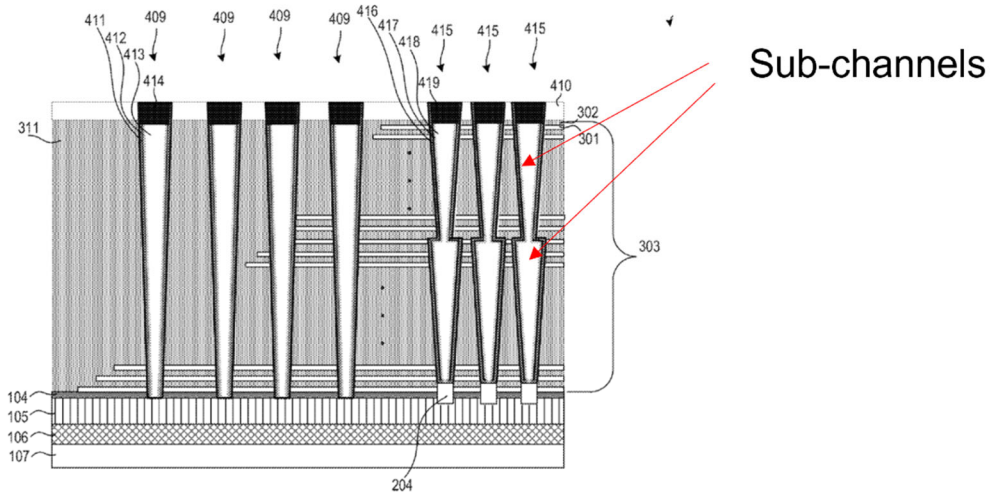


FIG. 4

Id., Fig. 4 (annotated), 14:35-44.

71. Unlike the two-etch processing steps used to form the channels, the '031 Patent teaches forming pillar structures using just a single etch process that is performed after the completion of both stacks, as shown in the annotated figures below.

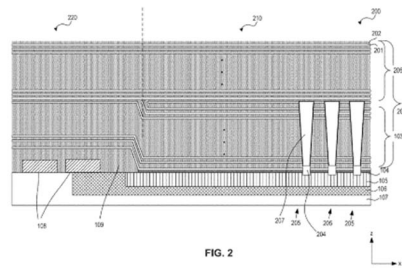


FIG. 2

Pillar holes

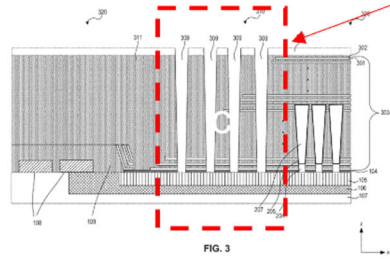
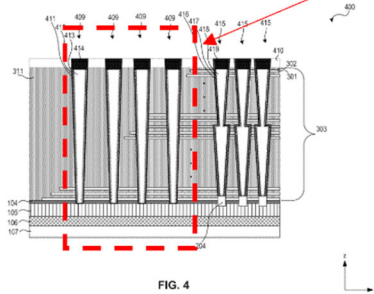


FIG. 3

Pillars



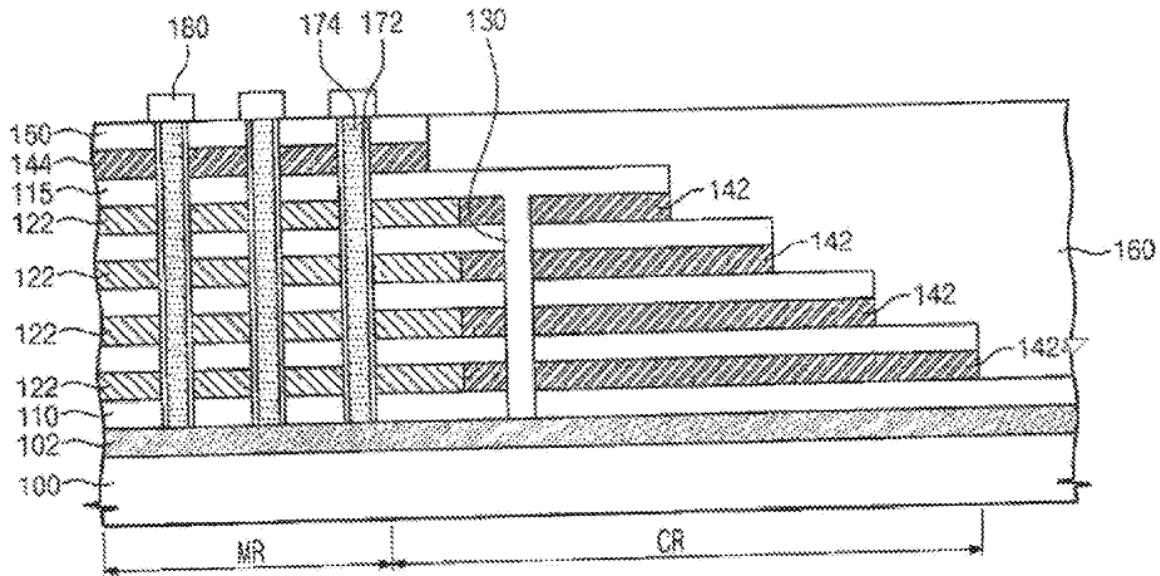
the bottom of each stack. Ex. 1001, 8:32-53. The '031 Patent explains that “unaligned surfaces can refer to the inconsistent hole dimensions caused by etching holes with high aspect-ratio (e.g., greater than 4).” *Id.*, 8:41-43. In contrast, the '031 Patent describes the sidewalls of the supporting pillars as being “aligned” because the pillars are formed using a single etch. *Id.*, 2:45-50.

B. Prosecution History of the '031 Patent

73. The substantive prosecution of the '031 Patent was quite short. The Examiner issued a restriction requirement on September 4, 2019. Ex. 1002, 662. The first (and only) prior art rejection was issued in an Office Action dated January 7, 2020. *Id.*, 824. In that Office Action, the Examiner made a single anticipation rejection based on Chae (US Publ. No. 2010/0133599), but made no obviousness rejections. *Id.*, 826-829.

74. In an Office Action Response dated April 2, 2020, the Applicant traversed the anticipation rejection on the basis that Chae did not disclose “unaligned sidewall surfaces” for the claimed “semiconductor channel.” Ex. 1002, 851-853. In particular, the Applicant argued that the channels in Chae on which the Examiner relied were “smooth and straight” (as shown in Chae Fig. 13 below) and thus are not unaligned as the claims require. *Id.*, 853.

Fig. 13G



Id., 852 (reproducing Chae Fig. 13G).

75. The Examiner then allowed the claims on July 1, 2020, specifically crediting the Applicant's argument about Chae's failure to disclose unaligned channel sidewalls. Ex. 1002, 864.

X. CLAIM CONSTRUCTION

76. I am not a legal expert or an attorney and offer no opinions on the law. I understand that claim construction is a matter of law. As discussed in §V.B above, I have been informed by counsel of the legal standards that apply to claim construction in an *inter partes* review and I have applied them in forming my opinions.

77. In my opinion, for purposes of this proceeding, the terms of the '031 Patent's claims do not require further construction and should be afforded their plain and ordinary meaning. Should Patent Owner advance any different constructions, I reserve the right to address those in a reply declaration.

XI. SUMMARY OF OPINIONS

78. I have reviewed and analyzed the prior art references and materials in §XIII-XVI.

79. For the reasons I explain in greater detail below, it is my opinion that before the earliest priority date of the '031 Patent (July 27, 2018), a POSITA would have considered claims 1-5 of the '031 Patent to be unpatentable as obvious based on the specific ground summarized in the table below.

Ground	Claim(s)	Prior Art Asserted
1	1-4	Obvious under §103 based on U.S. Pat. No. 10,381,369 (Ex. 1005, "Kim") ²
2	1-2 and 4-5	Obvious under §103 based on U.S. Pat. App. Pub. No. 2019/0081061 (Ex. 1006, "Tessariol") ³
3	4	Obvious under §103 based on Kim in view of Tessariol

² Kim was filed December 14, 2017. I have been informed that it qualifies as prior art under at least AIA §102(a)(2).

³ Tessariol was filed September 14, 2017. I have been informed that it qualifies as prior art under at least AIA §102(a)(2).

Ground	Claim(s)	Prior Art Asserted
4	1-2 and 4-5	Obvious under §103 based on Tessariol in view of Kim

XII. OVERVIEW OF THE PRIOR ART

80. Next, I provide an overview of the main prior art references that I discuss throughout this Declaration.

1. The Kim Reference (Ex. 1005)

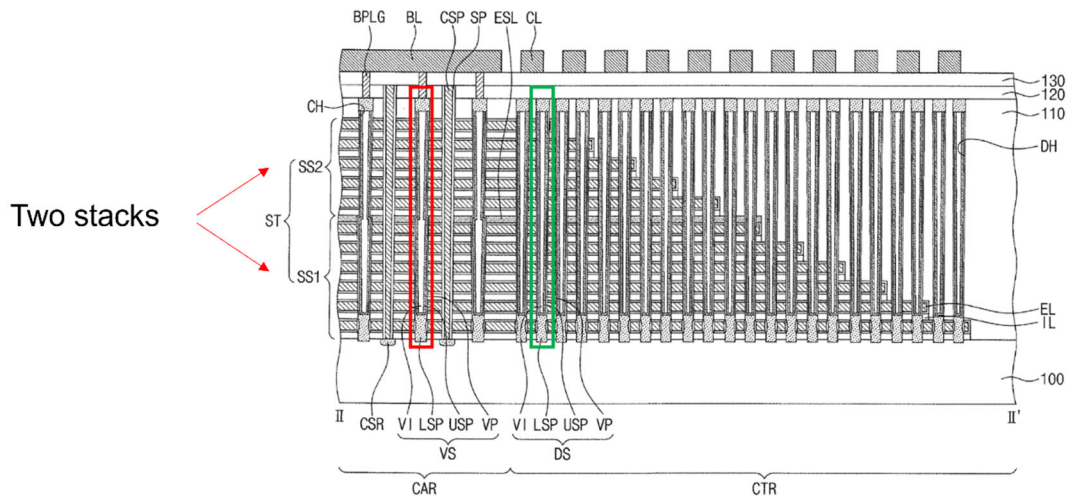
81. The Kim reference (Ex. 1005) is U.S. Pat. 10,381,369 and was filed on December 14, 2017. It is titled “Vertical Semiconductor Memory Device Structures Including Vertical Channel Structures and Vertical Dummy Structures” and was assigned to Samsung Electronics Co., Ltd.

82. As stated in Kim’s BACKGROUND section, Kim relates to “a *three-dimensional (3D) semiconductor memory device* with an improved integration density and a *method for manufacturing the same*.” Ex. 1005, 1:15-21 (emphasis added); *see also id.*, 4:56-58. Kim further discloses that “the 3D semiconductor memory device according to some embodiments of the inventive concepts may be an NAND flash memory device.” *Id.*, 8:27-30.

83. As can be seen in Fig. 4B below, Kim illustrates a multi-stack staircase structure comprised of two stacks which Kim labels “SS1” and “SS2.” Ex. 1005, 5:65-6:1 (referring to “a lower structure SS1 and an upper structure SS2.”). Kim

explains that “[t]he upper structure SS2 may be disposed on the lower structure SS1.” *Id.* Importantly, as highlighted in Fig. 4B below, Kim discloses two types of vertically oriented structures just like those found in the ’031 Patent: (1) unaligned channel structures (CH, shown in red); and (2) aligned supporting pillars (DS, shown in green).

FIG. 4B



Id., Fig. 4B (annotated).

84. Each of Kim’s “lower structure SS1” and “upper structure SS2” include their own respective “staircase” portions, which can be seen in the “CTR” region, and which makes the overall structure a multi-stack staircase structure. Ex. 1005, 5:60-6:11, 6:30-40. It should be noted that “vertical channel holes CH may penetrate each of the stack structures ST on the cell array region CAR.” *Id.*, 7:4-5. Further, Kim states that “[t]he dummy structures DS may be provided on the connection region CTR but may not be provided on the cell array region CAR.” *Id.*, 9:24-27.

85. With respect to the “vertical channel holes CH,” Kim discloses that they extend through the multi-stack staircase structure (*viz.*, both of stacks SS1 and SS2) in the CAR region. Ex. 1005, 7:4-24. “A vertical structure VS (sometimes referred to as a vertical channel structure) may be provided in each of the channel holes CH.” *Id.* It is these “vertical channel structure[s]” that comprise the strings/pillars of memory cells. *Id.*, 5:37-39. Importantly, as in the ’031 Patent, Kim discloses that the channel structures include “misaligned” sidewalls, because the channel structures in each stack are formed separately from those in the other stack. *Id.*, 11:32-35; *see also id.*, 1:45-48, Figs. 7-11. Kim explains:

Referring to FIGS. 3 and 11, second channel holes (sometimes referred to as upper channel holes) CH2 may be formed to penetrate the upper mold structure MT2 on the cell array region CAR. ... A diameter of each of the second channel holes CH2 may become progressively less toward the substrate 100. The second channel holes CH2 may vertically overlap with the first channel holes CH1, respectively. A method of forming the second channel holes CH2 may be substantially the same as the method of forming the first channel holes CH1. In some embodiments, ***the second channel holes CH2 may be misaligned with the first channel holes CH1*** when the second channel holes CH2 are formed (see FIG. 5C).

Id. 11:25-37 (emphasis added).

86. Kim explains that the misalignment is a result of using two separate etching processes to form the vertical structure holes: “[T]he process of forming the channel holes CH []includes two etching processes (i.e., the etching process for forming the first channel holes CH1 and the etching process for forming the second channel holes CH2).” Ex. 1005, 12:58-67.

87. Like Kim’s *channel structures* (viz., “vertical structure VS”), Kim discloses *support pillars* (viz., “dummy structures DS”) that also extend vertically through both of the “lower structure SS1” and “upper structure SS2” staircase structures. See, e.g., Ex. 1005, Fig 4B. However, unlike the top and bottom portions of Kim’s “vertical structures VS,” which are “misaligned” relative to each other, Kim’s “dummy structures DS” are fully aligned because these pillars are formed in a single processing step after the formation of both stacks. *Id.*, 12:58-67. Kim expressly teaches that “the dummy holes DH [for the dummy structures DS] may be formed by one etching process after the formation of the lower mold structure MT1 and the upper mold structure MT2. Thus, the process of forming the dummy holes DH may be simpler than the process of forming the channel holes CH, which includes two etching processes (i.e., the etching process for forming the first channel holes CH1 and the etching process for forming the second channel holes CH2).” *Id.* Kim further teaches that “dummy structures DS” “may physically support the stack structure.” *Id.*, 9:30-38.

88. The distinction between channels with misaligned sidewalls and support structures with planar sidewalls is so fundamental to Kim that it is described prominently in the Abstract:

A vertical memory device structure can include a vertical channel structure that vertically penetrates through an upper structure and a lower structure of a stack structure in a cell array region of the device. The vertical channel structure can have a side wall with a stepped profile at a level in the vertical channel structure where the upper structure meets the lower structure. A vertical dummy structure can vertically penetrate through a staircase structure that is defined by the upper structure and the lower structure in a connection region of the device, and the vertical dummy structure can have a side wall with a planar profile at the level where the upper structure meets the lower structure.

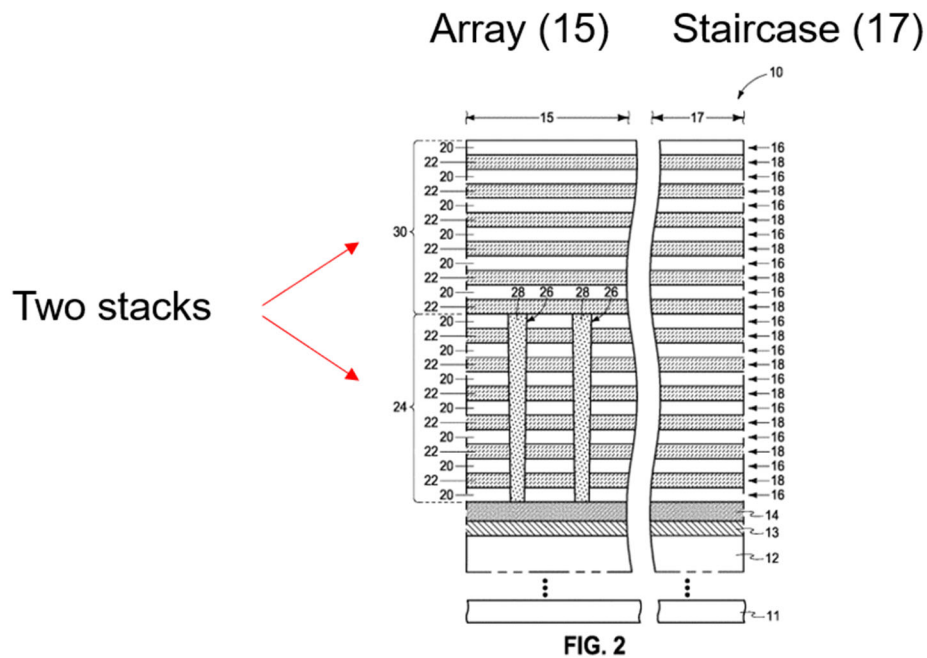
Ex. 1005, Abstract.

2. The Tessariol Reference (Ex. 1006)

89. The Tessariol reference (Ex. 1006) is a U.S. Pat. Application Publication that was filed on September 14, 2017 and published on March 14, 2019. It is titled “Device, a Method Used in Forming a Circuit Structure, a Method Used in Forming an Array of Elevationally-Extending Transistors and a Circuit Structure Adjacent Thereto” and is assigned to Micron Technology, Inc.

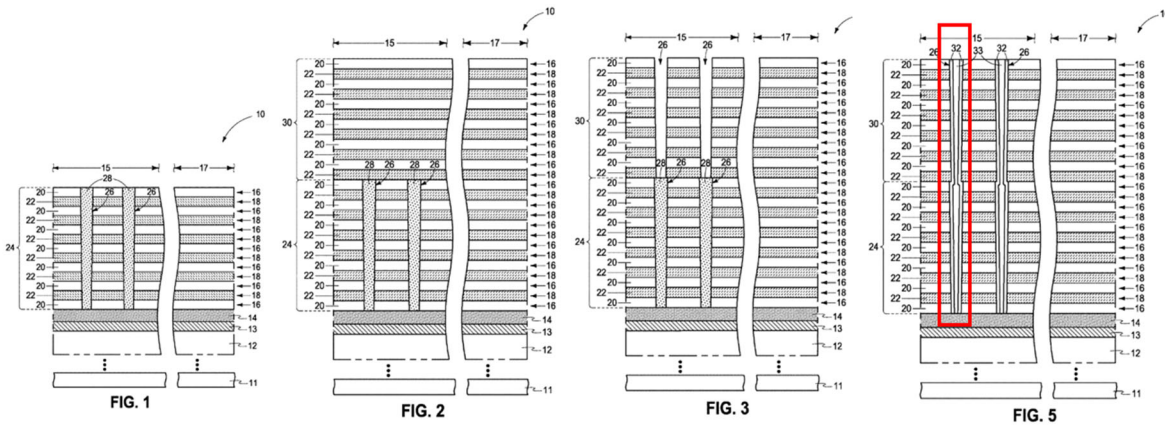
90. As its BACKGROUND section indicates, Tessariol relates to 3D NAND memory. Ex. 1006, [0006]; *see also id.*, [0027]. As I describe in further detail below, Tessariol discloses a multi-stack staircase structure, unaligned channel structures, and aligned supporting pillars, all of which are like those used in the '031 Patent.

91. As can be seen in Fig. 2 below, Tessariol illustrates a multi-stack staircase structure comprised of two stacks which Tessariol calls “first stack 24” and “second stack 30.” Ex. 1006, [0031] (“Referring to FIG. 2, a second stack 30 of vertically-alternating tiers 18, 16 of different composition materials 22, 20 has been formed over first stack 24”). Both the first stack and second stack structures include an “array portion 15” with channel structures and an “adjacent portion 17” with a stair step portion and supporting pillars. *Id.*, [0028], [0029], [0031], [0034].



Id., Fig. 2 (annotated).

92. The sequence of Figs. 1-3 and 5 below illustrate the formation of Tessariol's channels (which extend through both stack 24 and stack 30). Just as in the '031 Patent, Tessariol discloses that its "channel" structures have unaligned sidewalls, because the channel structures are formed using two separate etch processes:



Ex. 1006, Figs. 1-3, 5, [0030]-[0033].

93. In addition to its *channel structures*, Tessariol also discloses “dummy-support structures 60” and “operative conductive vias 58” that act as *support pillars* to provide structural support to the stack structures. Ex. 1006, [0038]-[0041]; *see also id.*, [0041] (referring to “dummy-support structures 60”). It is important to note that, in contrast to its *channel structures*, Tessariol’s *support pillars* are aligned, because these pillars are made in one etch step after the formation of both stacks (as shown in Figs. 8-9 below). *Id.*, [0037] (forming openings through both stacks with one etch).

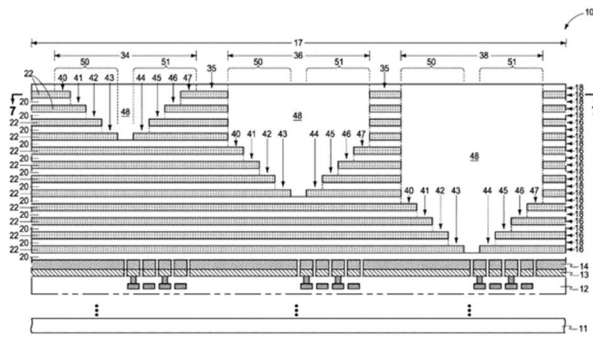


FIG. 6

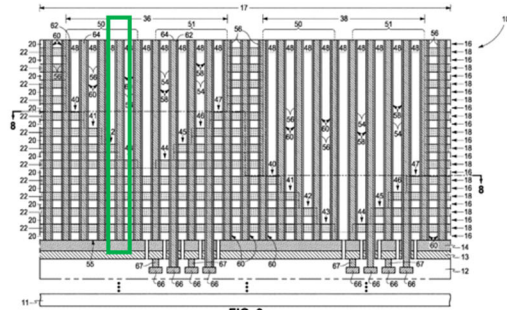


FIG. 9

Id., Figs. 8, 9 (annotated).

XIII. GROUND 1: KIM WITH THE KNOWLEDGE OF A POSITA RENDERS CLAIMS 1-4 OBVIOUS

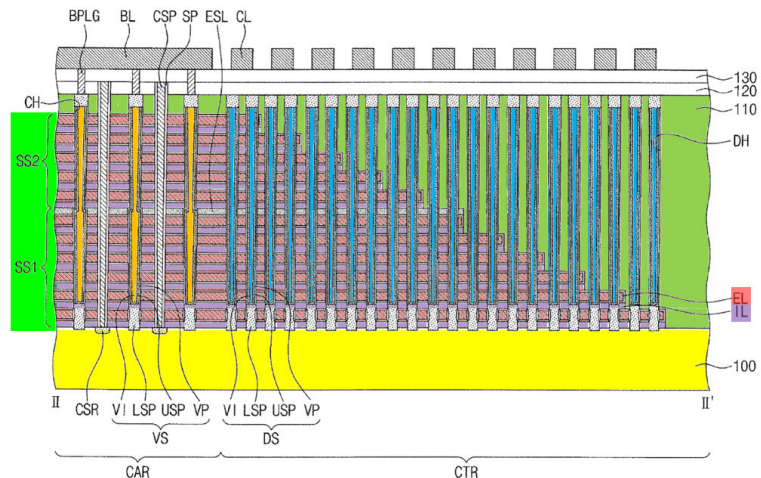
94. Ground 1 demonstrates that claims 1-4 are rendered obvious over Kim in view of the knowledge of a POSITA.

A. Claim 1

95. I analyze each element of claim 1 separately in more detail below, but provide here a high-level color-coded mapping of Kim to claim 1 for ease of reference and a wholistic view of my analysis.

Kim, Fig. 4B

'031 Patent, Claim 1	
I. A memory device comprising:	
a substrate;	
a multiple-stack staircase structure comprising a plurality of staircase structures stacked over the substrate, wherein each of the plurality of staircase structures comprises a plurality of conductor layers, wherein each of the plurality of conductor layers is located between two insulating layers;	
a filling structure surrounding the multiple-stack staircase structure;	
a semiconductor channel extending through the multiple-stack staircase structure, wherein the semiconductor channel comprises unaligned sidewall surfaces; and	
a supporting pillar extending through at least one of the multiple-stack staircase structure and the filling structure, wherein the supporting pillar comprises aligned sidewall surfaces.	



1. [1.PRE] “A memory device comprising:”

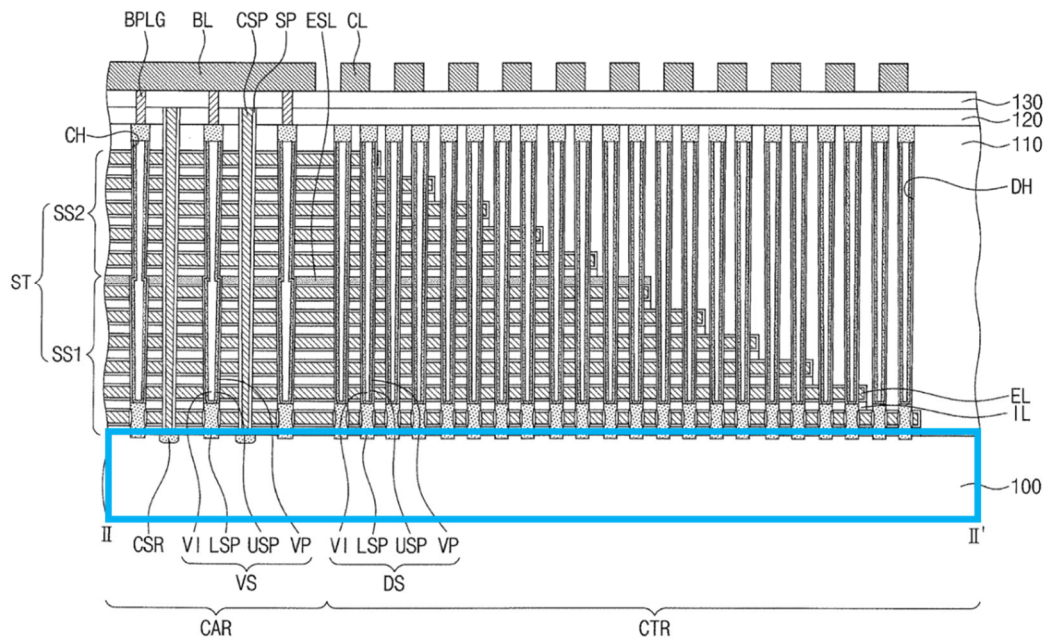
96. I offer no opinion on whether the preamble is or is not limiting. However, if the preamble is considered to be a limitation, my opinion is that Kim discloses it. Indeed, the title of the Kim reference is “Vertical Semiconductor *Memory Device* Structure ...” (emphasis added). *See also* Ex. 1005, 1:17-20 (“Embodiments of the inventive concepts relate to ... a three-dimensional (3D) semiconductor memory device.”); *id.*, 1:38-41 (disclosing “vertical semiconductor memory device structures including vertical channel structures and vertical dummy structures and methods of forming the same”). Therefore, Kim discloses a *memory device*⁴ (e.g., “semiconductor memory device”).

2. [1.A] “a substrate;”

97. Kim discloses “*a substrate*.” Substrates are extremely common in semiconductor memory devices and are typically used as the base or platform on top of which the memory is fabricated. Kim is no different, and discloses “a substrate 100” that includes “a cell array region CAR and a connection region CTR.” Ex. 1005, 5:53-59. Kim’s substrate 100 is shown in light blue below:

⁴ In this Declaration, I denote claim language using red and italics.

FIG. 4B



Id., Fig. 4B (annotated).

98. Thus, Kim discloses a *substrate* (e.g., substrate 100).

3. [1.B] “a multiple-stack staircase structure comprising a plurality of staircase structures stacked over the substrate,”

99. Kim discloses this claim element. To begin, the '031 specification explains that a “‘staircase structure’ or a ‘stepped cavity structure,’ or similar refer to a structure having stepped surfaces.” Ex. 1001, 9:39-41. The claim uses *staircase structure* in the same manner to refer not only to the staircase region, but more generally to encompass the broader structure that includes a staircase region. Likewise, the claimed *multiple-stack staircase structure* encompasses the overall structure that includes a staircase region, but is not limited to just the staircase region of the structure. This is apparent from examining claim element [1.E] which recites

on the right hand side of Fig. 4B.⁵ *See also id.*, 9:11-13 (“the electrodes EL are arranged in a staircase structure on the connection region CTR”); 10:60-62 (disclosing that “the mold structure MT disposed on the connection region CTR may be formed into a staircase structure”). The upper and lower stacks themselves, however, extend across both the CTR region (which has the staircase profile) and the CAR region (where the memory cells reside). *See id.*, 6:1-3 (“Each of the stack structures ST may include a lower structure SS1 and an upper structure SS2 [which] ... may extend from the cell array region CAR onto the connection region CTR in a second direction D2.”). Additionally, both the upper (SS1) and lower (SS2) structures are on top of substrate 100 (identified in blue above), and are thus *stacked over the substrate*. *See id.*, 5:67-6:1 (“The upper structure SS2 may be disposed on the lower structure SS1.”); *see also id.* 10:50-59.

⁵ The creation of a *staircase structure* is facilitated by the presence of the “insulating layers IL and electrode[] layers EL which are vertically alternately stacked (sometimes referred to as alternating electrode layers and insulating layers).” Ex. 1005, 5:61-6:1. The layers are deposited and/or etched using conventional semiconductor fabrication techniques to create the distinctive and easily recognizable “staircase” profile.

101. Next, I address the requirement of *a multiple-stack staircase structure*. That Kim meets this requirement follows naturally from Kim’s disclosure of “lower structure SS1” and “upper structure SS2” discussed in the previous paragraph. As shown in Fig. 4B, the “upper structure SS2” sits on top of the “lower structure SS1,” as would be expected by their names (*i.e.*, “upper” and “lower”). Together, the “lower structure SS1” and “upper structure SS2” form *a multiple-stack staircase structure* because there are two (*i.e.*, multiple) staircase structures. In particular, Kim refers to the combination of the upper and lower staircase structures as a “stack structure[] ST.” Ex. 1005, 5:60-6:1 (“Each of the stack structures ST may include a lower structure SS1 and an upper structure SS2. The upper structure SS2 may be disposed on the lower structure SS1.”). The stack structure ST can be seen in Fig. 4B and is labelled by Kim itself on the lefthand side of the figure.

102. I note that an *optional* etch stop layer (ESL) may exist between the two staircase structures. Ex. 1005, 6:41-54 (“An etch stop layer ESL *may be provided* at the uppermost layer of the lower structure SS1”) (emphasis added). However, Kim discloses that the ESL “may be omitted.” *See id.*, 13:41-50 (“In some embodiments, referring to FIGS. 3 and 15, the etch stop layer ESL of the uppermost layer of the lower structure SS1 may be omitted.”). But even when the ESL is present, Kim still satisfies the claim limitation because the ’031 Patent claims expressly provide that a structure may exist between the stacks. Ex. 1001, claim 6

(“a connection layer in the semiconductor channel between two adjacent staircase structures”).

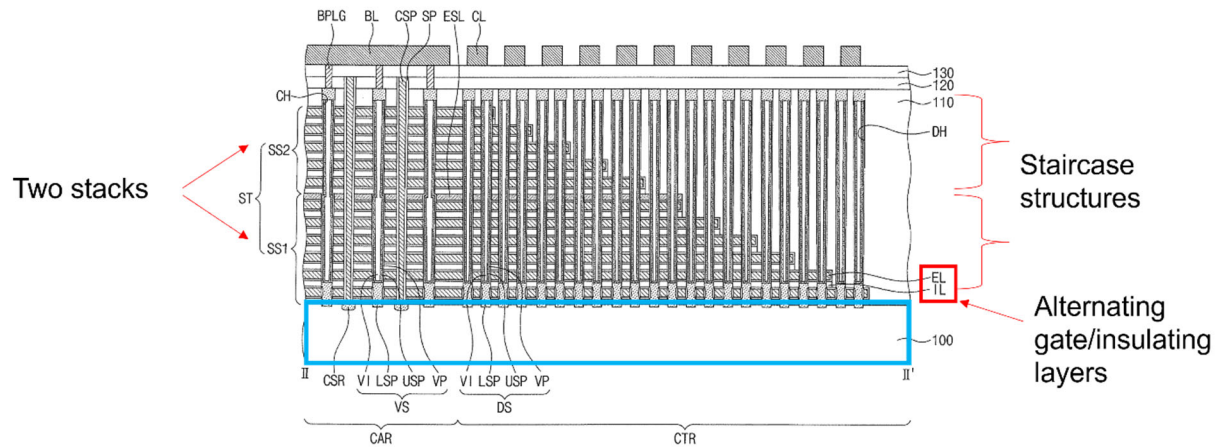
103. Although not a requirement of claim 1, I note that the '031 Patent discloses forming both stacks (*viz.*, upper and lower stacks) and then creating the multi-stack staircase structure in the same way as Kim. Ex. 1001, Figs. 2-3, 13:11-21.

104. In summary, Kim discloses a *multiple-stack staircase structure* (stack structure ST) *comprising a plurality of staircase structures* (lower and upper structures SS1 and SS2) *stacked over the substrate* (substrate 100).

4. [1.C] “wherein each of the plurality of staircase structures comprises a plurality of conductor layers, wherein each of the plurality of conductor layers is located between two insulating layers;”

105. Kim satisfies this limitation. In particular, the “lower structure SS1” and “upper structure SS2” (*i.e.*, *the plurality of staircase structures*) are each formed, respectively, from “insulating layers IL and electrodes layers EL which are vertically alternately stacked (sometimes referred to as alternating electrode layers and insulating layers).” Ex. 1005, 5:61-64. This can be seen in Fig. 4B below.

FIG. 4B



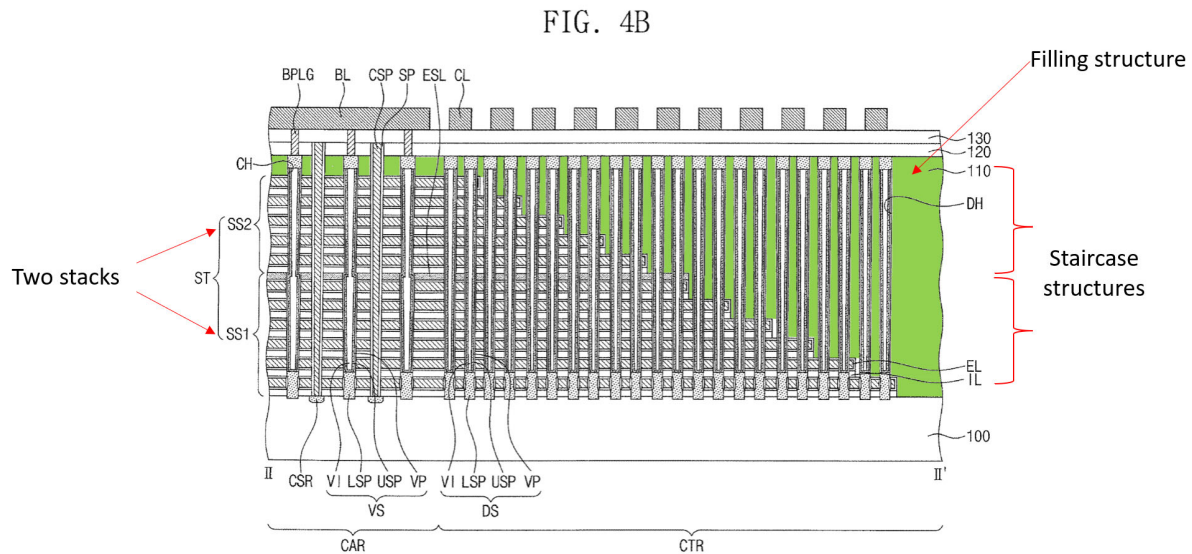
Id., Fig. 4B (annotated). Kim discloses that “[t]he electrodes EL may be vertically isolated from each other by the insulating layers IL disposed there between.” *Id.*, 6:30-35. A POSITA would understand that the “electrode layers EL” are conductors, and Kim discloses that the electrode layers may be formed from a variety of different conductive materials such as “tungsten, copper, or aluminum,” among others. *Id.*, 6:55-63. And the insulating layers IL “may include a silicon oxide layer.” *Id.*, 6:59-61.

106. Thus, Kim discloses that the plurality of staircase structures comprises “*a plurality of conductor layers, wherein each of the plurality of conductor layers is located between two insulating layers*” (e.g., the EL and IL layers).

5. [1.D] “a filling structure surrounding the multiple-stack staircase structure;”

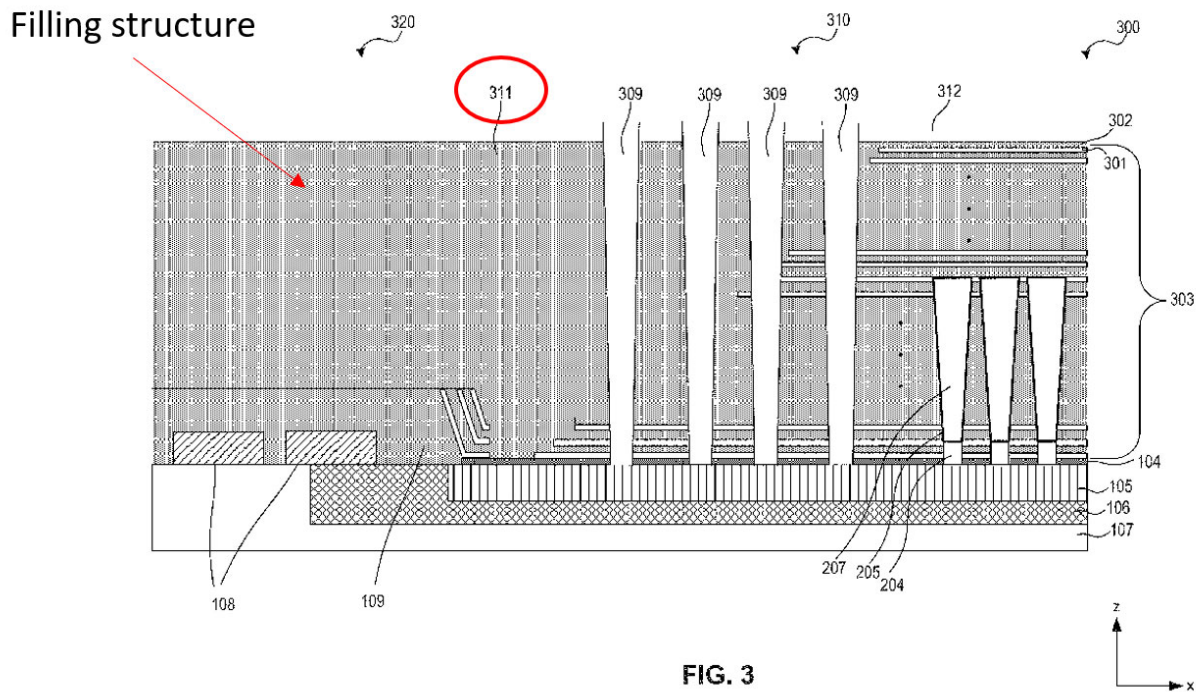
107. Kim discloses, or at least renders obvious, this claim element. In particular, Kim discloses that a “filling insulating layer 110” “may be disposed on

the substrate 100 and may cover the stack structures ST. The filling insulation layer 110 may have a planarized top surface.” Ex. 1005, 9:53-56. The insulating layer 110 fills the voids after the staircase structures are formed. *Id.*, 10:60-11:21, Figs. 9-10.



Id., Fig. 4B (annotated).

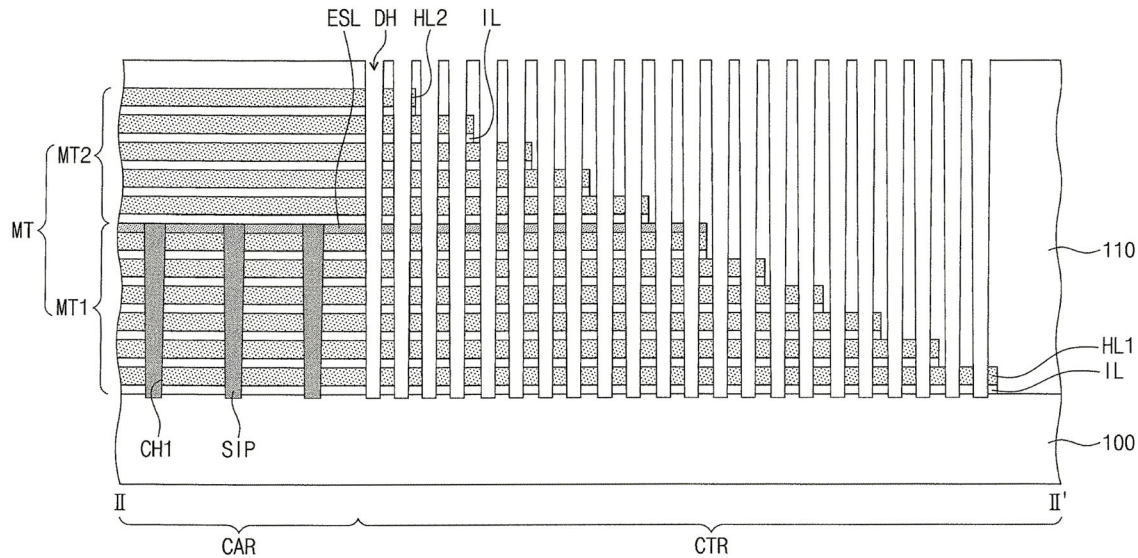
108. Kim’s “filling insulation layer 110” *surrounds* the multi-stack staircase structure (ST). As the ’031 Patent illustrates in Figure 3 below, following formation of the staircase, a “dielectric filling material (*e.g.*, over staircase structure 303 and isolation layer 109)” is deposited to form “dielectric filling structure 311 that surrounds staircase structure 303.” Ex. 1001, 13:44-48.



Id., Fig. 3 (annotated).

109. Kim discloses the same. As illustrated in Kim Fig. 10 below, after forming the staircase region, Kim forms insulation layer 110 that fills all of the voids. Ex. 1005, 11:10-21 (“a filling insulation layer 110 may be formed on an entire top surface of the substrate 100 to cover the mold structure MT.”).

FIG. 10



Id., Fig. 10. Note that Figures 6-13 describe the manufacturing process and label the stacks MT1 and MT2 instead of ST1 and ST2. Ex. 1005, 10:4-7.

110. In my opinion, a POSITA would understand that Kim discloses that “filling insulation layer 110” *surrounds* the multi-stack structure (ST) as that term is used in the '031 Patent and claims. In this regard, I note that the '031 Patent never discloses any embodiment (in its figures or text) in which the filling structure exists on each and every side of the multi-stack structure. If the Patent Owner were to contend otherwise, it runs headlong into the disclosure of the '031 specification.

111. In any event, Kim discloses (or at least renders obvious) element [1.D] for at least three reasons.

112. First, as previously noted, Kim discloses a “filling insulating layer 110” that “may be disposed on the substrate 100 and may cover the stack structures ST. The filling insulation layer 110 may have a planarized top surface.” Ex. 1005, 9:53-56; *see also id.*, 11:11-21 (“Referring to FIGS. 3 and 10, a filling insulation layer 110 may be formed on an entire top surface of the substrate 100 to cover the mold structure MT.”). Kim’s disclosure of depositing the filling insulation layer over “substrate 100” to cover the stacks means that the filling material will encase the memory device. This can be seen in Fig. 4B, including planarizing the top surface of the filling insulation layer. Note that from a practical standpoint, the top surface above the stack must be planar. This is because the upper-level metal layers must be highly planar, or otherwise, there will be challenges patterning them due to depth of focus issues during optical lithography. There will also be challenges etching the metal interconnects on non-planar topographies. Depending on the layout, there can be residual metal filaments or “stringers” at notches in the underlying topography, leading to electrical shorts. The interface to the metal layers must be planar, and each metal layer itself must be planar. Thus, such filling insulators are understood to surround the stack structures to create a planar surface for the upper-level metal layer. Ex. 1023, 14.

113. Second, as shown in Fig. 10 above, Kim discloses filling material on the outer edge of where the staircase region ends (*e.g.*, on the far-right side of the

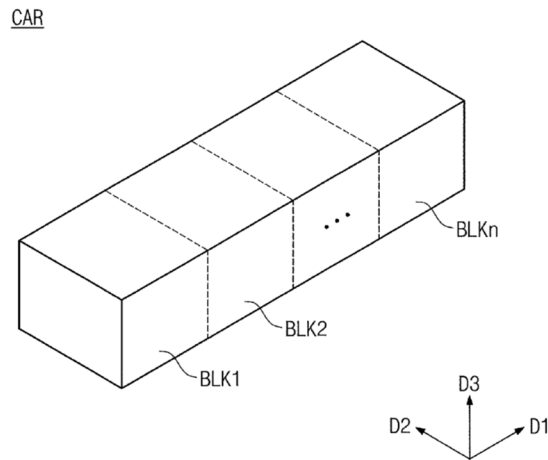
figure). Consistent with this filling pattern, a POSITA would have understood, and certainly found it obvious, that the filling material would similarly extend to the other outer edges of the memory device as well, not just the right side (*viz.*, the filling material would be present on all sides/edges of the memory device). This is consistent with traditional semiconductor fabrication processing and chip design techniques. PECVD (Plasma-Enhanced Chemical Vapor Deposition), which is often used for this purpose, is an isotropic process leading to deposition on all sides, except the bottom surface which is blocked. No extra manufacturing steps would be needed to accomplish this result, and having uniform filling material on all sides would make for a symmetric device, which is generally desirable.

114. Third, in view of Kim Fig. 3 and the knowledge of a POSITA, it also would have been understood, or at least obvious, that insulating layer 110 (or other similar dielectric fill) would surround all sides⁶ of the multiple-stack structure.

115. Kim discloses a multi-block memory (*i.e.*, a memory device comprised of multiple blocks (BLK) of memory), as shown below:

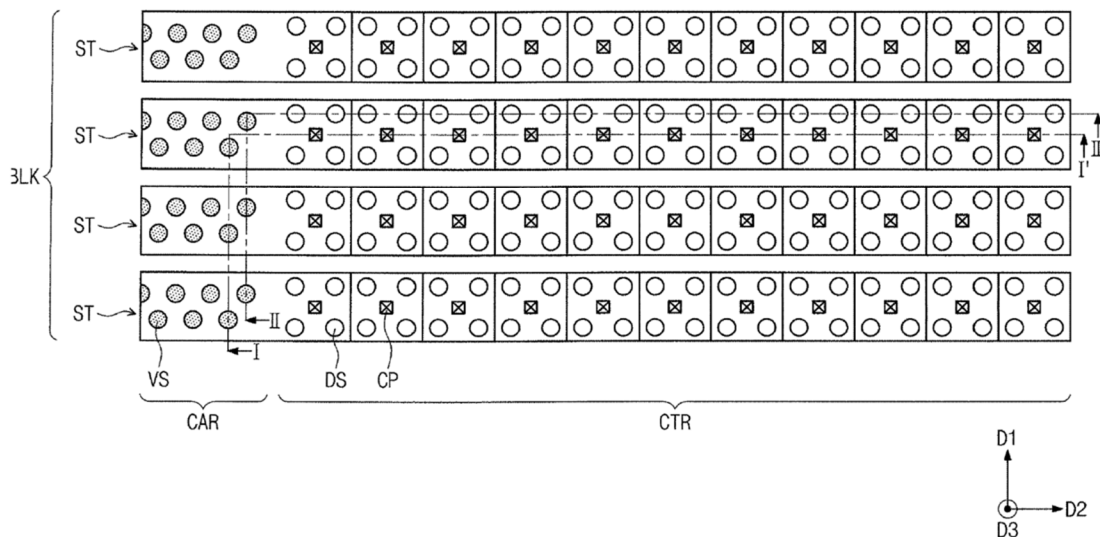
⁶ This excludes the bottom side. In all cases, the bottom of a staircase structure will sit on the substrate (or on a layer which is on the substrate). Here, I'm not using surround to include the bottom side.

FIG. 2



Ex. 1005, Fig. 2, 5:29-42. Kim Fig. 3 depicts a top view of such a memory block:

FIG. 3



Id., Fig. 3, 5:43-52.

116. It was well-known to POSITAs that in memory block arrangements (which were very common in the art), a common technique was to isolate the blocks



Ex. 1011 (U.S. Pat. 10,559,583 to Park), Fig. 3 (highlighted). As Park discloses, source lines 102 and insulating layers 111 are used to isolate BK1 and BK2 for better operation. *Id.*, 5:66-6:12 (“[T]he string select line and the ground select line may be separated from each other between the first to eighth unit areas UA1 to UA8 ... by the first common source lines 102 and first lines 103 of the second common source lines 105. Moreover, portions of the ground select line may be separated from each other at the boundaries between the first to eighth unit areas UA1 to UA8 by the first common source lines 102, the second common source lines 105, and isolation

insulating layers 111.”). As was well known, the common source lines 102 include (1) a conductive core, because these structures serve as an interconnect to connect an upper-level source connection to the substrate, and (2) an insulating liner, because the common source line cannot electrically contact the conductive gate layers. *Id.*, 10:46-11:8, Fig. 11. These common lines extend from the top of the alternating layer stack to the substrate. *Id.* By analogy, the common source lines are like a wall with the outer portions of that wall being the insulating liner. With respect to Figure 3 of Kim, these common source lines run in direction 2 and surround the staircase and array regions along direction 2. Thus, Kim would have been understood to disclose (or at least render obvious) that additional insulating material (filling structure) would exist that encases the array and staircase portions, resulting in a filling structure on all sides of the staircase structures.

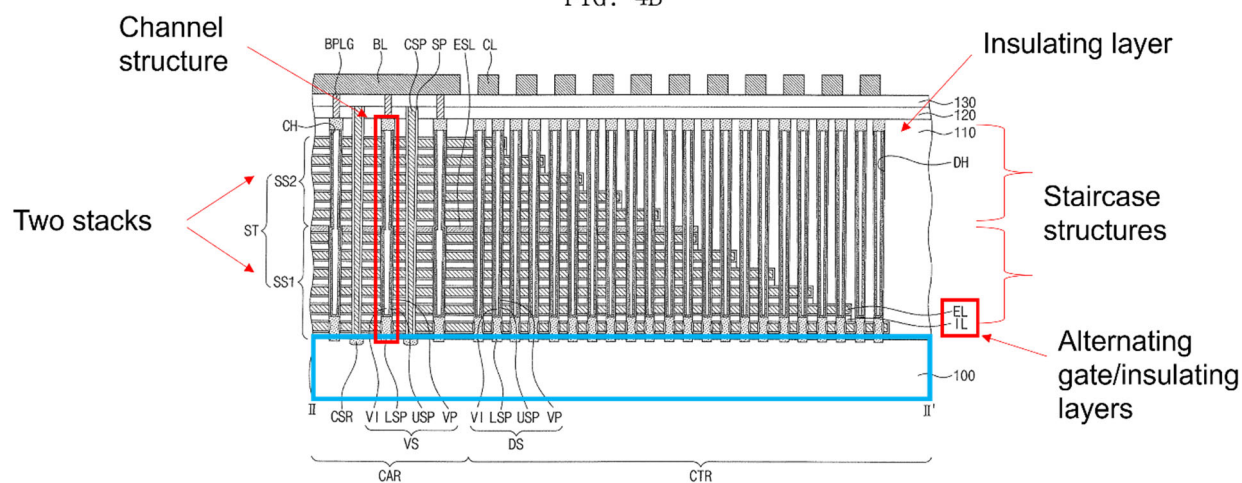
117. In summary, Kim discloses, or at least renders obvious, “*a filling structure (e.g., insulation layer 110) surrounding the multiple-stack staircase structure.*”

6. [1.E] “a semiconductor channel extending through the multiple-stack staircase structure,”

118. Kim satisfies this claim element. Kim’s vertical structure (VS) (where the memory cells are formed) is the claimed *semiconductor channel*. In particular, Kim discloses “[a] memory cell array (or a cell array) including a plurality of

memory cells may be disposed in the cell array region CAR.” Ex. 1005, 5:1-3. According to Kim, the cell array region (CAR) includes a “stack structure [ST]. . . coupled to a plurality of vertical structures [VS] (e.g., *semiconductor pillars*) to constitute memory cells three-dimensionally arranged.” *Id.*, 5:37-39 (emphasis added). Kim explains that these vertical memory device structures are “channels,” namely, the VS structures (shown in Fig. 4B below in red) are “vertical channel structure[s] that vertically penetrate [] through an upper structure [SS2] and a lower structure [SS1] of a stack structure [ST] in a cell array region of the device.” *Id.*, 1:42-45.

FIG. 4B

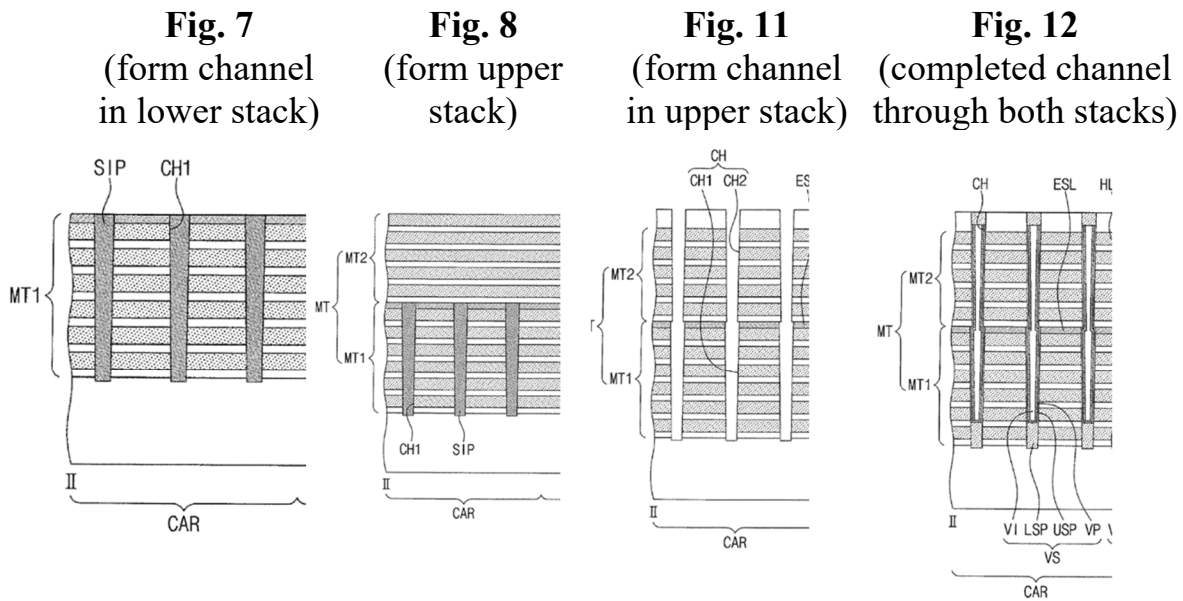


Id., Fig. 4B (annotated), 7:15-24 (semiconductor channel material).

119. Accordingly, Kim meets the requirement of a *semiconductor channel* (e.g., vertical channel structure VS) *extending through the multiple-stack staircase structure* (e.g., stack structure ST).

7. [1.F] “wherein the semiconductor channel comprises unaligned sidewall surfaces; and”

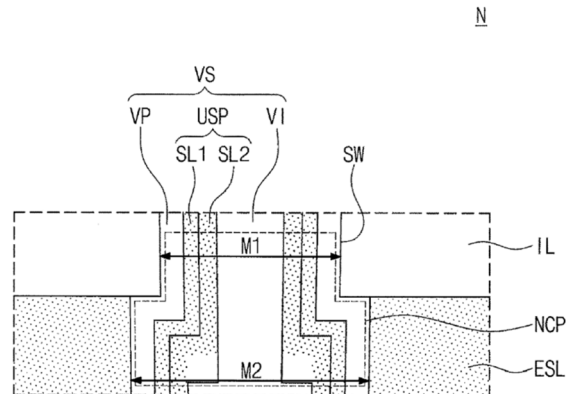
120. Kim discloses this claim element. In particular, Kim discloses that its “vertical channel structure” (viz., the claimed *semiconductor channel*) “can have a side wall with a *stepped profile* at a level in the vertical channel structure where the upper structure meets the lower structure.” Ex. 1005, 1:45-48 (emphasis added). A POSITA would understand that the Kim’s “stepped profile” results in an *unaligned sidewall surface*. Kim explains that the reason for having unaligned sidewalls in its vertical channels is that the channels are formed by first etching a channel hole (CH1) in the lower stack, then forming the second stack and etching another hole (CH2) in the upper stack, and thereafter forming the channel structure (VS):



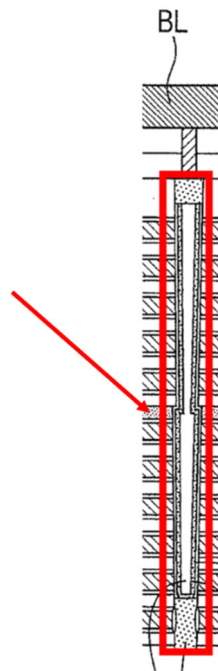
Id., Figs. 7, 8, 11, 12 (figures are all partial), 10:26-12:9.

121. Kim explains that the result of the two-step etch process is that the top portion of the first stack sub-channel (CH1 in MT1) is wider in diameter than the bottom portion of the second stack sub-channel (CH2 in MT2). Ex. 1005, 7:65-8:20. There can also be some misalignment between the two photolithography steps for the lower and upper stack memory cell hole etches, as described later. With respect to the interface region (which Kim call the “NCP” area), Kim expressly discloses that “[t]he diameter of the portion NCP may increase [sic] (sharply) at an interface the upper structure SS2 and the lower structure SS1.” *Id.*, 8:15-17. In other words, there exist *unaligned sidewall surfaces* at the interface/boundary of the upper and lower sub-channels. Kim depicts these unaligned sidewall surfaces of the channel in Figure 5B:

FIG. 5B



Id., Fig. 5B. The unaligned sidewall channel surfaces can be seen in Figure 4B as well:

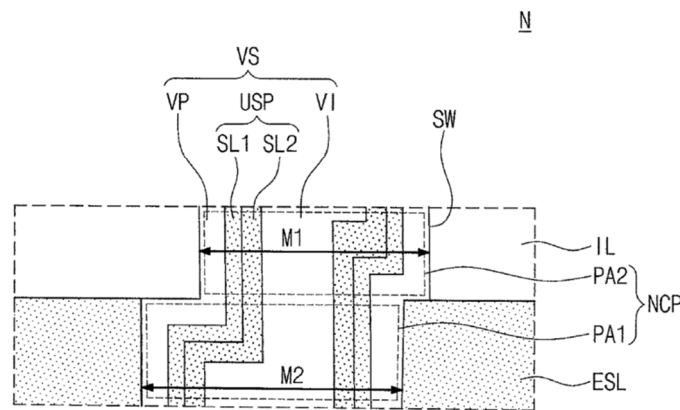


Id., Fig. 4B (partial and annotated).

122. Moreover, Kim further discloses related embodiments in which “the second channel holes CH2 may be ***misaligned*** with the first channel holes CH1 when

the second channel holes CH2 are formed (see FIG. 5C).” Ex. 1005, 11:32-35 (emphasis added). This misalignment primarily results from manufacturing imperfections and tolerances which make it difficult to precisely position the upper sub-channel exactly on top of the lower sub-channel. This is another artifact of using a two-etch process and is another way in which element [1.F] (*viz.*, *unaligned sidewall surfaces*) is satisfied by Kim.

FIG. 5C



Id., Fig. 5C.

123. In summary, Kim *discloses semiconductor channels* (e.g., vertical channel structures VS) *comprising unaligned sidewall surfaces* (e.g., the misalignment that occurs at the interface/boundary of the upper and lower sub-channels).

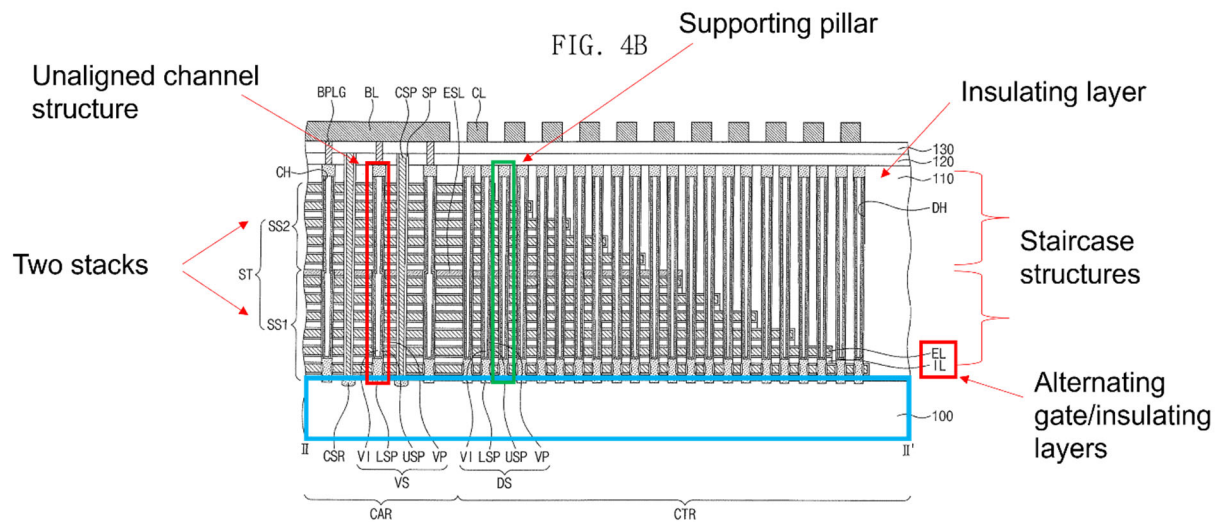
8. [1.G] “a supporting pillar extending through at least one of the multiple-stack staircase structure and the filling structure,”

124. Kim discloses this claim element. The *supporting pillars* in Kim are “dummy structures DS.” *See, e.g.*, Ex. 1005, 2:2-6. To frame my analysis, it is helpful to refer to how the ’031 Patent uses the term *supporting pillar*. Consistent with the plain and ordinary meaning of those words, the ’031 Patent uses “supporting pillar” to refer to a vertical column that functions to support the stack structure and “prevent collapse during formation of the word lines.” *See, e.g.*, Ex. 1001-7:22-25.

125. In like manner, Kim discloses that “dummy structures DS may physically support the stack structures ST on the connection region CTR.” Ex. 1005, 9:30-31; 16:60-62 (same). A POSITA would have understood that Kim describes the function of the dummy structures as providing “support” because these structures support the stack during, *e.g.*, the removal of the sacrificial gate layer. *Id.*, 9:30-31, 10:8-16.

126. Kim explains that “[a] vertical dummy structure can vertically penetrate through the staircase structure, where the vertical dummy structure has a side wall with a planar profile at the level in the vertical dummy structure where the upper structure meets the etch stop layer.” Ex. 1005, 1:64-2:6. Bearing in mind that the Kim’s CTR region is a region of the multiple-stack staircase structure (*id.*, 9:4-19), Kim discloses that “[a] plurality of dummy holes DH may penetrate a filling

insulation layer 110 and the stack structure ST on the connection region CTR. A dummy structure (sometimes referred to as a vertical dummy structure) DS may be provided in each of the dummy holes DH, respectively” (*id.*, 9:20-24). A dummy structure DS (*viz.*, the claimed *supporting pillar*) is shown in Fig. 4B below and highlighted in green.



Id., Fig. 4B (annotated). As can be seen, the dummy structures DS extend vertically through the entirety of ST (the *multiple-stack staircase structure*) and the filling structure 110.

127. In summary, Kim discloses *a supporting pillar* (e.g., dummy structures DS) *extending through at least one* (both) *of the multiple-stack staircase structure* (e.g., stack structure ST, including lower structure SS1 and upper structure SS2) and the *filling structure* (e.g., filling insulation layer 110).

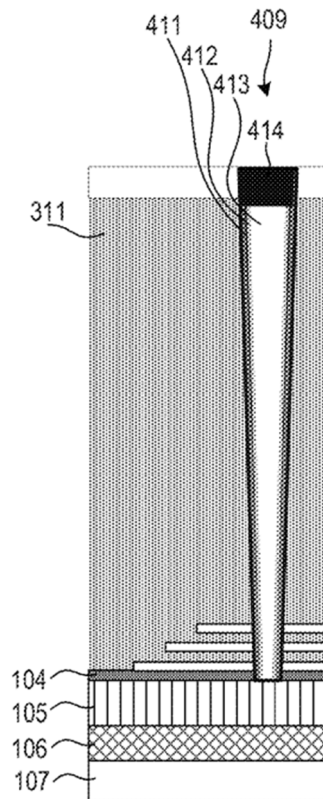
9. [1.H] “wherein the supporting pillar comprises aligned sidewall surfaces.”

128. Kim discloses this claim element. In particular, Kim discloses that “[a] diameter of the dummy structure DS may become progressively less toward the substrate 100. The diameter of the dummy structure DS may become continuously less from the upper structure SS2 to the lower structure SS1. In other words, unlike the vertical structure VS described above, the diameter of the dummy structure DS may not be sharply changed, rather *a side wall of the dummy structure DS may have a planar profile.*” Ex. 1005, 9:39-46 (emphasis added).

129. More specifically, unlike Kim’s process for forming the vertical channel structures VS (*viz.*, two step etch where the upper and lower stacks are separately etched), Kim discloses using a single-step etch process to form the supporting pillars (dummy structures DS) after formation of the multi-stack structure ST: “[i]n the manufacturing method according to some embodiments of the inventive concepts, *the dummy holes DH may be formed by one etching process after the formation of the lower mold structure MT1 and the upper mold structure MT2 [(stack structure ST)].* Thus, the process of forming the dummy holes DH may be simpler than the process of forming the channel holes CH, which includes two etching processes (*i.e.*, the etching process for forming the first channel holes CH1

and the etching process for forming the second channel holes CH2).” Ex. 1005, 12:58-67 (emphasis added).

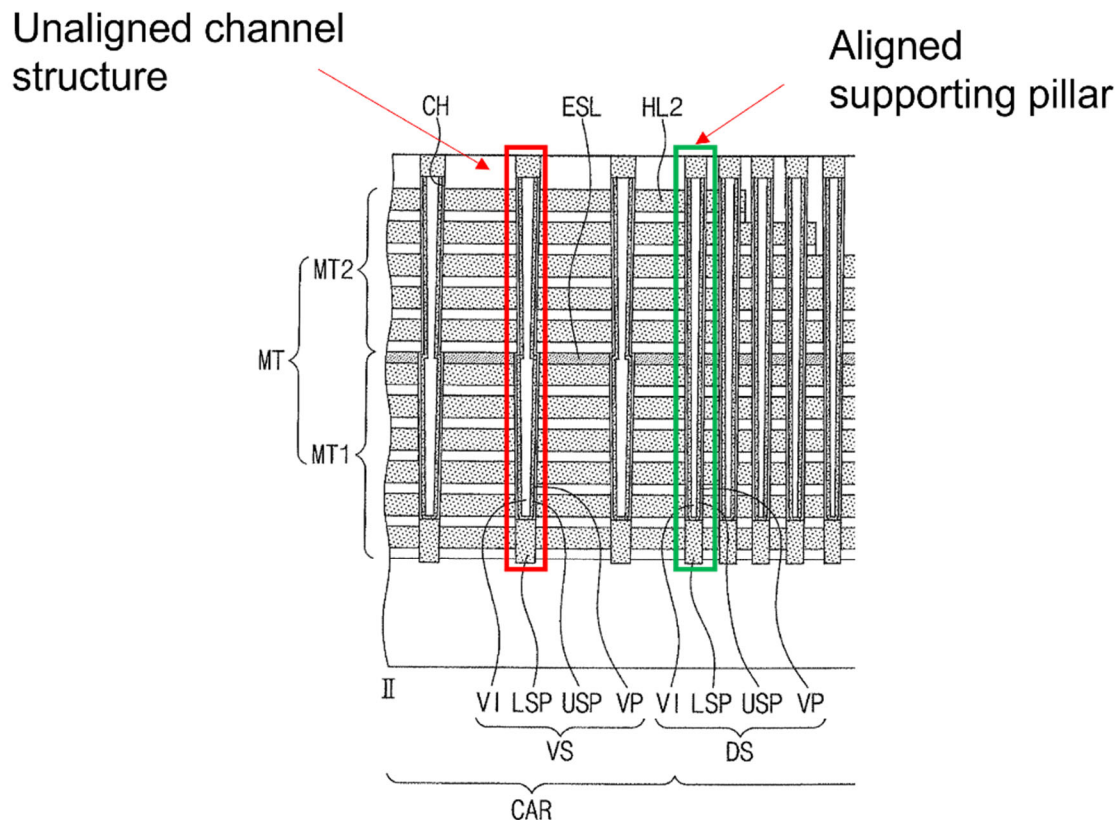
130. As a result of the one-etch process used to create the dummy holes DH (subsequently filled in to create the dummy structure DS which are the *supporting pillars*), Kim discloses that “the vertical dummy structure can have a side wall with a *planar profile* at the level where the upper structure meets the lower structure.” Ex. 1005, 1:51-53 (emphasis added). Indeed, Kim’s pillars have the same profile as the *supporting pillars* in the ’031 Patent, an example of which is shown below:



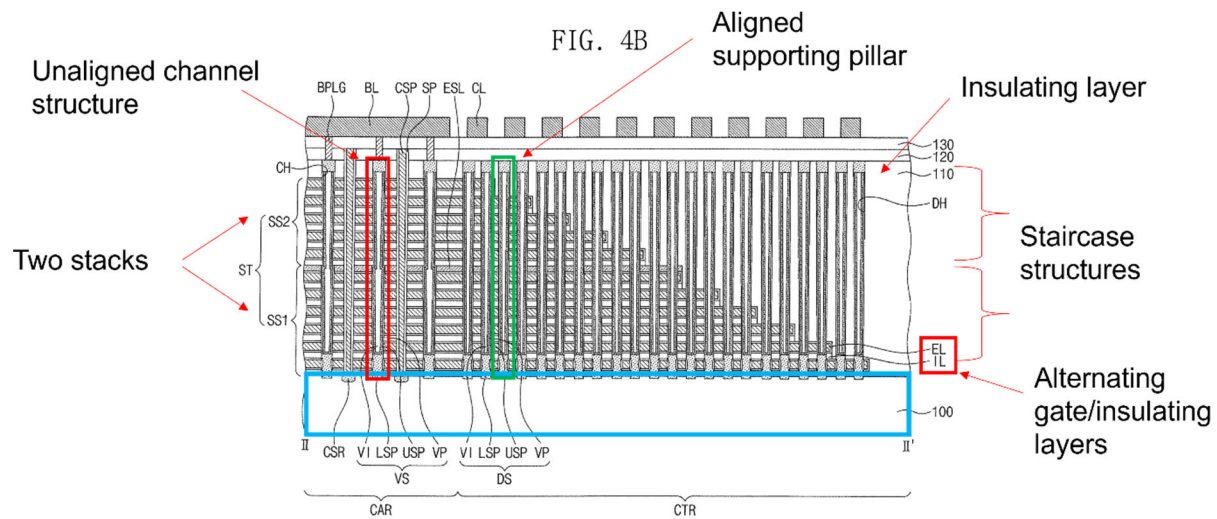
Ex. 1001, Fig. 4 (partial), 9:4-12 (“[p]illar holes through the multiple-stack staircase structure can be formed after the formation of the multiple-stack staircase structures

by one patterning process. Pillar holes can be formed . . . after the formation of the channel holes of the upper dielectric stack”).

131. While the difference between Kim’s aligned/planar sidewalls in dummy structures DS and the unaligned/misaligned sidewalls in vertical structure (VS) can be seen in Kim Fig. 4B, the difference is more prominent and easily recognizable in Kim Fig. 12. Both figures are reproduced below.



Ex. 1005, Fig. 12 (partial and annotated).



Id., Fig. 4B (annotated).

132. In summary, Kim discloses that *the supporting pillar* (e.g., dummy structure DS) *comprises aligned sidewall surfaces* (planar sidewalls).

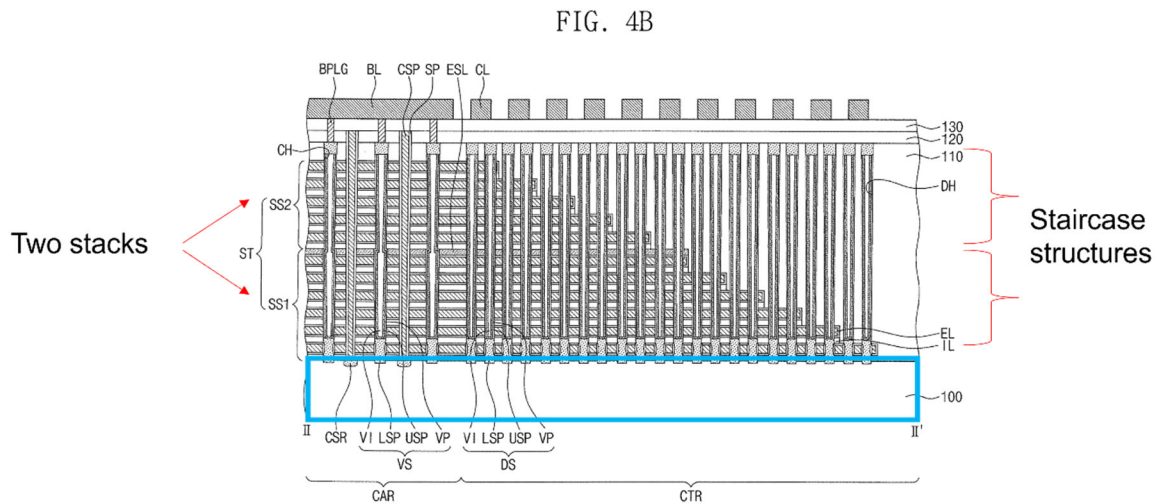
B. Claim 2

133. Claim 2 is a dependent claim that depend on claim 1. I address how Kim satisfies both the additional elements of claim 2 below.

1. [2.A] “the multi-stack staircase structure comprises a first staircase structure over the substrate and a second staircase structure over the first staircase structure; and”

134. Kim discloses this claim element. As already discussed for element [1.B], Kim discloses *a multiple-stack staircase structure comprising a plurality of staircase structures stacked over the substrate*. See also element [1.A]. In particular, Kim discloses that an upper staircase structure (SS2) located on top of a

lower staircase structure (SS1), which itself is located over substrate 100, as shown in the cross-sectional view of Fig. 4B below.



Ex. 1005, Fig. 4B (annotated), 10:50-59. Thus, Kim satisfies element [2.A].

2. [2.B] “the supporting pillar extends from a top surface of the second staircase structure to a bottom surface of the first staircase structure.”

135. Kim discloses this claim element. As discussed in connection with claim element [1.G], Kim discloses *supporting pillars* in the form of dummy structures (DS). As can be seen in the annotated version of Fig. 4B below, the dummy structures DS reach from the top of the upper stack SS2 to the bottom of the lower stack SS1 (and into the substrate 100). To reach the bottom of the lower stack SS1, Kim explains that the “lower semiconductor patterns LSP may be formed on the substrate 100 exposed through the channel holes CH and the dummy holes DH” and that “[t]he lower semiconductor patterns LSP may fill lower regions of the

Kim's *supporting pillars* (dummy structures DS) extend to the *bottom surface* of SS1.



Id., Fig. 4B (annotated), 9:30-34. Thus, Kim satisfies element [2.B].

C. Claim 3

claim 3 below.

1. [3.A] “the supporting pillar and the semiconductor channel comprise same filling layers; and”

filling layers refer to the material(s) located inside the etched holes that actually form

the *supporting pillar* and *semiconductor channel*. Kim discloses that “the vertical dummy structures and the vertical channel structures may include the identical layers in some embodiments.” Ex. 1005, 9:36-38; *compare id.*, 7:16-19 (“Each of the vertical structures VS may include a vertical insulating layer VP, an upper semiconductor pattern USP, a lower semiconductor pattern LSP, and a filling insulation pattern VI”) and 9:32-36 (“Each of the dummy structures DS may include a vertical insulating layer VP, an upper semiconductor pattern USP, a lower semiconductor pattern LSP, and a filling insulation pattern VI, like the vertical structure VS”).

138. Thus, Kim satisfies claim element [3.A].

2. [3.B] “the supporting pillar and the semiconductor channel are each filled with at least one of a charge trapping film, a semiconductor channel film, and a dielectric core.”

139. Kim discloses, or renders obvious, this claim element. For ease of analysis, I break up this element in three sub-parts, each of which I discuss below. Because Kim discloses that its dummy structure DS (the *supporting pillar*) and vertical structure VS (the *semiconductor channel*) may be made with identical layers, I discuss the sub-elements below in the context of Kim’s vertical structures VS, but the analysis applies to both. Ex. 1005, 9:32-38.

a. Charge trapping film

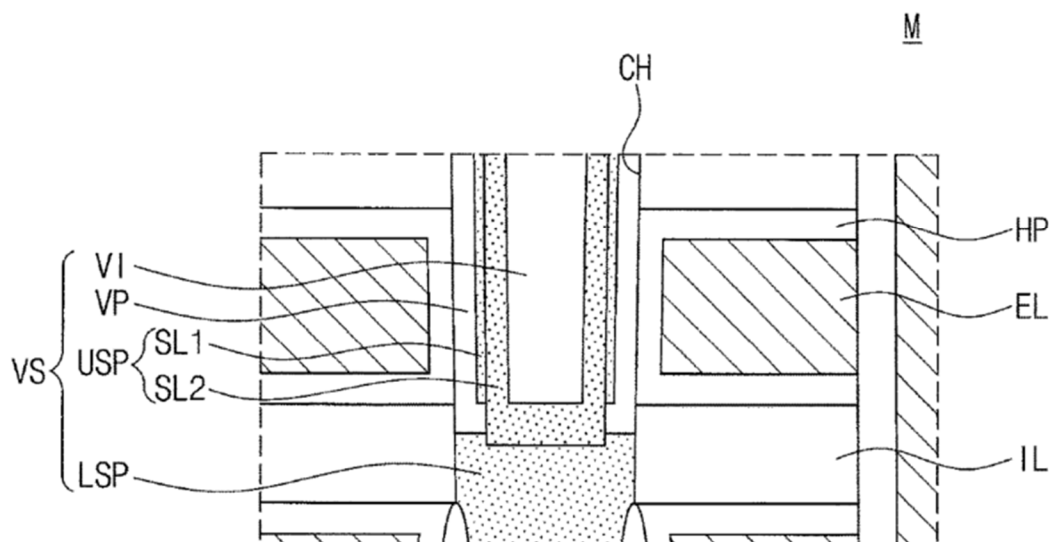
140. Kim discloses that its vertical structures (and by extension its dummy structures) can be filled with a *charge trapping film*. Before examining Kim, the '031 Patent provides some useful context on this topic. In particular, the '031 Patent explains that

In some embodiments, *a charge trapping film 416* (e.g., or sacrificial film) is deposited over the sidewall of channel holes and pillar holes 309. Charge trapping film 416 can include one or more block *dielectric layers over the sidewall of channel hole* to insulate other layers in the channel hole from staircase structure 303. Charge trapping film 416 can also include *a storage unit layer (memory layer) over* and surrounded by the block dielectric layers for trapping charges and forming a plurality of charge storage regions along the z axis. Charge trapping film 416 can also include *a tunneling layer (e.g., tunneling dielectric)* over and surrounded by the memory layer. Charge tunneling can be performed through the tunneling layer under a suitable electric bias.

Ex. 1001, 15:44-57 (emphasis added); *see also id.*, Fig. 4, 16:17-20 (storage unit layer “can include a charge trapping material (e.g. silicon nitride).”). The '031 Patent further discloses that the tunneling layer “can include silicon oxide, silicon nitride, silicon oxynitride, dielectric metal oxides, dielectric metal oxynitride, dielectric metal silicates, alloys, and/or other suitable materials.” *Id.*, 16:24-28.

141. Kim discloses the same charge trapping film as the '031 Patent. To begin, Kim discloses that its 3D memory may be NAND flash memory where the memory cells/strings formed by the vertical structures VS have a “data storage layer.” Ex. 1005, 8:23-29. Kim’s data storage layer may be comprised of “a tunnel insulating layer, a charge storage layer, and a blocking insulating layer.” *Id.*, 8:30-33. “The tunnel insulating layer may be in direct contact with the upper semiconductor pattern USP” and “[t]he blocking insulating layer may be in direct contact with the electrode EL.” *Id.*, 8:33-36. Kim further discloses that “[t]he charge storage layer may be disposed between the tunnel insulating layer and the blocking insulating layer.” *Id.*, 8:36-38. A cross-sectional depiction of this layering is illustrated in Kim Fig. 5A below.

FIG. 5A



Id., Fig. 5A (partial).

142. Kim goes on to explain that its charge storage layer “may include a silicon nitride layer, a silicon oxynitride layer, or a silicon-rich nitride layer.” Ex. 1005, 8:47-49. Silicon nitride is one of the examples in the ’031 Patent of a charge storage layer. *See* Ex. 1001, 16:17-20.

143. Kim further states that its tunnel insulating layer “may include a material of which an energy band gap is greater than that of the charge storage layer” and “may include at least one of a high-k dielectric layer (e.g., an aluminum oxide layer or a hafnium oxide layer) or a silicon oxide layer.” Ex. 1005, 8:42-47. Various of these exemplary materials for Kim’s tunnel insulating layer are the same as the materials set forth by the ’031 Patent. *See* Ex. 1001, 16:24-28; *see also id.*, 15:44-57.

144. Collectively, the layers forming Kim’s “data storage layer” would have been understood to comprise *a charge trapping film*. Indeed, Kim itself explain that “[t]he charge storage layer may be disposed between the tunnel insulating layer and the blocking insulating layer” such that “[d]ata stored in the data storage layer may be changed using a Fowler-Nordheim tunneling effect induced by a difference in voltage between the electrode EL and the upper semiconductor pattern USP.” Ex. 1005, 8:38-41. Fowler-Nordheim tunneling has been known and used (*i.e.*, for decades) by POSITAs to store and remove charge (*viz.*, from a charge storage layer that is adjacent to an insulator). Typically, Fowler-Nordheim tunneling applies a

relatively strong electric field across an insulating material to store/remove charge that adjusts/changes the threshold voltage of a transistor even when the strong electric field is no longer present.

145. Also note that Figures 4-5 of Kim disclose a continuous charge storage layer. This confirms a charge-trap memory. Ex. 1020, 105. In contrast, conductive floating gate cells have separated gates, because as I explain in Section VIII.A, the gates are conductive and the charge would be shared among the gates unless they were separated. *Id.*, 145.

146. Thus, when Kim discusses Fowler-Nordheim tunneling, a POSITA would understand that Kim's disclosure discussed above to be *a charge trapping film*.

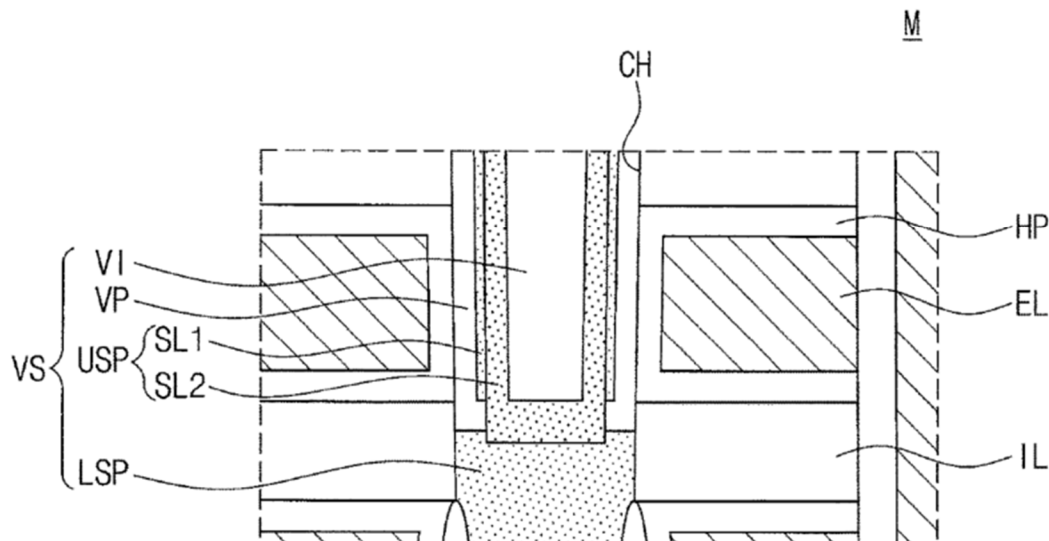
b. Semiconductor channel film

147. Kim discloses this claim element. The '031 Patent states that "a semiconductor channel film 417 can be formed over the charge trapping film in the channel holes and pillar holes," and can include "one or more layers of any suitable semiconductor materials such as silicon, silicon germanium, germanium . . . and/or other suitable semiconductor materials." Ex. 1001, 16:32-38.

148. Kim discloses using various of the same materials as the '031 Patent as part of Kim's vertical structures VS. For example, as illustrated in Kim Fig. 5A below, Kim discloses an upper semiconductor pattern USP, including first and

second semiconductor patterns SL1 and SL2, that “may cover an inner side wall of the vertical insulating layer VP [a component of the data storage]” (Ex. 1005, 7:21-23), and “may include *silicon (Si), germanium (Ge) or a mixture thereof*” (*id.*, 7:54-57) (emphasis added).

FIG. 5A



Id., Fig. 5A (partial).

149. A POSITA would have understood materials such as silicon and germanium (or a combination of the two) as used in Kim’s vertical structures VS to comprise a *semiconductor channel film*, especially considering that the same materials are expressly recited and used in the ’031 Patent’s semiconductor channel. *See* Ex. 1001, 16:32-38, 15:44-57.

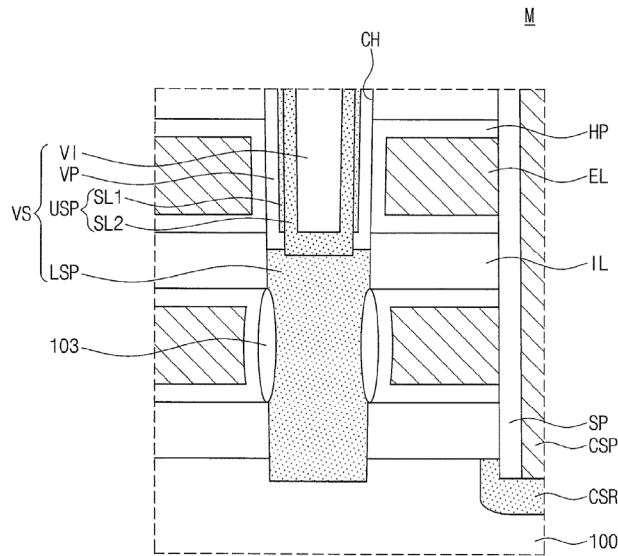
c. Dielectric core

150. Kim discloses, or renders obvious, this claim element. The '031 Patent discloses that “a dielectric core 418 can be formed by depositing a suitable dielectric material over semiconductor channel films in channel holes and pillar holes,” that “[d]ielectric core 418 can fill the space at the center of the channel hole and the pillar hole,” and that the “[d]ielectric core 418 can include a suitable dielectric material such as silicon oxide.” Ex. 1001, 16:49-55.

151. Kim discloses the same *dielectric core*. Kim Fig. 5A (reproduced below) illustrates an insulation pattern VI that fills the center of the vertical structure. Ex. 1005, 12:1-3. This same is true for Kim’s dummy structure. *Id.* Kim expressly discloses that “[a]n inner space of the second semiconductor pattern SL2 [a component of upper semiconductor pattern USP], may be filled with the filling insulation pattern VI.” *Id.*, 7:39-41. A POSITA would have understood, and at least found obvious, that Kim’s “insulation pattern” at the center of the hole is a *dielectric core*. Kim describes other “insulating” features expressly as being made with dielectric materials, and thus it would have been understood that other similar insulators were made with dielectric materials. *Id.*, 6:59-61, 8:42-51. Also note that the concept of using a core filler was conventional in 3D NAND. Ex. 1020, 105. And it was conventional to use “a core filler dielectric” as this core filler in charge-trap memory cell strings. Ex. 1016 (U.S. Pat. No. 9,142,302), 7:33-52. I also note

that Kim already discloses depositing dielectric materials into pillar holes, which both illustrates its ease and that Kim would have been understood to, likewise, deposit such a dielectric material to create the core filler. Ex. 1005, 8:42-51. Finally, the use of dielectric materials, such as silicon oxide, was advantageous because of its compatibility with semiconductor processing. For this application, the silicon dioxide will be deposited by chemical vapor deposition (CVD) or plasma enhanced CVD (PECVD), rather than being thermally grown. This is because the silicon substrate is not available for thermal oxidation at this stage of the fabrication. CVD or PECVD by the reaction of precursors such as silane (SiH_4) and oxygen requires lower temperatures than thermal oxidation, which is a bonus. CVD silicon dioxide is chemically very stable and provides excellent refilling properties of the core, without leading voids which could have deleterious effects such as trapping contaminants. Its location at the center of the channel make it a *core* and would be understood to be a *dielectric*.

FIG. 5A



Id., Fig. 5A.

152. Thus, Kim discloses a *dielectric core*.

D. Claim 4

153. Claim 4 is a dependent claim that depends on claim 2 (which in turn depends on claim 1). I address how Kim satisfies the three additional elements of claim 4 below.

1. [4.A] “the supporting pillar and the semiconductor channel are filled with different filling layers; and”

154. Kim discloses this claim element. In contrast to claim element [3.A] which requires that *the supporting pillar and the semiconductor channel comprise [the] same filling layers*, claim element [4.A] requires *different filling layers*. Kim discloses embodiments in which “[a] layer or component of each of the dummy structures DS [*supporting pillar*] may be different from the layer(s) or component(s)

of each of the vertical structures VS [*semiconductor channel*].” Ex. 1005, 13:28-33.

Thus, Kim meets claim element [4.A].

155. As I discuss below, it would have been obvious for the Kim supporting pillar to be made with completely different materials than the channel, namely, with a metal core.

2. [4.B] “the supporting pillar is filled with at least one of an insulating material and a pillar-support material surrounded by the insulating material,”

156. Kim renders obvious this claim element. As a reminder, Kim’s dummy structure DS is the claimed *supporting pillar*. Kim further discloses embodiments in which the dummy structures DS include a “dummy pattern,” which Kim describes as “[a] layer or component ... [that] may be different from the layer(s) or component(s) of each of the vertical structures VS.” Ex. 1005, 13:28-33. A POSITA would have understood that Kim’s dummy structures could include a conductive core as the supporting material and that doing so would have been obvious. Consider, for example, the teachings of Ex. 1012 (U.S. Pat. No. 9,768,186), which describes “pillar-shaped support members 107” that includes an “electrically conductive core material 111” which “may comprise any suitable electrically conductive material, such as a metal material (e.g., a metal or metal alloy, including a metal nitride or metal silicide).” Ex. 1012, 4:60-5:12. This is not a one-off example, but represents the knowledge of a POSITA. This is further confirmed by

Tessariol, which discloses that supporting pillars may be either conductive vias or dummy versions of the conductive vias. Ex. 1006, [0037], [0038], [0041].

157. Accordingly, it would have been obvious simply to use conductive vias (which have an insulating liner and conductive core) in Kim’s dummy structures, and this would have been beneficial because the process to form them would use the same process steps as the conductive vias. In addition, because it was known, as taught by, *e.g.*, Tessariol, that supporting pillars could be either dummy support pillars (here, inactive conductive vias) or active conductive vias (here, active conductive vias), the supporting pillar as an active conductive via beneficially could serve two roles (support and interconnect) and reduce the need for additional structures. Given the well-known structural and electrical characteristics of common metal conductors like copper, nickel, aluminum, etc., and established fabrication techniques regarding the same in vertical structures such as contacts and vias, a POSITA would have had more than a reasonable expectation of success in using those materials as *pillar-support materials*.

3. [4.C] “and the semiconductor channel is filled with at least one of a charge trapping film, a semiconductor channel film, and a dielectric core.”

158. Kim discloses this claim element for the same reasons I explained with respect to claim element [3.B], which includes the same requirements for the *semiconductor channel*.

XIV. GROUND 2: INDEPENDENT CLAIM 1 AND DEPENDENT CLAIMS 2 AND 4-5 ARE OBVIOUS OVER TESSARIOL

159. Ground 2 demonstrates that claims 1, 2, and 4-5 are obvious over Tessariol in view of the knowledge of a POSITA.

A. Claim 1

1. [1.PRE] “A memory device comprising:”

160. I offer no opinion on whether the preamble is or is not limiting. However, if the preamble is considered to be a limitation, my opinion is that Tessariol discloses it. The BACKGROUND section of Tessariol explains that “NAND may be a basic architecture of integrated flash memory” which “may be configured in a three-dimensional arrangement comprising vertically-stacked memory cells individually comprising a reversibly programmable vertical transistor.” Ex. 1006, [0006]. Tessariol describes its embodiments in the context of “a construction 10” (*id.*, [0027]), which a POSITA would have understood to be a memory device. For example, Tessariol discloses that construction 10 may include “memory cells.” *Id.*, [0042]. One exemplary embodiment of construction 10 is a 3D NAND memory. Therefore, Tessariol discloses a *memory device* (e.g., construction 10).

2. [1.A] “a substrate;”

161. Tessariol discloses this claim element. Substrates are extremely common in semiconductor memory devices and are typically used as the base or

platform on top of which the memory is fabricated. Tessariol is no different. For example, Tessariol discloses that “construction 10 comprises a base substrate 11,” which is highlighted in Fig. 1 below in blue. Ex. 1006, [0027].

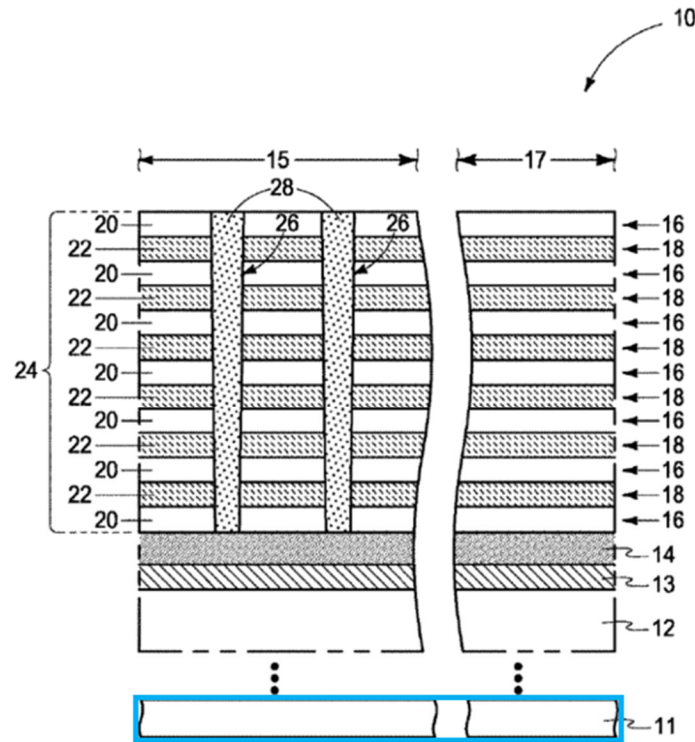


FIG. 1

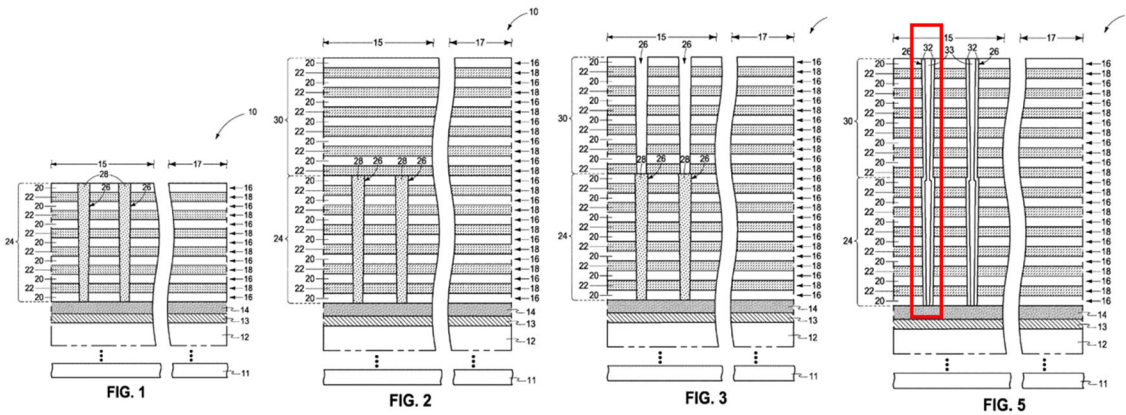
Id., Fig. 1 (annotated).

162. Thus, Tessariol discloses a *substrate* (e.g., base substrate 11).

3. [1.B] “a multiple-stack staircase structure comprising a plurality of staircase structures stacked over the substrate,”

163. Tessariol discloses, or at a minimum renders obvious, this claim element. I first address Tessariol’s disclosure of *a multiple-stack staircase structure comprising a plurality of staircase structures*. To begin, Tessariol states that its

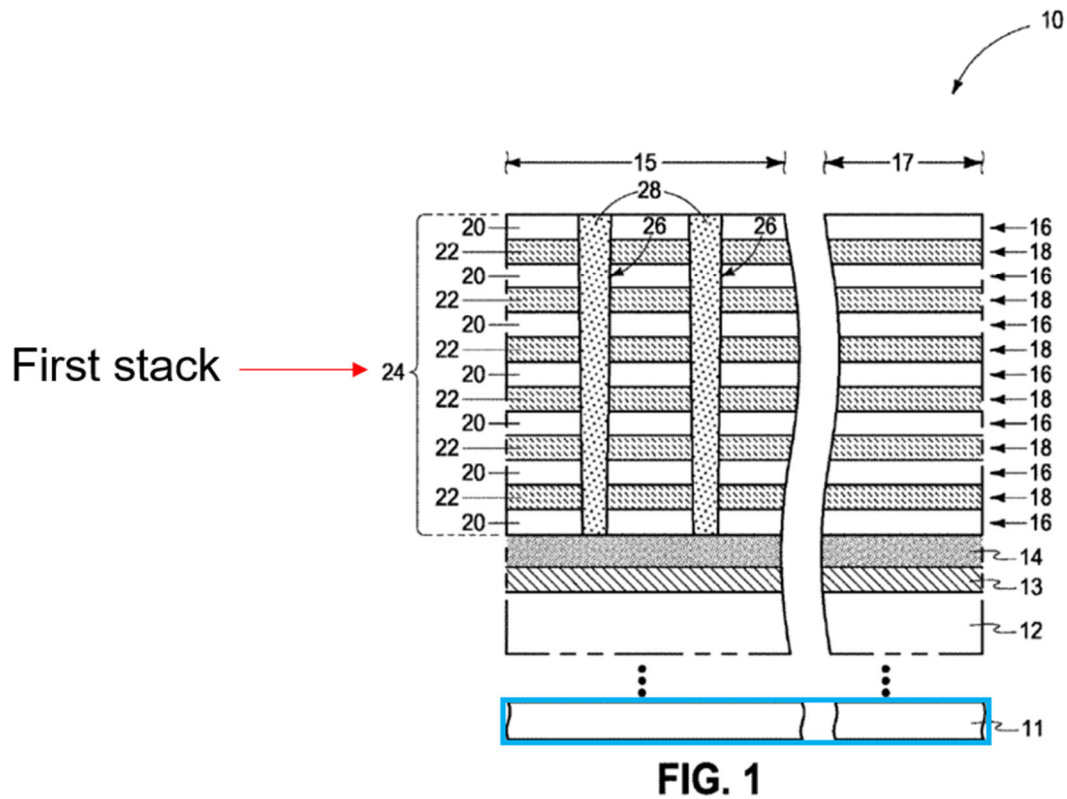
“discussion largely proceeds with a fabrication method forming two stacks.” Ex. 1006, [0028]. I observe that Tessariol Figs. 1-3 and 5 illustrate a manufacturing process in which two stacks (*viz.*, “first stack 24” and “second stack 30”) are formed, with the second stack 30 on top of first stack 24. *See, e.g., id.*, [0030]-[0032].



Id., Figs. 1-3 and 5 (annotated).

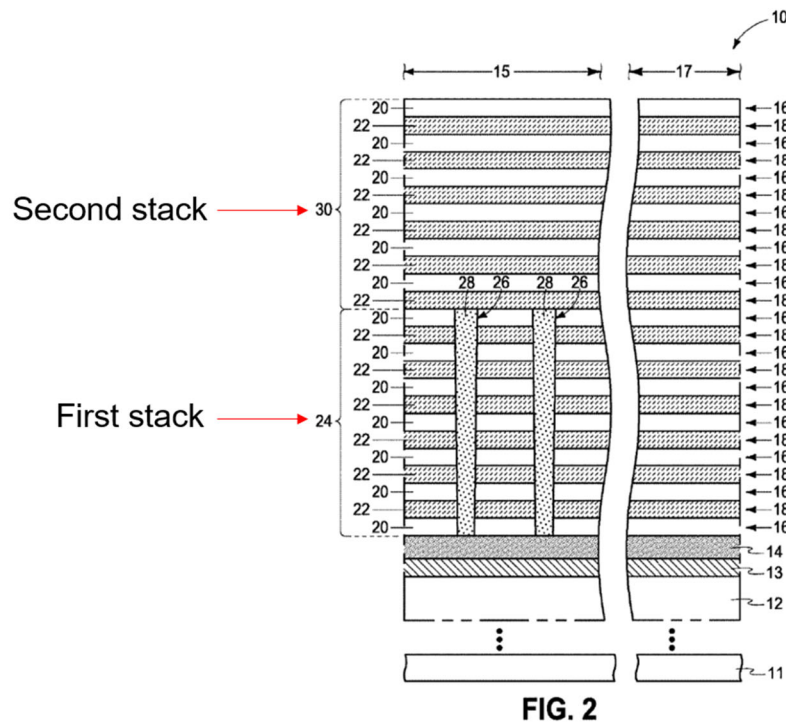
164. More specifically, Tessariol discloses that each stack includes “vertically-alternating tiers 16 and 18 of different composition first [20] and second materials [22], with the vertically-alternating tiers comprising an array portion [15] and a portion adjacent to the array portion [17].” Ex. 1006, [0029].

165. Looking at Fig. 1 in more detail, Tessariol discloses first forming “a *first stack 24* of vertically-alternating tiers 16 and 18.” Ex. 1006, [0029] (emphasis added).



Id., Fig. 1 (annotated).

166. And Fig. 2 discloses formation of “a *second stack 30* of vertically alternating tiers 18, 16, of different composition materials 22, 20 . . . over first stack 24.” Ex. 1006, [0031] (emphasis added).



Id., Fig. 2 (annotated).

167. Collectively, first stack 24 and second stack 30 form a multi-stack structure. Claim element [1.B] requires *a multiple-stack staircase structure* that is comprised of *a plurality of staircase structures*, so I address the *staircase* requirement next.

168. As shown in Fig. 2 above, Tessariol's two stacks each include a region 17. Although not shown in Fig. 2, other figures in Tessariol (such as Fig. 6 shown below) do show that region 17 has a staircase profile: "FIGS. 6 and 7 show an expanded, yet reduced-scale, version of adjacent portion 17 as comprising three stair step structures 34, 36, and 38." Ex. 1006, [0034].

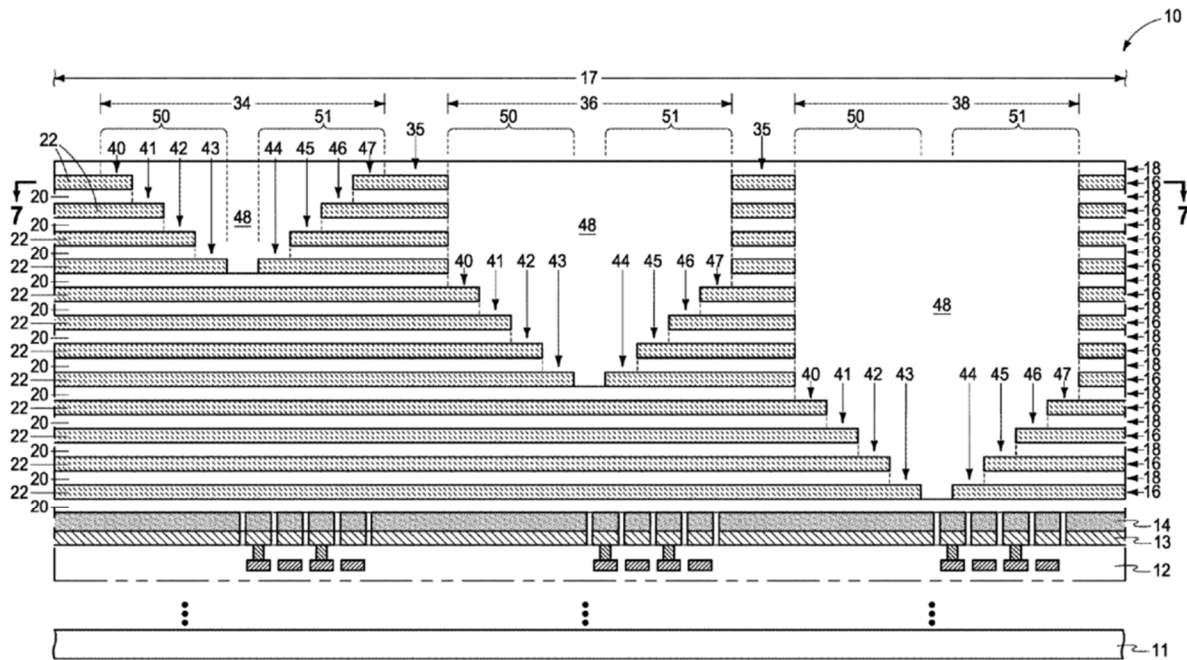


FIG. 6

Id., Fig. 6. As seen in Fig. 6 above, a staircase profile exists in both the upper stack (see region 34 on the lefthand side of Fig. 6) and the lower stack (see region 38 on the righthand side of Fig. 6). Thus, each of first stack 24 (lower stack) and second stack 30 (upper stack) have a region with a staircase profile and each stack is a *staircase structure* in its own right. Collectively, the two stacks comprise the claimed *multiple-stack staircase structure*.

169. The '031 Patent notes that “[a] ‘stack’ refers to a pile of objects, arranged along a designated direction.” Ex. 1001, 7:12-13. As discussed above, Tessariol discloses two such stacks, each of which comprises a staircase portion,

thereby forming a *multiple-stack staircase structure comprising a plurality of staircase structures*.

170. Were the Patent Owner to argue that claim 1 is limited to a single staircase portion with continuous steps spanning both stacks, Patent Owner would be incorrect because the claim language does not limit the *staircase structure* in this manner. The '031 Patent simply states that a “‘staircase structure’ or a ‘stepped cavity structure,’ or similar refer to a structure having stepped surfaces.” Ex. 1001, 9:39-41. In other words, the '031 Patent does not define *staircase structure* as only one step region per stack or to a continuous series of steps.

171. In any event, a POSITA would have understood such a staircase arrangement (*viz.*, a continuous single set of steps spanning both stack) to have been within the disclosure of Tessariol, and it certainly would have at least been obvious. More specifically, Tessariol discloses that “[a]dditionally, only one stair step structure, two stair step structures, or more than three stair step structures may be formed.” Ex. 1006, [0034]. And Tessariol further states that “[i]n one embodiment and as shown, stair step structures 34, 36, and 38 individually comprise opposing first and second sets/flights 50, 51, respectively, of steps 40-47. Alternately, by way of examples only, only one flight of steps may be formed” *Id.*, [0035].

172. My opinion is further supported by the knowledge of a POSITA, as reflected in my explanation of Ground 1 where Kim discloses two staircase portions

corresponding to two stacks. *See* §VIII.A.3. Accordingly, in view of Tessariol's option of two stair step structures and a POSITA's knowledge (*e.g.*, Kim's exemplarily two-staircase structure), it would have been obvious to employ two staircase portions, one for each stack, that each have continuous steps that connect to form a single continuous staircase profile. And such an arrangement would have been routine to implement, as Tessariol expressly recognizes that many staircase options are available and readily applicable to its invention.

173. Second, I address the claim requirement that the claimed staircase structures are *stacked over the substrate*. Tessariol discloses this. To begin, I note that the claim does not require that the *staircase regions* of the *staircase structures* be vertically aligned with one another. Rather, the '031 Patent uses "*stacked*" in this context to simply refer to the staircase structures (each of which have a staircase region) being located on top of another; it does not require that the *staircase region* of one staircase structure be located directly on top of the *staircase region* of another staircase structure. This is evident in Figure 11 of the '031 Patent:

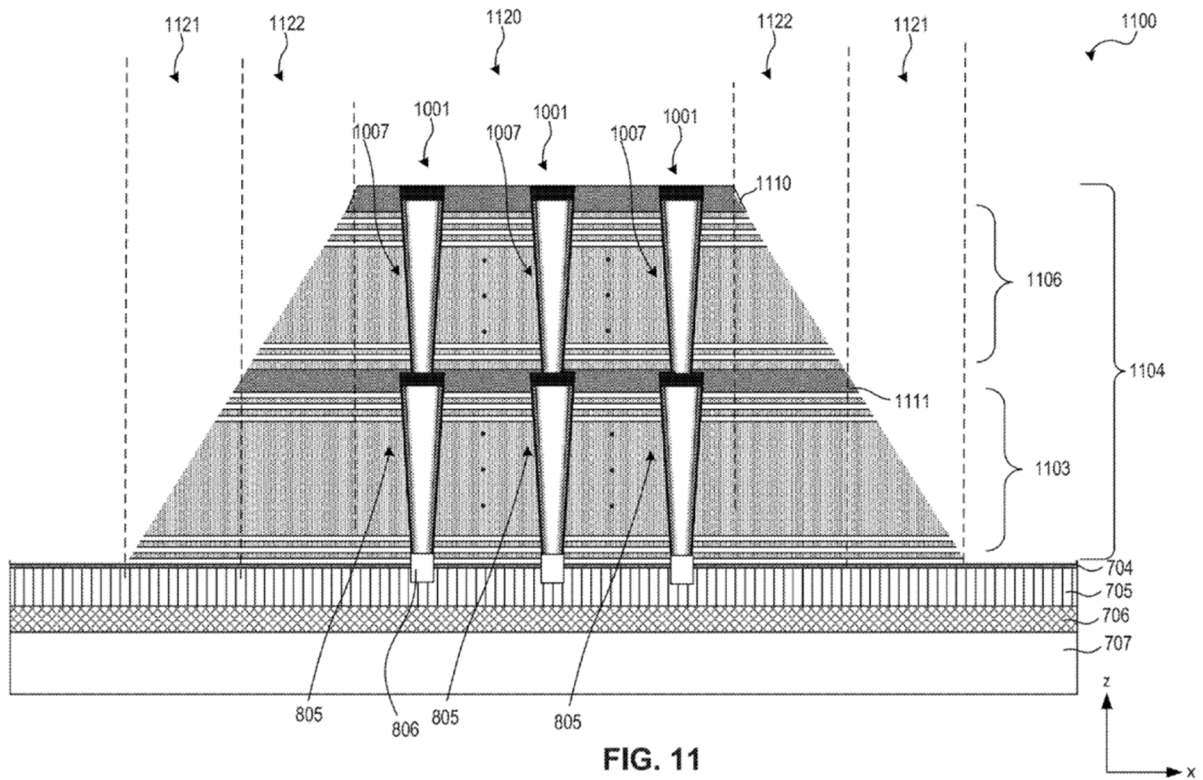


FIG. 11

Ex. 1001, Fig. 11.

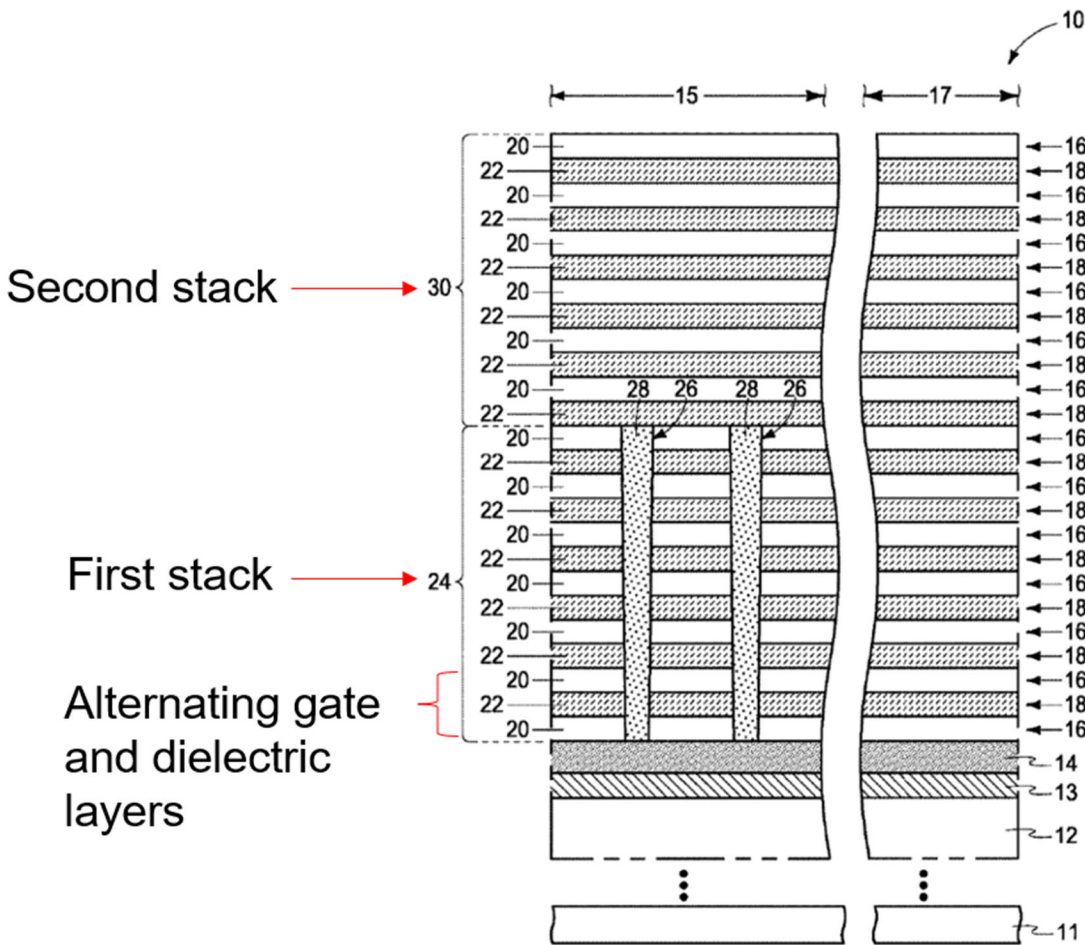
174. In the figure above, the “second staircase region 1122” is not vertically aligned with the “first staircase region 1121.” Ex. 1001, 22:27-32. But both stacks 1103 and 1106 include a staircase region and thus are staircase structures, and one staircase structure is nevertheless on top of the other. In like manner, as discussed above, Tessariol discloses the two stacks, each with a staircase structure, one on top of the other.

175. In summary, Tessariol discloses, or at least renders obvious, a *multiple-stack staircase structure* (e.g., first stack 24 and second stack 30, having staircase regions, e.g., 34, 36, 38) *comprising a plurality of staircase structures* (e.g., first

stack 24 and second stack 30, both of which have staircase regions, *e.g.*, 34, 36, 38 or the two-staircase variation) *stacked over the substrate* (*e.g.*, base substrate 11).

4. [1.C] “wherein each of the plurality of staircase structures comprises a plurality of conductor layers, wherein each of the plurality of conductor layers is located between two insulating layers;”

176. Tessariol discloses this claim element. In particular, Tessariol discloses that the first and second stacks 24 and 30 (including their respective stair step regions 34, 36, and 38) are formed from “[v]ertically-alternating tiers 16 and 18 of different composition first and second materials 20 and 22.” Ex. 1006, [0029]. Tessariol goes on to explain that “[i]deally, materials 20 and 22 are of the same relative compositions with respect to one another in first stack 24 and second stack 30.” *Id.*, [0031]. Tessariol further explains that “[f]irst material 20 comprises an insulative material” and “[s]econd material 22 . . . may comprise any one or more of conductive, semiconductive, and insulative materials. *Id.*, [0029]. Alternating layer of conductive material (which form the gate lines) and insulating material are illustrated in Fig. 2 below.



First stack

Alternating gate and dielectric layers

FIG. 2

Id., Fig. 2 (annotated).

177. I note here that Tessariol discloses that, in some embodiments, layers 22 comprise a sacrificial material and are subsequently etched away and replaced with gate layers 72. Ex. 1006, [0041] (“FIGS. 11-13 show the void space (not shown) resulting from etching away material 22 (not shown) as having been filled with conductive material 72 (e.g., metal material). Steps 40-47 now comprise

conductive steps due to presence of conductive material 72 and that are at least partially elevationally separated from one another by insulative material 20.”).

178. Thus, Tessariol discloses a *plurality of staircase structures* (first stack 24 and second stack 30 with respective staircase regions, e.g., 34, 36, 38 or two-staircase variation) *comprising a plurality of conductor layers wherein each of the plurality of conductor layers* (layers 18 composed of second material 22 (or material 72 in embodiments where material 22 is a sacrificial material)) *is located between two insulating layers* (layers 16 composed of first material 20).

5. [1.D] “a filling structure surrounding the multiple-stack staircase structure;”

179. Tessariol discloses, or at least renders obvious, this claim element. I discussed the *multiple-stack staircase structure* in Tessariol above in claim element [1.C]. With respect to the claim *filling structure*, Tessariol discloses (as shown in Figure 6 below) that “[a]n insulating material 48 (e.g., silicon dioxide and/or silicon nitride) is above steps 40-47.” Ex. 1006, [0034].

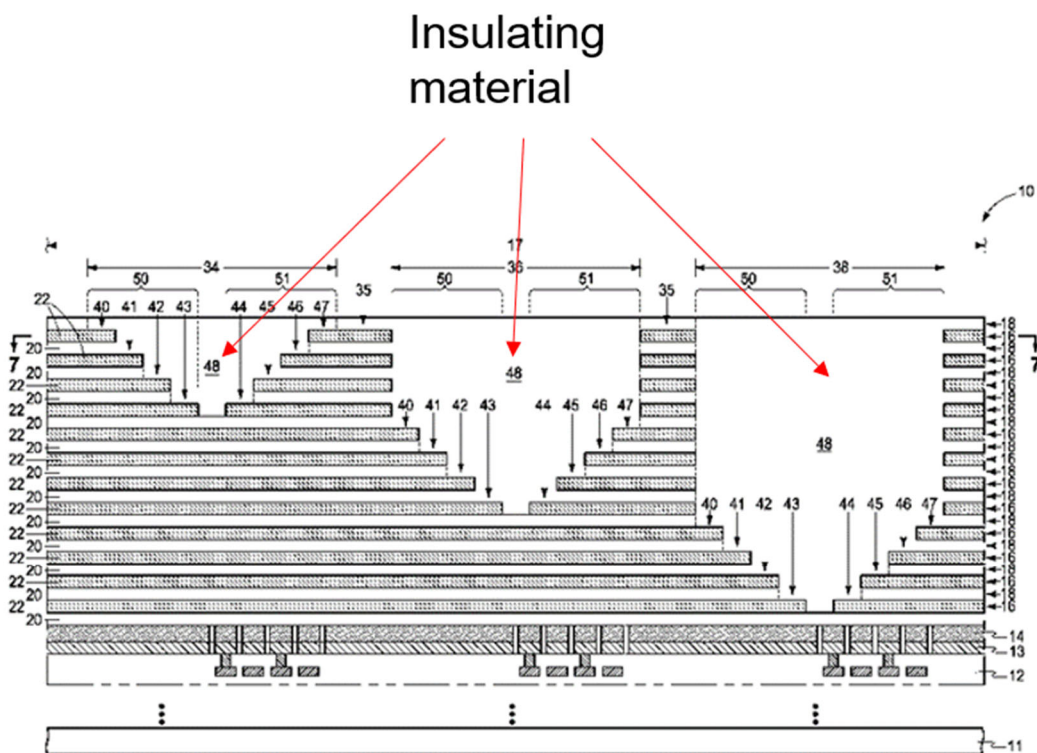


FIG. 6

Id., Fig. 6 (annotated).

180. And Tessariol further discloses depositing “dielectric material 74” around the staircase structures, as shown in Fig. 11 below. Ex. 1006, [0043].

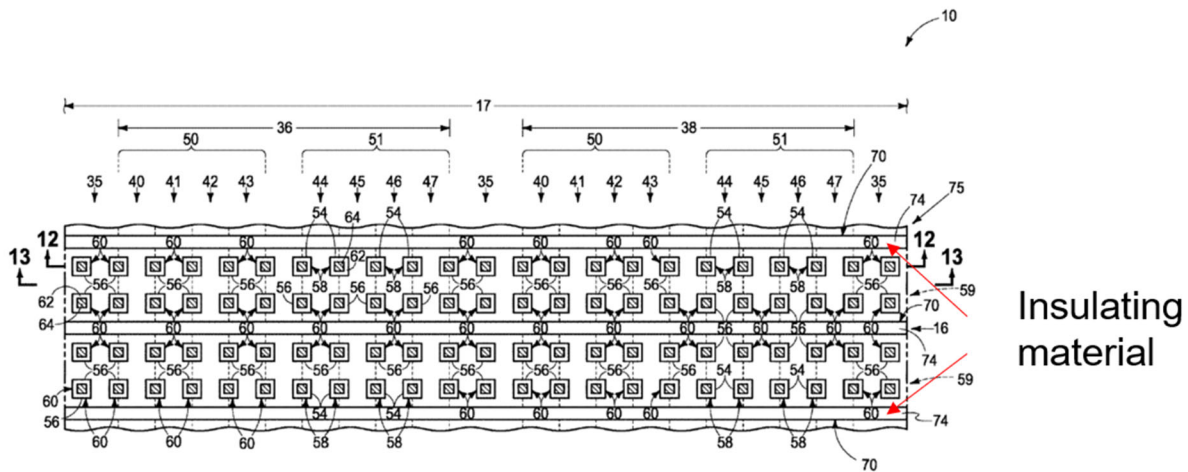


FIG. 11

Id., Fig.11 (annotated). I note that the dielectric material 74 in Tessariol may extend through the array region. *Id.*, [0043].

181. Tessariol also discloses an additional dielectric filling structure (86). Ex. 1006, [0046] (“Insulator material 86 (e.g., silicon nitride and/or silicon dioxide) is shown surrounding components 69, 82, 81, and 84.”). This insulator material 86 encases the entire stack structure to provide a region for metal layer connections to the lower layers:

183. Based on the knowledge of a POSITA as reflected, *e.g.*, in the Kim reference, a POSITA would have understood, or at least found obvious, that Tessariol's "dielectric material 74" and "insulator material 86" is like Kim's "filling insulating layer 110," and "may be disposed on the substrate 100 and may cover" the entire stack structure, and "may have a planarized top surface." Ex. 1005, 9:53-56; *see also id.*, 11:11-21 ("Referring to FIGS. 3 and 10, a filling insulation layer 110 may be formed on an entire top surface of the substrate 100 to cover the mold structure MT."). This planarized top surface, as shown above in Tessariol's Figures 17-18, creates the interface between the lower layers and the upper metal layers, and interconnects are formed through to connect upper-level components to the lower-layer device. This was a conventional, routine insulating technique in chip fabrication that electrically isolates the structure. Such a step would encase all sides of the memory device, as in Kim. Again, such filling insulators are understood to surround the stack structures to create a planar surface for the upper-level metal layer. Ex. 1023, 14.

184. I note that the figures in Tessariol do not show the outer ends/sides of the device. *E.g.*, Ex. 1006, [0008] ("FIG. 1 is a diagrammatic cross-sectional view of a portion of a substrate construction in process in accordance with an embodiment of the invention."). Nonetheless, for the reasons that I explain above, a POSITA

would have understood that filling structures 48 and 86 encase the entire array and staircase regions.

185. In summary, Tessariol discloses (or at least renders obvious) a *filling structure* (e.g., insulating material 48, dielectric material 74, and insulator material 86) *surrounding the multiple-stack staircase structure* (e.g., first stack 24 and second stack 30, having staircase regions, e.g., 34, 36, 38 or a two-staircase variation).

6. [1.E] “a semiconductor channel extending through the multiple-stack staircase structure,”

186. Tessariol discloses this claim element. This is shown, for example, in Tessariol Fig. 5 below. With reference to Fig. 5, Tessariol explains that “transistor material 32 has been formed in individual channel openings 26 in each of first stack 24 and second stack 30. Such may comprise, for example and in order of deposition, a charge-blocking material (e.g., silicon dioxide and/or silicon nitride), a charge-storage material (e.g., floating gate material such as doped or undoped silicon, etc. or charge-trapping material such as silicon nitride, metal dots, etc.).” Ex. 1006, [0033].

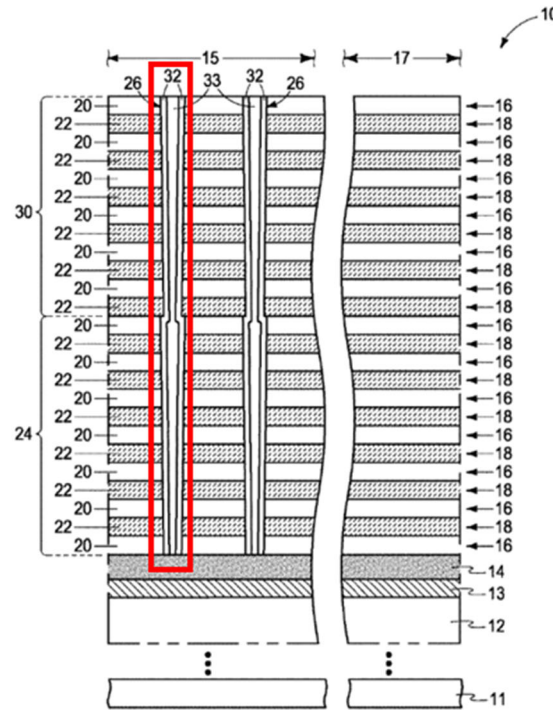


FIG. 5

Id., Fig. 5 (annotated).

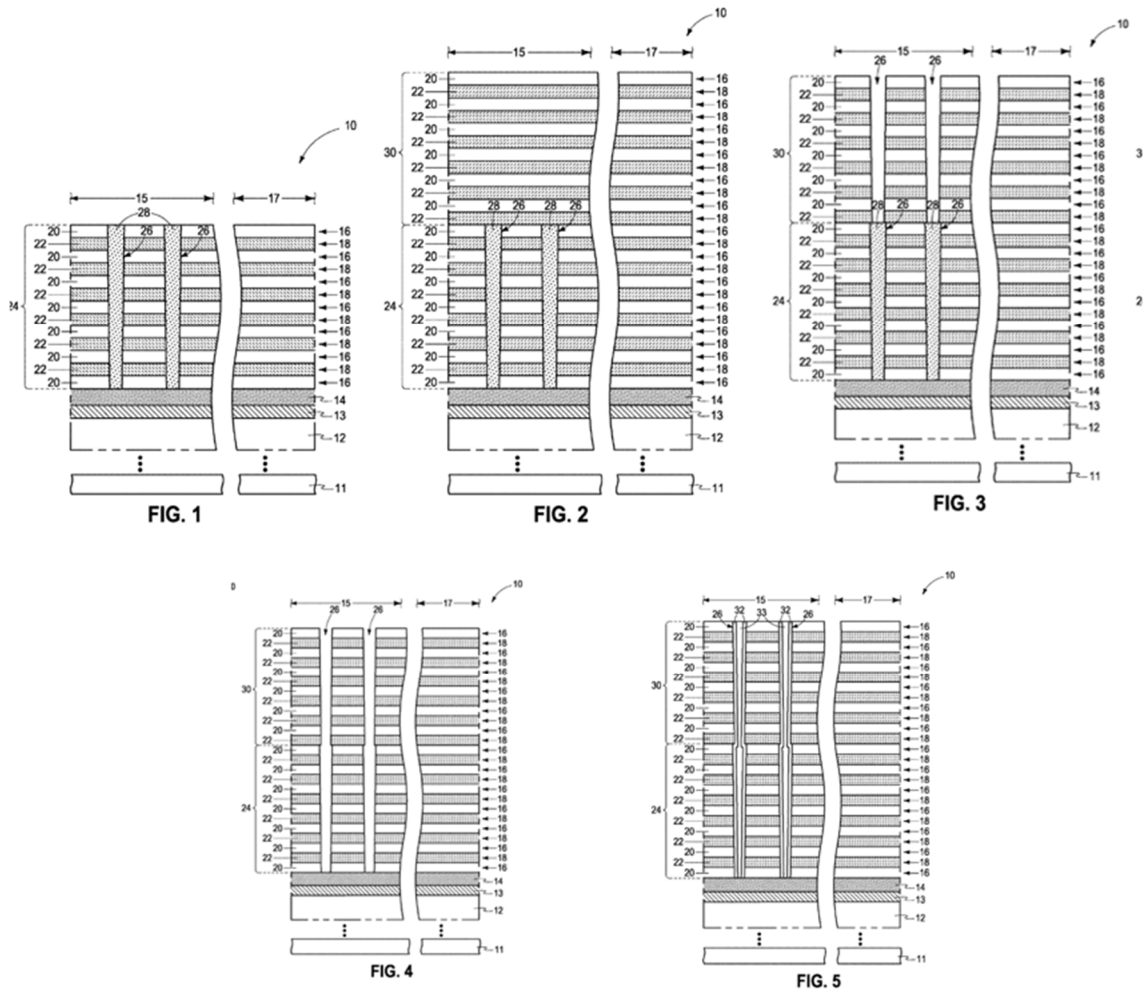
187. A POSITA would have understood that the structure of Fig. 5 highlighted above is a *semiconductor channel* such as is commonly used, *e.g.*, in charge-trap memory strings. Moreover, as is apparent in Fig. 5 above, Tessariol discloses that the *semiconductor channel* extends *through the multi-stack structure* (*i.e.*, all the way through the first stack 24 and second stack 30).

188. In summary, Tessariol discloses a *semiconductor channel* (*e.g.*, within channel opening 26, a transistor material 32) *extending through the multiple-stack staircase structure* (*e.g.*, first stack 24 and second stack 30, having staircase regions, *e.g.*, 34, 36, 38).

7. [1.F] “wherein the semiconductor channel comprises unaligned sidewall surfaces; and”

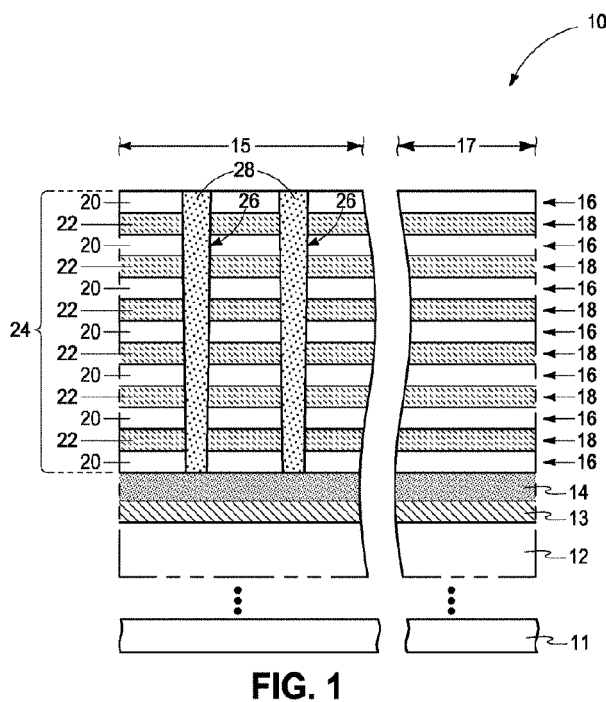
189. Tessariol discloses, or at least renders obvious, this claim element. To begin, as the series of Figs. 1-5 reproduced below illustrate, Tessariol discloses a two-step etch process that is used to form the channel structures in channel openings

26.



Ex. 1006, Figs. 1-5.

190. In Fig. 1, Tessariol discloses the formation of channel openings 26 in the first stack 24. Ex. 1006, [0030]. At this point, the second stack 30 has not yet been formed. The channel openings 26 are then filled with a second sacrificial material 28. *Id.* As reflected in Fig. 1 (see enlarged version below), channel openings 26 in first stack 24 progressively taper in diameter as they approach base substrate 11. This is consistent with typical semiconductor fabrication etch processes which have an anisotropy factor less than 1, as described earlier. *See supra* §VIII.B.



Ex. 1006, Fig. 1.

191. The second stack 30 is then formed on top of the first stack 24 (*see* Fig. 2). As shown below in Fig. 3, following the formation of second stack 30 over first

stack 24, Tessariol discloses forming channel openings 26 in second stack 30. Ex. 1006, [0032].

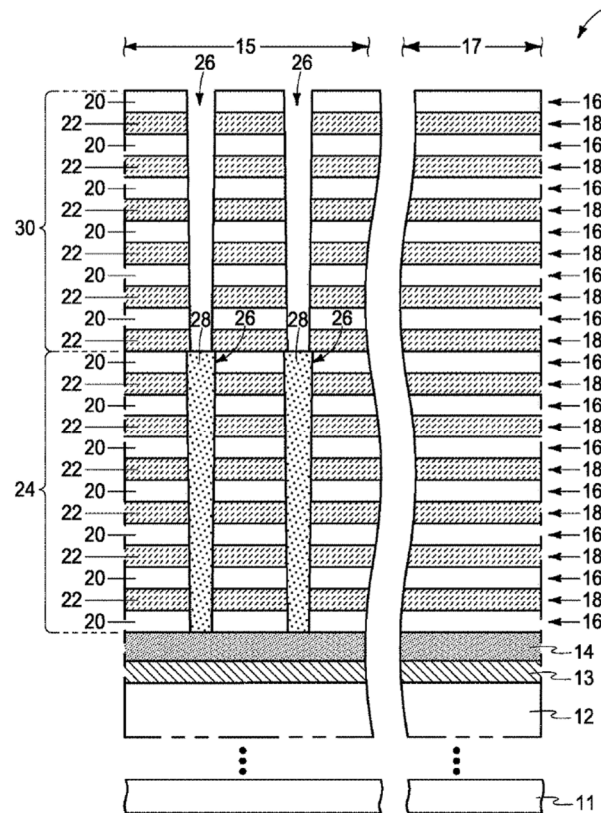
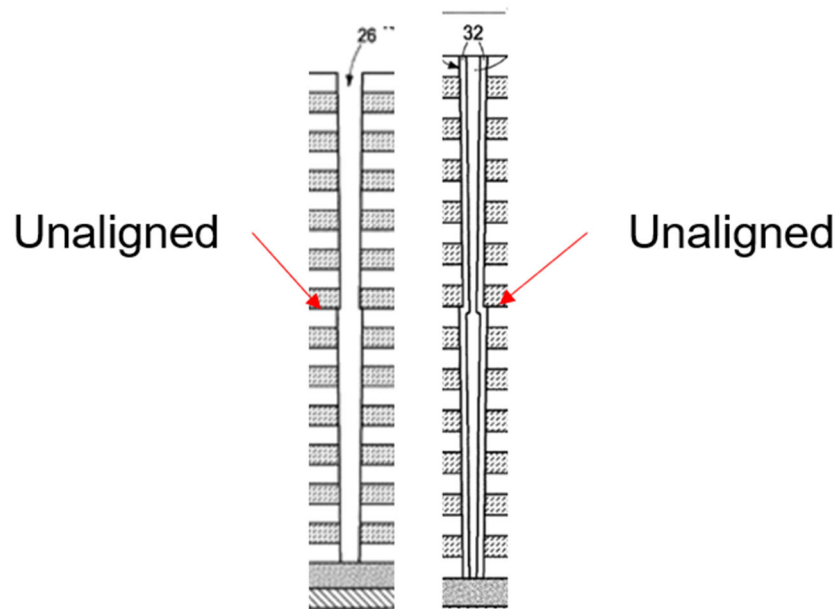


FIG. 3

Id., Fig. 3.

192. The channel openings 26 in second stack 30 (as can be seen in Fig. 3) progressively taper in diameter from top toward the bottom. As a result of processing tolerances and imperfection (as well as the tapered profile), the channel openings 26 in upper stack 30 become misaligned with channel openings 26 in first stack 24. Next, Tessariol discloses removing the “second sacrificial material 28 . . . from channel opening 26 in first stack 24 through channel openings 26 in second

stack 30.” Ex. 1006, [0032]. The resulting joined channel openings 26 of first and second stacks 24 and 30 have unaligned sidewalls as can be seen in the partial expanded views of Tessariol Figs. 4 and 5 below. The misaligned sidewalls remain in place after the channel is completely formed. *Id.*, [0034].



Id., Figs. 4-5 (partial and annotated).

193. In summary, Tessariol discloses that the *semiconductor channel comprises unaligned sidewall surfaces* (e.g., sidewalls of transistor material in channel holes 26).

194. If Patent Owner contends that Tessariol’s disclosure is lacking because it does not explicitly use the term “unaligned,” Tessariol at least renders obvious “unaligned sidewalls” in view of a POSITA’s knowledge concerning two-step etch processes. *See* §VIII.B. The knowledge of a POSITA is reflected, for example, by

the Kim reference, which discloses a process (just like Tessariol) that etches separate first channel holes (CH1) and second channel holes (CH2). Ex. 1005, 11:49-50. Kim discloses that this results in misaligned channel holes. See §XIII.A.6. In view of a POSITA's knowledge as reflected in Kim and §VIII.B, it would have been obvious that Tessariol results in unaligned channel holes.

8. [1.G] “a supporting pillar extending through at least one of the multiple-stack staircase structure and the filling structure,”

195. Tessariol discloses this claim element. For example, Tessariol discloses “dummy-structure openings 56” that are “formed through insulating material 48 [filling structure] and vertically-alternating tiers 16 and 18 in adjacent portion 17.” Ex. 1006, [0037]. Dummy-structure openings 56 extend through the insulating layer 86. *Id.*, Fig. 16. Tessariol also discloses via openings 54. *Id.*, [0037]. Subsequently, dummy structures 60 are “formed within dummy openings 56, thereby also individually extending elevationally through ... vertically-alternating tiers 16, 18.” *Id.*, [0038]. And vias 58 are formed in the via openings. *Id.*

196. Tessariol's operative vias 58 and dummy structures 60 are both *supporting pillars*. In particular, Tessariol discloses that alternating layers 16 and 18 are “elevationally supported and prevented from collapsing within array portion 15 by transistor material 32 *and by both dummy-support structures 60 and*

operative conductive vias 58 within the stair step structures in adjacent portion 17.”

Id., [0041] (emphasis added). Tessariol further discloses that ““a dummy structure” refers to a structure which is used to mimic a physical property of another structure (e.g., presence, or ***physical load-carrying supporting ability*** of an operative structure) and which may comprise a circuit inoperable electrical dead end (e.g., is not part of a current flow path of a circuit even if conductive.)” *Id.*, [0068] (emphasis added). Fig. 9, reproduced below, illustrates an exemplary dummy structure. As can be seen, it extends through both stacks (*i.e.*, ***the multiple-stack staircase structure***).

Dummy structure 60

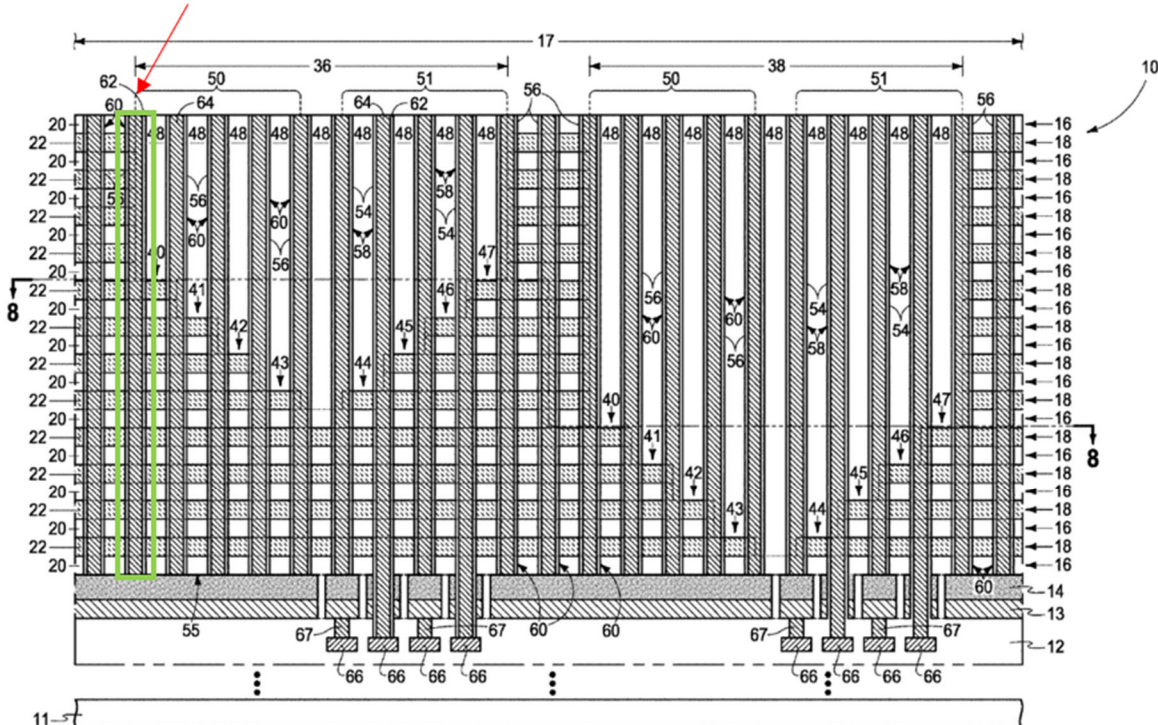


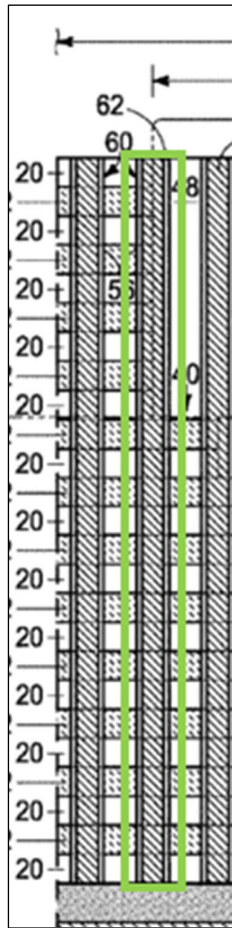
FIG. 9

Id., Fig. 9 (annotated).

197. In summary, Tessariol discloses a *supporting pillar* (e.g., dummy structures 60 and operative vias 58) *extending through at least one of* [in fact, both] *the multiple-stack staircase structure* (e.g., first stack 24 and second stack 30, having staircase regions, e.g., 34, 36, 38) *and the filling structure* (e.g., portions of the insulating material 48, dielectric material 74, and insulator material 86).

9. [1.H] “wherein the supporting pillar comprises aligned sidewall surfaces.”

198. Tessariol discloses, or at least renders obvious, this claim element. In contrast to Tessariol’s channel openings 26 (which are formed by a two-step etch process), Tessariol discloses that dummy structure openings 56 and via openings 54 are formed by a single etch step: “dummy-structure openings 56 and via openings 54 are formed using a single masking step (e.g., using masking material [not shown] formed atop structure 10).” Ex. 1006, [0037]. The dummy structures 60 have aligned sidewalls as shown in Fig. 9 below. This is consistent with conventional one-step etch processes. *See* §VIII.B.



Ex. 1006, Fig. 9 (partial, annotated). As reflected in the full version of Fig. 9, the conductive vias 58 also include the same aligned sidewall profile. *Id.*, [0038]-[0039].

199. To the extent that Patent Owner argues Tessariol's disclosure is lacking because it does not explicitly use the word "aligned," Tessariol would at least render obvious *aligned sidewalls* in view of a POSITA's knowledge of single-step etching. For example, Kim is representative of the knowledge of a POSITA in this regard and discloses a manufacturing method wherein "the dummy holes DH may be formed

by one-step etching process after the formation of the lower mold structure MT1 and the upper mold structure MT2 [(stack structure ST)].” Ex. 1005, 12:58-67. Kim further discloses that “[a] dummy structure . . . DS may be provided in each of the dummy holes DH” (*id.*, 9:20-24) and that the vertical dummy structures DS formed in the holes “have a side wall with a planar profile at the level where the upper structure meets the lower structure” (*id.*, 1:51-53). *See also* §VIII.B. Given that Tessariol uses the same basic process for forming dummy and via holes as Kim, a POSITA would have understood Tessariol to disclose aligned dummy pillars and aligned conductive vias, and/or certainly would have found it obvious.

200. In summary, Tessariol discloses the *supporting pillar comprises aligned sidewall surfaces* (e.g., dummy structures 60 and operative vias 58).

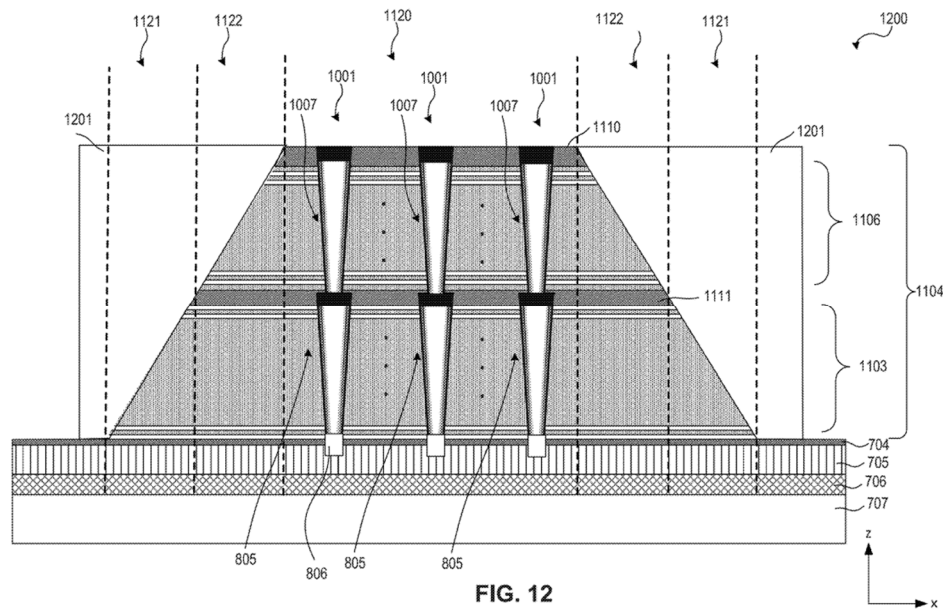
B. Claim 2

201. Claim 2 is a dependent claim that depend on claim 1. I address how Tessariol satisfies both the additional elements of claim 2 below.

1. [2.A] “the multi-stack staircase structure comprises a first staircase structure over the substrate and a second staircase structure over the first staircase structure; and”

202. Tessariol discloses this claim element for the reasons I discuss in connection with claim elements [1.A] and [1.B]. Claim element [2.A] uses the term *over*, but this does not mean the claim requires the *staircase portions* of the first and second staircase structures to be on top of the other. This is confirmed, e.g., by Fig.

12 of the '031 Patent, which is pasted below and shows that the *staircase portions* do not overlap one another.

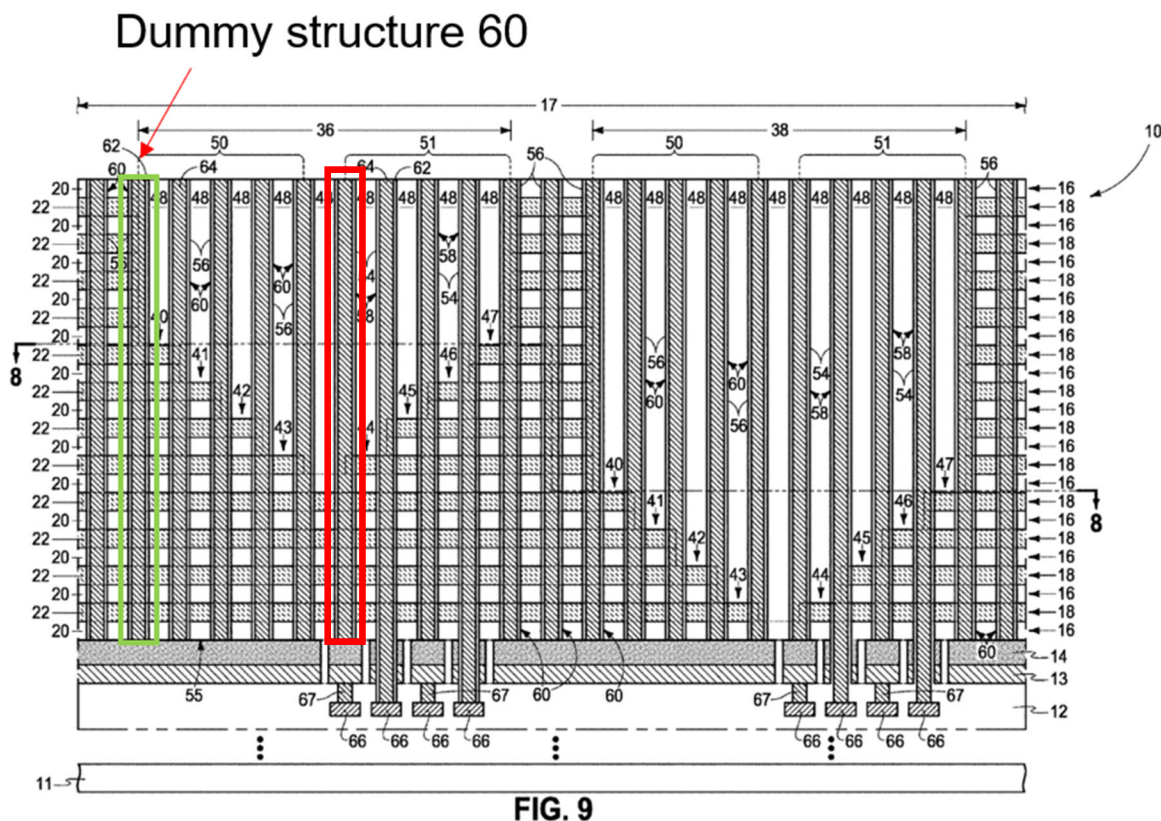


Ex. 1001, Fig. 12.

203. In particular, the “second staircase region 1122” does not align with “first staircase region 1121.” Ex. 1001, 22:27-32. As can be seen, the upper staircase region of stack structure 1106 is not on top of the lower staircase region of stack structure 1103. But the staircase structures (*viz.*, stacks 1106 and 1103), which each include a staircase region, are nonetheless on top of one another. Tessariol discloses the same.

2. [2.B] “the supporting pillar extends from a top surface of the second staircase structure to a bottom surface of the first staircase structure.”

204. Tessariol discloses this claim element for largely the same reasons that I explained in connection with claim element [1.G]. This is also evident from Tessariol Fig. 9, which shows a *supporting pillar* (e.g., dummy structure 60) extending from a top surface of the second staircase structure to a bottom surface of the first staircase structure. Likewise, Tessariol’s operative vias (e.g., vias 58 shown in red below) extend from the top of the upper stack to the bottom surface of the first staircase. Ex. 1006, [0038]-[0039].



Id., Fig. 9 (annotated).

C. Claim 4

205. Claim 4 is a dependent claim that depends on claim 2 (which in turn depends on claim 1). I address how Tessariol satisfies the three additional elements of claim 4 below.

1. [4.A] “the supporting pillar and the semiconductor channel are filled with different filling layers; and”

206. Tessariol discloses this claim element. Tessariol discloses embodiments in which the *semiconductor channel* (channel opening 26 with transistor material 32) and *supporting pillar* (dummy structure 60 and/or via 58) have different filling layers. For example, Tessariol discloses that transistor material 32 is “formed in individual channel openings 26 in each of the first stack 24 and second stack 30,” and can comprise “a charge-blocking material (e.g., silicon dioxide and/or silicon nitride), a charge-storage material (e.g., floating gate material such as doped or undoped silicon, etc. or charge-trapping material such as silicon nitride, metal dots, etc.), a charge-passage material (e.g., a bandgap-engineered structure having nitrogen-containing material such as silicon nitride laterally sandwiched between two insulating oxide layers such as silicon dioxide), and transistor channel material (e.g., suitably doped polysilicon, etc.).” Ex. 1006, [0033].

207. By contrast, Tessariol discloses that dummy structures 60 may comprise only two components: “an insulative lining 62 ... and a conductive core.” Ex. 1006, [0038]. The operative vias 58 also have the same insulative lining and conductive core as dummy structures 60. *Id.* Thus, Tessariol’s *supporting pillar* (dummy structure 60 and/or via 58) has *different filling layers* than Tessariol’s channel openings 26 with transistor material 32 (*semiconductor channel*).

2. [4.B] “the supporting pillar is filled with at least one of an insulating material and a pillar-support material surrounded by the insulating material,”

208. Tessariol discloses this claim element. For example, Tessariol discloses that “the dummy structures may individual [sic] comprise a conductive core (e.g., 64) and an insulative periphery (e.g., 62).” Ex. 1006, [0049]. Here, the conductive core is the *pillar-support material*, which is surrounded by the “insulative periphery [62]” (the *insulating material*). *Id.* The operative vias 58 have these same elements. *Id.*, [0038].

3. [4.C] “and the semiconductor channel is filled with at least one of a charge trapping film, a semiconductor channel film, and a dielectric core.”

209. Tessariol discloses this claim element. In particular, Tessariol discloses that “transistor material 32” (which fills the *semiconductor channel*) “may comprise, for example and in order of deposition, a charge-blocking material (e.g., silicon dioxide and/or silicon nitride), *a charge-storage material (e.g., ... charge-trapping*

material such as silicon nitride, metal dots, etc.), a charge-passage material (e.g., a bandgap-engineered structure having nitrogen-containing material such as silicon nitride laterally sandwiched between two insulating oxide layers such as silicon dioxide), and *transistor channel material (e.g., suitably doped polysilicon, etc.)*. Material 22 may be laterally recessed back (not shown) from original channel openings 26 prior to deposition of the example charge-blocking material. *Central portions of channel openings 26 may be filled with ... [a] solid insulator material 33.*” Ex. 1006, [0033] (emphases added). A POSITA would have understood that the Tessariol’s charge-trapping material is a *charge trapping film*, the channel material is a *semiconductor channel film*, and the solid insulator material is a *dielectric core*.

D. Claim 5: “wherein the insulating material comprises silicon oxide and the pillar-support material comprises at least one of copper, cobalt, nickel, and aluminum.”

210. Claim 5 is a dependent claim that depends on claim 4 (which in turn depends on claim 1). Tessariol discloses, or at least renders obvious, this claim element. Tessariol discloses that dummy structures 60 (the claimed *support pillars*) “comprise an insulative lining [insulative periphery] 62 (e.g., *silicon dioxide* and/or silicon nitride).” Ex. 1006, [0038] (emphasis added). The conductive vias include the same materials. *Id.* A POSITA would understand that silicon dioxide is a “silicon oxide.” Silicon dioxide, SiO₂, is a solid, glassy insulative material very

commonly used in the manufacture of 3D NAND and other semiconductor devices. The other silicon oxide, silicon monoxide, SiO, is a gas and would be entirely unsuitable for this purpose.

211. Tessariol also discloses that dummy structures 60 (the claimed *support pillars*) “comprise ... a conductive core 64 (e.g., metal material).” Ex. 1006, [0038]. A POSITA would have understood that by disclosing that the conductive core can be a “metal material,” Tessariol discloses that the pillar-support material may be one of *copper, cobalt, nickel, and aluminum*. Tessariol discloses that the dummy structures and metal vias may be the same material. *Id.*, [0038]. Copper, for example, was a well-known metal interconnect materials used extensively in semiconductor chips, including in 3D NAND devices before the filing date of the ’031 Patent. *See, e.g.*, Ex. 1014 (U.S. Pat. No. 9,299,641), 2:32-43 (copper interconnects); Ex. 1015 (U.S. Pat. No. 11,244,725), 11:36-44 (copper interconnects).

XV. GROUND 3: DEPENDENT CLAIM 4 IS OBVIOUS OVER KIM IN VIEW OF TESSARIOL

212. My analysis for Ground 1 demonstrates how Kim’s disclosures in view of the knowledge of a POSITA render claim 4 unpatentable because it would have been obvious to a POSITA to fabricate Kim’s dummy structures (*supporting pillars*) with a conductive core (e.g., made of a common metal such copper or aluminum)

and insulating liner. Section XIII.D.2. Ground 1 relies, in part, on Tessariol to show that the use of such metal-core dummy structures was well known to a POSITA. *Id.* Ground 3 is substantially identical to my claim 4 analysis for Ground 1, except that Ground 3 expressly combines Kim with Tessariol to demonstrate the same point: Kim combined with Tessariol renders obvious the use of a conductive metal core and insulating liner for Kim’s dummy structure DS. My analysis for underlying claims 1 and 2 (on which claim 4 depends) is the same and I only address claim 4 here.

213. As explained below, a POSITA would have been motivated to employ supporting pillars with metal cores and insulating liners as Kim’s dummy structures DS with a reasonable expectation of success.

A. Motivation To Combine And Reasonable Expectation Of Success

214. A POSITA would have had several motivations to apply Tessariol’s teaching of using support pillars with conductive cores to Kim’s dummy structures (*supporting pillars*). *First*, a POSITA would have been motivated to consider a variety of different materials because Kim states that the function of the dummy structure is to “support the stack structure ST.” Ex. 1005, 9:30-31. And Tessariol discloses pillars in multi-stack 3D memory devices that provide this same function, namely, to “support[] and prevent[] [the stack] from collapsing.” Ex. 1006, [0041].

215. *Second*, as an initial matter, Kim's dummy pillars are made with various layers, including thin layers, and the vast majority of the overall material percentage of the pillar is dielectric material (see Section XIII.C.2). The various thin layers are less suitable as a structural support than, *e.g.*, Tessariol's metal cores. Ex. 1012 (U.S. Pat. No. 9,768,186), 4:60-5:12. In addition, the mechanical support provided by a material is determined by its elastic properties such as the bulk modulus and Young's modulus. *See* Exs. 1021 and 1022 (describing and characterizing mechanical and structural properties of thin films, thick films, and metals). These parameters determine how a solid deforms (*i.e.*, the strain) in response to the force applied (*i.e.* the stress). Materials deform elastically up to the so-called yield point where they revert back to the original shape once the applied stress is removed. Beyond the yield point, there can be irreversible, inelastic deformation and fracture. Many metals such as Al and Cu tend to deform inelastically without fracturing because they are malleable and ductile. On the other hand, dielectrics such as silicon dioxide and silicon nitride are brittle, and fracture once the yield point is exceeded. These properties determine the suitability of a material as the pillar. Properties of some materials used for device fabrication are given in references Exs. 1021 and 1022.

216. *Third*, Kim expressly teaches that its dummy pillars can be made from different materials than its vertical channel structures. Ex. 1005, 13:28-33. This

would have motivated a POSITA to consider support pillars of other types, and Tessariol provides precisely such other types of support pillars. Ex. 1006, [0037], [0038], [0041].

217. *Fourth*, the supporting pillars in Tessariol are described as either active conductive vias or dummy conductive vias. Ex. 1006, [0041]. A POSITA would have understood that using active conductive vias as supporting pillars in Kim would be beneficial because doing so would serve the dual purpose of both (1) a support function and (2) an interconnect function.

218. Next I discuss ***reasonable expectation of success***. A POSITA would have had at least a reasonable expectation of success deploying a metal core in Kim's dummy pillars for a variety of reasons. *First*, Tessariol's support pillars extend all the way through the through the stack. Ex. 1006, Fig. 9. And Kim's fabrication process for dummy pillars already does the same (using a single-step etch process). Ex. 1005, Fig. 4B. *Second*, the support pillars described in Tessariol include both an insulating liner and a conductive core. Kim's fabrication process already employs such structures that extend through the stack, namely, a common source line. *Id.*, 6:24-30, Fig. 4A ("CSR"). This structure creates a connection between an upper-level source line to common source regions in the substrate, and it includes an insulating liner and conductive core. The *third* reason a POSITA would have a

reasonable expectation of success is that the processing techniques to create supporting conductive vias, such as those in Tessariol, were well-known.

B. Claim 4

219. Claim 4 is a dependent claim that depends on claim 2 (which in turn depends on claim 1). I address how Kim in view of Tessariol satisfies the three additional elements of claim 4 below.

1. [4.A] “the supporting pillar and the semiconductor channel are filled with different filling layers; and”

220. Kim in view of Tessariol renders this claim element obvious. As I discuss in Section XIII.A.6, Kim describes a semiconductor channel that includes semiconductor and memory elements. Kim states that for certain embodiments “each of dummy structures DS may include a dummy pattern. A layer or component of each of the dummy structures DS [*supporting pillar*] may be different from the layer(s) or component(s) of each of the vertical structures VS [*semiconductor channel*].” Ex. 1005, 13:28-33. For the reasons I explain in Sections XIII.D.2 and XV.A, a POSITA would have been motivated to employ a conductive core with an insulating liner as Kim’s dummy structures, which are *different filling layers* than Kim’s semiconductor channel. See Ex. 1006, [0037], [0038], [0041].

2. **[4.B] “the supporting pillar is filled with at least one of an insulating material and a pillar-support material surrounded by the insulating material,”**

221. Kim in view of Tessariol renders this claim element obvious. As I discuss in Sections XIII.D.2 and XV.A, a POSITA would have been motivated to employ a conductive core with an insulating liner as Kim’s dummy structure (*supporting pillar*). Ex. 1006, [0037], [0038], [0041]. Tessariol discloses using a conductive core as a support material, with insulating material surrounding the core. *Id.*

3. **[4.C] “and the semiconductor channel is filled with at least one of a charge trapping film, a semiconductor channel film, and a dielectric core.”**

222. Kim discloses this claim element for the same reasons I explained in Ground 1 with respect to claim element [3.B], which includes the same requirements for the *semiconductor channel*.

XVI. GROUND 4: INDEPENDENT CLAIM 1 AND DEPENDENT CLAIMS 2 AND 4-5 ARE OBVIOUS OVER TESSARIOL IN VIEW OF KIM

223. My analysis for Ground 2 demonstrates how Tessariol’s disclosure, in view of the knowledge of a POSITA, renders obvious claims 1-2, and 4-5. I relied on Kim in Ground 2 to demonstrate a POSITA’s knowledge in four respects: (1) for limitation [1.B], that a two-stack staircase structure was well-known; (2) for limitation [1.D], that filling techniques to encase the 3D structure were conventional and routine to employ, (3) for limitation [1.F], that utilizing a two-step etch process

typically results in unaligned sidewalls; and (4) for limitation [1.H], that utilizing a single-step etch process will typically result in aligned sidewalls.

224. If Patent Owner argues that Kim does not reflect the knowledge of a POSITA and must be separately combined with Tessariol (which would be incorrect, because an obviousness ground always considers a POSITA's knowledge), Ground 4 expressly combines Tessariol with Kim. For all other claim elements, Ground 4 relies on the same analysis I provided for Ground 2. Thus, I only address claim elements [1.B], [1.F], and [1.H] below.

A. Motivation To Combine And Reasonable Expectation Of Success

225. A POSITA would have had several motivations to apply Kim's teachings regarding continuous staircase structures, filling techniques, two-step etch profiles, and one-step etch profiles with Tessariol, including with a reasonable expectation of success.

226. ***Staircase Regions.*** To begin, Tessariol expressly provides an open-ended list of the type of staircase regions that may be used. Ex. 1006, [0034] (disclosing that "only one stair step structure, two stair step structures, or more than three stair step structures may be formed" and such structures "may be formed by any suitable existing or yet-to-be-developed technique, with photolithographic patterning and etch being one example"), [0035] (disclosing the use of different

flight configurations). These teachings would have encouraged a POSITA to consider other types of staircase region teachings, including those disclosed in Kim.

227. *Second*, the staircase regions in Tessariol and Kim both utilize substantially the same landing pad architecture for the wordline contacts. *Compare* Ex. 1005, Figs. 4A, 18 (showing contacts to staircase), Ex. 1006, Fig. 17 (showing contacts to staircase). This similarity would have motivated a POSITA to consider the staircase profile disclosed by Kim.

228. *Third*, Tessariol's use of a sacrificial gate replacement in the staircase region process necessitates the use of dummy support structures. §XIV.A.8. Likewise, Kim's staircase region includes dummy support pillars. §XIII.A.8. Given that Kim's approach to supporting its staircase regions meets Tessariol's structural support requirements, a POSITA would have been motivated to apply Kim's teachings to Tessariol.

229. *Fourth*, Kim's contiguous staircase profile is more efficient because half of Tessariol's staircase region may go unused. Ex. 1006, Fig. 17 (the right portion, 44-47, of each staircase is not shown as being used). Thus, a POSITA would have been motivated to consider more efficient staircase regions, such as those in Kim, which are not made of non-functional steps.

230. A POSITA would have had a reasonable expectation of success in applying Kim's staircase teachings to Tessariol for multiple reasons. To begin,

recall that Tessariol's staircase region "may be formed by any suitable existing or yet-to-be-developed technique, with photolithographic patterning and etch being one example." Ex. 1006, [0034]. In other words, as a POSITA would have understood, Tessariol is saying that its memory device does not require any particular type of staircase profile. And Kim's continuous staircase profile that spans two stacks is suitable for Tessariol because, *e.g.*, it allows for support pillars which are required by Tessariol. Additionally, staircase technology (and the fabrication processes for forming it) were well-known at the time of the alleged invention, and it would have been routine to apply such teachings from one 3D NAND design to another 3D NAND design. §VIII.

231. *Filling Techniques.* Tessariol and Kim both depict a planar surface that is an interface to upper layer metal layers. Ex. 1005, Fig. 4A (110/120/130), Ex. 1006, Fig. 17 (86). Thus, a POSITA would have been motivated to consider Kim's fill techniques to provide for the planarized surface. In fact, both Tessariol and Kim employ a multi-stack staircase structure. *See* Grounds 1 and 2. Thus, a POSITA would have been particularly motivated to consider Kim's teaching regarding the fill technique to accomplish the planarized surface given the large amounts of space (due to the stairstep regions) that are required to be filled. It would have been routine to apply Kim's filling teachings to Tessariol. As described above, both have the same fundamental structures. And the deposition of such fills was textbook material,

because it was fundamental to formation of the upper-level metal layers. Ex. 1023, 14.

232. ***Etch Processes.*** To begin, Tessariol discloses both one- and two-step etch processes. In particular, Tessariol discusses one-step etching to form its supporting pillars (*see* §XIV.A.9) and a two-step etch to form its dummy channel structures (*see* §XIV.A.7). Kim also discloses one- and two-step etch processes for creating its supporting pillars and semiconductor channels, respectively, but also expressly discusses the effect of these etches on the sidewall profiles. *See* §§XIII.A.7 and XII.A.9. Accordingly, a POSITA would have been motivated to consider Kim's etch teachings to better understand and improve the structures in Tessariol. Next, both Tessariol and Kim use the supporting pillars and channel structures for the same purposes. *See* §§XIII.A.7, 9 and XIV.A.7, 9. This would have further motivated a POSITA to consider Kim, because its etch teachings are directly relevant to the same structures in Tessariol.

233. A POSITA would have had a reasonable expectation of success in applying Kim's etch teachings to Tessariol for multiple reasons. For example, as described above, Kim's etch teachings relate to the same structures, namely, supporting pillars and channel structures. Additionally, not only do the teachings relate to the same structures, but those structures are within the same type of memory device, namely, 3D NAND.

B. Claim 1

1. [1.B] “a multiple-stack staircase structure comprising a plurality of staircase structures stacked over the substrate,”

234. Tessariol, in view of Kim, renders this claim element obvious. As I discuss in §XIV.A.3, Tessariol discloses a multi-stack structure with a “*first stack 24*” and “*second stack 30*.” Ex. 1006, [0029], [0031] (emphasis added). And as previously discussed, Tessariol further discloses that each stack includes a staircase region. *Id.*, [0034]. As I discuss in §XVI.A, it would have been obvious to apply Kim’s staircase teachings to Tessariol. In particular, applying Kim’s teaching of a continuous staircase region for each stack to Tessariol would result in a continuous staircase region for each stack (as Kim illustrates, Ex. 1005, Fig. 4B). *See* §XIII.A.3. Ground 4 makes no other changes to Tessariol’s stack structure, *e.g.*, the alternating material layers that help form the staircase region as set forth in Tessariol remain the same.

235. In summary, Tessariol in view of Kim renders obvious a *multiple-stack staircase structure* (*e.g.*, first stack 24 and second stack 30, having two continuous staircase structures) *comprising a plurality of staircase structures* (*e.g.*, each of the first stack 24 and second stack 30, both of which have a continuous staircase structure portion) *stacked over the substrate* (*e.g.*, base substrate 11).

2. [1.F] “wherein the semiconductor channel comprises unaligned sidewall surfaces; and”

236. Tessariol in view of Kim render this claim element obvious. As I discuss in §XIV.A.7, Tessariol employs a two-step etch process to create its channel structures. *See* Ex. 1006, Figs. 1-5, [0030], [0032], [0034]. Like Tessariol, Kim discloses a fabrication process that etches separate first channel holes (CH1) and second channel holes (CH2) to form the channel structures. Ex. 1005, 11:49-50. Kim discloses that this results in “misaligned” channel structures. §XIII.A.7. Given Kim’s express teaching of misaligned channel structures, a POSITA would have understood (and certainly would have found it obvious) that Tessariol’s two-step etch process will likewise result in unaligned channel sidewalls.

237. Accordingly, Tessariol in view of Kim renders obvious that the *semiconductor channel comprises unaligned sidewall surfaces* (e.g., sidewalls of transistor material in channel holes 26).

3. [1.H] “wherein the supporting pillar comprises aligned sidewall surfaces.”

238. Tessariol, in view of Kim, renders this claim element obvious. As I discuss in §XIV.A.8, Tessariol employs a one-step etch process to create its supporting pillars. *See* Ex. 1006, [0037]. Kim, like Tessariol, discloses a fabrication process wherein “the dummy holes DH may be formed by one etching process after the formation of the lower mold structure MT1 and the upper mold structure MT2

[(stack structure ST)].” Ex. 1005, 12:58-67. Kim teaches that this results in aligned dummy structures. §XIII.A.8. In view of Kim’s teaching, it would have been obvious that Tessariol’s one-step etch process will result in aligned supporting pillars.

239. Accordingly, Tessariol in view of Kim renders obvious that the *supporting pillar comprises aligned sidewall surfaces* (e.g., dummy structures 60 and operative vias 58).

XVII. SECONDARY CONSIDERATIONS OF NON-OBVIOUSNESS

240. During my review of the materials discussed herein, I did not become aware of any evidence suggesting the existence of any secondary indicia or considerations of non-obviousness. In the event that Patent Owner proffers any such evidence, I reserve the right to provide my opinions on such evidence in a reply Declaration.

XVIII. DECLARATION

241. In signing this declaration, I realize that this declaration will be filed as evidence in a contested case before the Patent Trial and Appeal Board of the USPTO.

242. I am aware that willfully false statements and the like made by me in connection with this declaration are punishable by fine or imprisonment, or both (18 U.S.C. § 1001) and may jeopardize the validity of the Petition. All statements herein made by me of my own knowledge are true and all statements made on information and belief are believed to be true. I declare under penalty of perjury that the foregoing is true and correct.

Executed this 17th day of April 2024 at Austin, Texas.



Sanjay Banerjee, Ph.D.