US009299641B2

(12) **United States Patent**
Sekar et al.

(10) **Patent No.: US 9,299,641 B2**
(45) **Date of Patent: *Mar. 29, 2016**

(54) **SEMICONDUCTOR SYSTEM, DEVICE AND STRUCTURE WITH HEAT REMOVAL**

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(73) Assignee: **MONOLITHIC 3D INC.**, San Jose, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

This patent is subject to a terminal disclaimer.

(21) Appl. No.: **14/747,599**

(22) Filed: **Jun. 23, 2015**

(65) **Prior Publication Data**

US 2015/0311142 A1 Oct. 29, 2015

Related U.S. Application Data

(63) Continuation-in-part of application No. 13/869,115, filed on Apr. 24, 2013, now Pat. No. 9,099,424, which is a continuation of application No. 13/571,614, filed on Aug. 10, 2012, now Pat. No. 8,450,804.

(51) **Int. Cl.**

H01L 23/48	(2006.01)
H01L 27/088	(2006.01)
H01L 23/367	(2006.01)
H01L 23/522	(2006.01)
H01L 27/06	(2006.01)

(52) **U.S. Cl.**

CPC ***H01L 23/481*** (2013.01); ***H01L 23/3677*** (2013.01); ***H01L 23/5225*** (2013.01); ***H01L 27/0688*** (2013.01); ***H01L 27/0886*** (2013.01); *H01L 2924/0002* (2013.01)

(58) **Field of Classification Search**

CPC H01L 23/3736; H01L 27/0688; H01L 27/11551

USPC 257/347, 758, 686, 712

See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

9,099,424 B1 * 8/2015 Sekar et al.

* cited by examiner

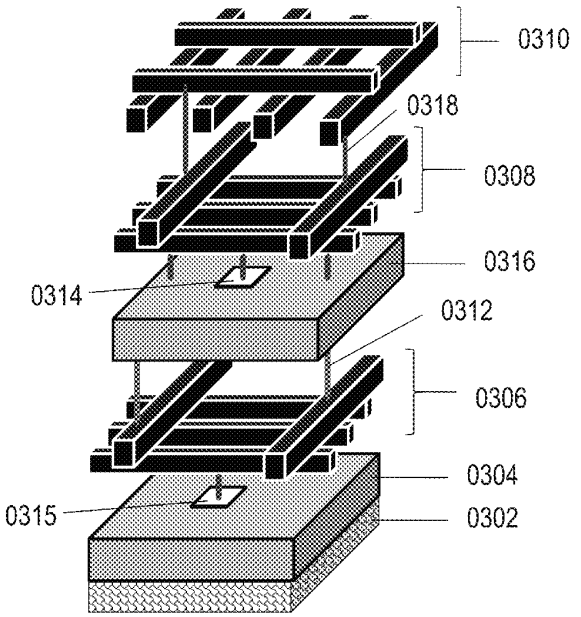
Primary Examiner — Cuong Q Nguyen

(74) *Attorney, Agent, or Firm* — Tran & Associates

(57) **ABSTRACT**

A 3D device including: a first layer including first transistors, the first layer overlaid by at least one interconnection layer; a second layer including second transistors, the second layer overlaying the interconnection layer; a plurality of electrical connections connecting the second transistors with the interconnection layer; and at least one thermally conductive and electrically non-conductive contact, where the at least one thermally conductive and electrically non-conductive contact thermally connects the second layer to a top or bottom surface of the 3D device.

20 Claims, 59 Drawing Sheets



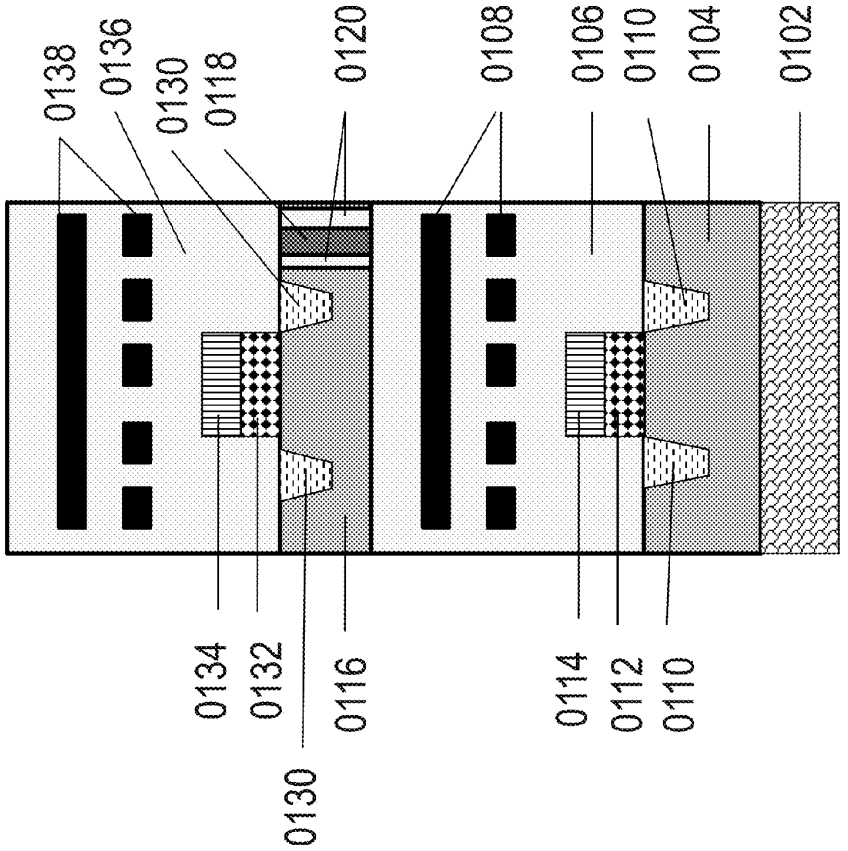

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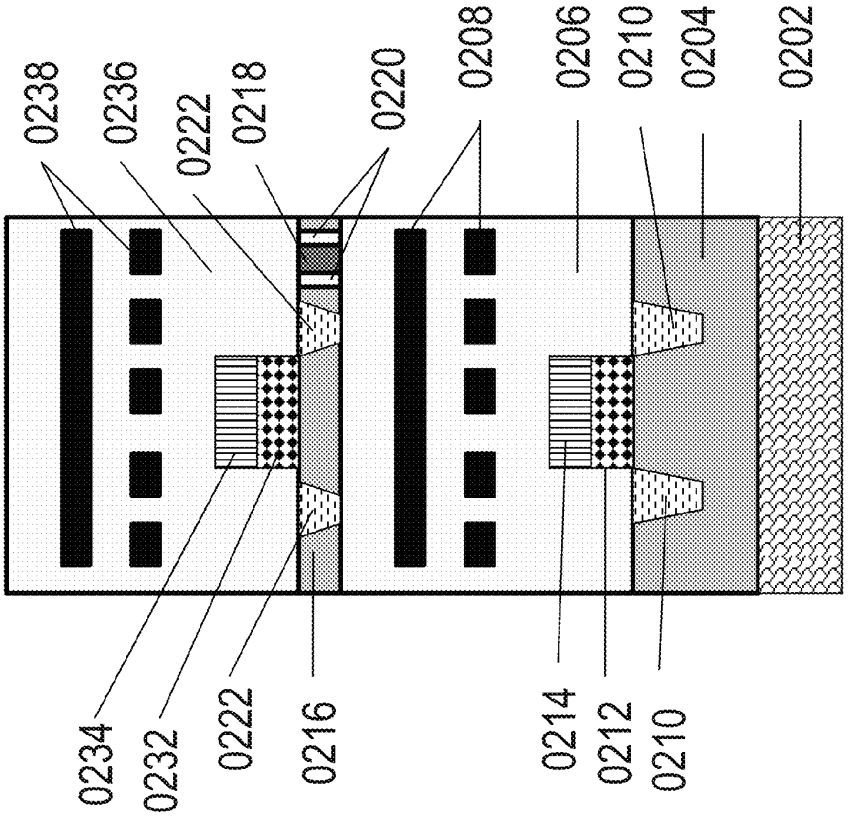
Fig. 1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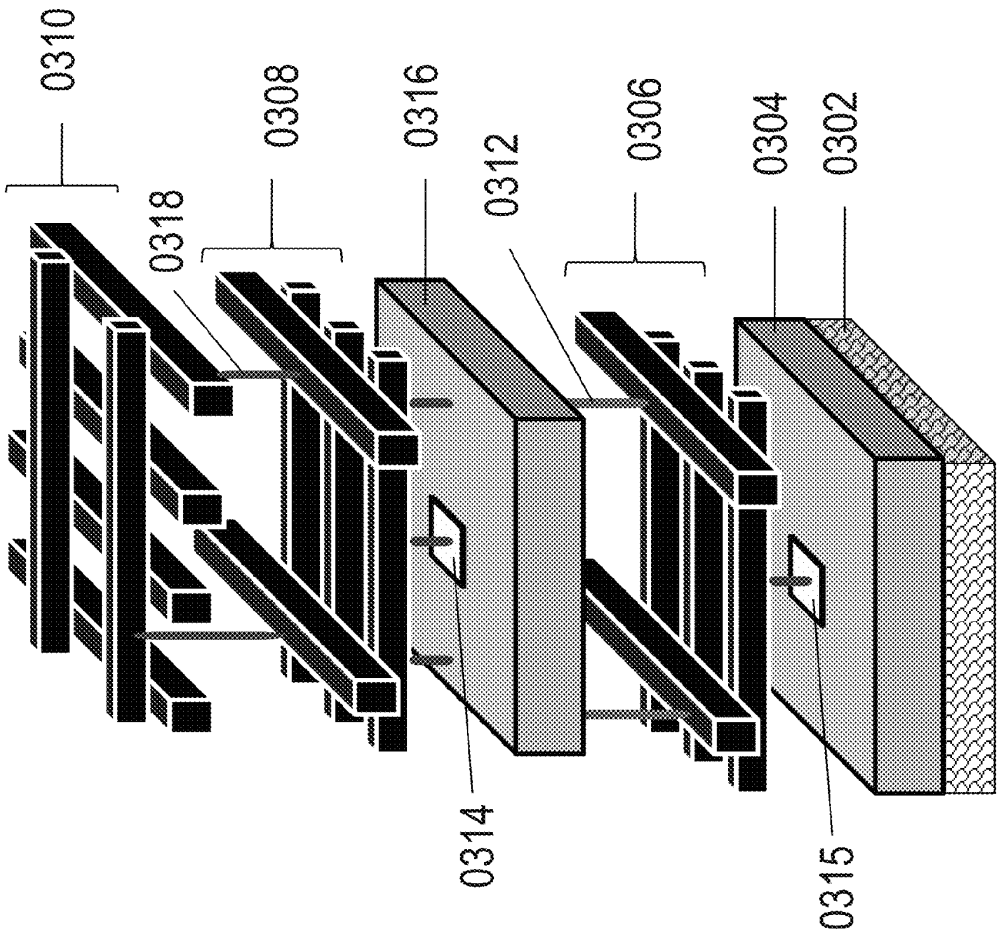
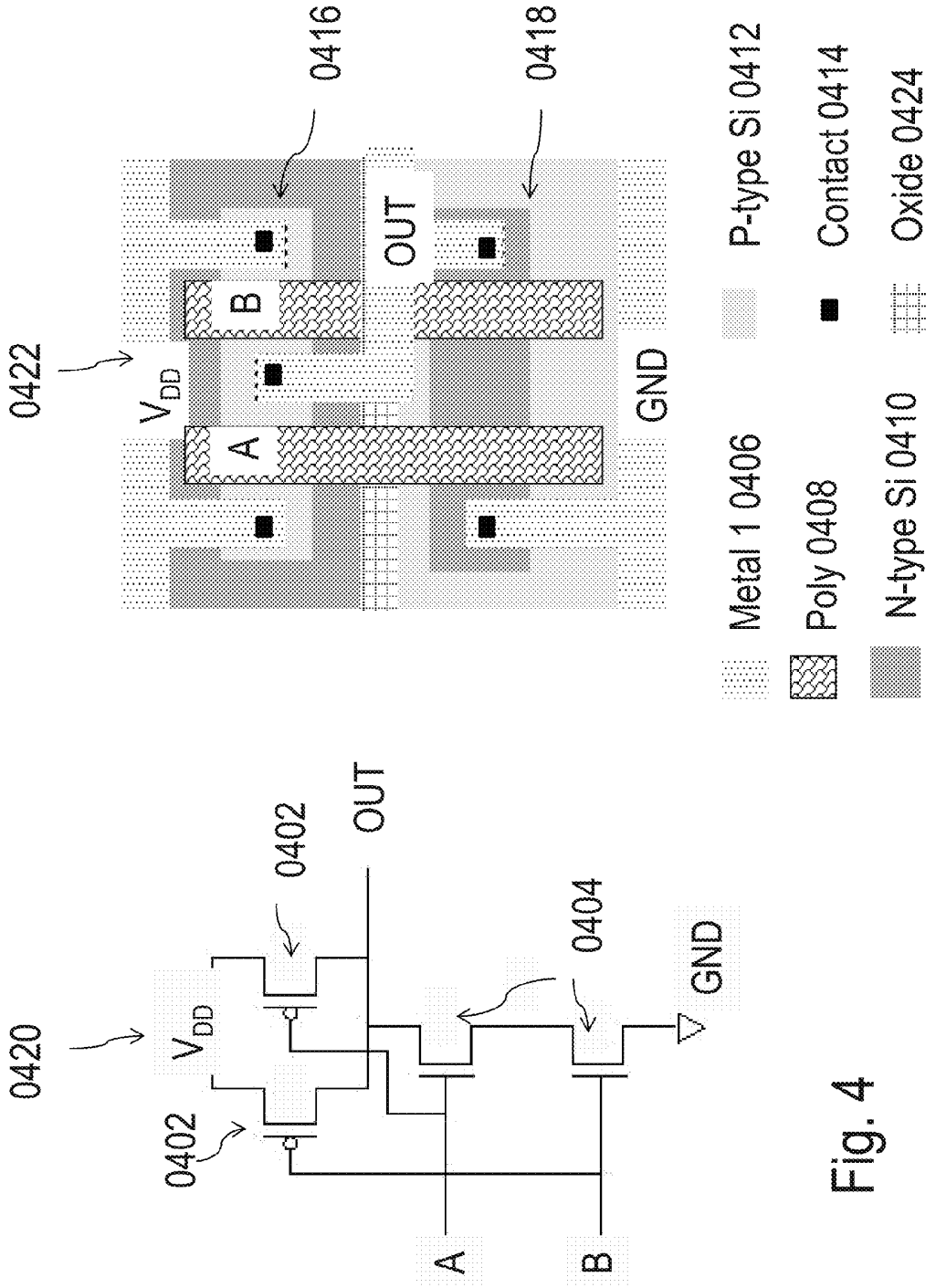
0212
0210

Fig. 2

Fig. 3

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OUT
0404
GND
A
B
0422
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0418
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A
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Poly 0408
N-type Si 0410
P-type Si 0412
Contact 0414
Oxide 0424

Fig. 4

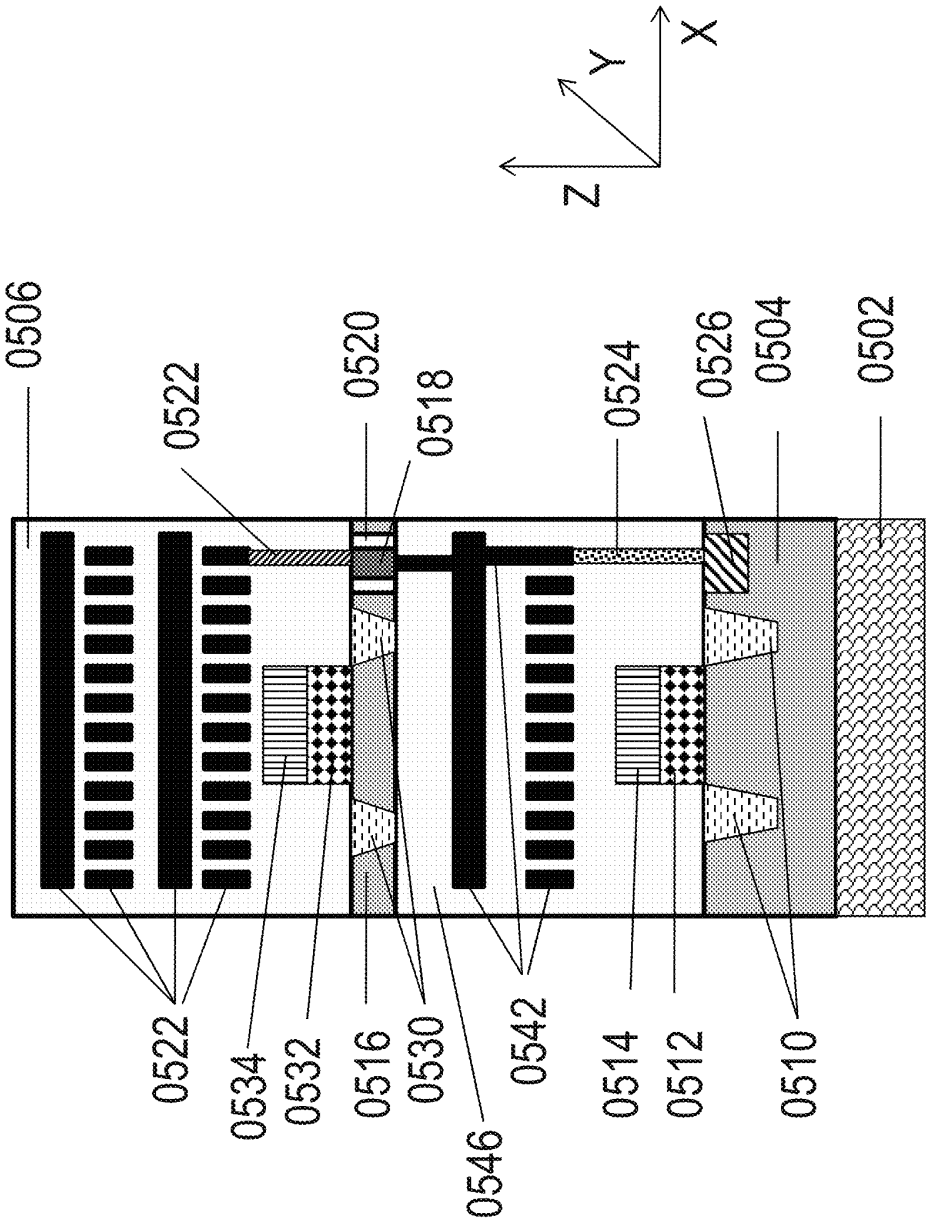
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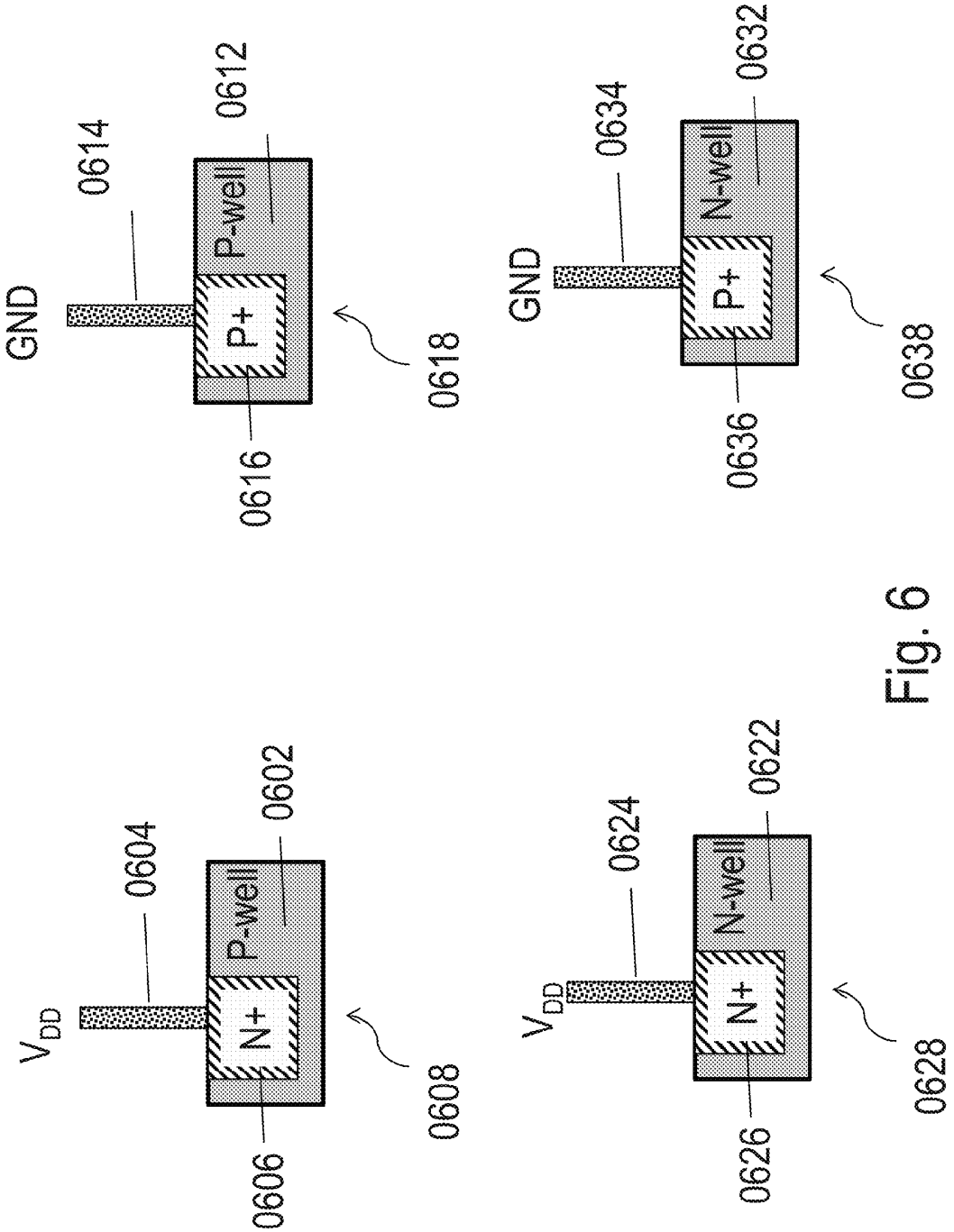
Fig. 5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P+
0616
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GND
0634
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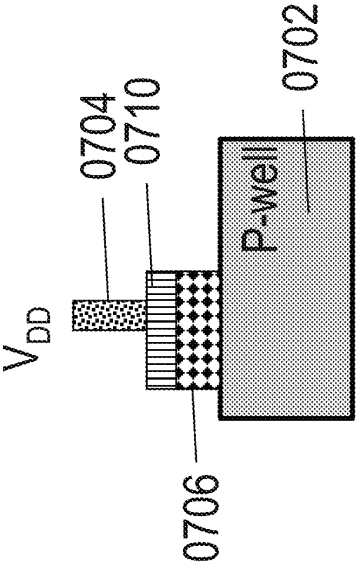
N-well
P+
0636
0638
V_{DD}
0604
0602
P-well
N+
0606
0608
V_{DD}
0624
0622
N-well
N+
0626
0628

Fig. 6



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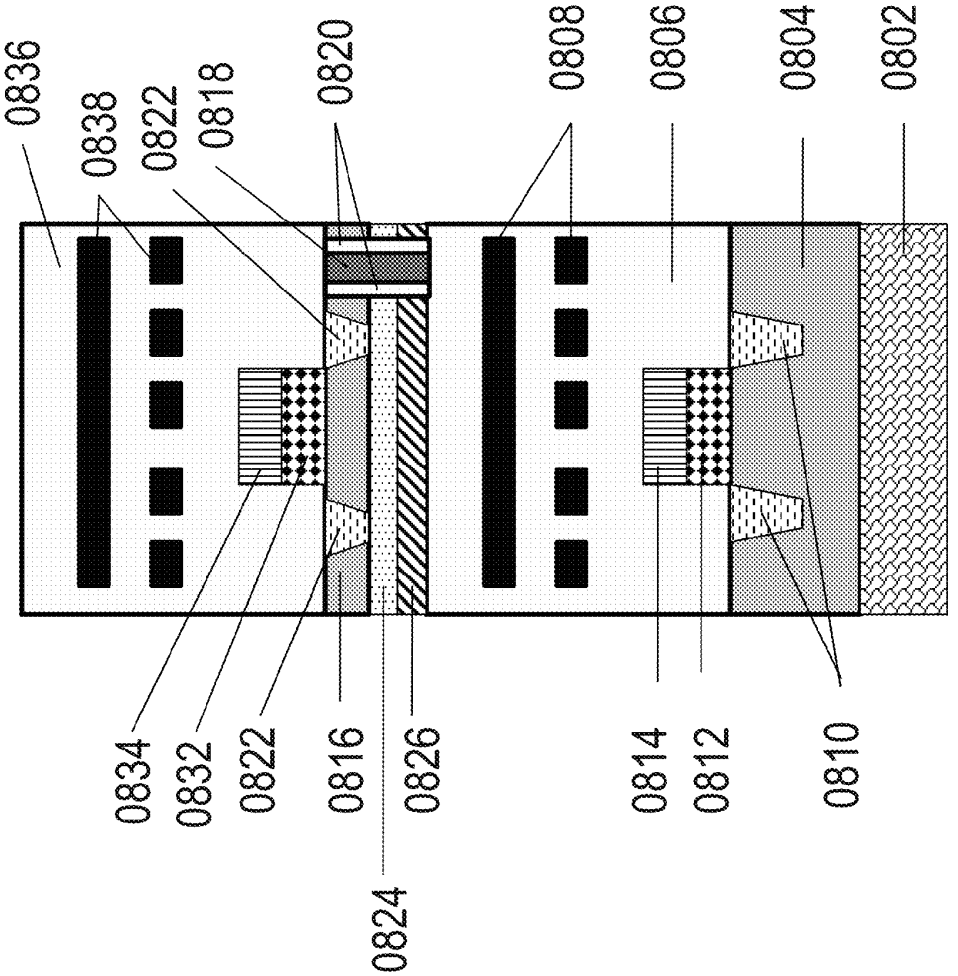
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Fig. 8

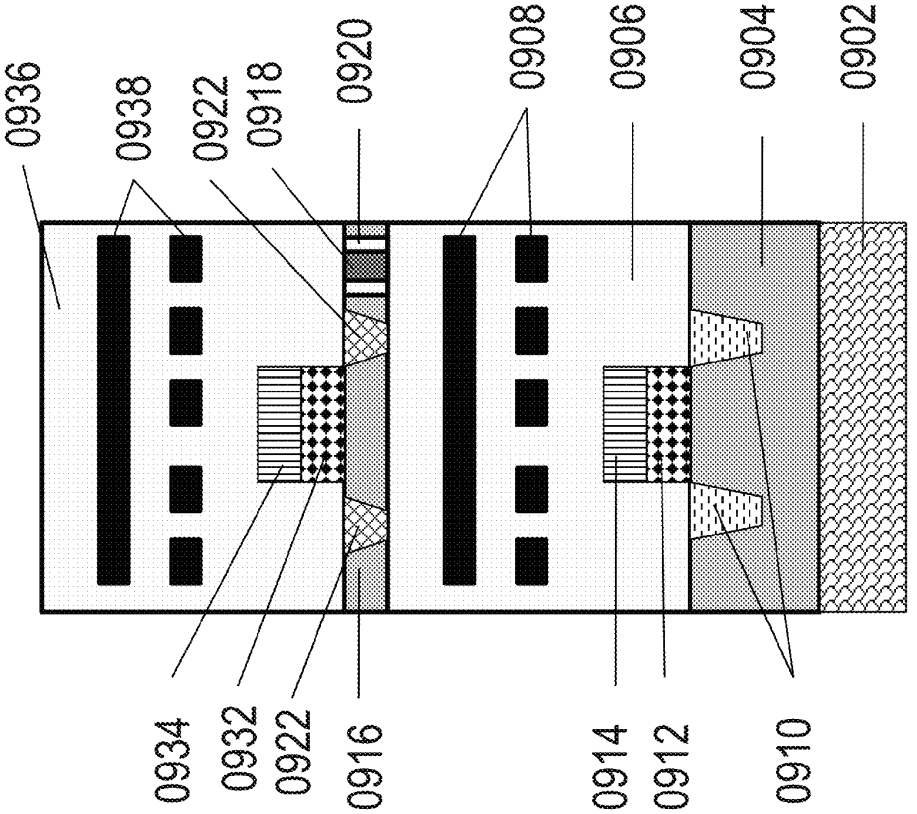
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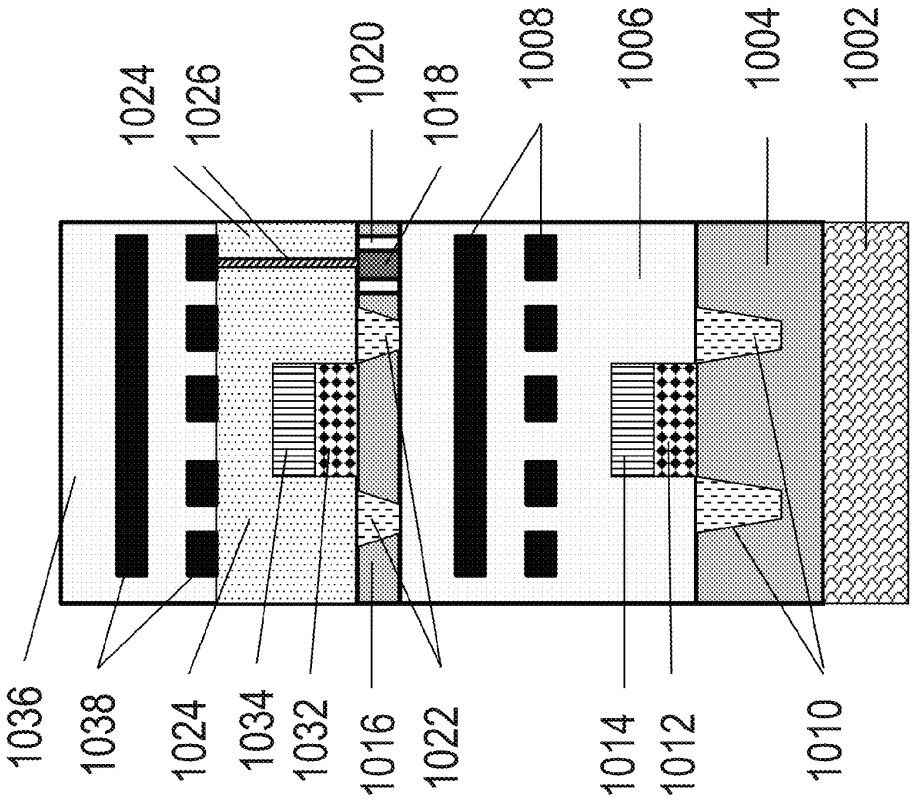
Fig. 9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1006
1004
1002

Fig. 10

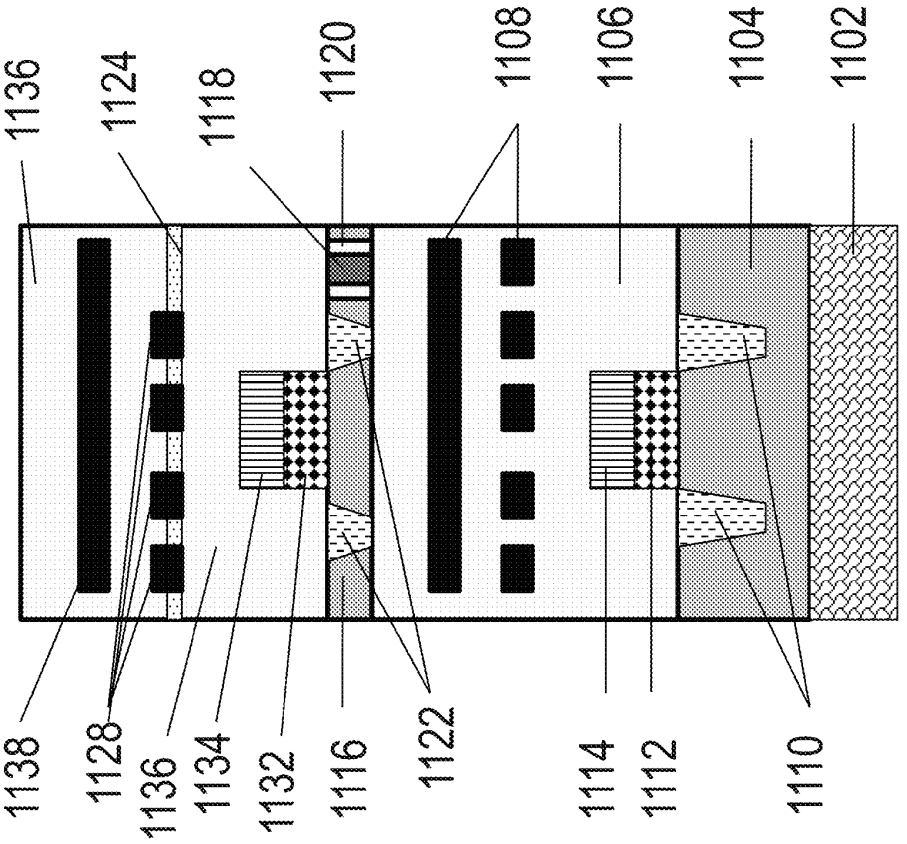
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Fig. 11

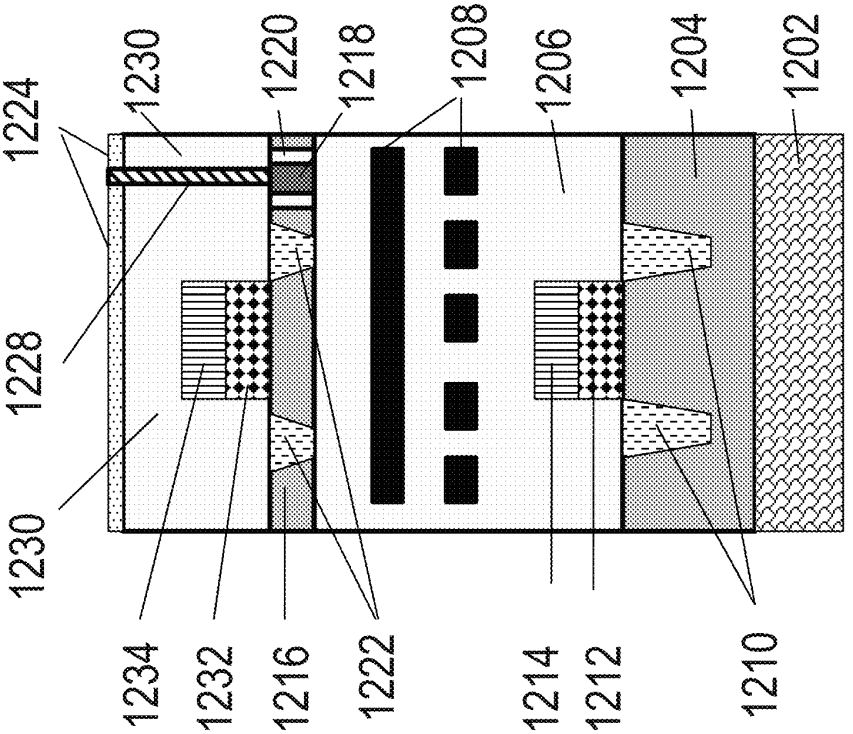


Fig. 12B

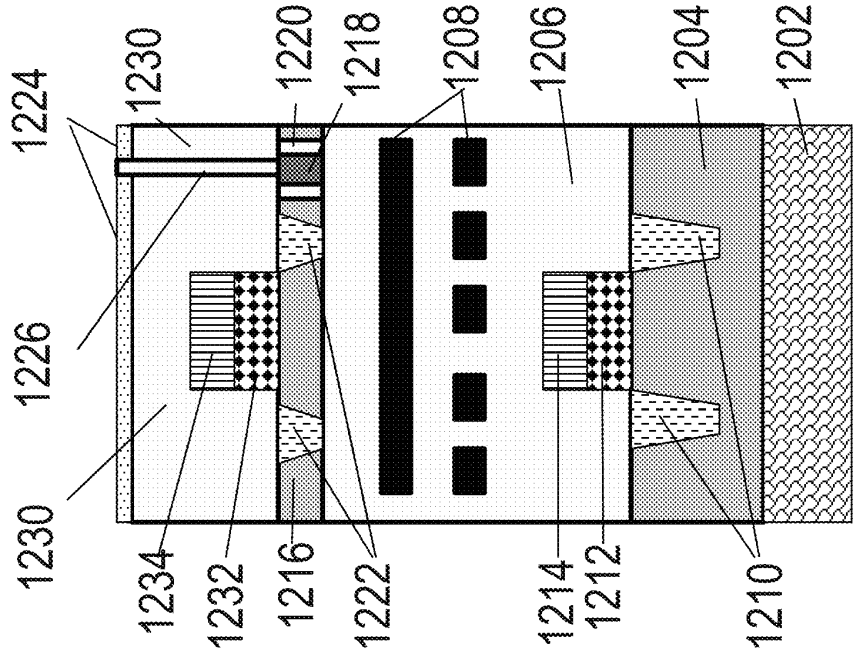
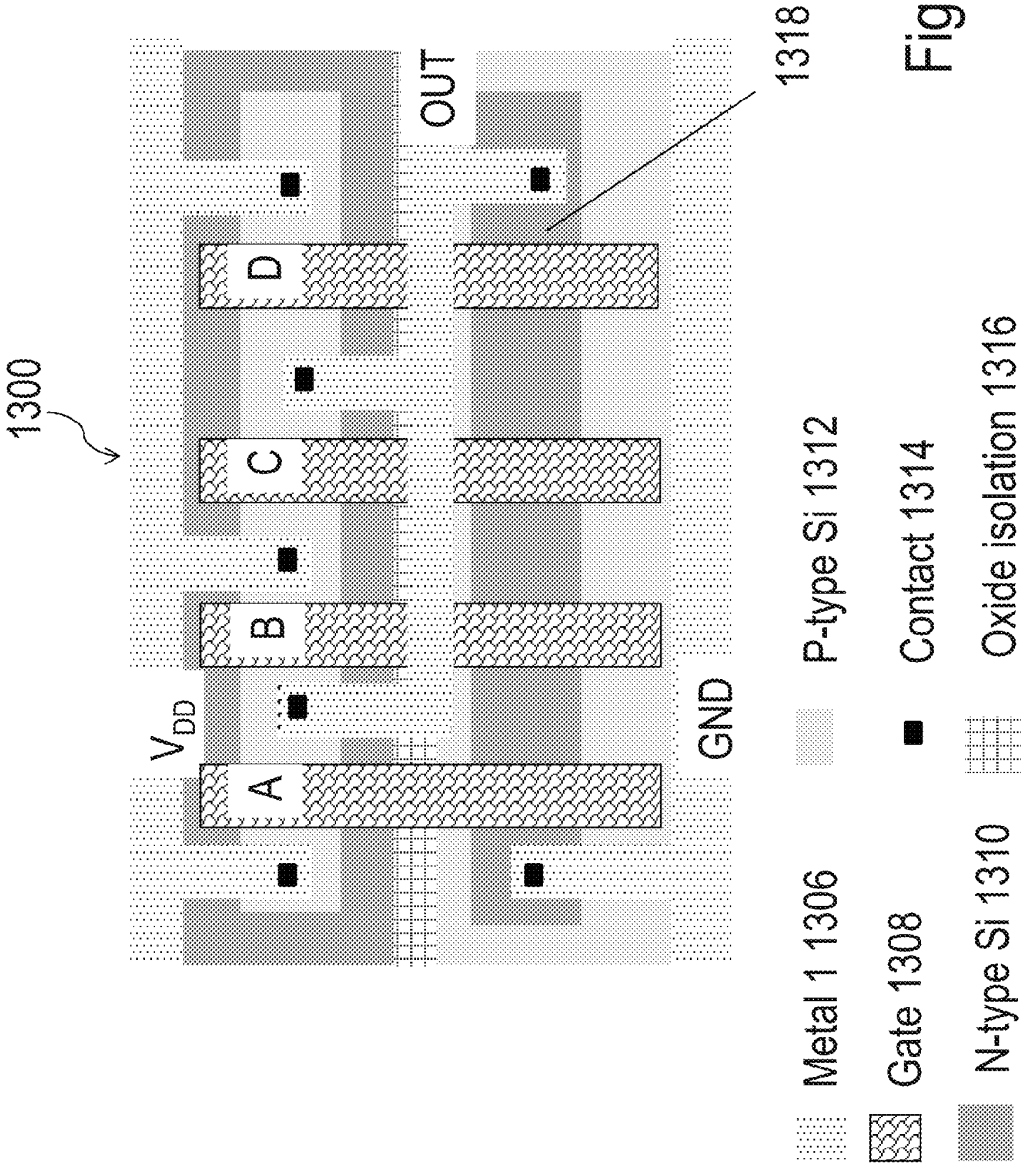


Fig. 12A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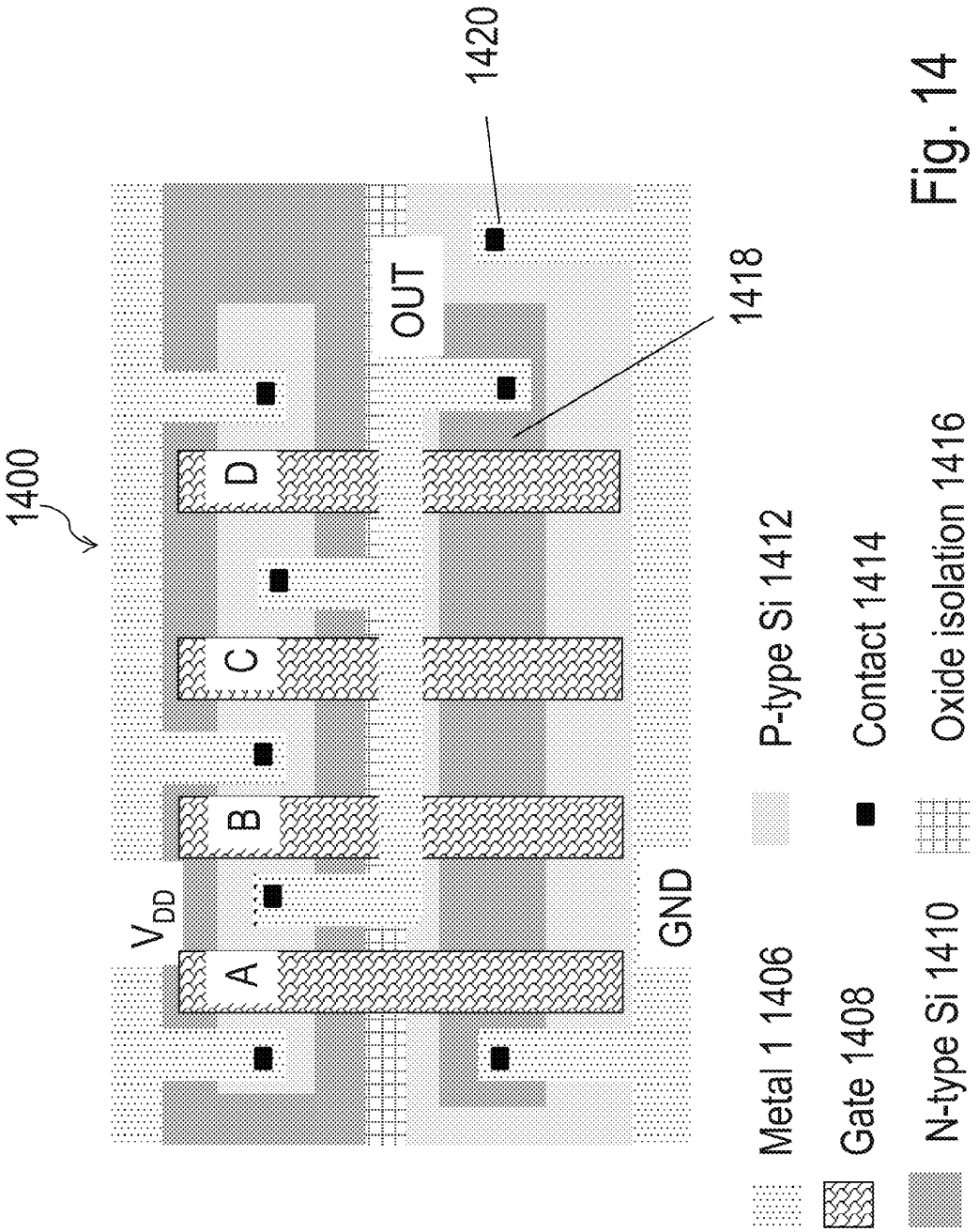
V_{DD}
A
B
C
D
OUT
GND
1318
Metal 1 1306
Gate 1308
N-type Si 1310
P-type Si 1312
Contact 1314
Oxide isolation 1316

Fig. 13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OUT
D
C
B
A
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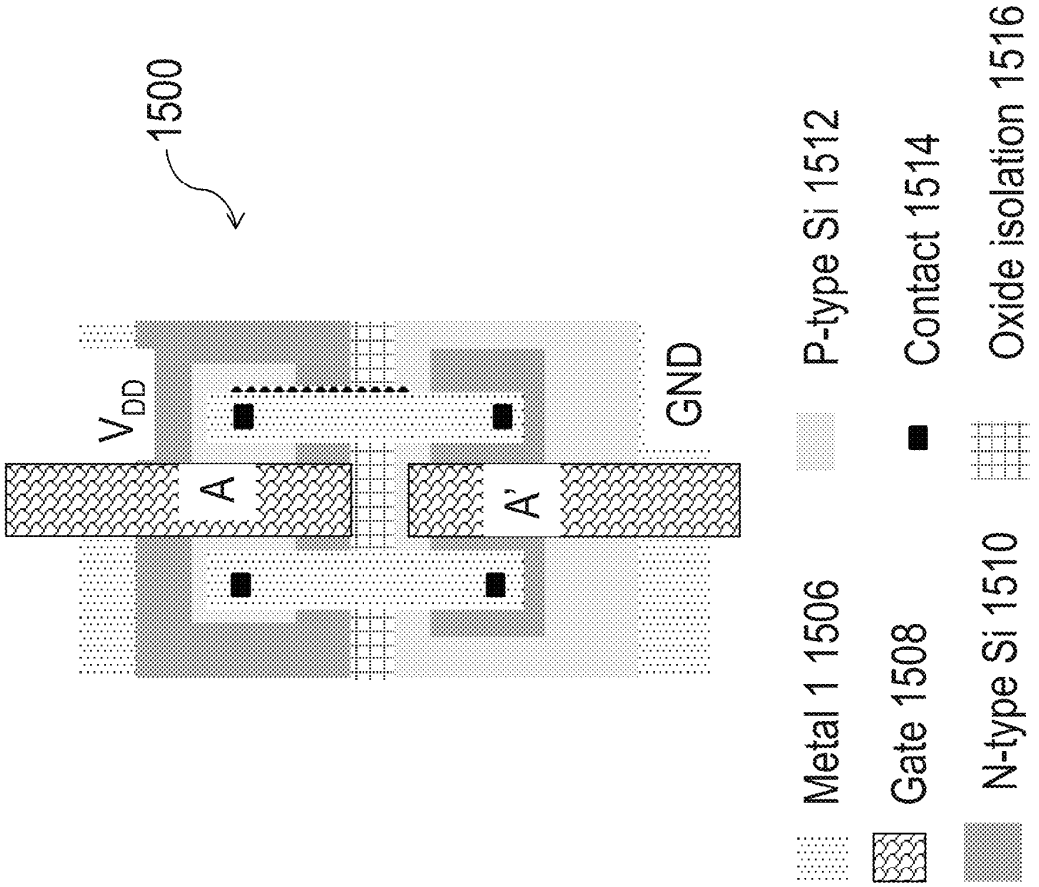
Gate 1408
N-type Si 1410
P-type Si 1412
Contact 1414
Oxide isolation 1416

Fig. 14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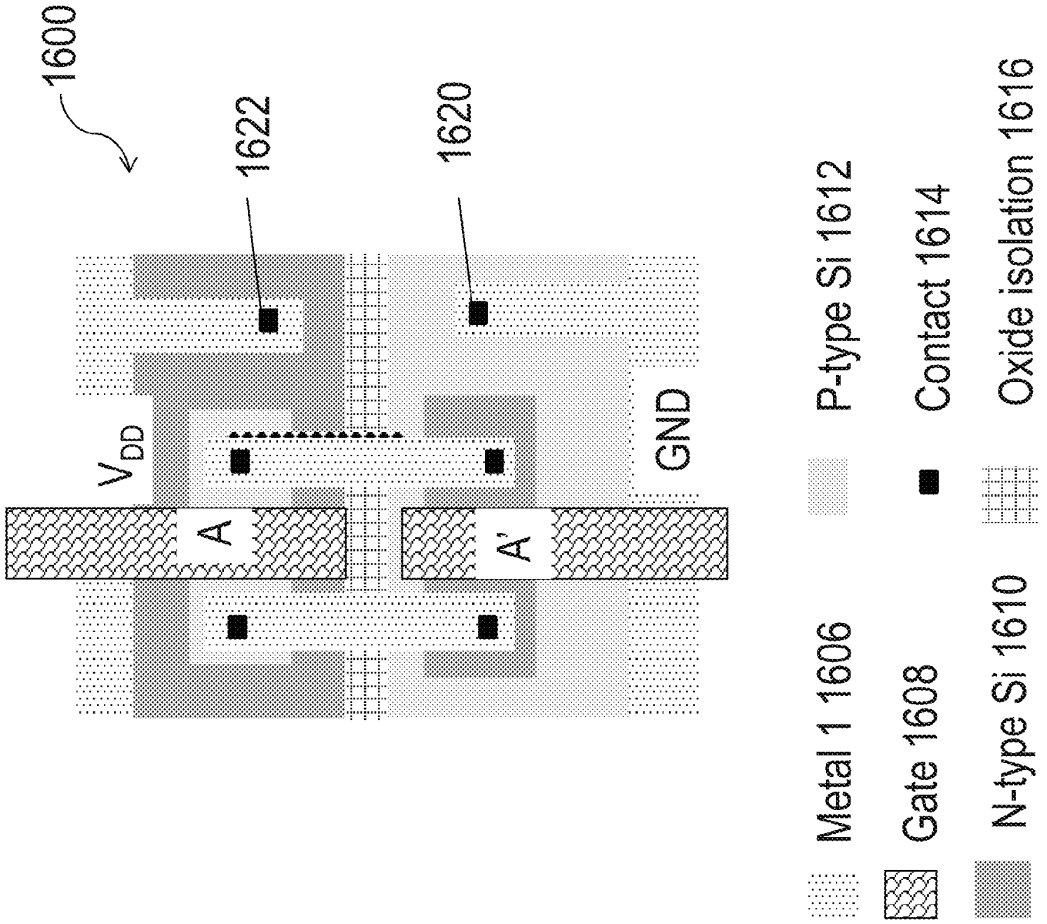
A'
GND
Metal 1 1506
Gate 1508
N-type Si 1510
P-type Si 1512
Contact 1514
Oxide isolation 1516

Fig. 15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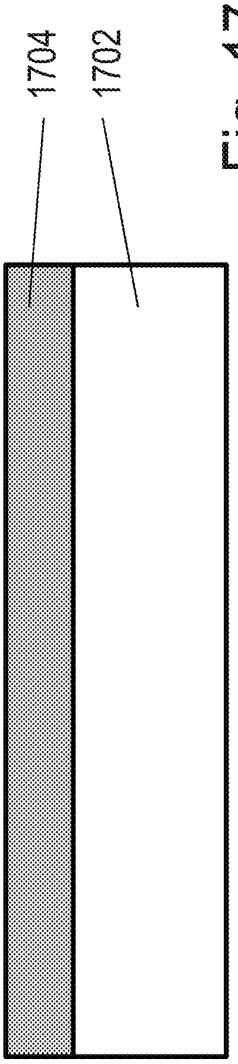
Oxide isolation 1616

Fig. 16



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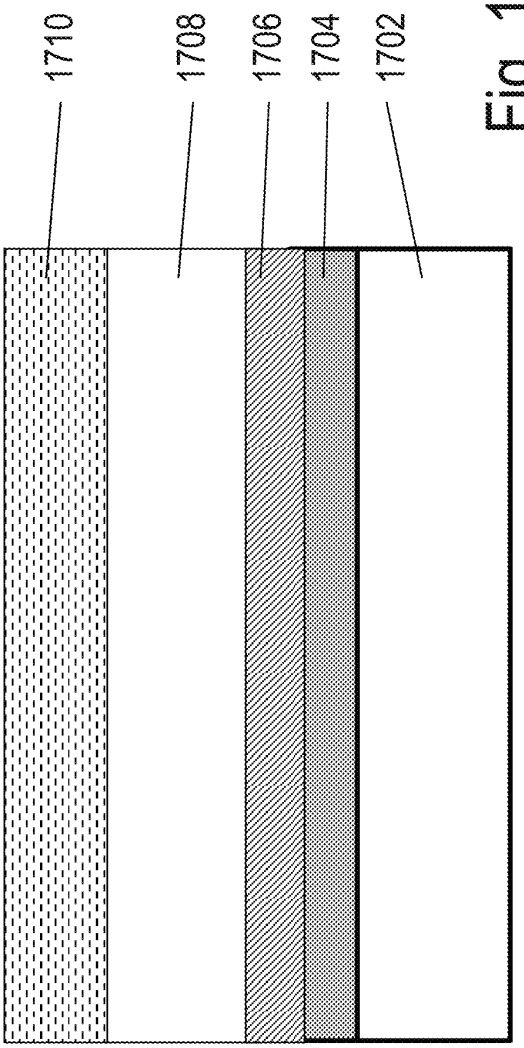


Fig. 17B

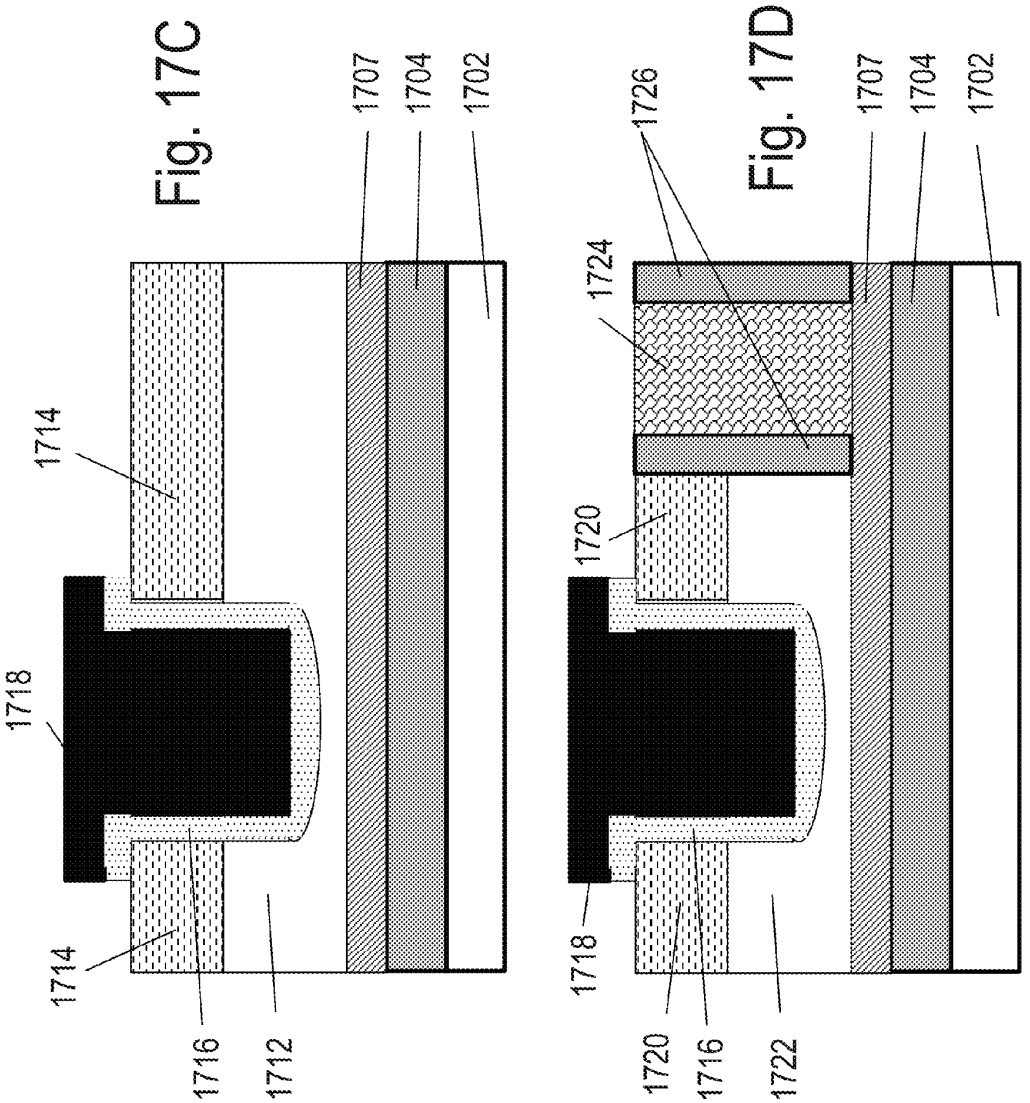
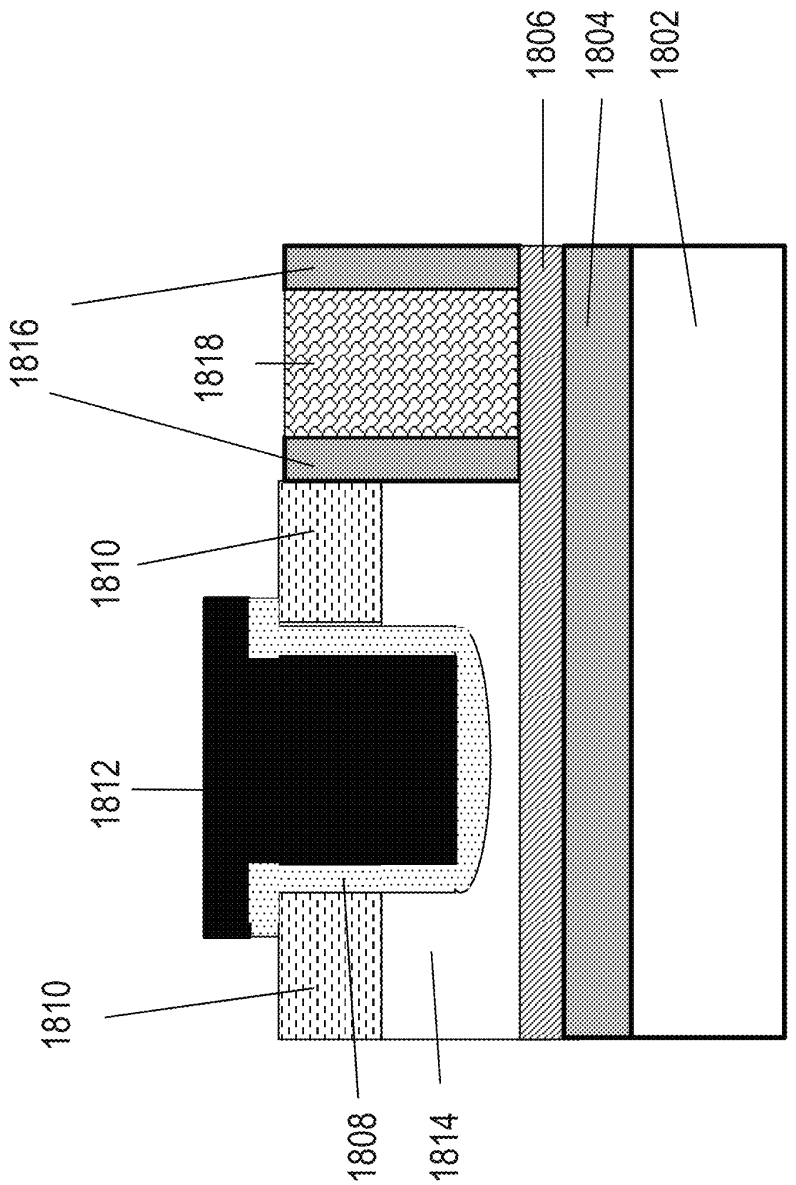


Fig. 17C

Fig. 17D



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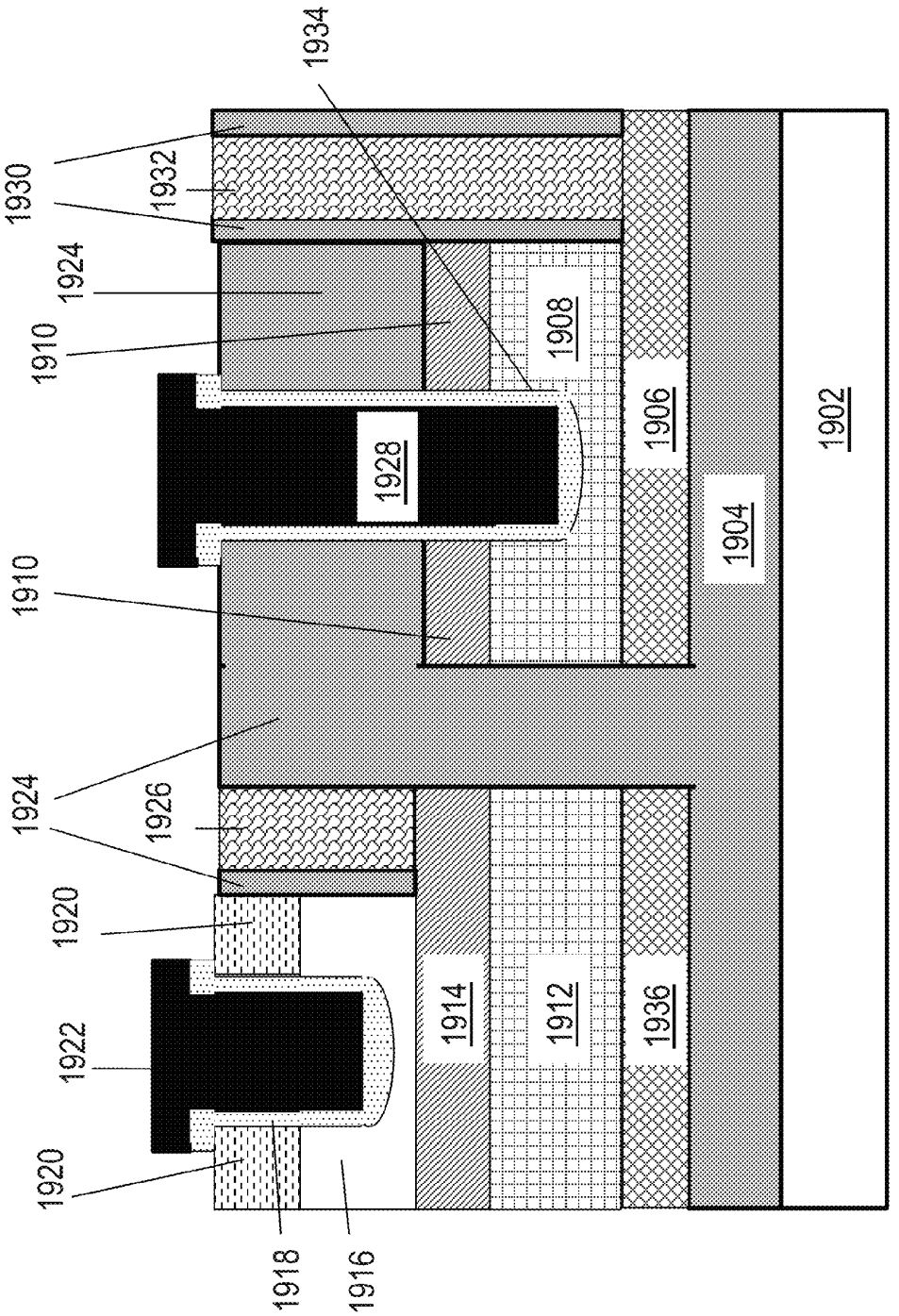
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Fig. 19

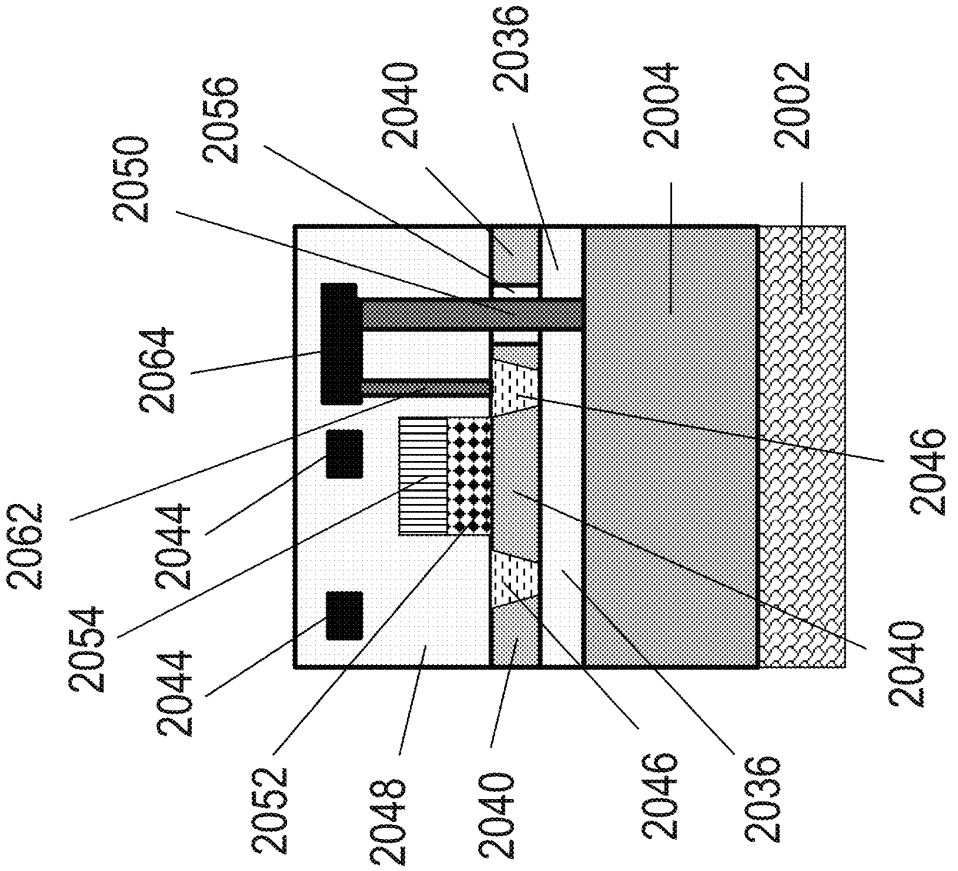
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Fig. 20

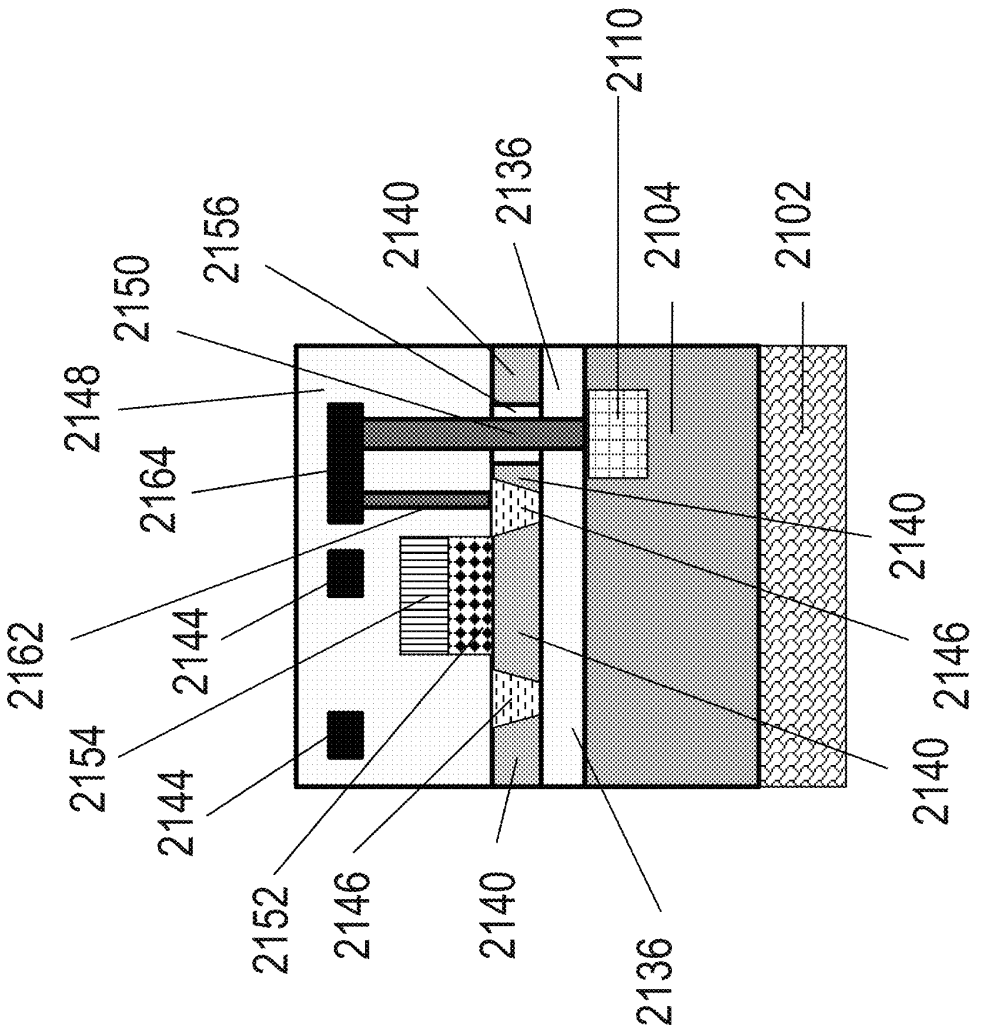
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Fig. 21

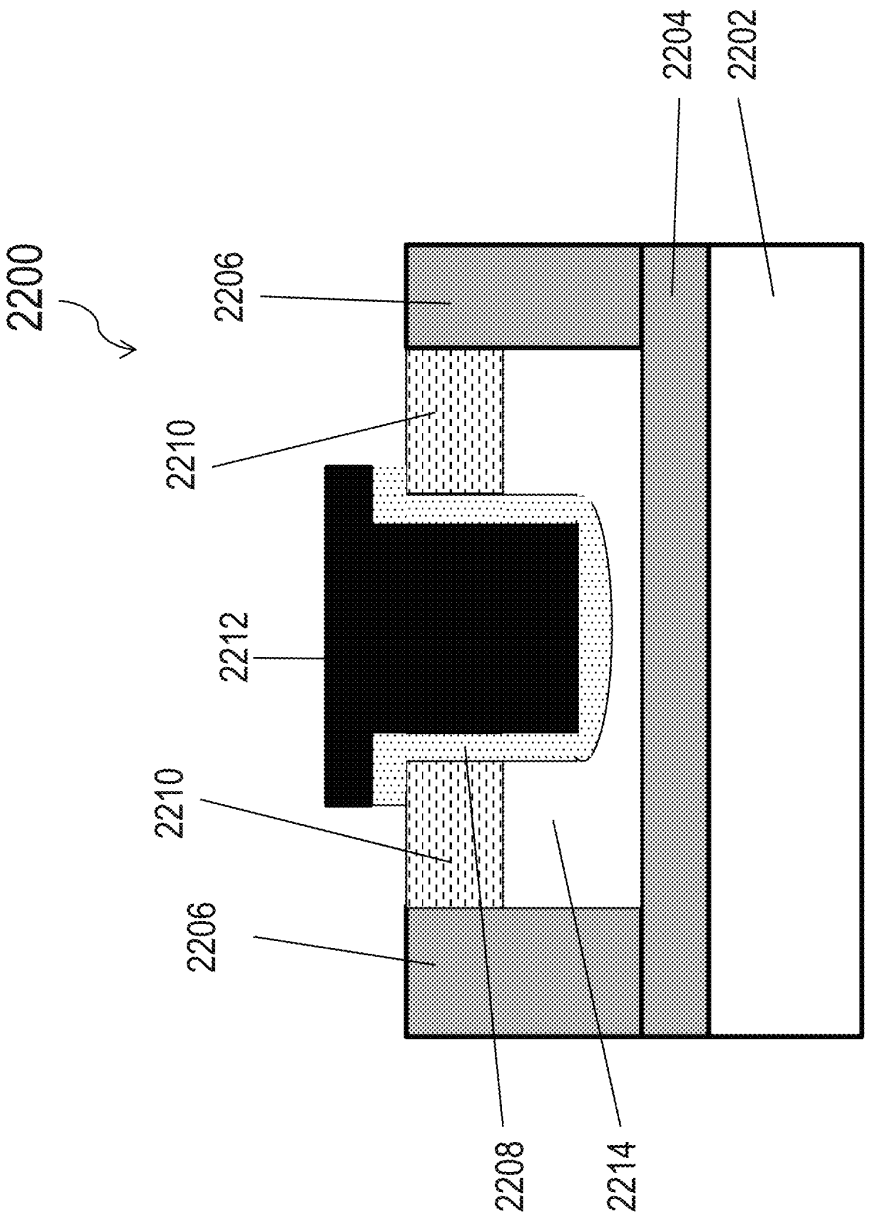

Fig. 22

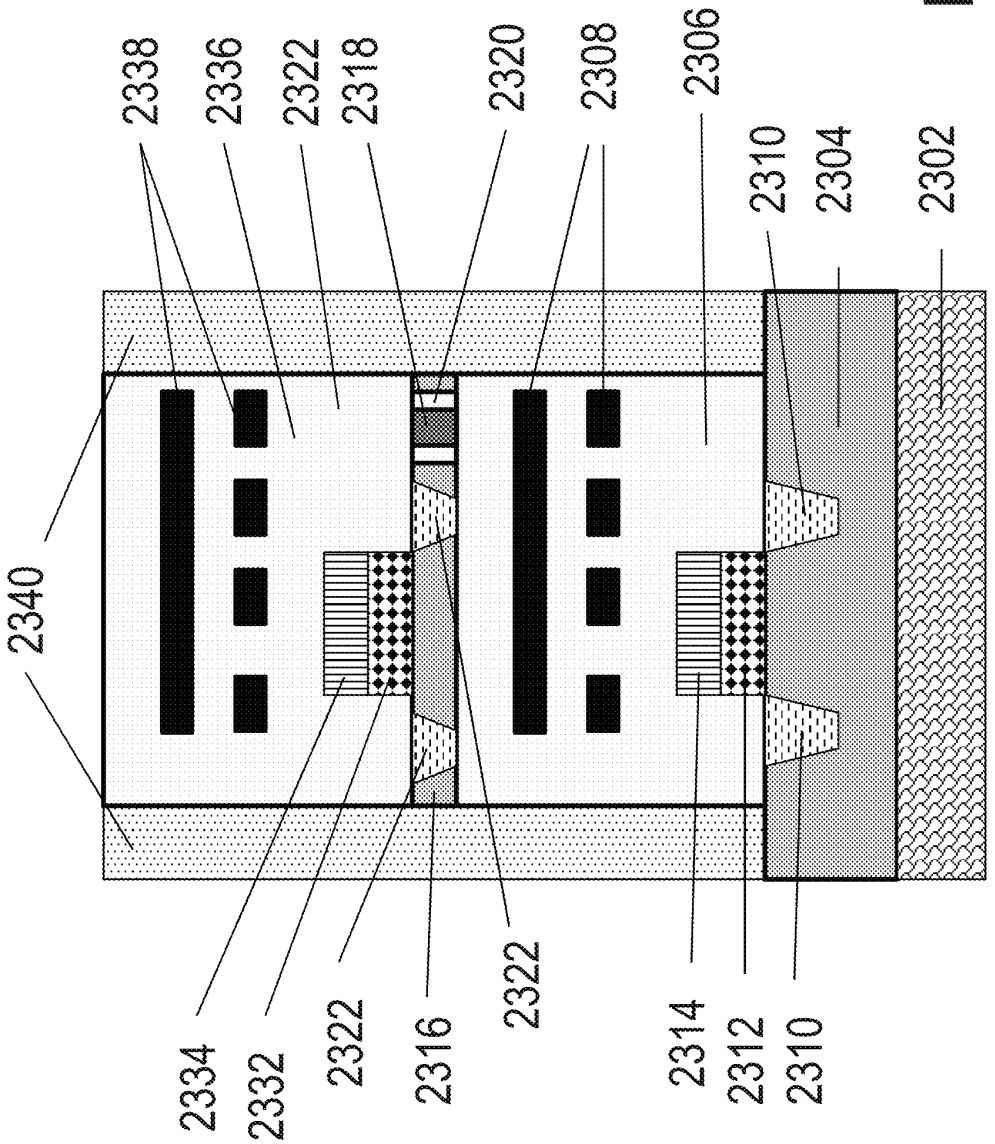
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Fig. 23

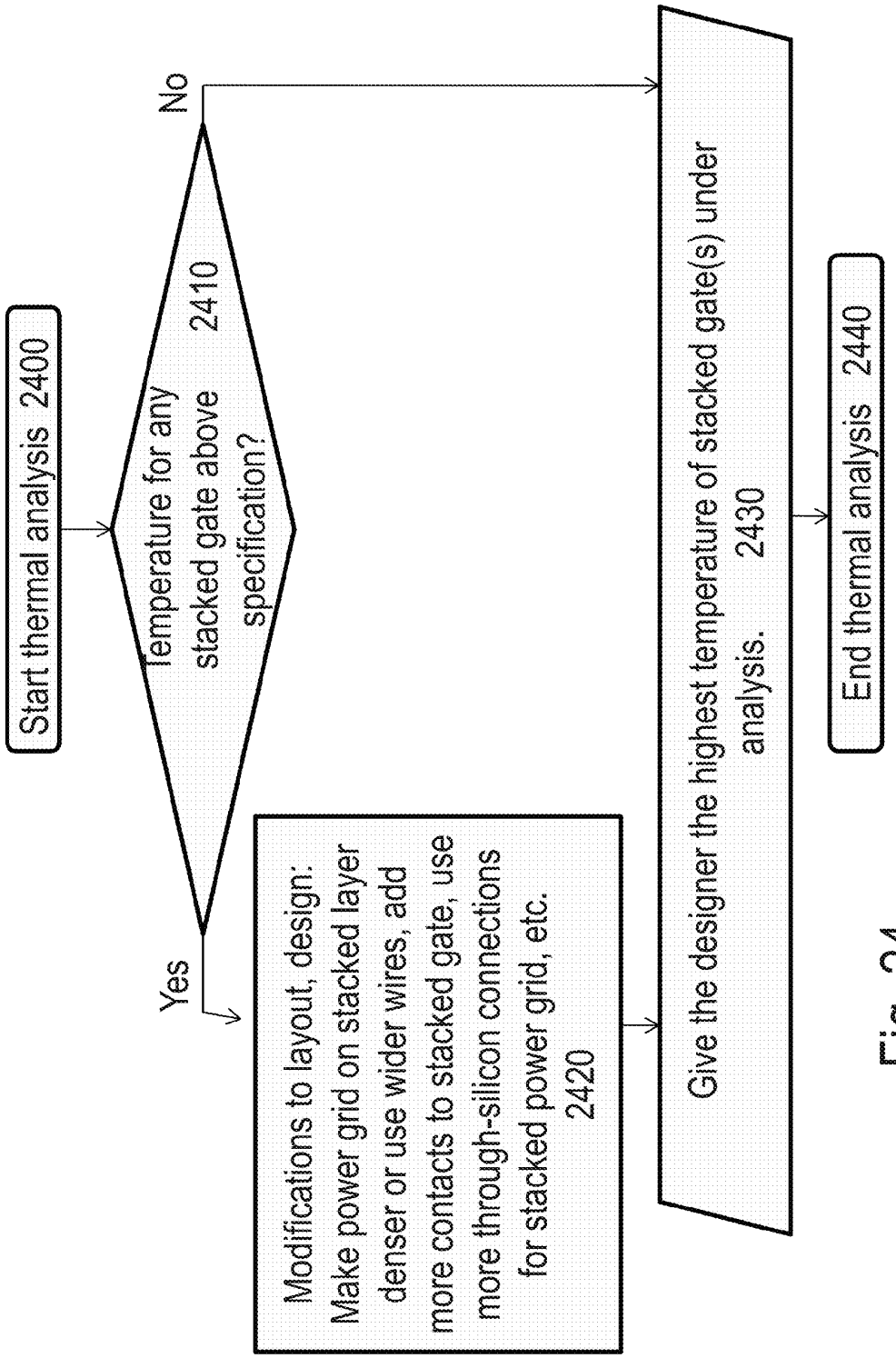
Start thermal analysis 2400
Temperature for any stacked gate above specification? 2410
No
Yes
Modifications to layout, design: Make power grid on stacked layer denser or use wider wires, add more contacts to stacked gate, use more through-silicon connections for stacked power grid, etc. 2420
Give the designer the highest temperature of stacked gate(s) under analysis. 2430
End thermal analysis 2440

Fig. 24

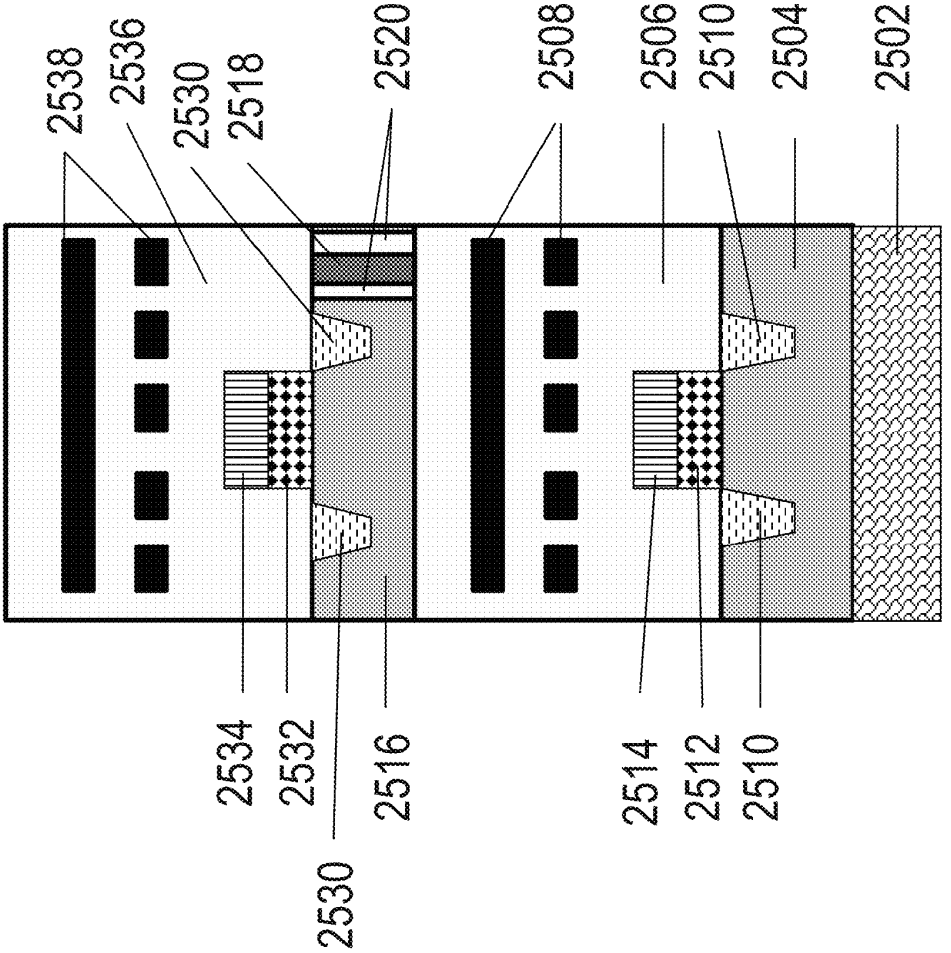
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Fig. 25

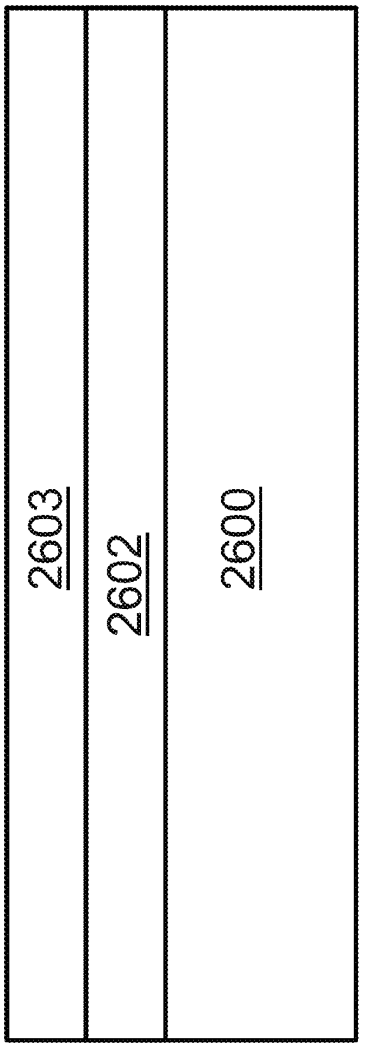

Fig. 26A

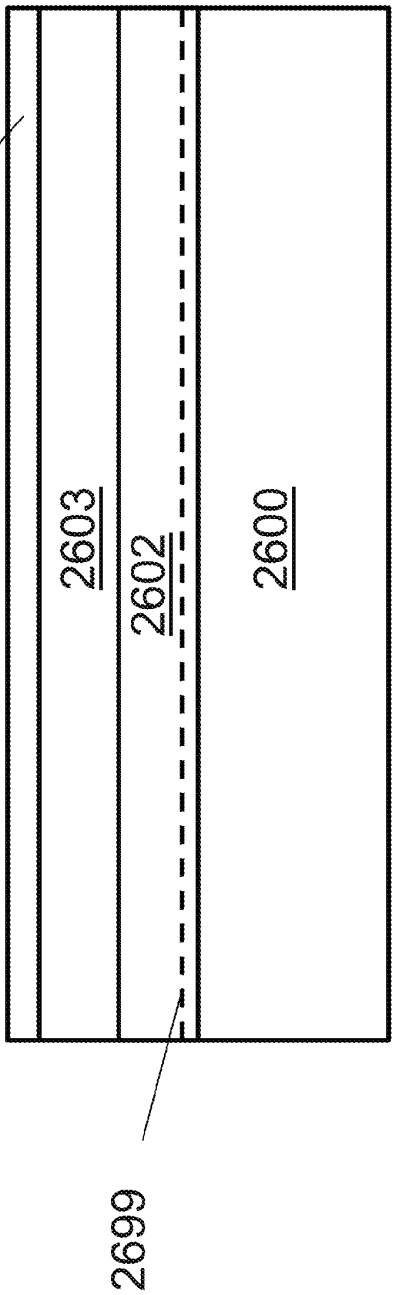

Fig. 26B

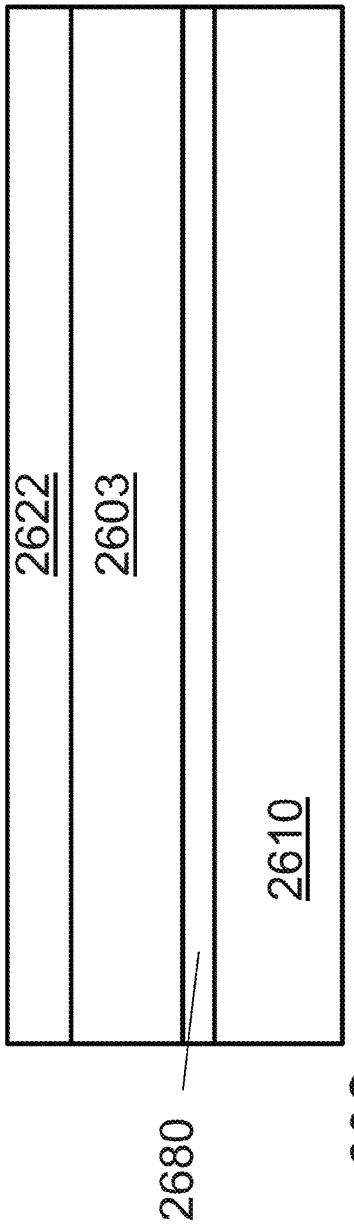

Fig. 26C

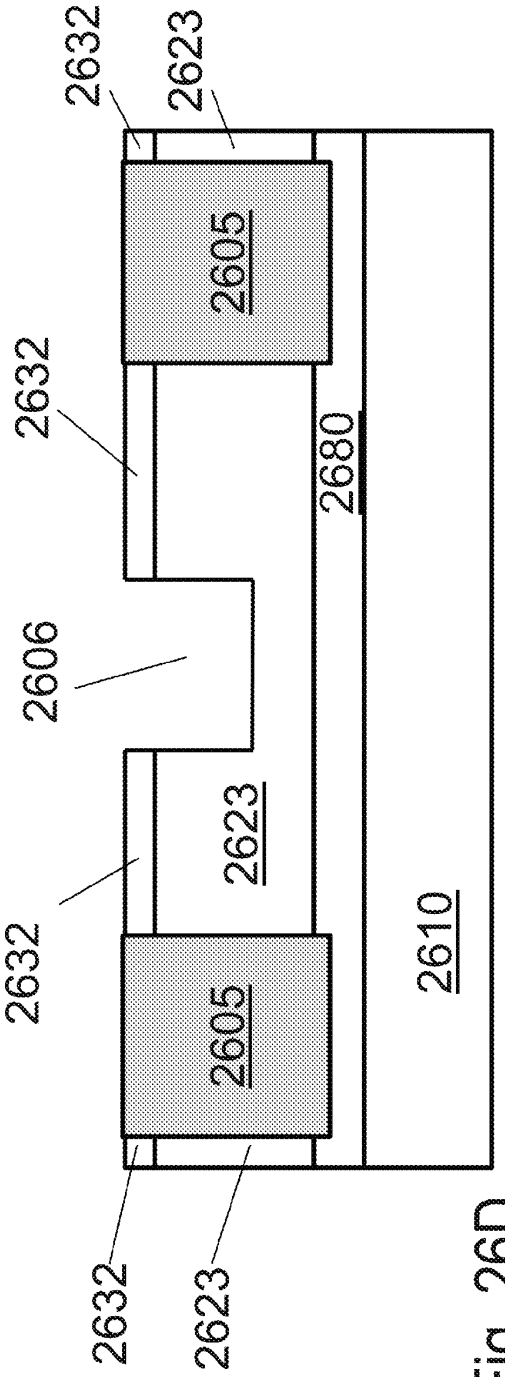

Fig. 26D

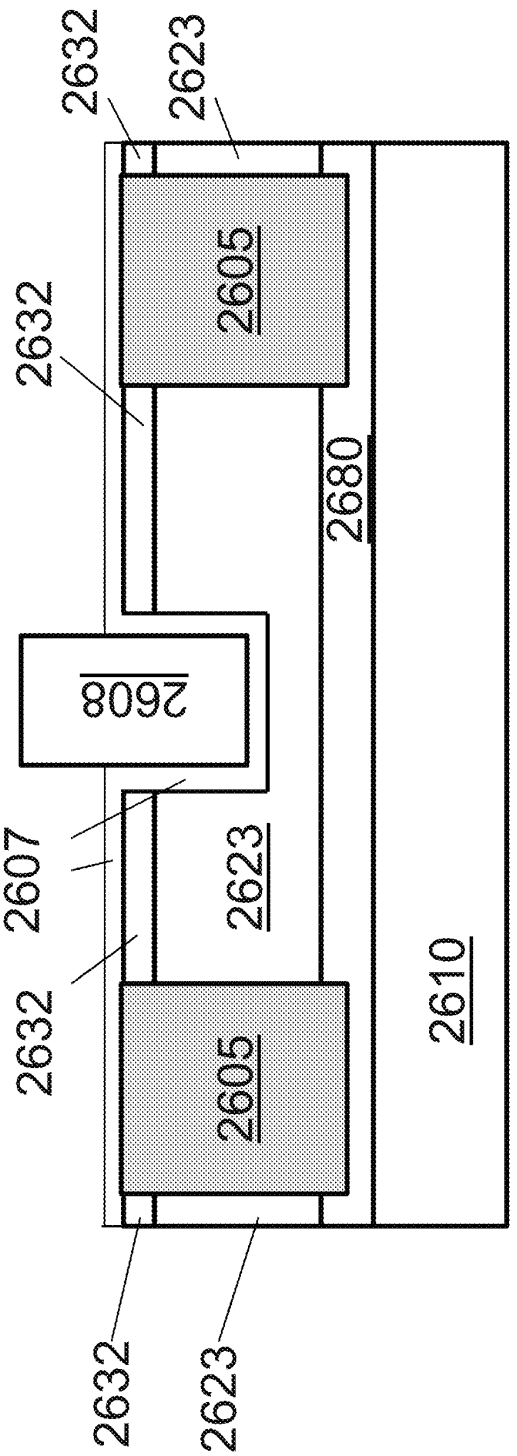
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Fig. 26E

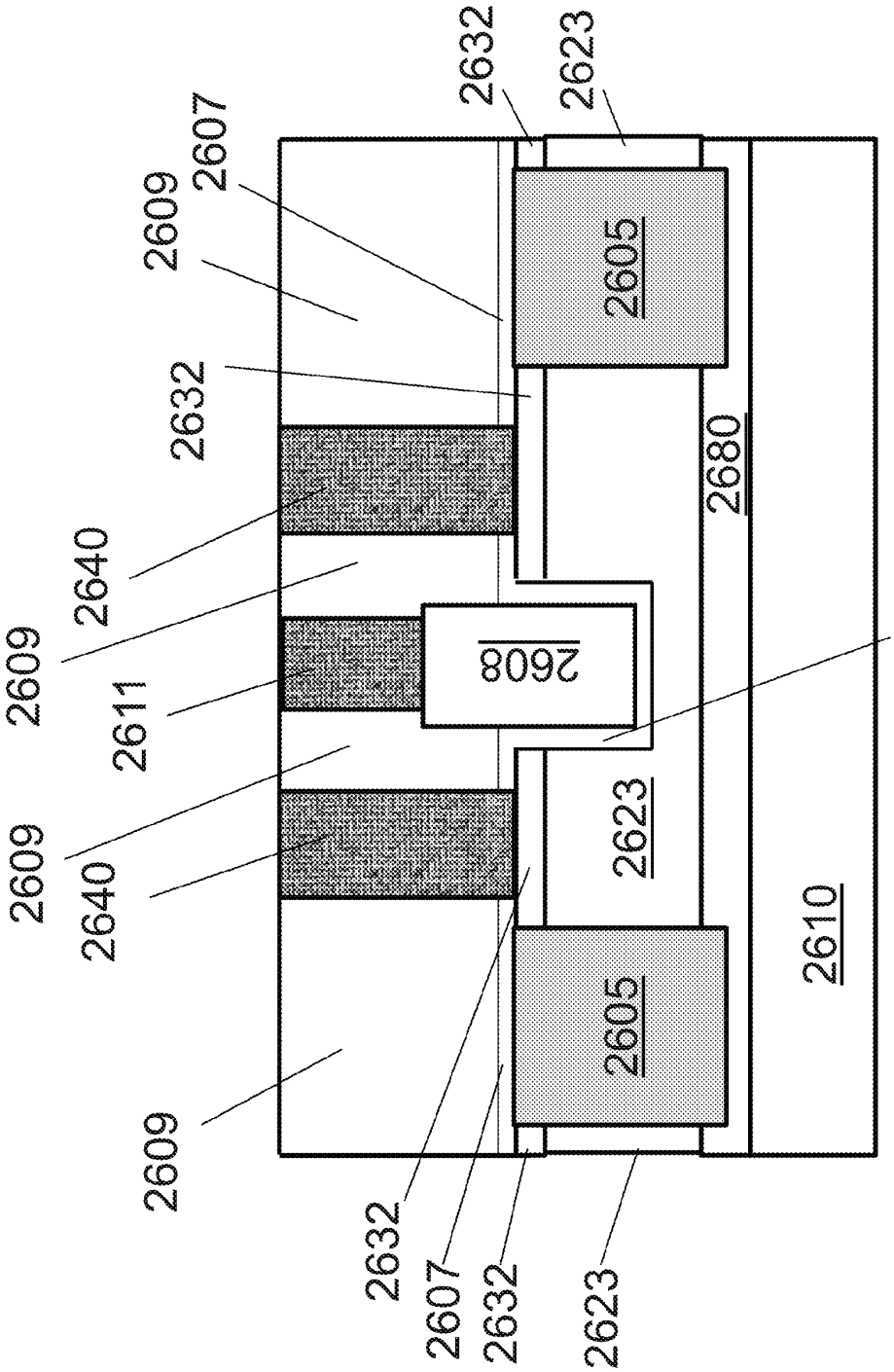
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Fig. 26F

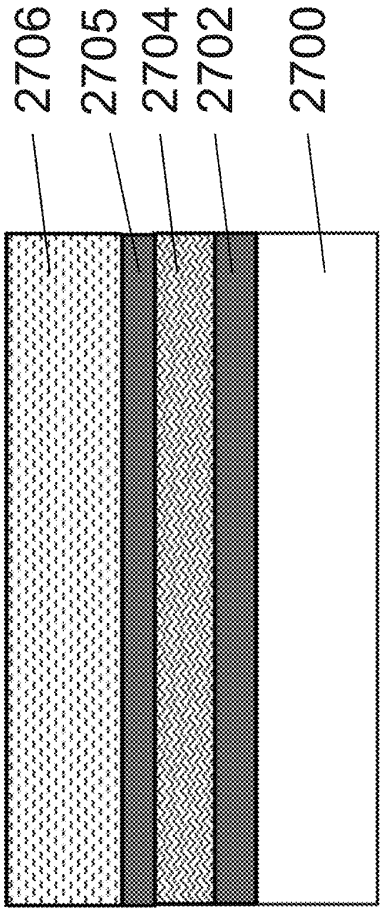

Fig. 27A

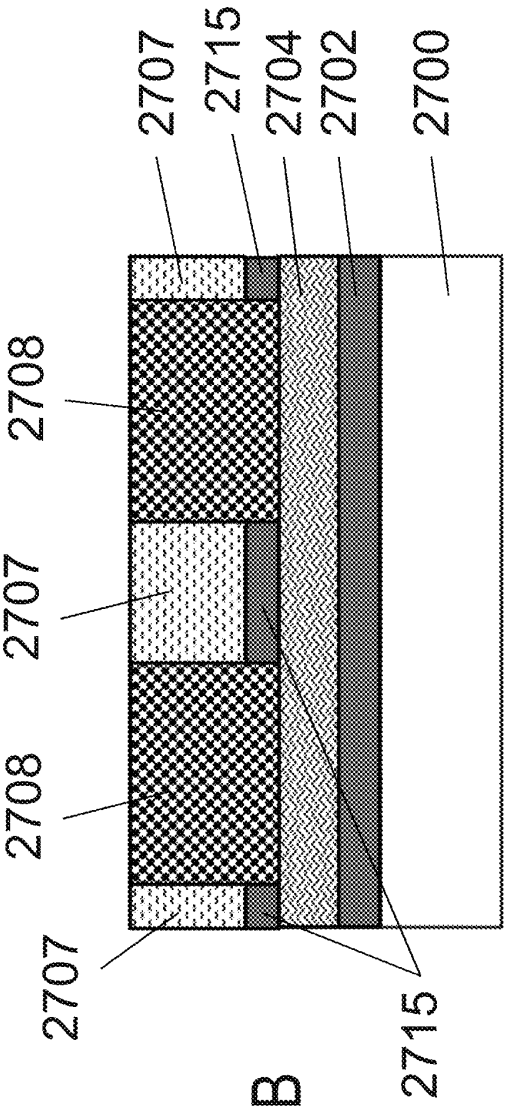

Fig. 27B

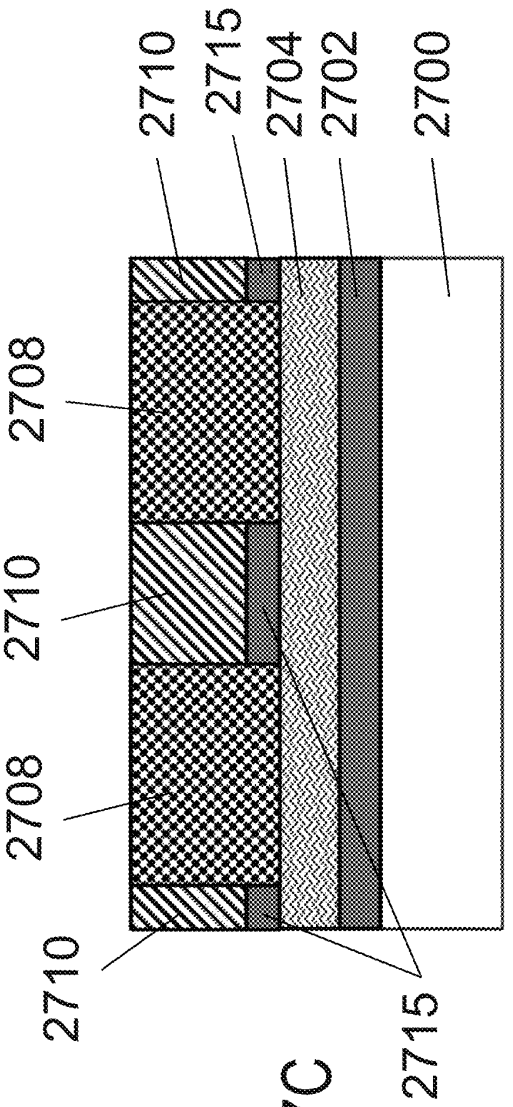

Fig. 27C

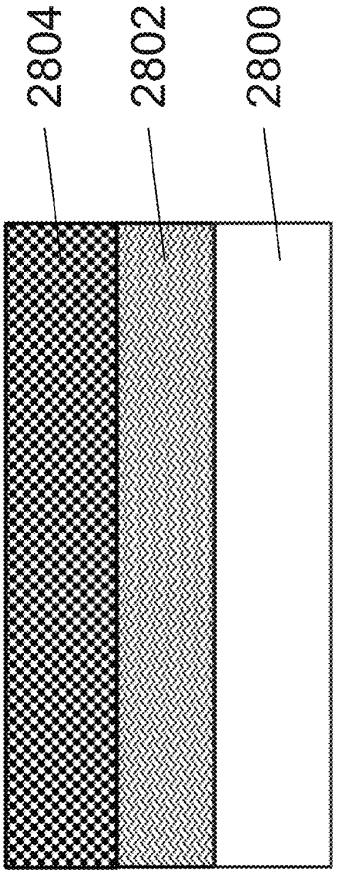

Fig. 28A

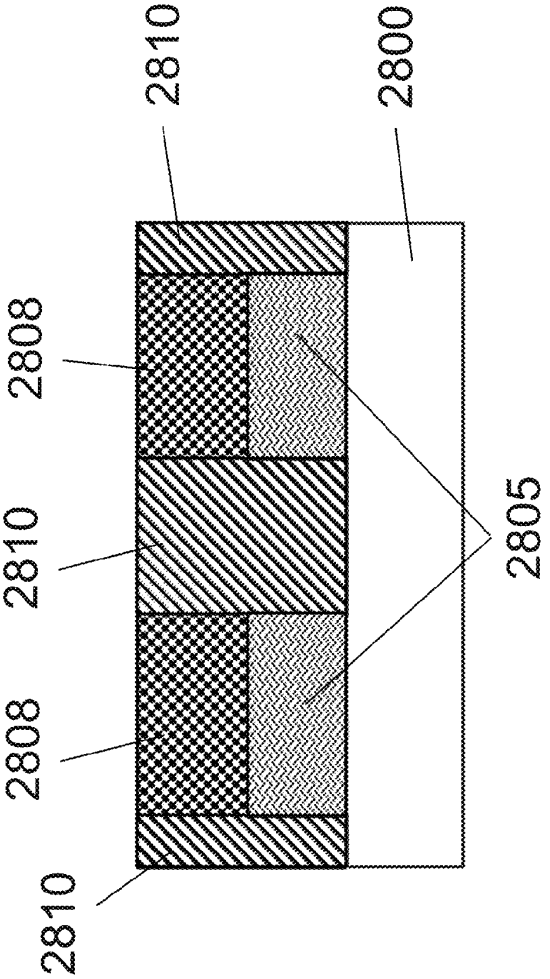

Fig. 28B

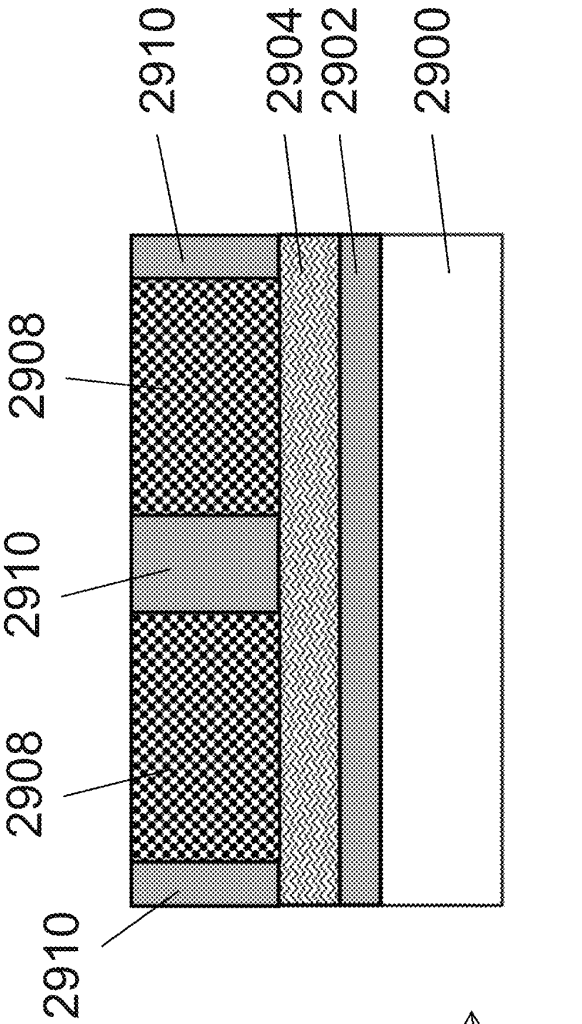

Fig. 29A

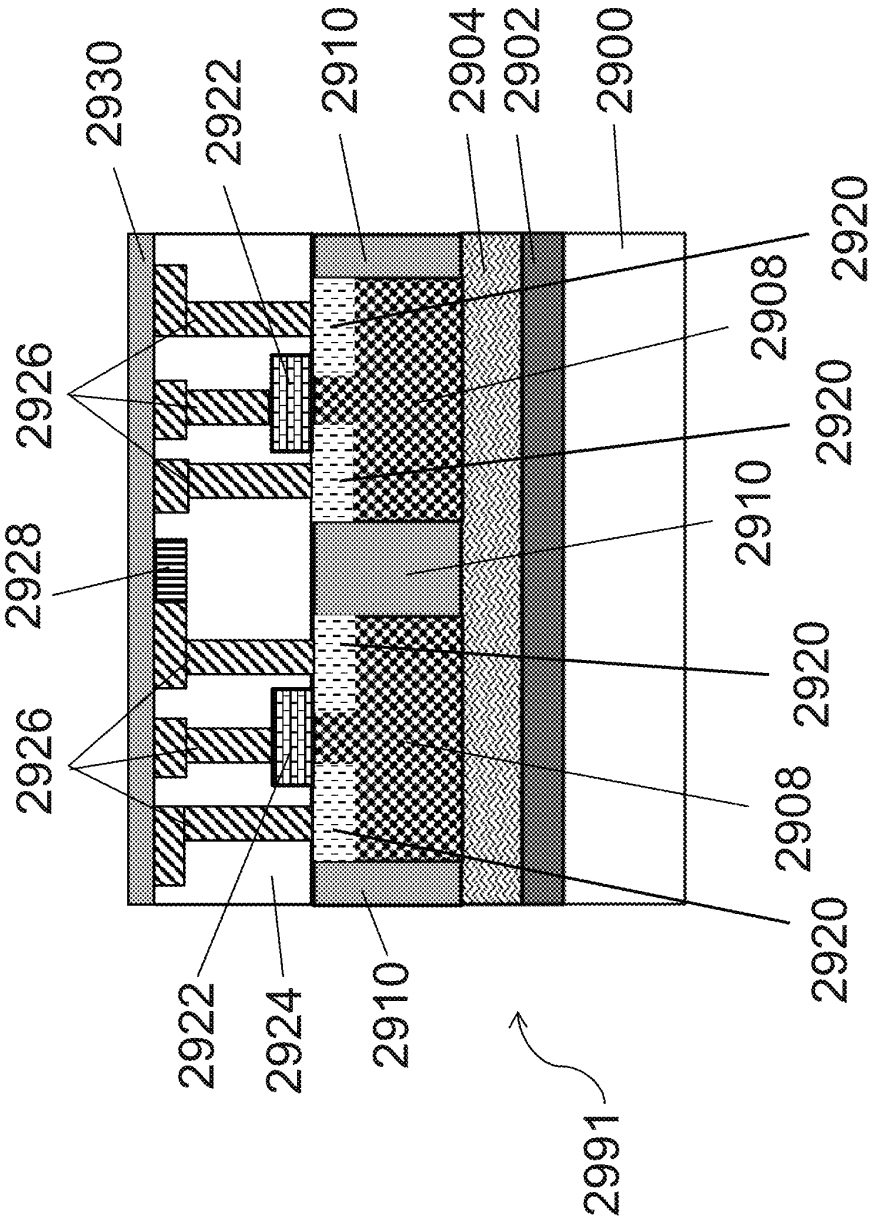
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Fig. 29B

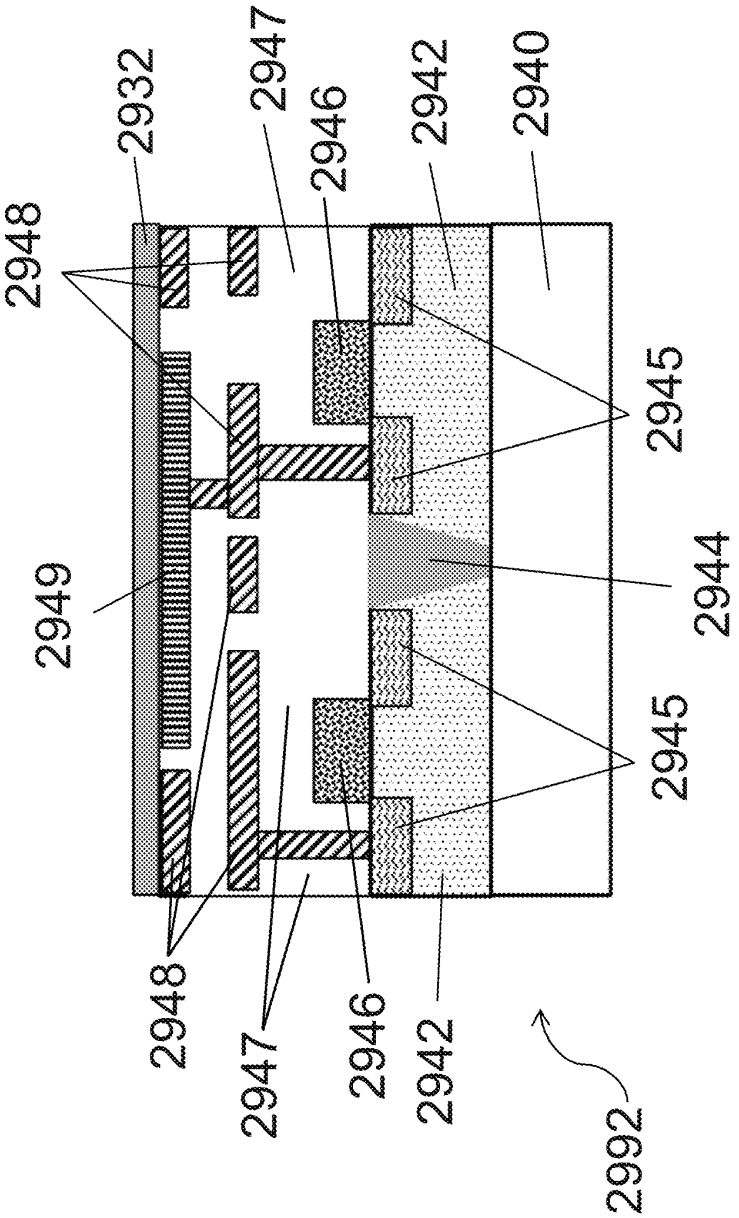
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Fig. 29C

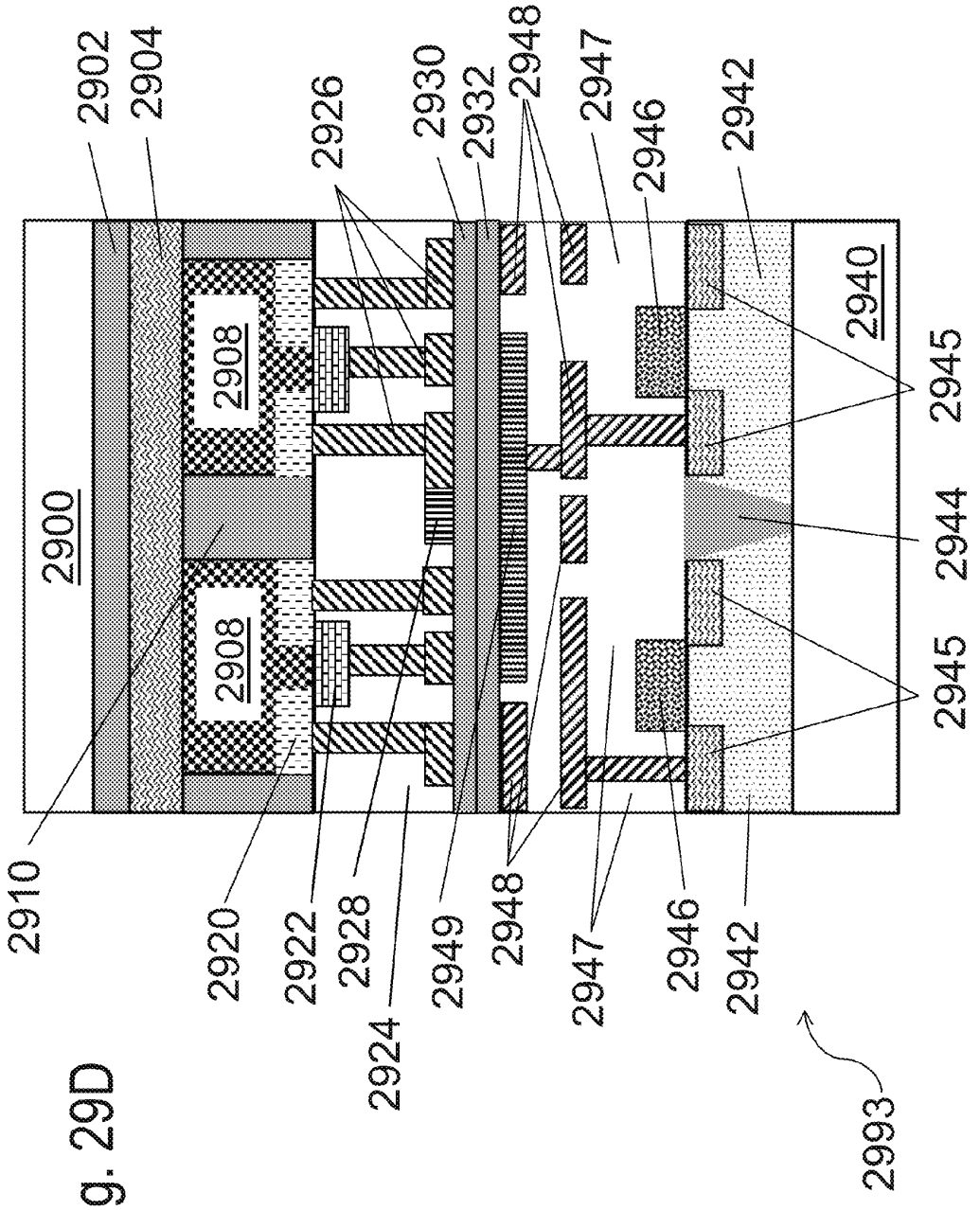
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Fig. 29D

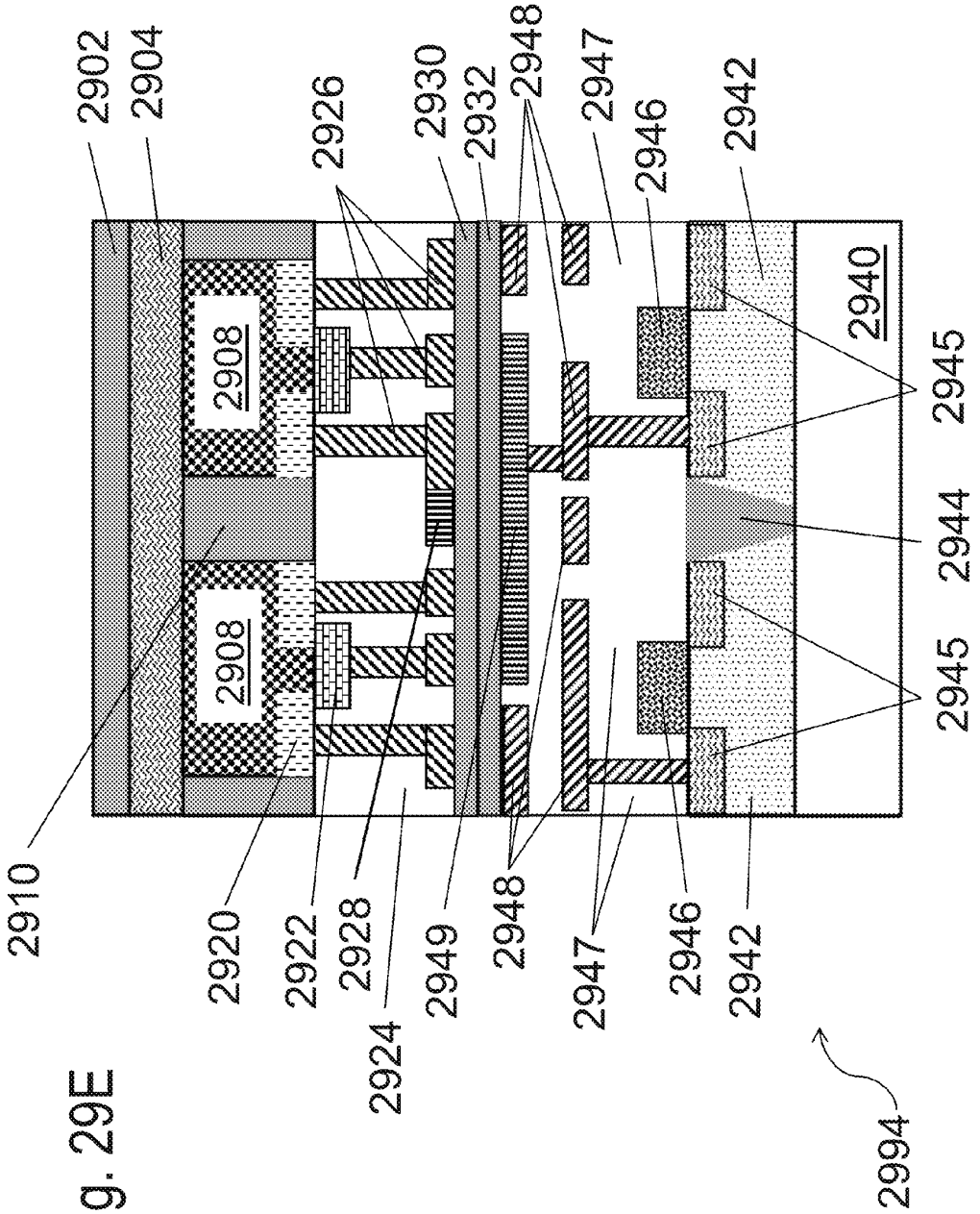
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Fig. 29E

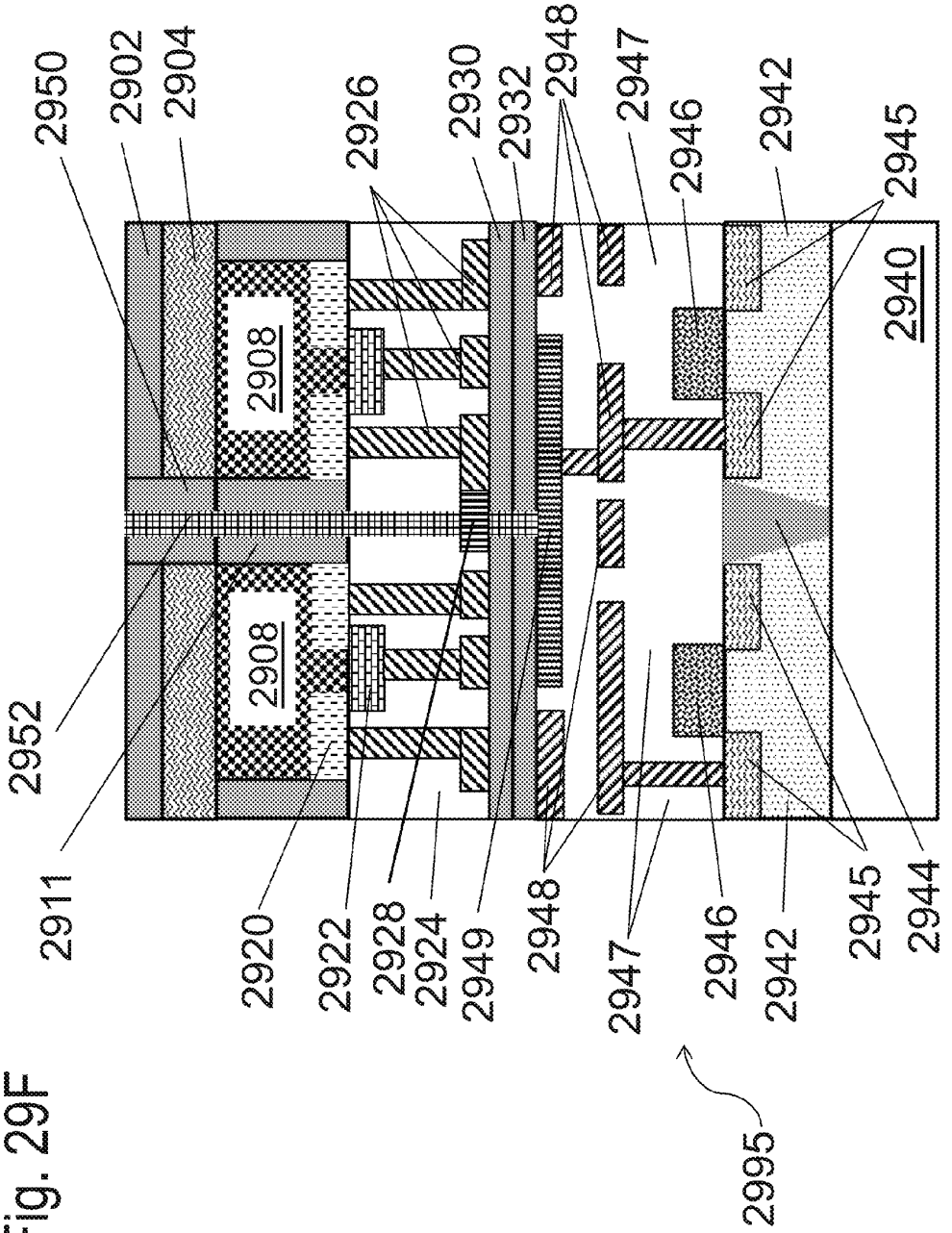
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Fig. 29F

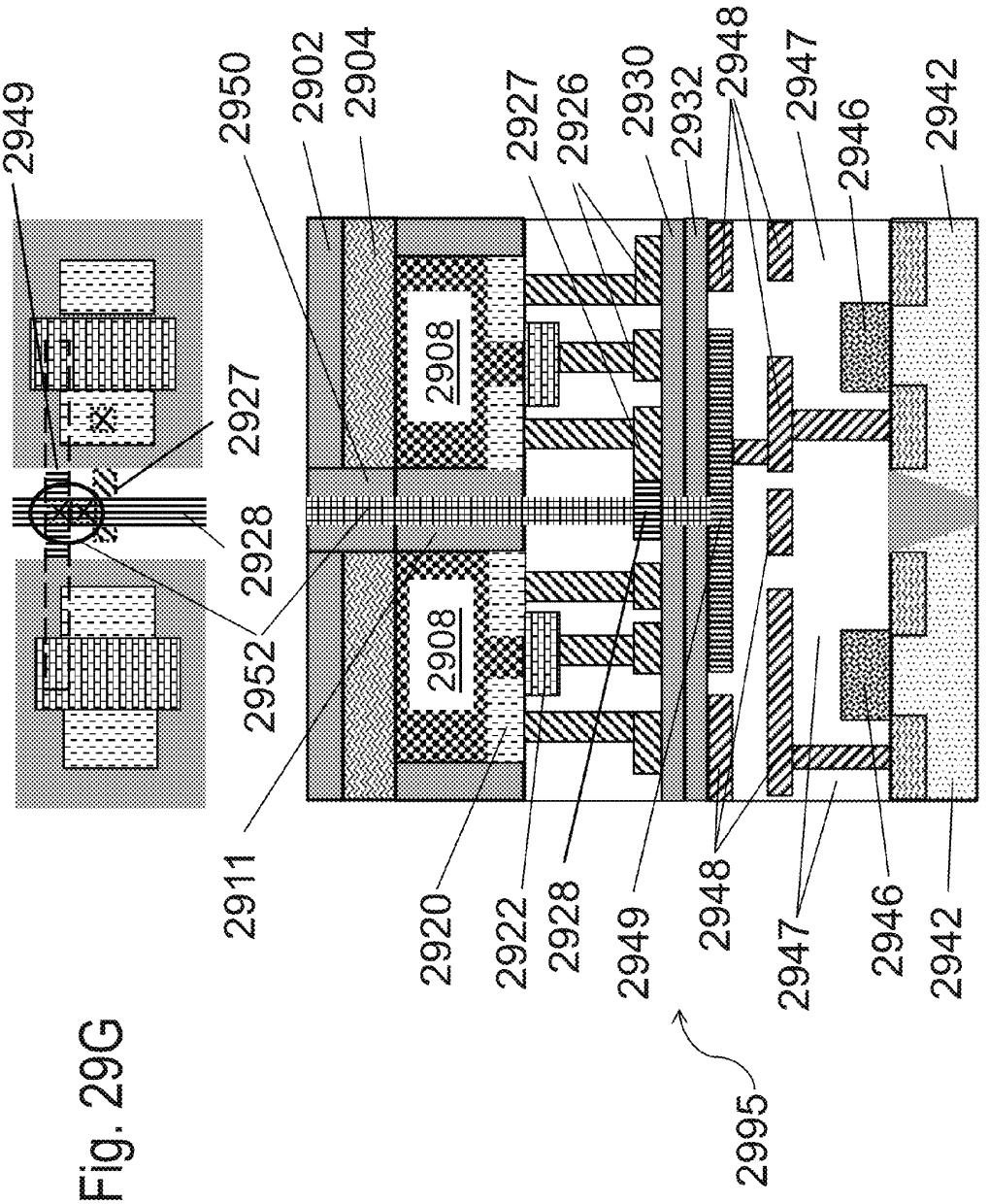
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Fig. 29G

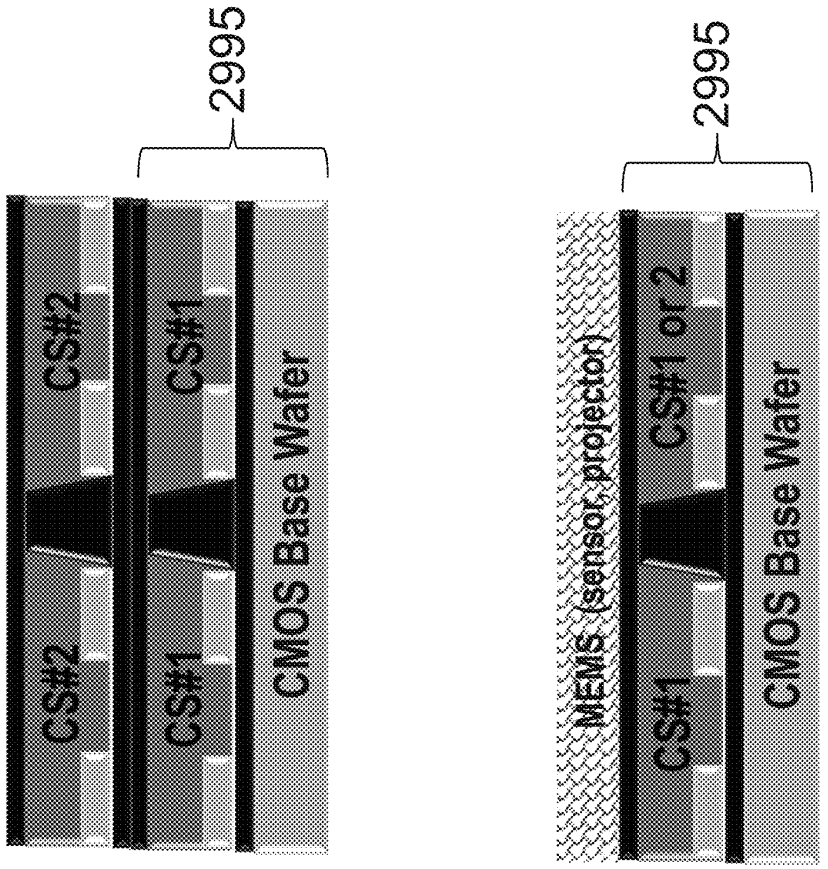
2995
CS#2
CS#2
CS#1
CS#1
CMOS Base Wafer
2995
MEMS (sensor, projector)
CS#1
CS#1 or 2
CMOS Base Wafer

Fig. 29H

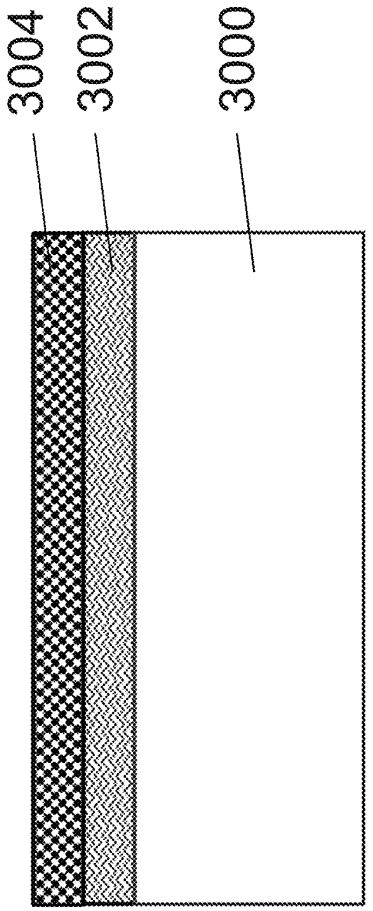

Fig. 30

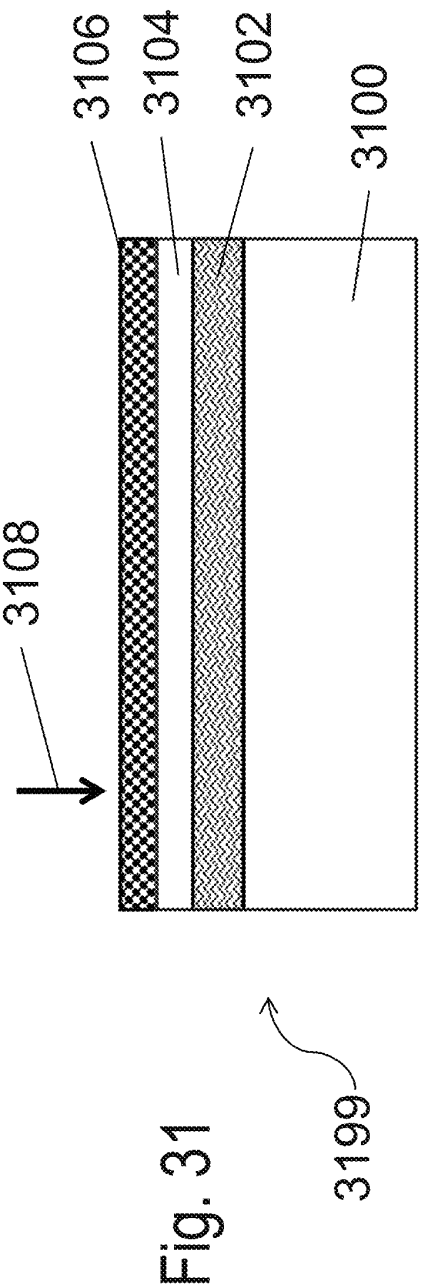

Fig. 31

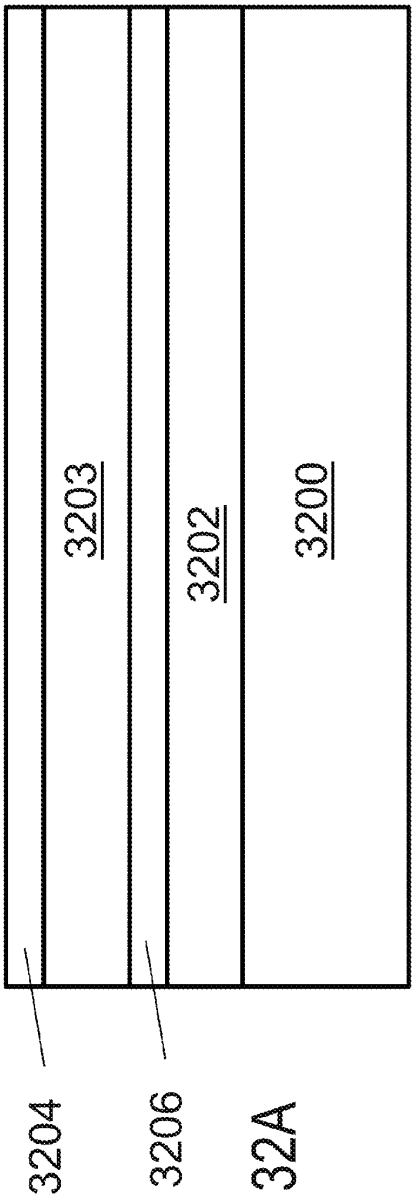

Fig. 32A

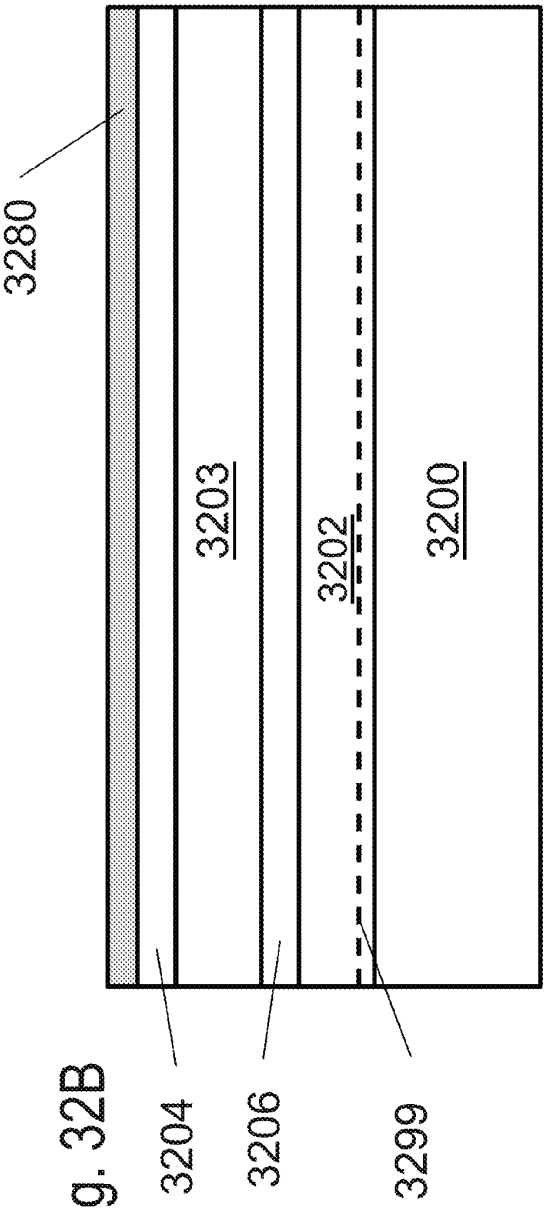

Fig. 32B

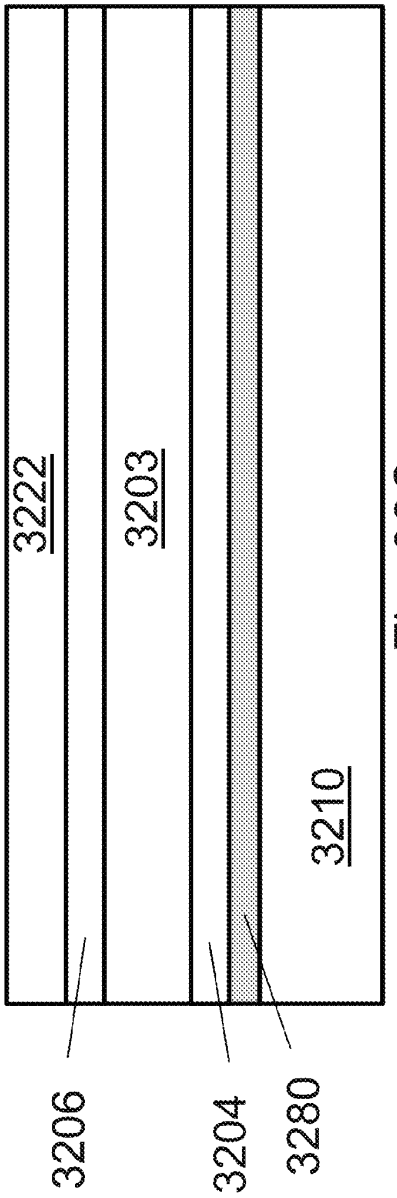

Fig. 32C

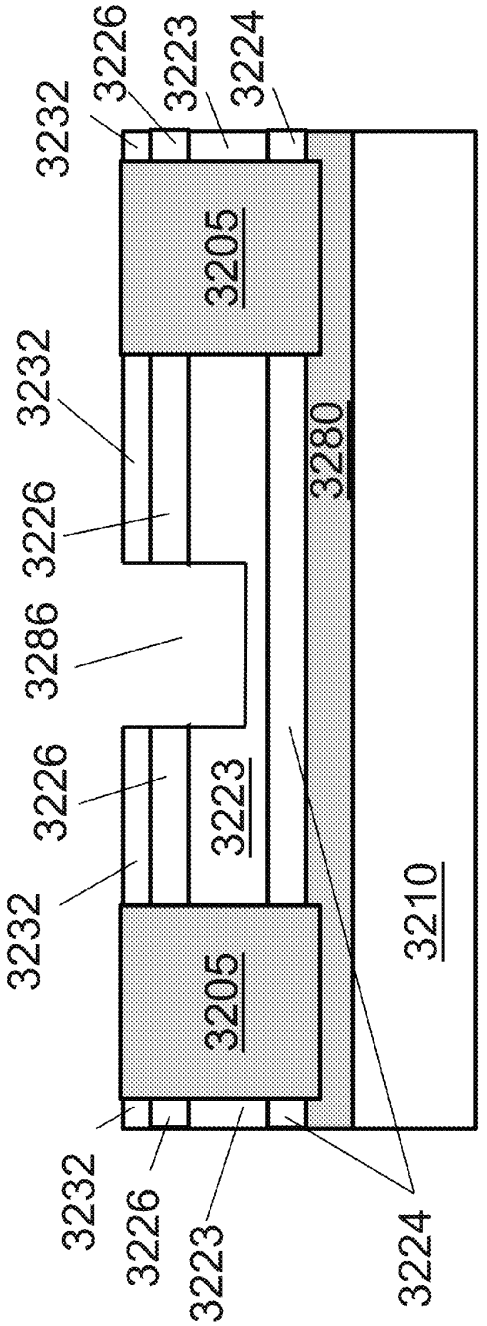

Fig. 32D

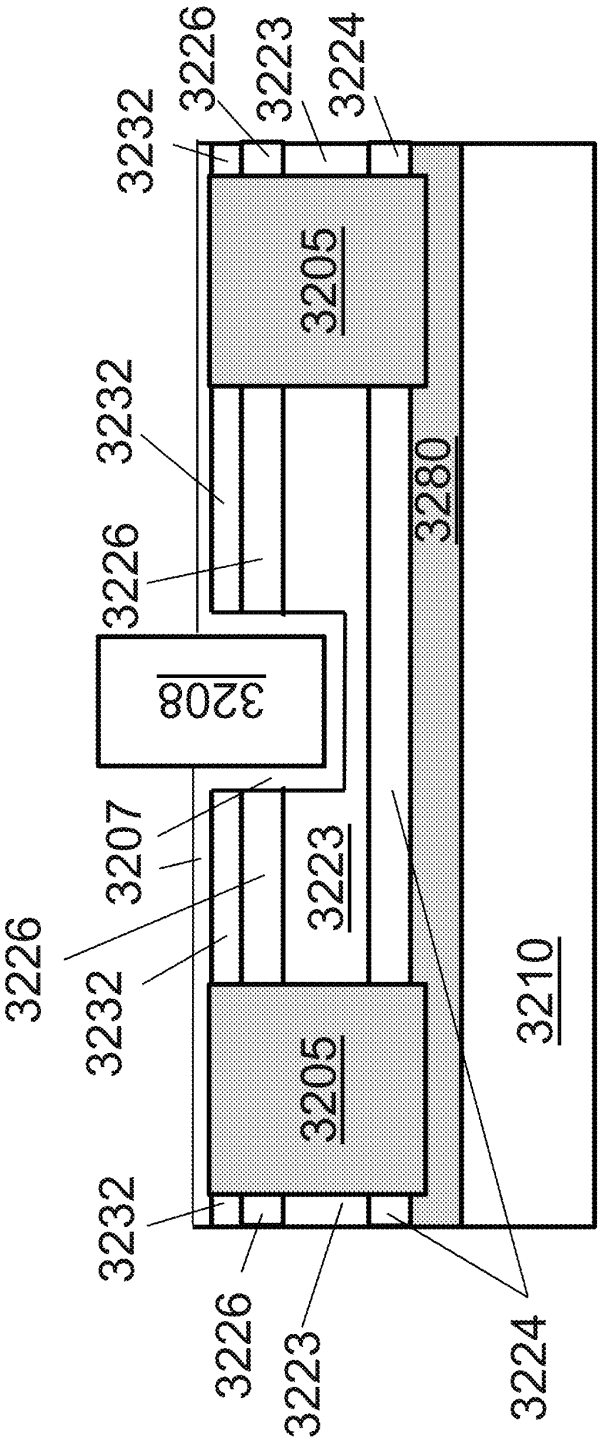
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Fig. 32E

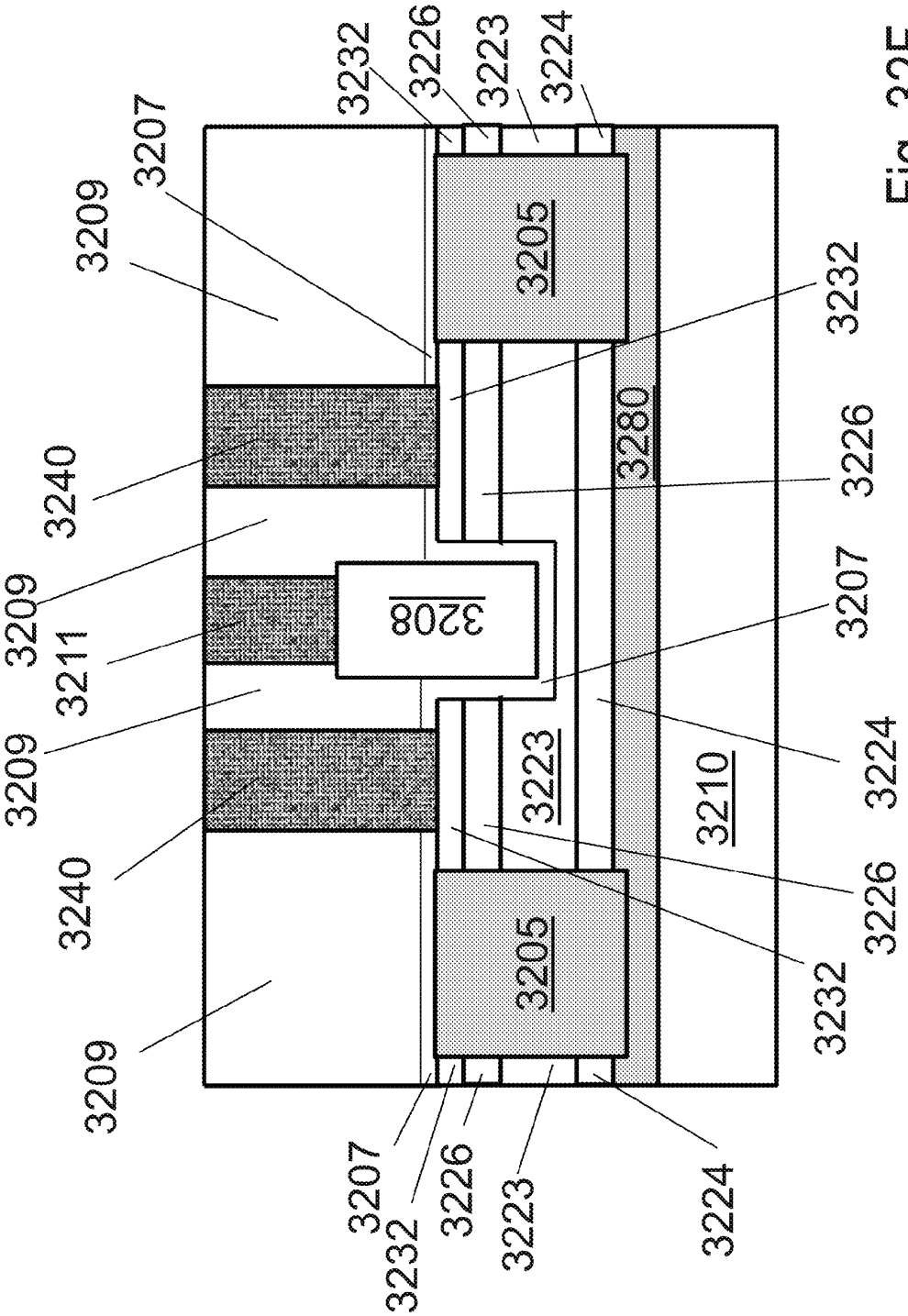
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Fig. 32F

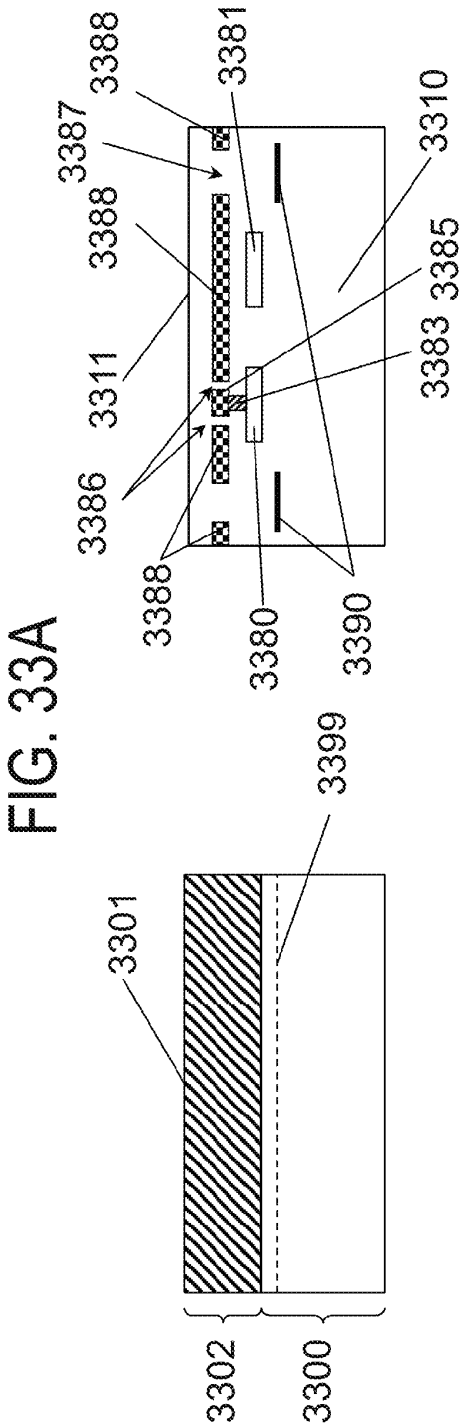


FIG. 33A

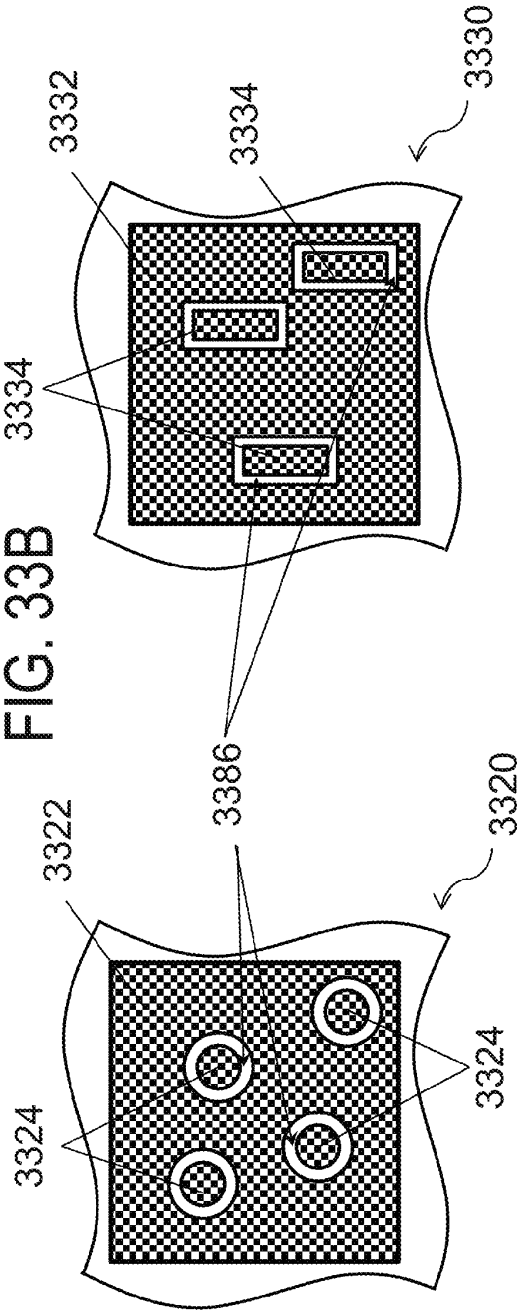


FIG. 33B

FIG. 33D

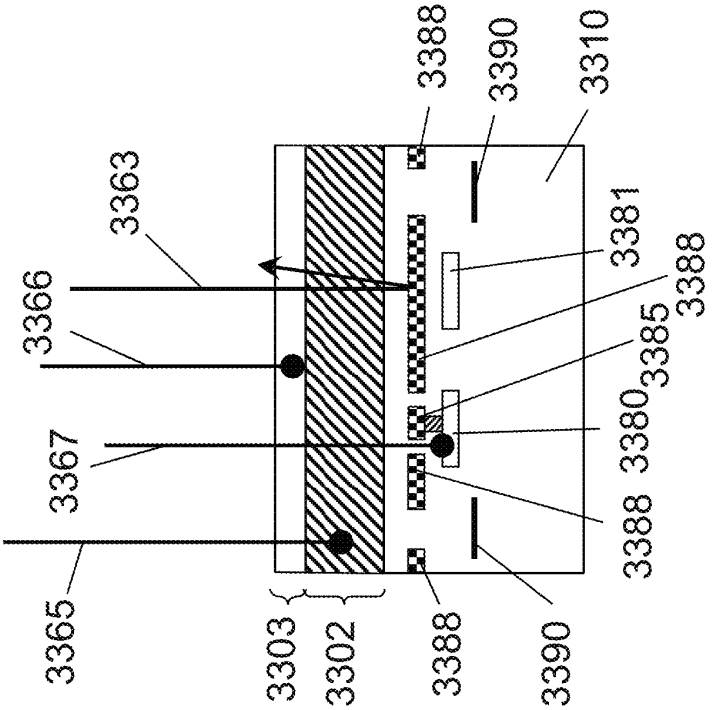


FIG. 33C

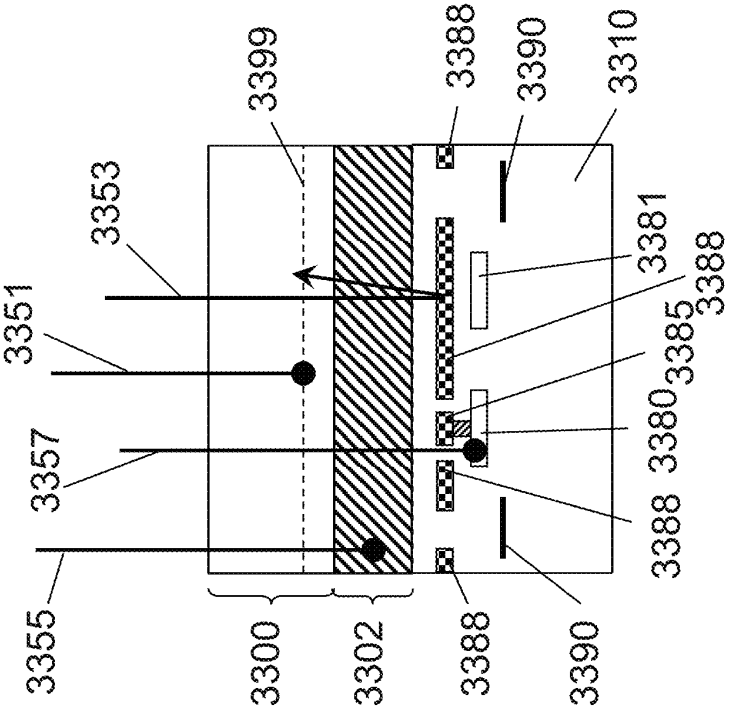


FIG. 33E

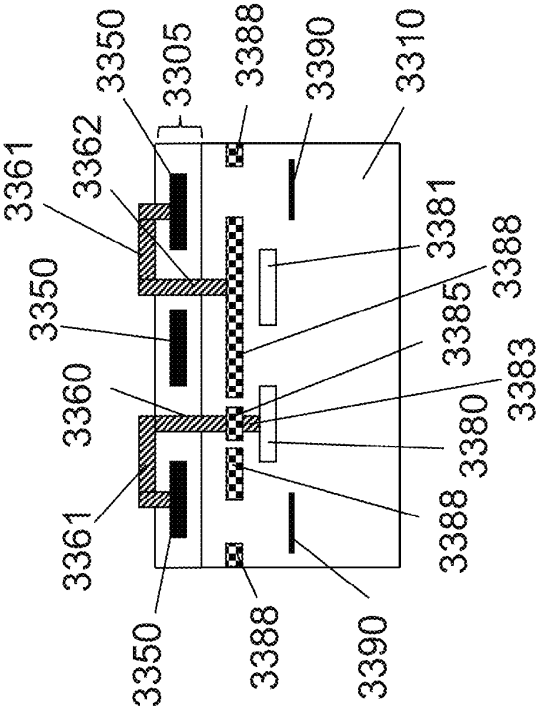
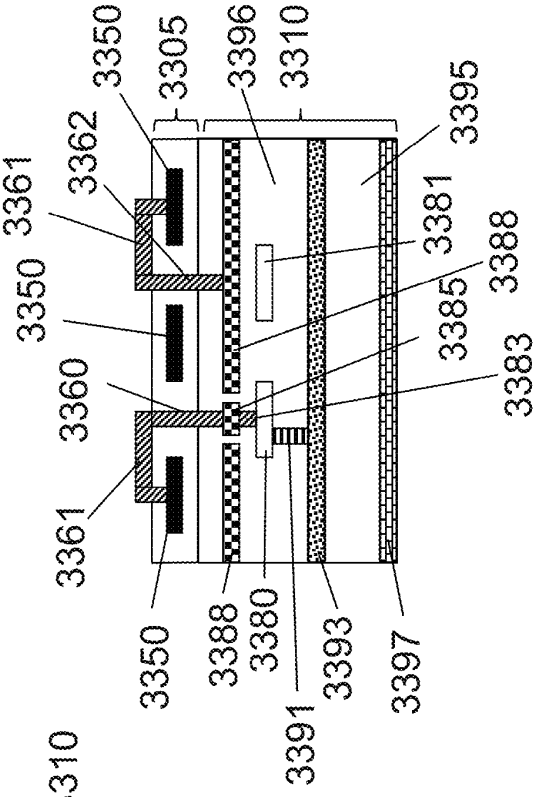


FIG. 33F



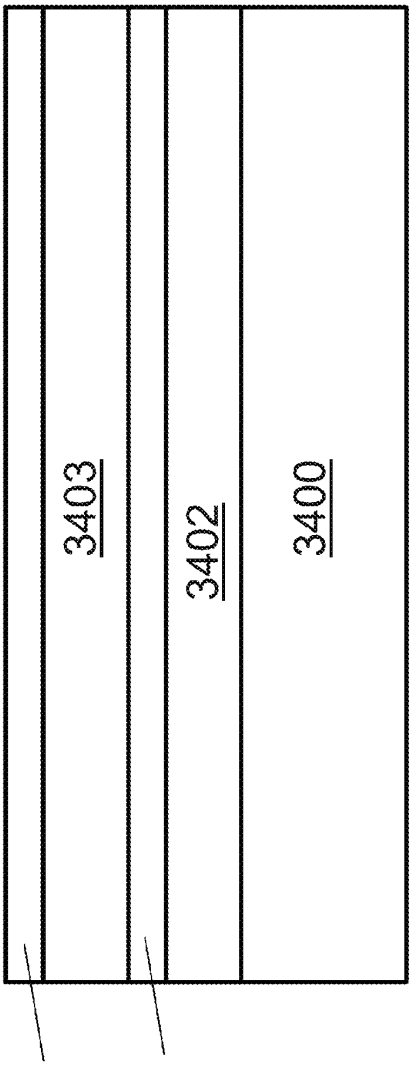


Fig. 34A

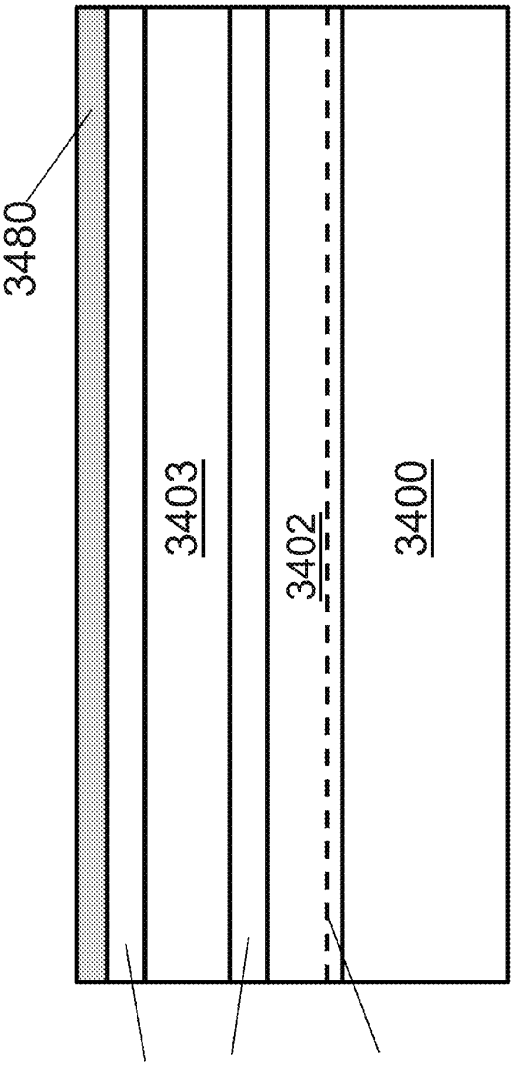


Fig. 34B

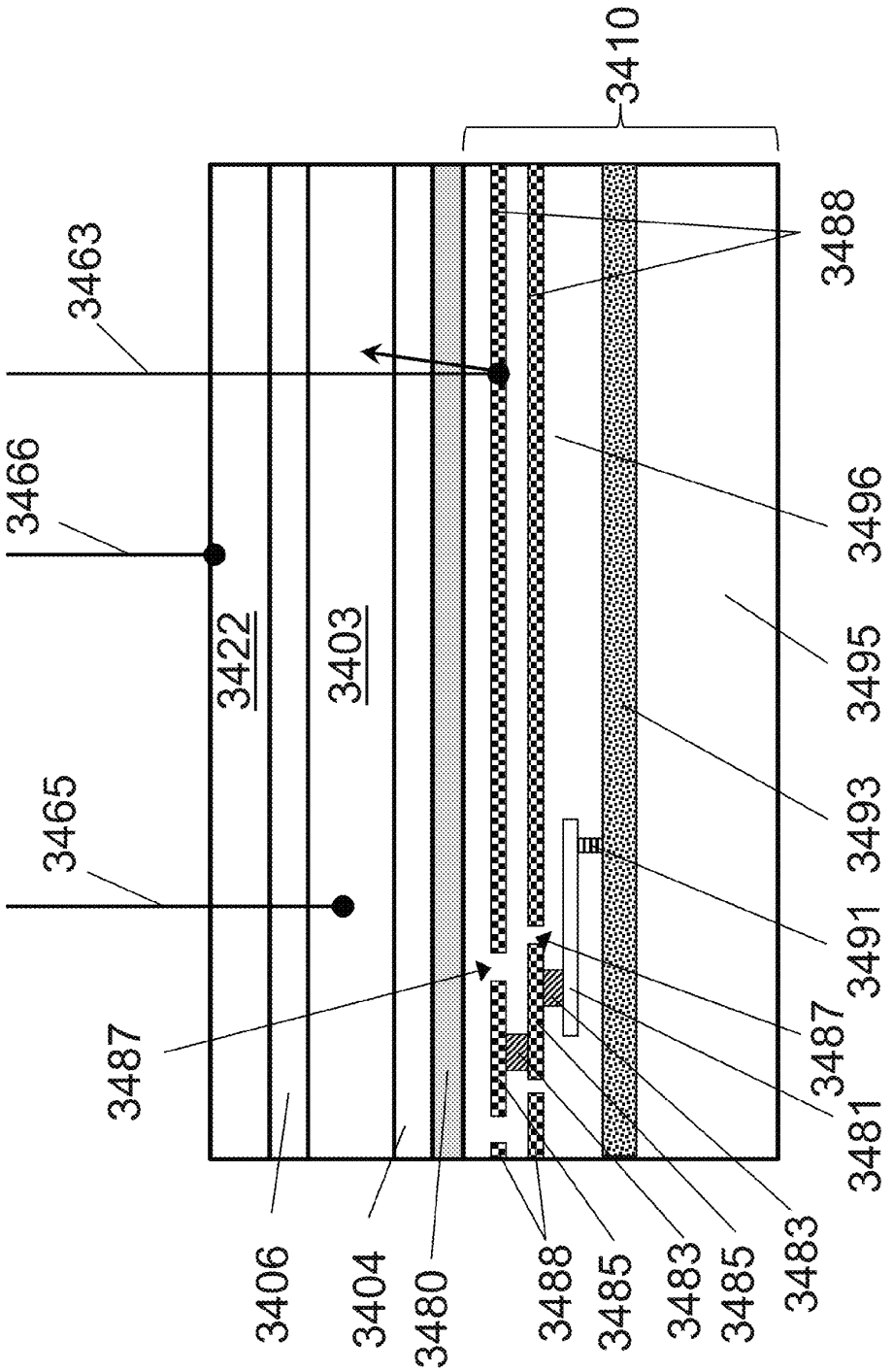

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Fig. 34C

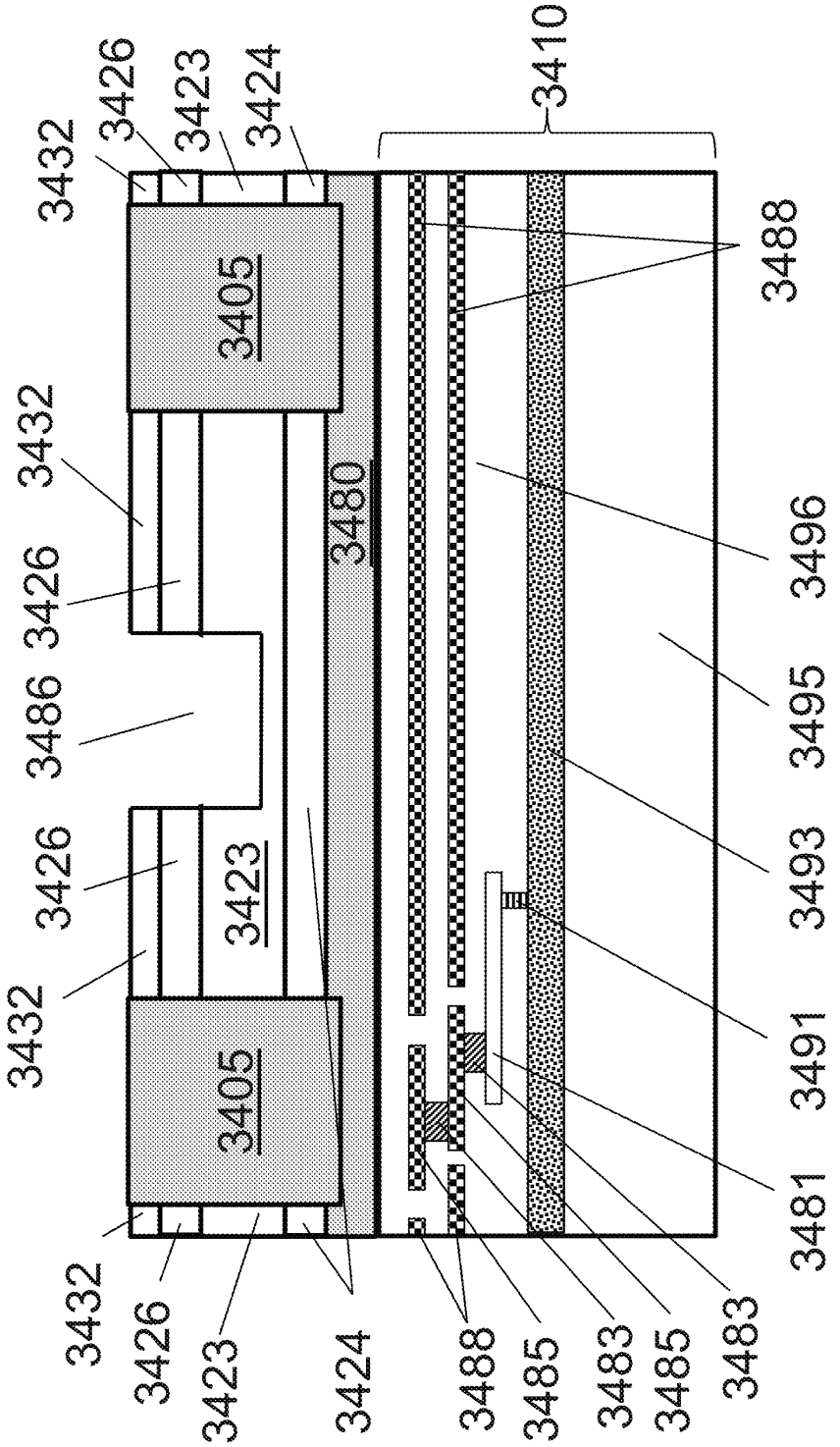
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Fig. 34D

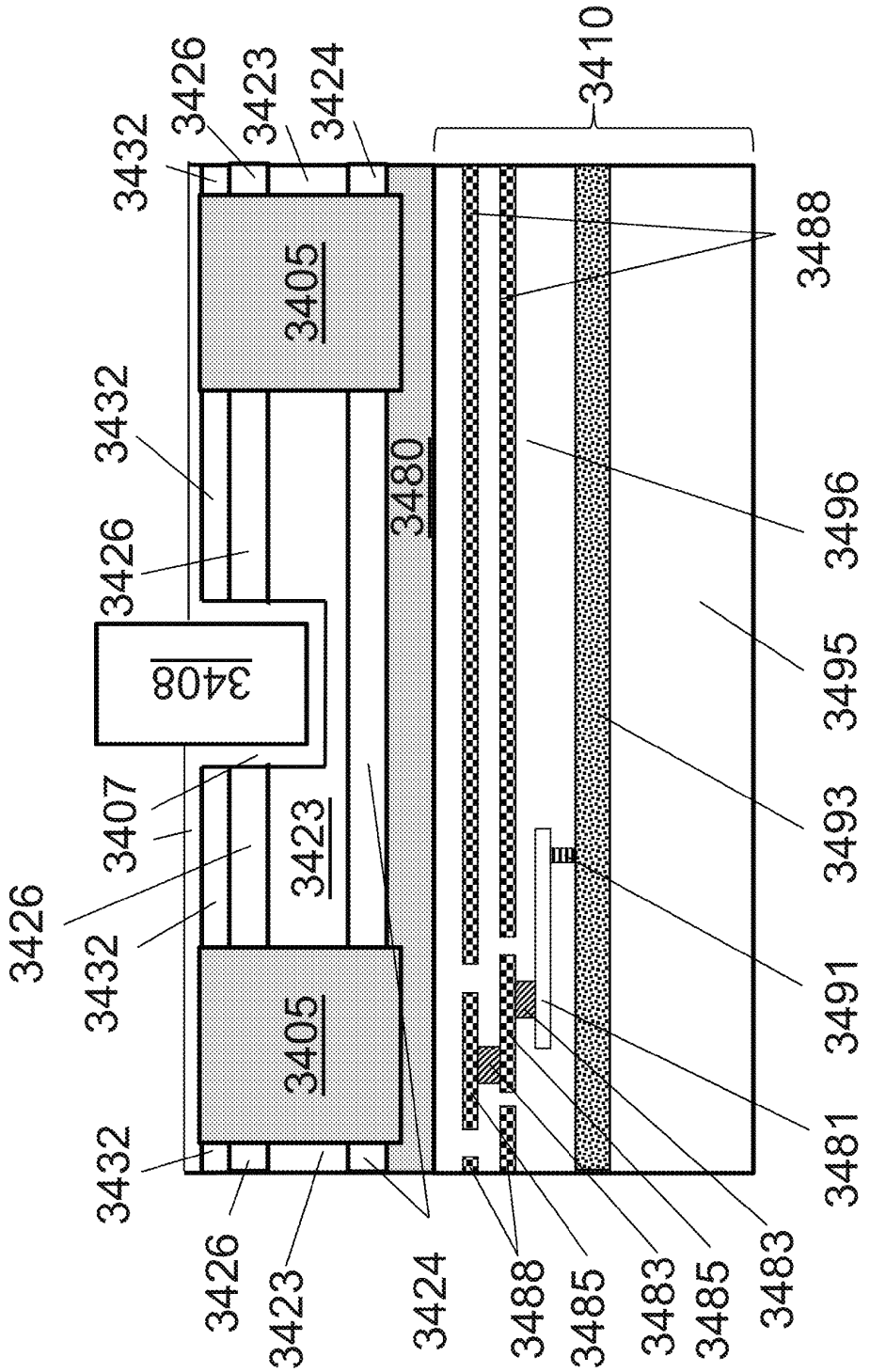
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Fig. 34E

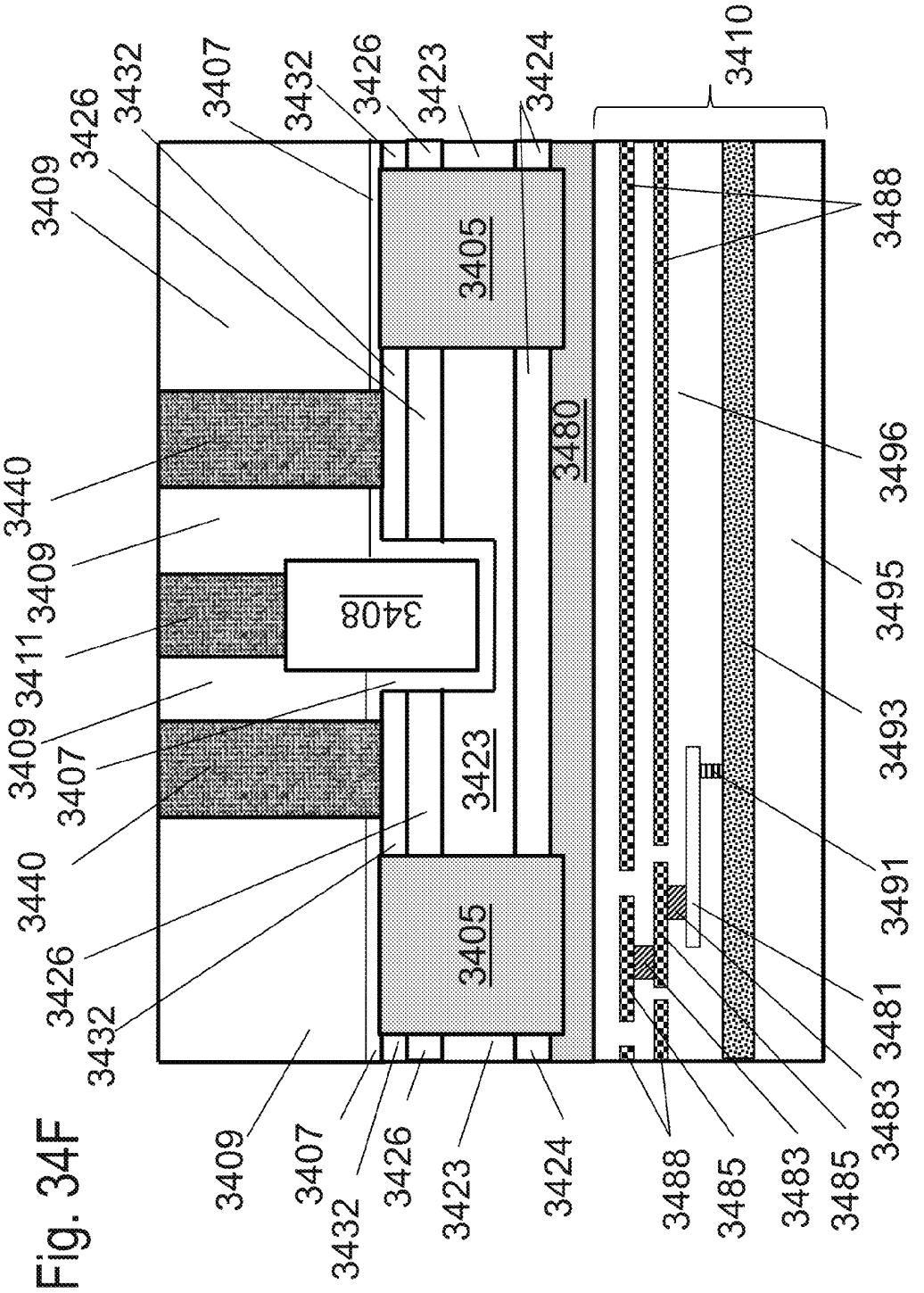
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Fig. 34F

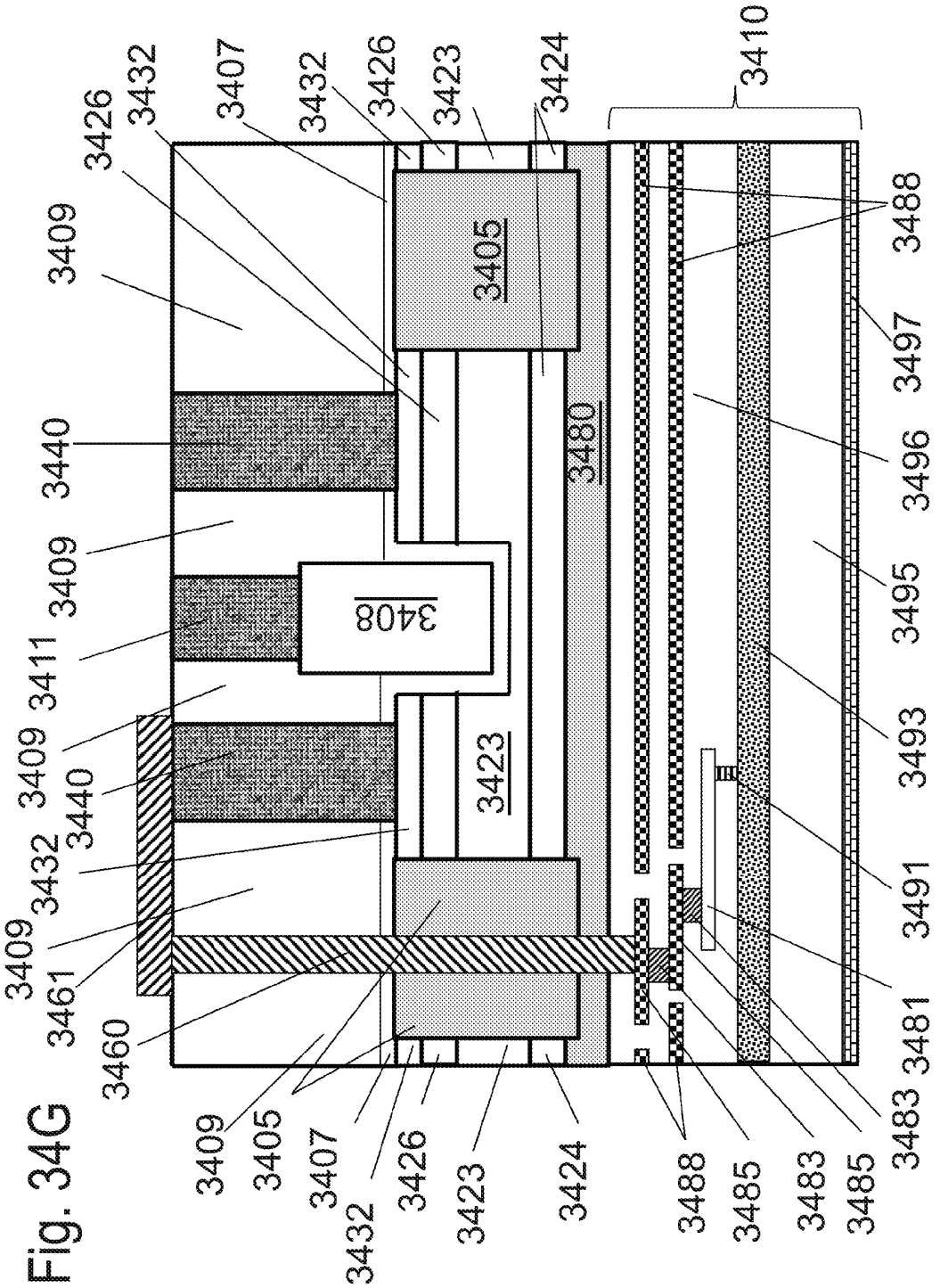
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Fig. 34G

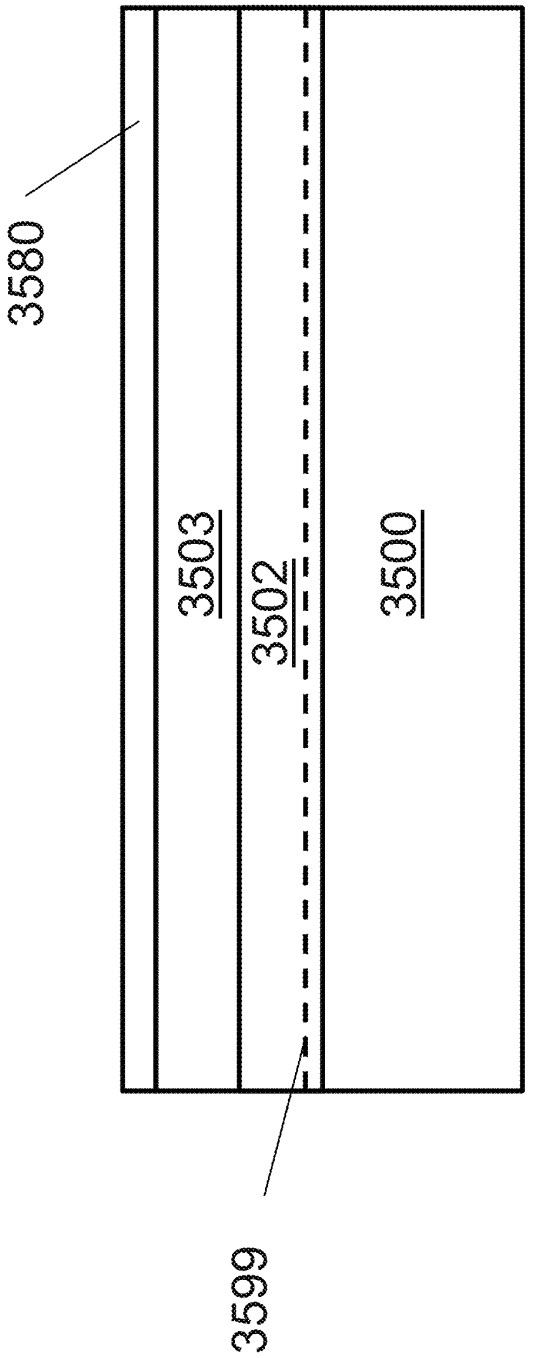


Fig. 35

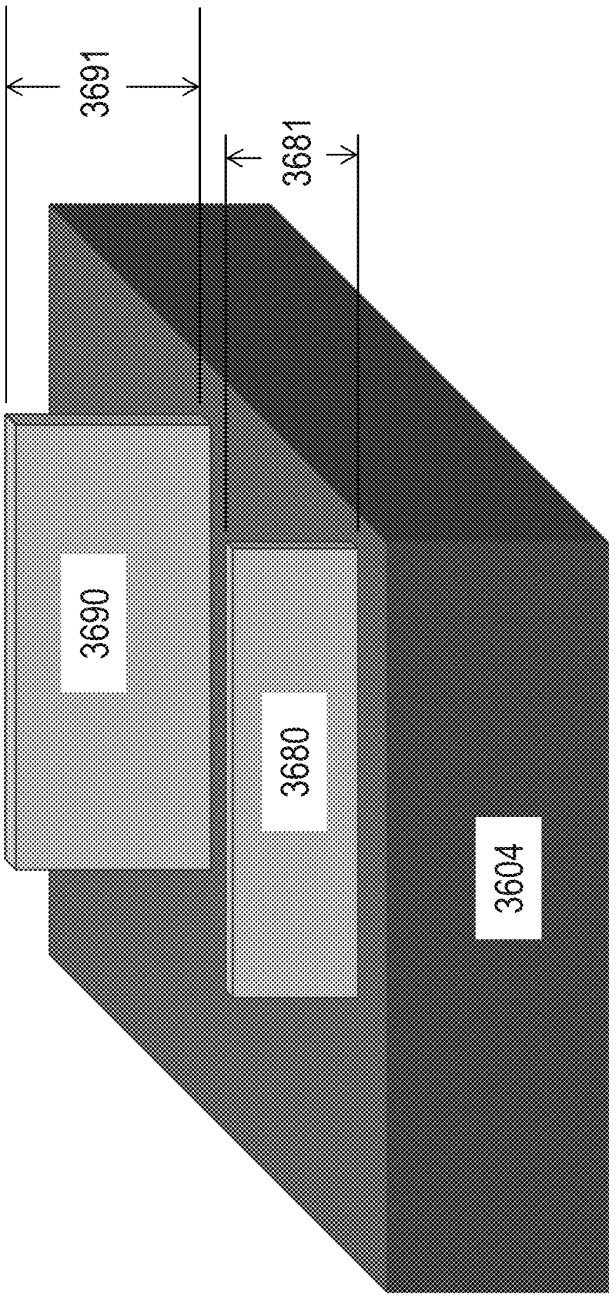
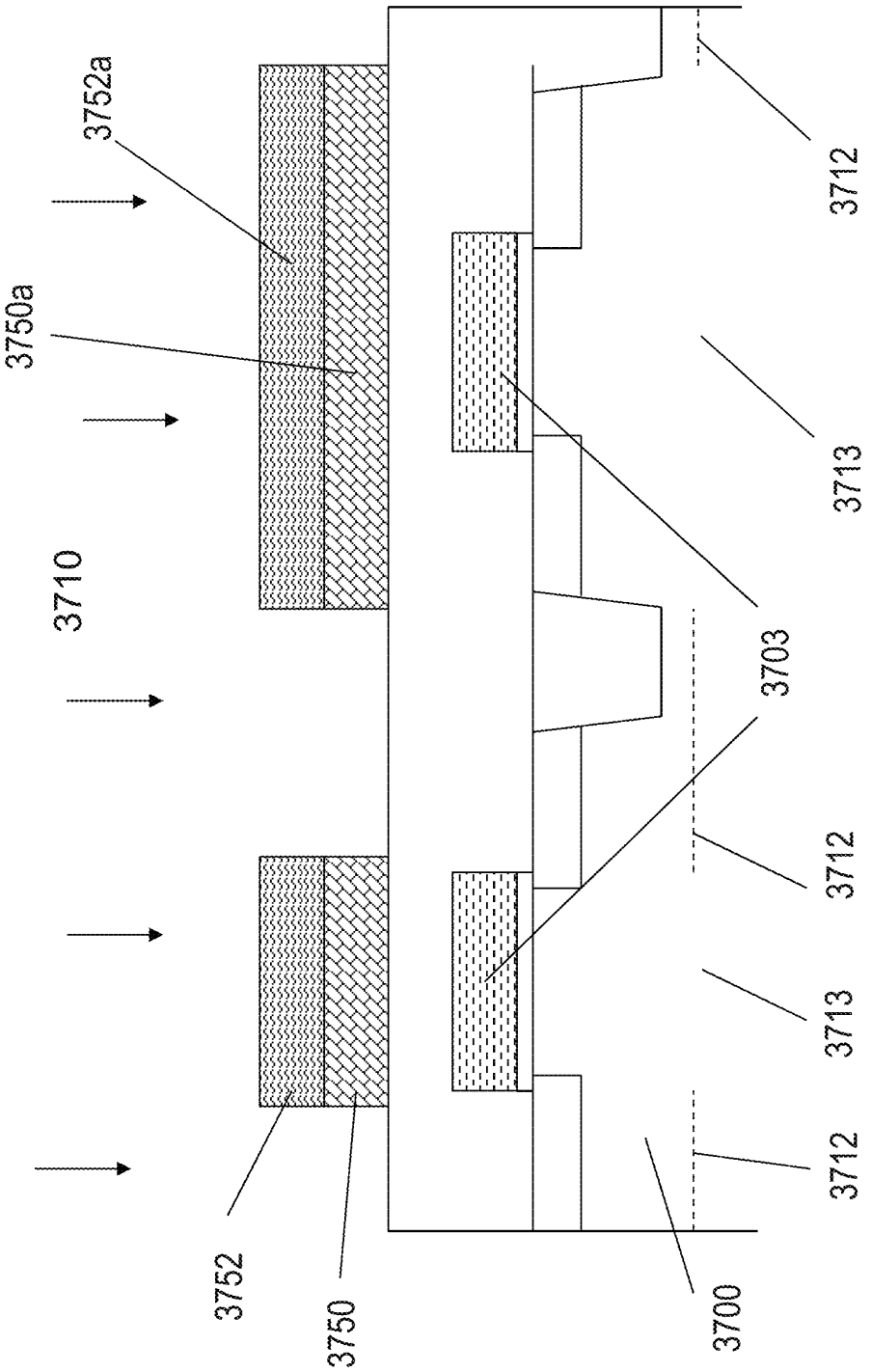


Fig. 36

Fig. 37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3700

Fig. 38A

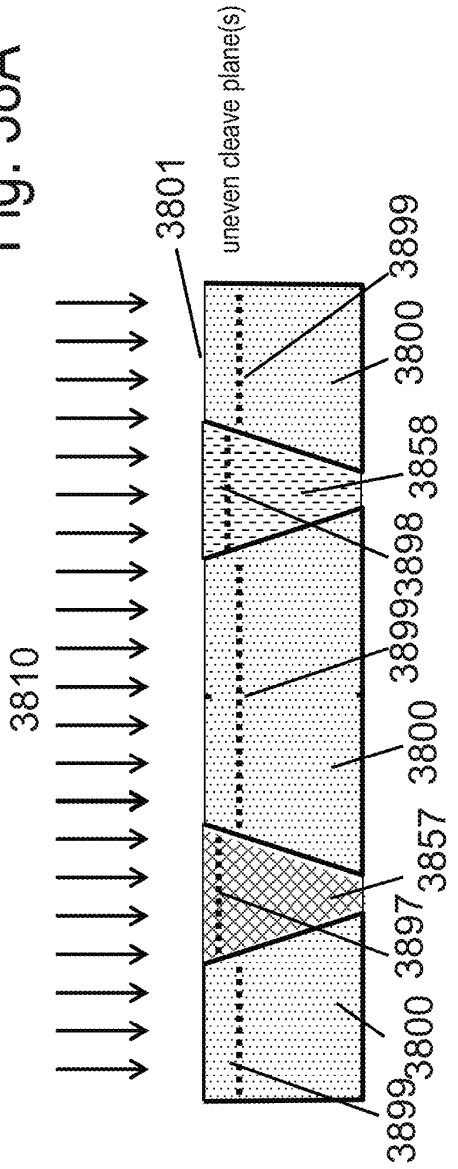
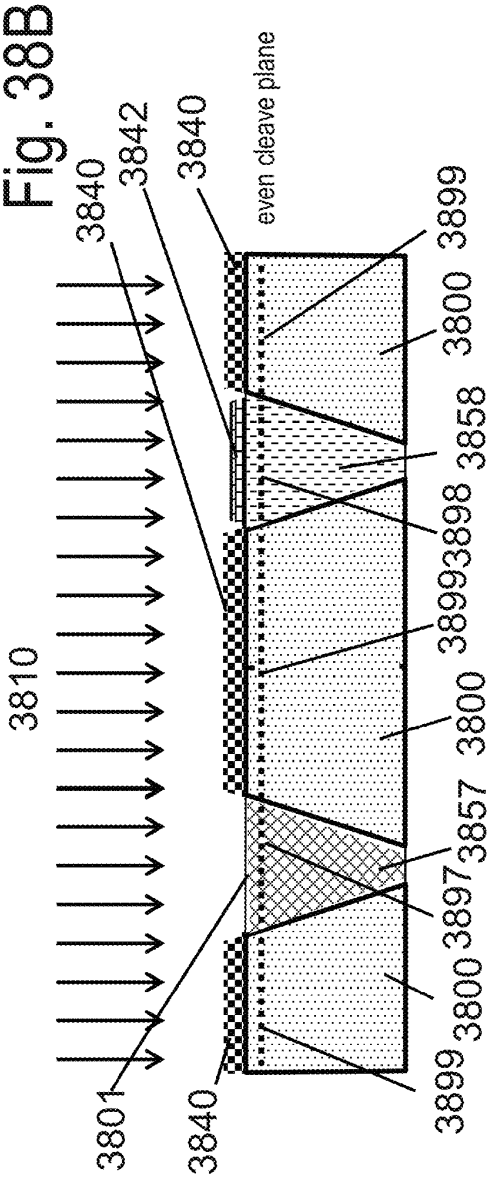


Fig. 38B



SEMICONDUCTOR SYSTEM, DEVICE AND STRUCTURE WITH HEAT REMOVAL

BACKGROUND OF THE INVENTION

1. Field of the Invention

This application relates to the general field of Integrated Circuit (IC) devices and fabrication methods, and more particularly to multilayer or Three Dimensional Integrated Circuit (3D-IC) devices and fabrication methods.

2. Discussion of Background Art

Over the past 40 years, there has been a dramatic increase in functionality and performance of Integrated Circuits (ICs). This has largely been due to the phenomenon of "scaling"; i.e., component sizes within ICs have been reduced ("scaled") with every successive generation of technology. There are two main classes of components in Complementary Metal Oxide Semiconductor (CMOS) ICs, namely transistors and wires. With "scaling", transistor performance and density typically improve and this has contributed to the previously-mentioned increases in IC performance and functionality. However, wires (interconnects) that connect together transistors degrade in performance with "scaling". The situation today is that wires dominate the performance, functionality and power consumption of ICs.

3D stacking of semiconductor devices or chips is one avenue to tackle the wire issues. By arranging transistors in 3 dimensions instead of 2 dimensions (as was the case in the 1990s), the transistors in ICs can be placed closer to each other. This reduces wire lengths and keeps wiring delay low.

There are many techniques to construct 3D stacked integrated circuits or chips including:

Through-silicon via (TSV) technology: Multiple layers of transistors (with or without wiring levels) can be constructed separately. Following this, they can be bonded to each other and connected to each other with through-silicon vias (TSVs).

Monolithic 3D technology: With this approach, multiple layers of transistors and wires can be monolithically constructed. Some monolithic 3D approaches are described in U.S. Pat. Nos. 8,273,610, 8,557,632, 8,298,875, 8,642,416, 8,378,715, 8,379,458, 8,450,804, 8,574,929, 8,581,349, 8,642,416, 8,687,399, 8,742,476, 8,674,470, 8,803,206, 8,902,663, 8,994,404, 9,021,414, 9,023,688; US patent publication 2013/0020707; and pending U.S. patent application Ser. Nos. 13/836,080, 62/077,280, 62/042,229, 13/803,437, 61/932,617, 14/607,077, 14/642,724, 62/139,636, 62/149,651, and 62/174,507. The entire contents of the foregoing patents, publications, and applications are incorporated herein by reference.

Electro-Optics: There is also work done for integrated monolithic 3D including layers of different crystals, such as U.S. Pat. No. 8,283,215, U.S. Pat. Nos. 8,163,581, 8,753,913, 8,823,122, and U.S. patent application Ser. Nos. 13/274,161 and 14/461,539. The entire contents of the foregoing patents, publications, and applications are incorporated herein by reference.

Regardless of the technique used to construct 3D stacked integrated circuits or chips, heat removal is a serious issue for this technology. For example, when a layer of circuits with power density P is stacked atop another layer with power density P, the net power density is 2P. Removing the heat produced due to this power density is a significant challenge. In addition, many heat producing regions in 3D stacked integrated circuits or chips have a high thermal resistance to the heat sink, and this makes heat removal even more difficult.

Several solutions have been proposed to tackle this issue of heat removal in 3D stacked integrated circuits and chips. These are described in the following paragraphs.

Publications have suggested passing liquid coolant through multiple device layers of a 3D-IC to remove heat. This is described in "Microchannel Cooled 3D Integrated Systems", Proc. Intl. Interconnect Technology Conference, 2008 by D. C. Sekar, et al., and "Forced Convective Interlayer Cooling in Vertically Integrated Packages," Proc. Intersoc. Conference on Thermal Management (ITHERM), 2008 by T. Brunschweiler, et al.

Thermal vias have been suggested as techniques to transfer heat from stacked device layers to the heat sink. Use of power and ground vias for thermal conduction in 3D-ICs has also been suggested. These techniques are described in "Allocating Power Ground Vias in 3D ICs for Simultaneous Power and Thermal Integrity" ACM Transactions on Design Automation of Electronic Systems (TODAES), May 2009 by Hao Yu, Joanna Ho and Lei He.

Other techniques to remove heat from 3D Integrated Circuits and Chips will be beneficial.

Additionally the 3D technology according to some embodiments of the invention may enable some very innovative IC alternatives with reduced development costs, increased yield, and other illustrative benefits.

SUMMARY

The invention may be directed to multilayer or Three Dimensional Integrated Circuit (3D IC) devices and fabrication methods.

In one aspect, a device, including: a first layer of first transistors, overlaid by at least one interconnection layer, where the interconnection layer includes copper or aluminum; a second layer including second transistors, the second layer overlaying the interconnection layer, where the second layer is less than about 0.4 micron thick; and a connection path connecting the second transistors to the interconnection layer, where the connection path includes at least one through-layer via, and the through-layer via includes material whose co-efficient of thermal expansion is within about 50 percent of the second layer coefficient of thermal expansion.

In another aspect, a device, including: a first layer of first transistors, overlaid by at least one interconnection layer, where the interconnection layer includes copper or aluminum; and a second layer including second transistors, the second layer overlaying the interconnection layer, where the second layer is less than about 0.4 micron thick, and the interconnection layer includes a power grid to provide power to at least one of the second transistors.

In another aspect, a device, including: a first layer of first transistors, overlaid by at least one interconnection layer, where the interconnection layer includes copper or aluminum; a second layer including second transistors, the second layer overlaying the interconnection layer, where the second layer is less than about 0.4 micron thick; and a thermal connection to at least one of the second transistors, where the thermal connection is electrically isolated from at least one of the second transistors, and the thermal connection provides a thermally conductive path between at least one of the second transistors and the top or bottom surface of the device.

In another aspect, a device, including: a first layer of first transistors, overlaid by at least one interconnection layer, where the interconnection layer includes copper or aluminum; a second layer including second transistors, the second layer overlaying the interconnection layer, where the second layer is less than about 0.4 micron thick; and a plurality of

thermally conducting paths from the second transistors to a heat sink, where at least one of the thermally conducting paths has a thermal conductivity of at least 100 W/m-K, and where the power delivery paths to at least one of the second transistors includes the thermally conducting paths.

In another aspect, a mobile system, comprising: a 3D device, said 3D device comprising: a first layer of first transistors, overlaid by at least one interconnection layer, wherein said interconnection layer comprises copper or aluminum; a second layer comprising second transistors, said second layer overlaying said interconnection layer, said second layer comprising: a plurality of electrical connections connecting said second transistors with said interconnection layer; and at least one thermally conductive and electrically non-conductive contact, said at least one thermally conductive and electrically non-conductive contact thermally connects said second layer to the top or bottom surface of said 3D device.

In another aspect, a system, comprising: a 3D device, said 3D device comprising: a first layer of first transistors, overlaid by at least one interconnection layer; a second layer comprising second transistors, said second layer overlaying said interconnection layer, said second layer comprising: a plurality of electrical connections connecting said second transistors with said interconnection layer; and a plurality of thermally conducting paths from said second transistors to the top or bottom surface of said 3D device.

In another aspect, a system, comprising: a 3D device, said 3D device comprising: a first layer of first transistors, overlaid by at least one interconnection layer, a second layer comprising second transistors, said second layer overlaying said interconnection layer, said second layer comprising: a plurality of electrical connections connecting said second transistors with said interconnection layer; said plurality of electrical connections comprising: a power distribution grid providing power to said second transistors, and a plurality of thermally conducting paths from said power distribution grid to the top or bottom surface of said 3D device.

In another aspect, a 3D device comprising: a first layer comprising first transistors, said first layer overlaid by at least one interconnection layer; a second layer comprising second transistors, said second layer overlaying said interconnection layer; a plurality of electrical connections connecting said second transistors with said interconnection layer; and at least one thermally conductive and electrically non-conductive contact, wherein said at least one thermally conductive and electrically non-conductive contact thermally connects said second layer to a top or bottom surface of said 3D device.

In another aspect, a system, comprising: a 3D device, said 3D device comprising: a first layer comprising first transistors, said first layer overlaid by a first interconnection layer; a second layer comprising second transistors, said second layer overlaying said first interconnection layer; a plurality of second interconnection layers overlaying said second layer; a plurality of electrical connections connecting at least one of said second interconnection layers with said first interconnection layer; and a plurality of thermally conducting paths from said second transistors to a top or bottom surface of said 3D device.

In another aspect, a system, comprising: a 3D device, said 3D device comprising: a first layer comprising first transistors, said first layer overlaid by at least one interconnection layer, a second layer comprising second transistors, said second layer overlaying said interconnection layer; a plurality of electrical connections connecting said second transistors with said interconnection layer; said plurality of electrical connections further comprising: a power distribution grid providing power to said second transistors, and a plurality of thermally conducting paths from said power distribution grid to a top or bottom surface of said 3D device, wherein said second layer has a thickness less than 2 microns

BRIEF DESCRIPTION OF THE DRAWINGS

Various embodiments of the invention will be understood and appreciated more fully from the following detailed description, taken in conjunction with the drawings in which:

FIG. **1** is an exemplary drawing illustration of a 3D integrated circuit;

FIG. **2** is an exemplary drawing illustration of another 3D integrated circuit;

FIG. **3** is an exemplary drawing illustration of the power distribution network of a 3D integrated circuit;

FIG. **4** is an exemplary drawing illustration of a NAND gate;

FIG. **5** is an exemplary drawing illustration of a thermal contact concept;

FIG. **6** is an exemplary drawing illustration of various types of thermal contacts;

FIG. **7** is an exemplary drawing illustration of another type of thermal contact;

FIG. **8** is an exemplary drawing illustration of the use of heat spreaders in 3D stacked device layers;

FIG. **9** is an exemplary drawing illustration of the use of thermally conductive shallow trench isolation (STI) in 3D stacked device layers;

FIG. **10** is an exemplary drawing illustration of the use of thermally conductive pre-metal dielectric regions in 3D stacked device layers;

FIG. **11** is an exemplary drawing illustration of the use of thermally conductive etch stop layers for the first metal layer of 3D stacked device layers;

FIG. **12**A-**12**B are exemplary drawing illustrations of the use and retention of thermally conductive hard mask layers for patterning contact layers of 3D stacked device layers;

FIG. **13** is an exemplary drawing illustration of a 4 input NAND gate;

FIG. **14** is an exemplary drawing illustration of a 4 input NAND gate where substantially all parts of the logic cell can be within desirable temperature limits;

FIG. **15** is an exemplary drawing illustration of a transmission gate;

FIG. **16** is an exemplary drawing illustration of a transmission gate where substantially all parts of the logic cell can be within desirable temperature limits;

FIG. **17**A-**17**D is an exemplary process flow for constructing recessed channel transistors with thermal contacts;

FIG. **18** is an exemplary drawing illustration of a pMOS recessed channel transistor with thermal contacts;

FIG. **19** is an exemplary drawing illustration of a CMOS circuit with recessed channel transistors and thermal contacts;

FIG. **20** is an exemplary drawing illustration of a technique to remove heat more effectively from silicon-on-insulator (SOI) circuits;

FIG. **21** is an exemplary drawing illustration of an alternative technique to remove heat more effectively from silicon-on-insulator (SOI) circuits;

FIG. **22** is an exemplary drawing illustration of a recessed channel transistor (RCAT);

FIG. **23** is an exemplary drawing illustration of a 3D-IC with thermally conductive material on the sides;

FIG. **24** is an exemplary procedure for a chip designer to ensure a good thermal profile for a design;

FIG. **25** is an exemplary drawing illustration of a monolithic 3D-IC structure with CTE adjusted through layer connections;

FIG. **26**A-**26**F are exemplary drawing illustrations of a process flow for manufacturing junction-less recessed channel array transistors;

FIG. **27**A-**27**C are exemplary drawing illustrations of Silicon or Oxide-Compound Semiconductor hetero donor or acceptor substrates which may be formed by utilizing an engineered substrate;

FIG. **28**A-**28**B are exemplary drawing illustrations of Silicon or Oxide-Compound Semiconductor hetero donor or acceptor substrates which may be formed by epitaxial growth directly on a silicon or SOI substrate;

FIGS. **29**A-**29**H are exemplary drawing illustrations of a process flow to form a closely coupled but independently optimized silicon and compound semiconductor device stack;

FIG. **30** is an exemplary drawing illustration of a partitioning of a circuit design into three layers of a 3D-IC;

FIG. **31** is an exemplary drawing illustration of a carrier substrate with an integrated heat sink/spreader and/or optically reflective layer;

FIGS. **32**A-**32**F are exemplary drawing illustrations of a process flow for manufacturing fully depleted Recessed Channel Array Transistors (FD-RCAT);

FIGS. **33**A-**33**F are exemplary drawing illustrations of the integration of a shield/heat sink layer in a 3D-IC;

FIGS. **34**A-**34**G are exemplary drawing illustrations of a process flow for manufacturing fully depleted Recessed Channel Array Transistors (FD-RCAT) with an integrated shield/heat sink layer;

FIG. **35** is an exemplary drawing illustration of the co-implantation ion-cut utilized in forming a 3D-IC;

FIG. **36** is an exemplary drawing illustration of forming multiple Vt finfet transistors on the same circuit, device, die or substrate;

FIG. **37** is an exemplary drawing illustration of an ion implant screen to protect transistor structures such as gate stacks and junctions;

FIGS. **38**A-**38**B are exemplary drawing illustrations of techniques to successfully ion-cut a silicon/compound-semiconductor hybrid substrate.

DETAILED DESCRIPTION

An embodiment of the invention is now described with reference to the drawing figures. Persons of ordinary skill in the art will appreciate that the description and figures illustrate rather than limit the invention and that in general the figures are not drawn to scale for clarity of presentation. Such skilled persons will also realize that many more embodiments are possible by applying the inventive principles contained herein and that such embodiments fall within the scope of the invention which is not to be limited except by the appended claims.

Some drawing figures may describe process flows for building devices. These process flows, which may be a sequence of steps for building a device, may have many structures, numerals and labels that may be common between two or more adjacent steps. In such cases, some labels, numerals and structures used for a certain step's figure may have been described in the previous steps' figures.

FIG. **1** illustrates a 3D integrated circuit. Two crystalline layers, **0104** and **0116**, which may include semiconductor materials such as, for example, mono-crystalline silicon, germanium, GaAs, InP, and graphene, are shown. For this illustration, mono-crystalline (single crystal) silicon may be used. Silicon layer **0116** could be thinned down from its original thickness, and its final thickness could be in the range of about 0.01 um to about 50 um, for example, 10 nm, 100 nm, 200 nm, 0.4 um, 1 um, 2 um or 5 um. Silicon layer **0104** could be thinned down from its original thickness, and its final thickness could be in the range of about 0.01 um to about 50 um, for example, 10 nm, 100 nm, 200 nm, 0.4 um, 1 um, 2 um or 5 um; however, due to strength considerations, silicon layer **0104** may also be of thicknesses greater than 100 um, depending on, for example, the strength of bonding to heat removal apparatus **0102**. Silicon layer **0104** may include transistors such as, for example, MOSFETS, FinFets, BJTs, HEMTs, HBTs, which may include gate electrode region **0114**, gate dielectric region **0112**, source and drain junction regions (not shown), and shallow trench isolation (STI) regions **0110**. Silicon layer **0116** may include transistors such as, for example, MOSFETS, FinFets, BJTs, HEMTs, HBTs, which may include gate electrode region **0134**, gate dielectric region **0132**, source and drain junction regions (not shown), and shallow trench isolation (STI) regions **0130**. A through-silicon via (TSV) **0118** could be present and may have an associated surrounding dielectric region **0120**. Wiring layers **0108** for silicon layer **0104** and wiring dielectric regions **0106** may be present and may form an associated interconnect layer or layers. Wiring layers **0138** for silicon layer **0116** and wiring dielectric **0136** may be present and may form an associated interconnect layer or layers. Through-silicon via (TSV) **0118** may connect to wiring layers **0108** and wiring layers **0138** (not shown). The heat removal apparatus **0102** may include a heat spreader and/or a heat sink. The heat removal problem for the 3D integrated circuit shown in FIG. **1** is immediately apparent. The silicon layer **0116** is far away from the heat removal apparatus **0102**, and it may be difficult to transfer heat among silicon layer **0116** and heat removal apparatus **0102**. Furthermore, wiring dielectric regions **0106** may not conduct heat well, and this increases the thermal resistance among silicon layer **0116** and heat removal apparatus **0102**. Silicon layer **0104** and silicon layer **0116** may be may be substantially absent of semiconductor dopants to form an undoped silicon region or layer, or doped, such as, for example, with elemental or compound species that form a p+, or p, or p−, or n+, or n, or n− silicon layer or region.

FIG. **2** illustrates an exemplary 3D integrated circuit that could be constructed, for example, using techniques described in U.S. Patent Application Publication 2012/0129301 (allowed U.S. patent application Ser. No. 13/273,712) and pending U.S. patent application Ser. Nos. 13/441,923 and 13/099,010. The contents of the foregoing applications are incorporated herein by reference. Two crystalline layers, **0204** and **0216**, which may include semiconductor materials such as, for example, mono-crystalline silicon, germanium, GaAs, InP, and graphene, are shown. For this illustration, mono-crystalline (single crystal) silicon may be used. Silicon layer **0216** could be thinned down from its original thickness, and its final thickness could be in the range of about 0.01 um to about 50 um, for example, 10 nm, 100 nm, 200 nm, 0.4 um, 1 um, 2 um or 5 um. Silicon layer **0204** could be thinned down from its original thickness, and its final thickness could be in the range of about 0.01 um to about 50 um, for example, 10 nm, 100 nm, 200 nm, 0.4 um, 1 um, 2 um or 5 um; however, due to strength considerations, silicon layer **0204** may also be of thicknesses greater than 100 um, depending on, for example, the strength of bonding to heat removal apparatus **0202**. Silicon layer **0204** may include transistors such as, for example, MOSFETS, FinFets, BJTs, HEMTs, HBTs, which may include gate electrode region **0214**, gate

dielectric region **0212**, source and drain junction regions (not shown for clarity) and shallow trench isolation (STI) regions **0210**. Silicon layer **0216** may include transistors such as, for example, MOSFETS, FinFets, BJTs, HEMTs, HBTs, which may include gate electrode region **0234**, gate dielectric region **0232**, source and drain junction regions (not shown for clarity), and shallow trench isolation (STI) regions **0222**. It can be observed that the STI regions **0222** can go right through to the bottom of silicon layer **0216** and provide good electrical isolation. This, however, may cause challenges for heat removal from the STI surrounded transistors since STI regions **0222** are typically composed of insulators that do not conduct heat well. Therefore, the heat spreading capabilities of silicon layer **0216** with STI regions **0222** are low. A through-layer via (TLV) **0218** may be present and may include an associated surrounding dielectric region **0220**. Wiring layers **0208** for silicon layer **0204** and wiring dielectric regions **0206** may be present and may form an associated interconnect layer or layers. Wiring layers **0238** for silicon layer **0216** and wiring dielectric **0236** may be present and may form an associated interconnect layer or layers. Through-layer via (TLV) **0218** may connect to wiring layers **0208** and wiring layers **0238** (not shown). The heat removal apparatus **0202** may include a heat spreader and/or a heat sink. The heat removal problem for the 3D integrated circuit shown in FIG. **2** is immediately apparent. The silicon layer **0216** may be far away from the heat removal apparatus **0202**, and it may be difficult to transfer heat among silicon layer **0216** and heat removal apparatus **0202**. Furthermore, wiring dielectric regions **0206** may not conduct heat well, and this increases the thermal resistance among silicon layer **0216** and heat removal apparatus **0202**. The heat removal challenge is further exacerbated by the poor heat spreading properties of silicon layer **0216** with STI regions **0222**. Silicon layer **0204** and silicon layer **0216** may be may be substantially absent of semiconductor dopants to form an undoped silicon region or layer, or doped, such as, for example, with elemental or compound species that form a p+, or p, or p−, or n+, or n, or n− silicon layer or region.

FIG. **3** and FIG. **4** illustrate how the power or ground distribution network of a 3D integrated circuit could assist heat removal. FIG. **3** illustrates an exemplary power distribution network or structure of the 3D integrated circuit. As shown in FIGS. **1** and **2**, a 3D integrated circuit, could, for example, be constructed with two silicon layers, first silicon layer **0304** and second silicon layer **0316**. The heat removal apparatus **0302** could include, for example, a heat spreader and/or a heat sink. The power distribution network or structure could consist of a global power grid **0310** that takes the supply voltage (denoted as V_{DD}) from the chip/circuit power pads and transfers V_{DD} to second local power grid **0308** and first local power grid **0306**, which transfers the supply voltage to logic/memory cells, transistors, and/or gates such as second transistor **0314** and first transistor **0315**. Second layer vias **0318** and first layer vias **0312**, such as the previously described TSV or TLV, could be used to transfer the supply voltage from the global power grid **0310** to second local power grid **0308** and first local power grid **0306**. The global power grid **0310** may also be present among first silicon layer **0304** and second silicon layer **0316**. The 3D integrated circuit could have a similarly designed and laid-out distribution networks, such as for ground and other supply voltages, as well. Typically, many contacts may be made among the supply and ground distribution networks and first silicon layer **0304**. Due to this, there could exist a low thermal resistance among the power/ground distribution network and the heat removal apparatus **0302**. Since power/ground distribution networks may be typically constructed of conductive metals and could have low effective electrical resistance, the power/ground distribution networks could have a low thermal resistance as well. Each logic/memory cell or gate on the 3D integrated circuit (such as, for example, second transistor **0314**) is typically connected to V_{DD} and ground, and therefore could have contacts to the power and ground distribution network. The contacts could help transfer heat efficiently (for example, with low thermal resistance) from each logic/memory cell or gate on the 3D integrated circuit (such as, for example, second transistor **0314**) to the heat removal apparatus **0302** through the power/ground distribution network and the silicon layer **0304**. Silicon layer **0304** and silicon layer **0316** may be may be substantially absent of semiconductor dopants to form an undoped silicon region or layer, or doped, such as, for example, with elemental or compound species that form a p+, or p, or p−, or n+, or n, or n− silicon layer or region.

FIG. **4** illustrates an exemplary NAND logic cell or NAND gate **0420** and how substantially all portions of this logic cell or gate could be designed and laid-out with low thermal resistance to the V_{DD} or ground (GND) contacts. The NAND gate **0420** could include two pMOS transistors **0402** and two nMOS transistors **0404**. The layout of the NAND gate **0420** is indicated in exemplary layout **0422**. Various regions of the layout may include metal regions **0406**, poly regions **0408**, n type silicon regions **0410**, p type silicon regions **0412**, contact regions **0414**, and oxide regions **0424**. pMOS transistors **0416** and nMOS transistors **0418** may be present in the layout. It can be observed that substantially all parts of the exemplary NAND gate **0420** could have low thermal resistance to V_{DD} or GND contacts since they may be physically very close to them, within a few design rule lambdas, wherein lambda is the basic minimum layout rule distance for a given set of circuit layout design rules. Thus, substantially all transistors in the NAND gate **0420** can be maintained at desirable temperatures, such as, for example, less than 25 or 50 or 70 degrees Centigrade, if the V_{DD} or ground contacts are maintained at desirable temperatures.

While the previous paragraph described how an existing power distribution network or structure can transfer heat efficiently from logic/memory cells or gates in 3D-ICs to their heat sink, many techniques to enhance this heat transfer capability will be described herein. Many embodiments of the invention can provide several benefits, including lower thermal resistance and the ability to cool higher power 3D-ICs. As well, thermal contacts may provide mechanical stability and structural strength to low-k Back End Of Line (BEOL) structures, which may need to accommodate shear forces, such as from CMP and/or cleaving processes. The heat transfer capability enhancement techniques may be useful and applied to different methodologies and implementations of 3D-ICs, including monolithic 3D-ICs and TSV-based 3D-ICs.

FIG. **5** illustrates an embodiment of the invention, wherein thermal contacts in a 3D-IC is described. The 3D-IC and associated power and ground distribution network may be formed as described in FIGS. **1**, **2**, **3**, and **4** herein. For example, two crystalline layers, **0504** and **0516**, which may include semiconductor materials such as, for example, mono-crystalline silicon, germanium, GaAs, InP, and graphene, may have transistors. For this illustration, mono-crystalline (single crystal) silicon may be used. Silicon layer **0516** could be thinned down from its original thickness, and its final thickness could be in the range of about 0.01 um to about 50 um, for example, 10 nm, 100 nm, 200 nm, 0.4 um, 1 um, 2 um or Sum. Silicon layer **0504** could be thinned down from its original thickness, and its final thickness could be in the range of about 0.01 um to about 50 um, for example, 10 nm, 100 nm,

200 nm, 0.4 um, 1 um, 2 um or Sum; however, due to strength considerations, silicon layer **0504** may also be of thicknesses greater than 100 um, depending on, for example, the strength of bonding to heat removal apparatus **0202**. Silicon layer **0504** may include transistors such as, for example, MOSFETS, FinFets, BJTs, HEMTs, HBTs, which may include STI regions **0510**, gate dielectric regions **0512**, gate electrode regions **0514** and several other regions that may be necessary for transistors such as source and drain junction regions (not shown for clarity). Silicon layer **0516** may include transistors such as, for example, MOSFETS, FinFets, BJTs, HEMTs, HBTs, which may include STI regions **0530**, gate dielectric regions **0532**, gate electrode regions **0534** and several other regions that may be necessary for transistors such as source and drain junction regions (not shown for clarity). Heat removal apparatus **0502** may include, for example, heat spreaders and/or heat sinks. In the example shown in FIG. **5**, silicon layer **0504** is closer to the heat removal apparatus **0502** than other silicon layers such as silicon layer **0516**. Wiring layers **0542** for silicon layer **0504** and wiring dielectric **0546** may be present and may form an associated interconnect layer or layers. Wiring layers **0522** for silicon layer **0516** and wiring dielectric **0506** may be present and may form an associated interconnect layer or layers. Through-layer vias (TLVs) **0518** for power delivery and interconnect and their associated dielectric regions **0520** are shown. Dielectric regions **0520** may include STI regions, such as STI regions **0530**. A thermal contact **0524** may connect the local power distribution network or structure to the silicon layer **0504**. The local power distribution network or structure may include wiring layers **0542** used for transistors in the silicon layer **0504**. Thermal junction region **0526** can be, for example, a doped or undoped region of silicon, and further details of thermal junction region **0526** will be given in FIG. **6**. The thermal contact **0524** can be suitably placed close to the corresponding through-layer via **0518**; this helps transfer heat efficiently as a thermal conduction path from the through-layer via **0518** to thermal junction region **0526** and silicon layer **0504** and ultimately to the heat removal apparatus **0502**. For example, the thermal contact **0524** could be located within approximately 2 um distance of the through-layer via **0518** in the X-Y plane (the through-layer via **0518** vertical length direction is considered the Z plane in FIG. **5**). While the thermal contact **0524** is described above as being between the power distribution network or structure and the silicon layer closest to the heat removal apparatus, it could also be between the ground distribution network and the silicon layer closest to the heat sink. Furthermore, more than one thermal contact **0524** can be placed close to the through-layer via **0518**. The thermal contacts can improve heat transfer from transistors located in higher layers of silicon such as silicon layer **0516** to the heat removal apparatus **0502**. While monocrystalline silicon has been mentioned as the transistor material in this document, other options are possible including, for example, poly-crystalline silicon, mono-crystalline germanium, mono-crystalline III-V semiconductors, graphene, and various other semiconductor materials with which devices, such as transistors, may be constructed within. Moreover, thermal contacts and vias may not be stacked in a vertical line through multiple stacks, layers, strata of circuits. Thermal contacts and vias may include materials such as sp2 carbon as conducting and sp3 carbon as non-conducting of electrical current. Thermal contacts and vias may include materials such as carbon nano-tubes. Thermal contacts and vias may include materials such as, for example, copper, aluminum, tungsten, titanium, tantalum, cobalt metals and/or silicides of the metals. Silicon layer **0504** and silicon layer **0516** may be may be substantially absent of semiconductor dopants to form an undoped silicon region or layer, or doped, such as, for example, with elemental or compound species that form a p+, or p, or p−, or n+, or n, or n− silicon layer or region.

FIG. **6** describes an embodiment of the invention, wherein various implementations of thermal junctions and associated thermal contacts are illustrated. P-wells in CMOS integrated circuits may be typically biased to ground and N-wells may be typically biased to the supply voltage V_{DD}. A thermal contact **0604** between the power (V_{DD}) distribution network and a P-well **0602** can be implemented as shown in N+ in P-well thermal junction and contact example **0608**, where an n+ doped region thermal junction **0606** may be formed in the P-well region at the base of the thermal contact **0604**. The n+ doped region thermal junction **0606** ensures a reverse biased p-n junction can be formed in N+ in P-well thermal junction and contact example **0608** and makes the thermal contact viable (for example, not highly conductive) from an electrical perspective. The thermal contact **0604** could be formed of a conductive material such as copper, aluminum or some other material with a thermal conductivity of at least 100 W/m-K. A thermal contact **0614** between the ground (GND) distribution network and a P-well **0612** can be implemented as shown in P+ in P-well thermal junction and contact example **0618**, where a p+ doped region thermal junction **0616** may be formed in the P-well region at the base of the thermal contact **0614**. The p+ doped region thermal junction **0616** makes the thermal contact viable (for example, not highly conductive) from an electrical perspective. The p+ doped region thermal junction **0616** and the P-well **0612** may typically be biased at ground potential. The thermal contact **0614** could be formed of a conductive material such as copper, aluminum or some other material with a thermal conductivity of at least 100 W/m-K. A thermal contact **0624** between the power (V_{DD}) distribution network and an N-well **0622** can be implemented as shown in N+ in N-well thermal junction and contact example **0628**, wherein an n+ doped region thermal junction **0626** may be formed in the N-well region at the base of the thermal contact **0624**. The n+ doped region thermal junction **0626** makes the thermal contact viable (for example, not highly conductive) from an electrical perspective. The n+ doped region thermal junction **0626** and the N-well **0622** may typically be biased at V_{DD} potential. The thermal contact **0624** could be formed of a conductive material such as copper, aluminum or some other material with a thermal conductivity of at least 100 W/m-K. A thermal contact **0634** between the ground (GND) distribution network and an N-well **0632** can be implemented as shown in P+ in N-well thermal junction and contact example **0638**, where a p+ doped region thermal junction **0636** may be formed in the N-well region at the base of the thermal contact **0634**. The p+ doped region thermal junction **0636** makes the thermal contact viable (for example, not highly conductive) from an electrical perspective due to the reverse biased p-n junction formed in P+ in N-well thermal junction and contact example **0638**. The thermal contact **0634** could be formed of a conductive material such as copper, aluminum or some other material with a thermal conductivity of at least 100 W/m-K. Note that the thermal contacts are designed to conduct negligible electricity, and the current flowing through them is several orders of magnitude lower than the current flowing through a transistor when it is switching. Therefore, the thermal contacts can be considered to be designed to conduct heat and conduct negligible (or no) electricity.

FIG. **7** describes an embodiment of the invention, wherein an additional type of thermal contact structure is illustrated. The embodiment shown in FIG. **7** could also function as a

decoupling capacitor to mitigate power supply noise. It could consist of a thermal contact **0704**, an electrode **0710**, a dielectric **0706** and P-well **0702**. The dielectric **0706** may be electrically insulating, and could be optimized to have high thermal conductivity. Dielectric **0706** could be formed of materials, such as, for example, hafnium oxide, silicon dioxide, other high k dielectrics, carbon, carbon based material, or various other dielectric materials with electrical conductivity below 1 nano-amp per square micron.

A thermal connection may be defined as the combination of a thermal contact and a thermal junction. The thermal connections illustrated in FIG. **6**, FIG. **7** and other figures in this document are designed into a chip to remove heat, and are designed to not conduct electricity. Essentially, a semiconductor device comprising power distribution wires is described wherein some of said wires have a thermal connection designed to conduct heat to the semiconductor layer and the wires do not substantially conduct electricity through the thermal connection to the semiconductor layer.

Thermal contacts similar to those illustrated in FIG. **6** and FIG. **7** can be used in the white spaces of a design, for example, locations of a design where logic gates or other useful functionality may not be present. The thermal contacts may connect white-space silicon regions to power and/or ground distribution networks. Thermal resistance to the heat removal apparatus can be reduced with this approach. Connections among silicon regions and power/ground distribution networks can be used for various device layers in the 3D stack, and may not be restricted to the device layer closest to the heat removal apparatus. A Schottky contact or diode may also be utilized for a thermal contact and thermal junction. Moreover, thermal contacts and vias may not have to be stacked in a vertical line through multiple stacks, layers, strata of circuits.

FIG. **8** illustrates an embodiment of the invention, which can provide enhanced heat removal from 3D-ICs by integrating heat spreader regions in stacked device layers. The 3D-IC and associated power and ground distribution network may be formed as described in FIGS. **1**, **2**, **3**, **4**, and **5** herein. For example, two crystalline layers, **0804** and **0816**, which may include semiconductor materials such as, for example, mono-crystalline silicon, germanium, GaAs, InP, and graphene, are shown. For this illustration, mono-crystalline (single crystal) silicon may be used. Silicon layer **0816** could be thinned from its original thickness, and its final thickness could be in the range of about 0.01 um to about 50 um, for example, 10 nm, 100 nm, 200 nm, 0.4 um, 1 um, 2 um or 5 um. Silicon layer **0804** could be thinned down from its original thickness, and its final thickness could be in the range of about 0.01 um to about 50 um, for example, 10 nm, 100 nm, 200 nm, 0.4 um, 1 um, 2 um or 5 um; however, due to strength considerations, silicon layer **0804** may also be of thicknesses greater than 100 um, depending on, for example, the strength of bonding to heat removal apparatus **0802**. Silicon layer **0804** may include transistors such as, for example, MOSFETS, FinFets, BJTs, HEMTs, HBTs, which may include gate electrode region **0814**, gate dielectric region **0812**, shallow trench isolation (STI) regions **0810** and several other regions that may be necessary for transistors such as source and drain junction regions (not shown for clarity). Silicon layer **0816** may include transistors such as, for example, MOSFETS, FinFets, BJTs, HEMTs, HBTs, which may include gate electrode region **0834**, gate dielectric region **0832**, shallow trench isolation (STI) regions **0822** and several other regions that may be necessary for transistors such as source and drain junction regions (not shown for clarity). A through-layer via (TLV) **0818** may be present and may include an associated surrounding dielectric region **0820**. Wiring layers **0808** for silicon layer **0804** and wiring dielectric **0806** may be present and may form an associated interconnect layer or layers. Wiring layers **0838** for silicon layer **0816** and wiring dielectric **0836** may be present and may form an associated interconnect layer or layers. Through-layer via (TLV) **0818** may connect to wiring layers **0808** and wiring layers **0838** (not shown). The heat removal apparatus **0802** may include, for example, a heat spreader and/or a heat sink. It can be observed that the STI regions **0822** can go right through to the bottom of silicon layer **0816** and provide good electrical isolation. This, however, may cause challenges for heat removal from the STI surrounded transistors since STI regions **0822** are typically composed of insulators that do not conduct heat well. The buried oxide layer **0824** typically does not conduct heat well. To tackle heat removal issues with the structure shown in FIG. **8**, a heat spreader **0826** may be integrated into the 3D stack. The heat spreader **0826** material may include, for example, copper, aluminum, graphene, diamond, carbon or any other material with a high thermal conductivity (defined as greater than 100 W/m-K). While the heat spreader concept for 3D-ICs is described with an architecture similar to FIG. **2**, similar heat spreader concepts could be used for architectures similar to FIG. **1**, and also for other 3D IC architectures. Silicon layer **0804** and silicon layer **0816** may be may be substantially absent of semiconductor dopants to form an undoped silicon region or layer, or doped, such as, for example, with elemental or compound species that form a p+, or p, or p−, or n+, or n, or n− silicon layer or region.

FIG. **9** illustrates an embodiment of the invention, which can provide enhanced heat removal from 3D-ICs by using thermally conductive shallow trench isolation (STI) regions in stacked device layers. The 3D-IC and associated power and ground distribution network may be formed as described in FIGS. **1**, **2**, **3**, **4**, **5** and **8** herein. For example, two crystalline layers, **0904** and **0916**, which may include semiconductor materials such as, for example, mono-crystalline silicon, germanium, GaAs, InP, and graphene, are shown. For this illustration, mono-crystalline (single crystal) silicon may be used. Silicon layer **0916** could be thinned from its original thickness, and its final thickness could be in the range of about 0.01 um to about 50 um, for example, 10 nm, 100 nm, 200 nm, 0.4 um, 1 um, 2 um or 5 um. Silicon layer **0904** could be thinned down from its original thickness, and its final thickness could be in the range of about 0.01 um to about 50 um, for example, 10 nm, 100 nm, 200 nm, 0.4 um, 1 um, 2 um or Sum; however, due to strength considerations, silicon layer **0904** may also be of thicknesses greater than 100 um, depending on, for example, the strength of bonding to heat removal apparatus **0802**. Silicon layer **0904** may include transistors such as, for example, MOSFETS, FinFets, BJTs, HEMTs, HBTs, which may include gate electrode region **0914**, gate dielectric region **0912**, shallow trench isolation (STI) regions **0910** and several other regions that may be necessary for transistors such as source and drain junction regions (not shown for clarity). Silicon layer **0916** may include transistors such as, for example, MOSFETS, FinFets, BJTs, HEMTs, HBTs, which may include gate electrode region **0934**, gate dielectric region **0932**, shallow trench isolation (STI) regions **0922** and several other regions that may be necessary for transistors such as source and drain junction regions (not shown for clarity). A through-layer via (TLV) **0918** may be present and may include an associated surrounding dielectric region **0920**. Dielectric region **0920** may include a shallow trench isolation region. Wiring layers **0908** for silicon layer **0904** and wiring dielectric **0906** may be present and may form an associated interconnect layer or layers. Wiring layers **0938** for silicon

layer **0916** and wiring dielectric **0936** may be present and may form an associated interconnect layer or layers. Through-layer via (TLV) **0918** may connect to wiring layers **0908** and wiring layers **0938** (not shown). The heat removal apparatus **0902** may include a heat spreader and/or a heat sink. It can be observed that the STI regions **0922** can go right through to the bottom of silicon layer **0916** and provide good electrical isolation. This, however, may cause challenges for heat removal from the STI surrounded transistors since STI regions **0922** are typically composed of insulators such as silicon dioxide that do not conduct heat well. To tackle possible heat removal issues with the structure shown in FIG. **9**, the STI regions **0922** in stacked silicon layers such as silicon layer **0916** could be formed substantially of thermally conductive dielectrics including, for example, diamond, carbon, or other dielectrics that have a thermal conductivity higher than silicon dioxide and/or have a thermal conductivity higher than 0.6 W/m-K. This structure can provide enhanced heat spreading in stacked device layers. Thermally conductive STI dielectric regions could be used in the vicinity of the transistors in stacked 3D device layers and may also be utilized as the dielectric that surrounds TLV **0918**, such as dielectric region **0920**. While the thermally conductive shallow trench isolation (STI) regions concept for 3D-ICs is described with an architecture similar to FIG. **2**, similar thermally conductive shallow trench isolation (STI) regions concepts could be used for architectures similar to FIG. **1**, and also for other 3D IC architectures and 2D IC as well. Silicon layer **0904** and silicon layer **0916** may be may be substantially absent of semiconductor dopants to form an undoped silicon region or layer, or doped, such as, for example, with elemental or compound species that form a p+, or p, or p−, or n+, or n, or n− silicon layer or region.

FIG. **10** illustrates an embodiment of the invention, which can provide enhanced heat removal from 3D-ICs using thermally conductive pre-metal dielectric regions in stacked device layers. The 3D-IC and associated power and ground distribution network may be formed as described in FIGS. **1**, **2**, **3**, **4**, **5**, **8** and **9** herein. For example, two crystalline layers, **1004** and **1016**, which may include semiconductor materials such as, for example, mono-crystalline silicon, germanium, GaAs, InP, and graphene, are shown. For this illustration, mono-crystalline (single crystal) silicon may be used. Silicon layer **1016** could be thinned from its original thickness, and its final thickness could be in the range of about 0.01 um to about 50 um, for example, 10 nm, 100 nm, 200 nm, 0.4 um, 1 um, 2 um or 5 um. Silicon layer **1004** could be thinned down from its original thickness, and its final thickness could be in the range of about 0.01 um to about 50 um, for example, 10 nm, 100 nm, 200 nm, 0.4 um, 1 um, 2 um or Sum; however, due to strength considerations, silicon layer **1004** may also be of thicknesses greater than 100 um, depending on, for example, the strength of bonding to heat removal apparatus **1002**. Silicon layer **1004** may include transistors such as, for example, MOSFETS, FinFets, BJTs, HEMTs, HBTs, which may include gate electrode region **1014**, gate dielectric region **1012**, shallow trench isolation (STI) regions **1010** and several other regions that may be necessary for transistors such as source and drain junction regions (not shown for clarity). Silicon layer **1016** may include transistors such as, for example, MOSFETS, FinFets, BJTs, HEMTs, HBTs, which may include gate electrode region **1034**, gate dielectric region **1032**, shallow trench isolation (STI) regions **1022** and several other regions that may be necessary for transistors such as source and drain junction regions (not shown for clarity). A through-layer via (TLV) **1018** may be present and may include an associated surrounding dielectric region **1020**, which may include an STI region. Wiring layers **1008** for silicon layer **1004** and wiring dielectric **1006** may be present and may form an associated interconnect layer or layers. Wiring layers **1038** for silicon layer **1016** and wiring dielectric **1036** may be present and may form an associated interconnect layer or layers. Through-layer via (TLV) **1018** may connect to wiring layers **1008** (not shown). The heat removal apparatus **1002** may include, for example, a heat spreader and/or a heat sink. It can be observed that the STI regions **1022** can go right through to the bottom of silicon layer **1016** and provide good electrical isolation. This, however, can cause challenges for heat removal from the STI surrounded transistors since STI regions **1022** are typically filled with insulators such as silicon dioxide that do not conduct heat well. To tackle this issue, the inter-layer dielectrics (ILD) **1024** for contact region **1026** could be constructed substantially with a thermally conductive material, such as, for example, insulating carbon, diamond, diamond like carbon (DLC), and various other materials that provide better thermal conductivity than silicon dioxide or have a thermal conductivity higher than 0.6 W/m-K. Thermally conductive pre-metal dielectric regions could be used around some of the transistors in stacked 3D device layers. While the thermally conductive pre-metal dielectric regions concept for 3D-ICs is described with an architecture similar to FIG. **2**, similar thermally conductive pre-metal dielectric region concepts could be used for architectures similar to FIG. **1**, and also for other 3D IC architectures and 2D IC as well. Silicon layer **1004** and silicon layer **1016** may be may be substantially absent of semiconductor dopants to form an undoped silicon region or layer, or doped, such as, for example, with elemental or compound species that form a p+, or p, or p−, or n+, or n, or n− silicon layer or region.

FIG. **11** describes an embodiment of the invention, which can provide enhanced heat removal from 3D-ICs using thermally conductive etch stop layers or regions for the first metal level of stacked device layers. The 3D-IC and associated power and ground distribution network may be formed as described in FIGS. **1**, **2**, **3**, **4**, **5**, **8**, **9** and **10** herein. For example, two crystalline layers, **1104** and **1116**, which may include semiconductor materials such as, for example, mono-crystalline silicon, germanium, GaAs, InP, and graphene, are shown. For this illustration, mono-crystalline (single crystal) silicon may be used. Silicon layer **1116** could be thinned from its original thickness, and its final thickness could be in the range of about 0.01 um to about 50 um, for example, 10 nm, 100 nm, 200 nm, 0.4 um, 1 um, 2 um or 5 um. Silicon layer **1104** could be thinned down from its original thickness, and its final thickness could be in the range of about 0.01 um to about 50 um, for example, 10 nm, 100 nm, 200 nm, 0.4 um, 1 um, 2 um or Sum; however, due to strength considerations, silicon layer **1104** may also be of thicknesses greater than 100 um, depending on, for example, the strength of bonding to heat removal apparatus **1102**. Silicon layer **1104** may include transistors such as, for example, MOSFETS, FinFets, BJTs, HEMTs, HBTs, which may include gate electrode region **1114**, gate dielectric region **1112**, shallow trench isolation (STI) regions **1110** and several other regions that may be necessary for transistors such as source and drain junction regions (not shown for clarity). Silicon layer **1116** may include transistors such as, for example, MOSFETS, FinFets, BJTs, HEMTs, HBTs, which may include gate electrode region **1134**, gate dielectric region **1132**, shallow trench isolation (STI) regions **1122** and several other regions that may be necessary for transistors such as source and drain junction regions (not shown for clarity). A through-layer via (TLV) **1118** may be present and may include an associated surround-

ing dielectric region **1120**. Wiring layers **1108** for silicon layer **1104** and wiring dielectric **1106** may be present and may form an associated interconnect layer or layers. Wiring layers for silicon layer **1116** may include first metal layer **1128** and other metal layers **1138** and wiring dielectric **1136** and may form an associated interconnect layer or layers. The heat removal apparatus **1102** may include, for example, a heat spreader and/or a heat sink. It can be observed that the STI regions **1122** can go right through to the bottom of silicon layer **1116** and provide good electrical isolation. This, however, can cause challenges for heat removal from the STI surrounded transistors since STI regions **1122** are typically filled with insulators such as silicon dioxide that do not conduct heat well. To tackle this issue, etch stop layer **1124** as part of the process of constructing the first metal layer **1128** of silicon layer **1116** can be substantially constructed out of a thermally conductive but electrically isolative material. Examples of such thermally conductive materials could include insulating carbon, diamond, diamond like carbon (DLC), and various other materials that provide better thermal conductivity than silicon dioxide and silicon nitride, and/or have thermal conductivity higher than 0.6 W/m-K. Thermally conductive etch-stop layer dielectric regions could be used for the first metal layer above transistors in stacked 3D device layers. While the thermally conductive etch stop layers or regions concept for 3D-ICs is described with an architecture similar to FIG. **2**, similar thermally conductive etch stop layers or regions concepts could be used for architectures similar to FIG. **1**, and also for other 3D IC architectures and 2D IC as well. Silicon layer **1104** and silicon layer **1116** may be may be substantially absent of semiconductor dopants to form an undoped silicon region or layer, or doped, such as, for example, with elemental or compound species that form a p+, or p, or p−, or n+, or n, or n− silicon layer or region.

FIG. **12**A-B describes an embodiment of the invention, which can provide enhanced heat removal from 3D-ICs using thermally conductive layers or regions as part of pre-metal dielectrics for stacked device layers. The 3D-IC and associated power and ground distribution network may be formed as described in FIGS. **1**, **2**, **3**, **4**, **5**, **8**, **9**, **10** and **11** herein. For example, two crystalline layers, **1204** and **1216**, are shown and may have transistors. For this illustration, mono-crystalline (single crystal) silicon may be used. Silicon layer **1216** could be thinned from its original thickness, and its final thickness could be in the range of about 0.01 um to about 50 um, for example, 10 nm, 100 nm, 200 nm, 0.4 um, 1 um, 2 um or 5 um. Silicon layer **1204** could be thinned down from its original thickness, and its final thickness could be in the range of about 0.01 um to about 50 um, for example, 10 nm, 100 nm, 200 nm, 0.4 um, 1 um, 2 um or 5 um; however, due to strength considerations, silicon layer **1204** may also be of thicknesses greater than 100 um, depending on, for example, the strength of bonding to heat removal apparatus **1202**. Silicon layer **1204** may include transistors such as, for example, MOSFETS, FinFets, BJTs, HEMTs, HBTs, which may include gate electrode region **1214**, gate dielectric region **1212**, shallow trench isolation (STI) regions **1210** and several other regions that may be necessary for transistors such as source and drain junction regions (not shown for clarity). Silicon layer **1216** may include transistors such as, for example, MOSFETS, FinFets, BJTs, HEMTs, HBTs, which may include gate electrode region **1234**, gate dielectric region **1232**, shallow trench isolation (STI) regions **1222** and several other regions that may be necessary for transistors such as source and drain junction regions (not shown for clarity). A through-layer via (TLV) **1218** may be present and may include an associated surrounding dielectric region **1220**. Wiring layers **1208** for silicon layer **1204** and wiring dielectric **1206** may be present and may form an associated interconnect layer or layers. Through-layer via (TLV) **1218** may connect to wiring layers **1208** and future wiring layers such as those for interconnection of silicon layer **1216** transistors (not shown). The heat removal apparatus **1202** may include a heat spreader and/or a heat sink. It can be observed that the STI regions **1222** can go right through to the bottom of silicon layer **1216** and provide good electrical isolation. This, however, can cause challenges for heat removal from the STI surrounded transistors since STI regions **1222** are typically filled with insulators such as silicon dioxide that do not conduct heat well. To tackle this issue, a technique is described in FIG. **12**A-B. FIG. **12**A illustrates the formation of openings for making contacts to the transistors of silicon layer **1216**. A hard mask layer **1224** or region is typically used during the lithography step for contact formation and hard mask layer **1224** or region may be utilized to define contact opening regions **1226** of the pre-metal dielectric **1230** that is etched away. FIG. **12**B illustrates the contact **1228** formed after metal is filled into the contact opening regions **1226** shown in FIG. **12**A, and after a chemical mechanical polish (CMP) process. The hard mask layer **1224** or region used for the process shown in FIG. **12**A-B may include a thermally conductive but electrically isolative material. Examples of such thermally conductive materials could include insulating carbon, diamond, diamond like carbon (DLC), and various other materials that provide better thermal conductivity than silicon dioxide and silicon nitride, and/or have thermal conductivity higher than 0.6 W/m-K and can be left behind after the process step shown in FIG. **12**B (hence, electrically non-conductive). Further steps for forming the 3D-IC (such as forming additional metal layers) may be performed (not shown). While the thermally conductive materials for hard mask concept for 3D-ICs is described with an architecture similar to FIG. **2**, similar thermally conductive materials for hard mask concepts could be used for architectures similar to FIG. **1**, and also for other 3D IC architectures and 2D IC as well. Silicon layer **1204** and silicon layer **1216** may be may be substantially absent of semiconductor dopants to form an undoped silicon region or layer, or doped, such as, for example, with elemental or compound species that form a p+, or p, or p−, or n+, or n, or n− silicon layer or region.

FIG. **13** illustrates the layout of an exemplary 4-input NAND gate **1300**, where the output OUT is a function of inputs A, B, C and D. 4-input NAND gate **1300** may include metal **1** regions **1306**, gate regions **1308**, N-type silicon regions **1310**, P-type silicon regions **1312**, contact regions **1314**, and oxide isolation regions **1316**. If the 4-input NAND gate **1300** is used in 3D IC stacked device layers, some regions of the NAND gate (such as, for example, sub-region **1318** of N-type silicon regions **1310**) are far away from V_{DD} and GND contacts of 4-input NAND gate **1300**. The regions, such as sub-region **1318**, could have a high thermal resistance to V_{DD} and GND contacts, and could heat up to undesired temperatures. This is because the regions of the NAND gate far away from V_{DD} and GND contacts cannot effectively use the low-thermal resistance power delivery network to transfer heat to the heat removal apparatus.

FIG. **14** illustrates an embodiment of the invention wherein the layout of exemplary 3D stackable 4-input NAND gate **1400** can be modified so that substantially all parts of the gate are at desirable temperatures during chip operation. Desirable temperatures during chip operation may depend on the type of transistors, circuits, and product application & use, and may be, for example, sub-150° C., sub-100° C., sub-75° C., sub-50° C. or sub-25° C. Inputs to the 3D stackable 4-input

NAND gate **1400** are denoted as A, B, C and D, and the output is denoted as OUT. The 4-input NAND gate **1400** may include metal **1** regions **1406**, gate regions **1408**, N-type silicon regions **1410**, P-type silicon regions **1412**, contact regions **1414**, and oxide isolation regions **1416**. As discussed above, sub-region **1418** could have a high thermal resistance to V_{DD} and GND contacts and could heat up to undesired temperatures. Thermal contact **1420** (whose implementation can be similar to those described in FIG. **6** and FIG. **7**) may be added to the layout, for example as shown in FIG. **13**, to keep the temperature of sub-region **1418** within desirable limits by reducing the thermal resistance from sub-region **1418** to the GND distribution network. Several other implementations of adding and placement of thermal contacts that would be appreciated by persons of ordinary skill in the art can be used to make the exemplary layout shown in FIG. **14** more desirable from a thermal perspective.

FIG. **15** illustrates the layout of an exemplary transmission gate **1500** with inputs A and A'. Transmission gate **1500** may include metal **1** regions **1506**, gate regions **1508**, N-type silicon regions **1510**, P-type silicon regions **1512**, contact regions **1514**, and oxide isolation regions **1516**. If transmission gate **1500** is used in 3D IC stacked device layers, many regions of the transmission gate could heat up to undesired temperatures since there are no V_{DD} and GND contacts. There could be a high thermal resistance to V_{DD} and GND distribution networks. Thus, the transmission gate cannot effectively use the low-thermal resistance power delivery network to transfer heat to the heat removal apparatus.

FIG. **16** illustrates an embodiment of the invention wherein the layout of exemplary 3D stackable transmission gate **1600** can be modified so that substantially all parts of the gate are at desirable temperatures during chip operation. Desirable temperatures during chip operation may depend on the type of transistors, circuits, and product application & use, and may be, for example, sub-150° C., sub-100° C., sub-75° C., sub-50° C. or sub-25° C. Inputs to the 3D stackable transmission gate **1600** are denoted as A and A'. 3D stackable transmission gate **1600** may include metal **1** regions **1606**, gate regions **1608**, N-type silicon regions **1610**, P-type silicon regions **1612**, contact regions **1614**, and oxide isolation regions **1616**. Thermal contacts, such as, for example thermal contact **1620** and second thermal contact **1622** (whose implementation can be similar to those described in FIG. **6** and FIG. **7**) may be added to the layout shown in FIG. **15** to keep the temperature of 3D stackable transmission gate **1600** within desirable limits (by reducing the thermal resistance to the V_{DD} and GND distribution networks). Several other implementations of adding and placement of thermal contacts that would be appreciated by persons of ordinary skill in the art can be used to make the exemplary layout shown in FIG. **16** more desirable from a thermal perspective.

The techniques illustrated with FIG. **14** and FIG. **16** are not restricted to cells such as transmission gates and NAND gates, and can be applied to a number of cells such as, for example, SRAMs, CAMs, multiplexers and many others. Furthermore, the techniques illustrated with at least FIG. **14** and FIG. **16** can be applied and adapted to various techniques of constructing 3D integrated circuits and chips, including those described in U.S. Patent Application Publication 2012/0129301 (allowed U.S. patent application Ser. No. 13/273,712) and pending U.S. patent application Ser. Nos. 13/441,923 and 13/099,010. The contents of the foregoing applications are incorporated herein by reference. Furthermore, techniques illustrated with FIG. **14** and FIG. **16** (and other similar techniques) need not be applied to all such gates on the chip, but could be applied to a portion of gates of that type, such as, for example, gates with higher activity factor, lower threshold voltage or higher drive current. Moreover, thermal contacts and vias may not have to be stacked in a vertical line through multiple stacks, layers, strata of circuits.

When a chip is typically designed a cell library consisting of various logic cells such as NAND gates, NOR gates and other gates is created, and the chip design flow proceeds using this cell library. It will be clear to one skilled in the art that a cell library may be created wherein each cell's layout can be optimized from a thermal perspective and based on heat removal criteria such as maximum allowable transistor channel temperature (for example, where each cell's layout can be optimized such that substantially all portions of the cell have low thermal resistance to the V_{DD} and GND contacts, and therefore, to the power bus and the ground bus).

FIG. **24** illustrates a procedure for a chip designer to ensure a good thermal profile for his or her design. After a first pass or a portion of the first pass of the desired chip layout process is complete, a thermal analysis may be conducted to determine temperature profiles for active or passive elements, such as gates, on the 3D chip. The thermal analysis may be started (**2400**). The temperature of any stacked gate, or region of gates, may be calculated, for example, by simulation such as a multi-physics solver, and compared to a desired specification value (**2410**). If the gate, or region of gates, temperature is higher than the specification, which may, for example, be in the range of 65° C.-150° C., modifications (**2420**) may be made to the layout or design, such as, for example, power grids for stacked layers may be made denser or wider, additional contacts to the gate may be added, more through-silicon (TLV and/or TSV) connections may be made for connecting the power grid in stacked layers to the layer closest to the heat sink, or any other method to reduce stacked layer temperature that may be described herein or in referenced documents, which may be used alone or in combination. The output (**2430**) may give the designer the temperature of the modified stacked gate ('Yes' tree), or region of gates, or an unmodified one ('No' tree), and may include the original un-modified gate temperature that was above the desired specification. The thermal analysis may end (**2440**) or may be iterated. Alternatively, the power grid may be designed (based on heat removal criteria) simultaneously with the logic gates and layout of the design, or for various regions of any layer of the 3D integrated circuit stack. The density of TLVs may be greater than 10^4 per cm^2, and may be 10×, 100×, 1000×, denser than TSVs.

Recessed channel transistors form a transistor family that can be stacked in 3D. FIG. **22** illustrates an exemplary Recessed Channel Transistor **2200** which may be constructed in a 3D stacked layer using procedures outlined in U.S. Patent Application Publication 2012/0129301 (allowed U.S. patent application Ser. No. 13/273,712) and pending U.S. patent application Ser. Nos. 13/441,923 and 13/099,010. The contents of the foregoing applications are incorporated herein by reference. Recessed Channel Transistor **2200** may include **2202** a bottom layer of transistors and wires **2202**, oxide layer **2204**, oxide regions **2206**, gate dielectric **2208**, n+ silicon regions **2210**, gate electrode **2212** and region of p− silicon region **2214**. The recessed channel transistor is surrounded on substantially all sides by thermally insulating oxide layers oxide layer **2204** and oxide regions **2206**, and heat removal may be a serious issue. Furthermore, to contact the p− silicon region **2214**, a p+ region may be needed to obtain low contact resistance, which may not be easy to construct at temperatures lower than approximately 400° C.

FIG. **17**A-D illustrates an embodiment of the invention wherein thermal contacts can be constructed to a recessed

channel transistor. Note that numbers used in FIG. **17**A-D are inter-related. For example, if a certain number is used in FIG. **17**A, it has the same meaning if present in FIG. **17**B. The process flow may begin as illustrated in FIG. **17**A with a bottom layer or layers of transistors and copper interconnects **1702** being constructed with a silicon dioxide layer **1704** atop it. Layer transfer approaches similar to those described in U.S. Patent Application Publication 2012/0129301 (allowed U.S. patent application Ser. No. 13/273,712) and pending U.S. patent application Ser. Nos. 13/441,923 and 13/099,010 may be utilized. The contents of the foregoing applications are incorporated herein by reference. An activated layer of p+ silicon **1706**, an activated layer of p− silicon **1708** and an activated layer of n+ silicon **1710** can be transferred atop the structure illustrated in FIG. **17**A to form the structure illustrated in FIG. **17**B. FIG. **17**C illustrates a next step in the process flow. After forming isolation regions such as, for example, STI-Shallow Trench Isolation (not shown in FIG. **17**C for simplicity) and thus forming p+ regions **1707**, gate dielectric regions **1716** and gate electrode regions **1718** could be formed, for example, by etch and deposition processes, using procedures similar to those described in U.S. Patent Application Publication 2012/0129301 (allowed U.S. patent application Ser. No. 13/273,712) and pending U.S. patent application Ser. Nos. 13/441,923 and 13/099,010. Thus, p− silicon region **1712** and n+ silicon regions **1714** may be formed. FIG. **17**C thus illustrates an RCAT (recessed channel transistor) formed with a p+ silicon region atop copper interconnect regions where the copper interconnect regions are not exposed to temperatures higher than approximately 400° C. FIG. **17**D illustrates a next step of the process where thermal contacts could be made to the p+ silicon region **1707**. FIG. **17**D may include final p− silicon region **1722** and final n+ silicon regions **1720**. Via **1724** may be etched and constructed, for example, of metals (such as Cu, Al, W, degenerately doped Si), metal silicides (WSi_2) or a combination of the two, and may include oxide isolation regions **1726**. Via **1724** can connect p+ region **1707** to the ground (GND) distribution network. Via **1724** could alternatively be connected to a body bias distribution network. Via **1724** and final n+ silicon regions **1720** may be electrically coupled, such as by removal of a portion of an oxide isolation regions **1726**, if desired for circuit reasons (not shown). The nRCAT could have its body region connected to GND potential (or body bias circuit) and operate correctly or as desired, and the heat produced in the device layer can be removed through the low-thermal resistance GND distribution network to the heat removal apparatus (not shown for clarity).

FIG. **18** illustrates an embodiment the invention, which illustrates the application of thermal contacts to remove heat from a pRCAT device layer that is stacked above a bottom layer of transistors and wires **1802**. The p-RCAT layer may include **1804** buried oxide region **1804**, n+ silicon region **1806**, n− silicon region **1814**, p+ silicon region **1810**, gate dielectric **1808** and gate electrode **1812**. The structure shown in FIG. **18** can be constructed using methods similar to those described in respect to FIG. **17**A-D above. The thermal contact **1818** could be constructed of, for example, metals (such as Cu, Al, W, degenerately doped Si), metal silicides (WSi_2) or a combination of two or more types of materials, and may include oxide isolation regions **1816**. Thermal contact **1818** may connect n+ region **1806** to the power (V_{DD}) distribution network. The pRCAT could have its body region connected to the supply voltage (V_{DD}) potential (or body bias circuit) and operate correctly or as desired, and the heat produced in the device layer can be removed through the low-thermal resistance V_{DD} distribution network to the heat removal apparatus. Thermal contact **1818** could alternatively be connected to a body bias distribution network (not shown for clarity). Thermal contact **1818** and p+ silicon region **1810** may be electrically coupled, such as by removal of a portion of an oxide isolation regions **1816**, if desired for circuit reasons (not shown).

FIG. **19** illustrates an embodiment of the invention that describes the application of thermal contacts to remove heat from a CMOS device layer that could be stacked atop a bottom layer of transistors and wires **1902**. The CMOS device layer may include insulator regions **1904**, sidewall insulator regions **1924**, thermal via insulator regions **1930**, such as silicon dioxide. The CMOS device layer may include nMOS p+ silicon region **1906**, pMOS p+ silicon region **1936**, nMOS p− silicon region **1908**, pMOS buried p− silicon region **1912**, nMOS n+ silicon regions **1910**, pMOS n+ silicon **1914**, pMOS n− silicon region **1916**, p+ silicon regions **1920**, pMOS gate dielectric region **1918**, pMOS gate electrode region **1922**, nMOS gate dielectric region **1934** and nMOS gate electrode region. A nMOS transistor could therefore be formed of regions **1934**, **1928**, **1910**, **1908** and **1906**. A pMOS transistor could therefore be formed of regions **1914**, **1916**, **1918**, **1920** and **1922**. This stacked CMOS device layer could be formed with procedures similar to those described in U.S. Patent Application Publication 2012/0129301 (allowed U.S. patent application Ser. No. 13/273,712) and pending U.S. patent application Ser. Nos. 13/441,923 and 13/099,010 and at least FIG. **17**A-D herein. The thermal contact **1926** may be connected between n+ silicon region **1914** and the power (V_{DD}) distribution network and helps remove heat from the pMOS transistor. This is because the pMOSFET could have its body region connected to the supply voltage (V_{DD}) potential or body bias distribution network and operate correctly or as desired, and the heat produced in the device layer can be removed through the low-thermal resistance V_{DD} distribution network to the heat removal apparatus as previously described. The thermal contact **1932** may be connected between p+ silicon region **1906** and the ground (GND) distribution network and helps remove heat from the nMOS transistor. This is because the nMOSFET could have its body region connected to GND potential or body bias distribution network and operate correctly or as desired, and the heat produced in the device layer can be removed through the low-thermal resistance GND distribution network to the heat removal apparatus as previously described.

FIG. **20** illustrates an embodiment of the invention that describes a technique that could reduce heat-up of transistors fabricated on silicon-on-insulator (SOI) substrates. SOI substrates have a buried oxide (BOX) or other insulator between the silicon transistor regions and the heat sink. This BOX region may have a high thermal resistance, and makes heat transfer from the transistor regions to the heat sink difficult. The nMOS transistor in SOI may include buried oxide regions **2036**, BEOL metal insulator regions **2048**, and STI insulator regions **2056**, such as silicon dioxide. The nMOS transistor in SOI may include n+ silicon regions **2046**, p− silicon regions **2040**, gate dielectric region **2052**, gate electrode region **2054**, interconnect wiring regions **2044**, and highly doped silicon substrate **2004**. Use of silicon-on-insulator (SOI) substrates may lead to low heat transfer from the transistor regions to the heat removal apparatus **2002** through the buried oxide regions **2036** (generally a layer) that may have low thermal conductivity. The ground contact **2062** of the nMOS transistor shown in FIG. **20** can be connected to the ground distribution network wiring **2064** which in turn can be connected with a low thermal resistance connection **2050** to highly doped silicon substrate **2004**. This enables low thermal

conductivity, a thermal conduction path, between the transistor shown in FIG. **20** and the heat removal apparatus **2002**. While FIG. **20** described how heat could be transferred among an nMOS transistor and the heat removal apparatus, similar approaches can also be used for pMOS transistors, and many other transistors, for example, FinFets, BJTs, HEMTs, and HBTs. Many of the aforementioned transistors may be constructed as fully depleted channel devices.

FIG. **21** illustrates an embodiment of the invention which describes a technique that could reduce heat-up of transistors fabricated on silicon-on-insulator (SOI) substrates. The nMOS transistor in SOI may include buried oxide regions **2136**, BEOL metal insulator regions **2148**, and STI insulator regions **2156**, such as silicon dioxide. The nMOS transistor in SOI may include n+ silicon regions **2146**, p− silicon regions **2140**, gate dielectric region **2152**, gate electrode region **2154**, interconnect wiring regions **2144**, and highly doped silicon substrate **2104**. Use of silicon-on-insulator (SOI) substrates may lead to low heat transfer from the transistor regions to the heat removal apparatus **2102** through the buried oxide regions **2136** (generally a layer) that may have low thermal conductivity. The ground contact **2162** of the nMOS transistor shown in FIG. **21** can be connected to the ground distribution network **2164** which in turn can be connected with a low thermal resistance connection **2150** to highly doped silicon substrate **2104** through an implanted and activated region **2110**. The implanted and activated region **2110** could be such that thermal contacts similar to those in FIG. **6** can be formed. This may enable low thermal conductivity, a thermal conduction path, between the transistor shown in FIG. **21** and the heat removal apparatus **2102**. This thermal conduction path, whilst thermally conductive, may not be electrically conductive (due to the reverse biased junctions that could be constructed in the path), and thus, not disturb the circuit operation. While FIG. **21** described how heat could be transferred among the nMOS transistor and the heat removal apparatus, similar approaches can also be used for pMOS transistors, and other transistors, for example, FinFets, BJTs, HEMTs, and HBTs.

FIG. **23** illustrates an embodiment of the invention wherein heat spreading regions may be located on the sides of 3D-ICs. The 3D integrated circuit shown in FIG. **23** could be potentially constructed using techniques described in U.S. Patent Application Publication 2012/0129301 (allowed U.S. patent application Ser. No. 13/273,712) and pending U.S. patent application Ser. Nos. 13/441,923 and 13/099,010. For example, two crystalline layers, **2304** and **2316**, which may include semiconductor materials such as, for example, monocrystalline silicon, germanium, GaAs, InP, and graphene, are shown. For this illustration, mono-crystalline (single crystal) silicon may be used. Silicon layer **2316** could be thinned from its original thickness, and its final thickness could be in the range of about 0.01 um to about 50 um, for example, 10 nm, 100 nm, 200 nm, 0.4 um, 1 um, 2 um or 5 um. Silicon layer **2304** could be thinned down from its original thickness, and its final thickness could be in the range of about 0.01 um to about 50 um, for example, 10 nm, 100 nm, 200 nm, 0.4 um, 1 um, 2 um or 5 um; however, due to strength considerations, silicon layer **2304** may also be of thicknesses greater than 100 um, depending on, for example, the strength of bonding to heat removal apparatus **2302**. Silicon layer **2304** may include transistors such as, for example, MOSFETS, FinFets, BJTs, HEMTs, HBTs, which may include gate electrode region **2314**, gate dielectric region **2312**, and shallow trench isolation (STI) regions **2310** and several other regions that may be necessary for transistors such as source and drain junction regions (not shown for clarity). Silicon layer **2316** may include transistors such as, for example, MOSFETS, FinFets, BJTs, HEMTs, HBTs, which may include gate electrode region **2334**, gate dielectric region **2332**, and shallow trench isolation (STI) regions **2322** and several other regions that may be necessary for transistors such as source and drain junction regions (not shown for clarity). It can be observed that the STI regions **2322** can go right through to the bottom of silicon layer **2316** and provide good electrical isolation. A through-layer via (TLV) **2318** may be present and may include an associated surrounding dielectric region **2320**. Dielectric region **2320** may include a shallow trench isolation region. Wiring layers **2308** for silicon layer **2304** and wiring dielectric **2306** may be present and may form an associated interconnect layer or layers. Wiring layers **2338** for silicon layer **2316** and wiring dielectric **2336** may be present and may form an associated interconnect layer or layers. Through-layer via (TLV) **2318** may connect to wiring layers **2308** and wiring layers **2338** (not shown). The heat removal apparatus **2302** may include a heat spreader and/or a heat sink. Thermally conductive material regions **2340** could be present at the sides of the 3D-IC shown in FIG. **23**. Thermally conductive material regions **2340** may be formed by sequential layer by layer etch and fill, or by an end of process etch and fill. Thus, a thermally conductive heat spreading region could be located on the sidewalls of a 3D-IC. The thermally conductive material regions **2340** could include dielectrics such as, for example, insulating carbon, diamond, diamond like carbon (DLC), and other dielectrics that have a thermal conductivity higher than silicon dioxide and/or have a thermal conductivity higher than 0.6 W/m-K. Another method that could be used for forming thermally conductive material regions **2340** could involve depositing and planarizing the thermally conductive material at locations on or close to the dicing regions, such as potential dicing scribe lines (described in U.S. Patent Application Publication 2012/0129301) of a 3D-IC after an etch process. The wafer could be diced. Those of ordinary skill in the art will appreciate that one could combine the concept of having thermally conductive material regions on the sidewalls of 3D-ICs with concepts shown in other figures of this patent application, such as, for example, the concept of having lateral heat spreaders shown in FIG. **8**. Silicon layer **2304** and silicon layer **2316** may be may be substantially absent of semiconductor dopants to form an undoped silicon region or layer, or doped, such as, for example, with elemental or compound species that form a p+, or p, or p−, or n+, or n, or n− silicon layer or region.

FIG. **25** illustrates an exemplary monolithic 3D integrated circuit. The 3D integrated circuit shown in FIG. **25** could be potentially constructed using techniques described in U.S. Patent Application Publication 2012/0129301 (allowed U.S. patent application Ser. No. 13/273,712) and pending U.S. patent application Ser. Nos. 13/441,923 and 13/099,010. For example, two crystalline layers, **2504** and **2516**, which may include semiconductor materials such as, for example, monocrystalline silicon, germanium, GaAs, InP, and graphene, are shown. For this illustration, mono-crystalline (single crystal) silicon may be used. Silicon layer **2516** could be thinned from its original thickness, and its final thickness could be in the range of about 0.01 um to about 50 um, for example, 10 nm, 100 nm, 200 nm, 0.4 um, 1 um, 2 um or 5 um. Silicon layer **2504** could be thinned down from its original thickness, and its final thickness could be in the range of about 0.01 um to about 50 um, for example, 10 nm, 100 nm, 200 nm, 0.4 um, 1 um, 2 um or 5 um; however, due to strength considerations, silicon layer **2504** may also be of thicknesses greater than 100 um, depending on, for example, the strength of bonding to heat removal apparatus **2502**. Silicon layer **2504**, or silicon

substrate, may include transistors such as, for example, MOSFETS, FinFets, BJTs, HEMTs, HBTs, which may include gate electrode region **2514**, gate dielectric region **2512**, transistor junction regions **2510** and several other regions that may be necessary for transistors such as source and drain junction regions (not shown for clarity). Silicon layer **2516** may include transistors such as, for example, MOSFETS, FinFets, BJTs, HEMTs, HBTs, which may include gate electrode region **2534**, gate dielectric region **2532**, transistor junction regions **2530** and several other regions that may be necessary for transistors such as source and drain junction regions (not shown for clarity). A through-silicon connection **2518**, or TLV (through-silicon via) could be present and may have a surrounding dielectric region **2520**. Surrounding dielectric region **2520** may include a shallow trench isolation (STI) region, such as one of the shallow trench isolation (STI) regions typically in a 3D integrated circuit stack (not shown). Silicon layer **2504** may have wiring layers **2508** and wiring dielectric **2506**. Wiring layers **2508** and wiring dielectric **2506** may form an associated interconnect layer or layers. Silicon layer **2516** may have wiring layers **2538** and wiring dielectric **2536**. Wiring layers **2538** and wiring dielectric **2536** may form an associated interconnect layer or layers. Wiring layers **2538** and wiring layers **2508** may be constructed of copper, aluminum or other materials with bulk resistivity lower than 2.8 uohm-cm. The choice of materials for through-silicon connection **2518** may be challenging. If copper is chosen as the material for through-silicon connection **2518**, the co-efficient of thermal expansion (CTE) mismatch between copper and the surrounding mono-crystalline silicon layer **2516** may become an issue. Copper has a CTE of approximately 16.7 ppm/K while silicon has a CTE of approximately 3.2 ppm/K. This large CTE mismatch may cause reliability issues and the need for large keep-out zones around the through-silicon connection **2518** wherein transistors cannot be placed. If transistors are placed within the keep-out zone of the through-silicon connection **2518**, their current-voltage characteristics may be different from those placed in other areas of the chip. Similarly, if Aluminum (CTE=23 ppm/K) is used as the material for through-silicon connection **2518**, its CTE mismatch with the surrounding mono-crystalline silicon layer **2516** could cause large keep-out zones and reliability issues. Silicon layer **2504** and silicon layer **2516** may be may be substantially absent of semiconductor dopants to form an undoped silicon region or layer, or doped, such as, for example, with elemental or compound species that form a p+, or p, or p−, or n+, or n, or n− silicon layer or region.

An embodiment of the invention utilizes a material for the through-silicon connection **2518** (TSV or TLV) that may have a CTE closer to silicon than, for example, copper or aluminum. The through-silicon connection **2518** may include materials such as, for example, tungsten (CTE approximately 4.5 ppm/K), highly doped polysilicon or amorphous silicon or single crystal silicon (CTE approximately 3 ppm/K), conductive carbon, or some other material with CTE less than 15 ppm/K. Wiring layers **2538** and wiring layers **2508** may have materials with CTE greater than 15 ppm/K, such as, for example, copper or aluminum.

Persons of ordinary skill in the art will appreciate that the illustrations in FIG. **25** are exemplary only and are not drawn to scale. Such skilled persons will further appreciate that many variations are possible such as, for example, the through-silicon connection **2518** may include materials in addition to those (such as Tungsten, conductive carbon) described above, for example, liners and barrier metals such as TiN, TaN, and other materials known in the art for via, contact, and through silicon via formation. Moreover, the transistors in silicon layer **2504** may be formed in a manner similar to silicon layer **2516**. Furthermore, through-silicon connection **2518** may be physically and electrically connected (not shown) to wiring layers **2508** and wiring layers **2538** by the same material as the wiring layers **2508**/**2538**, or by the same materials as the through-silicon connection **2518** composition, or by other electrically and/or thermally conductive materials not found in the wiring layers **2508**/**2538** or the through-silicon connection **2518**. Many other modifications within the scope of the invention will suggest themselves to such skilled persons after reading this specification. Thus the invention is to be limited only by the appended claims.

A planar n-channel Junction-Less Recessed Channel Array Transistor (JL-RCAT) suitable for a monolithic 3D IC may be constructed as follows. The JL-RCAT may provide an improved source and drain contact resistance, thereby allowing for lower channel doping, and the recessed channel may provide for more flexibility in the engineering of channel lengths and transistor characteristics, and increased immunity from process variations. FIG. **26**A-F illustrates an exemplary n-channel JL-RCAT which may be constructed in a 3D stacked layer using procedures outlined below and in U.S. Patent Application Publication 2012/0129301 (allowed U.S. patent application Ser. No. 13/273,712) and pending U.S. patent application Ser. Nos. 13/441,923 and 13/099,010. The contents of the foregoing applications are incorporated herein by reference.

As illustrated in FIG. **26**A, a N− substrate donor wafer **2600** may be processed to include wafer sized layers of N+ doping **2602**, and N− doping **2603** across the wafer. The N+ doped layer **2602** may be formed by ion implantation and thermal anneal. N− doped layer **2603** may have additional ion implantation and anneal processing to provide a different dopant level than N− substrate donor wafer **2600**. N− doped layer **2603** may have graded or various layers of N− doping to mitigate transistor performance issues, such as, for example, short channel effects, after the JL-RCAT is formed. The layer stack may alternatively be formed by successive epitaxially deposited doped silicon layers of N+ **2602** and N− **2603**, or by a combination of epitaxy and implantation. Annealing of implants and doping may include, for example, conductive/inductive thermal, optical annealing techniques or types of Rapid Thermal Anneal (RTA or spike). The N+ doped layer **2602** may have a doping concentration that may be more than 10× the doping concentration of N− doped layer **2603**. N− doped layer **2603** may have a thickness that may allow fully-depleted channel operation when the JL-RCAT transistor is substantially completely formed, such as, for example, less than 5 nm, less than 10 nm, or less than 20 nm.

As illustrated in FIG. **26**B, the top surface of N− substrate donor wafer **2600** may be prepared for oxide wafer bonding with a deposition of an oxide or by thermal oxidation of N− doped layer **2603** to form oxide layer **2680**. A layer transfer demarcation plane (shown as dashed line) **2699** may be formed by hydrogen implantation or other methods as described in the incorporated references. The N− substrate donor wafer **2600** and acceptor wafer **2610** may be prepared for wafer bonding as previously described and low temperature (less than approximately 400° C.) bonded. Acceptor wafer **2610**, as described in the incorporated references, may include, for example, transistors, circuitry, and metal, such as, for example, aluminum or copper, interconnect wiring, and thru layer via metal interconnect strips or pads. The portion of the N+ doped layer **2602** and the N− substrate donor wafer **2600** that may be above the layer transfer demarcation plane

2699 may be removed by cleaving or other low temperature processes as described in the incorporated references, such as, for example, ion-cut or other layer transfer methods.

As illustrated in FIG. 26C, oxide layer 2680, N− doped layer 2603, and remaining N+ layer 2622 have been layer transferred to acceptor wafer 2610. The top surface of N+ layer 2622 may be chemically or mechanically polished. Now transistors may be formed with low temperature (less than approximately 400° C.) processing and aligned to the acceptor wafer alignment marks (not shown) as described in the incorporated references.

As illustrated in FIG. 26D, the transistor isolation regions 2605 may be formed by mask defining and plasma/RIE etching N+ layer 2622 and N− doped layer 2603 substantially to the top of oxide layer 2680 (not shown), substantially into oxide layer 2680, or into a portion of the upper oxide layer of acceptor wafer 2610 (not shown). A low-temperature gap fill oxide may be deposited and chemically mechanically polished, the oxide remaining in isolation regions 2605. The recessed channel 2606 may be mask defined and etched thru N+ doped layer 2622 and partially into N− doped layer 2603. The recessed channel surfaces and edges may be smoothed by processes, such as, for example, wet chemical, plasma/RIE etching, low temperature hydrogen plasma, or low temperature oxidation and strip techniques, to mitigate high field effects. The low temperature smoothing process may employ, for example, a plasma produced in a TEL (Tokyo Electron Labs) SPA (Slot Plane Antenna) machine. Thus N+ source and drain regions 2632 and N− channel region 2623 may be formed, which may substantially form the transistor body. The doping concentration of N+ source and drain regions 2632 may be more than 10× the concentration of N− channel region 2623. The doping concentration of the N− channel region 2623 may include gradients of concentration or layers of differing doping concentrations. The etch formation of recessed channel 2606 may define the transistor channel length. The shape of the recessed etch may be rectangular as shown, or may be spherical (generally from wet etching, sometimes called an S-RCAT: spherical RCAT), or a variety of other shapes due to etching methods and shaping from smoothing processes, and may help control for the channel electric field uniformity. The thickness of N− channel region 2623 in the region below recessed channel 2606 may be of a thickness that allows fully-depleted channel operation. The thickness of N− channel region 2623 in the region below N+ source and drain regions 2632 may be of a thickness that allows fully-depleted transistor operation.

As illustrated in FIG. 26E, a gate dielectric 2607 may be formed and a gate metal material may be deposited. The gate dielectric 2607 may be an atomic layer deposited (ALD) gate dielectric that may be paired with a work function specific gate metal in the industry standard high k metal gate process schemes described in the incorporated references. Alternatively, the gate dielectric 2607 may be formed with a low temperature processes including, for example, oxide deposition or low temperature microwave plasma oxidation of the silicon surfaces and a gate material with proper work function and less than approximately 400° C. deposition temperature such as, for example, tungsten or aluminum may be deposited. The gate material may be chemically mechanically polished, and the gate area defined by masking and etching, thus forming the gate electrode 2608.

As illustrated in FIG. 26F, a low temperature thick oxide 2609 may be deposited and planarized, and source, gate, and drain contacts, and thru layer via (not shown) openings may be masked and etched preparing the transistors to be connected via metallization. Thus gate contact 2611 connects to gate electrode 2608, and source & drain contacts 2640 connect to N+ source and drain regions 2632. The thru layer via (not shown) provides electrical coupling among the donor wafer transistors and the acceptor wafer metal connect pads or strips (not shown) as described in the incorporated references.

The formation procedures of and use of the N+ source and drain regions 2632 that may have more than 10× the concentration of N− channel region 2623 may enable low contact resistance in a FinFet type transistor, wherein the thickness of the transistor channel is greater than the width of the channel, the transistor channel width being perpendicular to a line formed between the source and drain.

Persons of ordinary skill in the art will appreciate that the illustrations in FIGS. 26A through 26F are exemplary only and are not drawn to scale. Such skilled persons will further appreciate that many variations are possible such as, for example, a p-channel JL-RCAT may be formed with changing the types of dopings appropriately. Moreover, the N− substrate donor wafer 2600 may be p type. Further, N− doped layer 2603 may include multiple layers of different doping concentrations and gradients to fine tune the eventual JL-RCAT channel for electrical performance and reliability characteristics, such as, for example, off-state leakage current and on-state current. Furthermore, isolation regions 2605 may be formed by a hard mask defined process flow, wherein a hard mask stack, such as, for example, silicon oxide and silicon nitride layers, or silicon oxide and amorphous carbon layers, may be utilized. Moreover, CMOS JL-RCATs may be constructed with n-JLRCATs in a first mono-crystalline silicon layer and p-JLRCATs in a second mono-crystalline layer, which may include different crystalline orientations of the mono-crystalline silicon layers, such as for example, <100>, <111> or <551>, and may include different contact silicides for optimum contact resistance to p or n type source, drains, and gates. Furthermore, a back-gate or double gate structure may be formed for the JL-RCAT and may utilize techniques described in the incorporated references. Further, efficient heat removal and transistor body biasing may be accomplished on a JL-RCAT by adding an appropriately doped buried layer (P− in the case of a n-JL-RCAT), forming a buried layer region underneath the N− channel region 2623 for junction isolation, and connecting that buried region to a thermal and electrical contact, similar to what is described for layer 1606 and region 1646 in FIGS. 16A-G in the incorporated reference pending U.S. patent application Ser. No. 13/441,923. Many other modifications within the scope of the invention will suggest themselves to such skilled persons after reading this specification. Thus the invention is to be limited only by the appended claims.

When formation of a 3D-IC is discussed herein, crystalline layers, for example, two crystalline layers, 2504 and 2516, are utilized to form the monolithic 3D-IC, generally utilizing layer transfer techniques. Similarly, donor layers and acceptor layers of crystalline materials which are referred to and utilized in the referenced US patent documents including U.S. Patent Application Publication 2012/0129301 (allowed U.S. patent application Ser. No. 13/273,712) and pending U.S. patent application Ser. Nos. 13/441,923 and 13/099,010 may be utilized to form a monolithic 3D-IC, generally utilizing layer transfer techniques. The crystalline layers, whether donor or acceptor layer, may include regions of compound semiconductors, such as, for example, InP, GaAs, and/or GaN, and regions of mono-crystalline silicon and/or silicon dioxide. Heterogeneous integration with short interconnects between the compound semiconductor transistors and the

silicon based transistors (such as CMOS) could be enabled by placing or constructing Si—CS hetero-layers into a monolithic 3D-IC structure.

As illustrated in FIG. **27**, an exemplary Si—CS hetero donor or acceptor substrate may be formed by utilizing an engineered substrate, for example, SOLES as manufactured and offered for sale by SOITEC S.A. As illustrated in FIG. **27**A, engineered substrate may include silicon substrate **2700**, buried oxide layer **2702**, compound semiconductor template layer **2704**, for example, Germanium, oxide layer **2705**, and silicon layer **2706**, for example, mono-crystalline silicon.

As illustrated in FIG. **27**B, regions of silicon layer **2706** may be mask defined and etched away, exposing regions of the top surface of compound semiconductor template layer **2704** and thus forming silicon regions **2707** and oxide regions **2715**. High quality compound semiconductor regions **2708** may be epitaxially grown in the exposed regions of compound semiconductor template layer **2704**. One example of compound semiconductor growth on an engineered substrate may be found in "Liu, W. K., et al., "Monolithic integration of InP-based transistors on Si substrates using MBE," J. Crystal Growth 311 (2009), pp. 1979-1983." Alternatively, an engineered substrate as described in FIG. **27**A but without silicon layer **2706** may be utilized to eliminate the silicon layer removal etch.

As illustrated in FIG. **27**C, silicon regions **2707** may be mask defined and etched partially or fully away and oxide isolation regions **2710** may be formed by, for example, deposition, densification and etchback/planarization of an SACVD oxide such as in a typical STI (Shallow Trench Isolation) process. Alternatively, compound semiconductor template layer **2704** regions that may be below silicon regions **2707** may also be etched away and the oxide fill may proceed.

As illustrated in FIG. **28**, alternatively, an exemplary Si—CS hetero donor or acceptor substrate may be formed by epitaxial growth directly on a silicon or SOI substrate. As illustrated in FIG. **28**A, buffer layers **2802** may be formed on mono-crystalline silicon substrate **2800** and high quality compound semiconductor layers **2804** may be epitaxially grown on top of the surface of buffer layers **2802**. Buffer layers **2802** may include, for example, MBE grown materials and layers that help match the lattice between the mono-crystalline silicon substrate **2800** and compound semiconductor layers **2804**. For an InP HEMT, buffer layers **2802** may include an AlAs initiation layer, GaAs lattice matching layers, and a graded $In_xAl_{1-x}As$ buffer, $0<x<0.6$. Compound semiconductor layers **2804** may include, for example, barrier, channel, and cap layers. One example of compound semiconductor growth directly on a mono-crystalline silicon substrate may be found in "Hoke, W. E., et al., "AlGaN/GaN high electron mobility transistors on 100 mm silicon substrates by plasma molecular beam epitaxy," Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures, (29) 3, May 2011, pp. 03C107-03C107-5."

As illustrated in FIG. **28**B, compound semiconductor layers **2804** and buffer layers **2802** may be mask defined and etched substantially away and oxide isolation regions **2810** may be formed by, for example, deposition, densification and etchback/planarization of an SACVD oxide such as in a typical STI (Shallow Trench Isolation) process. Thus, compound semiconductor regions **2808** and buffer regions **2805** may be formed.

The substrates formed and described in FIGS. **27** and **28** may be utilized in forming 3D-ICs, for example, as donor layers and/or acceptor layers of crystalline materials, as described in the referenced US patent documents including U.S. Patent Application Publication 2012/0129301 (allowed U.S. patent application Ser. No. 13/273,712) and pending U.S. patent application Ser. Nos. 13/441,923 and 13/099,010 generally by layer transfer techniques, such as, for example, ion-cut. For example, repetitive preformed transistor structures such as illustrated in at least FIGS. 32, 33, 73-80 and related specification sections in U.S. Patent Application Publication 2012/0129301 (allowed U.S. patent application Ser. No. 13/273,712) may be utilized on Si—CS substrates such as FIGS. **27**B, **27**C, and/or **28**B to form stacked 3D-ICs wherein at least one layer may have compound semiconductor transistors. For example, non-repetitive transistor structures such as illustrated in at least FIGS. 57, 58, 65-68, 151, 152, 157, 158 and 160-161 and related specification sections in U.S. Patent Application Publication 2012/0129301 (allowed U.S. patent application Ser. No. 13/273,712) may be utilized on Si—CS substrates such as FIGS. **27**A and/or **28**A to form stacked 3D-ICs wherein at least one layer may have compound semiconductor transistors. Defect anneal techniques, such as those illustrated in at least FIGS. **184**-**189** and related specification sections in U.S. Patent Application Publication 2012/0129301 (allowed U.S. patent application Ser. No. 13/273,712) may be utilized to anneal and repair defects in the layer transferred, generally ion-cut, substrates of FIGS. **27** and **28** herein this document.

FIGS. **29**A-H illustrate via cross section drawings the use of the Oxide-CS substrate of FIG. **27**C to form a closely coupled but independently optimized silicon and compound semiconductor device stack by using layer transfer techniques. The oxide-CS substrate of FIG. **28**B may also be utilized.

As illustrated in FIG. **29**A, Oxide-CS engineered substrate **2990** may include silicon substrate **2900**, buried oxide layer **2902**, compound semiconductor template layer **2904**, for example, Germanium, compound semiconductor regions **2908**, and oxide isolation regions **2910**. Oxide regions **2715** such as shown in FIG. **27**C are omitted for clarity. Oxide-CS engineered substrate **2990** may include alignment marks (not shown).

As illustrated in FIG. **29**B, Oxide-CS engineered substrate **2990** may be processed to form compound semiconductor transistor, such as, for example, InP, GaAs, SiGe, GaN HEMTs and HBTs, and a metal interconnect layer or layers wherein the top metal interconnect layer may include a CS donor wafer orthogonal connect strip **2928**. The details of the orthogonal connect strip methodology may be found as illustrated in at least FIGS. 30-33, 73-80, and 94 and related specification sections of U.S. Patent Application Publication 2012/0129301 (allowed U.S. patent application Ser. No. 13/273,712). The length of CS donor wafer orthogonal connect strip **2928** may be drawn/layed-out over and parallel to the oxide isolation regions **2910**. CS donor wafer bonding oxide **2930** may be deposited in preparation for oxide-oxide bonding. Thus, CS donor substrate **2991** may include silicon substrate **2900**, buried oxide layer **2902**, compound semiconductor template layer **2904**, compound semiconductor regions **2908**, oxide isolation regions **2910**, compound semiconductor transistor source and drain regions **2920**, compound semiconductor transistor gate regions **2922**, CS donor substrate metallization isolation dielectric regions **2924**, CS donor substrate metal interconnect wire and vias **2926**, CS donor wafer orthogonal connect strip **2928**, and CS donor wafer bonding oxide **2930**.

As illustrated in FIG. **29**C, crystalline substrate **2940** may be processed to form transistors, such as, for example, mono-crystalline silicon PMOSFETs and NMOSFETs, and a metal interconnect layer or layers wherein the top metal intercon-

nect layer may include a base substrate orthogonal connect strip **2949**. The details of the orthogonal connect strip methodology may be found as illustrated in at least FIGS. 30-33, 73-80, and 94 and related specification sections of U.S. Patent Application Publication 2012/0129301 (allowed U.S. patent application Ser. No. 13/273,712). Crystalline substrate **2940** may include semiconductor materials such as mono-crystalline silicon. The base substrate orthogonal connect strip **2949** may be drawn/laid-out in an orthogonal and mid-point intersect crossing manner with respect to the CS donor wafer orthogonal connect strip **2928**. Acceptor wafer bonding oxide **2932** may be deposited in preparation for oxide-oxide bonding. Thus, acceptor base substrate **2992** may include crystalline substrate **2940**, well regions **2942**, Shallow Trench Isolation (STI) regions **2944**, transistor source and drain regions **2945**, transistor gate stack regions **2946**, base substrate metallization isolation dielectric regions **2947**, base substrate metal interconnect wires and vias **2948**, base substrate orthogonal connect strip **2949**, and acceptor wafer bonding oxide **2932**. Acceptor base substrate **2992** may include alignment marks (not shown).

As illustrated in FIG. **29**D, CS donor substrate **2991** may be flipped over, aligned (using information from alignment marks in CS donor substrate **2991** and acceptor base substrate **2992**), and oxide to oxide bonded to acceptor base substrate **2992**. The bonding may take place between the large area surfaces of acceptor wafer bonding oxide **2932** and CS donor wafer bonding oxide **2930**. The bond may be made at low temperatures, such as less than about 400° C., so to protect the base substrate metallization and isolation structures. Thus, CS-base bonded substrate structure **2993** may be formed. The lengths of base substrate orthogonal connect strip **2949** and CS donor wafer orthogonal connect strip **2928** may be designed to compensate for misalignment of the wafer to wafer bonding process and other errors, as described in the referenced related specification cited previously. Pre-bond plasma pre-treatments and thermal anneals, such as a 250° C. anneal, may be utilized to strengthen the low temperature oxide-oxide bond.

As illustrated in FIG. **29**E, crystalline substrate **2940** of CS-base bonded substrate structure **2993** may be removed by processes such as wet etching crystalline substrate **2940** with warm KOH after protecting the sidewalls and backside of CS-base bonded substrate structure **2993** with, for example, resist and/or wax. Plasma, RIE, and/or CMP processes may also be employed. Thus CS-base bonded structure **2994** may be formed.

As illustrated in FIG. **29**F, CS-base bonded structure **2994** may be processed to connect base substrate orthogonal connect strip **2949** to CS donor wafer orthogonal connect strip **2928** and thus form a short CS transistor to base CMOS transistor interconnect. Buried oxide layer **2902** and compound semiconductor template layer **2904** may be mask defined and etched substantially away in regions and oxide region **2950** may be formed by, for example, deposition, densification and etchback/planarization of a low temperature oxide, such as an SACVD oxide. Stitch via **2952** may be masked and etched through oxide region **2950**, the indicated oxide isolation region **2910** (thus forming oxide regions **2911**), CS donor substrate metallization isolation dielectric regions **2924**, acceptor wafer bonding oxide **2932** and CS donor wafer bonding oxide **2930**. Stitch via **2952** may be processed with a metal fill such as, for example, barrier metals such as TiN or CoN, and metal fill with Cu, W, or Al, and CMP polish to electrically (and physically) bridge or stitch base substrate orthogonal connect strip **2949** to CS donor wafer orthogonal connect strip **2928**, thus forming a CS transistor to base CMOS transistor interconnect path. CS-base interconnected structure **2995** may thus be formed. FIG. **29**G includes a top view of the CS-base interconnected structure **2995** showing stitch via **2952** connecting the base substrate orthogonal connect strip **2949** to CS donor wafer orthogonal connect strip **2928**. Highlighted CS donor substrate metal interconnect CS source wire and via **2927** (one of the CS donor substrate metal interconnect wire and vias **2926**) may provide the connection from the CS transistor to the CS donor wafer orthogonal connect strip **2928**, which may be connected to the base substrate metal interconnect wires and vias **2948** (and thus the base substrate transistors) thru the stitch via **2952** and base substrate orthogonal connect strip **2949**. Thus, a connection path may be formed between the CS transistor of the second, or donor, layer of the stack, and the CMOS transistors residing in the base substrate layer, or first layer.

As illustrated in FIG. **29**H top drawing, CS-base interconnected structure **2995** may be further processed to create orthogonal metal interconnect strips and stacking of a second CS transistor layer (thus the third layer in the stack) in a similar manner as described above in FIGS. **29**A-F. Thus a third layer including CS#2 transistors, which may be a different type of CS transistor than the CS#1 transistors on the second layer, may be stacked and connected to the CS (#1) transistors of the second layer of CS-base interconnected structure **2995** and the CMOS transistors of the first layer of CS-base interconnected structure **2995**. As illustrated in FIG. **29**H bottom drawing, CS-base interconnected structure **2995** may be further processed to create orthogonal metal interconnect strips and stacking of a third layer in a similar manner as described above in FIGS. **29**A-F, wherein that third layer may be a layer that includes, for example, MEMS sensor, image projector, SiGe transistors, or CMOS.

Persons of ordinary skill in the art will appreciate that the illustrations in FIG. **29** are exemplary and are not drawn to scale. Such skilled persons will further appreciate that many variations may be possible such as, for example, various types and structures of CS transistors may be formed and are not limited to the types and structures of transistors that may be suggested by the drawing illustrations. Moreover, non-repetitive transistor structures, techniques and formation process flows of CMOS and/or CS transistors at low temp on top of CMOS such as illustrated in at least FIGS. 57, 58, 65-68, 151, 152, 157, 158 and 160-161 and related specification sections in U.S. Patent Application Publication 2012/0129301 (allowed U.S. patent application Ser. No. 13/273,712) may be utilized. Further, during the backside etch step of FIG. **29**E to remove crystalline substrate **2940**, the etch may be continued (may switch chemistries, techniques) to remove buried oxide layer **2902** and partially or substantially remove compound semiconductor template layer **2904**. Moreover, bonding methods other than oxide to oxide, such as oxide to metal, hybrid (metal and oxide to metal and oxide), may be utilized. Further, an ion-cut process may be used as part of the layer transfer process. Many other modifications within the scope of the illustrated embodiments of the invention will suggest themselves to such skilled persons after reading this specification. Thus the invention is to be limited only by the appended claims.

Three dimensional devices offer a new possibility of partitioning designs into multiple layers or strata based various criteria, such as, for example, routing demands of device blocks in a design, lithographic process nodes, speed, cost, and density. Many of the criteria are illustrated in at least FIGS. 13, 210-215, and 239 and related specification sections in U.S. Patent Application Publication 2012/0129301 (al-

lowed U.S. patent application Ser. No. 13/273,712), the contents are incorporated herein by reference. An additional criterion for partitioning decision-making may be one of trading cost for process complexity/attainment. For example, spacer based patterning techniques, wherein a lithographic critical dimension can be replicated smaller than the original image by single or multiple spacer depositions, spacer etches, and subsequent image (photoresist or prior spacer) removal, are becoming necessary in the industry to pattern smaller linewidths while still using the longer wavelength steppers and imagers. Other double, triple, and quad patterning techniques, such as pattern and cut, may also be utilized to overcome the lithographic constraints of the current imaging equipment. However, the spacer based and multiple pattering techniques are expensive to process and yield, and generally may be constraining to design and layout: they generally require regular patterns, sometimes substantially all parallel lines. An embodiment of the invention is to partition a design into those blocks and components that may be amenable and efficiently constructed by the above expensive patterning techniques onto one or more layers in the 3D-IC, and partition the other blocks and components of the design onto different layers in the 3D-IC. As illustrated in FIG. **30**, third layer of circuits and transistors **3004** may be stacked on top of second layer of circuits and transistors **3002**, which may be stacked on top of first layer/substrate of circuits and transistors **3000**. The formation of, stacking, and interconnect within and between the three layers may be done by techniques described herein, in the incorporated by reference documents, or any other 3DIC stacking technique that can form vertical interconnects of a density greater than 10,000 vias/cm^2. Partitioning of the overall device between the three layers may, for example, consist of the first layer/substrate of circuits and transistors **3000** including the portion of the overall design wherein the blocks and components do not require the expensive patterning techniques discussed above; and second layer of circuits and transistors **3002** may include a portion of the overall design wherein the blocks and components require the expensive patterning techniques discussed above, and may be aligned in, for example, the 'x' direction, and third layer of circuits and transistors **3004** may include a portion of the overall design wherein the blocks and components require the expensive patterning techniques discussed above, and may be aligned in a direction different from second layer of circuits and transistors **3002**, for example, the 'y' direction (perpendicular to the second layer's pattern). The partitioning constraint discussed above related to process complexity/attainment may be utilized in combination with other partitioning constraints to provide an optimized fit to the design's logic and cost demands. For example, the procedure and algorithm (illustrated in FIG. **239** and related specification found in the referenced patent document) to partition a design into two target technologies may be adapted to also include the constraints and criterion described herein FIG. **30**.

Ion implantation damage repair, and transferred layer annealing, such as activating doping, may utilize carrier wafer liftoff techniques as illustrated in at least FIGS. 184-189 and related specification sections in U.S. Patent Application Publication 2012/0129301 (allowed U.S. patent application Ser. No. 13/273,712), the contents are incorporated herein by reference. High temperature glass carrier substrates/wafers may be utilized, but may locally be structurally damaged or de-bond from the layer being annealed when exposed to LSA (laser spike annealing) or other optical anneal techniques that may locally exceed the softening or outgassing temperature threshold of the glass carrier. An embodiment of the invention is to improve the heat-sinking capability and structural strength of the glass carrier by inserting a layer of a material that may have a greater heat capacity and/or heat spreading capability than glass or fused quartz, and may have an optically reflective property, for example, aluminum, tungsten or forms of carbon such as carbon nanotubes. As illustrated in FIG. **31**, carrier substrate **3199** may include substrate **3100**, heat sink reflector material **3102**, bonding material **3104**, and desired transfer layer **3106**. Substrate **3100** may include, for example, monocrystalline silicon wafers, high temperature glass or fused quartz wafers/substrates, germanium wafers, InP wafers, or high temperature polymer substrates. Substrate **3100** may have a thickness greater than about 50 um, such as 100 um, 1000 um, 1 mm, 2 mm, 5 mm to supply structural integrity for the subsequent processing. Heat sink reflector material **3102** may include material that may have a greater heat capacity and/or heat spreading capability than glass or fused quartz, and may have an optically reflective property, for example, aluminum, tungsten, silicon based silicides, or forms of carbon such as carbon nanotubes. Bonding material **3104** may include silicon oxides, indium tin oxides, fused quartz, high temperature glasses, and other optically transparent to the LSA beam or optical annealing wavelength materials. Bonding material **3104** may have a thickness greater than about 5 nm, such as 10 nm, 20 nm, 100 nm, 200 nm, 300 nm, 500 nm. Desired transfer layer **3106** may include any layer transfer devices and/or layer or layers contained herein this document or the referenced document, for example, the gate-last partial transistor layers, DRAM Si/SiO2 layers, sub-stack layers of circuitry, RCAT doped layers, or starting material doped monocrystalline silicon. Carrier substrate **3199** may be exposed to an optical annealing beam, such as, for example, a laser-spike anneal beam from a commercial semiconductor material oriented single or dual-beam laser spike anneal DB-LSA system of Ultratech Inc., San Jose, Calif., USA or a short pulse laser (such as 160 ns), with 308 nm wavelength, such as offered by Excico of Gennevilliers, France. Optical anneal beam **3108** may locally heat desired transfer layer **3106** to anneal defects and/or activate dopants. The portion of the optical anneal beam **3108** that is not absorbed by desired transfer layer **3106** may pass through bonding material **3104** and be absorbed and or reflected by heat sink reflector material **3102**. This may increase the efficiency of the optical anneal/activation of desired transfer layer **3106**, and may also provide a heat spreading capability so that the temperature of desired transfer layer **3106** and bonding material **3104** locally near the optical anneal beam **3108**, and in the beam's immediate past locations, may not exceed the debond temperature of the bonding material **3104** to desired transfer layer **3106** bond. The annealed and/or activated desired transfer layer **3106** may be layer transferred to an acceptor wafer or substrate, as described, for example, in the referenced patent document FIG. **186**. Substrate **3100**, heat sink reflector material **3102**, and bonding material **3104** may be removed/decoupled from desired transfer layer **3106** by being etched away or removed during the layer transfer process.

A planar fully depleted n-channel Recessed Channel Array Transistor (FD-RCAT) suitable for a monolithic 3D IC may be constructed as follows. The FD-RCAT may provide an improved source and drain contact resistance, thereby allowing for lower channel doping (such as undoped), and the recessed channel may provide for more flexibility in the engineering of channel lengths and transistor characteristics, and increased immunity from process variations. The buried doped layer and channel dopant shaping, even to an un-doped channel, may allow for efficient adaptive and dynamic body biasing to control the transistor threshold and threshold varia-

tions, as well as provide for a fully depleted or deeply depleted transistor channel. Furthermore, the recessed gate allows for an FD transistor but with thicker silicon for improved lateral heat conduction. FIG. **32**A-F illustrates an exemplary n-channel FD-RCAT which may be constructed in a 3D stacked layer using procedures outlined below and in U.S. Patent Application Publication 2012/0129301 (allowed U.S. patent application Ser. No. 13/273,712) and pending U.S. patent application Ser. Nos. 13/441,923 and 13/099,010. The contents of the foregoing applications are incorporated herein by reference.

As illustrated in FIG. **32**A, a P− substrate donor wafer **3200** may be processed to include wafer sized layers of N+ doping **3202**, P− doping **3206**, channel **3203** and P+ doping **3204** across the wafer. The N+ doped layer **3202**, P− doped layer **3206**, channel layer **3203** and P+ doped layer **3204** may be formed by ion implantation and thermal anneal. P− substrate donor wafer **3200** may include a crystalline material, for example, mono-crystalline (single crystal) silicon. P− doped layer **3206** and channel layer **3203** may have additional ion implantation and anneal processing to provide a different dopant level than P− substrate donor wafer **3200**. P− substrate donor wafer **3200** may be very lightly doped (less than 1e15 atoms/cm^3) or nominally un-doped (less than 1e14 atoms/cm^3). P− doped layer **3206**, channel layer **3203**, and P+ doped layer **3204** may have graded or various layers doping to mitigate transistor performance issues, such as, for example, short channel effects, after the FD-RCAT is formed, and to provide effective body biasing, whether adaptive or dynamic. The layer stack may alternatively be formed by successive epitaxially deposited doped silicon layers of N+ doped layer **3202**, P− doped layer **3206**, channel layer **3203** and P+ doped layer **3204**, or by a combination of epitaxy and implantation. Annealing of implants and doping may include, for example, conductive/inductive thermal, optical annealing techniques or types of Rapid Thermal Anneal (RTA or spike). The N+ doped layer **3202** may have a doping concentration that may be more than 10× the doping concentration of P− doped layer **3206** and/or channel layer **3203**. The P+ doped layer **3204** may have a doping concentration that may be more than 10× the doping concentration of P-doped layer **3206** and/or channel layer **3203**. The P− doped layer **3206** may have a doping concentration that may be more than 10× the doping concentration of channel layer **3203**. Channel layer **3203** may have a thickness that may allow fully-depleted channel operation when the FD-RCAT transistor is substantially completely formed, such as, for example, less than 5 nm, less than 10 nm, or less than 20 nm.

As illustrated in FIG. **32**B, the top surface of the P− substrate donor wafer **3200** layer stack may be prepared for oxide wafer bonding with a deposition of an oxide or by thermal oxidation of P+ doped layer **3204** to form oxide layer **3280**. A layer transfer demarcation plane (shown as dashed line) **3299** may be formed by hydrogen implantation or other methods as described in the incorporated references. The P− substrate donor wafer **3200** and acceptor wafer **3210** may be prepared for wafer bonding as previously described and low temperature (less than approximately 400° C.) bonded. Acceptor wafer **3210**, as described in the incorporated references, may include, for example, transistors, circuitry, and metal, such as, for example, aluminum or copper, interconnect wiring, a metal shield/heat sink layer, and thru layer via metal interconnect strips or pads. The portion of the N+ doped layer **3202** and the P− substrate donor wafer **3200** that may be above (when the layer stack is flipped over and bonded to the acceptor wafer) the layer transfer demarcation plane **3299** may be removed by cleaving or other low temperature processes as described in the incorporated references, such as, for example, ion-cut or other layer transfer methods.

As illustrated in FIG. **32**C, oxide layer **3280**, P+ doped layer **3204**, channel layer **3203**, P− doped layer **3206**, and remaining N+ layer **3222** have been layer transferred to acceptor wafer **3210**. The top surface of N+ layer **3222** may be chemically or mechanically polished. Now transistors may be formed with low temperature (less than approximately 400° C. exposure to the acceptor wafer **3210**) processing and aligned to the acceptor wafer alignment marks (not shown) as described in the incorporated references.

As illustrated in FIG. **32**D, the transistor isolation regions **3205** may be formed by mask defining and plasma/RIE etching remaining N+ layer **3222**, P− doped layer **3206**, channel layer **3203**, and P+ doped layer **3204** substantially to the top of oxide layer **3280** (not shown), substantially into oxide layer **3280**, or into a portion of the upper oxide layer of acceptor wafer **3210** (not shown). Additionally, a portion of the transistor isolation regions **3205** may be etched (separate step) substantially to P+ doped layer **3204**, thus allowing multiple transistor regions to be connected by the same P+ doped region **3224**. A low-temperature gap fill oxide may be deposited and chemically mechanically polished, the oxide remaining in isolation regions **3205**. The recessed channel **3286** may be mask defined and etched thru remaining N+ doped layer **3222**, P− doped layer **3206** and partially into channel layer **3203**. The recessed channel surfaces and edges may be smoothed by processes, such as, for example, wet chemical, plasma/RIE etching, low temperature hydrogen plasma, or low temperature oxidation and strip techniques, to mitigate high field effects. The low temperature smoothing process may employ, for example, a plasma produced in a TEL (Tokyo Electron Labs) SPA (Slot Plane Antenna) machine. Thus N+ source and drain regions **3232**, P− regions **3226**, and channel region **3223** may be formed, which may substantially form the transistor body. The doping concentration of N+ source and drain regions **3232** may be more than 10× the concentration of channel region **3223**. The doping concentration of the N− channel region **3223** may include gradients of concentration or layers of differing doping concentrations. The doping concentration of N+ source and drain regions **3232** may be more than 10× the concentration of P− regions **3226**. The etch formation of recessed channel **3286** may define the transistor channel length. The shape of the recessed etch may be rectangular as shown, or may be spherical (generally from wet etching, sometimes called an S-RCAT: spherical RCAT), or a variety of other shapes due to etching methods and shaping from smoothing processes, and may help control for the channel electric field uniformity. The thickness of channel region **3223** in the region below recessed channel **3286** may be of a thickness that allows fully-depleted channel operation. The thickness of channel region **3223** in the region below N+ source and drain regions **3232** may be of a thickness that allows fully-depleted transistor operation.

As illustrated in FIG. **32**E, a gate dielectric **3207** may be formed and a gate metal material may be deposited. The gate dielectric **3207** may be an atomic layer deposited (ALD) gate dielectric that may be paired with a work function specific gate metal in the industry standard high k metal gate process schemes described in the incorporated references. Alternatively, the gate dielectric **3207** may be formed with a low temperature processes including, for example, oxide deposition or low temperature microwave plasma oxidation of the silicon surfaces and a gate material with proper work function and less than approximately 400° C. deposition temperature such as, for example, tungsten or aluminum may be deposited. The gate material may be chemically mechanically pol-

ished, and the gate area defined by masking and etching, thus forming the gate electrode **3208**. The shape of gate electrode **3208** is illustrative, the gate electrode may also overlap a portion of N+ source and drain regions **3232**.

As illustrated in FIG. **32**F, a low temperature thick oxide **3209** may be deposited and planarized, and source, gate, and drain contacts, P+ doped region contact (not shown) and thru layer via (not shown) openings may be masked and etched preparing the transistors to be connected via metallization. P+ doped region contact may be constructed thru isolation regions **3205**, suitably when the isolation regions **3205** is formed to a shared P+ doped region **3224**. Thus gate contact **3211** connects to gate electrode **3208**, and source & drain contacts **3240** connect to N+ source and drain regions **3232**. The thru layer via (not shown) provides electrical coupling among the donor wafer transistors and the acceptor wafer metal connect pads or strips (not shown) as described in the incorporated references.

Persons of ordinary skill in the art will appreciate that the illustrations in FIGS. **32**A through **32**F are exemplary only and are not drawn to scale. Such skilled persons will further appreciate that many variations are possible such as, for example, a p-channel FD-RCAT may be formed with changing the types of dopings appropriately. Moreover, the P− substrate donor wafer **3200** may be n type or un-doped. Further, P− doped channel layer **3203** may include multiple layers of different doping concentrations and gradients to fine tune the eventual FD-RCAT channel for electrical performance and reliability characteristics, such as, for example, off-state leakage current and on-state current. Furthermore, isolation regions **3205** may be formed by a hard mask defined process flow, wherein a hard mask stack, such as, for example, silicon oxide and silicon nitride layers, or silicon oxide and amorphous carbon layers, may be utilized. Moreover, CMOS FD-RCATs may be constructed with n-JLRCATs in a first mono-crystalline silicon layer and p-JLRCATs in a second mono-crystalline layer, which may include different crystalline orientations of the mono-crystalline silicon layers, such as for example, <100>, <111> or <551>, and may include different contact silicides for optimum contact resistance to p or n type source, drains, and gates. Furthermore, P+ doped regions **3224** may be utilized for a double gate structure for the FD-RCAT and may utilize techniques described in the incorporated references. Further, efficient heat removal and transistor body biasing may be accomplished on a FD-RCAT by adding an appropriately doped buried layer (N− in the case of a n-FD-RCAT), forming a buried layer region underneath the P+ doped region **3224** for junction isolation, and connecting that buried region to a thermal and electrical contact, similar to what is described for layer **1606** and region **1646** in FIGS. **16**A-G in the incorporated reference pending U.S. patent application Ser. No. 13/441,923. Many other modifications within the scope of the invention will suggest themselves to such skilled persons after reading this specification. Thus the invention is to be limited only by the appended claims.

Defect annealing, such as furnace thermal or optical annealing, of thin layers of the crystalline materials generally included in 3D-ICs to the temperatures that may lead to substantial dopant activation or defect anneal, for example above 600° C., may damage or melt the underlying metal interconnect layers of the stacked 3D-IC, such as copper or aluminum interconnect layers. An embodiment of the invention is to form 3D-IC structures and devices wherein a heat spreading, heat conducting and/or optically reflecting material layer or layers is incorporated between the sensitive metal interconnect layers and the layer or regions being optically irradiated and annealed, or annealed from the top of the 3D-IC stack using other methods. An exemplary generalized process flow is shown in FIGS. **33**A-F. An exemplary process flow for an FD-RCAT with an integrated heat spreader is shown in FIGS. **34**A-G. The 3D-ICs may be constructed in a 3D stacked layer using procedures outlined in U.S. Patent Application Publication 2012/0129301 (allowed U.S. patent application Ser. No. 13/273,712) and pending U.S. patent application Ser. Nos. 13/441,923 and 13/099,010. The contents of the foregoing applications are incorporated herein by reference. The topside defect anneal may include optical annealing to repair defects in the crystalline 3D-IC layers and regions (which may be caused by the ion-cut implantation process), and may be utilized to activate semiconductor dopants in the crystalline layers or regions of a 3D-IC, such as, for example, LDD, halo, source/drain implants. The 3D-IC may include, for example, stacks formed in a monolithic manner with thin layers or stacks and vertical connection such as TLVs, and stacks formed in an assembly manner with thick (>2 um) layers or stacks and vertical connections such as TSVs. Optical annealing beams or systems, such as, for example, a laser-spike anneal beam from a commercial semiconductor material oriented single or dual-beam continuous wave (CW) laser spike anneal DB-LSA system of Ultratech Inc., San Jose, Calif., USA (10.6 um laser wavelength) or a short pulse laser (such as 160 ns), with 308 nm wavelength, and large area irradiation such as offered by Excico of Gennevilliers, France, may be utilized. Additionally, the defect anneal may include, for example, laser anneals, Rapid Thermal Anneal (RTA), flash anneal, Ultrasound Treatments (UST), megasonic treatments, and/or microwave treatments. The topside defect anneal ambient may include, for example, vacuum, high pressure (greater than about 760 torr), oxidizing atmospheres (such as oxygen or partial pressure oxygen), and/or reducing atmospheres (such as nitrogen or argon). The topside defect anneal may include temperatures of the layer being annealed above about 400° C. (a high temperature thermal anneal), including, for example, 600° C., 800° C., 900° C., 1000° C., 1050° C., 1100° C. and/or 1120° C. The topside defect anneal may include activation of semiconductor dopants, such as, for example, ion implanted dopants or PLAD applied dopants.

As illustrated in FIG. **33**A, a generalized process flow may begin with a donor wafer **3300** that may be preprocessed with wafer sized layers **3302** of conducting, semi-conducting or insulating materials that may be formed by deposition, ion implantation and anneal, oxidation, epitaxial growth, combinations of above, or other semiconductor processing steps and methods. For example, donor wafer **3300** and wafer sized layers **3302** may include semiconductor materials such as, for example, mono-crystalline silicon, germanium, GaAs, InP, and graphene. For this illustration, mono-crystalline (single crystal) silicon may be used. The donor wafer **3300** may be preprocessed with a layer transfer demarcation plane (shown as dashed line) **3399**, such as, for example, a hydrogen implant cleave plane, before or after (typical) wafer sized layers **3302** are formed. Layer transfer demarcation plane **3399** may alternatively be formed within wafer sized layers **3302**. Other layer transfer processes, some described in the referenced patent documents, may alternatively be utilized. Damage/defects to crystalline structure of donor wafer **3300** may be annealed by some of the annealing methods described, for example the short wavelength pulsed laser techniques, wherein the donor wafer **3300** wafer sized layers **3302** and portions of donor wafer **3300** may be heated to defect annealing temperatures, but the layer transfer demarcation plane **3399** may be kept below the temperate for cleav-

ing and/or significant hydrogen diffusion. Dopants in at least a portion of wafer sized layers **3302** may also be electrically activated. Thru the processing, donor wafer **3300** and/or wafer sized layers **3302** could be thinned from its original thickness, and their/its final thickness could be in the range of about 0.01 um to about 50 um, for example, 10 nm, 100 nm, 200 nm, 0.4 um, 1 um, 2 um or Sum. Donor wafer **3300** and wafer sized layers **3302** may include preparatory layers for the formation of transistors such as, for example, MOSFETS, FinFets, FD-RCATs, BJTs, HEMTs, HBTs, or partially processed transistors (for example, the replacement gate process described in the referenced patent documents). Donor wafer **3300** and wafer sized layers **3302** may include the layer transfer devices and/or layer or layers contained herein this document or referenced patent documents, for example, DRAM Si/SiO2 layers, RCAT doped layers, or starting material doped or undoped monocrystalline silicon, or polycrystalline silicon. Donor wafer **3300** and wafer sized layers **3302** may have alignment marks (not shown). Acceptor wafer **3310** may be a preprocessed wafer that may have fully functional circuitry including metal layers (including aluminum or copper metal interconnect layers that may connect acceptor wafer **3310** transistors) or may be a wafer with previously transferred layers, or may be a blank carrier or holder wafer, or other kinds of substrates suitable for layer transfer processing. Acceptor wafer **3310** may have alignment marks **3390** and metal connect pads or strips **3380** and ray blocked metal interconnect **3381**. Acceptor wafer **3310** may include transistors such as, for example, MOSFETS, FinFets, FD-RCATs, BJTs, HEMTs, and/or HBTs. Acceptor wafer **3310** may include shield/heat sink layer **3388**, which may include materials such as, for example, Aluminum, Tungsten, Copper, silicon or cobalt based silicides, or forms of carbon such as carbon nanotubes. Shield/heat sink layer **3388** may have a thickness range of about 50 nm to about 1 mm, for example, 50 nm, 100 nm, 200 nm, 300 nm, 500 nm, 0.1 um, 1 um, 2 um, and 10 um. Shield/heat sink layer **3388** may include isolation openings **3386**, and alignment mark openings **3387**, which may be utilized for short wavelength alignment of top layer (donor) processing to the acceptor wafer alignment marks **3390**. Shield/heat sink layer **3388** may include shield path connect **3385** and shield path via **3383**. Shield path via **3383** may thermally and/or electrically couple and connect shield path connect **3385** to acceptor wafer **3310** interconnect metallization layers such as, for example, metal connect pads or strips **3380** (shown). If two shield/heat sink layers **3388** are utilized, one on top of the other and separated by an isolation layer common in semiconductor BEOL, such as carbon doped silicon oxide, shield path connect **3385** may also thermally and/or electrically couple and connect each shield/heat sink layer **3388** to the other and to acceptor wafer **3310** interconnect metallization layers such as, for example, metal connect pads or strips **3380**, thereby creating a heat conduction path from the shield/heat sink layer **3388** to the acceptor wafer substrate, and a heat sink (shown in FIG. **33**F.).

As illustrated in FIG. **33**B, two exemplary top views of shield/heat sink layer **3388** are shown. In shield/heat sink portion **3320** a shield area **3322** of the shield/heat sink layer **3388** materials described above and in the incorporated references may include TLV/TSV connects **3324** and isolation openings **3386**. Isolation openings **3386** may be the absence of the material of shield area **3322**. TLV/TSV connects **3324** are an example of a shield path connect **3385**. TLV/TSV connects **3324** and isolation openings **3386** may be drawn in the database of the 3D-IC stack and may formed during the acceptor wafer **3310** processing. In shield/heat sink portion **3330** a shield area **3332** of the shield/heat sink layer **3388** materials described above and in the incorporated references may have metal interconnect strips **3334** and isolation openings **3386**. Metal interconnect strips **3334** may be surrounded by regions, such as isolation openings **3386**, where the material of shield area **3332** may be etched away, thereby stopping electrical conduction from metal interconnect strips **3334** to shield area **3332** and to other metal interconnect strips. Metal interconnect strips **3334** may be utilized to connect/couple the transistors formed in the donor wafer layers, such as **3302**, to themselves from the 'backside' or 'underside' and/or to transistors in the acceptor wafer level/layer. Metal interconnect strips **3334** and shield/heat sink layer **3388** regions such as shield area **3322** and shield area **3332** may be utilized as a ground plane for the transistors above it residing in the donor wafer layers.

Bonding surfaces, donor bonding surface **3301** and acceptor bonding surface **3311**, may be prepared for wafer bonding by depositions (such as silicon oxide), polishes, plasma, or wet chemistry treatments to facilitate successful wafer to wafer bonding.

As illustrated in FIG. **33**C, the donor wafer **3300** with wafer sized layers **3302** and layer transfer demarcation plane **3399** may be flipped over, aligned, and bonded to the acceptor wafer **3310**. The donor wafer **3300** with wafer sized layers **3302** may have alignment marks (not shown). Various topside defect anneals may be utilized. For this illustration, an optical beam such as the laser annealing previously described is used. Optical anneal beams may be optimized to focus light absorption and heat generation at or near the layer transfer demarcation plane (shown as dashed line) **3399** to provide a hydrogen bubble cleave with exemplary cleave ray **3351**. The laser assisted hydrogen bubble cleave with the absorbed heat generated by exemplary cleave ray **3351** may also include a pre-heat of the bonded stack to, for example, about 100° C. to about 400° C., and/or a thermal rapid spike to temperatures above about 200° C. to about 600° C. The laser assisted ion-cut cleave may provide a smoother cleave surface upon which better quality transistors may be manufactured. Reflected ray **3353** may be reflected and/or absorbed by shield/heat sink layer **3388** regions thus blocking the optical absorption of ray blocked metal interconnect **3381**. Additionally, shield/heat sink layer **3388** may laterally spread and conduct the heat generated by the topside defect anneal, and in conjunction with the dielectric materials (low heat conductivity) above and below shield/heat sink layer **3388**, keep the interconnect metals and low-k dielectrics of the acceptor wafer interconnect layers cooler than a damage temperature, such as, for example, 400 C. Annealing of dopants or annealing of damage, such as from the H cleave implant damage, may be accomplished by a rays such as repair ray **3355**. A small portion of the optical energy, such as unblocked ray **3357**, may hit and heat, or be reflected, by (a few rays as the area of the heat shield openings, such as **3324**, is small compared to the die or device area) such as metal connect pads or strips **3380**. Heat generated by absorbed photons from, for example, cleave ray **3351**, reflected ray **3353**, and/or repair ray **3355** may also be absorbed by shield/heat sink layer **3388** regions and dissipated laterally and may keep the temperature of underlying metal layers, such as ray blocked metal interconnect **3381**, and other metal layers below it, cooler and prevent damage. Shield/heat sink layer **3388** may act as a heat spreader. A second layer of shield/heat sink layer **3388** (not shown) may have been constructed (during the acceptor wafer **3310** formation) with a low heat conductive material sandwiched between the two heat sink layers, such as silicon oxide or carbon doped 'low-k' silicon oxides, for improved thermal protection of the acceptor wafer interconnect layers,

metal and dielectrics. Electrically conductive materials may be used for the two layers of shield/heat sink layer **3388** and thus may provide, for example, a Vss and a Vdd plane for power delivery that may be connected to the donor layer transistors above, as well may be connected to the acceptor wafer transistors below. Shield/heat sink layer **3388** may include materials with a high thermal conductivity greater than 10 W/m-K, for example, copper (about 400 W/m-K), aluminum (about 237 W/m-K), Tungsten (about 173 W/m-K), Plasma Enhanced Chemical Vapor Deposited Diamond Like Carbon-PECVD DLC (about 1000 W/m-K), and Chemical Vapor Deposited (CVD) graphene (about 5000 W/m-K). Shield/heat sink layer **3388** may be sandwiched and/or substantially enclosed by materials with a low thermal conductivity less than 10 W/m-K, for example, silicon dioxide (about 1.4 W/m-K). The sandwiching of high and low thermal conductivity materials in layers, such as shield/heat sink layer **3388** and under & overlying dielectric layers, spreads the localized heat/light energy of the topside anneal laterally and protect the underlying layers of interconnect metallization & dielectrics, such as in the acceptor wafer, from harmful temperatures or damage.

As illustrated in FIG. **33**D, the donor wafer **3300** may be cleaved at or thinned to (or past, not shown) the layer transfer demarcation plane **3399**, leaving donor wafer portion **3303** and the pre-processed layers **3302** bonded to the acceptor wafer **3310**, by methods such as, for example, ion-cut or other layer transfer methods. The layer transfer demarcation plane **3399** may instead be placed in the pre-processed layers **3302**. Optical anneal beams may be optimized to focus light absorption and heat generation within or at the surface of donor wafer portion **3303** and provide surface smoothing and/or defect annealing (defects may be from the cleave and/or the ion-cut implantation) with exemplary smoothing/annealing ray **3366**. The laser assisted smoothing/annealing with the absorbed heat generated by exemplary smoothing/annealing ray **3366** may also include a pre-heat of the bonded stack to, for example, about 100° C. to about 400° C., and/or a thermal rapid spike to temperatures above about 200° C. to about 600° C. Reflected ray **3363** may be reflected and/or absorbed by shield/heat sink layer **3388** regions thus blocking the optical absorption of ray blocked metal interconnect **3381**. Annealing of dopants or annealing of damage, such as from the H cleave implant damage, may be also accomplished by a set of rays such as repair ray **3365**. A small portion of the optical energy, such as unblocked ray **3367**, may hit and heat, or be reflected, by a few rays (as the area of the heat shield openings, such as **3324**, is small) such as metal connect pads or strips **3380**. Heat generated by absorbed photons from, for example, smoothing/annealing ray **3366**, reflected ray **3363**, and/or repair ray **3365** may also be absorbed by shield/heat sink layer **3388** regions and dissipated laterally and may keep the temperature of underlying metal layers, such as ray blocked metal interconnect **3381**, and other metal layers below it, cooler and prevent damage. A second layer of shield/heat sink layer **3388** may be constructed with a low heat conductive material sandwiched between the two heat sink layers, such as silicon oxide or carbon doped 'low-k' silicon oxides, for improved thermal protection of the acceptor wafer interconnect layers, metal and dielectrics. Shield/heat sink layer **3388** may act as a heat spreader. Electrically conductive materials may be used for the two layers of shield/heat sink layer **3388** and thus may provide, for example, a Vss and a Vdd plane that may be connected to the donor layer transistors above, as well may be connected to the acceptor wafer transistors below.

As illustrated in FIG. **33**E, the remaining donor wafer portion **3303** may be removed by polishing or etching and the transferred layers **3302** may be further processed to create second device layer **3305** which may include donor wafer device structures **3350** and metal interconnect layers (such as second device layer metal interconnect **3361**) that may be precisely aligned to the acceptor wafer alignment marks **3390**. Donor wafer device structures **3350** may include, for example, CMOS transistors such as N type and P type transistors, or any of the other transistor or device types discussed herein this document or referenced patent documents. Second device layer metal interconnect **3361** may include electrically conductive materials such as copper, aluminum, conductive forms of carbon, and tungsten. Donor wafer device structures **3350** may utilize second device layer metal interconnect **3361** and thru layer vias (TLVs) **3360** to electrically couple (connection paths) the donor wafer device structures **3350** to the acceptor wafer metal connect pads or strips **3380**, and thus couple donor wafer device structures (the second layer transistors) with acceptor wafer device structures (first layer transistors). Thermal TLVs **3362** may be constructed of thermally conductive but not electrically conductive materials, for example, DLC (Diamond Like Carbon), and may connect donor wafer device structures **3350** thermally to shield/heat sink layer **3388**. TLVs **3360** may be constructed out of electrically and thermally conductive materials, such as Tungsten, Copper, or aluminum, and may provide a thermal and electrical connection path from donor wafer device structures **3350** to shield/heat sink layer **3388**, which may be a ground or Vdd plane in the design/layout. TLVs **3360** and thermal TLVs **3362** may be also constructed in the device scribelanes (predesigned in base layers or potential dicelines) to provide thermal conduction to the heat sink, and may be sawed/diced off when the wafer is diced for packaging. Shield/heat sink layer **3388** may be configured to act as an emf (electro-motive force) shield to prevent direct layer to layer cross-talk between transistors in the donor wafer layer and transistors in the acceptor wafer. In addition to static ground or Vdd biasing, shield/heat sink layer **3388** may be actively biased with an anti-interference signal from circuitry residing on, for example, a layer of the 3D-IC or off chip. TLVs **3360** may be formed through the transferred layers **3302**. As the transferred layers **3302** may be thin, on the order of about 200 nm or less in thickness, the TLVs may be easily manufactured as a typical metal to metal via may be, and said TLV may have state of the art diameters such as nanometers or tens to a few hundreds of nanometers, such as, for example about 150 nm or about 100 nm or about 50 nm. The thinner the transferred layers **3302**, the smaller the thru layer via diameter obtainable, which may result from maintaining manufacturable via aspect ratios. Thus, the transferred layers **3302** (and hence, TLVs **3360**) may be, for example, less than about 2 microns thick, less than about 1 micron thick, less than about 0.4 microns thick, less than about 200 nm thick, less than about 150 nm thick, or less than about 100 nm thick. The thickness of the layer or layers transferred according to some embodiments of the invention may be designed as such to match and enable the most suitable obtainable lithographic resolution, such as, for example, less than about 10 nm, 14 nm, 22 nm or 28 nm linewidth resolution and alignment capability, such as, for example, less than about 5 nm, 10 nm, 20 nm, or 40 nm alignment accuracy/precision/error, of the manufacturing process employed to create the thru layer vias or any other structures on the transferred layer or layers. Transferred layers **3302** may be considered to be overlying the metal layer or layers of acceptor wafer **3310**. Alignment marks in acceptor wafer **3310** and/or in transferred layers **3302** may be utilized

to enable reliable contact to transistors and circuitry in transferred layers **3302** and donor wafer device structures **3350** and electrically couple them to the transistors and circuitry in the acceptor wafer **3310**. The donor wafer **3300** may now also be processed, such as smoothing and annealing, and reused for additional layer transfers.

As illustrated in FIG. **33**F, a thermal conduction path may be constructed from the devices in the upper layer, the transferred donor layer and formed transistors, to the acceptor wafer substrate and associated heat sink. The thermal conduction path from the donor wafer device structures **3350** to the acceptor wafer heat sink **3397** may include second device layer metal interconnect **3361**, TLVs **3360**, shield path connect **3385**, shield path via **3383**, metal connect pads or strips **3380**, first (acceptor) layer metal interconnect **3391**, acceptor wafer transistors and devices **3393**, and acceptor substrate **3395**. The elements of the thermal conduction path may include materials that have a thermal conductivity greater than 10 W/m-K, for example, copper (about 400 W/m-K), aluminum (about 237 W/m-K), and Tungsten (about 173 W/m-K). The acceptor wafer interconnects may be substantially surrounded by BEOL dielectric **3396**.

A planar fully depleted n-channel Recessed Channel Array Transistor (FD-RCAT) with an integrated shield/heat sink layer suitable for a monolithic 3D IC may be constructed as follows. The FD-RCAT may provide an improved source and drain contact resistance, thereby allowing for lower channel doping (such as undoped), and the recessed channel may provide for more flexibility in the engineering of channel lengths and transistor characteristics, and increased immunity from process variations. The buried doped layer and channel dopant shaping, even to an un-doped channel, may allow for efficient adaptive and dynamic body biasing to control the transistor threshold and threshold variations, as well as provide for a fully depleted or deeply depleted transistor channel. Furthermore, the recessed gate allows for an FD transistor but with thicker silicon for improved lateral heat conduction. Moreover, a heat spreading, heat conducting and/or optically reflecting material layer or layers may be incorporated between the sensitive metal interconnect layers and the layer or regions being optically irradiated and annealed to repair defects in the crystalline 3D-IC layers and regions and to activate semiconductor dopants in the crystalline layers or regions of a 3D-IC without harm to the sensitive metal interconnect and associated dielectrics. FIG. **34**A-G illustrates an exemplary n-channel FD-RCAT which may be constructed in a 3D stacked layer using procedures outlined below and in U.S. Patent Application Publication 2012/0129301 (allowed U.S. patent application Ser. No. 13/273,712) and pending U.S. patent application Ser. Nos. 13/441,923 and 13/099,010. The contents of the foregoing applications are incorporated herein by reference.

As illustrated in FIG. **34**A, a P− substrate donor wafer **3400** may be processed to include wafer sized layers of N+ doping **3402**, P− doping **3406**, channel **3403** and P+ doping **3404** across the wafer. The N+ doped layer **3402**, P− doped layer **3406**, channel layer **3403** and P+ doped layer **3404** may be formed by ion implantation and thermal anneal. P− substrate donor wafer **3400** may include a crystalline material, for example, mono-crystalline (single crystal) silicon. P− doped layer **3406** and channel layer **3403** may have additional ion implantation and anneal processing to provide a different dopant level than P− substrate donor wafer **3400**. P− substrate donor wafer **3400** may be very lightly doped (less than 1e15 atoms/cm^3) or nominally un-doped (less than 1e14 atoms/cm^3). P− doped layer **3406**, channel layer **3403**, and P+ doped layer **3404** may have graded or various layers doping to mitigate transistor performance issues, such as, for example, short channel effects, after the FD-RCAT is formed, and to provide effective body biasing, whether adaptive or dynamic. The layer stack may alternatively be formed by successive epitaxially deposited doped silicon layers of N+ doped layer **3402**, P− doped layer **3406**, channel layer **3403** and P+ doped layer **3404**, or by a combination of epitaxy and implantation, or by layer transfer. Annealing of implants and doping may include, for example, conductive/inductive thermal, optical annealing techniques or types of Rapid Thermal Anneal (RTA or spike). The N+ doped layer **3402** may have a doping concentration that may be more than 10× the doping concentration of P− doped layer **3406** and/or channel layer **3403**. The P+ doped layer **3404** may have a doping concentration that may be more than 10× the doping concentration of P− doped layer **3406** and/or channel layer **3403**. The P− doped layer **3406** may have a doping concentration that may be more than 10× the doping concentration of channel layer **3403**. Channel layer **3403** may have a thickness that may allow fully-depleted channel operation when the FD-RCAT transistor is substantially completely formed, such as, for example, less than 5 nm, less than 10 nm, or less than 20 nm.

As illustrated in FIG. **34**B, the top surface of the P− substrate donor wafer **3400** layer stack may be prepared for oxide wafer bonding with a deposition of an oxide or by thermal oxidation of P+ doped layer **3404** to form oxide layer **3480**. A layer transfer demarcation plane (shown as dashed line) **3499** may be formed by hydrogen implantation or other methods as described in the incorporated references. The P− substrate donor wafer **3400** and acceptor wafer **3410** may be prepared for wafer bonding as previously described and low temperature (less than approximately 400° C.) bonded. Acceptor wafer **3410**, as described in the incorporated references, may include, for example, transistors, circuitry, and metal, such as, for example, aluminum or copper, interconnect wiring, a metal shield/heat sink layer, and thru layer via metal interconnect strips or pads. Acceptor wafer **3410** may include transistors such as, for example, MOSFETS, FinFets, FD-RCATs, BJTs, HEMTs, and/or HBTs. The portion of the N+ doped layer **3402** and the P− substrate donor wafer **3400** that may be above (when the layer stack is flipped over and bonded to the acceptor wafer) the layer transfer demarcation plane **3499** may be removed by cleaving or other low temperature processes as described in the incorporated references, such as, for example, ion-cut or other layer transfer methods. Damage/defects to crystalline structure of N+ doped layer **3402**, P− doped layer **3406**, channel layer **3403** and P+ doped layer **3404** may be annealed by some of the annealing methods described, for example the short wavelength pulsed laser techniques, wherein the N+ doped layer **3402**, P− doped layer **3406**, channel layer **3403** and P+ doped layer **3404** or portions of them may be heated to defect annealing temperatures, but the layer transfer demarcation plane **3499** may be kept below the temperate for cleaving and/or significant hydrogen diffusion. The optical energy may be deposited in the upper layer of the stack, for example in P+ doped layer **3404**, and annealing of the other layer may take place via heat diffusion. Dopants in at least a portion of N+ doped layer **3402**, P− doped layer **3406**, channel layer **3403** and P+ doped layer **3404** may also be electrically activated by the anneal.

As illustrated in FIG. **34**C, oxide layer **3480**, P+ doped layer **3404**, channel layer **3403**, P− doped layer **3406**, and remaining N+ layer **3422** have been layer transferred to acceptor wafer **3410**. The top surface of N+ layer **3422** may be chemically or mechanically polished. Thru the processing, the wafer sized layers such as N+ layer **3422** P+ doped layer

3404, channel layer 3403, and P− doped layer 3406, could be thinned from its original total thickness, and their/its final total thickness could be in the range of about 0.01 um to about 50 um, for example, 10 nm, 100 nm, 200 nm, 0.4 um, 1 um, 2 um or 5 um. Acceptor wafer 3410 may include one or more (two are shown in this example) shield/heat sink layers 3488, which may include materials such as, for example, Aluminum, Tungsten, Copper, silicon or cobalt based silicides, or forms of carbon such as carbon nanotubes. Each shield/heat sink layer 3488 may have a thickness range of about 50 nm to about 1 mm, for example, 50 nm, 100 nm, 200 nm, 300 nm, 500 nm, 0.1 um, 1 um, 2 um, and 10 um. Shield/heat sink layer 3488 may include isolation openings 3487, and alignment mark openings (not shown), which may be utilized for short wavelength alignment of top layer (donor) processing to the acceptor wafer alignment marks (not shown). Shield/heat sink layer 3488 may include one or more shield path connect 3485 and shield path via 3483. Shield path via 3483 may thermally and/or electrically couple and connect shield path connect 3485 to acceptor wafer 3410 interconnect metallization layers such as, for example, acceptor metal interconnect 3481 (shown). Shield path connect 3485 may also thermally and/or electrically couple and connect each shield/heat sink layer 3488 to the other and to acceptor wafer 3410 interconnect metallization layers such as, for example, acceptor metal interconnect 3481, thereby creating a heat conduction path from the shield/heat sink layer 3488 to the acceptor substrate 3495, and a heat sink (shown in FIG. 34G.). Isolation openings 3486 may include dielectric materials, similar to those of BEOL isolation 3496. Acceptor wafer 3410 may include first (acceptor) layer metal interconnect 3491, acceptor wafer transistors and devices 3493, and acceptor substrate 3495. Various topside defect anneals may be utilized. For this illustration, an optical beam such as the laser annealing previously described is used. Optical anneal beams may be optimized to focus light absorption and heat generation within or at the surface of N+ layer 3422 and provide surface smoothing and/or defect annealing (defects may be from the cleave and/or the ion-cut implantation) with exemplary smoothing/annealing ray 3466. The laser assisted smoothing/annealing with the absorbed heat generated by exemplary smoothing/annealing ray 3466 may also include a pre-heat of the bonded stack to, for example, about 100° C. to about 400° C., and/or a rapid thermal spike to temperatures above about 200° C. to about 600° C. Reflected ray 3463 may be reflected and/or absorbed by shield/heat sink layer 3488 regions thus blocking the optical absorption of ray blocked metal interconnect 3481. Annealing of dopants or annealing of damage, such as from the H cleave implant damage, may be also accomplished by a set of rays such as repair ray 3465. Heat generated by absorbed photons from, for example, smoothing/annealing ray 3466, reflected ray 3463, and/or repair ray 3465 may also be absorbed by shield/heat sink layer 3488 regions and dissipated laterally and may keep the temperature of underlying metal layers, such as metal interconnect 3481, and other metal layers below it, cooler and prevent damage. Shield/heat sink layer 3488 and associated dielectrics may laterally spread and conduct the heat generated by the topside defect anneal, and in conjunction with the dielectric materials (low heat conductivity) above and below shield/heat sink layer 3488, keep the interconnect metals and low-k dielectrics of the acceptor wafer interconnect layers cooler than a damage temperature, such as, for example, 400° C. A second layer of shield/heat sink layer 3488 may be constructed (shown) with a low heat conductive material sandwiched between the two heat sink layers, such as silicon oxide or carbon doped 'low-k' silicon oxides, for improved thermal protection of the acceptor wafer interconnect layers, metal and dielectrics. Shield/heat sink layer 3488 may act as a heat spreader. Electrically conductive materials may be used for the two layers of shield/heat sink layer 3488 and thus may provide, for example, a Vss and a Vdd plane that may be connected to the donor layer transistors above, as well may be connected to the acceptor wafer transistors below. Shield/heat sink layer 3488 may include materials with a high thermal conductivity greater than 10 W/m-K, for example, copper (about 400 W/m-K), aluminum (about 237 W/m-K), Tungsten (about 173 W/m-K), Plasma Enhanced Chemical Vapor Deposited Diamond Like Carbon-PECVD DLC (about 1000 W/m-K), and Chemical Vapor Deposited (CVD) graphene (about 5000 W/m-K). Shield/heat sink layer 3488 may be sandwiched and/or substantially enclosed by materials with a low thermal conductivity (less than 10 W/m-K), for example, silicon dioxide (about 1.4 W/m-K). The sandwiching of high and low thermal conductivity materials in layers, such as shield/heat sink layer 3488 and under & overlying dielectric layers, spreads the localized heat/light energy of the topside anneal laterally and protect the underlying layers of interconnect metallization & dielectrics, such as in the acceptor wafer, from harmful temperatures or damage. Now transistors may be formed with low temperature (less than approximately 400° C. exposure to the acceptor wafer 3410) processing, and may be aligned to the acceptor wafer alignment marks (not shown) as described in the incorporated references. The donor wafer 3400 may now also be processed, such as smoothing and annealing, and reused for additional layer transfers.

As illustrated in FIG. 34D, transistor isolation regions 3405 may be formed by mask defining and plasma/RIE etching remaining N+ layer 3422, P− doped layer 3406, channel layer 3403, and P+ doped layer 3404 substantially to the top of oxide layer 3480 (not shown), substantially into oxide layer 3480, or into a portion of the upper oxide layer of acceptor wafer 3410 (not shown). Additionally, a portion of the transistor isolation regions 3405 may be etched (separate step) substantially to P+ doped layer 3404, thus allowing multiple transistor regions to be connected by the same P+ doped region 3424. A low-temperature gap fill oxide may be deposited and chemically mechanically polished, the oxide remaining in isolation regions 3405. The recessed channel 3486 may be mask defined and etched thru remaining N+ doped layer 3422, P− doped layer 3406 and partially into channel layer 3403. The recessed channel surfaces and edges may be smoothed by processes, such as, for example, wet chemical, plasma/RIE etching, low temperature hydrogen plasma, or low temperature oxidation and strip techniques, to mitigate high field effects. The low temperature smoothing process may employ, for example, a plasma produced in a TEL (Tokyo Electron Labs) SPA (Slot Plane Antenna) machine. Thus N+ source and drain regions 3432, P− regions 3426, and channel region 3423 may be formed, which may substantially form the transistor body. The doping concentration of N+ source and drain regions 3432 may be more than 10× the concentration of channel region 3423. The doping concentration of the N− channel region 3423 may include gradients of concentration or layers of differing doping concentrations. The doping concentration of N+ source and drain regions 3432 may be more than 10× the concentration of P− regions 3426. The etch formation of recessed channel 3486 may define the transistor channel length. The shape of the recessed etch may be rectangular as shown, or may be spherical (generally from wet etching, sometimes called an S-RCAT: spherical RCAT), or a variety of other shapes due to etching methods and shaping from smoothing processes, and

may help control for the channel electric field uniformity. The thickness of channel region **3423** in the region below recessed channel **3486** may be of a thickness that allows fully-depleted channel operation. The thickness of channel region **3423** in the region below N+ source and drain regions **3432** may be of a thickness that allows fully-depleted transistor operation.

As illustrated in FIG. **34**E, a gate dielectric **3407** may be formed and a gate metal material may be deposited. The gate dielectric **3407** may be an atomic layer deposited (ALD) gate dielectric that may be paired with a work function specific gate metal in the industry standard high k metal gate process schemes described in the incorporated references. Alternatively, the gate dielectric **3407** may be formed with a low temperature processes including, for example, oxide deposition or low temperature microwave plasma oxidation of the silicon surfaces and a gate material with proper work function and less than approximately 400° C. deposition temperature such as, for example, tungsten or aluminum may be deposited. The gate material may be chemically mechanically polished, and the gate area defined by masking and etching, thus forming the gate electrode **3408**. The shape of gate electrode **3408** is illustrative, the gate electrode may also overlap a portion of N+ source and drain regions **3432**.

As illustrated in FIG. **34**F, a low temperature thick oxide **3409** may be deposited and planarized, and source, gate, and drain contacts, P+ doped region contact (not shown) and thru layer via (not shown) openings may be masked and etched preparing the transistors to be connected via metallization. P+ doped region contact may be constructed thru isolation regions **3405**, suitably when the isolation regions **3405** is formed to a shared P+ doped region **3424**. Thus gate contact **3411** connects to gate electrode **3408**, and source & drain contacts **3440** connect to N+ source and drain regions **3432**.

As illustrated in FIG. **34**G, thru layer vias (TLVs) **3460** may be formed by etching thick oxide **3409**, gate dielectric **3407**, isolation regions **3405**, oxide layer **3480**, into a portion of the upper oxide layer BEOL isolation **3496** of acceptor wafer **3410** BEOL, and filling with an electrically and thermally conducting material or an electrically non-conducting but thermally conducting material. Second device layer metal interconnect **3461** may be formed by conventional processing. TLVs **3460** may be constructed of thermally conductive but not electrically conductive materials, for example, DLC (Diamond Like Carbon), and may connect the FD-RCAT transistor device and other devices on the top (second) crystalline layer thermally to shield/heat sink layer **3488**. TLVs **3460** may be constructed out of electrically and thermally conductive materials, such as Tungsten, Copper, or aluminum, and may provide a thermal and electrical connection path from the FD-RCAT transistor device and other devices on the top (second) crystalline layer to shield/heat sink layer **3488**, which may be a ground or Vdd plane in the design/layout. TLVs **3460** may be also constructed in the device scribelanes (pre-designed in base layers or potential dicelines) to provide thermal conduction to the heat sink, and may be sawed/diced off when the wafer is diced for packaging not shown). Shield/heat sink layer **3488** may be configured to act (or adapted to act) as an emf (electro-motive force) shield to prevent direct layer to layer cross-talk between transistors in the donor wafer layer and transistors in the acceptor wafer. In addition to static ground or Vdd biasing, shield/heat sink layer **3488** may be actively biased with an anti-interference signal from circuitry residing on, for example, a layer of the 3D-IC or off chip. A thermal conduction path may be constructed from the devices in the upper layer, the transferred donor layer and formed transistors, to the acceptor wafer substrate and associated heat sink. The thermal conduction path from the FD-RCAT transistor device and other devices on the top (second) crystalline layer, for example, N+ source and drain regions **3432**, to the acceptor wafer heat sink **3497** may include source & drain contacts **3440**, second device layer metal interconnect **3461**, TLV **3460**, shield path connect **3485** (shown as twice), shield path via **3483** (shown as twice), metal interconnect **3481**, first (acceptor) layer metal interconnect **3491**, acceptor wafer transistors and devices **3493**, and acceptor substrate **3495**. The elements of the thermal conduction path may include materials that have a thermal conductivity greater than 10 W/m-K, for example, copper (about 400 W/m-K), aluminum (about 237 W/m-K), and Tungsten (about 173 W/m-K).

Persons of ordinary skill in the art will appreciate that the illustrations in FIGS. **34**A through **34**G are exemplary only and are not drawn to scale. Such skilled persons will further appreciate that many variations are possible such as, for example, a p-channel FD-RCAT may be formed with changing the types of dopings appropriately. Moreover, the P− substrate donor wafer **3400** may be n type or un-doped. Further, P− doped channel layer **3403** may include multiple layers of different doping concentrations and gradients to fine tune the eventual FD-RCAT channel for electrical performance and reliability characteristics, such as, for example, off-state leakage current and on-state current. Furthermore, isolation regions **3405** may be formed by a hard mask defined process flow, wherein a hard mask stack, such as, for example, silicon oxide and silicon nitride layers, or silicon oxide and amorphous carbon layers, may be utilized. Moreover, CMOS FD-RCATs may be constructed with n-JLRCATs in a first mono-crystalline silicon layer and p-JLRCATs in a second mono-crystalline layer, which may include different crystalline orientations of the mono-crystalline silicon layers, such as for example, <100>, <111> or <551>, and may include different contact silicides for optimum contact resistance to p or n type source, drains, and gates. Furthermore, P+ doped regions **3424** may be utilized for a double gate structure for the FD-RCAT and may utilize techniques described in the incorporated references. Further, efficient heat removal and transistor body biasing may be accomplished on a FD-RCAT by adding an appropriately doped buried layer (N− in the case of a n-FD-RCAT), forming a buried layer region underneath the P+ doped regions **3424** for junction isolation, and connecting that buried region to a thermal and electrical contact, similar to what is described for layer **1606** and region **1646** in FIGS. **16**A-G in the incorporated reference pending U.S. patent application Ser. No. 13/441,923. Implants after the formation of the isolation regions **3405** may be annealed by optical (such as pulsed laser) means as previously described and the acceptor wafer metallization may be protected by the shield/heat sink layer **3488**. Many other modifications within the scope of the invention will suggest themselves to such skilled persons after reading this specification. Thus the invention is to be limited only by the appended claims.

The ion-cut implant that forms the layer transfer demarcation plane in the donor wafer in many of the 3D stacked layer procedures outlined herein and in U.S. Patent Application Publication 2012/0129301 (allowed U.S. patent application Ser. No. 13/273,712) and pending U.S. patent application Ser. Nos. 13/441,923 and 13/099,010, the contents of the foregoing applications are incorporated herein by reference, is implanted into a doped layer or region. This now allows the ion-cut process to take advantage of the co-implantation effect, wherein the effect of ion-cut species, generally hydrogen, is enhanced die to the presence of another dopant and/or that dopant's damage creation, for example, boron, in the crystalline silicon. This may allow a lower temperature cleav-

ing, for example, under about 400° C. and under about 250° C., may allow the use of a lower ion-cut species dose (and the resultant lower cost process), and may allow a smoother cleave. Two of the papers on the co-implantation topic are Tong, Q.-Y., et al., "Low Temperature Si Layer Splitting", Proceedings 1997 IEEE International SOI Conference, October 1997, pp. 126-127 and Ma, X., et al., "A high-quality SOI structure fabricated by low-temperature technology with B+/H+co-implantation and plasma bonding", Semiconductor Science and Technology, Vol., 21, 2006, pp. 959-963.

As illustrated in FIG. **35**, a P− substrate donor wafer **3500** may be processed to include wafer sized layers of P+ doping **3502**, and N− doping **3503** across the wafer, or in regions across the wafer (not shown). The P+ doped layer **3502** may be formed by ion implantation and thermal anneal. N− doped layer **3503** may have additional ion implantation and anneal processing to provide a different dopant level than P− substrate donor wafer **3500**. N− doped layer **3503** and P+ doped layer **3502** may have graded or various layers of N− doping. The layer stack may alternatively be formed by successive epitaxially deposited doped silicon layers of P+ **3502** and N− **3503**, or by a combination of epitaxy and implantation. Annealing of implants and doping may include, for example, conductive/inductive thermal, optical annealing techniques or types of Rapid Thermal Anneal (RTA or spike). The P+ doped layer **3502** may have a doping concentration that may be more than 10× the doping concentration of N− doped layer **3503**. N− doped layer **3503** may have a thickness that may allow fully-depleted channel operation. The types of doping of P− substrate donor wafer **3500**, N− doped layer **3503**, and P+ doped layer **3502** may be changed according to the type, such an n-channel or p-channel, of transistor desired. P− substrate donor wafer **3500** and/or N− doped layer **3503** may be undoped. There may also be more layers or regions formed, such as, for example, as shown herein this document for the FD-RCAT. The top surface of P− substrate donor wafer **3500** may be prepared for oxide wafer bonding with a deposition of an oxide or by thermal oxidation of N− doped layer **3503** to form oxide layer **3580**. A layer transfer demarcation plane (shown as dashed line) **3599** may be formed by hydrogen implantation or other methods as described in the incorporated references. Layer transfer demarcation plane **3599** may be formed within or close to P+ doped layer **3502** to take advantage of the co-implantation effect.

Various methods and procedures to form Finfet transistors and thin-side-up transistors, many as part of a 3D stacked layer formation, are outlined herein and in U.S. Patent Application Publication 2012/0129301 (allowed U.S. patent application Ser. No. 13/273,712) (at least in FIGS. 58, 146, 220 and associated specification paragraphs) and pending U.S. patent application Ser. Nos. 13/441,923 and 13/099,010, the contents of the foregoing applications are incorporated herein by reference. An embodiment of the invention is to modify the finfet/thin-side-up transistor formation process wherein multiple regions of differing fin thickness are formed, thus allowing multiple Vt finfet transistors on the same circuit, device, die or substrate. Threshold voltage dependence of fin height has been described in Pei, G., et al., *IEEE Transactions on Electron Devices*, vol. 49, no. 8, p. 1411-1419 (2002).

As illustrated in FIG. **36**, the crystalline fins, for example, monocrystalline silicon fins, made be formed by conventional lithography (spacer enabled) and etch, forming a multiplicity of tall fins **3690** on substrate **3604**. Substrate **3604** may be a bulk crystalline substrate or wafer, such as monocrystalline silicon, doped or undoped, or substrate **3604** may be and SOI wafer (Silicon On Insulator). Tall fins **3690** may have a fin height **3691**, which may be in a range from about 3 nm to about 300 nm. Short fins **3680** may be formed by protecting the desired at end-of-process tall fins **3690**, lithographically exposing the tall fins **3690** that are desired to become short fins **3680**, and partially etching (by plasma, RIE, or wet etching) the crystalline material of the exposed tall fins **3690**. An approach may be to deposit a filling material (not shown), such as an oxide, covering tall fins **3690**, and planarize (with CMP or like processes). The planarized level may be above the top of the tall fins **3690**, or just at the top level exposing the tops of tall fins **3690**, or below the top of tall fins **3690**. Lithography processes (may have hard masks employed as well) may be utilized to cover the desired at end-of-process tall fins **3690** and exposing the tall fins **3690** that are desired to become short fins **3680**, and partially etching (by plasma, RIE, or wet etching) the crystalline material of the exposed tall fins **3690**, thus resulting in short fins **3680** of short fin height **3681**, which may be in a range from about 3 nm to about 300 nm. Short fin height **3681** may be less than fin height **3691**, typically by at least 10% of fin height **3691**. The filling material may be fully or partially removed, and the conventional finfet processing may continue.

With reference to at least FIG. 70B-1 and associated specification descriptions in U.S. Patent Application Publication 2012/0129301 (allowed U.S. patent application Ser. No. 13/273,712, the contents of the foregoing applications are incorporated herein by reference, an ion-implant may be screened from regions on a chip. For example, this may be applied to the ion-cut implant may be used to form the layer transfer demarcation plane and form various 3D structures as described herein this document and the referenced applications incorporated. As illustrated in FIG. **37**, the implant of an atomic species **3710** (illustrated as arrows), such as, for example, H+, may be screened from the sensitive gate areas **3703**, which may include gate dielectrics and gate metals, by first masking and etching a shield implant stopping layer of a dense material **3750**, for example about 5000 angstroms of Tantalum, and may be combined with about 5,000 angstroms of photoresist **3752**. The ion implant screen may also be formed by a thick layer of photoresist, for example, about 3 microns of KTI 950K PMMA and Shipley 1400-30 as described in Yun, C. H., et al., "Transfer of patterned ion-cut silicon layers", *Applied Physics Letters*, vol. 73, no. 19, p. 2772-2774 (November 2008). Various materials and thicknesses could be utilized for the defined screen layer dense material **3752** and photoresist **3752** to effectively screen the implant from harming the underlying structures. In general, the higher the atomic weight and denser the material, the more effective implant screening that can be obtained for a given thickness of the material. The implant of an atomic species **3710** may create a segmented cleave plane **3712** in the bulk (or other layers) of the donor substrate **3700**, for example, a monocrystalline silicon wafer. Thus, ion masked region **3713** may be formed. The source and drain of a transistor structure may also be protected from the implant of an atomic species **3710** by the dense material **3752***a* and photoresist **3752***a*, thus ion masked region **3713***a* may be formed. Ion masked regions **3713***a* may be combined by merging the regions of dense material **3752***a* and photoresist **3752***a* to create large regions of ion masked regions. The large regions of ion-masking could be, for example, in the range of 100× 100 nm and even greater than 4 um by 4 um, and may protect a multiplicity of transistors at a time. Many top-viewed shapes and sizes of the ion-masked and ion-implanted regions may be utilized. After cleaving, additional polishing may be applied to provide a smooth bonding surface for layer transfer suitability. To mitigate the inclined ion profile after implant from the sloping edge of the photoresist, photoresist **3752**

could be removed prior to the implant and the thickness of dense material **3752** may be adjusted appropriately to substantially block the implant.

It is desirable to tightly integrate compound semiconductor (CS) devices, such as GaN HBTs, InP HEMTs, etc. with silicon based CMOS devices; substantially all formed monolithically (2D or 3D) on the same die and in close proximity to each other (a few microns, etc.). One approach to doing so is to manufacture a hybrid substrate that can be processed to form CS and silicon (Si) based CMOS transistors wherein the hybrid substrate may have high quality and close proximity silicon and CS regions and high quality surfaces. One of the approaches to generating this CS/Si hybrid substrate is to take a monocrystalline silicon wafer (bulk or SOI), etch holes entirely thru the thickness of the monocrystalline silicon wafer, such as TSVs, oxidize to form a thin layer of silicon dioxide, attach the TSV'd monocrystalline silicon wafer to one or more CS template wafers or portions (generally a substantially pure crystalline CS so to provide a perfect epi template), and grow high quality CS epi in the TSV hole, generally via LPE (Liquid Phase Epitaxy) or MOCVD (Metal-Organic Chemical Vapor Deposition) techniques. The TSVs may have many possible sidewall angles with respect to the top surface of the monocrystalline silicon wafer, such as, for example, at about a 90 degree angle or about a 45 degree angle. Generally, the TSV'd silicon substrate may be thinner than the standard thickness-for-wafer-diameter standard (to enable good epitaxial growth quality, rates and efficiencies), and as such, may not be acceptable for standard conventional transistor processing in a production wafer fabrication facility. As well, reuse of the CS/Si hybrid wafer may be desired, as it may generate multiple usable thin layers for processing hybrid (heterogeneous) circuits and devices. It may be desirable to ion-cut a thin layer of the CS/Si hybrid substrate and layer transfer this thin layer (about 5 nm to 1000 nm thick, can be as thick as about 50 um if the transferred to substrate is thinned) to a standard sized silicon substrate, which could be conventionally processed in a production wafer fab. The TSVs of CS may also be trenches, or other shaped regions. The TSVs may be selectively filled with different CS materials, for example, one region of CS filled TSVs may include GaAs, another region on the same silicon substrate may have GaN filled TSVs, and so on, by use of different CS templates attached to the bottom of the TSV'd silicon substrate.

As illustrated in FIG. **38**A, a silicon/CS hybrid wafer may include monocrystalline silicon substrate **3800**, CS#1 in CS#1 via **3857**, CS#2 in CS#2 via **3858**, and surface **3801**. For this example, CS#1 and CS#2 are different CS materials and CS#1 may have a higher atomic density than CS#2. An ion-cut implant **3810** of an atomic species, for example hydrogen, may be performed to generate a plane of defects (a perforation layer) in silicon substrate **3800**, CS#1 in CS#1 via **3857**, CS#2 in CS#2 via **3858** that may be utilized for cleaving a thin hybrid layer to transfer to another substrate for further processing/manufacturing. However, an uneven cleave plane of defects may result from the differing ion-implant ranges from surface **3801** due to the differing densities of material into which it is implanted. This may substantially preclude a high quality ion-cut cleave for the desired layer transfer. For example, Si perforation plane **3899** may be deeper with respect to surface **3801** than CS#2 perforation plane **3898**, both which may be deeper than CS#1 perforation plane **3897**. If the three perforation planes are close enough in depth to each other, on the order of about 0-100 nm or less, the ion-cut implant dose may be increased and a high quality cut may be obtained. However, this may also create a higher electrical and physical defectivity in the thin films and material that the ion implant travels thru. The defects may be annealed with techniques disclosed in the referenced documents and herein, such as short wavelength laser anneals and perforated carrier wafer techniques.

As illustrated in FIG. **38**B, if a higher implant dose cannot accomplish a high quality ion-cut cleave, the material stack that ion-cut implant **3810** travels thru may be modulated over each substrate region by deposition/growth of an implant depth modulation material. Implant modulation material for silicon regions **3840** may be deposited, etched, formed over the silicon substrate **3800** regions at exposed surface **3801**, and an implant modulation material for CS#2 regions **3842** may be deposited, etched, formed over CS#2 via **3858** regions at exposed surface **3801**. Thus, the three perforation planes, Si perforation plane **3899**, CS#2 perforation plane **3898**, and CS#1 perforation plane **3897**, may be brought close enough in depth to each other to allow a high quality cleave with an even cleave plane. Implant modulation material for silicon regions **3840** and implant modulation material for CS#2 regions **3842** may include, for example, silicon oxide, indium tin oxide, photoresist, silicon nitride, and other semiconductor thin film materials, including combinations of materials, such as, for example, photoresist and silicon oxide. Implant modulation material for silicon regions **3840** and implant modulation material for CS#2 regions **3842** may be constructed with different materials from each other, or may simply be the same material with a different thickness. The edges of implant modulation material for silicon regions **3840** and implant modulation material for CS#2 regions **3842** may be sloped (shown) to approximately match the slope of the silicon substrate TSVs so that the perforated planes at the interface between Si and CS#1 or Si and CS#2 may be substantially even. The sloping may be accomplished with well-known photoresist exposure and develop techniques or with etching (plasma and wet chemical) techniques. Alternatively to or in combination with the modulation layer regions, a selective chemical etch that is selective to the denser CS#1 material may be utilized to remove a the top portion (not shown) of CS#1 via **3857** to achieve an even cleave plane.

While concepts in this patent application have been described with respect to 3D-ICs with two stacked device layers, those of ordinary skill in the art will appreciate that it can be valid for 3D-ICs with more than two stacked device layers. Additionally, some of the concepts may be applied to 2D ICs.

Some embodiments of the invention may include alternative techniques to build IC (Integrated Circuit) devices including techniques and methods to construct 3D IC systems. Some embodiments of the invention may enable device solutions with far less power consumption than prior art. The device solutions could be very useful for the growing application of mobile electronic devices and mobile systems such as, for example, mobile phones, smart phone, and cameras, those mobile systems may also connect to the internet. For example, incorporating the 3D IC semiconductor devices according to some embodiments of the invention within the mobile electronic devices and mobile systems could provide superior mobile units that could operate much more efficiently and for a much longer time than with prior art technology.

Smart mobile systems may be greatly enhanced by complex electronics at a limited power budget. The 3D technology described in the multiple embodiments of the invention would allow the construction of low power high complexity mobile electronic systems. For example, it would be possible to integrate into a small form function a complex logic circuit with high density high speed memory utilizing some of the

3D DRAM embodiments of the invention and add some non-volatile 3D NAND charge trap or RRAM described in some embodiments of the invention. Mobile system applications of the 3D IC technology described herein may be found at least in FIG. 156 of U.S. Pat. No. 8,273,610, the contents of which are incorporated by reference.

Furthermore, some embodiments of the invention may include alternative techniques to build systems based on integrated 3D devices including techniques and methods to construct 3D IC based systems that communicate with other 3DIC based systems. Some embodiments of the invention may enable system solutions with far less power consumption and intercommunication abilities at lower power than prior art. These systems may be called 'Internet of Things", or IoT, systems, wherein the system enabler is a 3DIC device which may provide at least three functions: a sensing capability, a digital and signal processing capability, and communication capability. For example, the sensing capability may include a region or regions, layer or layers within the 3DIC device which may include, for example, a MEMS accelerometer (single or multi-axis), gas sensor, electric or magnetic field sensor, microphone or sound sensing (air pressure changes), image sensor of one or many wavelengths (for example, as disclosed in at least U.S. Pat. Nos. 8,283,215 and 8,163,581, incorporated herein by reference), chemical sensing, gyroscopes, resonant structures, cantilever structures, ultrasonic transducers (capacitive & piezoelectric). Digital and signal processing capability may include a region or regions, layer or layers within the 3D IC device which may include, for example, a microprocessor, digital signal processor, microcontroller, FPGA, and other digital land/or analog logic circuits, devices, and subsystems. Communication capability, such as communication from at least one 3D IC of IoT system to another, or to a host controller/nexus node, may include a region or regions, layer or layers within the 3D IC device which may include, for example, an RF circuit and antenna or antennas for wireless communication which might utilize standard wireless communication protocols such as G4, WiFi or Bluetooth, I/O buffers and either mechanical bond pads/wires and/or optical devices/transistors for optical communication, transmitters, receivers, codecs, DACs, digital or analog filters, modulators.

Energy harvesting, device cooling and other capabilities may also be included in the system. The 3DIC inventions disclosed herein and in the incorporated referenced documents enable the IoT system to closely integrate different crystal devices, for example a layer or layers of devices/transistors formed on and/or within mono or poly crystalline silicon combined with a layer or layers of devices/transistors formed on and/or within Ge, or a layer of layers of GaAs, InP, differing silicon crystal orientations, and so on. For example, incorporating the 3D IC semiconductor devices according to some embodiments of the invention as or within the IoT systems and mobile systems could provide superior IoT or mobile systems that could operate much more efficiently and for a much longer time than with prior art technology. The 3D IC technology herein disclosed provides a most efficient path for heterogeneous integration with very effective integration reducing cost and operating power with the ability to support redundancy for long field life and other advantages which could make such an IoT System commercially successful.

Alignment is a basic step in semiconductor processing. For most cases it is part of the overall process flow that every successive layer is patterned when it is aligned to the layer below it. These alignments could all be done to one common alignment mark, or to some other alignment mark or marks that are embedded in a layer underneath. In today's equipment such alignment would be precise to below a few nanometers and better than 40 nm or better than 20 nm and even better than 10 nm. In general such alignment could be observed by comparing two devices processed using the same mask set. If two layers in one device maintain their relative relationship in both devices—to few nanometers—it is clear indication that these layers are aligned each to the other. This could be achieved by either aligning to the same alignment mark (sometimes called a zero mark alignment scheme), or one layer is using an alignment mark embedded in the other layer (sometimes called a direct alignment), or using different alignment marks of layers that are aligned to each other (sometimes called an indirect alignment).

In this document, the connection made between layers of, generally, single crystal, transistors, which may be variously named for example as thermal contacts and vias, Thru Layer Via (TLV), TSV (Thru Silicon Via), may be made and include electrically and thermally conducting material or may be made and include an electrically non-conducting but thermally conducting material or materials. A device or method may include formation of both of these types of connections, or just one type. By varying the size, number, composition, placement, shape, or depth of these connection structures, the coefficient of thermal expansion exhibited by a layer or layers may be tailored to a desired value. For example, the coefficient of thermal expansion of the second layer of transistors may be tailored to substantially match the coefficient of thermal expansion of the first layer, or base layer of transistors, which may include its (first layer) interconnect layers.

Base wafers or substrates, or acceptor wafers or substrates, or target wafers substrates herein may be substantially comprised of a crystalline material, for example, mono-crystalline silicon or germanium, or may be an engineered substrate/wafer such as, for example, an SOI (Silicon on Insulator) wafer or GeOI (Germanium on Insulator) substrate. Similarly, donor wafers herein may be substantially comprised of a crystalline material and may include, for example, mono-crystalline silicon or germanium, or may be an engineered substrate/wafer such as, for example, an SOI (Silicon on Insulator) wafer or GeOI (Germanium on Insulator) substrate, depending on design and process flow choices.

While mono-crystalline silicon has been mentioned as a transistor material in this document, other options are possible including, for example, poly-crystalline silicon, mono-crystalline germanium, mono-crystalline III-V semiconductors, graphene, and various other semiconductor materials with which devices, such as transistors, may be constructed within. Moreover, thermal contacts and vias may or may not be stacked in a substantially vertical line through multiple stacks, layers, strata of circuits. Thermal contacts and vias may include materials such as sp2 carbon as conducting and sp3 carbon as non-conducting of electrical current. Thermal contacts and vias may include materials such as carbon nanotubes. Thermal contacts and vias may include materials such as, for example, copper, aluminum, tungsten, titanium, tantalum, cobalt metals and/or silicides of the metals. First silicon layers or transistor channels and second silicon layers or transistor channels may be may be substantially absent of semiconductor dopants to form an undoped silicon region or layer, or doped, such as, for example, with elemental or compound species that form a p+, or p, or p−, or n+, or n, or n− silicon layer or region. A heat removal apparatus may include an external surface from which heat transfer may take place by methods such as air cooling, liquid cooling, or attachment to another heat sink or heat spreader structure. Furthermore, raised source and drain contact structures, such as etch and epi SiGe and SiC, and implanted S/Ds (such as C) may be

utilized for strain control of transistor channel to enhance carrier mobility and may provide contact resistance improvements. Damage from the processes may be optically annealed. Strain on a transistor channel to enhance carrier mobility may be accomplished by a stressor layer or layers as well.

In this specification the terms stratum, tier or layer might be used for the same structure and they may refer to transistors or other device structures (such as capacitors, resistors, inductors) that may lie substantially in a plane format and in most cases such stratum, tier or layer may include the interconnection layers used to interconnect the transistors on each. In a 3D device as herein described there may at least two such planes called tier, or stratum or layer.

In a 3D IC system stack, each layer/stratum may include a different operating voltage than other layers/stratum, for example, one stratum may have Vcc of 1.0 v and another may have a Vcc of 0.7 v. For example, one stratum may be designed for logic and have the appropriate Vcc for that process/device node, and another stratum in the stack may be designed for analog devices, and have a different Vcc, likely substantially higher in value—for example, greater than 3 volts, greater than 5 volts, greater than 8 volts, greater than 10 volts. In a 3D IC system stack, each layer/stratum may include a different gate dielectric thickness than other layers/stratum. For example, one stratum may include a gate dielectric thickness of 2 nm and another 10 nm. The definition of dielectric thickness may include both a physical definition of material thickness and an electrically 'effective' thickness of the material, given differing permittivity of the materials. In a 3D IC system stack, each layer/stratum may include different gate stack materials than other layers/stratum. For example, one stratum may include a HKMG (High k metal gate) stack and another stratum may include a polycide/silicon oxide gate stack. In a 3D IC system stack, each layer/stratum may include a different junction depth than other layers/stratum. For example, the depth of the junctions may include a FET transistor source or drain, bipolar emitter and contact junctions, vertical device junctions, resistor or capacitor junctions, and so on. For example, one stratum may include junctions of a fully depleted MOSFET, thus its junction depth may be defined by the thickness of the stratum device silicon to the vertical isolation, and the other stratum may also be fully depleted devices with a junction depth defined similarly, but one stratum has a thicker silicon layer than the other with respect to the respective edges of the vertical isolation. In a 3D IC system stack, each layer/stratum may include a different junction composition and/or structure than other layers/stratum. For example, one stratum may include raised source drains that may be constructed from an etch and epitaxial deposition processing, another stratum in the stack may have implanted and annealed junctions or may employ dopant segregation techniques, such as those utilized to form DSS Schottky transistors.

Some 3D device flows presented herein suggest the use of the ELTRAN or modified ELTRAN techniques and in other time a flow is presented using the ion-cut technique. It would be obvious for someone skilled in the art to suggest an alternative process flow by exchanging one layer transfer technique with another. Just as in some steps one could exchange these layer transfer techniques with others presented herein or in other publication such as the bonding of SOI wafer and etch back. These would be variations for the described and illustrated 3D process flows presented herein.

In various places here or in the incorporated by reference disclosures of heat removal techniques have been presented and illustrated. It would be obvious to person skilled in the art to apply these techniques to any of the other variations of 3D devices presented herein.

In various places here or in the incorporated by reference disclosures of repair and redundancy techniques have been presented and illustrated. It would be obvious to person skilled in the art to apply these techniques to any of the other variations of 3D devices presented herein.

In various places here or in the incorporated by reference disclosures memories and other circuit and techniques of customizing and integrating these structures have been presented and illustrated. It would be obvious to person skilled in the art to apply these techniques and structures to any of the other variations of 3D devices presented herein.

It should be noted that one of the design requirements for a monolithic 3D IC design may be that substantially all of the stacked layers and the base or substrate would have their respective dice lines (may be called scribe-lines) aligned. As the base wafer or substrate is processed and multiple circuits may be constructed on semiconductor layers that overlay each other, the overall device may be designed wherein each overlaying layer would have its respective dice lines overlying the dice lines of the layer underneath, thus at the end of processing the entire layer stacked wafer/substrate could be diced in a single dicing step. There may be test structures in the streets between dice lines, which overall may be called scribe-lanes or dice-lanes. These scribe-lanes or dice-lanes may be 10 um wide, 20 um wide, 50 um wide 100 um wide, or greater than 100 um wide depending on design choice and die singulation process capability. The scribe-lanes or dice-lanes may include guard-ring structures and/or other die border structures. In a monolithic 3D design each layer test structure could be connected through each of the overlying layers and then to the top surface to allow access to these 'buried' test structure before dicing the wafer. Accordingly the design may include these vertical connections and may offset the layer test structures to enable such connection. In many cases the die borders comprise a protection structure, such as, for example, a guard-ring structure, die seal structure, ESD structure, and others elements. Accordingly in a monolithic 3D device these structures, such as guard rings, would be designed to overlay each other and may be aligned to each other during the course of processing. The die edges may be sealed by a process and structure such as, for example, described in relation to FIG. 183C of incorporated U.S. Pat. No. 8,273,610, and may include aspects as described in relation to FIGS. 183A and 183B of same reference. One skilled in the art would recognize that the die seal can be passive or electrically active. On each 3D stack layer, or stratum, the electronic circuits within one die, that may be circumscribed by a dice-lane, may not be connected to the electronic circuits of a second die on that same wafer, that second die also may be circumscribed by a dice-lane. Further, the dice-lane/scribe-lane of one stratum in the 3D stack may be aligned to the dice-lane/scribe-lane of another stratum in the 3D stack, thus providing a direct die singulation vector for the 3D stack of strata/layers.

It will also be appreciated by persons of ordinary skill in the art that the invention is not limited to what has been particularly shown and described hereinabove. For example, drawings or illustrations may not show n or p wells for clarity in illustration. Moreover, transistor channels illustrated or discussed herein may include doped semiconductors, but may instead include undoped semiconductor material. Further, any transferred layer or donor substrate or wafer preparation illustrated or discussed herein may include one or more undoped regions or layers of semiconductor material. Rather,

the scope of the invention includes both combinations and sub-combinations of the various features described hereinabove as well as modifications and variations which would occur to such skilled persons upon reading the foregoing description. Thus the invention is to be limited only by the appended claims.

We claim:

1. A 3D device comprising:

a first layer comprising first transistors, said first layer overlaid by at least one interconnection layer;

a second layer comprising second transistors, said second layer overlaying said interconnection layer;

a plurality of electrical connections connecting said second transistors with said interconnection layer; and

at least one thermally conductive and electrically non-conductive contact,

wherein said at least one thermally conductive and electrically non-conductive contact thermally connects said second layer to a top or bottom surface of said 3D device.

2. A 3D device according to claim **1**,

wherein said plurality of electrical connections comprises at least one through-silicon-via, said at least one through-silicon-via comprises a material which has a thermal conductivity greater than 10 W/m-K.

3. A 3D device according to claim **1**, further comprising:

a heat-spreader layer disposed between said first layer and said second layer.

4. A 3D device according to claim **1**, further comprising:

a power distribution network to provide power to said second transistors,

wherein said power distribution network provides a heat removal path between at least one of said second transistors and the top or bottom surface of said 3D device.

5. A 3D device according to claim **1**,

wherein said plurality of electrical connections comprise thru layer vias and,

wherein said thru layer vias have a density greater than 10,000 vias/cm^2.

6. A 3D device according to claim **1**, further comprising:

a via through said second layer,

wherein said via is part of a heat removal structure of said device.

7. A 3D device according to claim **1**,

wherein said interconnection layer comprises a power grid to provide power to at least one of said second transistors.

8. A system, comprising: a 3D device, said 3D device comprising:

a first layer comprising first transistors, said first layer overlaid by a first interconnection layer;

a second layer comprising second transistors, said second layer overlaying said first interconnection layer;

a plurality of second interconnection layers overlaying said second layer;

a plurality of electrical connections connecting at least one of said second interconnection layers with said first interconnection layer; and

a plurality of thermally conducting paths from said second transistors to a top or bottom surface of said 3D device.

9. A system according to claim **8**,

wherein said second layer has a thickness less than 2 microns.

10. A system according to claim **8**, further comprising:

a heat-spreader layer disposed between said first layer and said second layer.

11. A system according to claim **8**, further comprising:

a power distribution network to provide power to said second transistors,

wherein said power distribution network provides a heat removal path between at least one of said second transistors and the top or bottom surface of said 3D device.

12. A system according to claim **8**,

wherein said plurality of electrical connections comprise thru layer vias and,

wherein said thru layer vias have a density greater than 10,000 vias/cm^2.

13. A system according to claim **8**, further comprising:

at least one thermally conductive and electrically non-conducting contact to said second layer.

14. A system, comprising: a 3D device, said 3D device comprising:

a first layer comprising first transistors, said first layer overlaid by at least one interconnection layer,

a second layer comprising second transistors, said second layer overlaying said interconnection layer;

a plurality of electrical connections connecting said second transistors with said interconnection layer; said plurality of electrical connections further comprising:

a power distribution grid providing power to said second transistors, and

a plurality of thermally conducting paths from said power distribution grid to a top or bottom surface of said 3D device,

wherein said second layer has a thickness less than 2 microns.

15. A system according to claim **14**,

wherein said plurality of electrical connections comprises a through-silicon connection, and

wherein at least one of said plurality of electrical connections comprises at least one thermally conductive and electrically non-conductive contact.

16. A system according to claim **14**, further comprising:

a heat-spreader layer disposed between said first layer and said second layer.

17. A system according to claim **14**,

wherein a portion of said power distribution grid is between said first layer and said second layer.

18. A system according to claim **14**,

wherein said plurality of electrical connections comprise thru layer vias and,

wherein said thru layer vias have a density greater than 10,000 vias/cm^2.

19. A system according to claim **14**, further comprising:

at least one thermally conductive and electrically non-conducting contact to said second layer.

20. A system according to claim **14**,

wherein said second transistors are FinFET type transistors.

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