

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,

Petitioner,

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,

Patent Owner.

Case No.: IPR2024-00790
U.S. Patent No. 10,868,031

**PATENT OWNER'S PRELIMINARY RESPONSE
UNDER 37 C.F.R. § 42.107**

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LIST OF EXHIBITS

Exhibit	Description
Ex. 2001	New Oxford American Dictionary, 3 rd Ed., 2010
Ex. 2002	The American Heritage® College Dictionary, 3 rd Ed., 2000
Ex. 2003	Webster's II New College Dictionary, 3 rd Ed., 2005
Ex. 2004	Merriam-Webster's Dictionary and Thesaurus, 5 th Printing, 2014
Ex. 2005	Declaration of Jonathan Bradford

LIST OF ABBREVIATIONS

Abbreviation	Term
'031	U.S. Pat. No. 10,868,031
'031FH	File History of U.S. Pat. No. 10,868,031
Challenged Claims	Ex. 1001, Claims 1-5
Office	U.S. Patent and Trademark Office
Kim	U.S. Patent No. 10,381,369
Petition or Pet.	Petition for <i>Inter Partes</i> Review of U.S. Patent No. 10,868,031 (IPR2024-00790, Paper 1)
Parallel district court litigation	<i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc.</i> , NDCA-3-23-cv-05792 (N.D. Cal.)
Patent Owner or PO	Yangtze Memory Technologies Co. Ltd.
Petitioner	Micron Technology, Inc.
POSITA	Person of ordinary skill in the art
Tessariol	U.S. Patent Publication No. 2019/0081061

Pursuant to § 42.107,¹ Patent Owner submits this Preliminary Response to the above-captioned Petition, which should be denied in its entirety based on Petitioner's failure to show a reasonable likelihood of prevailing on any asserted ground as to any Challenged Claim.

I. INTRODUCTION

U.S. Patent No. 10,868,031 ("the '031," Ex. 1001) is directed to a novel three-dimensional (3D) memory device having multiple stacks of word lines. Fabrication of 3D NAND memory devices generally involves stacks of alternating dielectric and sacrificial materials, which can be patterned in a staircase formation and with semiconductor channels and mechanical supports (supporting pillars) that help prevent the deformation during the replacement of the sacrificial materials with conducting word lines. '031, 1:23-38, 7:19-25. The prior art at the time of filing of the '031 Patent used multiple patterning processes for the multiple stacks, which was "time-consuming and costly." '031, 1:33-37, 7:57-62. The '031 simplifies the fabrication process of these "multi-stack 3D NAND memory devices" by using a single patterning process for the multiple stacks. '031, 1:33-37, 1:42-49, 9:15-18.

¹ All emphasis and color annotations herein are added, and all statutory and regulatory citations are to either 35 U.S.C. or 37 C.F.R., as the context indicates, unless otherwise stated.

The '031 avoids several issues with the prior art including: 1) using different photomasks for each dielectric stack, which was both costly and time consuming because it increased the number of photomasks and photolithography operations; 2) processing on the lower structures before forming the upper dielectric stack, which leads to quality issues; and 3) using different dimensions for sub-channel holes and sub-pillar holes, which complicated fabrication and required higher precision control. '031, 8:5-31.

The '031 introduced a 3D memory device in which the stacks of the device are “patterned by one staircase-forming patterning process to form the multiple-stack staircase structure.” '031, 8:63-9:1. The supporting pillars formed using the multiple patterning process of prior art can result in pillars with “unaligned (or disjointed) surfaces at the connection portions;” in contrast, the '031's supporting pillars have “aligned sidewall surfaces.” '031, 8:32-53. The claimed invention recites “a filling structure that surrounds the multiple-stack staircase structure,” a “semiconductor channel [which] comprises unaligned sidewall surfaces,” and a “supporting pillar [which] comprises aligned sidewall surfaces.” *See* '031, Claim 1, 2:40-45, 8:48-53. As a result, the claimed invention avoids the issues arising from using multiple patternings and “improves device yield and performance.” '031, 9:1-28.

Institution should be denied because the Petition fails to establish a reasonable likelihood of prevailing with respect to any of Challenged Claims.

Petitioner does not assert that any of the cited references anticipates the independent Challenged Claims. Instead, Petitioner raises obviousness arguments based on a mix of contradictory assertions, faulty analysis, and conclusory testimony from its expert.

Petitioner's Ground 1 relies on the "Kim" reference (Ex. 1005) for each limitation of the Challenged Claims, but Petitioner fails to show that Kim discloses or renders obvious each and every limitation of claim 1. In particular, Kim does not disclose or render obvious that its alleged filling structure is surrounding the multiple-stack staircase structure as required by the Challenged Claims. Under the proper construction of the term "surrounding," the Challenged Claims require the filling structure to encircle the multiple-stack staircase structure. The alleged filling structure of Kim, however, merely covers the top and one side of the staircase structure, but does not encircle the staircase structure. Petitioner's arguments for obviousness provide only conclusory and illogical arguments that are belied by Kim's teachings.

Petitioner's Ground 2 relies on the "Tessariol" reference (Ex. 1006) for each limitation of the Challenged Claims, but again, Petitioner fails to show that Tessariol discloses or renders obvious at least the limitation reciting "a filling structure

surrounding the multiple-stack staircase structure.” Because no single element in Tessariol’s memory device surrounds the staircase structure, Petitioner combines multiple elements from Tessariol in an attempt to patch together a purported “filling structure” that meets the claim requirements. But even if Petitioner’s patchwork of elements were considered a filling structure, Tessariol still does not disclose or render obvious a filling structure that surrounds the staircase structure under the correct interpretation of “surrounding” because there is no purported filling structure at the lateral ends of Tessariol’s staircase structures. Petitioner’s obviousness arguments are again conclusory, illogical, and contradict the evidence.

Petitioner’s Ground 3 applies Tessariol’s teachings to Kim for claim 4, but otherwise relies on Kim for claim 1. Therefore, Petitioner’s arguments fail for at least the reasons provided with regard to Petitioner’s Ground 1.

Petitioner’s Ground 4 applies Kim’s teaching to Tessariol but only as to particular requirements of claim 1. Specifically, Petitioner does not raise any new arguments as to the “filling structure” limitation and instead relies on its Ground 2 arguments (Pet. 90). Petitioner does not otherwise address this limitation (*see* Pet. 90-96). Therefore, Petitioner’s arguments fail for at least the reasons provided with regard to Petitioner’s Ground 2.

Because each prior art reference, individually or combined, fails to disclose or render obvious at least one limitation of the Challenged Claims, the Board should deny institution.

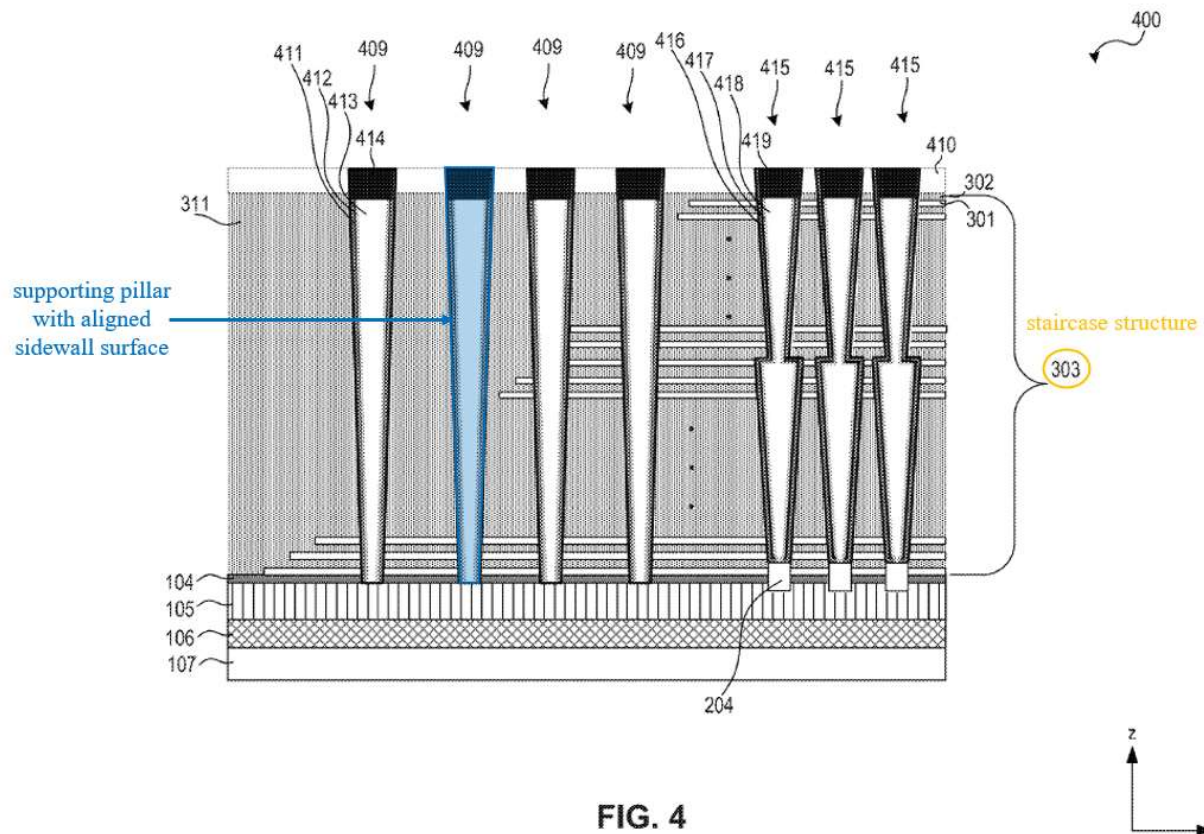
II. THE CLAIMED INVENTION OF THE '031 PATENT

The claimed invention of the '031 is directed to “three-dimensional memory device architectures” that address issues arising from the fabrication techniques known in the prior art and, as a result, “improves device yield and performance.” '031, 1:42-49, 9:15-28.

Specifically, the '031 is directed to an improved memory device fabrication technique that involves “one staircase-forming patterning process to form the multiple-stack staircase structure.” '031, 8:63-9:1. Techniques known in the prior art involved employing multiple staircase-forming patterning processes to obtain a multiple-stack memory device, which was “time-consuming and costly.” '031, 1:33-37, 7:57-62. There were several reasons for these disadvantages. First, having to use different photomasks for different dielectric stacks increased the number of required photomasks and photolithography operations, raising cost and time. Second, forming an upper dielectric stack after the lower one led to quality issues in the upper stack due to processing it on top of the lower structures. Third, sub-channel holes and sub-pillar holes often had different dimensions, making it

challenging to achieve uniformity and required higher precision control. '031, 8:5-31.

The novel device the '031 teaches and recites in the claims is characterized by forming the **staircase structure**, which has alternating layers (e.g., conductor and insulating layers) that are etched to form a step-like pattern, by one patterning process, thereby avoiding the issues that arise from multiple patterning of different stacks and “improv[ing] device yield and performance.” '031, 9:1-28. As a result of this single patterning process, **the supporting pillars** have **aligned sidewall surfaces**, in contrast with the unaligned sidewall surfaces of the supporting pillars in the prior art. '031, 8:35-53.



'031, Fig. 4 (annotated).

The device of the '031 also includes “**dielectric filling structure 311** that surrounds **staircase structure 303**,” which comprises staircase regions that “can each surround memory structure [] along the x-y plane.” '031, 13:44-48, 22:30-32. After the staircase structure 303 is formed, a dielectric filling material is deposited to fill the space created by the removal of parts of the dielectric stack. **Dielectric filling structure 311** is deposited in both the periphery region and the core region. Excessive dielectric filling material from the top surface is removed using a suitable planarization method. The remaining dielectric filling material forms the **dielectric filling structure 311** that surrounds the **staircase structure 303**. **Dielectric filling structure 311** can be made of any suitable dielectric material that provides electrical insulation for the **staircase structure 300**. '031, 13:36-64, 22:27-32.

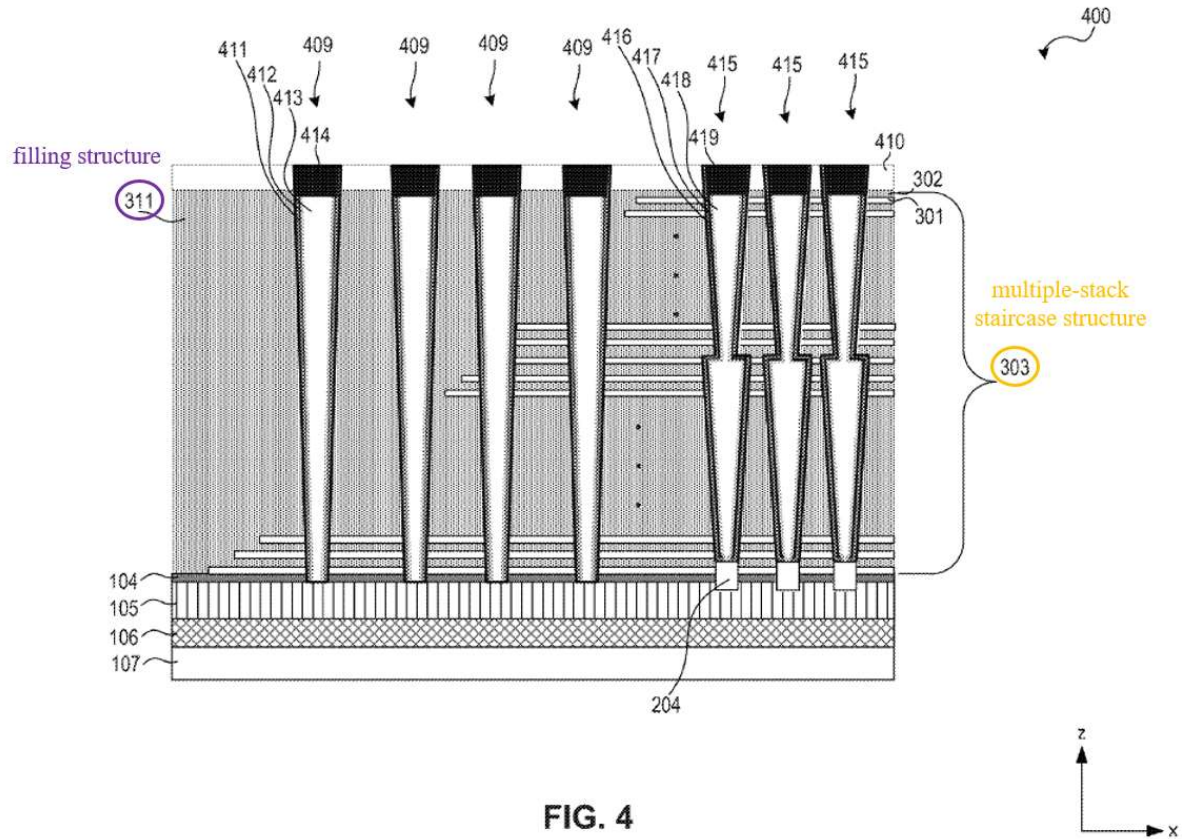
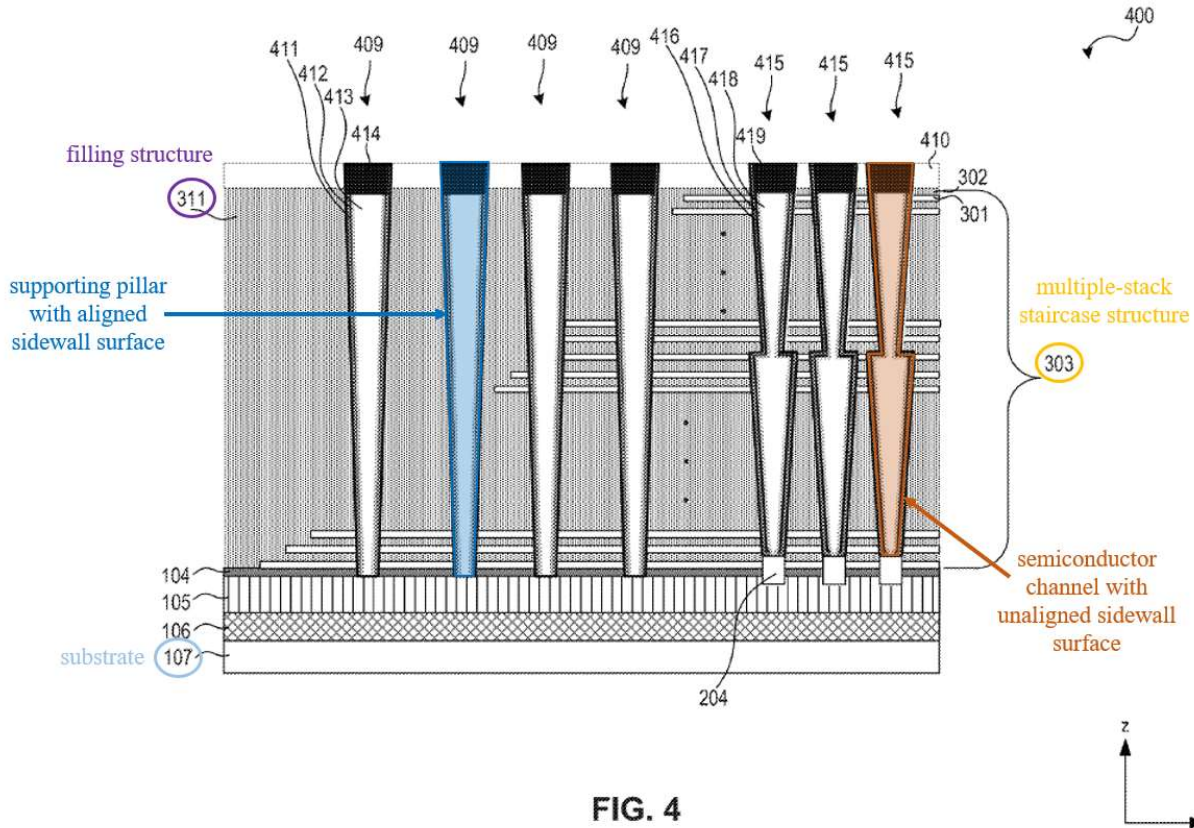


FIG. 4

'031, Fig. 4 (annotated).

A representative embodiment of the '031's memory device includes: (1) a “**substrate 107**” ('031, 10:17-23); (2) a “**multiple-stack staircase structure 303**” ('031, 13:30-35); (3) a “**filling structure 311**” surrounding the multiple-stack staircase structure ('031, 13:36-49); (4) “**semiconductor channels 415**” ('031, 2:45-50, 14:37-44); and (5) “**supporting pillars 409**” ('031, 2:45-50, 14:37-44). A cross-section view of the memory device with these features is illustrated below.



'031, Fig. 4 (annotated).

The only independent claim of the Challenged Claims, claim 1, is directed to aspects of the above-described invention:

[1.pre] A memory device comprising:

[1.a] a substrate;

[1.b] a multiple-stack staircase structure comprising a plurality of staircase structures stacked over the substrate, [1.c] wherein each of the plurality of staircase structures comprises a plurality of conductor layers, wherein each of the plurality of conductor layers is located between two insulating layers;

[1.d] a filling structure surrounding the multiple-stack staircase structure;

[1.e] a semiconductor channel extending through the multiple-stack staircase structure, wherein the semiconductor channel comprises unaligned sidewall surfaces; and

[1.f] a supporting pillar extending through at least one of the multiple-stack staircase structure and the filling structure, wherein the supporting pillar comprises aligned sidewall surfaces.

III. FILE HISTORY

The claims of the '031 remain patentable over the prior art for at least the same reason identified during prosecution. As discussed further below in § VI, the prior art does not disclose or render obvious, *inter alia*, the claimed “filling structure surrounding the multiple-stack staircase structure” of the '031. Claims directed to this limitation were allowed after thorough prosecution and consideration of numerous prior art references.

The '031 was filed on September 10, 2018. During the pendency of the application, Applicant was required to restrict the invention to that of “a memory device” or “a method for forming a memory device.” Ex. 1002, 663-667 (09/04/2019 Requirement for Restriction/Election). Applicant elected, without

traverse, claims that restricted the invention of the '031 to that of “a memory device.”

Ex. 1002, 668-669 (09/23/2019 Reply to Restriction Requirement).

In a non-final office action, the Examiner rejected all the elected claims under 35 U.S.C. § 102(a)(1) as being allegedly anticipated by U.S. Publication No. 2010/0133599 (“Chae”). Ex. 1002, 825-830 (01/07/2020 Office Action). Applicant filed a response and argued against the rejection, pointing out that Chae fails to disclose at least “a semiconductor channel extending through the multiple-stack staircase structure, wherein *the semiconductor channel comprises unaligned sidewall surfaces.*” Ex. 1002, 851-854 (04/02/2020 Reply to Office Action). The Examiner subsequently allowed all pending claims. Ex. 1002, 862-865 (07/01/2020 Notice of Allowance). The '031 issued on December 15, 2020 with six claims. Ex. 2002, 938 (11/24/2020 Issue Notification).

IV. CLAIM CONSTRUCTION

The Board construes claim terms “using the same claim construction standard that would be used to construe the claim in a civil action.” § 42.100(b). Under this standard, claim terms are “generally given their ordinary and customary meaning” to a person of ordinary skill in the art. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312 (Fed. Cir. 2005) (*en banc*). A POSITA ascertains the meaning of the claims based on the claim language, specification, prosecution history, and relevant extrinsic

evidence, although the claims and patent specification are the primary sources for construing claims. *Id.*, 1314-16.

The parties have not yet exchanged proposed claim constructions in the parallel district court proceeding. Petitioner contends that “the terms of the ’031 Patent’s claims do not require further construction and can be afforded their plain and ordinary meaning.” Pet. 22. Patent Owner disagrees with Petitioner and submits a proposed construction of the claim term “surrounding,” which is recited in claim 1 of the ’031. Other than the term “surrounding,” Patent Owner submits that constructions of the claim terms are not necessary to assess whether the prior art reads on the Challenged Claims for the purposes of institution. Patent Owner reserves the right to modify its proposed construction and to raise further claim construction issues if the Board institutes IPR, and to raise claim construction issues in the underlying district court proceedings.

A. “surrounding” (Claim 1)

The term “surrounding,” which is a limitation of all Challenged Claims because it occurs in claim 1, should be construed according to its plain and ordinary meaning as to be all the way around (something)—in other words, encircling. This construction is both consistent with the plain and ordinary meaning of the term and is supported by the intrinsic evidence.

The plain meaning of “surrounding” is “encircling.” *See, e.g.*, Ex. 2001 (New Oxford American Dictionary 2010 defining “surround” as “be all around (someone or something); ... encircle (someone or something) so as to cut off communication or escape”); Ex. 2002 (American Heritage College 2000 defining “surround” as “encircle”); Ex. 2003 (Webster’s II New College 2005 defining “surround” as “to encircle on all sides of simultaneously”); Ex. 2004 (Merriam-Webster’s Dictionary and Thesaurus 2014 defining “surround” as “to enclose on all sides : ENCIRCLE”).

In the context of claim 1, the term “surrounding” occurs in limitation [1.d], which recites “*a filling structure surrounding the multiple-stack staircase structure.*” The claims use the term “surrounding” instead of narrower alternatives, such as “covering” or the concept of being “between” two structures.

Figs. 4 and 12 of the ’031 reproduced below show that the multiple-stack staircase structure is encircled by the filling structure (1201, 311). In Fig. 12, staircase regions (“first staircase region 1121” and “second staircase region 1122”) are shown to extend in the +x and –x directions. The ’031 makes clear that the staircase regions also extend in the +y and –y directions, and therefore “surround”

the memory structure.² '031, 13:27-28 (“Dielectric pairs of different tiers can be etched to *form staircases extending along the x-y plane.*”); 22:30-32 (“First staircase region 1121 and second staircase region 1122 can each *surround memory structure 1100 along the x-y plane.*”).

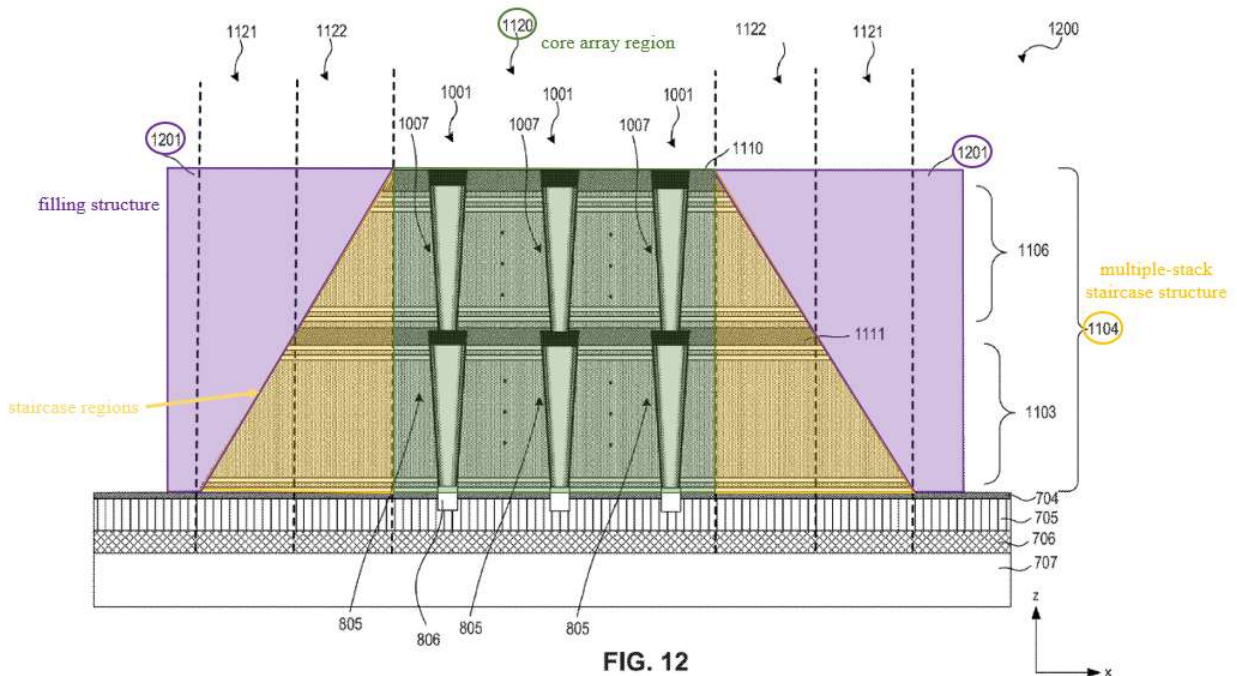
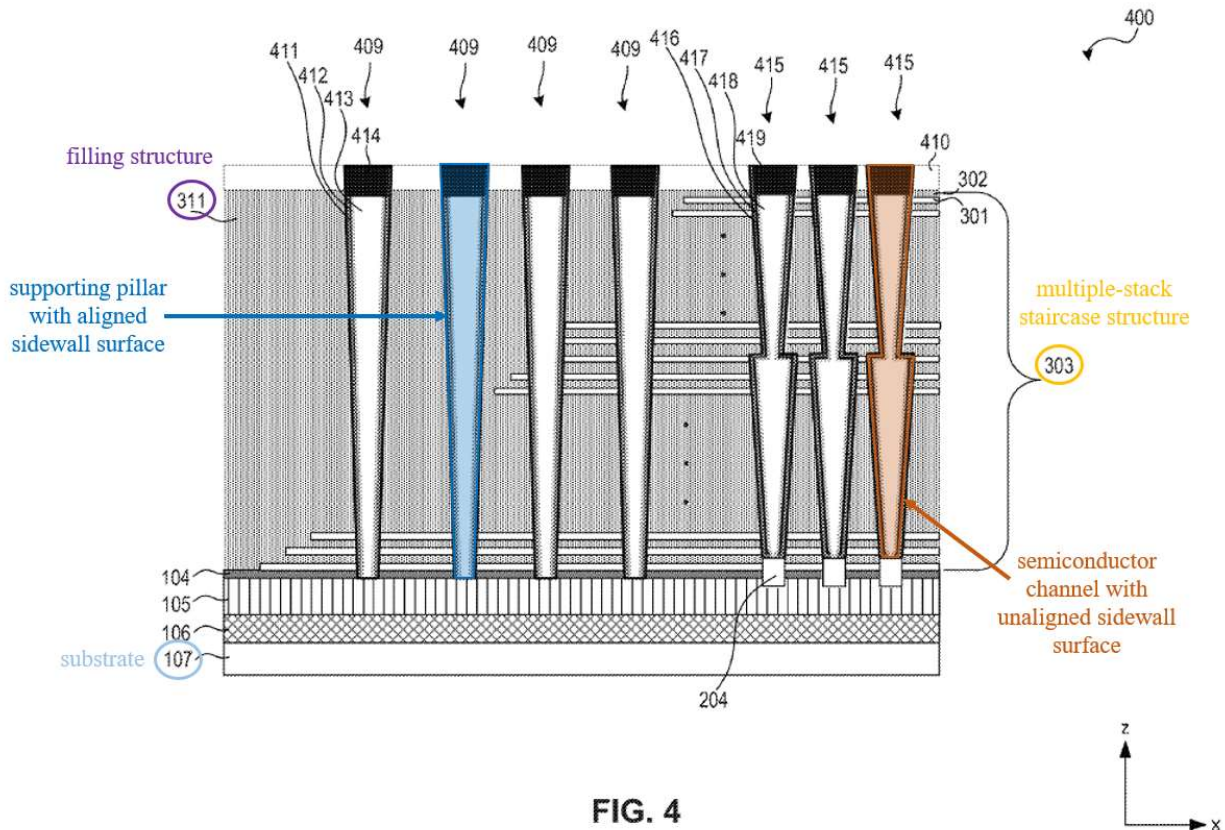


FIG. 12

'031 Patent, Fig. 12 (annotated).

² Fig. 12 has labels provided for x and z directions, and the y direction is perpendicular to both directions and points into the page.



'031 Patent, Fig. 4 (annotated).

After the patterning of the staircase regions, the filling structure is deposited to fill the space surrounding the staircase structure. *See* '031, 13:36-48 (“Further, **a dielectric filling material can be deposited after staircase structure 303 is formed to fill in the space formed by the removal of the portions of dielectric stack 203.** Dielectric filling structure 311 is deposited in periphery region 320 and core region 310 to fill in the space formed by the removal of the portions of dielectric stack 203.”); *see also* '031, 22:61-23:9. The filling structure therefore surrounds/encircles the multiple-stack staircase structure when it is deposited to the left, right, back, and front of the staircase structure.

Moreover, the '031 uses the term “surrounding” consistently as “encircling” in multiple other instances. *See* '031, 2:12-14 (“In some embodiments, the supporting pillar is filled with at least one of an insulating material and a pillar-support material ***surrounded by the insulating material.***”); 15:49-57 (“Charge trapping film 416 can also include a storage unit layer (memory layer) over and ***surrounded by the block dielectric layers*** for trapping charges and forming a plurality of charge storage regions along the z axis. Charge trapping film 416 can also include a tunneling layer (e.g., tunneling dielectric) over and ***surrounded by the memory layer.***”); *see also, e.g.*, '031, 3:31-35, 4:13-17, 18:25-26.

Although Petitioner does not argue explicitly for a construction of the term “surrounding,” Petitioner nonetheless argues:

To the extent PO argues that “surrounding” requires the dielectric filling structure be on all sides of the multi-stack staircase structure, such an interpretation is inconsistent with all embodiments of the '031 Patent, which never describes or illustrates the filling structure on each and every side of the multi-stack structure.

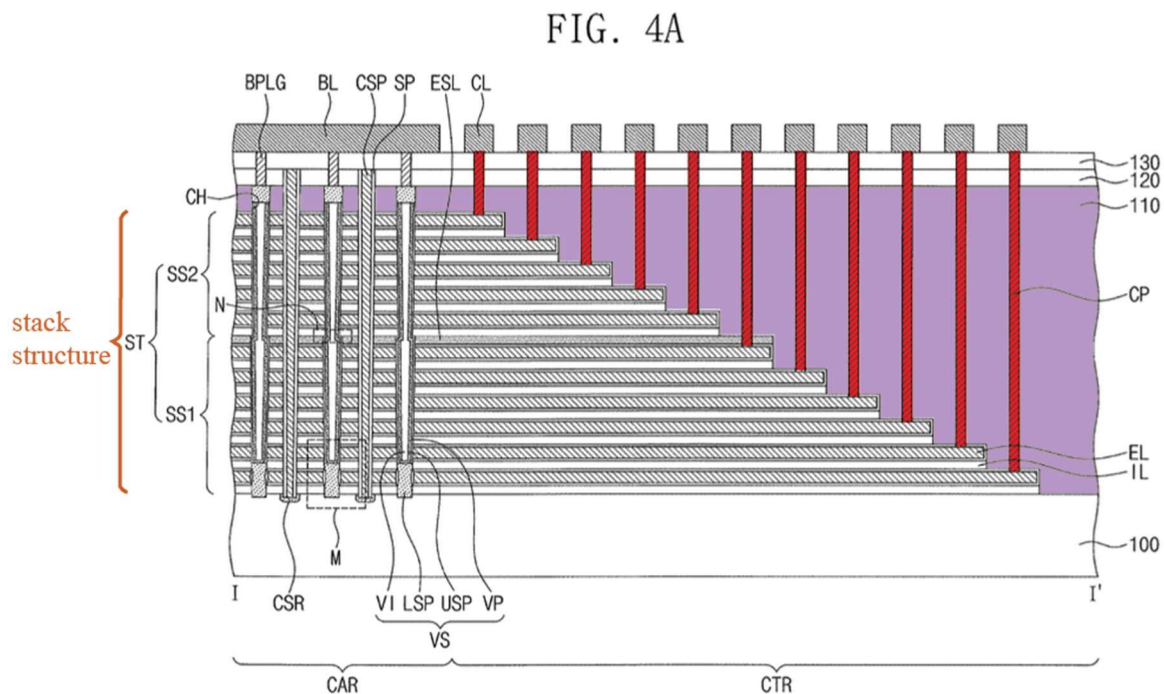
Pet. 34. Patent Owner’s construction, however, does not require filling structure on ***all*** sides of the multi-stack staircase structure—i.e., it does not require filling structure on the top and bottom of the staircase structure. As demonstrated above, the '031 does describe the filling structure on all sides of the multi-stack structure in the horizontal plane—i.e., the filling structure encircles the multi-stack structure.

V. BACKGROUND OF THE ASSERTED PRIOR ART

A. U.S. Patent No. 10,381,369 (“Kim”) (Ex. 1005)

Petitioner does not contend that Kim anticipates the Challenged Claims, and instead argues only that it renders obvious certain claims, including the sole independent Challenged Claim, claim 1. Pet. 8, 27-56.

Kim’s memory device includes a cell array region (“CAR”), and a connection region (“CTR”) with a **stack structure (ST)** composed of alternating electrode layers and insulating layers. Kim’s device further has **contact plugs** that each connect to a top electrode layer of the **stack structure**. Ex. 1005, 9:4-11. As shown in Figure 4A below, Kim’s **stack structure** is covered by a **filling insulation layer**:



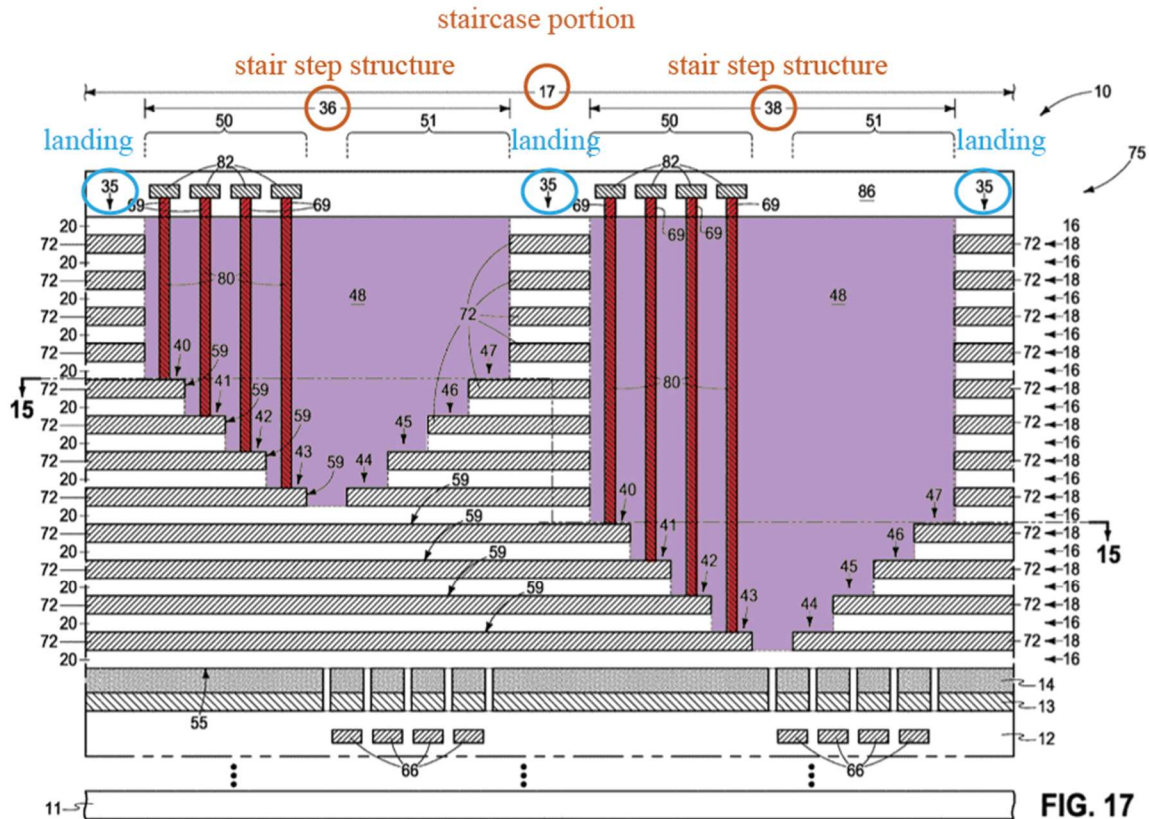
Ex. 1005, Fig. 4A (annotated); *see also* Ex. 1005, 9:53-58. Neither Kim’s figures nor its specification suggests filling insulation to the left of the staircase structure or perpendicular to the plane of Fig. 4A below (denoted as “D1” in Kim). As a result, Kim does not disclose or render obvious that the filling insulation layer surrounds the staircase structure.

B. U.S. Patent Publication No. 2019/0081061 (“Tessariol”) (Ex. 1006)

Petitioner does not contend that Tessariol anticipates the Challenged Claims, and instead argues only that it renders obvious certain claims, including the sole independent Challenged Claim, claim 1. Pet. 8, 57-86.

Tessariol describes a device with memory cells that includes an “**adjacent/staircase portion 17**” having multiple **stair step structures**, which are formed on the base substrate composed of vertically-stacked alternating tiers of first and second materials (*e.g.*, insulative, conductive, and semiconductive materials). Ex. 1006, [0029], [0031], [0034], [0048]. Tessariol’s device further has **operating conductive vias** that each connect to a top conductive step of the **stair step structures** and are “directly electrically coupled to one another by an interconnect line” above the alternating layers. Ex. 1006, [0046], [0052].

Tessariol’s **stair step structures** are in the shape of stadiums with **landings** that “define a crest between immediately adjacent stadiums” and an **insulating material** above the steps. Ex. 1006, [0035].



Ex. 1006, Fig. 17 (annotated).

As Petitioner’s expert acknowledges in the declaration, “the figures in Tessariol do not show the outer ends/sides of the device.” Ex. 1003, ¶ 184; *see also* Pet. 70 (“Note that Tessariol does not expressly depict the lateral ends of the device.”). Nor does Tessariol describe the lateral ends of the stair step structures as being bordered by insulating material. To the extent that the ends of the device are depicted in Tessariol’s figures (*e.g.*, Fig. 17), they appear exposed. As a result, Tessariol does not disclose or render obvious that insulating structure surrounds the staircase structure.

**VI. PETITIONER FAILS TO ESTABLISH A REASONABLE
LIKELIHOOD THAT IT WOULD PREVAIL WITH RESPECT TO
THE CHALLENGED CLAIMS**

Petitioner fails to establish a reasonable likelihood that it would prevail with respect to the Challenged Claims because Petitioner has failed to show that the prior art discloses or renders obvious “a filling structure surrounding the multiple-stack staircase structure” as required by the Challenged Claims. As explained below, Petitioner cites two references—Kim and Tessariol—and asserts that they, individually or in combination, show this feature. Each of Petitioner’s arguments fails.

First, Kim alone does not render obvious the Challenged Claims. For example, Kim does not disclose or render obvious that its alleged filling structure is “surrounding the multiple-stack staircase structure” as required by the Challenged Claims because Kim’s alleged filling structure merely covers the top and one side of the staircase structure. Under the proper construction of “surrounding” (§ IV.A), it is insufficient to cover parts of a structure without encircling it. Petitioner’s argument for obviousness provides only a conclusory and illogical argument as a purported motivation to modify the reference.

Second, Tessariol does not render obvious the Challenged Claims. Petitioner has not shown that Tessariol discloses or renders obvious that the alleged filling structure is “surrounding the multiple-stack staircase structure” as

required by the Challenged Claims because the lateral ends of the staircase structure are exposed, and nothing in Tessariol suggests having the purported filling structure encircle the staircase structure.

Ground 3 relies on the same disclosures as Ground 1 for claim 1 (Pet. 86-87) and fails at least for the reasons Ground 1 fails.

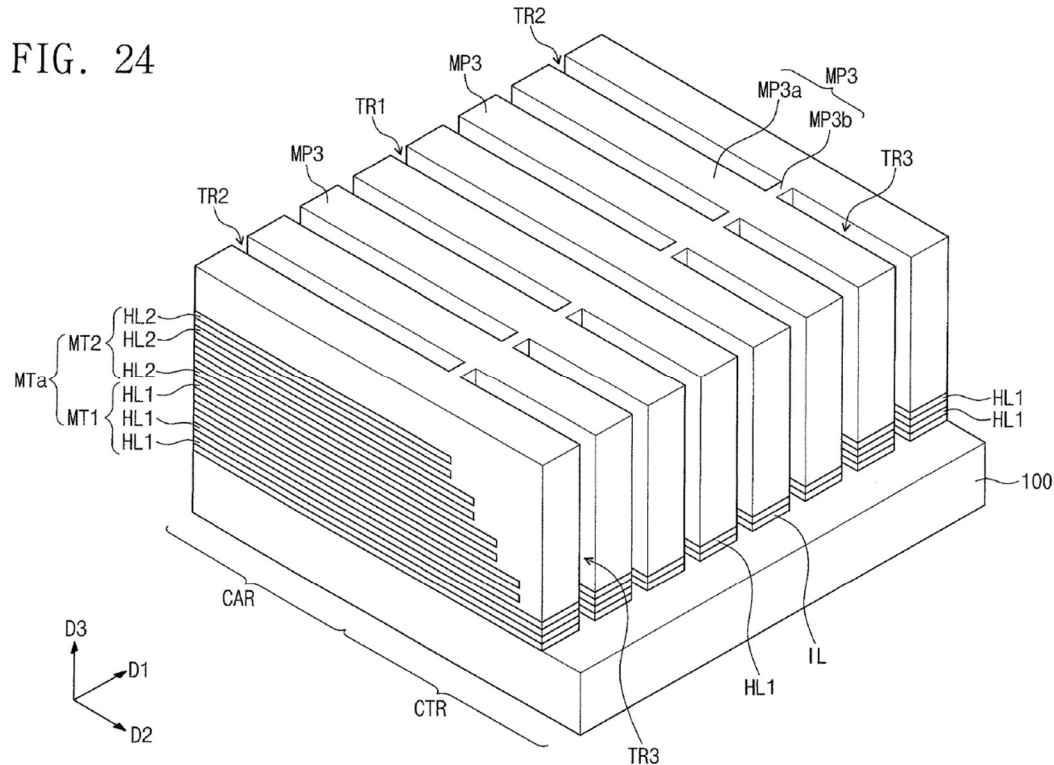
Ground 4 builds on Ground 2 to apply Kim’s teachings to Tessariol. Since both references fail to disclose or render obvious “a filling structure surrounding the multiple-stack staircase structure” and no arguments beyond those raised for Ground 2 are presented for this limitation in the proposed combination, the combination fails for the same reasons.

A. Ground 1: Petitioner Fails to Show That Kim Discloses or Renders Obvious “a Filling Structure Surrounding the Multiple-Stack Staircase Structure”

Petitioner fails to show that Kim discloses or renders obvious a filling structure “surrounding” a multiple-stack staircase structure because, at most, Kim teaches covering the top and one side of the staircase structure. Limitation [1.d] recites “*a filling structure surrounding the multiple-stack staircase structure.*” As discussed in § IV.A, the term “surrounding” means “encircling.” Kim does not disclose or render obvious a filling structure that encircles the staircase structure.

Petitioner erroneously points to Kim’s “filling insulation layer 110,” which covers but does not surround Kim’s “stack structures ST.” However, as shown in

Fig. 24 of Kim, the filling insulation layer does not cover three of the four sides (i.e., $-D2$, $+D1$, $-D1$) of its multiple-stack structure:

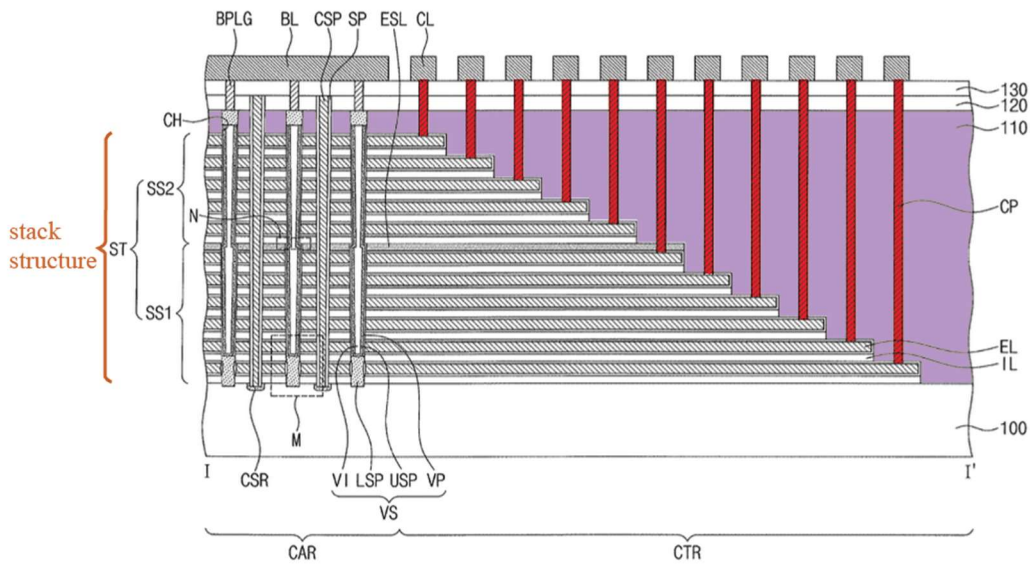


Ex. 1005, Fig. 24. Kim discloses that “[t]he filling insulation layer 110 may be disposed on the substrate 100 and may **cover** the stack structures ST.” Ex. 1005, 9:53-58 (emphasis added). Kim also discloses that “a filling insulation layer 110 may be formed on an entire top surface of the substrate 100 to **cover** the mold structure MT.” Ex. 1005, 11:11-13 (emphasis added). This is the full extent of Kim’s relevant disclosure, which says nothing to suggest that the insulation layer encircles the stack structures. For example, Kim does not suggest that the insulation layer covers the sides of the structure in the direction that extends perpendicular to

Figure 4B, i.e. the “D1” direction. Petitioner misrepresents Kim by stating “after forming the staircase region, Kim further discloses forming insulation layer 110 to fill all voids.” Pet. 33. Kim never discloses that the insulation layer “fill[s] all voids” or anything close to it. The only description Kim provides regarding the relationship between the filling insulation layer and the stack structures is that the former covers the latter, as quoted above.

Kim’s figures depict the purported **filling insulation layer** as covering the **stack structure** from the right and the top (“D2” and “D3” directions in Kim). As also discussed in § V.A, neither the figures nor the specification in Kim indicates whether the filling insulation layer extends beyond the stack structure in the direction perpendicular to Fig. 4A below (the D1 direction).

FIG. 4A



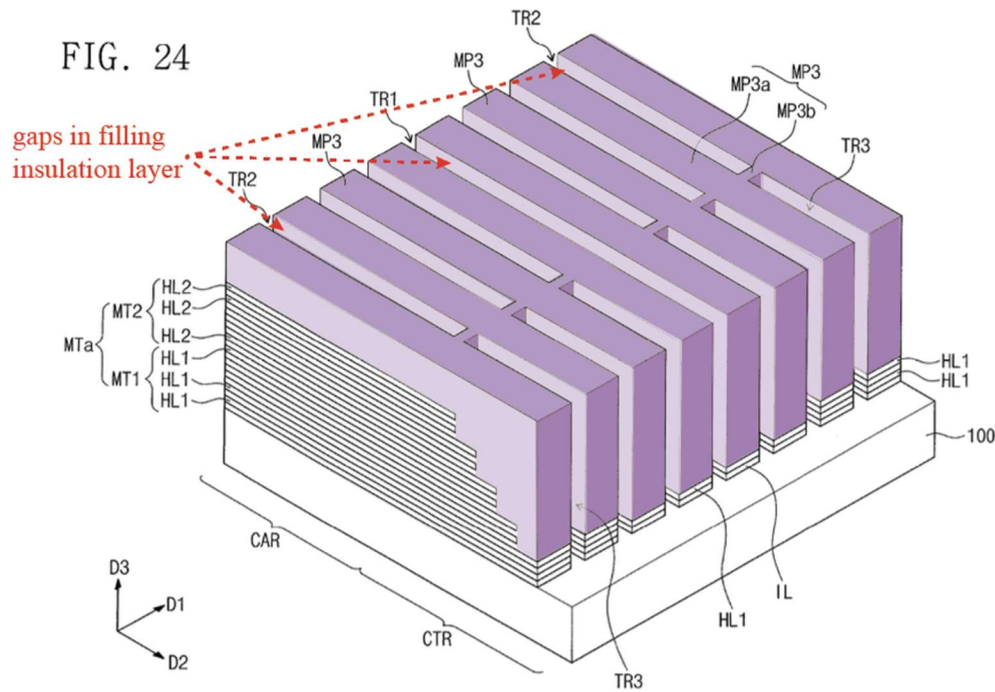
Ex. 1005, Fig. 4A (annotated).³ As a result, Kim does not disclose that the filling insulation layer surrounds the staircase structure. Kim at most discloses that the filling insulation layer covers the staircase from the top and one side.

Petitioner argues that “[b]ecause Kim discloses depositing the filling insulating layer onto ‘substrate 100’ to cover the stacks and planarizing the material on the top surface, this means that the filling material will encase the memory device.” Pet. 35 (citing Ex. 1003, ¶ 112). Petitioner, however, fails to explain why Kim’s disclosure means the filling material will encase the memory device. Planarizing

³ Figure 4A is a “cross-sectional view[] taken along line[] I-I’ ... of FIG.3” which runs along the direction D2 in the connection region (CTR) and direction D1 in the cell array region (CAR). See Ex. 1005, Fig. 3, 4:21-22.

simply refers to making the uppermost layer flat; it does not suggest that there is filling material on the sides of the staircase structure. Regardless of whether Kim's filling insulation layer "covers" the top surface of the stacks and is then planarized (made flat), Kim still does not disclose a filling insulation layer that encircles the stacks. Indeed, as shown above, Kim's filling insulation layer is deposited to the right and top of the staircase structure but not to the left, front, and back of the staircase structure.

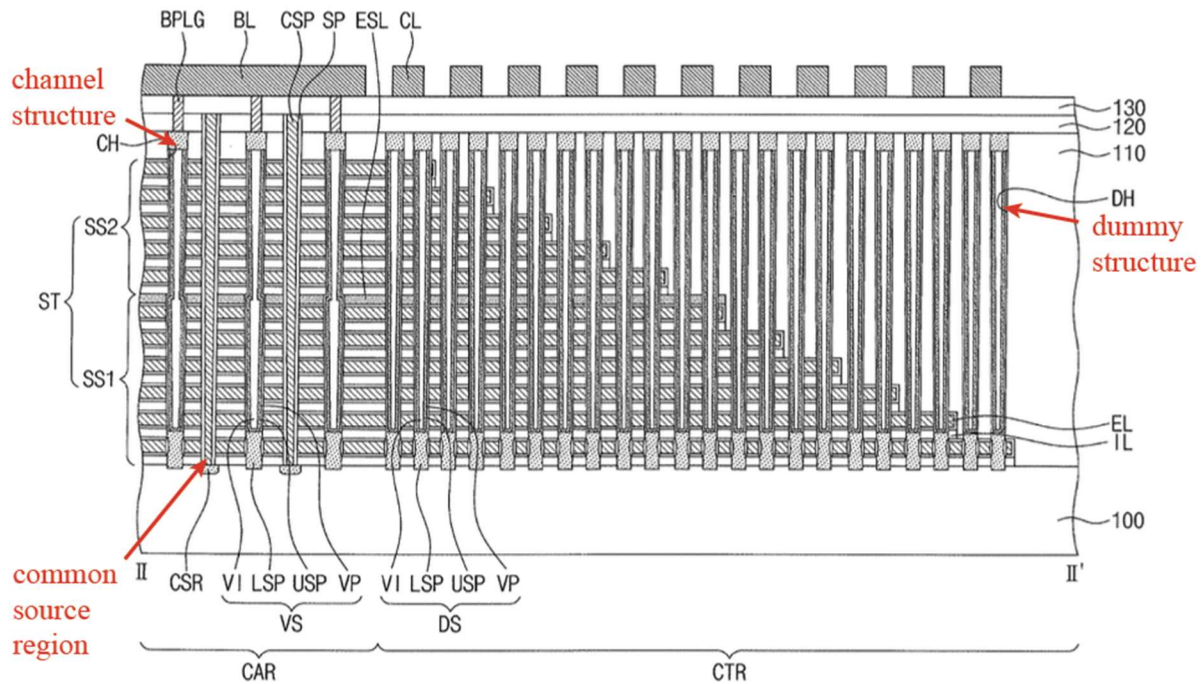
In its next argument, Petitioner asserts that a POSITA would have found it obvious that a structure that extends in one direction must also extend in a perpendicular direction. Pet. 35 ("[I]t would have been understood by a POSITA, and certainly obvious, that the filling material would extend to the outer edge in the other directions, namely, on the other three sides of the structure."). However, this argument is not only conclusory and based on hindsight, but it is also inconsistent with the evidence. For example, Kim's Figure 24, which shows the perspective view of the stack region, shows that the insulation layer is only on the top and one side. Indeed, the figure shows that in gaps where the staircase structure is absent, the **filling insulation layer** is also absent:



Ex. 1005, Fig. 24 (annotated).

And contrary to Petitioner's assertion, many of Kim's components extend in one direction and not others. To name just a few examples from components mentioned in § V.A, channel structures, dummy structures, and contact plugs extend in the D3 direction but not in D1 or D2; common source regions extend in D2 and D3 directions but not in D1.

FIG. 4B

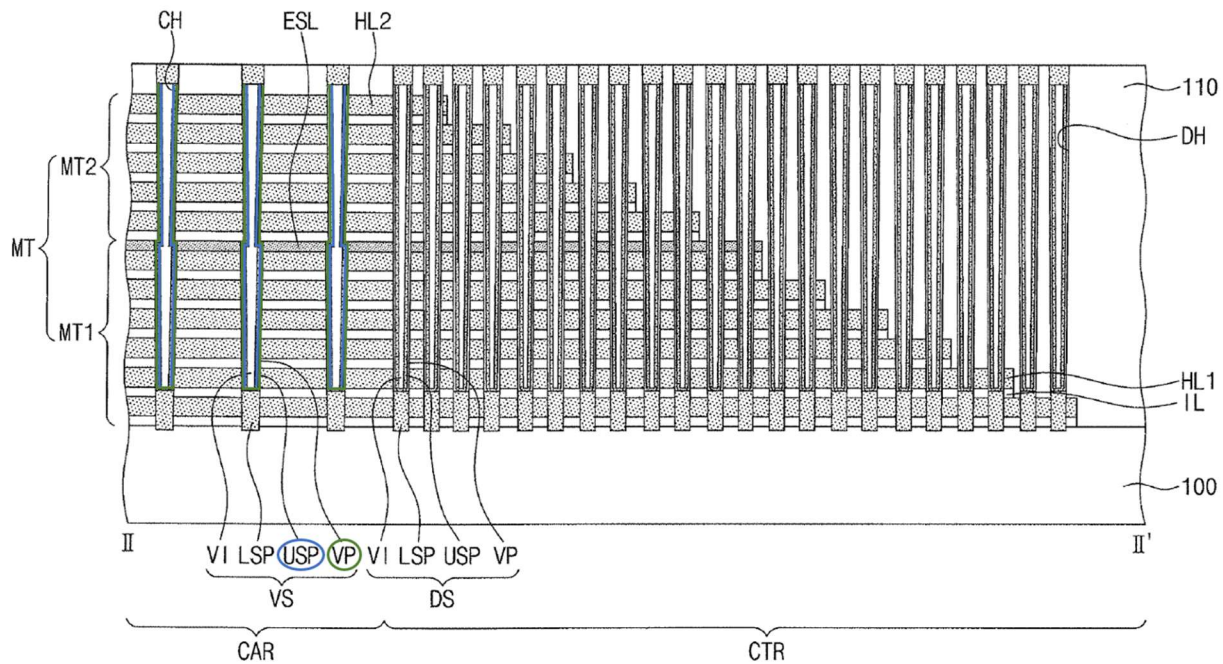


Ex. 1005, Figs. 3, 4A-B.

Petitioner's expert argues that chemical vapor deposition (CVD) is often used to deposit materials like Kim's insulation layer, and "is an isotropic process leading to deposition on all sides, except the bottom surface which is blocked." Ex. 1003, ¶ 113. However, Petitioner's expert omits that Kim teaches using CVD for localized deposition of material that results in localized, anisotropic structures. For example, Petitioner ignores that Kim discloses, in reference to Fig. 12 below, that "[e]ach of the vertical insulating layer VP and the upper semiconductor pattern USP may be formed using [...] a CVD process." Ex. 1005, 11:66-12:1. As seen in the annotated

Fig. 12 below, “vertical insulating layer VP” and “upper semiconductor pattern USP” are both highly localized and anisotropic components.

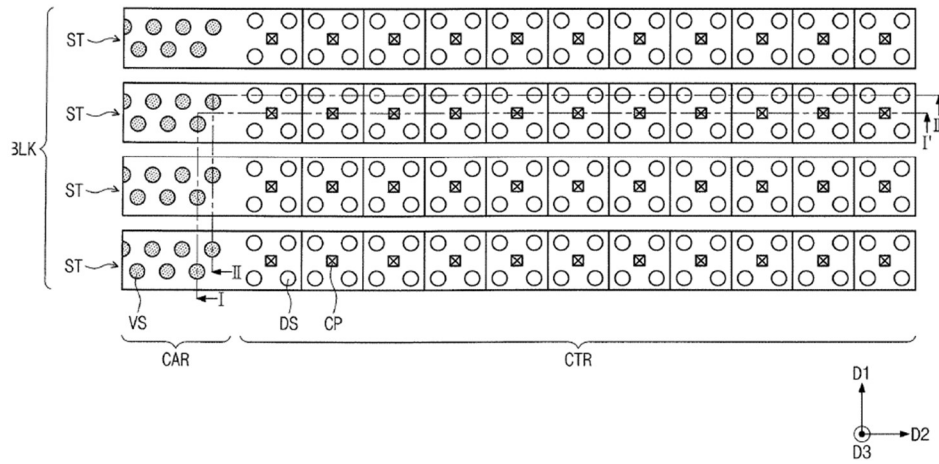
FIG. 12



Ex. 1005, Fig. 12 (annotated).

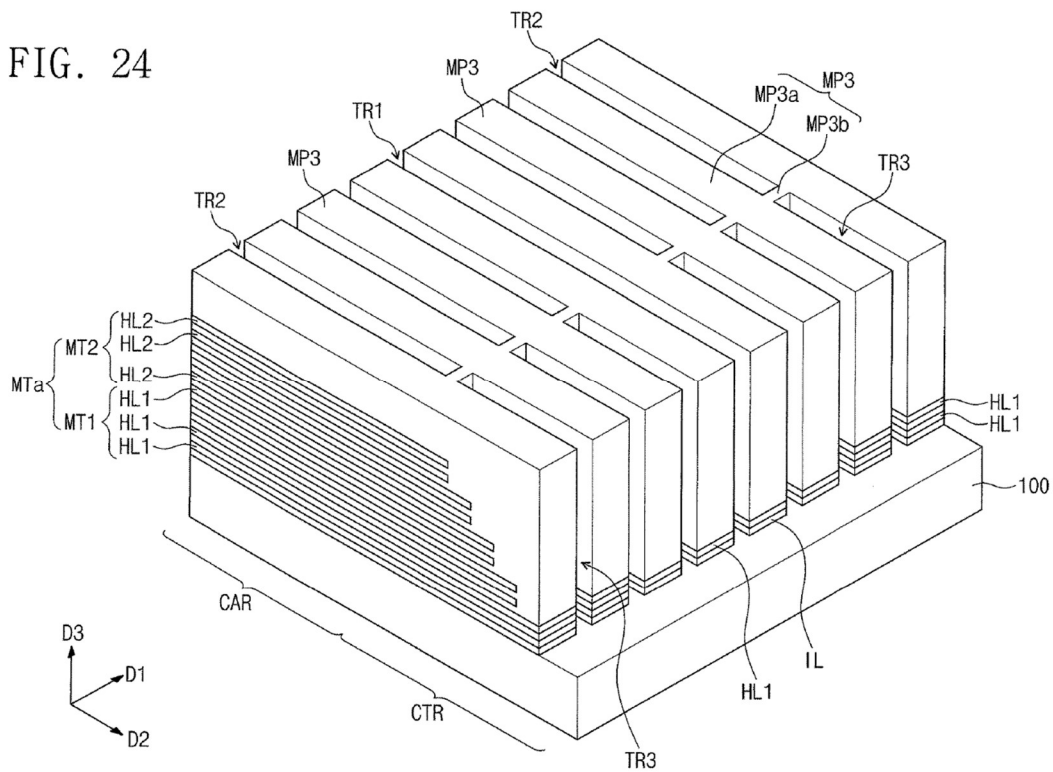
Petitioner’s expert also argues that “having uniform filling material on all sides would make for a symmetric device, which is generally desirable” (Ex. 1003, ¶ 113), but this ignores that Kim’s device is intentionally not symmetrical. For example, Kim’s device is different in the mutually perpendicular D1 and D2 directions, as depicted in the figures below.

FIG. 3



Ex. 1005, Fig. 3, *also* Pet. 36.

FIG. 24



Ex. 1005, Fig. 24.

As seen in the reproduced figures above, Kim's stack structure extends in the D2 direction and not in the D1 direction, and therefore Petitioner's allusions to Kim's device being symmetric or desiring symmetry are directly contradicted. In contrast, the '031 teaches a different device structure in which the staircase structure can "extend[] along the x-y plane" (instead of only extending along the x or y direction) and can "surround memory structure 1100 along the x-y plane." '031, 13:27-28 ("Dielectric pairs of different tiers can be etched to *form staircases extending along the x-y plane.*"); 22:30-32 ("First staircase region 1121 and second staircase region 1122 can each *surround memory structure 1100 along the x-y plane.*"). See also § IV.A.

Realizing that Kim's insulation layer does not surround the staircase structure, Petitioner goes beyond Kim's disclosures and attempts to bring in teachings from another reference to explain how Kim "would have been understood," but the teachings contradict Kim's disclosures. Petitioner relies on Park (Ex. 1011, "Park") to assert that "a common technique was to isolate the blocks with, e.g., common source lines 102" that have a "conductive core" and "an outer portion of insulating material." Pet. 36-37.

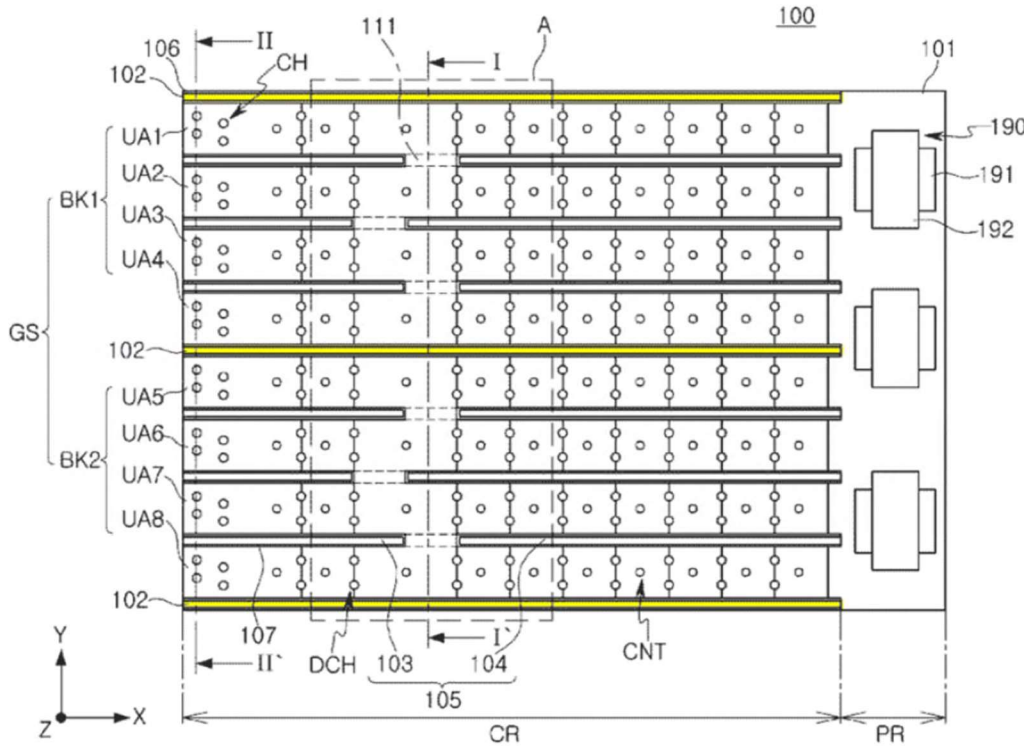


FIG. 3

Ex. 1011, Fig. 3 (annotated by Petitioner at Pet. 37). Petitioner’s expert argues that Park’s “common source lines are like a wall with the outer portions of that wall being the insulating liner.” Ex. 1003, ¶116. He further suggests that the same types of common source lines within insulating liner are present in Kim, extending in the D2 direction. Specifically, Petitioner’s expert asserts “[w]ith respect to Figure 3 of Kim, these common source lines run in direction 2 and surround the staircase and array regions along direction 2.” *Id.* Therefore, Petitioner asserts that “this additional insulating liner **surrounds** the multiple-stack structure.” Pet. 37 (emphasis original).

Petitioner’s reliance on Park for how Kim “would have been understood” is misplaced. First, Kim does not reference Park, Petitioner does not propose

combining Kim and Park, and Petitioner does not argue or establish that Park's teachings are the only way to implement Kim's teachings.

Second, Kim's common source regions and common source plugs are formed after the forming of the **filling insulation layer 110**, which is not disclosed to surround the stack structure; instead the common source regions and common source plugs simply divide the stack structure into blocks. Ex. 1005, Figs. 6-13, 12:15-33. As depicted below, after the deposition of the **filling insulation layer 110**, trenches TR are formed "between the mold structures MT" used to form the steps. Ex. 1005, 12:15-19. Kim's trenches are subsequently filled to form **common source regions CSR**. Ex. 1005, 12:9-33. Thus, even if Kim's common source regions is considered a filling structure, Kim still fails to disclose that the stack structure is encircled by the filling insulation layer 110 (or any other structure) at the ends of the device along the D1 direction.

FIG. 12

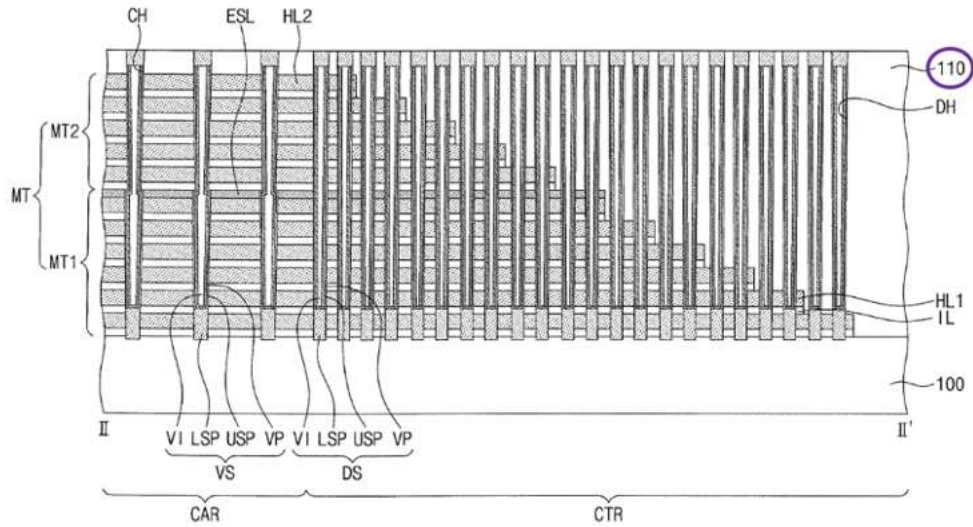
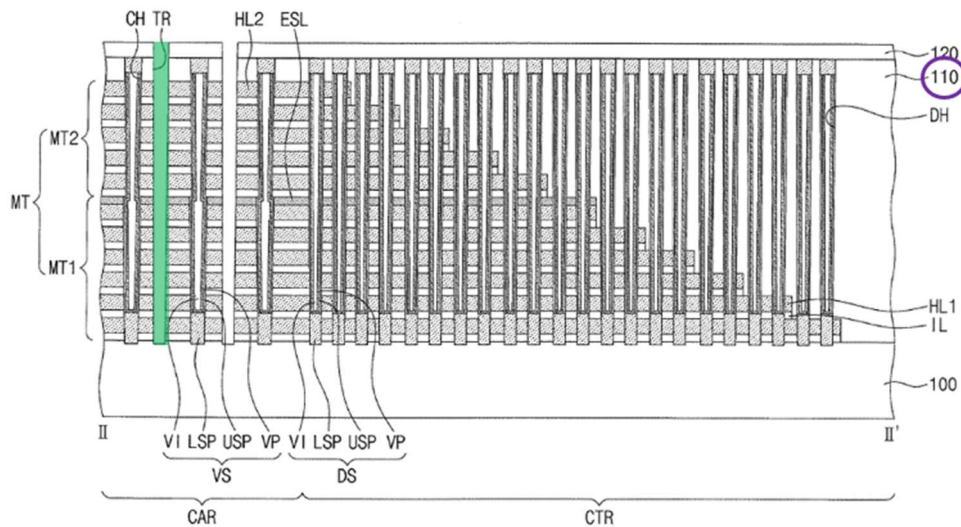


FIG. 13



Ex. 1005, Figs. 12-13 (annotated).⁴ And to the extent that Petitioner's argument is that the insulating liners of the common source in combination with the filling insulation layer 110 show the filling structure of the '031, this combination of

elements still fails to surround the stack structure. Kim's device in the D1 direction is neither depicted nor described.

Accordingly, Kim does not disclose or render obvious a filling structure "surrounding" a multiple-stack staircase structure, and the Board should find that Petitioner has failed to meet its burden of showing Kim discloses or renders obvious limitation [1.d] in Ground 1.

B. Ground 2: Petitioner Fails to Show That Tessariol Discloses or Renders Obvious "a Filling Structure Surrounding the Multiple-Stack Staircase Structure"

Petitioner fails to show that Tessariol discloses or renders obvious a filling structure "surrounding" a multiple-stack staircase structure because none of the features identified by Petitioner, either individually or in combination, encircles Tessariol's "steps." Limitation [1.d] recites "*a filling structure surrounding the multiple-stack staircase structure.*" As discussed in § IV.A, the term "surrounding" means "encircling." Tessariol does not disclose or render obvious a filling structure that surrounds the staircase structure. Petitioner seems to point to Tessariol's "insulating material 48," "dielectric material 74," and "insulator material 86" as the

⁴ Figures 12 and 13 are "cross-sectional views taken along line II-II' of FIG.3" which runs along the direction D2 in the connection region (CTR) and direction D1 in the cell array region (CAR). *See* Ex. 1005, Fig. 3, 4:29-32.

alleged filling structure (Pet. 66-69), but none of these components, individually or in combination, surrounds Tessariol's "steps."

First, Tessariol’s “insulating material 48” covers but does not surround Tessariol’s “steps.”

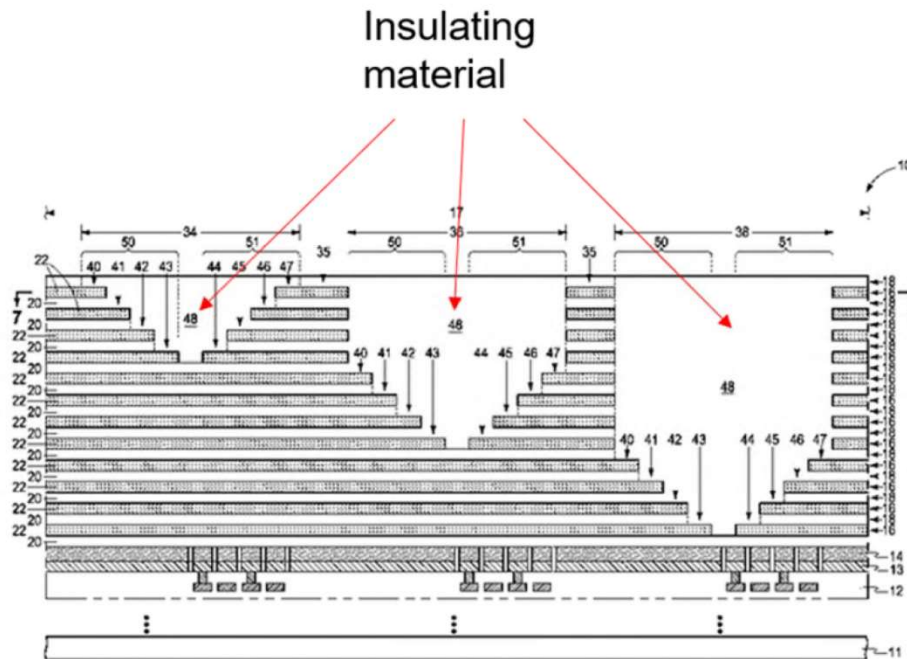


FIG. 6

Ex. 1006, Fig. 6 (annotated by Petitioner at Pet. 67). Tessariol discloses that “[a]n insulating material 48 (e.g., silicon dioxide and/or silicon nitride) is *above* steps 40-47.” Ex. 1006, [0034] (emphasis added). Tessariol recites similar language in its claims, disclosing “the stair step structure comprising insulating material *above* the steps.” Ex. 1006, Claims 1, 8, 16 (emphasis added). This is the full extent of Tessariol’s relevant disclosure. In Tessariol’s figures, **insulating material 48** is

depicted to be above the steps, and between **landings 35**, as seen in Fig. 6 (cross-section view) and Fig. 7 (top view) below.

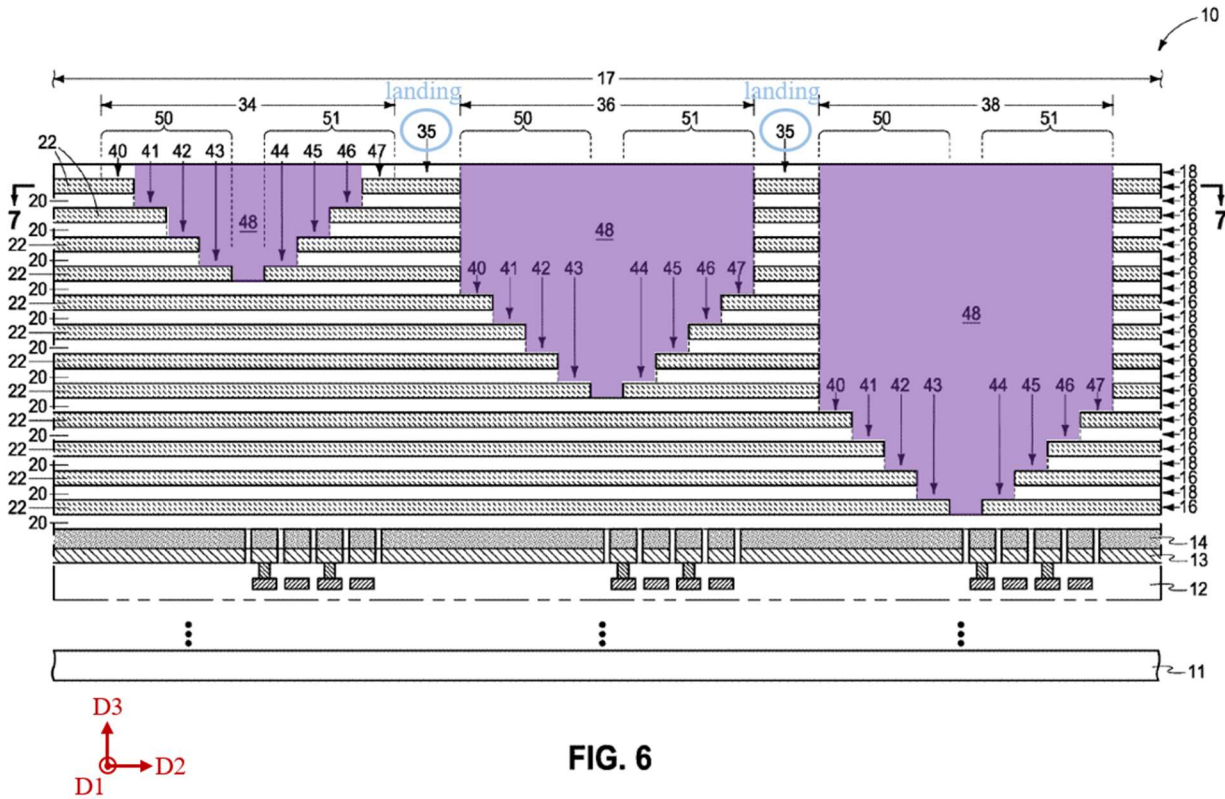


FIG. 6

Ex. 1006, Fig. 6 (annotated).

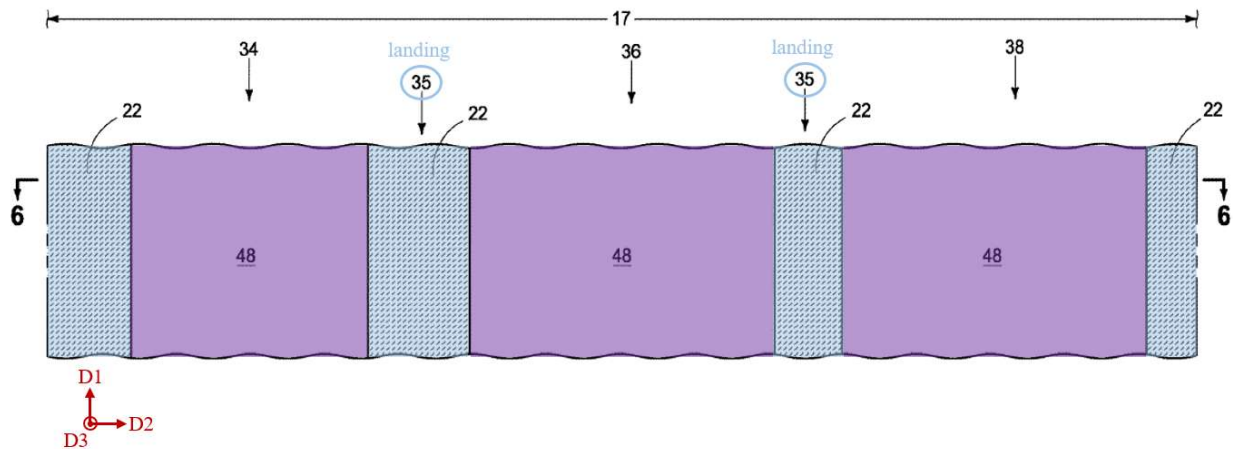


FIG. 7

Ex. 1006, Fig. 7 (annotated). As shown in Tessariol's Figs. 6-7, the steps are covered by **insulating material 48** from above and divided into "stadiums" by **landings 35** in the D2 direction.⁵ Ex. 1006, [0035]. However, as Petitioner's expert acknowledges in the declaration, "the figures in Tessariol do not show the outer ends/sides of the device" (i.e., in the D1 and D2 directions in Fig. 7). Ex. 1003, ¶ 184; *see also* Pet. 70 ("Note that Tessariol does not expressly depict the lateral ends of the device."). Therefore, Tessariol does not disclose **insulating material 48** surrounding, or encircling, the steps.

Second, Tessariol's "dielectric material 74" divides but does not surround Tessariol's "steps."

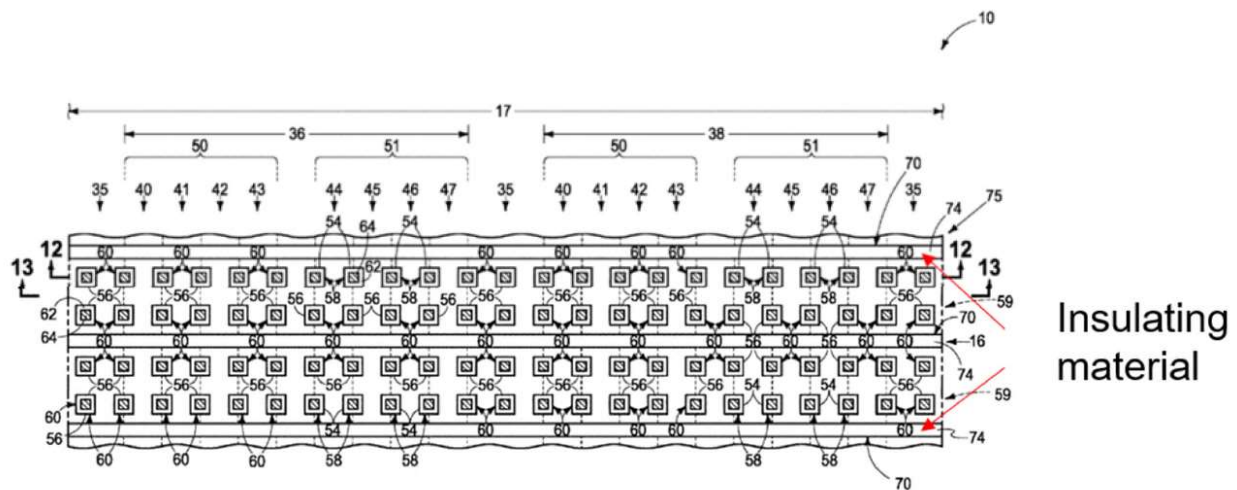


FIG. 11

⁵ The D1, D2, and D3 directions are defined in a way similar to the D1, D2, and D3 directions of Kim.

Ex. 1006, Fig. 11 (annotated by Petitioner at Pet. 68). Tessariol's **dielectric material 74** is formed in “trenches 70” that “extend elevationally into vertically-alternating tiers.” Ex. 1006, [0041], [0043].

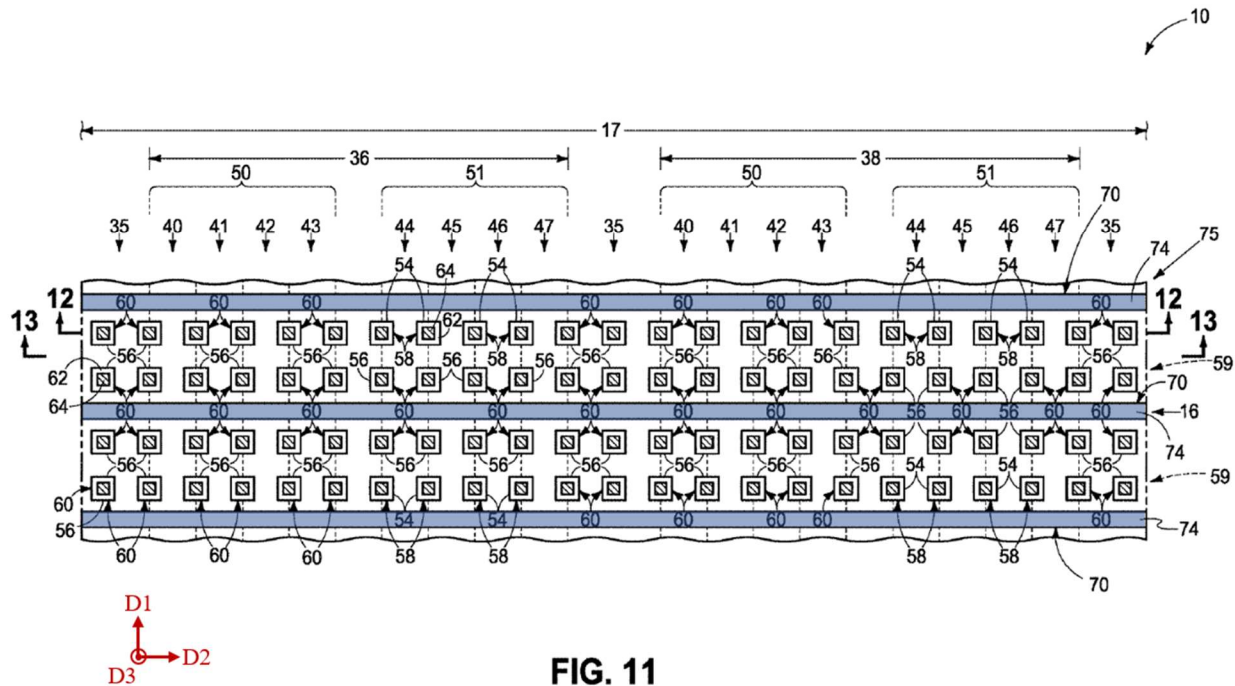
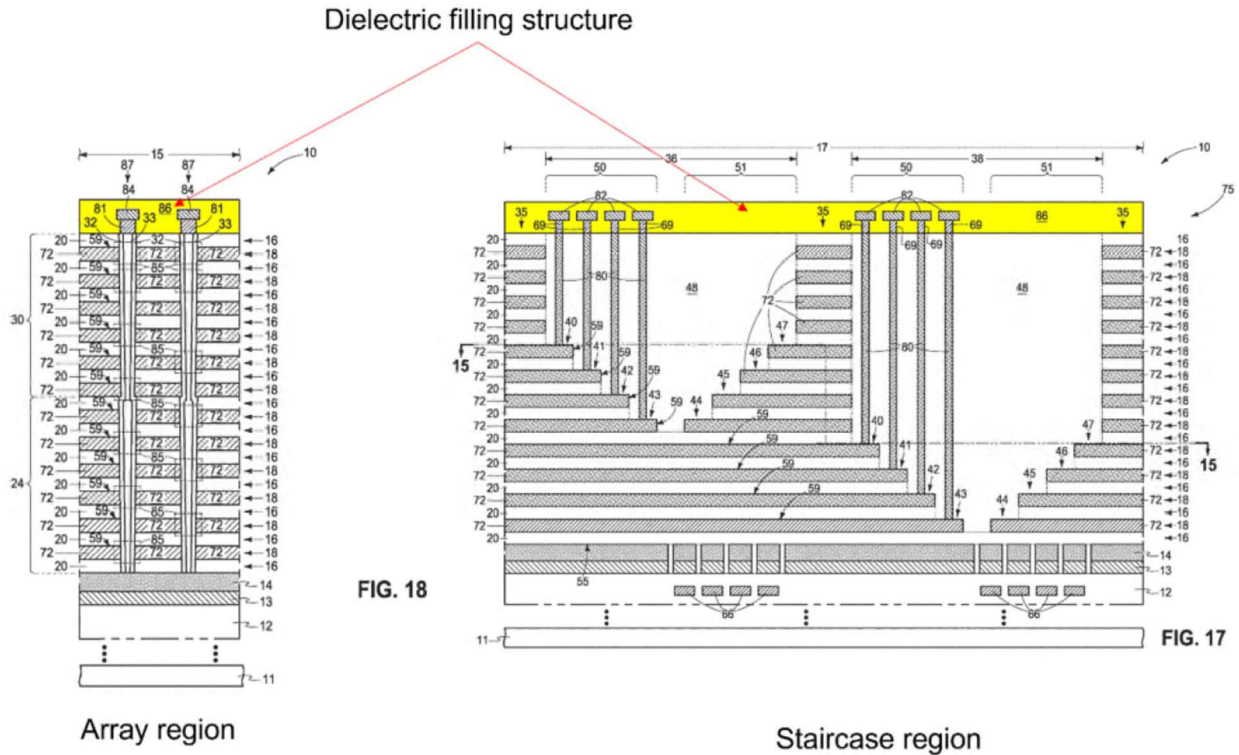


FIG. 11

Ex. 1006, Fig. 11 (annotated). Tessariol's “trenches 70” extend along the D2 direction and divide the alternating tiers along the D1 direction. Tessariol does not suggest that such a trench is present at the ends of the D1 direction. Thus, Tessariol fails to disclose that the stack is encircled by any structure at the ends of the device along either the D1 or D2 directions.

Third, Tessariol's “insulator material 86” covers but does not surround Tessariol's “steps.”



Ex. 1006, Figs. 17-18 (annotated by Petitioner at Pet. 69). As can be seen in the figures, the insulator material 86 covers the top surface of the stacks. However, insulator material 86 does not surround or encircle the staircase structure below—it covers, at most, the top surface. While Tessariol discloses that “[i]nsulator material 86 ... is shown surrounding components 69, 82, 81, and 84” (Ex. 1006, [0046]), which are “conductive extensions 69,” “conductive extensions 81,” “interconnect lines 82,” and “conductive lines 84,” all of these components are *above* the stacks, as seen in the figures above. Next, Petitioner’s expert again conflates planarizing with surrounding, declaring that “filling insulators are understood to surround the stack structures to create a planar surface for the upper-level metal layer.” Ex. 1003, ¶ 183 (citing Ex. 1023, 14). However, the cited exhibit is about planarization, and

does not include teachings about “encas[ing] all sides of the memory device,” as Petitioner’s expert alleges. Thus, his assertion regarding what was “conventional,” “routine,” and obvious, is conclusory, unsupported, and contradicted by Tessariol’s disclosures.

Petitioner’s argument that various combinations of “insulating material 48,” “dielectric material 76” within trenches, and/or “insulator material 86” teach the filling structure of the ’031 is wrong. Even the combination of Tessariol’s “insulating material 48,” “dielectric material 76” within trenches, and/or “insulator material 86” fails to surround the stack structure, as Tessariol does not teach or suggest an insulator material at the ends of Tessariol’s device in either the D1 or D2 direction.

Accordingly, Tessariol does not disclose or render obvious a filing structure “surrounding” a multiple-stack staircase structure. The Board should find that Petitioner has failed to meet its burden of showing Tessariol discloses or renders obvious limitation [1.d] in Ground 2.

C. Ground 3: Petitioner Fails to Show That Kim in view of Tessariol Discloses or Renders Obvious Dependent Claim 4

Petitioner fails to show that Kim in view of Tessariol discloses or renders obvious dependent claim 4 for the same reasons discussed above for Ground 1.

In Ground 3, Petitioner relies on Kim in view of Tessariol as allegedly rendering obvious dependent claim 4 of the ’031, which depends from claim 2,

which in turn depends from claim 1. As Petitioner acknowledges, “Ground 3 relies on the same disclosures as Ground 1 for claims 1 and 2, and [...] only addresses claim 4.” Pet. 86-87. Thus, Petitioner has failed to show that claim 4 is obvious for at least the same reasons as for Ground 1. Specifically, as explained in § VI.A (Ground 1), Petitioner fails to show that limitation [1.d] is disclosed or rendered obvious, and as a result, also fails in Ground 3.

D. Ground 4: Petitioner Fails to Show That Tessariol in view of Kim Discloses or Renders Obvious “a Filling Structure Surrounding the Multiple-Stack Staircase Structure”

Petitioner fails to show that Tessariol in view of Kim discloses or renders obvious a filling structure “surrounding” a multiple-stack staircase structure for the same reasons discussed above for Ground 2. In Ground 4, Petitioner relies on Tessariol in view of Kim as allegedly rendering obvious claims 1-2 and 4-5 of the ’031. However, the Petition does not raise any new arguments as to limitation [1.d] (“*a filling structure surrounding the multiple-stack staircase structure*”). See Pet. 90-96 (addressing only limitations [1.b], [1.f], and [1.h]). As explained in § VI.B, Petitioner fails in Ground 2 to show that limitation [1.d] is disclosed or rendered obvious by Tessariol, and since no additional arguments are introduced regarding this limitation, Petitioner also fails in Ground 4.

Accordingly, the Board should find that Petitioner has failed to meet its burden of showing that Tessariol in view of Kim renders obvious limitation [1.d] in Ground 4.

VII. CONCLUSION

For the foregoing reasons, Patent Owner respectfully requests that the Board deny institution.

Dated: July 29, 2024

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CERTIFICATE OF WORD COUNT

The undersigned certifies that the foregoing PATENT OWNER'S PRELIMINARY RESPONSE UNDER 37 C.F.R. § 42.107 complies with the type-volume limitation in 37 C.F.R. § 42.24(c)(1). According to the word-processing system's word count, the brief contains 6,822 words, excluding the parts of the brief exempted by 37 C.F.R. § 42.24(c).

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CERTIFICATE OF SERVICE

The undersigned certifies that the foregoing PATENT OWNER'S PRELIMINARY RESPONSE UNDER 37 C.F.R. § 42.107 was served in its entirety by filing through the Patent Trial and Appeal Case Tracking System (P-TACTS), as well as providing a courtesy copy via e-mail to the following attorneys of record for Petitioner listed below:

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