

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner,

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,
Patent Owner.

IPR2024-00790
Patent 10,868,031 B2

Before JO-ANNE M. KOKOSKI, KIMBERLY McGRAW, and
MICHAEL T. CYGAN, *Administrative Patent Judges*.

KOKOSKI, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

Micron Technology, Inc. (“Petitioner”) filed a Petition to institute an *inter partes* review of claims 1–5 of U.S. Patent No. 10,868,031 B2 (“the ’031 patent,” Ex. 1001). Paper 1 (“Pet.”). Yangtze Memory Technologies Company, Ltd. (“Patent Owner”) filed a Preliminary Response. Paper 8 (“Prelim. Resp.”).

Institution of an *inter partes* review is authorized by statute when “the information presented in the petition . . . and any response . . . shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” 35 U.S.C. § 314 (2018); *see also* 37 C.F.R. § 42.4 (2023). For the reasons discussed below, we determine that Petitioner establishes a reasonable likelihood of prevailing with respect to the unpatentability of at least one claim of the ’031 patent. Accordingly, we institute an *inter partes* review of claims 1–5 of the ’031 patent.

A. *Real Parties in Interest*

Petitioner identifies “Micron Technology Inc. and its subsidiaries, including Micron Consumer Products Group LLC” as the real parties in interest. Pet. 6. Patent Owner identifies itself as the real party in interest. Paper 4 (Mandatory Notice), 2.

B. *Related Matters*

The parties indicate that the ’031 patent is asserted in *Yangtze Memory Techs. Co., Ltd. v. Micron Tech. Inc.*, Case No. 3:23-cv-05792-RFL (N.D. Cal.). Pet. 6–7; Paper 4, 2.

C. *The ’031 Patent*

The ’031 patent, titled “Multiple-Stack Three-Dimensional Memory Device and Fabrication Method Thereof,” relates to “structures and methods

for forming a 3D memory device.” Ex. 1001, code (54), 8:63–64. The Specification teaches that “multiple dielectric stacks or multiple stacks of dielectric pairs (e.g., sacrificial material layer/insulating material layer pairs) are formed sequentially along a direction perpendicular to the surface of a substrate.” *Id.* at 7:25–28. The lower dielectric stack closest to the top surface of the substrate is formed first, sub-channel holes and sub-pillar holes are formed therein, and a patterning process is performed to form a staircase structure (e.g., the lower staircase structure). *Id.* at 7:31–37. An upper staircase structure is formed over the lower staircase structure, with sub-channel holes and sub-pillar holes that align and join with the sub-channel holes and sub-pillar holes in the lower staircase structure. *Id.* at 7:37–44. The upper staircase structure and the lower staircase structure form a multi-stack staircase structure, with the adjoined sub-channel holes and sub-pillar holes “filled with suitable materials to form semiconductor channels and supporting pillars, respectively.” *Id.* at 7:44–49. The supporting pillars “can include one or more connection portion formed by the adjoining sub-pillar holes,” and “[t]he sidewall can thus have unaligned (or disjointed) surfaces at the connection portions.” *Id.* at 8:35–41.

Figure 3 is reproduced below.

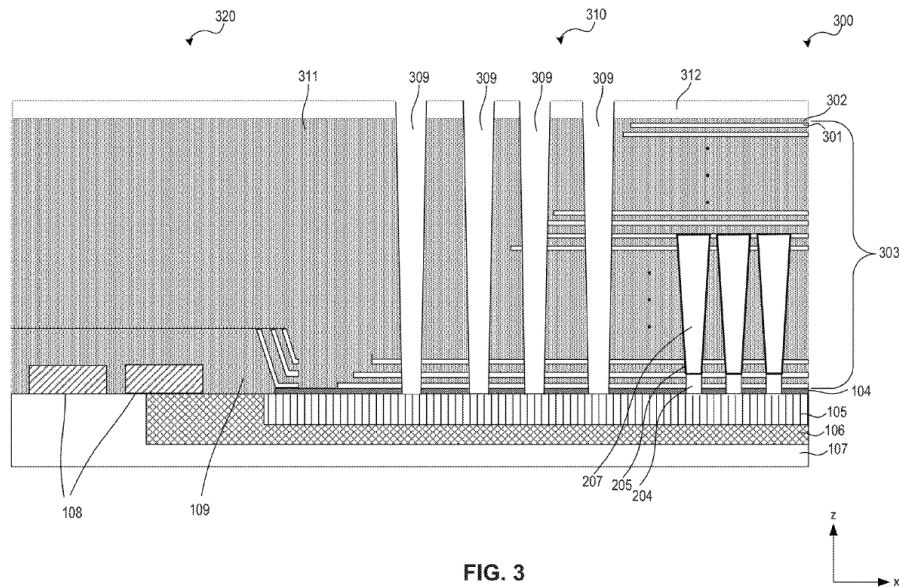


Figure 3 is an illustration of a cross-sectional view of a 3D memory device at a stage of the fabrication process. Ex. 1001, 5:24–26. Memory structure 300 includes two-stack staircase structure 303, dielectric filling structure 311, and plurality of pillar holes 309. *Id.* at 13:11–17. The Specification explains that “[d]ielectric filling structure 311 is deposited in periphery region 320 and core region 310 to fill in the space” created by removing portions of the dielectric stack to form stair case structure 303. *Id.* at 13:36–41. A suitable planarization method “can be performed to remove any excessive dielectric filling material overlying the topmost surface of staircase structure 303,” and “[t]he remaining portion of the deposited dielectric filling material (e.g., over staircase structure 303 and isolation layer 109) can form dielectric filling structure 311 that surrounds staircase structure 303.” *Id.* at 13:41–48.

Figure 4 is reproduced below.

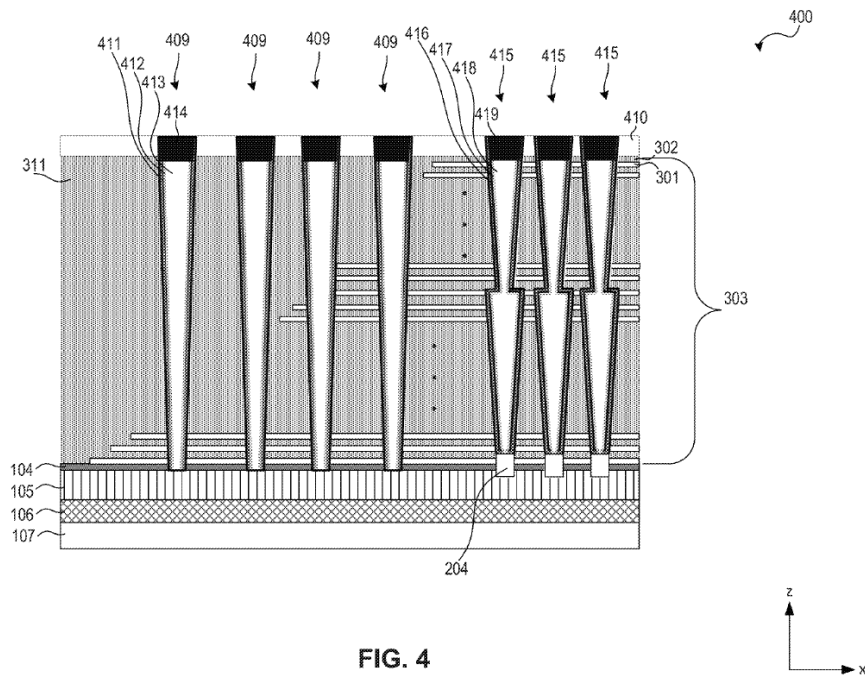


Figure 4 illustrates memory structure 400 formed based on memory structure 300 depicted in Figure 3 above. Ex. 1001, 14:35–36. “[M]emory structure 400 can be formed by forming a plurality of second sub-channel holes over first sub-channel holes 205 [shown in Figure 3], filling the first and second sub-channel holes and pillar holes 309 to form semiconductor channels 415 and supporting pillars 409” along with “drain regions 419 over semiconductor channels 415 and dummy drain regions 404 over supporting pillars 409.” *Id.* at 14:37–43.

D. Illustrative Claim

Petitioner challenges claims 1–5 of the ’031 patent. Claim 1, the only independent claim challenged, is illustrative of the claimed subject matter and is reproduced below.

1. [1.PRE] A memory device, comprising:
[1.A] a substrate;

- [1.B] a multiple-stack staircase structure comprising a plurality of staircase structures stacked over the substrate, [1.C] wherein each of the plurality of staircase structures comprises a plurality of conductive layers, wherein each of the plurality of conductor layers is located between two insulating layers;
- [1.D] a filling structure surrounding the multiple-stack staircase structure;
- [1.E] a semiconductor channel extending through the multiple-stack staircase structure, [1.F] wherein the semiconductor channel comprises unaligned sidewall surfaces; and
- [1.G] a supporting pillar extending through at least one of the multiple-stack supporting structure and the filling structure, [1.H] wherein the supporting pillar comprises aligned sidewall surfaces.

Ex. 1001, 26:15–32 (bracketed material added).

E. Asserted Grounds

Petitioner asserts that claims 1–5 would have been unpatentable on the following grounds:

Claim(s) Challenged	35 U.S.C. §	Reference(s)/Basis
1–4	103 ¹	Kim ²
1, 2, 4, 5	103	Tessariol ³
4	103	Kim, Tessariol
1, 2, 4, 5	103	Tessariol, Kim

¹ The Leahy-Smith America Invents Act (“AIA”), Pub. L. No. 112–29, 125 Stat. 284 (2011), revised 35 U.S.C. §§ 102 and 103 effective March 16, 2013. Because the ’031 patent has an effective filing date after March 16, 2013 (Ex. 1001, codes (22), (63)), we refer to the AIA version of Sections 102 and 103.

² Kim, US 10,381,369 B2, issued Aug. 13, 2019 (Ex. 1005).

³ Tessariol, US 2019/0081061 A1, published Mar. 14, 2019 (Ex. 1006).

Pet. 8. Petitioner relies on the Declaration of Sanjay Banerjee, Ph. D. (“Banerjee Dec.,” Ex. 1003) in support of its contentions.

II. ANALYSIS

A. *Level of Ordinary Skill in the Art*

Petitioner contends that a person of ordinary skill in the art (“POSITA”) would have had “a bachelor of science degree in electrical engineering or a similar discipline” with “2–3 years of professional experience working with (*e.g.*, researching, designing, or teaching) monolithic 3D structures and NAND memory devices,” or “an equivalent level of skill, knowledge, and experience (*e.g.*, an advanced degree may replace some of the professional experience).” Pet. 22–23. Petitioner further contends that a “POSITA would have been aware of and generally knowledgeable about 3D NAND’s structure, its component parts, how it operates, and how it is controlled.” *Id.* at 23 (citing Ex. 1003 ¶¶ 41–44). At this stage of the proceeding, Patent Owner neither responds to Petitioner’s proposed definition, nor provides a definition of its own. *See generally*, Prelim. Resp. Petitioner’s undisputed proposed definition appears to be consistent with the cited prior art and the disclosure of the ’031 patent, and we adopt it for purposes of this Decision. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001) (explaining that specific findings regarding ordinary skill level are not required “where the prior art itself reflects an appropriate level and need for testimony is not shown” (quoting *Litton Indus. Prods., Inc. v. Solid State Sys. Corp.*, 755 F.2d 158, 163 (Fed. Cir. 1985))).

B. *Claim Construction*

We construe each claim “in accordance with the ordinary and customary meaning of such claim as understood by one of ordinary skill in

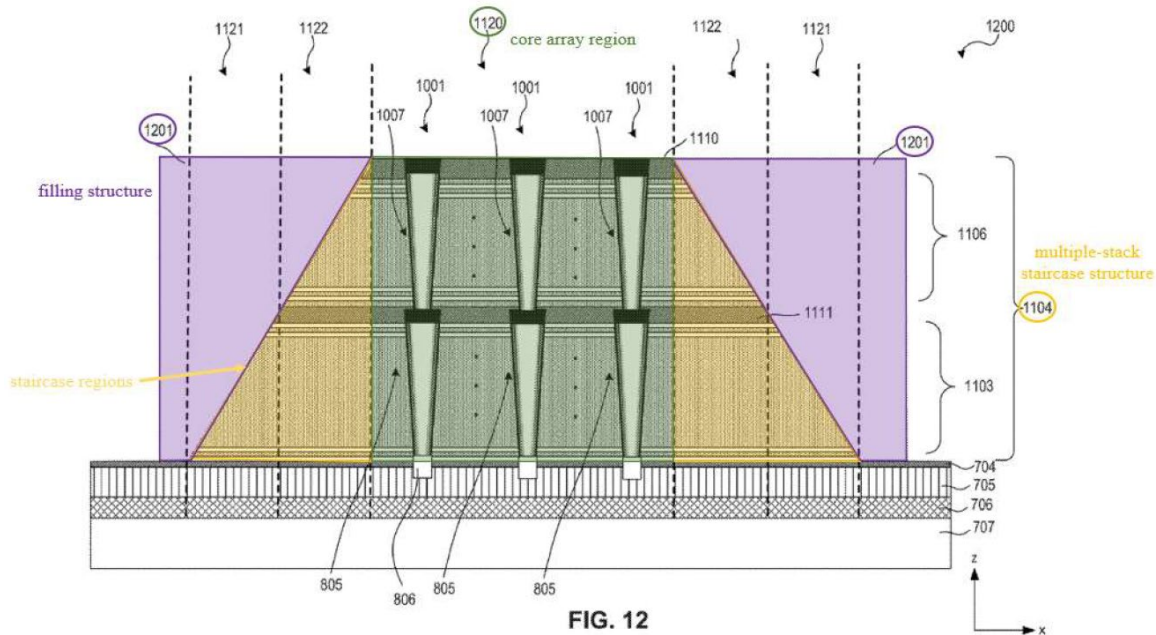
the art and the prosecution history pertaining to the patent.” 37 C.F.R. § 42.100(b). Under this standard, claim terms are generally given their plain and ordinary meaning as would have been understood by a person of ordinary skill in the art at the time of the invention and in the context of the entire patent disclosure. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1313 (Fed. Cir. 2005) (en banc). Only those terms in controversy need to be construed, and only to the extent necessary to resolve the controversy. *Realtime Data, LLC v. Iancu*, 912 F.3d 1368, 1375 (Fed. Cir. 2019).

Petitioner contends that “the terms of the ’031 Patent’s claims do not require further construction and can be afforded their plain and ordinary meaning.” Pet. 22 (citing Ex. 1003 ¶¶ 76–77). Patent Owner proposes a construction for the term “surrounding” in claim 1. Prelim. Resp. 12–16.

1. “surrounding”

Claim 1 recites, in relevant part, “a filling structure surrounding the multiple-stack staircase structure.” Ex. 1001, 26:24–25. Patent Owner argues that “surrounding” “should be construed according to its plain and ordinary meaning as to be all the way around (something)—in other words, encircling.” Prelim. Resp. 12. Patent Owner cites to several dictionary definitions to support its contention that this is the plain meaning of “surrounding,” and contends that “[t]he claims use the term ‘surrounding’ instead of narrower alternatives, such as ‘covering’ or the concept of being ‘between’ two structures.” *Id.* at 13 (citing Exs. 2001–2004).

Patent Owner provides an annotated version of the '031 patent's Figure 12 (reproduced below) to illustrate its contentions.



Id. at 13–14. Annotated Figure 12 is an illustration of a cross-sectional view of a 3D memory device described in the '031 patent, with Petitioner's addition of purple shading to area 1201, labeled "filling structure," yellow shading to component 1104, labeled "multiple-stack staircase structure," and green shading to area 1120, labeled "core array." *Id.* After noting that "Fig. 12 has labels provided for x and z directions, and the y direction is perpendicular to both directions and points into the page," Patent Owner contends that "staircase regions ('first staircase region 1121' and 'second staircase region 1122') are shown to extend in the +x and -x directions" and "[t]he '031 [patent] makes clear that the staircase regions also extend in the +y and -y directions, and therefore 'surround' the memory structure." *Id.* at 13–14 and n.2 (citing Ex. 1001, 13:27–28, 22:30–32). Patent Owner also contends that the '031 patent "uses the term 'surrounding' consistently as

‘encircling’ in multiple other instances.” *Id.* at 16 (citing Ex. 1001, 2:12–14, 15:49–57).

Petitioner argues that

[t]o the extent that [Patent Owner] argues that “surrounding” requires the dielectric filling structure to be on all sides of the multi-stack staircase structure, such an interpretation is inconsistent with all embodiments of the ’031 Patent, which never describes or illustrates the filling structure on each and every side of the multi-stack structure.

Pet. 34, 69. Patent Owner responds that its proposed construction “does not require filling structure on *all* sides of the multi-stack staircase structure—i.e., it does not require fil[l]ing structure on the top and bottom of the staircase structure.” Prelim. Resp. 16. Instead, Patent Owner argues, the ’031 patent “describe[s] the filling structure on all sides of the multi-stack structure in the horizontal plane—i.e., the filling structure encircles the multi-stack structure.” *Id.*

The ’031 patent teaches that “[s]taircase structure 303 can be formed by repetitively patterning/etching sacrificial material layers 201 and insulating material layers 202 of dielectric stack 203 in core region 310” and that the staircase extends along the x–y plane. Ex. 1001, 13:24–28.

The ’031 patent further teaches that “[d]uring the staircase-forming patterning process, the photoresist layer is repeatedly trimmed (e.g., etched by a suitable dry etch and/wet etch) along various directions (e.g., the x axis, the y axis, and the z axis) so dielectric pairs of dielectric stack 1003 can be repeatedly exposed.” *Id.* at 22:8–13. The ’031 patent also teaches that the first staircase region and the second staircase region “can each surround” the memory structure “along the x-y plane.” *Id.* at 22:30–33. The ’031 patent then teaches that the space created when the staircase structures are formed

is filled with a dielectric filling structure. *Id.* at 13:13–15, 22:63–65.

According to the '031 patent, the dielectric filling structure surrounds the multiple-stack staircase. *Id.* at 1:57–58 (stating in “some embodiments, the memory device also includes a filling structure surrounding the multiple-stack staircase structure”), 13:44–48 (discussing forming “dielectric filling structure 311 that surrounds staircase structure 303”).

These disclosures in the '031 patent indicate that the staircase structure is etched along the x-, y-, and z-axes, the dielectric filling structure fills the spaces in the x-, y-, and z-directions created when the staircase structure is etched, and the staircase structure surrounds the memory structure in the x-y plane. Therefore, based on the current record, it appears that the dielectric filling structure surrounds or encircles the staircase structure on four sides (front, back, left, and right) in the x-y plane. This understanding of “surround” is consistent with the way “surround” is used in the '031 patent and with the plain and ordinary meaning of “surround.” *See, e.g.*, 2:12–14 (“the supporting pillar is filled with at least one of an insulating material and a pillar-support material surrounded by the insulating material”), 10:25–27 (periphery region 120 “can surround core region 110” and “can also be under core region 110, depending on the type of the memory device”), 15:49–53 (“Charge trapping film 416 can also include a storage unit layer (memory layer) over and surrounded by the block dielectric layers for trapping charges and forming a plurality of charge storage regions along the z axis.”), 18:25–26 (“In some embodiments, the insulating liner/spacer layer surrounds the support material.”); Ex. 2001–2004.

Accordingly, and for purposes of this Decision, we determine that “surrounding” as used in claim 1 of the '031 patent means “encircling” or

“to be all the way around (something).” The parties are invited to address the construction of “surrounding” during trial.

C. Asserted Obviousness over Kim

Petitioner contends that claims 1–4 would have been obvious over Kim. Pet. 27–56.

1. Overview of Kim

Kim relates “to a three-dimensional (3D) semiconductor memory device with an improved integration density and a method for manufacturing the same.” Ex. 1005, 1:17–21. Figure 4B is reproduced below.

FIG. 4B

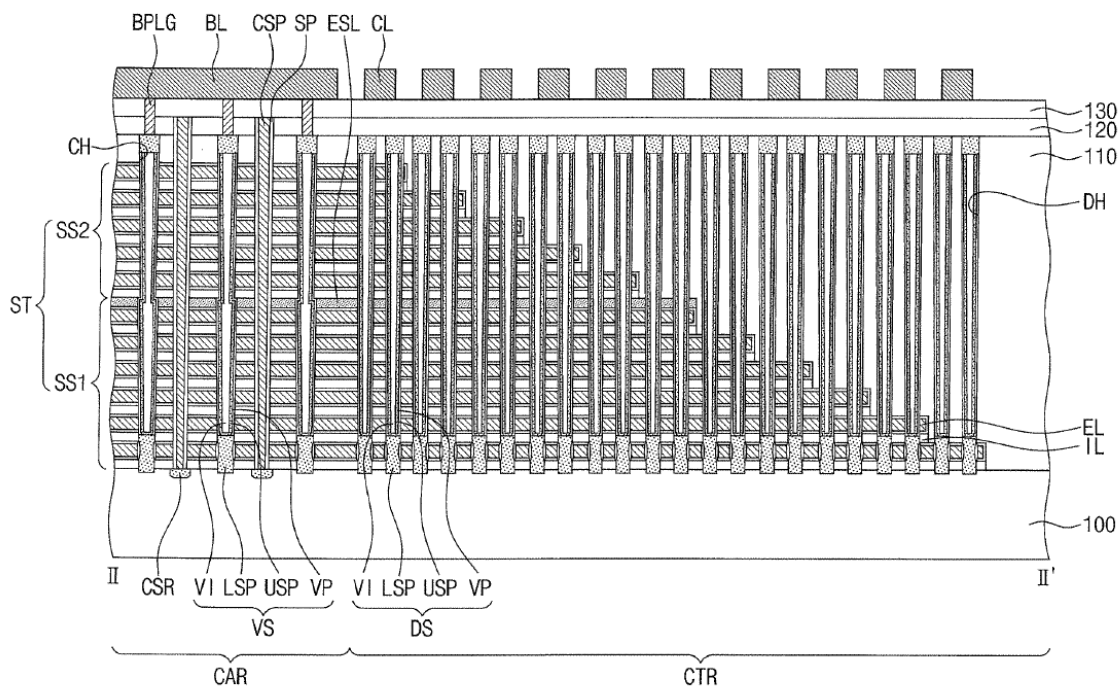


Figure 4B is a cross-sectional view of a 3D semiconductor memory device described in Kim. *Id.* at 4:21–22. Substrate 100 includes cell array region CAR and connection region CTR. *Id.* at 5:54–55. Stack structures ST includes lower structure SS1 and upper structure SS2, and “upper structure SS2 may be disposed on the lower structure SS1.” *Id.* at 5:65–6:1.

Common source regions CSR are provided in cell array region CAR, and are “disposed in the substrate 100 between the stack structures ST laterally adjacent to each other.” *Id.* at 6:11–14. Common source plug CSP is connected to common source region CSR and extend in parallel to stack structures ST. *Id.* at 6:24–27. Insulating spacers SP are disposed between common source plug CSP and stack structures ST. *Id.* at 6:27–29. Vertical structures VS are provided in each of channel holes CH and “may penetrate each of the stack structures ST on the cell array region CAR.” *Id.* at 7:4–8. Vertical structure VS includes vertical insulating layer VP, upper semiconductor pattern USP, lower semiconductor pattern LSP, and filling insulation pattern VI. *Id.* at 7:16–19. “The filling insulation layer 110 may be disposed on the substrate 100 and may cover the stack structure ST.” *Id.* at 9:53–54.

Kim teaches that “[p]lanar areas of the electrodes EL on the connection region CTR may increase sequentially as a distance from the top surface of the substrate 100 in the third direction D3 increases,” and the lowest electrode EL of stack structure ST “may have the largest planar area,” while the uppermost electrode EL of stack structure ST “may have the smallest planar area.” Ex. 1005, 6:63–7:3.

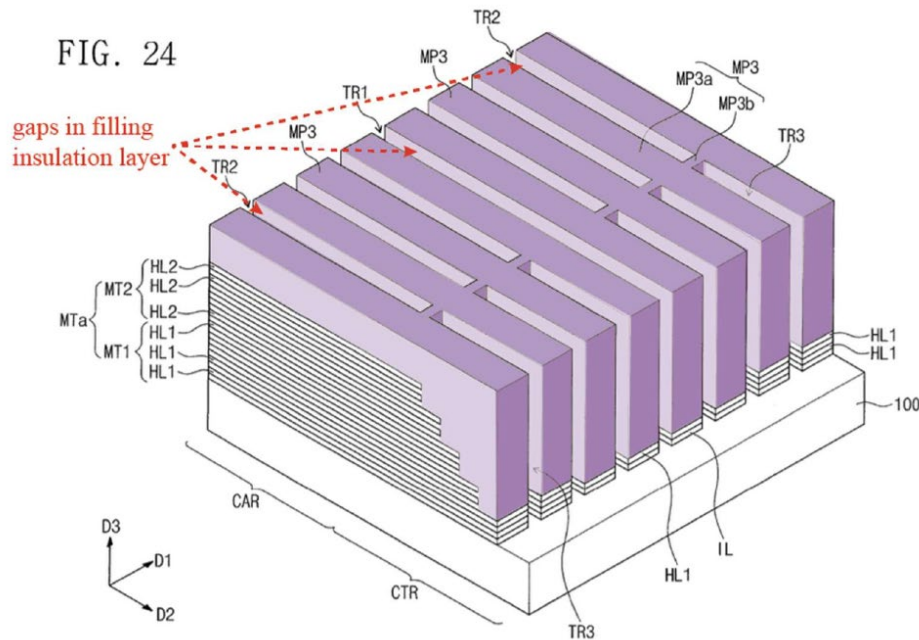
2. *Claim 1*

Petitioner contends that Kim teaches all of the limitations of claim 1. Pet. 27–47. For example, Petitioner contends Kim teaches “a substrate” (substrate 100), “a multiple-stack staircase structure comprising a plurality of staircase structures stacked over the substrate” (stack structure ST including lower substrate SS1 and upper substrate SS2), “each of the plurality of staircase structures comprises a plurality of conductor layers, wherein each of the plurality of conductor layers is located between two

insulating layers” (electrode layers EL and insulating layers IL), and “a semiconductor channel extending through the multiple-stack staircase structure” (vertical structure VS extending through stack structure ST). *Id.* at 27–31 (citing Ex. 1005, 5:60–6:1, 6:30–35, 6:41–63, 9:11–13, 9:39–41, 10:8–16, 10:50–59, 13:41–50, Figs. 4B, 12; Ex. 1003 ¶¶ 97, 99–106), 38–39 (citing Ex. 1005, 1:42–45, 5:1–3, 5:37–39, 7:15–24, Fig. 4B; Ex. 1003 ¶¶ 118–119).

With respect to limitation [1.D] (“a filling structure surrounding the multiple-stack staircase structure”), Petitioner contends that “Kim discloses a ‘filling insulating layer 110’ that ‘may be disposed on the substrate 100 and may cover the stack structures ST. The filling insulation layer 100 may have a planarized top surface.’” Pet. 32 (citing Ex. 1005, 9:53–56). Petitioner further contends that “after forming the staircase structures, the insulating layer 110 fills the voids.” *Id.* (citing Ex. 1005, 10:60–11:21, Figs. 9, 10).

Patent Owner responds that, “at most, Kim teaches covering the top and one side of the staircase structure.” Prelim. Resp. 21. Patent Owner provides an annotated version of Kim’s Figure 24, reproduced below, to illustrate its contentions.



Prelim. Resp. 26. Figure 24 is a perspective view illustrating a method of manufacturing a 3D semiconductor memory device described in Kim, to which Patent Owner adds purple shading and red arrows labeled “gaps in insulation layer.” Ex. 1005, 4:49–51. Patent Owner argues that, “as shown in Fig. 24 of Kim, the filling insulation layer does not cover three of the four sides (i.e., $-D2$, $+D1$, $-D1$) of its multiple-stack structure.” Prelim.

Resp. 21–22. Patent Owner notes that “Kim discloses that “[t]he filling insulation layer 110 may be disposed on the substrate 100 and may **cover** the stack structure ST,”” and “a filling insulation layer 110 may be formed on an entire top surface of the substrate 100 to **cover** the mold structure MT,” and argues that “[t]his is the full extent of Kim’s relevant disclosure, which says nothing to suggest that the insulation layer encircles the stack structures.”

Id. (citing Ex. 1005, 9:53–58, 11:11–13). Patent Owner argues that “Kim at most discloses that the filling insulation layer covers the staircase from the top and one side.” *Id.* at 24.

We are persuaded, on this record, that Petitioner adequately establishes that Kim teaches “a filling structure surrounding the multiple-step staircase structure” recited in limitation [1.D].

The main dispute between the parties, at this stage of the proceeding, is whether Kim’s filling insulation material surrounds Kim’s staircase structure. As set forth above, we construe “surrounding” to mean “encircling,” or “to be all the way around (something).” Section II.B.1, *supra*. Kim teaches that “filling insulation layer 110 may be formed on *an entire top surface* of the substrate 100 to cover the mold structure MT.” Ex. 1005, 11:11–13 (emphases added); *see also* 9:53–54 (“The filling insulation layer 110 may be disposed on the substrate 100 and may cover the stack structures ST.”). Prior to this step, mold structure MT is formed “on an entire top surface of a substrate” by vertically and alternately stacking insulation layers on the substrate, and mold structure MT is formed into a staircase structure. *Id.* at 10:8–11, 10:50–55, 10:60–63. Because Kim teaches that mold structure MT is formed on the entire top surface of the substrate, and filling layer 110 is also formed on an entire top surface of the substrate, it follows that filling layer 110 is also formed on the structures already present on the substrate, including the staircase structure in mold structure MT.

Moreover, Dr. Banerjee testifies that “Kim’s disclosure of depositing the filling insulation layer over ‘substrate 100’ to cover the stacks means that the filling material will encase the memory device.” Ex. 1003 ¶ 112. Dr. Banerjee states that providing filling material on all sides of the memory device “is consistent with traditional semiconductor fabrication processing and chip design techniques,” such as “PECVD (Plasma-Enhanced Chemical Vapor Deposition), which is often used for this purpose, [and] is an isotropic

process leading to deposition on all sides.” *Id.* ¶ 113. Because Chemical Vapor Deposition (“CVD”) is described in both the ’031 patent (Ex. 1001, 13:53–59) and in Kim (Ex. 1005, 10:17–20) as a mechanism for forming insulating layers, we credit Dr. Banerjee’s testimony that such deposition would lead to filling material that covers all sides, not just one side.

In this regard, Patent Owner’s argument that Kim’s CVD is used “for localized deposition of material that results in localized, anisotropic structures” is based upon attorney argument rather than testimony from the vantage point of one having ordinary skill in the art. PO Resp. 27–28 (citing Ex. 1005, 11:66–12:1, Fig. 12 (arguing that Kim teaches that “vertical insulating layer VP and the upper semiconductor pattern USP may be formed using [. . .] a CVD process” and “‘vertical insulating layer VP’ and ‘upper semiconductor pattern USP’ are both highly localized and anisotropic components”)). Moreover, a resulting structure that is localized may result from the patterning of the underlying structure; for example, Kim’s vertical insulating layer VP is formed in the “channel holes” created in a previous step, which does not inform whether CVD is isotropic or anisotropic, just that it adds material to the structures exposed to it. *See* Ex. 1005, 11:63–66 (“A vertical insulating layer VP and an upper semiconductor pattern USP may be formed to sequentially cover an inner side wall of each of the channel and dummy holes CH and DH.”). And, although Kim’s figures show filling material only on one side, they neither show nor describe that filling material is limited to one side, or that there is no filling material on the other sides of the structure that are undergoing the same processes. *See id.* at 11:11–13 (stating that insulation layer 110 covers the “entire top surface of substrate 100” not just one side of the top surface).

Even if Kim's Figure 24 shows that the filling insulation layer does not cover three of the four sides (i.e., -D2, +D1, -D1) of its multiple stack structure as Patent Owner contends, the result does not change on this record. As we understand it, Petitioner's arguments are based on the embodiment illustrated in Kim's Figures 3–16. Kim's Figure 24, however, relates to a different embodiment that is illustrated in Figures 17–20. *See* Ex. 1005, 17:15–18 (“FIGS. 21 to 24 are perspective views illustrating a method for forming the first staircase structure and the second staircase structure of the stack structure described with reference to FIGS. 17, 18, 19A, 19B, 20A, and 20B.”). Accordingly, Petitioner does not rely on Figure 24 with respect to limitation [1.D].

At this stage of the proceeding, Patent Owner does not address Petitioner's specific contentions with respect to the other limitations of claim 1. We reviewed Petitioner's contentions for all the elements of independent claim 1, as well as the supporting evidence. Pet. 27–47. Based on the record before us, we are persuaded that Petitioner's discussions of the particular structures and methods in Kim establishes a reasonable likelihood that Kim teaches or suggests all of the limitations of independent claim 1. *Id.*

3. *Claims 2–4*

Petitioner also contends that Kim teaches or suggests all of the limitations of claims 2–4 that depend, directly or indirectly, from claim 1. Pet. 47–56. At this stage of the proceeding, Patent Owner does not address Petitioner's contentions with respect to dependent claims 2, 3, and 4. We reviewed Petitioner's contentions with regard to claims 2–4, and are persuaded that Petitioner establishes a reasonable likelihood that Kim

teaches or suggests all of the limitations of these dependent claims as well.
Id.

D. Asserted Obviousness over Tessariol

Petitioner contends that claims 1, 2, 4, and 5 would have been obvious over Tessariol. Pet. 57–86. Patent Owner argues that Petitioner does not establish that Tessariol teaches or suggests “a filling structure surrounding the multiple-stack staircase structure” recited in claim 1. Prelim. Resp. 34–40. Having already determined that Petitioner establishes a reasonable likelihood of establishing that claims 1–4 would have been obvious over Kim, we need not address this ground in full. We offer the following comments in response to the parties’ arguments and evidence to provide guidance to the parties.

1. Overview of Tessariol

Tessariol is directed “to devices, to methods used in forming a circuit structure, and to methods used in forming an array of elevationally-extending transistors and a circuit structure adjacent thereto.” Ex. 1006 ¶ 1. Tessariol teaches construction 10 comprises base substrate 11 and various materials formed elevationally over base substrate 11. *Id.* ¶ 27.

Figure 6 is reproduced below.

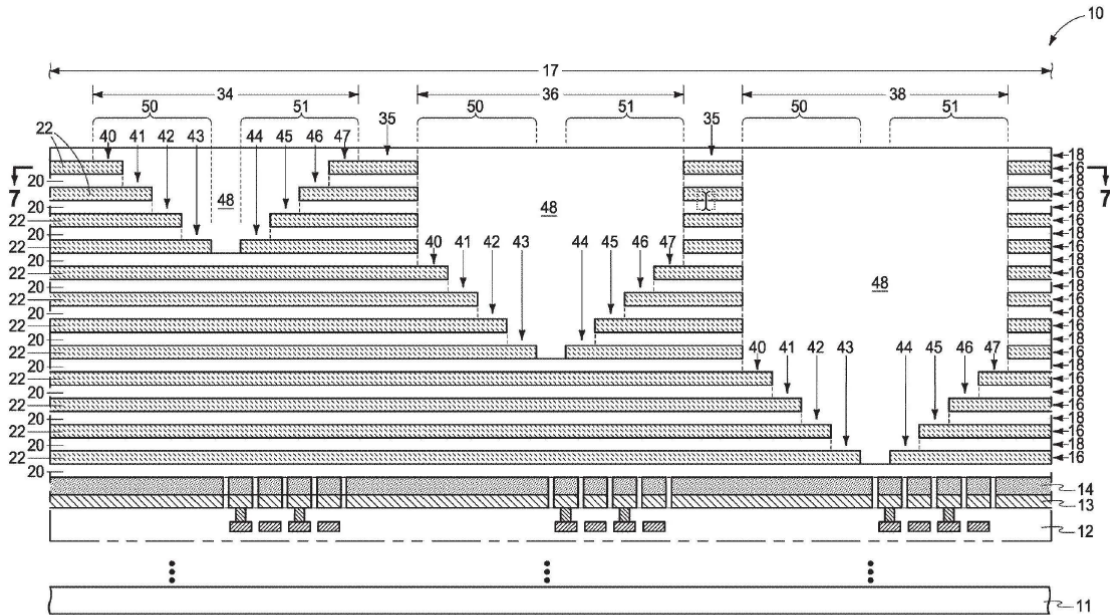


FIG. 6

Figure 6 is a diagrammatical cross-sectional view of a portion of the substrate construction in process as described in Tessariol. Ex. 1006 ¶ 13. Vertically-alternating tiers 16 and 18 of different composition first and second materials 20 and 22 are formed above substrate 11. *Id.* ¶ 29. Stair step structures 34, 36, and 38 individually comprise steps 40–47 and are separated from one another by an elevationally-outer landing 35. *Id.* ¶ 34. Insulating material 48 is above steps 40–47 in each of stair step structures 34, 36, and 38.

Figure 9 is reproduced below.

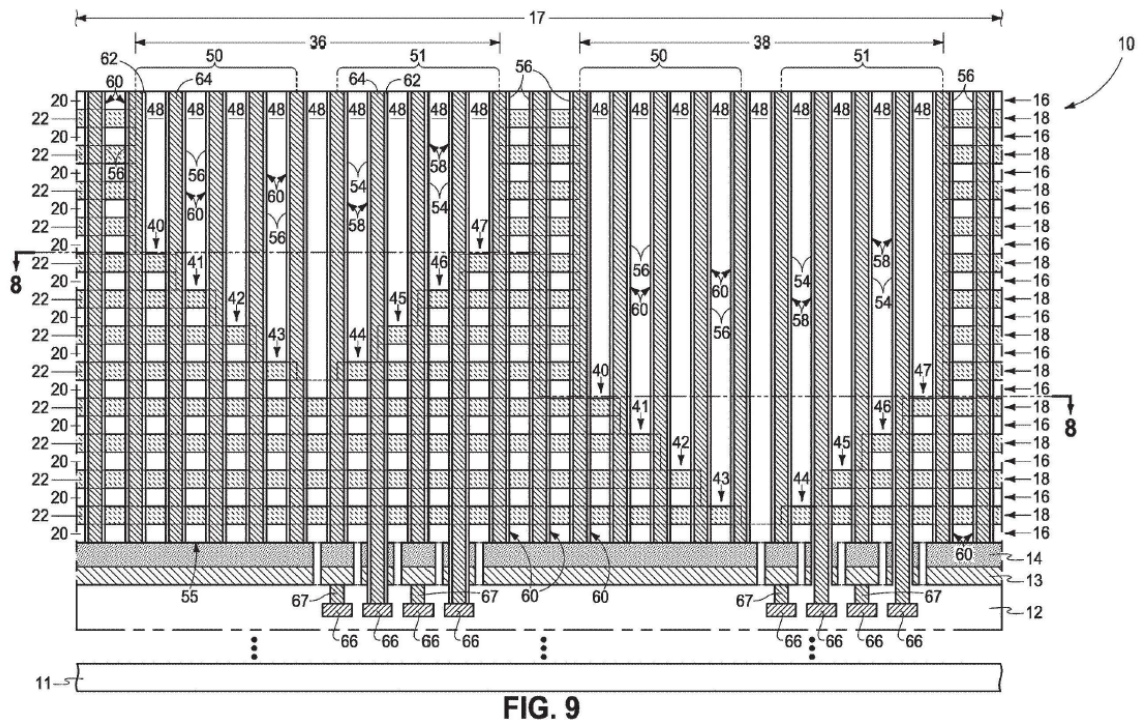


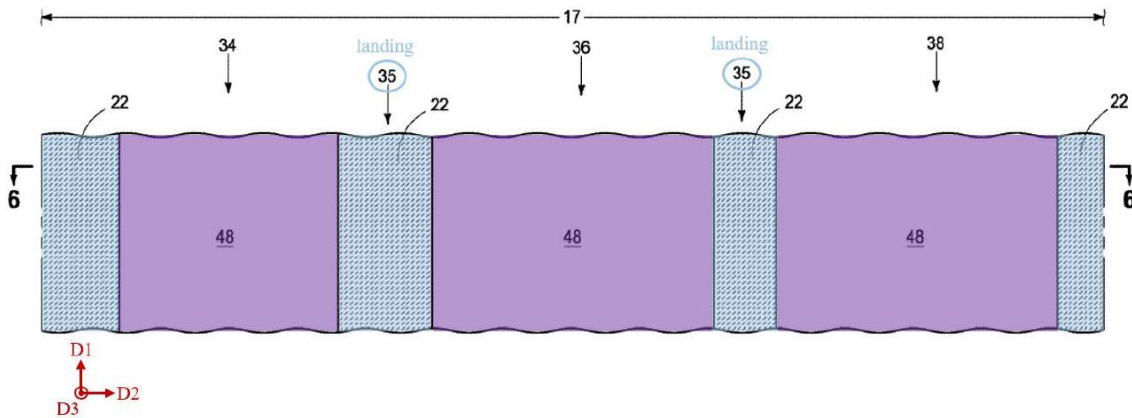
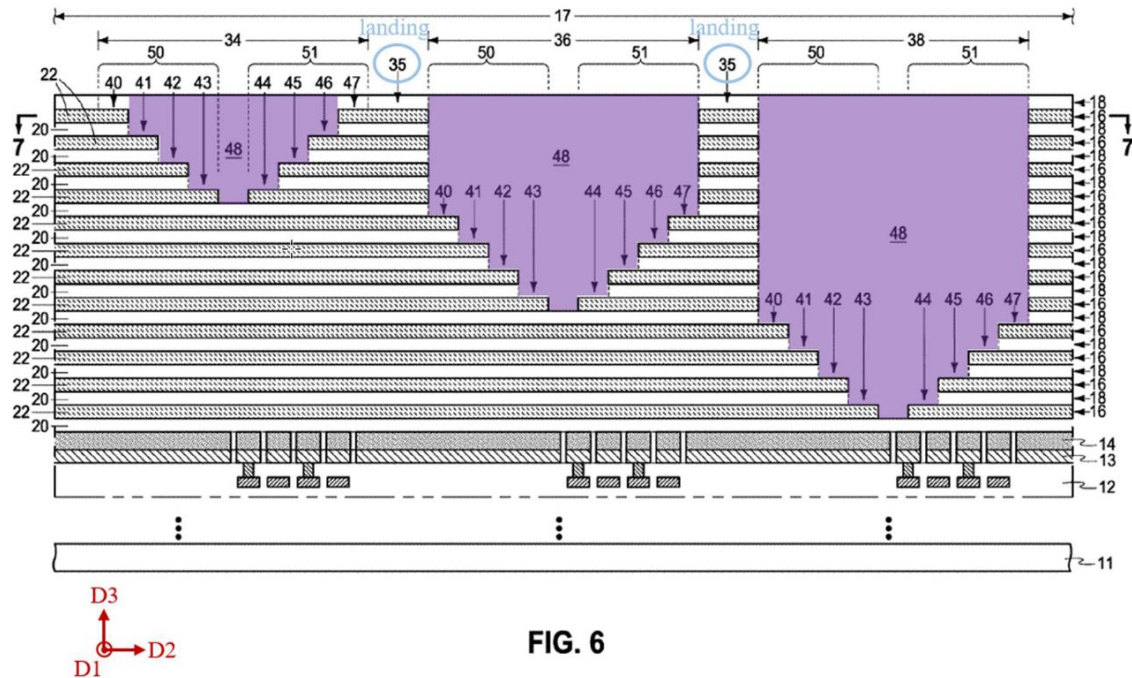
FIG. 9

Figure 9 is a diagrammatic cross-sectional view of a portion of a substrate construction in process as described in Tessariol. *Id.* ¶ 16. Dummy-structure openings 56 and via openings 54 are formed through insulating material 48 and vertically-alternating tiers 16 and 18. *Id.* ¶ 37. Operative conductive vias 58 are formed within via openings 54, and dummy structures 60 are formed within dummy-structure openings 56. *Id.* ¶ 38. Operative conductive vias 58 and dummy structures 60 comprise insulative lining 62 and conductive core 64. *Id.* Some alternate ones of operative conductive vias 58 are directly electrically coupled to individual conductive lines 66 through source material 14, conductive material 13, and conductive vias 67, and other alternate ones of operative conductive vias 58 are directly electrically coupled to individual conductive lines 66 through materials 14 and 13 to be directly against individual conductive lines 66. *Id.* ¶ 39.

2. *Claim 1*

With respect to limitation [1.D] (“a filling structure surrounding the multiple-stack staircase structure”), Petitioner contends that Tessariol teaches that insulating material 48 (e.g., silicon dioxide and/or silicon nitride) is above steps 40–47, and “additionally discloses the deposition of ‘dielectric material 74’ around the staircase structures,” which “may extend through the array region.” Pet. 66–68 (citing Ex. 1006 ¶¶ 34, 43, Figs. 6, 11). Petitioner also contends that Tessariol’s insulator material 86 that surrounds components 69, 81, 82, and 84 is a dielectric filling structure that “encases the entire stack structure to provide a region for metal layer connections to the lower layers.” *Id.* at 68–69 (citing Ex. 1006 ¶ 46, Figs. 17, 18; Ex. 1003 ¶¶ 179–181).

Patent Owner responds that “Tessariol does not teach or suggest an insulator material at the ends of Tessariol’s device in either the D1 or D2 direction.” Prelim. Resp. 40. First, Patent Owner argues that Tessariol’s insulating material 48 is above steps 40–47, and is depicted in Tessariol “to be above the steps, and between landings 35, as seen in Fig. 6 (cross-section view) and Fig. 7 (top view)” reproduced below. *Id.* at 36.



Tessariol’s Figure 6 (top) is a diagrammatic cross-sectional view of a portion of Tessariol’s substrate construction in process taken through line 6–6 in Figure 7, and Figure 7 is a diagrammatic cross-sectional view taken through line 7–7 in Figure 6, both with Petitioner’s addition of purple shading to insulating material 48 and labeling landings 35. Ex. 1006 ¶¶ 13–14; Prelim. Resp. 36. Patent Owner argues that annotated Figures 6 and 7 show “the steps are covered by insulating material 48 from above and divided into

‘stadiums’ by landings 35 in the D2 direction.” Prelim. Resp. 37 (citing Ex. 1006 ¶ 35).

Patent Owner further argues that “Tessariol’s ‘dielectric material 74’ divides but does not surround Tessariol’s ‘steps’” because “dielectric material 74 is formed in ‘trenches 70’” that “extend along the D2 direction and divide the alternating tiers along the D1 direction.” Prelim. Resp. 37–38 (citing Ex. 1006 ¶¶ 41, 43, Fig. 11). According to Patent Owner, Tessariol therefor “fails to disclose that the stack is encircled by any structure at the ends of the device along either the D1 or D2 directions.” *Id.* at 38. Patent Owner also argues that Tessariol’s insulator material 86 “covers the top surface of the stacks” but “does not surround or encircle the staircase structure below—it covers, at most, the top surface.” *Id.* at 39.

As set forth above, we construe “surrounding” to mean “encircling” or “to be all the way around (something).” Section II.B.1, *supra*. Thus, Petitioner must show that Tessariol’s insulating material 48, dielectric material 74, and insulation material 68 encircle, or are all the way around, Tessariol’s staircase structures. *Harmonic Inc. v. Avid Tech. Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016) (stating that it is Petitioner’s burden to show with particularity why a challenged claim is unpatentable); *see also* 37 C.F.R. § 42.104(b)(4) (A petition “must specify where each element is found in the prior art patents or printed publications relied upon.”). On this record, we find that Patent Owner’s arguments in this regard to have merit.

Petitioner and Dr. Banerjee acknowledge that Tessariol’s figures do not show the outer ends/sides of the described device. Pet. 70; Ex. 1003 ¶ 184. Tessariol teaches that insulating material 48 is above steps 40–47, which indicates that it covers the top of the steps. Ex. 1006 ¶ 34. Tessariol teaches that dielectric material 74 fills trenches 70, and trenches 70 are

“horizontally-elongated” and “formed to extend elevationally into vertically-alternating tiers 16, 18.” Ex. 1006 ¶¶ 41, 43. Based on these disclosures, we question whether “Tessariol additionally discloses the deposition of ‘dielectric material 74’ *around the staircase structures*” as Petitioner contends. Pet. 67 (emphases added). In particular, Petitioner does not adequately describe what parts or sections of the staircase structure dielectric material is deposited “around.” We also question Petitioner’s contention that insulator material 86 “encases the entire stack structure.” *Id.* at 68. Tessariol teaches that insulator material 86 “surround[s] components 69, 82, 81, and 84.” Ex. 1006 ¶ 46. With respect to components 69, 81, 82, and 81, Tessariol teaches:

Interconnect lines 82 have been formed above stair structures 36 and 38 and individually directly electrically couple together different individual conducting vias 80 to different individual operative conductive vias 58 through conductive extensions 69. . . . Strings 87 of transistors 85 may connect with individual conductive lines 84 through conductive extensions 81.

Id. Given these teachings in Tessariol, it is not clear that insulator material 86 “encases the entire stack structure.”

We invite the parties to develop these arguments further at trial, to the extent permitted by our rules.

E. Asserted Obviousness over Kim and Tessariol

Petitioner contends that claim 4 would have been obvious over the combined teachings of Kim and Tessariol. Pet. 86–89. Claim 4 ultimately depends from claim 1, and Patent Owner argues that claim 4 would not have been obvious over Kim and Tessariol for the same reasons set forth above with respect to Petitioner’s ground based on Kim alone. Prelim. Resp. 40–41. Having already determined that Petitioner establishes a reasonable

likelihood that claim 4 would have been obvious over Kim alone, we decline to address this ground. *See* Section II.C, *supra*.

F. Asserted Obviousness over Tessariol and Kim

Petitioner contends that claims 1, 2, 4, and 5 would have been obvious over the combined teachings of Tessariol and Kim. Pet. 90–96. Petitioner relies on the same arguments with respect to limitations [1.A], [1.C–E] and [1.G] as it does in its ground based on Tessariol alone. *Id.* at 90. Having already determined that Petitioner establishes a reasonable likelihood of establishing that claims 1–4 would have been obvious over Kim, we need not address this ground. However, we note that because Petitioner does not rely on Kim with respect to limitation [1.D], we have the same concerns with Petitioner’s arguments that Tessariol teaches limitation [1.D] here as set forth above with respect to Petitioner’s contentions based on Tessariol alone. *See* Section. II.D.2

III. CONCLUSION

Based on the arguments in the Petition and the Preliminary Response, and the evidence of record, we determine that Petitioner establishes a reasonable likelihood that it will prevail on its challenge to at least one claim of the ’031 patent. Accordingly, we institute an *inter partes* review of all the challenged claims on all the challenged grounds.

The factual findings set forth in this Decision are preliminary and provided for the sole purpose of deciding whether to institute a review. Any final findings will be based on the full trial record, including any information presented in a timely filed response to the Petition. *See Trivascular, Inc. v. Samuels*, 812 F.3d 1056, 1068 (Fed. Cir. 2016) (noting that “there is a significant difference between a petitioner’s burden to establish a ‘reasonable likelihood of success’ at institution, and actually proving

invalidity by a preponderance of the evidence at trial”) (quoting 35 U.S.C. § 314(a); comparing *id.*, with § 316(e)).

IV. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that an *inter partes* review is instituted with respect to all of the grounds asserted in the Petition; and

FURTHER ORDERED that, pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is hereby given of the institution of a trial, which shall commence on the entry date of this Decision.

IPR2024-00790
Patent 10,868,031 B2

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