

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,

Petitioner,

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,

Patent Owner.

Case No.: IPR2024-00790
U.S. Patent No. 10,868,031

PATENT OWNER'S RESPONSE
UNDER 37 C.F.R. § 42.120

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Ex. 2001	New Oxford American Dictionary, 3 rd Ed., 2010
Ex. 2002	The American Heritage® College Dictionary, 3 rd Ed., 2000
Ex. 2003	Webster’s II New College Dictionary, 3 rd Ed., 2005
Ex. 2004	Merriam-Webster’s Dictionary and Thesaurus, 5 th Printing, 2014
Ex. 2005	Declaration of Jonathan Bradford
Ex. 2006	Deposition Transcript of Dr. Banerjee
Ex. 2007	Micron’s Preliminary Claim Constructions (District Court)
Ex. 2008	Plaintiff’s Proposed Claim Constructions (District Court)
Ex. 2009	Gosset, “General review of issues and perspectives for advanced copper interconnections using air-gaps as ultra-low K material” (2003)
Ex. 2010	Harada, “Extremely Low Keff (1.9) Cu Interconnects with Air Gap Formed Using SiOC” (2007)
Ex. 2011	Ashby, Michael, “Materials Selection in Mechanical Design, Chapter 4, Material Property Charts” (4 th Ed. 2011)
Ex. 2012	Nitta, “Performance and reliability of airgaps for advanced BEOL Interconnects” (2008)
Ex. 2013	January 17, 2025, Declaration of Dr. Kuhn (“KuhnII”)
Ex. 2014	Electrical Conductivity, Wolfram Research
Ex. 2015	Young’s Modulus, Wolfram Research
Ex. 2016	Thermal Expansion Coefficients, Wolfram Research

LIST OF ABBREVIATIONS

Abbreviation	Term
'031 or '031 patent	U.S. Pat. No. 10,868,031
'031FH	File History of U.S. Pat. No. 10,868,031
Challenged Claims	Ex. 1001, Claims 1-5
Office	U.S. Patent and Trademark Office
Kim	U.S. Patent No. 10,381,369
Petition or Pet.	Petition for <i>Inter Partes</i> Review of U.S. Patent No. 10,868,031 (IPR2024-00790, Paper 1)
Parallel district court litigation	<i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc.</i> , NDCA-3-23-cv-05792 (N.D. Cal.)
Patent Owner or PO	Yangtze Memory Technologies Co. Ltd.
Petitioner	Micron Technology, Inc.
POSITA	Person of ordinary skill in the art
Tessariol	U.S. Patent Publication No. 2019/0081061

I. INTRODUCTION

The references in Petitioner's Grounds fail to disclose or render obvious the Challenged Claims of U.S. Patent No. 10,868,031 ("’031," Ex. 1001). For example, the art fails to disclose or render obvious "a filling structure surrounding the multiple-stack staircase structure" as required by limitation [1.d] of the sole challenged independent claim. In addition, the art fails to disclose or render obvious "a supporting pillar [that] is filled with ... a pillar-support material surrounded by the insulating material" as required by claims 4-5.

The ’031 is directed to a novel three-dimensional (3D) memory device having multiple stacks of word lines. Fabrication of 3D NAND memory devices generally involves stacks of alternating dielectric and sacrificial materials, which can be patterned in a staircase formation and with semiconductor channels and mechanical supports (supporting pillars) that help prevent deformation during the replacement of the sacrificial materials with conducting word lines. ’031, 1:23-38, 7:19-25. The prior art at the time of filing of the ’031 Patent used multiple patterning processes for the multiple stacks, which was "time-consuming and costly." ’031, 1:33-37, 7:57-62. The ’031 simplifies the fabrication process of these "multi-stack 3D NAND memory devices" by using a single patterning process for the multiple stacks. ’031, 1:33-37, 1:42-49, 9:15-18. The ’031 Patent's invention's novel design provides at least three benefits: (1) avoiding the use of different photomasks for each

dielectric stack in forming the supporting pillars and reducing cost and effort by decreasing the number of photomasks and photolithography operations needed; (2) processing on multiple stacks and thereby avoiding the quality issues that arise from processing on the lower structures before forming the upper stack(s); and (3) avoiding different dimensions for sub-pillar holes that result from multiple patterning processes, which complicates fabrication and required higher precision control. '031, 8:5-31.

The '031 introduced a 3D memory device in which the stacks of the device are “patterned by one staircase-forming patterning process to form the multiple-stack staircase structure.” '031, 8:63-9:1. The supporting pillars formed during the multiple staircase-forming patterning process of the prior art can result in pillars with “unaligned (or disjointed) surfaces at the connection portions”; in contrast, the '031's supporting pillars have “aligned sidewall surfaces,” as they are formed during one staircase-forming patterning process. '031, 8:32-53. The claimed invention recites “a filling structure that surrounds the multiple-stack staircase structure,” a “semiconductor channel [which] comprises unaligned sidewall surfaces,” and a “supporting pillar [which] comprises aligned sidewall surfaces.” *See* '031, Claim 1, 2:40-45, 8:48-53. As a result, the claimed invention avoids the issues arising from using multiple patternings and “improves device yield and performance.” '031, 9:1-28.

Petitioner fails to show that the prior art references disclose or renders obvious the Challenged Claims.

For Ground 1, Kim fails to disclose or renders obvious the Challenged Claims at least because Kim fails to disclose or render obvious that its alleged filling structure is surrounding the multiple-stack staircase structure as required by the Challenged Claims. Under the proper construction of the term “surrounding,” the Challenged Claims require the filling structure to encircle the multiple-stack staircase structure. The alleged filling structure of Kim, however, merely covers the top and one side of the staircase structure but does not encircle the staircase structure. Petitioner’s arguments for obviousness provide only conclusory and illogical arguments that are belied by Kim’s teachings.

For Ground 2, Tessariol fails to disclose or render obvious the Challenged Claims at least because, again, Petitioner fails to show that the art discloses or renders obvious “a filling structure surrounding the multiple-stack staircase structure.” Because no single element in Tessariol’s memory device surrounds the staircase structure, Petitioner combines multiple elements from Tessariol in an attempt to patch together a purported “filling structure” that meets the claim requirements. But even if Petitioner’s patchwork of elements were considered a filling structure, Tessariol still does not disclose or render obvious a filling structure that surrounds the staircase structure under the correct interpretation of “surrounding”

because there is no purported filling structure at the lateral ends of Tessariol's staircase structures. Petitioner's obviousness arguments are again conclusory, illogical, and contradict the evidence.

Petitioner's Ground 3 applies Tessariol's teachings to Kim for claim 4, but otherwise relies on Kim for claim 1. Therefore, Petitioner's arguments fail for at least the reasons provided with regard to Petitioner's Ground 1.

Petitioner's Ground 4 applies Kim's teaching to Tessariol but only as to particular requirements of claim 1, and Petitioner does not raise any new arguments as to the claimed "filling structure" recited in limitation [1.d]. Instead, Petitioner again relies on its Ground 2 arguments. Therefore, Petitioner's arguments fail for at least the reasons provided with regard to Petitioner's Ground 2.

Furthermore, for both Grounds 3 and 4, a POSITA would not have been motivated to combine Kim and Tessariol.

Finally, Petitioner's various grounds fail to disclose or render obvious "a supporting pillar [that] is filled with ... a pillar-support material surrounded by the insulating material" as required by claims 4-5 because Petitioner has not shown that the alleged conductive cores are "pillar support materials" (and in some cases, has not even shown that the identified structure is a conductive core—the first link its multi-stage obviousness argument).

As set forth herein, the Grounds presented in the Petition fail to make the required showing of obviousness.¹

II. THE '031 PATENT

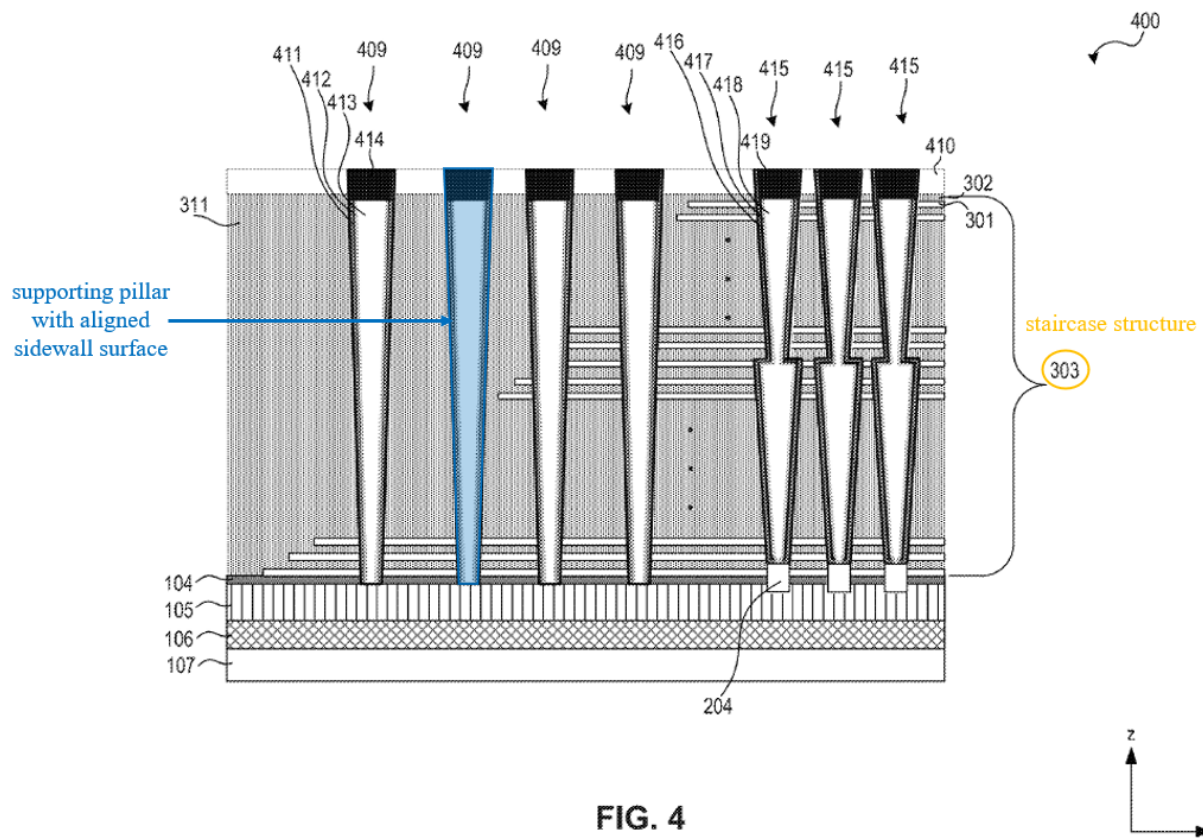
The claimed invention of the '031 is directed to “three-dimensional memory device architectures” that address issues arising from the fabrication techniques known in the prior art and, as a result, “improves device yield and performance.” '031, 1:42-49, 9:15-28.

Specifically, the '031 is directed to an improved memory device fabrication technique that involves “one staircase-forming patterning process to form the multiple-stack staircase structure.” '031, 8:63-9:1. Techniques known in the prior art involved employing multiple staircase-forming patterning processes to obtain a multiple-stack memory device, which was “time-consuming and costly.” '031, 1:33-37, 7:57-62. There were several reasons for these disadvantages. KuhnII, ¶43. First, having to use different photomasks for different dielectric stacks increased the number of required photomasks and photolithography operations, raising cost and time. KuhnII, ¶44. Second, forming an upper dielectric stack after the lower one

¹ This Patent Owner Response is supported by the declaration of Dr. Kuhn. *See* Ex. 2013 (“KuhnII”). All emphasis and color annotations have been added unless otherwise noted.

led to quality issues in the upper stack due to processing it on top of the lower structures. *Id.*, ¶45. Third, sub-channel holes and sub-pillar holes often had different dimensions, making it challenging to achieve uniformity and required higher precision control. '031, 8:5-31; KuhnII, ¶46.

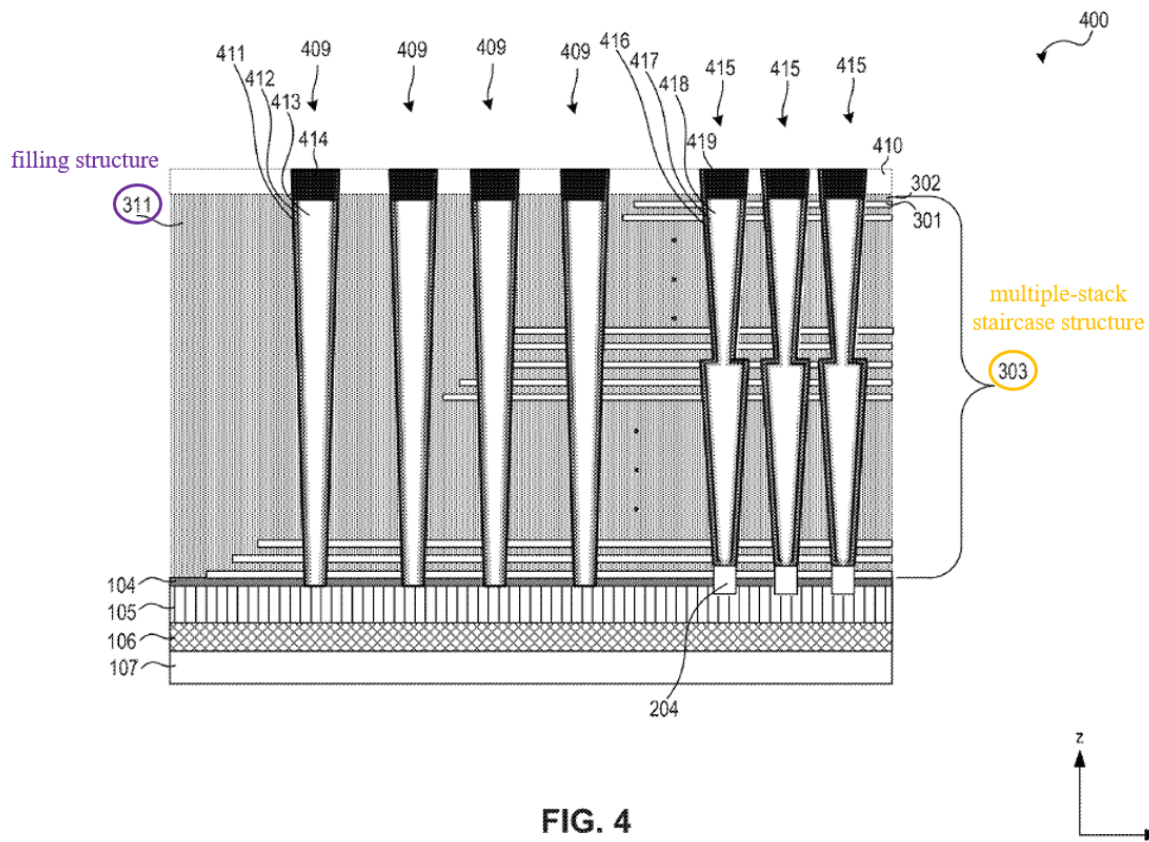
The novel device taught in the '031 and recited in its claims is characterized by forming the **staircase structure**, which has alternating layers (e.g., conductor and insulating layers) that are etched to form a step-like pattern, by one patterning process, thereby avoiding the issues that arise from multiple patterning of different stacks and “improv[ing] device yield and performance.” '031, 9:1-28; KuhnII, ¶47. As a result of this single patterning process, **the supporting pillars** have **aligned sidewall surfaces**, in contrast with the unaligned sidewall surfaces of the supporting pillars in the prior art. '031, 8:35-53; KuhnII, ¶48.



'031, Fig. 4 (annotated).

The device of the '031 also includes “**dielectric filling structure 311** that surrounds **staircase structure 303**,” which comprises staircase regions that “can each surround memory structure [] along the x-y plane.” '031, 13:44-48, 22:30-32. After the staircase structure 303 is formed, a dielectric filling material is deposited to fill the space created by the removal of parts of the dielectric stack. **Dielectric filling structure 311** is deposited in both the periphery region and the core region. KuhnII, ¶49. Excessive dielectric filling material from the top surface is removed using a suitable planarization method. *Id.*, ¶50. The remaining dielectric filling

material forms the **dielectric filling structure 311** that surrounds the **staircase structure 303**. *Id.* **Dielectric filling structure 311** can be made of any suitable dielectric material that provides electrical insulation for the **staircase structure 300**. '031, 13:36-64, 22:27-32. *Id.*



'031, Fig. 4 (annotated).

A representative embodiment of the '031's memory device includes: (1) a “**substrate 107**” ('031, 10:17-23); (2) a “**multiple-stack staircase structure 303**” ('031, 13:30-35); (3) a “**filling structure 311**” surrounding the multiple-stack staircase structure ('031, 13:36-49); (4) “**semiconductor channels 415**” ('031, 2:45-

50, 14:37-44); and (5) “**supporting pillars 409**” (’031, 2:45-50, 14:37-44). KuhnII, ¶51.

The ’031 patent cogently explains these features as they relate to the Challenged Claims. *Id.*, ¶52. For example, the ’031 patent explains that multiple-stack staircase structure allows “more memory cells to be formed along the direction perpendicular to the [] substrate” in a 3D NAND memory device. ’031, 1:23-25; KuhnII, ¶52.

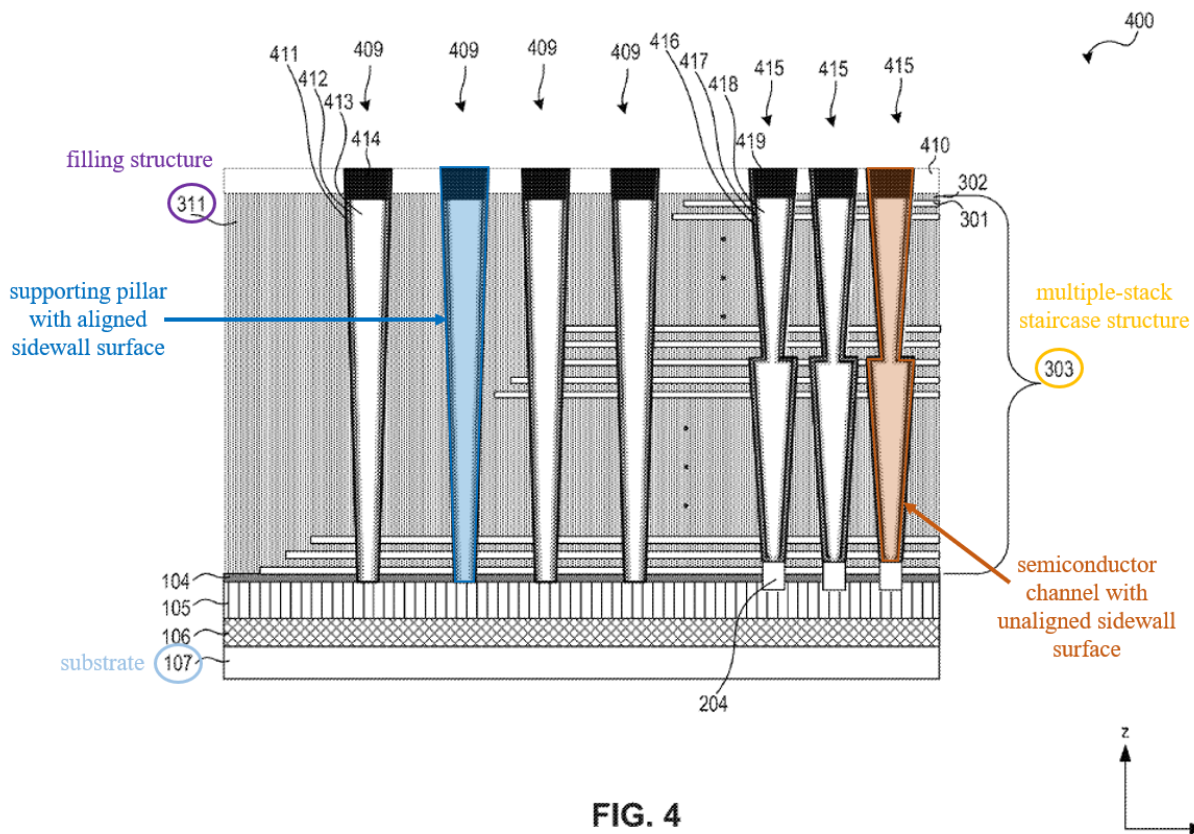
Furthermore, regarding supporting pillars, the specification explains that the 3D NAND memory device “includes multiple stacks of word lines arranged along the direction perpendicular to the substrate” in which “supporting pillars are used in the fabrication process to provide mechanical support and prevent pattern collapse.” ’031, 1:23-25, 33-36. These supporting pillars “extend through the multiple-stack staircase structure.” *Id.*, 1:56-62. KuhnII, ¶53. The ’031 patent also explains the process of forming the supporting pillars in detail. KuhnII, ¶54. In one embodiment, the process involves depositing dielectric material in a pillar hole² to

² A pillar hole is formed by etching through at least one of the filling structure and the multiple-stack staircase structure. ’031, 2:57-63; KuhnII, ¶141.

form an insulating liner and the metal material is deposited to fill up the pillar hole. '031, 25:15-21; KuhnII, ¶54.

The supporting material used in the supporting pillars is important because, as the name suggests, it provides support to the pillars. '031, 25:15-21; KuhnII, ¶55. For this reason, a material must have “sufficient stiffness and/or support functions” to be considered as a supporting material. '031, 18:26-28; KuhnII, 56. Supporting material, for example, can include “copper, cobalt, nickel, and aluminum.” '031, 18:28-30; KuhnII, 56.

Semiconductor channels that permit current flow are also formed on the 3D memory device. '031, 1:25-28; KuhnII, ¶57. Importantly, the “supporting pillar and the semiconductor channel are filled with different filling layers.” '031, 1:56-62, 2:10-11. KuhnII, ¶57. Specifically, the supporting pillar is filled with “at least one of an insulating material and a pillar-support material surrounded by the insulating material,” while the semiconductor channel is filled with “at least one of a charge trapping film, a semiconductor channel film, and a dielectric core.” '031, 2:12-17. A cross-section view of the memory device with these features is illustrated below. KuhnII, ¶58.



'031, Fig. 4 (annotated).

The only independent claim of the Challenged Claims, claim 1, is directed to aspects of the above-described invention:

[1.pre] A memory device comprising:

[1.a] a substrate;

[1.b] a multiple-stack staircase structure comprising a plurality of staircase structures stacked over the substrate,

[1.c] wherein each of the plurality of staircase structures comprises a plurality of conductor layers, wherein each of the

plurality of conductor layers is located between two insulating layers;

[1.d] a filling structure surrounding the multiple-stack staircase structure;

[1.e] a semiconductor channel extending through the multiple-stack staircase structure, wherein the semiconductor channel comprises unaligned sidewall surfaces; and

[1.f] a supporting pillar extending through at least one of the multiple-stack staircase structure and the filling structure, wherein the supporting pillar comprises aligned sidewall surfaces.

III. FILE HISTORY

The claims of the '031 remain patentable over the prior art for at least the same reason identified during prosecution. As discussed further below in §§VII-X, the prior art does not disclose or render obvious, *inter alia*, the claimed “filling structure surrounding the multiple-stack staircase structure” of the '031. Claims directed to this limitation were allowed after thorough prosecution and consideration of numerous prior art references.

The '031 was filed on September 10, 2018. During the pendency of the application, Applicant was required to restrict the invention to that of “a memory device” or “a method for forming a memory device.” Ex. 1002, 663-667 (9/4/2019

Requirement for Restriction/Election). Applicant elected, without traverse, claims that restricted the invention of the '031 to that of “a memory device.” Ex. 1002, 668-669 (9/23/2019 Reply to Restriction Requirement). KuhnII, ¶61.

In a non-final office action, the Examiner rejected all the elected claims under 35 U.S.C. § 102(a)(1) as being allegedly anticipated by U.S. Publication No. 2010/0133599 (“Chae”). Ex. 1002, 825-830 (1/7/2020 Office Action). Applicant filed a response and argued against the rejection, pointing out that Chae fails to disclose at least “a semiconductor channel extending through the multiple-stack staircase structure, wherein *the semiconductor channel comprises unaligned sidewall surfaces.*” Ex. 1002, 851-854 (4/2/2020 Reply to Office Action). The Examiner subsequently allowed all pending claims. Ex. 1002, 862-865 (7/1/2020 Notice of Allowance). The '031 issued on December 15, 2020 with six claims. Ex. 2002, 938 (11/24/2020 Issue Notification). KuhnII, ¶62.

IV. LEVEL OF ORDINARY SKILL IN THE ART

For purposes of this proceeding only, Patent Owner does not object to the definition of a person of ordinary skill in the art (“POSITA”) proffered by Petitioner and adopted by the Board at institution—i.e., a person with “bachelor of science degree in electrical engineering or a similar discipline, along with 2-3 years of professional experience working with (e.g., researching, designing, or teaching) memory devices, or an equivalent level of skill, knowledge, and experience (e.g., an

advanced degree may replace some of the professional experience).” Pet. 22. The Challenged Claims are valid regardless of the precise definition used for a POSITA. KuhnII, ¶¶63-67.

V. CLAIM CONSTRUCTION

Other than the term identified below, Patent Owner submits that constructions of the claim terms are not necessary to assess whether the prior art reads on the Challenged Claims for the purposes of the *inter partes* review. Patent Owner, however, reserves the right to modify or elaborate on its proposed constructions and to raise further claim construction issues in the parallel district court proceedings.

The parties exchanged proposed claim constructions in the parallel district court proceeding. Ex. 2007 (“Micron’s Preliminary Claim Constructions”), Ex. 2008 (“Plaintiff’s Proposed Claim Constructions”). The claim construction disputes in district court do not impact the issues raised in this Response.

A. “surrounding” (Claim 1)

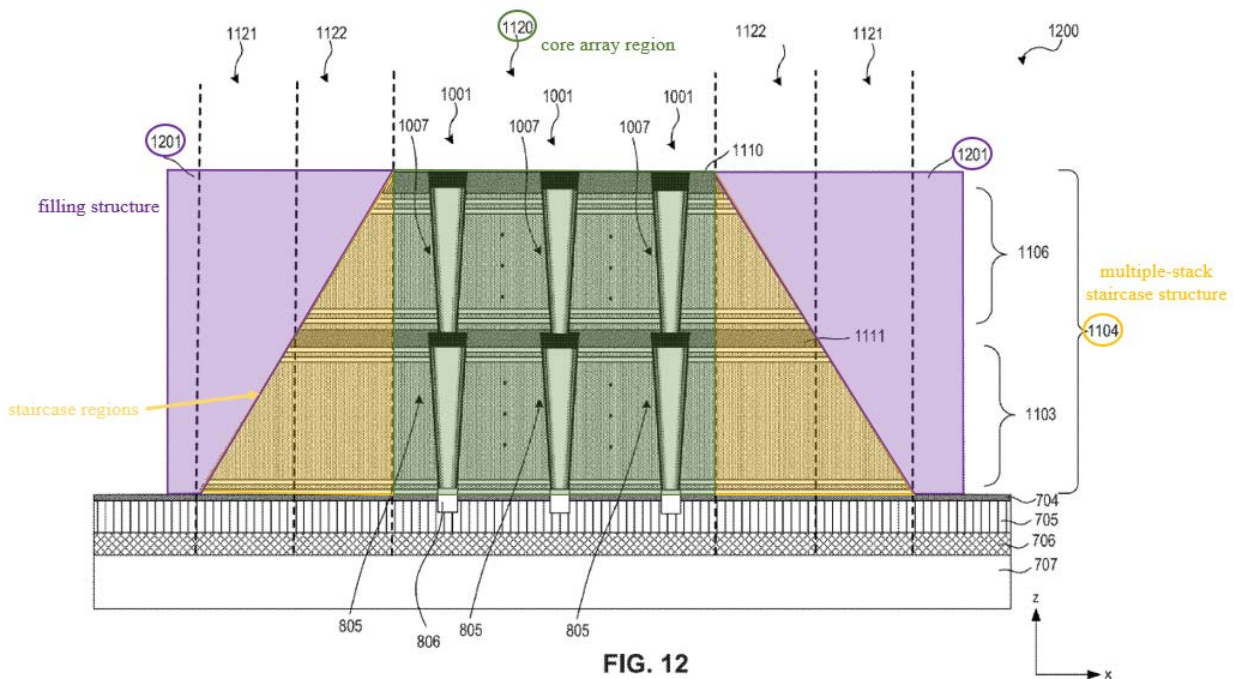
The term “surrounding,” which is a limitation of all Challenged Claims because it occurs in claim 1, should be construed according to its plain and ordinary meaning as to be all the way around (something)—in other words, encircling. KuhnII, ¶¶69-78. This construction is both consistent with the plain and ordinary meaning of the term and supported by the intrinsic evidence. KuhnII, ¶69.

The plain meaning of “surrounding” is “encircling.” *See, e.g.*, Ex. 2001 (New Oxford American Dictionary 2010 defining “surround” as “be all around (someone or something); ... encircle (someone or something) so as to cut off communication or escape”); Ex. 2002 (American Heritage College 2000 defining “surround” as “encircle”); Ex. 2003 (Webster’s II New College 2005 defining “surround” as “to encircle on all sides of simultaneously”); Ex. 2004 (Merriam-Webster’s Dictionary and Thesaurus 2014 defining “surround” as “to enclose on all sides : ENCIRCLE”). KuhnII, ¶70.

In the context of claim 1, the term “surrounding” occurs in limitation [1.d], which recites “**a filling structure surrounding the multiple-stack staircase structure.**” The claims use the term “surrounding” instead of narrower alternatives, such as “covering” or the concept of being “between” two structures. KuhnII, ¶71.

The specification is likewise consistent with the plain meaning. Figs. 4 and 12 of the ’031, reproduced below, show that the multiple-stack staircase structure is encircled by the filling structure (1201, 311). In Fig. 12, staircase regions (“first staircase region 1121” and “second staircase region 1122”) are shown to extend in the +x and –x directions. The ’031 makes clear that the staircase regions (which have the filling structure) also extend in the +y and –y directions, and therefore

“surround” the memory structure.³ ’031, 13:27-28 (“Dielectric pairs of different tiers can be etched to **form staircases extending along the x-y plane.**”), 22:30-32 (“First staircase region 1121 and second staircase region 1122 can each **surround memory structure 1100 along the x-y plane.**”). KuhnII, ¶72.



’031 Patent, Fig. 12 (annotated).

³ Fig. 12 has labels provided for x and z directions, and the y direction is perpendicular to both directions and points into the page.

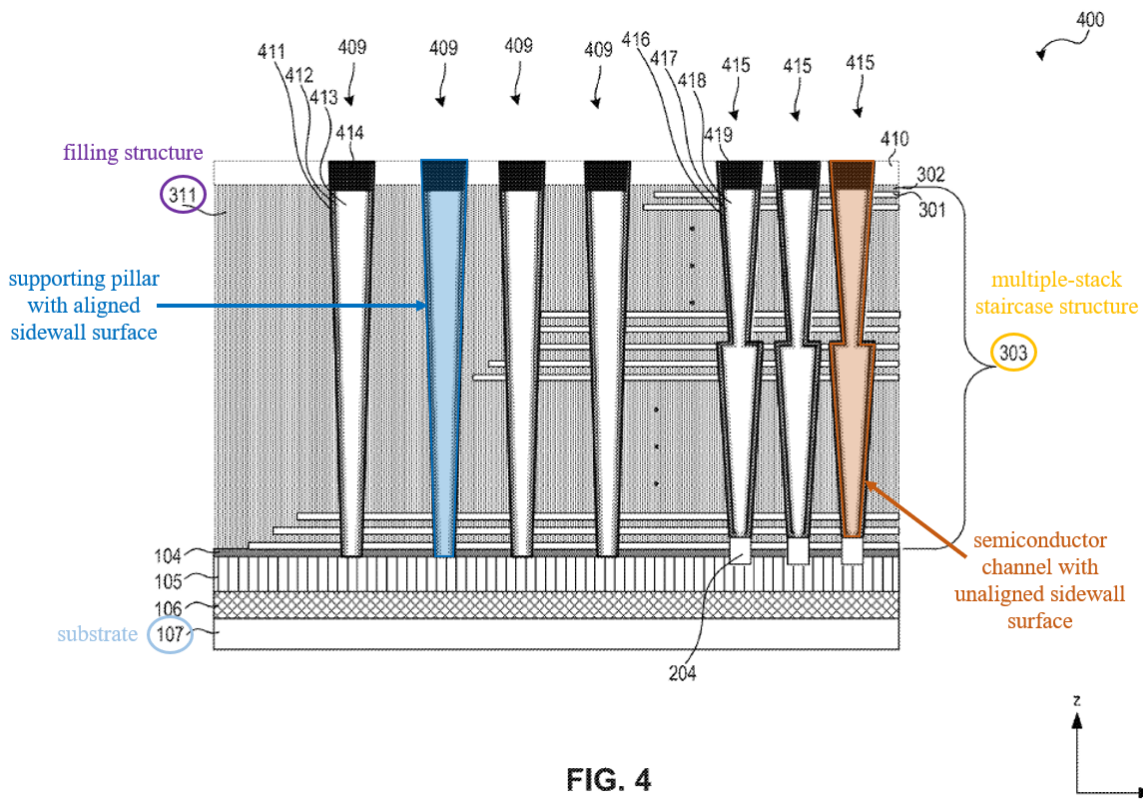


FIG. 4

'031 Patent, Fig. 4 (annotated).

After the patterning of the staircase regions, the filling structure is deposited to fill the space surrounding the staircase structure. *See* '031, 13:36-48 (“Further, a **dielectric filling material can be deposited after staircase structure 303 is formed to fill in the space formed by the removal of the portions of dielectric stack 203.** Dielectric filling structure 311 is deposited in periphery region 320 and core region 310 to fill in the space formed by the removal of the portions of dielectric stack 203.”); *see also* '031, 22:61-23:9. The filling structure therefore surrounds/encircles the multiple-stack staircase structure when it is deposited to the left, right, back, and front of the staircase structure. KuhnII, ¶73.

Moreover, the '031 uses the term “surrounding” consistently as “encircling” in multiple other instances. See '031, 2:12-14 (“In some embodiments, the supporting pillar is filled with at least one of an insulating material and a pillar-support material **surrounded by the insulating material.**”), 15:49-57 (“Charge trapping film 416 can also include a storage unit layer (memory layer) over and **surrounded by the block dielectric layers** for trapping charges and forming a plurality of charge storage regions along the z axis. Charge trapping film 416 can also include a tunneling layer (e.g., tunneling dielectric) over and **surrounded by the memory layer.**”); *see also, e.g.*, '031, 3:31-35, 4:13-17, 18:25-26. KuhnII, ¶74.

Although Petitioner does not argue explicitly for a construction of the term “surrounding,” Petitioner nonetheless argues:

To the extent PO argues that “surrounding” requires the dielectric filling structure be on all sides of the multi-stack staircase structure, such an interpretation is inconsistent with all embodiments of the '031 Patent, which never describes or illustrates the filling structure on each and every side of the multi-stack structure.

Pet. 34. KuhnII, ¶75. Patent Owner’s construction, however, does not require filling structure on **all** sides of the multi-stack staircase structure—i.e., it does not require filling structure on the top and bottom of the staircase structure. As demonstrated above, the '031 does describe the filling structure on all sides of the multi-stack structure in the horizontal plane (e.g., in the +x and -x direction as well as the +y and

-y direction)—i.e., the filling structure encircles the multi-stack structure. KuhnII, ¶76.

Furthermore, in the Board’s Decision on Institution (“DI”), the Board correctly concluded that the intrinsic record supports the plain meaning of “surrounding.” As the Board noted:

[The] disclosures in the ’031 patent indicate that the staircase structure is etched along the x-, y-, and z-axes, the dielectric filling structure fills the spaces in the x-, y-, and z-directions created when the staircase structure is etched, and the staircase structure surrounds the memory structure in the x-y plane.

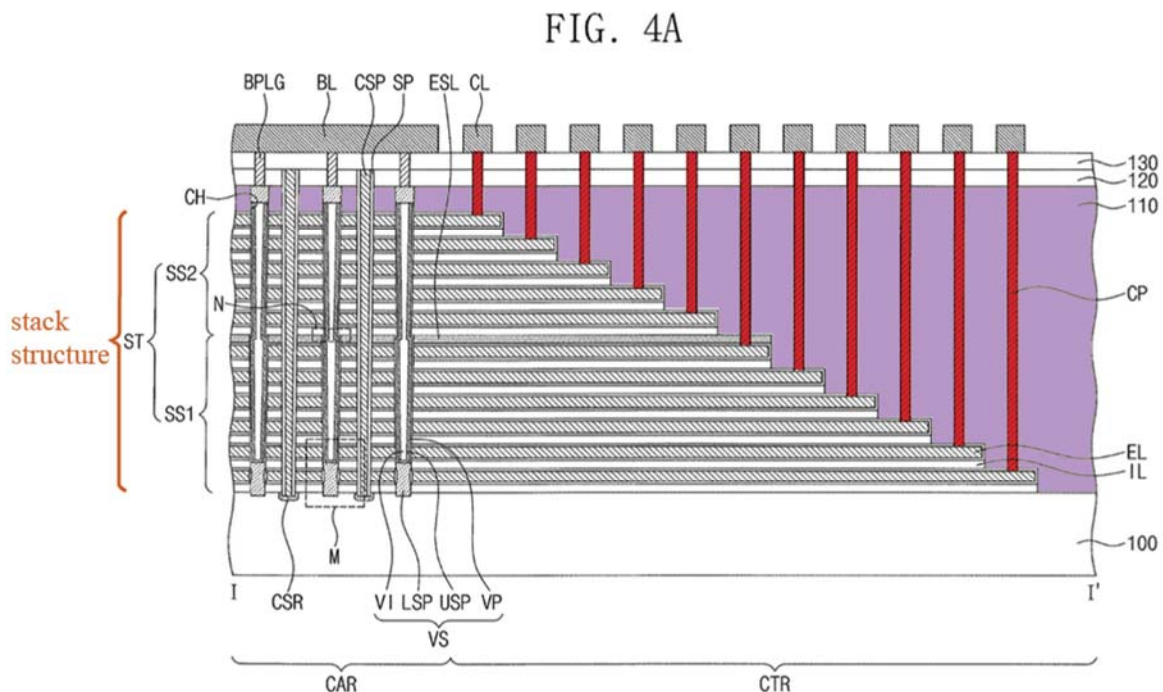
DI, 11; KuhnII, ¶77. Based on these disclosures, the Board stated that “it appears that the dielectric filling structure surrounds or encircles the staircase structure on four sides (front, back, left, and right) in the x-y plane,” and that this “understanding of ‘surround’ is consistent with the way ‘surround’ is used in the ’031 patent and with the plain and ordinary meaning of ‘surround.’” *Id.* Ultimately, the Board correctly determined that “‘surrounding’ as used in claim 1 of the ’031 patent means ‘encircling’ or ‘to be all the way around (something).’” *Id.*, 11-12. KuhnII, ¶78.

VI. THE PRIOR ART REFERENCES RELIED UPON

A. U.S. Patent No. 10,381,369 (“Kim”) (Ex. 1005)

Petitioner does not contend that Kim anticipates the Challenged Claims, and instead argues only that it renders obvious certain claims, including the sole independent Challenged Claim, claim 1. Pet. 8, 27-56; KuhnII, ¶79.

Kim’s memory device includes a cell array region (“CAR”), and a connection region (“CTR”) with a **stack structure (ST)** composed of alternating electrode layers and insulating layers. Kim’s device further has **contact plugs** that each connect to a top electrode layer of the **stack structure**. Ex. 1005, 9:4-11. As shown in Figure 4A below, Kim’s **stack structure (ST)** is covered by a **filling insulation layer (110)**:



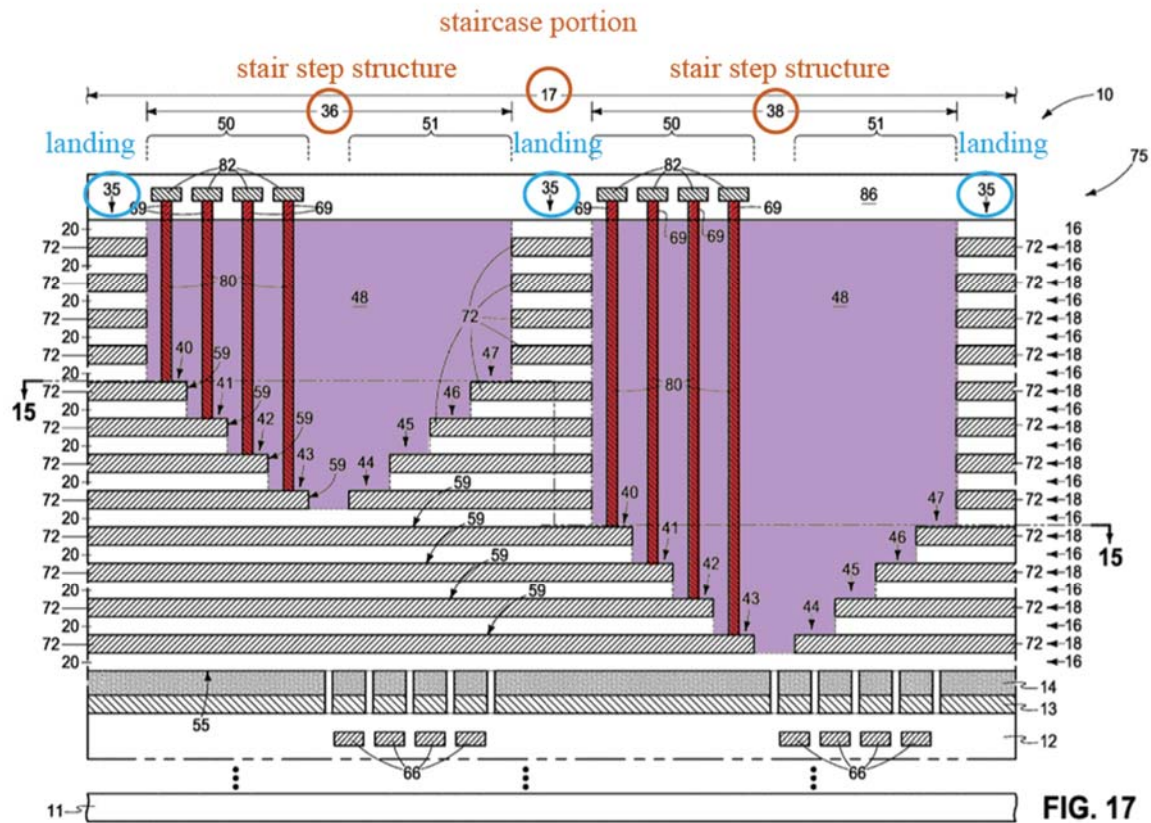
Ex. 1005, Fig. 4A (annotated); KuhnII, ¶80; *see also* Ex. 1005, 9:53-58. Neither Kim’s figures nor its specification suggests filling insulation to the left of the staircase structure (a staircase structure can be defined by the upper and lower structures of the stack structure, Ex. 1005, 1:61-63) or perpendicular to the plane of Fig. 4A below (denoted as “D1” in Kim). As a result, Kim does not disclose or render obvious that the filling insulation layer surrounds the staircase structure. KuhnII, ¶81.

B. U.S. Patent Publication No. 2019/0081061 (“Tessariol”) (Ex. 1006)

Petitioner does not contend that Tessariol anticipates the Challenged Claims, and instead argues only that it renders obvious certain claims, including the sole independent Challenged Claim, claim 1. Pet. 8, 57-86. KuhnII, ¶82.

Tessariol describes a device with memory cells that includes an “**adjacent/staircase portion 17**” having multiple **stair step structures 36 and 38**, which are formed on the base substrate composed of vertically-stacked alternating tiers of first and second materials (*e.g.*, insulative, conductive, and semiconductive materials). Ex. 1006, [0029], [0031], [0034], [0048]. Tessariol’s device further has **operating conductive vias** that each connect to a top conductive step of the **stair step structures** and are “directly electrically coupled to one another by an interconnect line” above the alternating layers. Ex. 1006, [0046], [0052]. Tessariol’s **stair step structures** are in the shape of stadiums with **landings 35** that

“define a crest between immediately adjacent stadiums” and an **insulating material 48** above the steps. Ex. 1006, [0035]; KuhnII, ¶83.



Ex. 1006, Fig. 17 (annotated).

As Petitioner’s expert, Dr. Banerjee, acknowledges in the declaration, “the figures in Tessariol do not show the outer ends/sides of the device.” Ex. 1003, ¶ 184; *see also* Pet. 70 (“Note that Tessariol does not expressly depict the lateral ends of the device.”). Nor does Tessariol describe the lateral ends of the stair step structures as being bordered by insulating material. To the extent that the ends of the device are depicted in Tessariol’s figures (*e.g.*, Fig. 17), they appear exposed. KuhnII, ¶84.

While Tessariol describes a filling material inside the stadium region (Ex. 1003, ¶ 34), nowhere is that material depicted or described as “surrounding” the staircase structure. KuhnII, ¶85.

As a result, Tessariol does not disclose or render obvious that insulating structure surrounds the staircase structure. *Id.*, 86.

VII. GROUND 1: KIM DOES NOT DISCLOSE OR RENDER OBVIOUS CLAIMS 1-4

Kim fails to disclose or render obvious the Challenge Claims⁴ at least because, under the proper construction of “surrounding” as encircling (§V.A), Kim fails to disclose or render obvious limitation [1.d] of the sole challenged independent claim, which requires filling structure that is “surrounding the multiple-stack staircase structure.” Petitioner also fails to show that Kim discloses or renders obvious a “supporting pillar” with a “pillar-support material” as required by dependent claim 4. KuhnII, ¶¶87-174.

A. Independent Claim 1: Kim Does Not Disclose or Render Obvious Limitation [1.d]

Petitioner fails to show that Kim discloses or renders obvious “a filling structure surrounding the multiple-stack staircase structure” as required by limitation [1.d] because, at most, Kim teaches that the alleged insulation material covers the

⁴ Petitioner does not assert Ground 1 against claim 5. Pet. 8.

top and one side of its stack structure but does not “surround” or encircle (§V.A) the stack structure. Moreover, Kim discloses that at least two sides of the stack structure are instead cut by trenches formed after the insulation material has already been deposited, and a third side is simply not shown or described in Kim. KuhnII, ¶¶88-138.

Petitioner’s flawed arguments can be divided into two sets. KuhnII, ¶89. The first set of arguments relies on the unsupported assertion that Kim’s insulation material covers the stack structure on all sides based on a conclusory statement from its expert. Pet., 32-38. As discussed further below, Kim has no teaching that the insulation layer encircles the stack structures, as required by the term “surrounding” in the Challenged Claims. KuhnII, ¶90. Petitioner’s second set of arguments rest on flawed obviousness arguments and improper extension of Kim’s limited disclosures. *Id.*, ¶91. Furthermore, throughout the obviousness arguments, Petitioner improperly relies on conclusory statements and fails to explain why it would have been obvious to a POSITA to make the alleged modifications. *Id.*, ¶92. These erroneous arguments are addressed in detail below.

1. Kim Does Not Disclose That Its Filling Insulation Layer “Surrounds” the Stack Structure

Contrary to Petitioner’s assertion, Kim’s insulation material does not surround the stack structure because it is disclosed as only covering the top and one side of

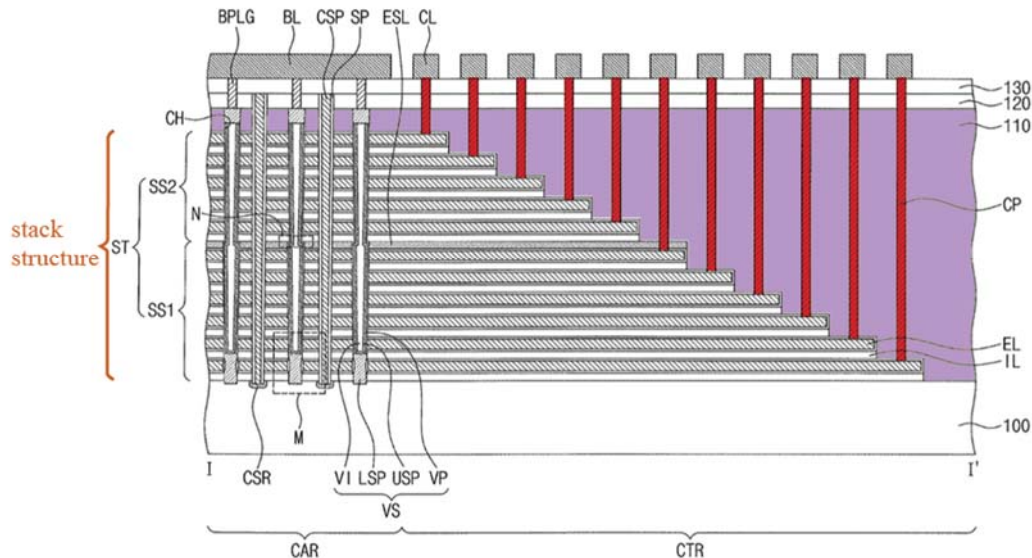
the structure. Limitation [1.d] requires “a filling structure surrounding the multiple-stack staircase structure.” As discussed in §V.A, the term “surrounding” means “encircling.” Kim does not disclose a filling structure that encircles the staircase structure. KuhnII, ¶¶93-94.

Petitioner’s arguments are based on misinterpretation of Kim’s disclosures, which do not teach the required encircling. Petitioner points to Kim’s filling insulating layer 110 as the “filling structure” that allegedly surrounds the stack structures. Pet. 32. But Kim discloses only that “[t]he filling insulation layer 110 may be disposed on the substrate 100 and may cover the stack structures ST” (Kim, 9:53-58). “a filling insulation layer 110 may be formed on an entire top surface of the substrate 100 to cover the mold structure MT” (*id.*, 11:11-13), and insulating layer 110 is on the right side of the staircase in the +D2 direction (*id.*, Fig. 4A). This is the entire extent of Kim’s disclosure on the relationship between the insulation layer and the stack structure. KuhnII, ¶95.

Petitioner relies on Kim’s disclosure that “filling insulation layer 110 may be disposed **on the substrate** 100 and may **cover** the stack structures ST,” but as shown in Figure 4A, this merely teaches that the **stack structures** may be covered by the **filling insulating layer 100** (i.e., the material is on top) and is on one side, but it

never says that the insulating layer **surrounds** the stack structure. Pet., 32; Kim, 9:53-56. KuhnII, ¶96.

FIG. 4A



Kim, Fig. 4A (annotated); *see also* Kim, Fig. 4B. The jump from Kim’s disclosure that filling insulation material covers the top surface of the stack structure to alleging that the insulation material surrounds the entire stack structure is without support. Although Kim states that insulation layer 110 covers the “entire top surface of substrate 100,” Kim does not disclose that the substrate continues past the stack structure in all four directions. Kim, 9:53-56. Specifically, Kim does not suggest that the insulation layer covers the sides of the structure in the direction that extends

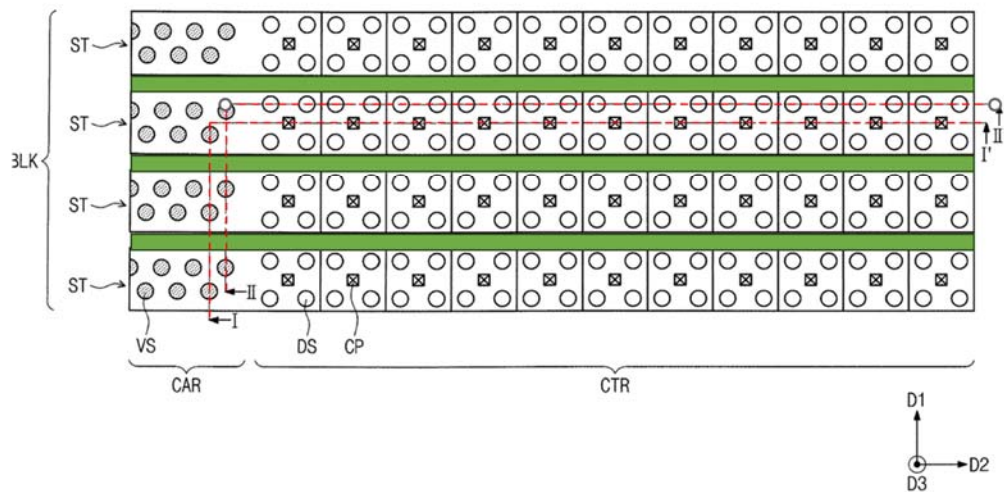
perpendicular to Figs. 4A-B, i.e. the -D1 and +D1 directions, or to the left in the -D2 direction. KuhnII, ¶97

There are multiple reasons that Kim does not show the insulation layer 110 covering the side of the staircase structure in these directions. First, Kim teaches a structure in the +D1 and -D1 direction wherein a trench cuts through the staircase structure. Second, in the -D2 direction Kim does not show insulating layer 110, and there is no fundamental reason why Kim cannot be fabricated as it is drawn, and even if the assumption is made that Kim is adjacent to another (undisclosed) structure, and thus requires some intervening isolation to that structure, there are a variety of common semiconductor processing techniques that produce an unfilled edge between the disclosed structure and other adjacent structures. KuhnII, ¶98.

First, in the +D2 and -D2 direction, Kim uses a method wherein trenches are formed in Kim's memory device after fabrication of the insulating layer. *See* Ex. 1005, Figs. 2 and 13, 18:21-33; KuhnII, 99. The trenches prevent the previously deposited filling insulation layer from "surrounding" the stack structures. As shown in Figs. 3 and 13 (below), **trenches (green)**, which are formed after the insulating layer has been deposited, cut across the entire length (Fig. 3) and height (Fig. 13) of the staircase region, forming an intervening opening on at least two sides of the stack

structure. The **red line II-II'** in Fig. 3 shows the location of the cross-section depicted in Fig. 13.⁵ KuhnII, ¶99.

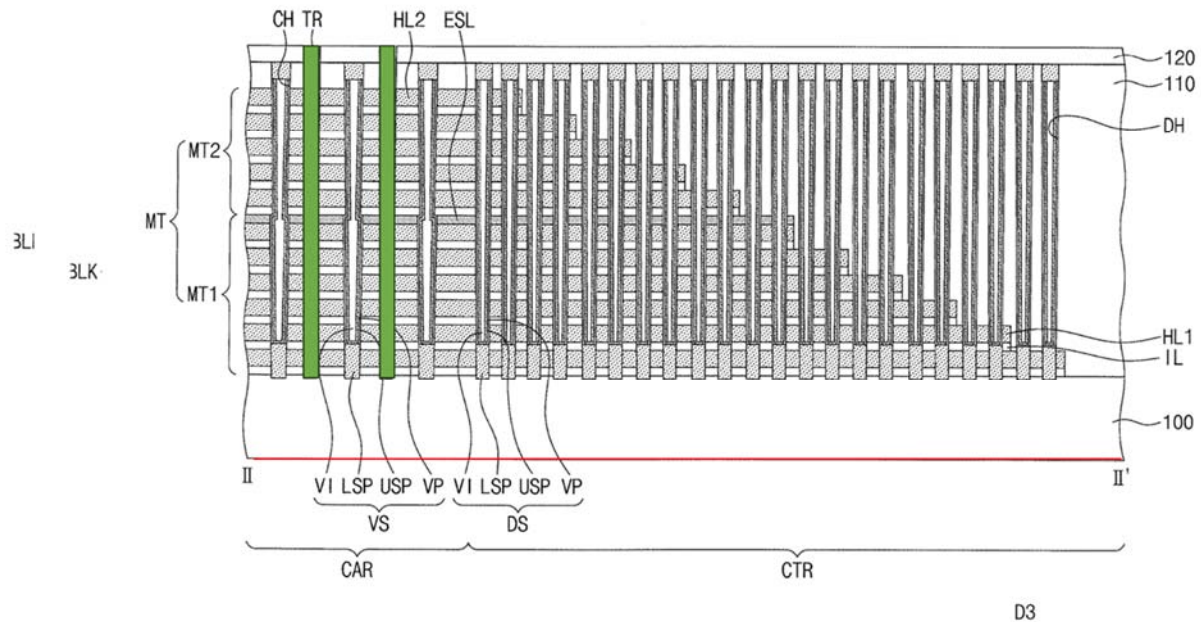
FIG. 3



Kim, Fig. 3.

⁵ This cross section does not follow the typical formalism of being a linear cross-section, but rather contains a 90-degree bend so the array and staircase cross-sections are perpendicular when viewed from above.

FIG. 13



Kim, Fig. 13. As shown above, these trenches do not contain any insulating layer 110 and separate the four staircase structures ST from each other. KuhnII, ¶100. Indeed, Kim discloses that in “Figs. 3 and 13 ... trench[es] TR may be defined between the mold structures MT⁶ ... [and] trenches TR may **expose portions of the substrate**,” which confirms that insulating layer 110 does not cover the side of the stack structures in the +D1 and -D1 directions. Kim, 12:9-18; KuhnII, 100. Petitioner and Dr. Banerjee fail to address these trenches in their analysis. KuhnII, 100. Indeed, contrary to Petitioner’s and Dr. Banerjee’s argument that it would have

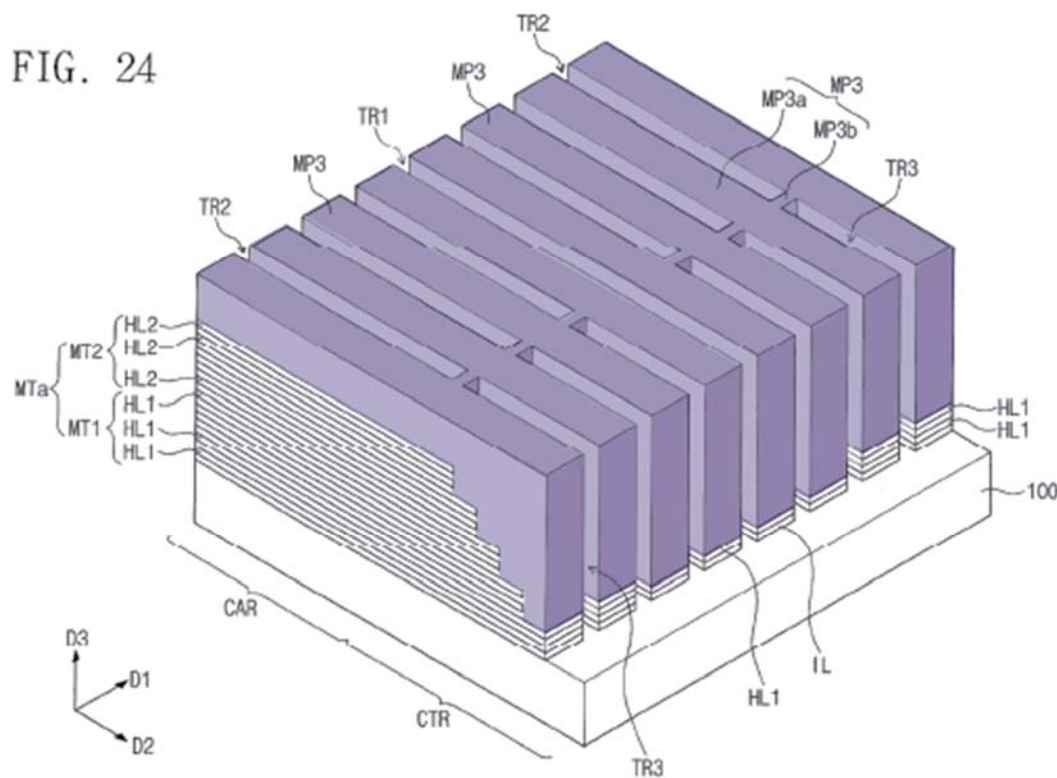
⁶ Mold structures are stack structures with sacrificial layers and can be formed into a staircase structure. See Kim, 10:50-62; KuhnII, .

been “obvious[] that the filling material would extend to the outer edge in the other directions, namely, on the other three sides of the structure” merely because “Kim discloses filling material on the outer edge of where the staircase region ends,” the presence of the trenches on the sides of the stack structure shows that Kim’s insulation layer does not have to extend to the “other three sides of the structure.” Pet., 35; Banerjee, ¶ 112. KuhnII, ¶100.

Second, in the -D2 direction, Kim does not show insulating layer 110. As shown above in Figure 3, for example, there is no depiction of insulating layer 110 to the left of the staircase structure. Even assuming there are adjacent structures (for example, another plane of memory) in that direction that require electrical isolation, it is not necessarily the case that an insulating layer would be used to provide that electrical isolation. As one example, creating an unfilled “air-gap” between structures for electrical isolation can be used. There is great motivation to do this, as an air-gap structure has the clear benefit of providing improved capacitance over filling structures such as silicon dioxide or silicon nitride (the dielectric constant of air at ~1 provides substantially better electrical isolation and thus lower capacitance than the dielectric constants of silicon oxide or silicon nitride, which are typically > 4). Because of the importance of capacitance reduction (particularly in back-end processing) there are a wide variety of techniques available in the art for creating air gaps, including such techniques as etching a trench in the material after the memory

structure is fabricated, using a sacrificial material early in the process and removing it after the memory structure is fabricated, or embedding an air gap during processing of the memory structure. Therefore, it is incorrect of Petitioner to assume that insulating layer 110 “would” cover the left side in the -D2 direction. KuhnII, ¶101.

Kim’s Fig. 24 (reproduced below) confirms that the **filling insulation layer** (purple) does not cover three of the four sides (i.e., -D2, +D1, -D1) of its multiple-stack structure. KuhnII, ¶102.



Kim, Fig. 24. While there are differences between Fig. 24 and the embodiment in Figs. 4, 12, 13 relied upon by Petitioner—such as the filling insulation layer 110 reaching the substrate 100 in Figs. 12-13 and only reaching the stacks in Fig. 24—

Fig. 24 is nonetheless relevant because it provides a 3D view of the relevant features and is therefore also applicable to the earlier embodiment for purposes of visualizing the memory device. The other differences between the two embodiments (the “electrode connecting portion ECP” that is formed by part of mask pattern “MP3 b”) are irrelevant to the issue of whether the filling insulating layer 110 surrounds the stacks. KuhnII, ¶103; *see also* Kim, 17:12-24.

Thus, the extent of Kim’s disclosures regarding the relationship between the filling insulation layer and the stack structure is that the filling insulation layer covers the stack structures on, at most, one side and on top. Specifically, there is no disclosure in Kim that the insulation layer covers a stack structure, if one even exists, on the +D1, -D1, and -D2 sides. KuhnII, ¶104.

Petitioner argues that “after forming the staircase region, Kim further discloses forming insulation layer 110 to fill all voids” which results in a planarized top surface and encases the memory device (Pet. 33), but Kim never discloses that the insulation layer “fill[s] all voids” or even the term “void.” Additionally, a planarized top surface does not necessarily mean that the stack is encased on all sides, and regardless, this argument does not consider subsequent steps, such as the trenches discussed above. KuhnII, ¶105.

First, Kim does not disclose that the insulating layer fills all voids. The only description Kim provides regarding the relationship between the filling insulation

layer and the stack structures is that the former covers the latter. Kim, 9:53-56; KuhnII, ¶106.

Second, a planarized top surface does not necessarily mean that the stack is encased on all sides. The fact that the upper surface of a structure has been polished flat does not provide any information on the cross-sectional nature of the structure. KuhnII, ¶107. Disregarding this fact, Petitioner and its expert conclusively asserts that “[b]ecause Kim discloses depositing the filling insulating layer onto ‘substrate 100’ to cover the stacks and planarizing the material on the top surface, this means that the filling material will encase the memory device.” Pet. 35. In other words, Dr. Banerjee simply extrapolates Kim’s thin disclosure of depositing insulation material over a substrate to erroneously conclude that the insulation material “will encase the memory device” (Ex. 1003, ¶ 112), which is a logical jump that cannot be made because it is not supported by Kim’s disclosures or other evidence. KuhnII, ¶108; Ex. 1005, 9:53-56. As explained above, there are trenches on two sides of the staircase structure. In addition, in a third side (the -D2 direction), if electrical separation is required, there is no requirement in the art that the separation use insulation material. Indeed, insulating with air has advantages such as capacitance reduction. KuhnII, ¶109. Capacitance reduction is so important in semiconductor technologies that multiple processes have been developed for creating air-gaps, such as self-assembly techniques that involve air-gaps without any liners as shown below:

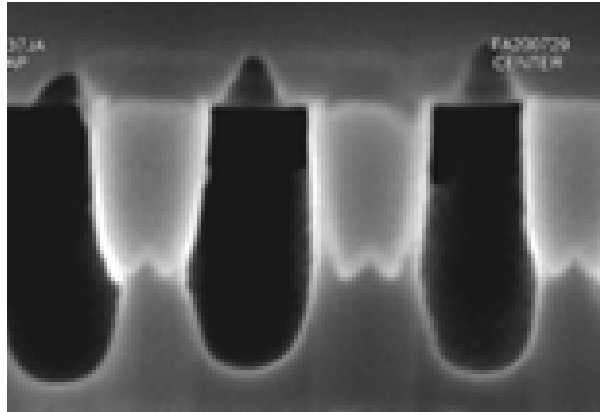


Fig. 1a: Self-Assembly Airgap

Ex. 2012, 191. KuhnII, ¶112.

Indeed, as explained above, there are a wide variety of techniques available in the art for creating unfilled air-gaps—etching a trench in the material after the memory structure is fabricated, using a sacrificial material early in the process and removing it after the memory structure is fabricated, or embedding an air-gap during processing of the memory structure—that do not even involve insulation material. KuhnII, ¶109. One common technique for creating an air-gap takes “advantage of the non-conformity of a CVD dielectric layer to create air cavities located inside trenches.” Ex. 2009, 65. This technique uses CVD for creating the capping dielectric layer for the air-gap (Ex. 2009, 65, Fig. 1) and can be used with chemical-mechanical polish (Ex. 2010, 141-142). These examples illustrate the creation of air-gaps in trenches in semiconductor devices using both CVD and CMP, which

shows that neither the use of CVD nor the use of CMP necessarily results in an isolation structure filled with silicon dioxide or silicon nitride. KuhnII, ¶¶110-111. In these examples, the isolation structure uses air instead of material such as Kim’s insulation material. *Id.*

Petitioner’s argument regarding forming a planarized top surface (Pet. 35) does not account for subsequent processing steps after the insulating layer has been deposited. KuhnII, ¶¶113-115. For example, as explained above, Petitioner and Dr. Banerjee fail to address the trenches in Figs. 3 and 13 in their analysis even though they are directed to Petitioner’s cited embodiment. *Id.*, ¶113. Indeed, even if Petitioner were correct that the insulating layer was deposited to cover all sides of the stack (it is not), the subsequent formation of trenches through the entire staircase structure, as taught by Kim, means that the memory device taught by Kim does not meet the claims. *Id.*, ¶114.

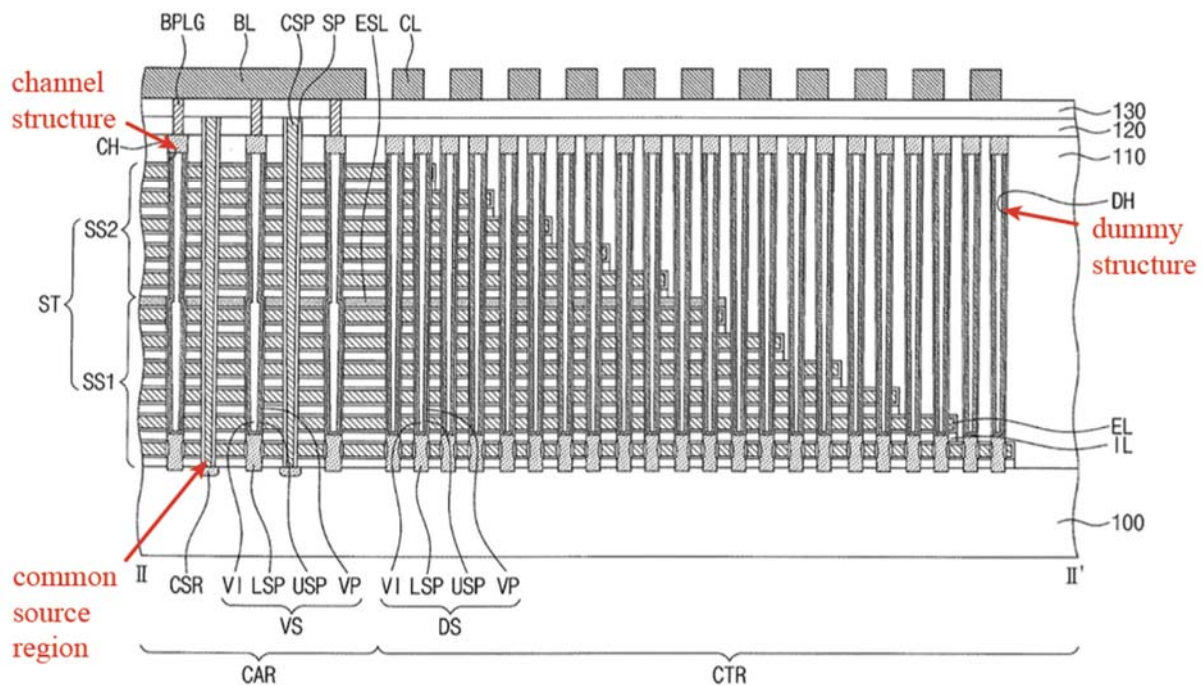
Accordingly, Kim does not disclose that its filling insulation layer “surrounds” the stack structure. KuhnII, ¶¶115-116.

2. Kim Does Not Render Obvious That Its Filling Insulation Layer “Surrounds” the Stack Structure

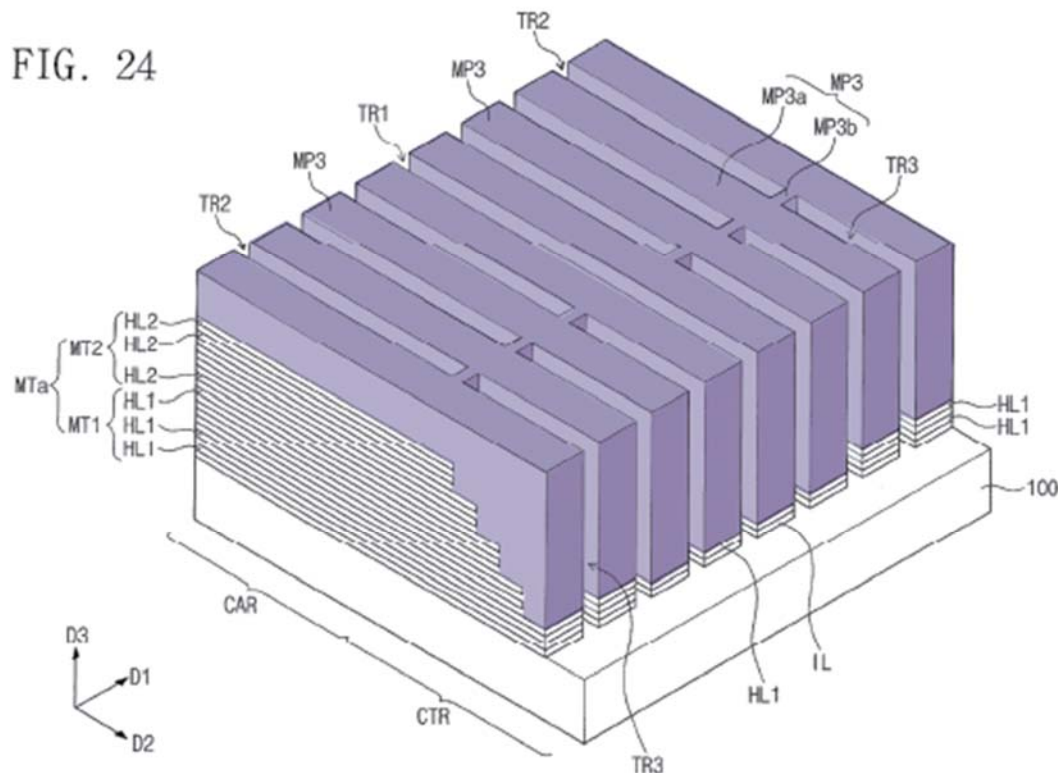
Petitioner’s obviousness arguments also fail to cure Kim’s deficiencies because they are inconsistent with the evidence and rely on nothing more than conclusory statements and impermissible hindsight. KuhnII, ¶117.

Petitioner first argues that a POSITA would have found it obvious that a structure that extends in one direction would also extend in a perpendicular direction (Pet. 35), but this argument is inconsistent with the evidence. KuhnII, ¶118. For example, this argument once again ignores the trenches, discussed above in §VII.A.1, that cut through the entire staircase structure to form an intervening opening after the insulating layer is deposited. And contrary to Petitioner's assertion, many of Kim's components extend in one direction and not others. *Id.*, ¶119. To name just a few examples from components mentioned in §VI.A, channel structures, dummy structures, and contact plugs extend in the D3 direction but not in D1 or D2; common source regions extend in D2 and D3 directions but not in D1. *Id.*, ¶120.

FIG. 4B



Kim, Figs. 3, 4A-B. In addition, Kim's Figure 24—which shows the perspective view of the stack region—shows that the insulation layer is only on the top and one side. Indeed, the figure below shows that in gaps where the staircase structure is absent, the **filling insulation layer** (purple) is also absent. KuhnII, ¶121.



Kim, Fig. 24 (annotated). Thus, it is incorrect to assume that a feature like the insulating layer 110 would extend in other directions simply because it is present in a different direction. KuhnII, ¶122.

To support an obviousness argument, Dr. Banerjee, also mischaracterizes established deposition processes and design requirements in the art. Dr. Banerjee initially admits that Kim discloses only “filling material on the outer edge of where

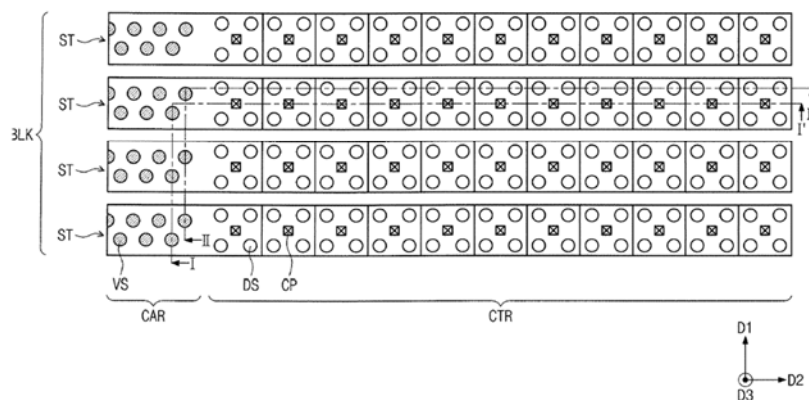
the staircase region ends,” but then argues that a POSITA would have found it obvious to extend the filling material to the entire memory device. Ex. 1003, ¶ 113; Petition, 35. KuhnII, ¶123. Specifically, Dr. Banerjee argues that chemical vapor deposition (CVD) is often used to deposit materials like Kim’s insulation layer and “is an isotropic process leading to deposition on all sides, except the bottom surface which is blocked.” Ex. 1003, ¶ 113. As an initial matter, Kim fails to disclose that the side surfaces are open and unblocked to allow the CVD process to impact them. Dr. Banerjee’s description of the CVD process fails to acknowledge that the process does not necessarily fill all structures, and that CVD can be designed to not fill specific structures. As explained above, one of several methods to create air-gaps in trenches “tak[es] advantage of the non-conformity of a CVD dielectric layer to create air cavities located inside trenches,” which contradicts Dr. Banerjee’s argument. Ex. 2009, 65; KuhnII, ¶124.

Because Dr. Banerjee fails to identify Kim disclosures or other evidence or reasoning that supports the motivation to deposit filling material on all sides of the memory device beyond identifying a generic depositing process, the presented evidence is nothing more than expert testimony that “conclude[s] with the stock phrase to one skilled in the art it would have been obvious to perform the [claims],” which is insufficient to support a determination of obviousness. *Innogenetics, N.V. v. Abbott Labs.*, 512 F.3d 1363, 1373 (Fed. Cir. 2008). And the mere existence of

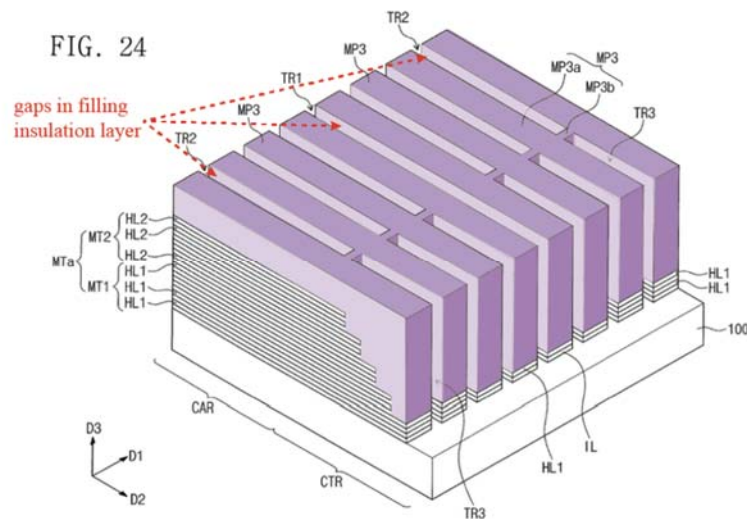
filling material on one side of a memory device and a CVD process in Kim does not provide a reason that a POSITA would have extended that filling material to all sides of the memory device. KuhnII, ¶124. Accordingly, it would not have obvious to a POSITA that Kim's filling material would extend to all sides of a memory device just because a CVD process has been used. KuhnII, ¶126; Pet., 35, Ex. 1003, ¶ 113.

Dr. Banerjee next argues that a general desire for symmetric designs makes it obvious that the insulation material would cover the stack structure instead of being deposited on only a few sides (Ex. 1003, ¶ 113), but this argument ignores that Kim's device is intentionally asymmetrical. KuhnII, ¶127. For example, Kim's device is different in the mutually perpendicular D1 and D2 directions, as depicted in the figures below. *Id.*, ¶128.

FIG. 3



Kim, Fig. 3, *also* Pet. 36.



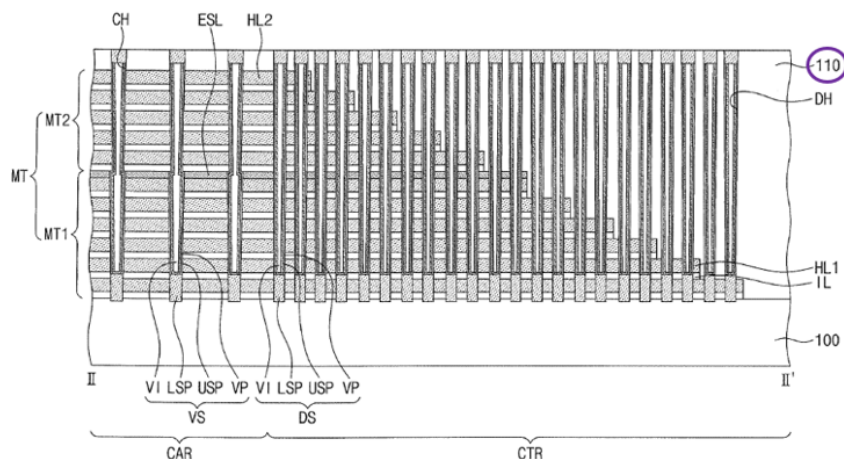
Kim, Fig. 24.⁷ As seen in the reproduced figures above, Kim’s stack structure extends in the D2 direction and not in the D1 direction, and therefore Petitioner’s allusions to Kim’s device being symmetric or desiring symmetry are directly contradicted. In contrast, the ’031 teaches a different device structure in which the staircase structure can “extend[] along the x-y plane” (instead of only extending along the x or y direction) and can “surround memory structure 1100 along the x-y plane.” ’031, 13:27-28 (“Dielectric pairs of different tiers can be etched to **form staircases extending along the x-y plane.**”), 22:30-32 (“First staircase region 1121 and second staircase region 1122 can each **surround memory structure 1100 along**

⁷ As explained in §VII.A.1, the Fig. 24 embodiment and the embodiment relied on by Petitioner do not differ in their disclosures about the issue of interest.

the x-y plane.”). Simply put, Kim and the '031 teach different memory devices with a different staircase design. KuhnII, ¶129.

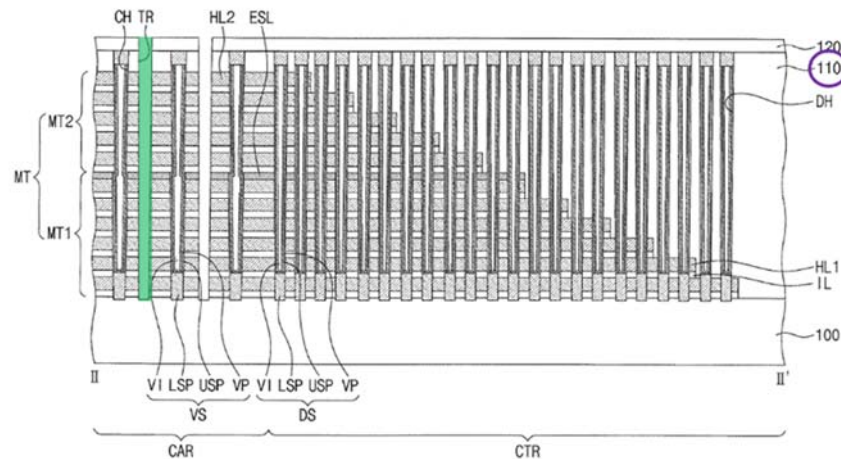
These differences exist between the '031 and Kim because Kim's filling insulation is not meant to encircle the stack structure. *Id.*, ¶129. As explained above in Section VII.A.1, Kim discloses that **trenches** filed with common source plugs are formed **after** the forming of the **filling insulation layer 110** (purple), such that the trench openings and subsequent features divide the stack structure into blocks. KuhnII, ¶130; Kim, Figs. 6-13, 12:15-33. As depicted below, the trenches TR are formed “between the mold structures MT” used to form the steps. KuhnII, ¶131; Kim, 12:15-19. Thus, even if it were obvious to extend the insulating layer 110 in all four directions, in view of the **trenches** Kim still fails to disclose or render obvious that the stack structure is encircled by the filling insulation layer 110 (or any other structure) at the sides of the stack along the D1 direction. KuhnII, ¶132.

FIG. 12



Kim, Fig. 12.

FIG. 13



Ex. 1005, Figs. 12-13 (annotated).⁸

Realizing that Kim’s insulation layer does not surround the staircase structure, Petitioner goes beyond Kim’s disclosures and attempts to bring in teachings from another reference, Park (Ex. 1011, “Park”), to explain how Kim “would have been understood,” but the teachings of Park do not explain Kim’s disclosures. KuhnII, ¶133. Petitioner relies on Park to imply that Kim would have used Park’s “common technique [] to isolate the blocks” with “common source lines 102” that have a “conductive core” and “an outer portion of insulating material” (Pet. 36-37), but

⁸ Figures 12 and 13 are “cross-sectional views taken along line II-II’ of FIG.3,” which runs along the direction D2 in the connection region (CTR) and direction D1 in the cell array region (CAR). See Ex. 1005, Fig. 3, 4:29-32.

Kim does not reference Park, Petitioner does not propose combining Kim and Park, and Petitioner does not argue or establish that Park's teachings are the only way to implement Kim's teachings such that it is how Kim "would have been understood." KuhnII, ¶134. Even if Park's common source lines was one possible technique that could have been used in Kim's memory device, Petitioner fails to establish that it would have been obvious for a POSITA to use that technique in Kim. KuhnII, ¶135; *Costco Wholesale Corp. v. Robert Bosch LLC*, IPR2016-00035, Paper 23 at 8 (PTAB Aug. 12, 2016) ("[A]n understanding that something 'could be applied to the problem at hand' does not establish that it would have been obvious to do so at the time the [] invention was made."). Finally, as Dr. Banerjee acknowledges (Ex. 1003, ¶116), Kim's technique uses common source lines extending only extending in one direction (which Dr. Banerjee maps to the D2 direction in Kim), which does not "surround" the stack structure (KuhnII, ¶136):

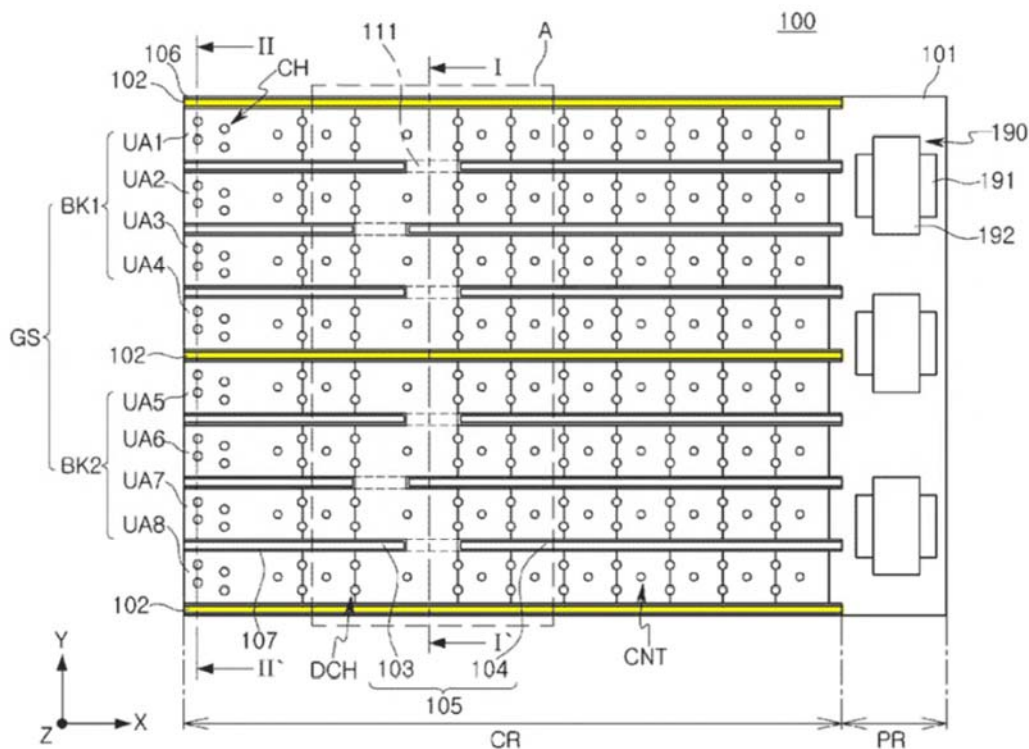


FIG. 3

Ex. 1011, Fig. 3 (annotated by Petitioner at Pet. 37).

To the extent that Petitioner's argument is that the insulating liners of the common source in combination with the filling insulation layer 110 show the filling structure of the '031, this combination of elements still fails to render obvious surrounding the stack structure at least because Kim's device in the -D2 direction is neither depicted nor described, and Petitioner has not shown that it would have been obvious to surround the stack structure on that side for at least the reasons discussed above. KuhnII, ¶137.

Kim, therefore, does not disclose or render obvious a filling structure “surrounding” a multiple-stack staircase structure as required by limitation [1.d]. KuhnII, ¶138.

B. Claims 4: Kim Does Not Disclose or Render Obvious That “the Supporting Pillar Is Filled with ... a Pillar-Support Material Surrounded by the Insulating Material”

Petitioner’s argument that Kim’s dummy structures (which Petitioner maps to the claimed “supporting pillars”) include a conductive core that is a “pillar supporting material” (Pet., 55-56) fails because Kim does not even disclose a conductive core, let alone disclose or render obvious one that is a “pillar-support material.” KuhnII, ¶¶139-174.

Claim 4 recites “the supporting pillar is filled with ... a pillar-support material surrounded by the insulating material.”⁹ The ’031 describes “supporting pillar” and “pillar support material” in detail. KuhnII, ¶140. For example, the ’031 specification explains that the 3D NAND memory device “includes multiple stacks of word lines arranged along the direction perpendicular to the substrate” in which “supporting pillars are used in the fabrication process to provide mechanical support and prevent pattern collapse.” ’031, 1:23-25, 33-36. The ’031 explains that the

⁹ Patent Owner’s arguments are focused on the portion of the claim that Petitioner mapped to Kim.

process of forming the supporting pillars involves depositing dielectric material in a pillar hole¹⁰ to form an insulating liner and the metal material is deposited to fill up the pillar hole. '031, 25:15-21. The supporting material used in the supporting pillars is important because, as the name suggests, it provides support to the pillars. '031, 25:15-21. For this reason, a material must have “sufficient stiffness and/or support functions” to be considered as a supporting material. '031, 18:26-28. KuhnII, ¶141. Support material, for example, can include “copper, cobalt, nickel, and aluminum.” '031, 18:28-30; KuhnII, ¶142.

Petitioner relies on Kim’s dummy structures as the alleged supporting pillar filled with a pillar support material surrounding by insulating material, but Kim’s dummy structures are single layer structures that do not map to this element. KuhnII, ¶143. As an initial matter, Kim discloses two possible relationships between its dummy structures (corresponding to the “supporting pillar”) and vertical channel structures (corresponding to the “semiconductor channels”), neither of which satisfies claim 4. KuhnII, ¶149. Claim 4 requires that “the supporting pillar and the semiconductor channel **are filled with different filling layers**” and that “the

¹⁰ A pillar hole is formed by etching through at least one of the filling structure and the multiple-stack staircase structure. '031, 2:57-63.

supporting pillar is filled with ... a pillar-support material surrounded by the insulating material.” Kim discloses that the **dummy structures may be identical to the vertical channel structures** (Kim, 9:31-37, 11:49-53) **or be formed from different material than the vertical channel structures** (*id.*, 13:29-33). KuhnII, ¶149. Kim does not disclose claim 4 when the dummy structures and vertical channel structures are made from the same material because, again, claim 4 requires that the “supporting pillars [allegedly Kim’s dummy structures] and the semiconductor channel [allegedly Kim’s vertical channels] are filled with **different filling layers**.” See Claim [4.a]; KuhnII, ¶150. Kim also does not disclose claim 4 when the dummy structures and vertical channel structures are made from different materials because, as discussed further below, for these structures Kim discloses only insulator/semiconductor material¹¹—silicon oxide, silicon nitride, silicon oxynitride, polysilicon (*id.*, 13:33-36)—which cannot be used to form a “conductive core,” i.e. the type of core upon which Petitioner bases its argument. KuhnII, ¶151. Indeed, Kim has no disclosure that the material for the dummy structure forms a conductive core. Kim also does not describe any of its materials as support materials that are suitable for forming a supporting pillar, as discussed further below. Kim’s

¹¹ In contrast, the ’031 explains that the “pillar support material” are metals such as “copper, cobalt, nickel, and aluminum.” ’031, 18:28-30.

lack of disclosure is confirmed by the fact that Petitioner does not argue that the reference expressly discloses limitation [4.b]. *Id.*, ¶152.

Petitioner’s argument that Kim’s dummy structures “**could have been made with a conductive core**” (Pet., 55-56) is not based on any disclosure of a conductive core and incorrectly assumes that a conductive core is a “pillar support material.” KuhnII, ¶142. First, Kim does not disclose a conductive core in the cited dummy structures. Indeed, Petitioner appears to acknowledge—based on obviousness arguments—that Kim does not expressly disclose that its dummy structures include either a pillar-support material or a conductive core surrounded by the insulating material. Pet., 55-56. Rather, Kim’s dummy structures are “formed **of a single layer**, e.g., a silicon oxide layer, a silicon nitride layer, a silicon oxynitride layer, or a polysilicon layer” (Kim, 13:33-36), and thus are not conductive cores surrounded by an insulating material. KuhnII, ¶143.

Second, even if Kim disclosed or rendered obvious a conductive core, it would not have been obvious to a POSITA that the mere inclusion of a conductive core would also constitute inclusion of a “pillar support material” because not all conductive (metal) cores have the required stiffness and/or support function to be considered a supporting material. *Id.*, ¶144. Petitioner’s attempt to backfill this absent disclosure instead illustrates that the entire argument relies on impermissible hindsight. *Sensonics, Inc. v. Aerosonic Corp.*, 81 F.3d 1566, 1570 (Fed. Cir. 1996)

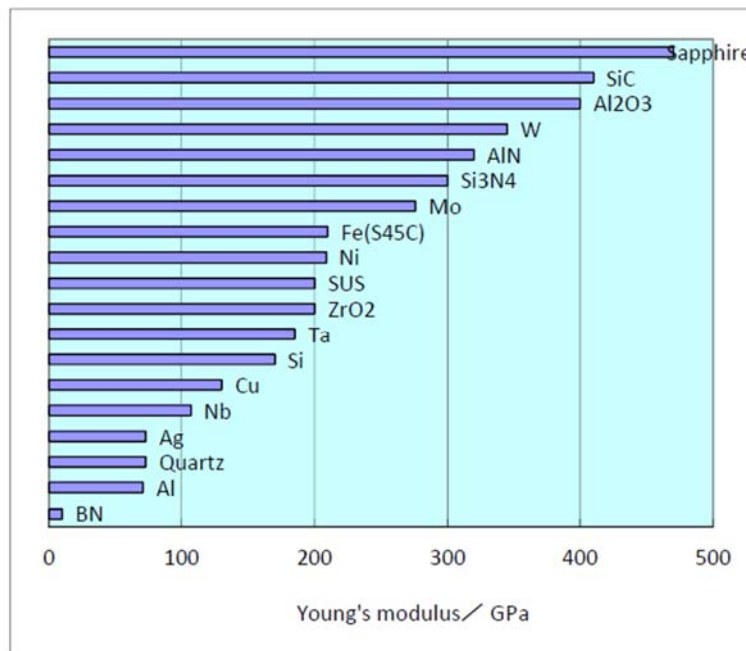
(“To draw on hindsight knowledge of the patented invention, when the prior art does not contain or suggest that knowledge, is to use the invention as a template for its own reconstruction—an illogical and inappropriate process by which to determine patentability.”).

Petitioner’s obviousness arguments rest on conclusory statements and are without merit. Based on Kim’s disclosure that dummy structures *may* be different from the vertical channel, Petitioner improperly jumps to the conclusion that “a POSITA would have understood that Kim’s dummy structures could have been made with a conductive core (the supporting material) and insulating liner,” without explaining why a POSITA would have been motivated to do so. Pet., 55-56; KuhnII, ¶154. Petitioner has not shown that Kim’s device needs or would even benefit from additional supporting structures. KuhnII, ¶155; *Belden Inc. v. Berk-Tek LLC*, 805 F.3d 1064, 1075 (Fed. Cir. 2015) (“[It does not] suffice[] for obviousness that a variation of the prior art would predictably work, but requires consideration of whether, in light of factors such as ‘design incentives and other market forces,’ the hypothetical skilled artisan would recognize the potential benefits and pursue the variation.”). Therefore, Petitioner has not shown that a POSITA would have been motivated to modify Kim’s dummy structures to include the alleged conductive core, or one that is a pillar-support material as required by claim 4. KuhnII, ¶155.

Dr. Banerjee attempts to explain away these deficiencies and argue obviousness based on an incorrect understanding of elastic and deformation properties of metals. For example, Dr. Banerjee asserts that it would have been obvious to include a metal core because metals provide a more suitable support material based on their superior elastic properties as measured by the bulk modulus and the Young modulus. Ex. 1003, ¶ 215; KuhnII, ¶157. However, there is no correlation between electrical conductivity and Young's modulus. For example, there are some materials (such as indium) with very good conductivity and poor Young's modulus (11 GPa), some materials (such as copper) with very good conductivity and moderate Young's modulus (130 GPa), and some materials such as iridium with very good conductivity and excellent Young's modulus (528 GPa). KuhnII, ¶148. Furthermore, Dr. Banerjee cites two references with limited disclosures, Ex. 1021 and Ex. 1022, to support his argument. Ex. 1003, ¶ 215; KuhnII, ¶156. These references do not support Dr. Banerjee's argument that metals are better as support materials than silicon nitride, silicon dioxide, or polysilicon. For example, the Young's modulus values¹² for silicon nitride—257 GPa. (Ex. 1022, 26)—and polysilicon—150 GPa (Ex. 1022, 12, 17)—are comparable to those of the four metals cited in '031, namely copper (130 GPa), aluminum (70 GPa), cobalt (209

¹² Young's modulus value for silicon dioxide could not be located in Ex. 1022.

GPa) and nickel (200 GPa). KuhnII, ¶160. Indeed, the Young's modulus for silicon nitride is greater than the Young's modulus for all four metals, the Young's modulus of polysilicon is roughly midway in value for the four metals (and very close to that of copper), and the Young's modulus of "glass" is in a range between aluminum and copper. KuhnII, ¶160. In other words, there is no basis to conclude that metals are generally better as support materials than silicon nitride, silicon dioxide, or polysilicon. *Id.* That is, contrary to Dr. Banerjee's statement, there is no general rule that the Young modulus of conductors is higher than that of insulators. And, as discussed earlier, there is no correlation between a material being conductive and its stiffness. Indeed, Petitioner's own source, Ex. 1021, shows that conductors (Al, W) and insulators (BN, Al₂O₃) can both be positioned at low and high ends of the Young modulus chart. KuhnII, ¶¶161-162.



Ex. 1021. This is why the '031 explains that stiffness is relevant to whether a material is a support material ('031, 18:26-28), rather than general categories such as whether a material is a “conductive core.” KuhnII, ¶163.

Additionally, Dr. Banerjee's attempts to show obviousness by pointing to metal and conductive cores disclosed by other references are unsuccessful because he does not sufficiently explain why a POSITA would have been motivated to modify Kim using these references. Ex. 1003, ¶¶ 156-157; KuhnII, ¶164. For example, Dr. Banerjee's argument that it would have been obvious to use Tessariol's conductive vias in Kim's dummy structures to show that the dummy structures are filled with pillar-support material is unconvincing. KuhnII, ¶165. First, Dr. Banerjee's argument relies on Tessariol's disclosure that its “dummy structures may

individual[ly] comprise a conductive core [] and an insulative periphery” (Tessariol, [0049]), but thus is subject to the same issue that a “conductive core” by itself is not necessarily sufficient to read on claim 4. Tessariol does not disclose the type of metal. KuhnII, ¶166. Second, Tessariol’s conductive vias are specific to its unique device and cannot be simply incorporated into Kim’s memory device without sufficient explanation and motivation for doing so. *Id.*, ¶167. Dr. Banerjee’s conclusion that using Tessariol’s conductive vias in Kim would provide support and interconnect functions completely disregards the fact that Kim does not need or even benefit from additional interconnecting structures. Ex. 1003, ¶ 217; KuhnII, ¶168. Kim does not disclose any circuitry (either transistors or interconnects) under the memory array or the staircase (also called a “PNC architecture”). KuhnII, ¶169. If there is no circuitry under the array or the staircase, there is no need to create connections to that circuitry. *Id.*, ¶169. As such, Kim has no clear motivation to make the dummy structures conductive for an interconnect function. *Id.* Tellingly, Petitioner does not explain why Kim’s device would need or benefit from additional interconnecting structures. *Id.*, ¶170.

Other references that Petitioner points to—such as Ex. 1012 (U.S. Patent No. 9,768,186)—do not include information about elastic properties that show pillar-supporting capabilities and, like Tessariol, merely mentions pillars with metal cores. Ex. 1012, 4:60-5:12; KuhnII, ¶171. Therefore, these references are subject to the

same issues discussed above in connection with Tessariol. KuhnII, ¶171. Ultimately, Petitioner has not sufficiently explained why a POSITA would have been motivated to replace Kim's insulator/semiconductor materials with the metal and conductive cores disclosed by U.S. Patent No. 9,768,186 and Tessariol, and even if Petitioner had done so, it has failed to show that such conductive core would have been a pillar support material. *Id.*

Finally, Petitioner and Dr. Banerjee ignore significant issues of thermal expansion mismatch that would result from their proposed modification of Kim. All materials have a thermal expansion coefficient, which indicates the amount a material will expand over a given temperature change. If two adjacent materials are subjected to high temperature, as routinely occurs in semiconductor manufacturing, differences in the thermal expansion coefficient between these materials can cause stress and lead to it causes structural damage such as dislocations or crack. As an initial matter, Petitioner simply does not address this issue, and indeed does not even consider what if any metals could work for adding a conductive core to Kim's dummy structures without causing stress or structural damage that would have dissuaded a POSITA from making the proposed modification. The only metal Petitioner proposes using for the conductive core, anywhere in its Petition, is copper (for Ground 2, Pet. 86), which has a significantly different thermal expansion coefficient than Kim's insulating materials. For example, copper has a thermal

expansion coefficient of 16.6, and silicon oxide has a coefficient of 0.64. Ex. 1021 at 3, 9. During subsequent processing, such an anneal or metal deposition step, the structure of copper surrounding by an insulating liner would likely lead to cracking. *See generally* Ex. 1023 (discussing high temperatures for various processing steps). Thus, it is clear that Petitioner did not consider thermal expansion issues that would be subject to stress and potentially result in structural damage. KuhnII, ¶172.

Accordingly, Kim does not disclose or render obvious the supporting pillar filled with a “pillar support material” as recited in claim 4. KuhnII, ¶¶173-174.

VIII. GROUND 2: TESSARIOL DOES NOT DISCLOSE OR RENDER OBVIOUS CLAIMS 1, 2, 4-5

Tessariol does not disclose or render obvious the Challenged Claims¹³ at least because Tessariol’s alleged filling structure does not surround (encircle, §V.A) a multi-stack staircase structure as required by limitation [1.d] of the sole independent claim, claim 1. Furthermore, Tessariol does not disclose claims 4-5 because its conductive core is not a “pillar-supporting material” (claim 4) made of copper, cobalt, nickel, or aluminum (claim 5). KuhnII, ¶¶175-212.

¹³ Petitioner does not assert Ground 2 against claim 3. Pet. 8.

A. Independent Claim 1: Tessariol Does Not Disclose or Render Obvious Limitation [1.d] Because Tessariol’s Alleged Filling Structures Do Not “Surround” Its Steps

Petitioner fails to show that Tessariol discloses or renders obvious “a filling structure surrounding the multiple-stack staircase structure” as required by limitation [1.d] because none of the features identified by Petitioner, either individually or in combination, surrounds Tessariol’s steps. KuhnII, ¶¶176-201. As discussed in §V.A, the term “surrounding” means “encircling.” Tessariol does not disclose or render obvious a filling structure that encircles Tessariol’s steps. KuhnII, ¶176.

Petitioner incorrectly identifies Tessariol’s insulating material 48 in Fig. 6, dielectric material 74 in Fig. 11, and insulator material 86 in Fig. 17 as the alleged filling structures (Pet., 66-70)—these features do not “surround” Tessariol’s steps, as required by limitation [1.d]. KuhnII, ¶¶177-178. Instead, these features are located above the steps in Tessariol and there is no disclosure that they extend to encircle the steps. KuhnII, ¶178.

Based on the proper construction of “surrounding” (§V.A), the Board correctly recognized that to read on limitation [1.d], the “Petitioner must show that Tessariol’s [alleged filling structures] insulating material 48, dielectric material 74, and insulation material 68 encircle, or are all the way around, Tessariol’s staircase structures.” *Id.*, ¶179. Petitioner, however, fails to do so, as explained in detail below. KuhnII, ¶180.

First, Tessariol’s “insulating material 48” (shown below) covers but does not surround Tessariol’s steps. KuhnII, ¶181.

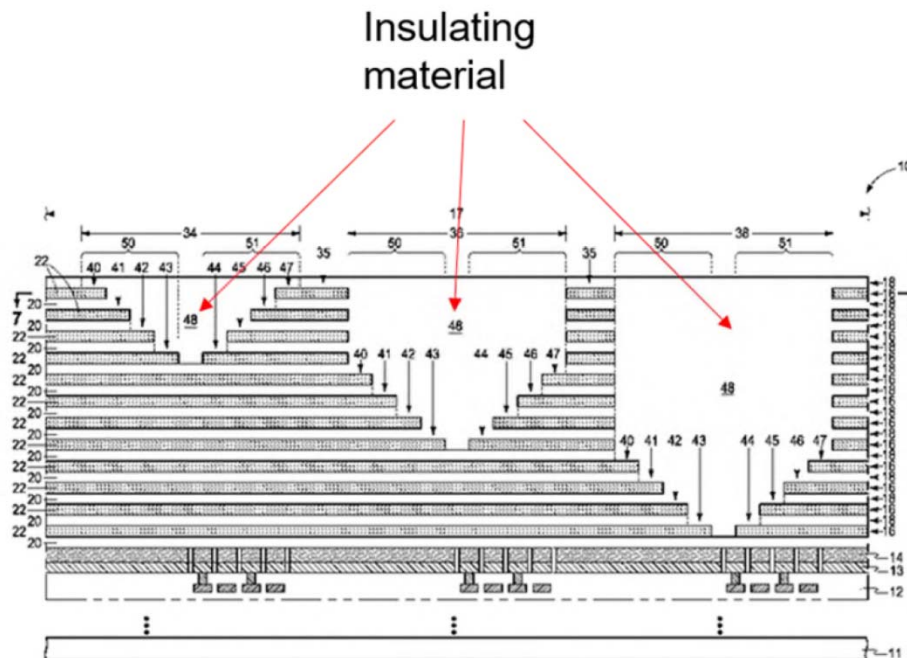


FIG. 6

Tessariol, Fig. 6 (annotated by Petitioner at Pet. 67). Tessariol discloses that “[a]n insulating material 48 (e.g., silicon dioxide and/or silicon nitride) is **above** steps 40-47.” Tessariol, [0034] (emphasis added). Tessariol recites similar language in its claims, disclosing “the stair step structure comprising insulating material **above** the steps.” Tessariol, Claims 1, 8, 16 (emphasis added). This is the full extent of Tessariol’s relevant disclosure. KuhnII, ¶182.

In Tessariol’s figures, **insulating material 48** is depicted to be above the steps, and between **landings 35**, as seen in Fig. 6 (cross-section view) and Fig. 7 (top view) below. KuhnII, ¶183.

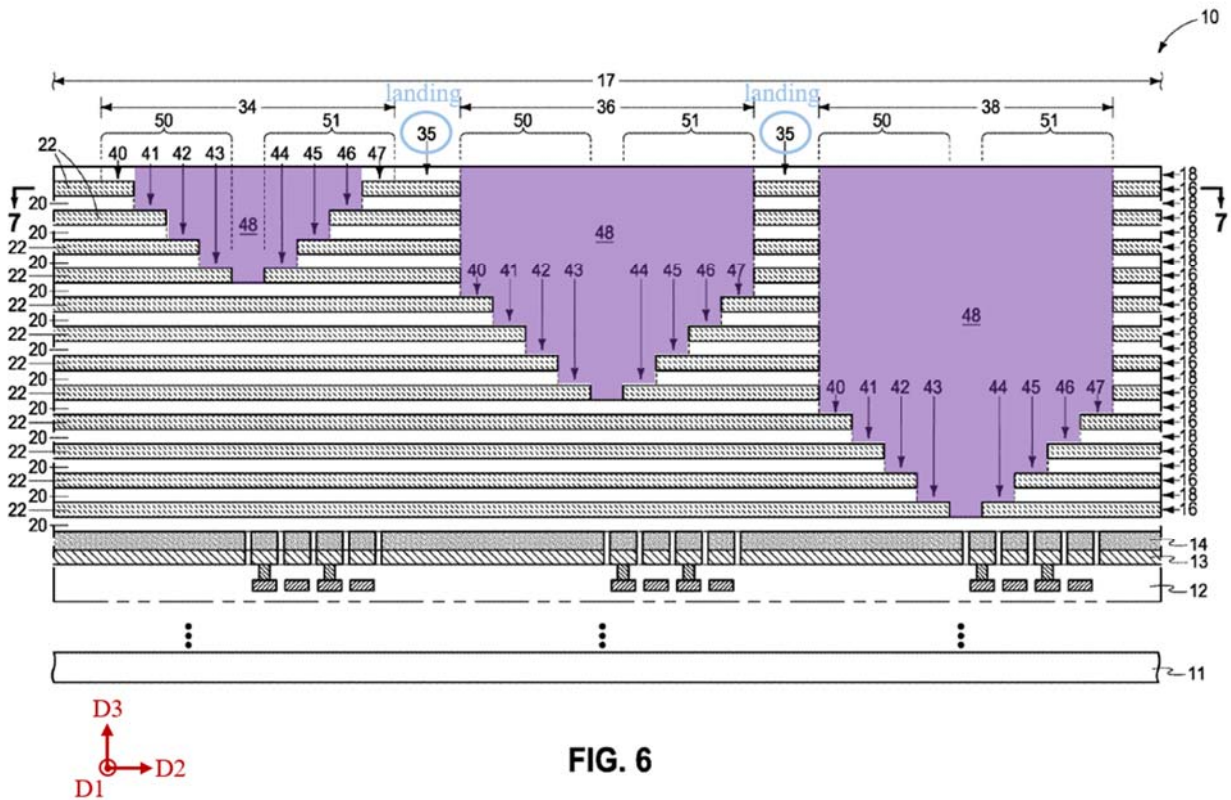


FIG. 6

Tessariol, Fig. 6 (annotated).

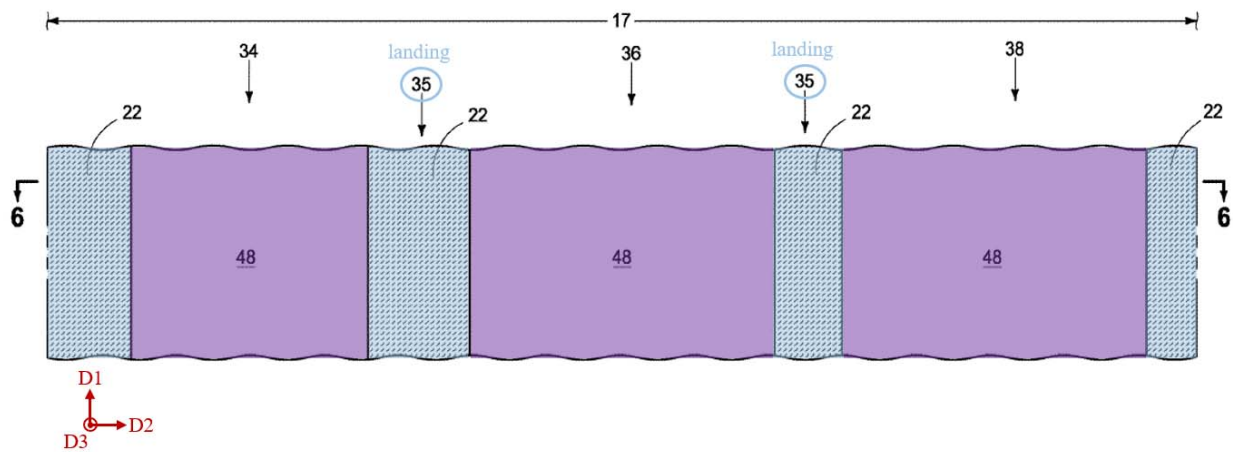


FIG. 7

Tessariol, Fig. 7 (annotated).

As shown in Tessariol's Figs. 6-7, the steps are covered by **insulating material 48** from above and divided into "stadiums" by **landings 35** in the D2 direction.¹⁴ Tessariol, [0035]. However, as Dr. Banerjee acknowledges in the declaration, "the figures in Tessariol do not show the outer ends/sides of the device" (i.e., in the D1 and D2 directions in Fig. 7). Ex. 1003, ¶ 184; *see also* Pet. 70 ("Note that Tessariol does not expressly depict the lateral ends of the device."). Nor does Tessariol describe covering the ends of the device with the insulating material. Therefore, Tessariol does not disclose **insulating material 48** surrounding, or encircling, the steps. KuhnII, ¶184.

Second, Tessariol's "dielectric material 74" divides but does not surround Tessariol's steps. KuhnII, ¶185.

¹⁴ The D1, D2, and D3 directions are defined in a way similar to the D1, D2, and D3 directions of Kim.

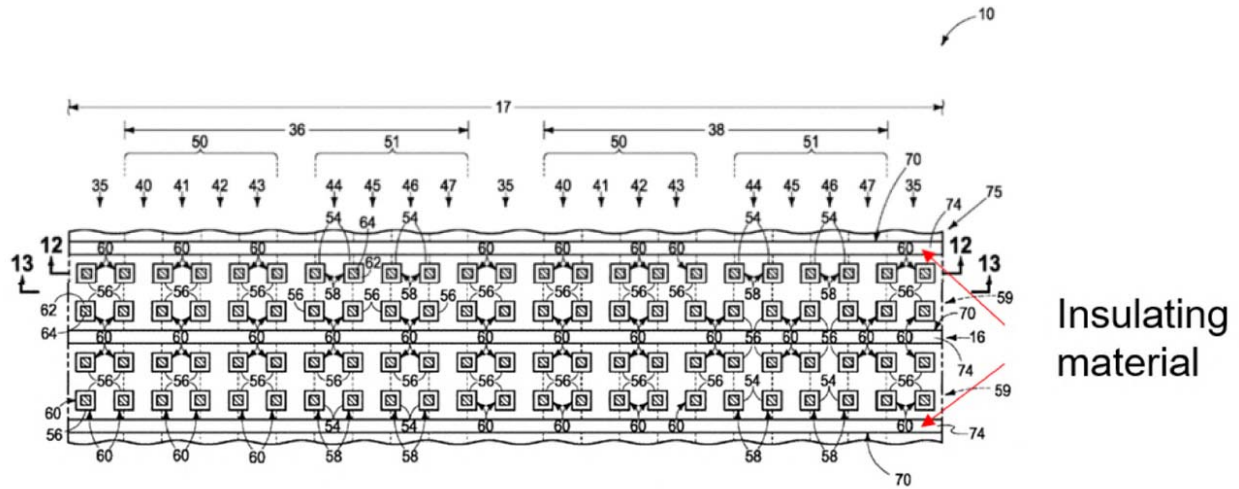


FIG. 11

Tessariol, Fig. 11 (annotated by Petitioner at Pet. 68). Tessariol’s **dielectric material 74** is formed in “trenches 70” that “extend elevationally into vertically-alternating tiers.” KuhnII, ¶186; Tessariol, [0041], [0043].

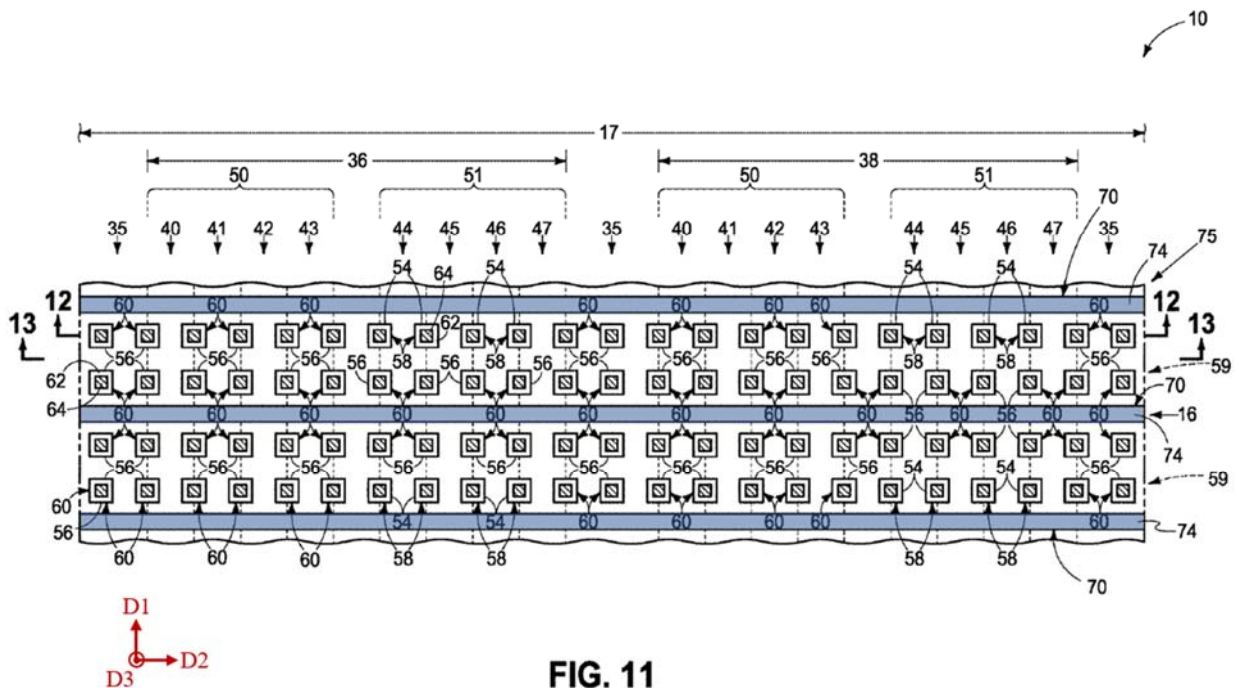
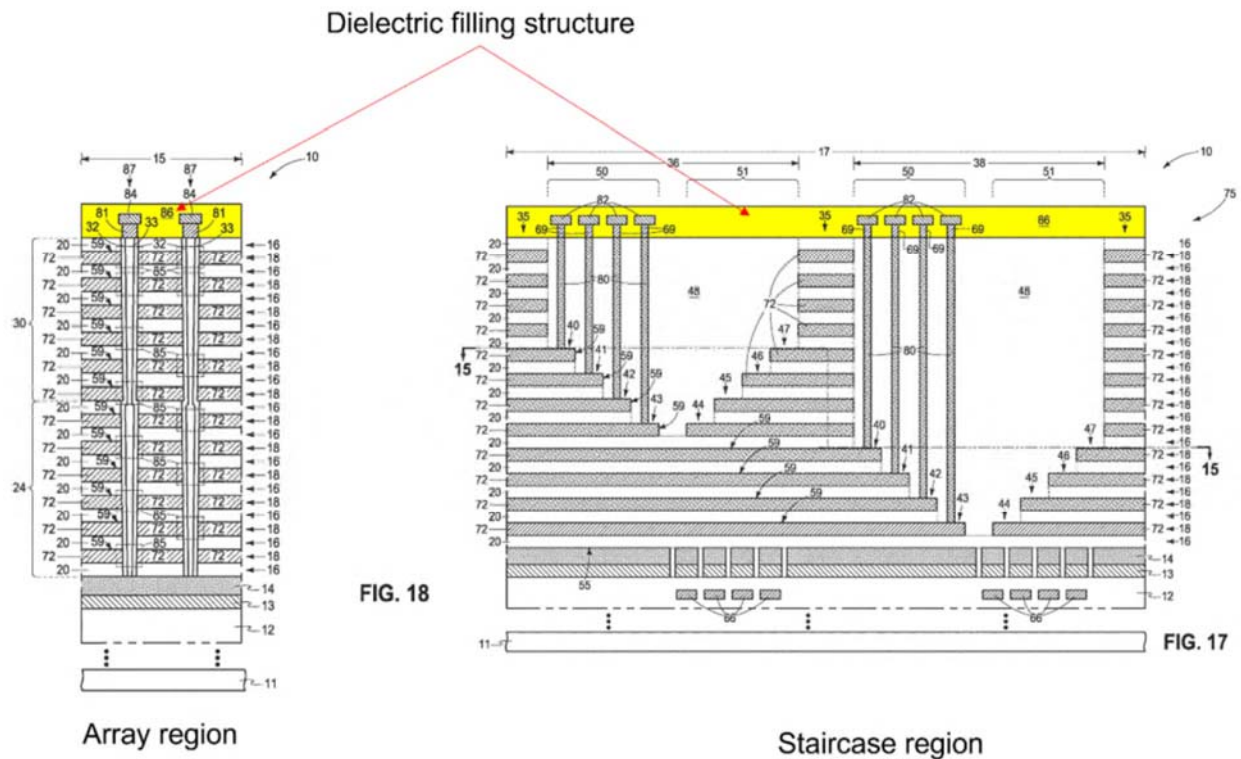


FIG. 11

Tessariol, Fig. 11 (annotated). As seen above, Tessariol's "trenches 70" extend along the D2 direction and divide the alternating tiers along the D1 direction. Tessariol, [0041], [0043]. Tessariol does not suggest that such a trench is present at the ends of the D1 direction. KuhnII, ¶187. Furthermore, the trenches are "horizontally-elongated" and "formed to extend elevationally into vertically alternating tiers 16, 18." Tessariol, [0041]; KuhnII, ¶187. Based on these teachings, the Board correctly questioned how Tessariol's dielectric material 74 could be deposited around the staircase structures. DI, 24-25. Thus, Tessariol fails to disclose that the stack is encircled by any structure at the ends of the device along either the D1 or D2 directions. KuhnII, ¶188. As noted earlier, this is confirmed by Dr. Banerjee. *See* Ex. 1003, ¶ 184 ("I note that the figures in Tessariol do not show the outer ends/sides of the device."); *see also* Pet. 70 ("Note that Tessariol does not expressly depict the lateral ends of the device."). *Id.*

Third, Tessariol's "insulator material 86" covers but does not surround Tessariol's steps. KuhnII, ¶189.



Tessariol, Figs. 17-18 (annotated by Petitioner at Pet. 69). Contrary to Petitioner’s assertion, Tessariol’s insulator material 86 in the figures above covers only the top surface of the stacks. KuhnII, ¶190; Pet., 68-69. Insulator material 86 does not surround or encircle the staircase structure. KuhnII, ¶191. While Tessariol discloses that “[i]nsulator material 86 ... is shown surrounding components [conductive extensions] 69, [interconnect lines] 82, [conductive extensions] 81, and [conductive lines] 84” (Ex. 1006, [0046]), these components are **above** the stacks, as seen in the figures above. KuhnII, ¶192. Based on this disclosure, the Board correctly questioned how Tessariol’s insulator material 86 could encase the entire stack

structure when the insulator material simply is formed above components 69, 81, 82, and 84. DI, 25. KuhnII, ¶193.

Petitioner therefore fails to show that Tessariol discloses a filling structure that encircles a multi-stack staircase structure as required by limitation [1.d]. KuhnII, ¶194.

Petitioner's and its expert's arguments also fail to show that Tessariol renders obvious limitation [1.d]. To show that it would have been obvious for Tessariol's filling material to encase the memory device, Dr. Banerjee first incorrectly conflates planarizing with surrounding, declaring that "filling insulators are understood to surround the stack structures to create a planar surface for the upper-level metal layer." Ex. 1003, ¶183 (citing Ex. 1023, 14). However, the cited exhibit is about planarization, and does not include teachings about "encas[ing] all sides of the memory device," as Dr. Banerjee alleges. KuhnII, ¶195. Planarizing simply refers to making the uppermost layer flat and does not suggest that there is filling material on the sides of the staircase structure in Tessariol. *Id.*, ¶196. Additionally, as discussed in detail with regards to Kim (See §VII.A) there are a variety of well-known techniques for creating embedded air-gaps in planarized structures, and so it is incorrect to assume that filling material would be on the sides of Tessariol that are not depicted or described. Thus, the expert's assertion regarding what was conventional, routine, and obvious, is conclusory, unsupported, and contradicted by

Tessariol’s disclosures. Ex. 1003, ¶ 183; KuhnII, ¶197. Petitioner then attempts to equate Tessariol’s dielectric material and insulator material to Kim’s filling insulation layer to show that it would be obvious to combine the two references to disclose claim 1 (Pet., 70), but this reasoning is misplaced because, like Tessariol, Kim fails to teach [1.d] and therefore the combination of the two references also do not disclose claim 1. See §VII.A; KuhnII, ¶198. Petitioner’s next argument that various combinations of insulating material 48, dielectric material 76 within trenches, and/or insulation material 86 teach the filling structure of the ’031 is incorrect. KuhnII, ¶199. Even the combination of these elements fails to surround the stack structure, as Tessariol does not teach or suggest an insulator material at the ends of Tessariol’s device in either the D1 or D2 direction in any of the figures or in the specification. *Id.*, ¶200.

Accordingly, Tessariol does not disclose or render obvious a filling structure “surrounding” a multiple-stack staircase structure as required by limitation [1.d]. KuhnII, ¶201.

B. Claims 4-5: Tessariol Does Not Disclose That “the Supporting Pillar Is Filled with ... a Pillar-Support Material Surrounded by the Insulating Material”

Petitioner’s argument that Tessariol’s dummy structures (which Petitioner maps to the claimed “supporting pillars”) include a conductive core that is a “pillar supporting material” (Pet., 83-84) fails because Tessariol does not disclose or render

obvious that the conductive core is a “pillar-support material” as required by claim 4. KuhnII, ¶202.

Claim 4 recites “the supporting pillar is filled with ... a pillar-support material surrounded by the insulating material.”¹⁵ As explained in connection with Ground 1, the ’031 explains that a material must have “sufficient stiffness and/or support functions” to be considered as a supporting material. ’031, 18:26-28; KuhnII, ¶203. Support material, for example, can include “copper, cobalt, nickel, and aluminum.” ’031, 18:28-30; KuhnII, ¶204.

Petitioner’s argument that Tessariol discloses claim 4 appears to rest solely on the argument that Tessariol’s conductive core is a “pillar support material” because the material is a metal (Pet., 84-86), but not all metals are pillar support materials, as explained in Section VII.B. KuhnII, ¶205. Tessariol merely discloses a conductive core. Tessariol, [0049]. Tessariol does not disclose the type of metal in its conductive core and does not disclose that the metal is a support material. KuhnII, ¶206. Tellingly, the Petition provides almost no analysis for this limitation. Pet., 84; KuhnII, ¶207. For example, Petitioner does not argue that Tessariol’s metal has sufficient stiffness and/or support functions, or even that its conductive core has a

¹⁵ Patent Owner’s arguments are focused on the portion of the claim that Petitioner mapped to Tessariol.

supporting function. KuhnII, ¶208. Accordingly, Petitioner has not shown that Tessariol discloses or renders obvious this limitation. KuhnII, ¶209.

In connection with dependent claim 5, which depends from claim 4, Petitioner erroneously argues that because the conductive core can be a metal material, a POSITA would have understood that Tessariol discloses that the metal may be “copper, cobalt, nickel, and aluminum” (i.e., the claim language)—without providing any motivation for using any of those materials in Tessariol’s dummy structures. Pet., 86; KuhnII, ¶210. This is improper. *In re Stephan Co.*, 868 F.3d 1342, 1346 (Fed. Cir. 2017) (“[T]here must be a motivation to make the combination and a reasonable expectation that such a combination would be successful, otherwise a skilled artisan would not arrive at the claimed combination.”); *see also Sensonics, Inc.*, 81 F.3d at 1570 (“To draw on hindsight knowledge of the patented invention, when the prior art does not contain or suggest that knowledge, is to use the invention as a template for its own reconstruction—an illogical and inappropriate process by which to determine patentability.”). While Petitioner cites a reference that teaches that copper was well-known, Petitioner does not argue that a POSITA would have been motivated or found it obvious to use that material in Tessariol’s dummy structures. KuhnII, ¶211. Indeed, copper poses significant diffusion and contamination issues in the processing of transistors and memory cells and Petitioner

does not explain how a POSITA would have been motivated or found it obvious to use copper (with all its attendant risks) in Tessariol's dummy structures. *Id.*, ¶212.

Accordingly, Tessariol does not disclose or render obvious claims 4-5.

IX. GROUND 3: KIM IN VIEW OF TESSARIOL DOES NOT DISCLOSE OR RENDER OBVIOUS CLAIM 4

Kim in view of Tessariol fails to cure the deficiencies in disclosure that are present in those individual references, and thus do not render obvious claim 4.¹⁶ KuhnII, ¶¶213-223. As a preliminary matter, Petitioner's arguments that "Ground 1 demonstrates that in view of Kim's disclosures and the knowledge of a POSITA, claim 4 is unpatentable" are incorrect because as shown in Ground 1, Kim does not disclose or render obvious claims 1 and 4 of the '031 patent. *See* §VII.A and §VII.B; Pet., 86; KuhnII, ¶213. In Ground 3, Petitioner's reliance on Kim in view of Tessariol to allegedly render obvious dependent claim 4—which indirectly depends on claim 1 (Pet. 86-87)—is misplaced because neither Kim nor Tessariol discloses or renders obvious at least limitation [1.d]. *See* §VII.A and §VIII.A; KuhnII, ¶214. In addition, as explained below, it would not have been obvious to combine these two references. KuhnII, ¶215.

¹⁶ Petitioner asserts Ground 3 against only claim 4. Pet. 8.

As in Grounds 1 and 2, the combination of Kim and Tessariol fails to render obvious claim 4's requirement that "the supporting pillar is filled with ... a pillar-support material surrounded by the insulating material" because Petitioner fails to show that a POSITA would have been motivated to make this proposed combination. KuhnII, ¶216. Petitioner applies Tessariol's conductive core to Kim's dummy structures (which Petitioner maps to the claimed "supporting pillar"). Pet., 125-128. But as explained in connection with Ground 1, a POSITA would not have been motivated to combine Kim and Tessariol. See §VII.A and VII.B. KuhnII, ¶217. For example, Petitioner has not shown that Kim's device needs or would even benefit from additional supporting structures as required by claim 4. KuhnII, ¶218. Furthermore, Kim has a PNC architecture with no transistors or circuitry under the array or the staircase, and therefore has no need to make its dummy structures conductive for an interconnect function. *Id.* Also, contrary to Petitioner's assertion, metals do not always provide better support than insulators. *Id.* Finally, a POSITA would not be incentivized to add a conductive core to Kim because that would unnecessarily complicate the manufacturing process. *Id.*, ¶219.

Moreover, Petitioner's purported motivation to combine Kim and Tessariol relies on Kim's mere disclosure that its dummy and channel structures may be formed on different material to conclude that a POSITA would have considered other types of support materials, such as allegedly taught by Tessariol (Pet., 87-88),

but Petitioner does not explain why a difference in the material in Kim’s dummy and channel structures would prompt a POSITA to incorporate Tessariol’s conductive vias into Kim’s structure. KuhnII, ¶220; See §VII.A and §VII.B. Dr. Banerjee asserts that “it would have been obvious simply to use conductive vias (which have an insulating liner and conductive core) in Kim’s dummy structures, and this would have been beneficial because the process to form them would use the same process steps as the conductive vias.” Ex. 1003, ¶¶ 157, 216. This makes little sense because Kim does not disclose anything about forming conductive vias and, thus, there is no “same process steps as the conductive vias” in the reference. KuhnII, ¶221. Dr. Banerjee also asserts that “the supporting pillar as an active conductive via beneficially could serve two roles (support and interconnect) and reduce the need for additional structures” (Ex. 1003, ¶ 217), but again, Petitioner has failed to show that Kim’s device needs or would benefit from additional supporting structures, or from making its dummy structures conductive for an interconnect function. KuhnII, ¶222.

The only motivation for combining Kim and Tessariol under these circumstances is, therefore, impermissible hindsight. *Nautilus Hyosung Inc. v. Diebold, Inc.*, IPR2016-00633, Pap. 9, *21 (“An assertion that something could be done does not articulate a reason why something would be done by one of ordinary

skill in the art at the time of the invention and, therefore, raises a specter of impermissible hindsight bias in an obviousness analysis.”).

Accordingly, Kim in view of Tessariol does not render obvious claim 4. KuhnII, ¶223.

X. GROUND 4: TESSARIOL IN VIEW OF KIM DOES NOT DISCLOSE OR RENDER OBVIOUS CLAIMS 1-2, 4-5

Neither Tessariol nor Kim discloses a filling structure “surrounding” a multiple-stack staircase structure as claimed by sole independent claim 1 (§VII.A, §VIII.A) and Petitioner does not raise any new arguments that show that their combination cures this fatal deficiency, and thus Tessariol in view of Kim fails to render obvious the Challenged Claims.¹⁷ Petitioner also does not raise any new arguments with respect to dependent claim 5, and therefore Tessariol in view of Kim fails to render claim 5 obvious. KuhnII, ¶¶224-235.

A. Independent Claim 1: Tessariol in View of Kim Does Not Disclose Limitation [1.d]

Petitioner fails to show that Tessariol in view of Kim discloses or renders obvious a filling structure “surrounding” a multiple-stack staircase structure for the same reasons discussed above for Ground 2. See §VIII.A. KuhnII, ¶¶226-233. In Ground 4, Petitioner relies on Tessariol in view of Kim as allegedly rendering

¹⁷ Petitioner does not assert Ground 4 against claim 3. Pet. 8.

obvious claims 1-2 and 4-5 of the '031. *See* Pet. 90-96. KuhnII, ¶227. However, the Petition does not raise any new arguments as to limitation [1.d] (“**a filling structure surrounding the multiple-stack staircase structure**”). *See* Pet. 90-96 (addressing only limitations [1.b], [1.f], and [1.h]); KuhnII, ¶228. As explained in Ground 2 (§VIII.A), Petitioner fails to show that limitation [1.d] is disclosed or rendered obvious by Tessariol, and since no additional arguments are introduced regarding this limitation, Petitioner also fails in Ground 4. KuhnII, ¶229. Petitioner’s motivation statements also do not address l

Furthermore, a POSITA would not have been motivated to combine Tessariol and Kim. *Id.*, ¶230. Petitioner’s statement that “a POSITA would have been motivated to consider Kim’s fill techniques to provide for the planarized surface” is vague and conclusory because the motivation to combine does not state which specific filling technique from Kim would be incorporated into Tessariol and how that incorporation would be executed such that limitation [1.d] would be rendered obvious. *See* §VIII.A; KuhnII, ¶231. Furthermore, Petitioner does not explain why a POSITA would be motivated to combine Tessariol and Kim simply because they both disclose planarized surfaces. KuhnII, ¶232.

Accordingly, Tessariol in view of Kim does not render obvious the Challenged Claims. KuhnII, ¶233.

B. Dependent Claims 4-5: Petitioner Fails to Show That Tessariol in View of Kim Discloses or Renders Obvious “the Supporting Pillar Is Filled with ... a Pillar-Support Material Surrounded by the Insulating Material”

Petitioner does not argue that Tessariol in view of Kim discloses claim 4 and 5, and instead argues that all limitations other than those specifically addressed rely on the same disclosures as Ground 2. Pet. 90. Thus, Tessariol in view of Kim fails to disclose these claims for the same reasons explained in Grounds 1 and 2 above. See §VII.B and §VIII.B; KuhnII, ¶¶234-235.

XI. CONCLUSION

For the reasons above, Petitioner has failed to demonstrate by a preponderance of the evidence that any of the Challenged Claims of the '031 are anticipated or obvious. Accordingly, the Board should find in favor of Patent Owner and uphold the validity of all Challenged Claims.

Dated: January 21, 2025

Respectfully submitted,

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CERTIFICATE OF WORD COUNT

The undersigned certifies that the foregoing PATENT OWNER'S RESPONSE UNDER 37 C.F.R. § 42.120 complies with the type-volume limitation in 37 C.F.R. § 42.24(c)(1). According to the word-processing system's word count, the brief contains 12,688 words, excluding the parts of the brief exempted by 37 C.F.R. § 42.24(c).

Dated: January 21, 2025

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CERTIFICATE OF SERVICE

The undersigned certifies that the foregoing PATENT OWNER'S RESPONSE UNDER 37 C.F.R. § 42.120 was served in its entirety by filing through the Patent Trial and Appeal Case Tracking System (P-TACTS), as well as providing a courtesy copy via e-mail to the following attorneys of record for Petitioner listed below:

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Dated: January 21, 2025

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