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Transcript of Sanjay Banerjee, Ph.D.

Date: December 20, 2024

Case: Micron Technology, Inc. -v- Yangtze Memory Technologies Company, LTD.,
(PTAB)

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WORLDWIDE COURT REPORTING & LITIGATION TECHNOLOGY

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5	BEFORE THE PATENT TRIAL AND APPEAL BOARD	3	QUESTIONS INSTRUCTED NOT TO ANSWER:
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7	MICRON TECHNOLOGY, INC.,	5	(None)
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10	YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,	8	REQUEST FOR PRODUCTION OF DOCUMENTS
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18	SANJAY KUMAR BANERJEE, Ph.D.	16	
19	FRIDAY, DECEMBER 20, 2024	17	
20	Remote Video Teleconference	18	QUESTIONS MARKED
21	7:59 a.m. PST	19	PAGE LINE
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25	Burgundy B. Ryan, RPR,	23	REPORTER'S NOTE:
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8	650.614.7400	8	EXHIBIT DESCRIPTION PAGE
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5 1 BE IT REMEMBERED that, pursuant to Notice 2 of Taking Deposition, and on Friday, December 20, 3 2024, commencing at 7:59 a.m. PST thereof, via 4 remote video teleconference, before me, Burgundy B. 5 Ryan, a Certified Shorthand Reporter in and for the 6 State of California, personally appeared 7 SANJAY KUMAR BANERJEE, Ph.D., 8 a witness called on behalf of PATENT OWNER, and who, 9 having been first duly sworn by me to testify to the 10 truth, was examined and testified as follows: 11 THE VIDEOGRAPHER: Here begins the 12 videotaped deposition of Dr. Sanjay Banerjee in the 13 matter of Micron Technology Incorporated versus 14 Yangtze Memory Technologies Company Limited, in the 15 United States Patent and Trademark Office before the 16 Patent and Trial Appeal Board, case number 17 IPR2024-00790. 18 Today's date is 12/20/2024. 19 The time on the video monitor is 7:59 20 Pacific time. 21 The remote videographer for today is 22 Parker Simpson representing Planet Depos. 23 All parties of this video deposition are 24 attending remotely. 25 Would Counsel please voice-identify	7 1 since this is another proceeding, just bear with me, 2 I need to get those same questions on the record 3 again. 4 What is your address? 5 A. 1742 Canonero Drive, C-a-n-o-n-e-r-o, 6 Austin, Texas 78746. 7 Q. And what is your occupation? 8 A. I'm the Cockrell Chair Professor of 9 Electrical and Computer Engineering at the 10 University of Texas at Austin. I'm also the 11 Director of the Microelectronics Research Center out 12 here. 13 Q. Do you have any materials with you? 14 A. I have an unmarked copy of my declaration 15 and an unmarked copy of the cover page and the 16 claims page of the '031 patent. 17 Q. And the declaration you are referring to is 18 your declaration in IPR2024-790? 19 A. Yes. 20 Q. Do you have any other materials in front of 21 you? 22 A. No. 23 Q. And other than the computer that you're 24 using for the deposition, do you have any other 25 electronic devices with you?
6 1 themselves and state whom they represent? 2 MR. BONNY: Christopher Bonny from Ropes & 3 Gray on behalf of Yangtze Memory Technologies 4 Company Limited, Patent Owner. 5 MR. LANG: Jason Lang from Orrick on behalf 6 of Petitioner Micron. 7 THE VIDEOGRAPHER: The court reporter today 8 is Brooke Ryan representing Planet Depos. 9 The witness will now be sworn. 10 COURT REPORTER: Good morning. My name is 11 Burgundy Brooke Ryan, California CSR No. 11373. 12 (Whereupon, the witness was sworn.) 13 COURT REPORTER: Thank you very much. 14 Counsel, you may proceed. 15 SANJAY KUMAR BANERJEE, Ph.D., 16 having first been duly sworn to tell the whole 17 truth, testified as follows: 18 EXAMINATION 19 By MR. BONNY: 20 Q. Please state your name for the record. 21 A. Sanjay Kumar Banerjee, S-a-n-j-a-y 22 K-u-m-a-r B-a-n-e-r-j-e-e. 23 Q. All right. So I will be going over a 24 number of background questions that you'll recall we 25 just covered a couple of days ago on Wednesday, but	8 1 A. No. 2 Q. And you understand that you are under oath 3 today? 4 A. Yes. 5 Q. Just as a recap, I'll be asking questions 6 during this depositions and you'll be providing 7 answers to those questions. I'll ask that you 8 please wait for me to finish, and I will do the same 9 for you when you're speaking so that we don't talk 10 over each other. 11 Does that make sense? 12 A. Yes. 13 Q. Is there any reason why you cannot testify 14 truthfully and fully today? 15 A. No. 16 Q. And one more item. If I ask a question 17 that you don't understand, please ask for 18 clarification; otherwise, I'll assume that you 19 understand the question. 20 Does that make sense? 21 A. Yes. 22 Q. Have you ever been deposed before, 23 Dr. Banerjee? 24 A. Yes. 25 Q. Approximately how many times?

9 1 A. I think approximately couple dozen times. 2 Q. You mentioned that you're currently a 3 professor at University of Texas at Austin. Do you 4 have any other occupations? 5 A. No. 6 Q. You do also do some consulting work; is 7 that correct? 8 A. That's correct. 9 Q. And how many times have you been retained 10 as a consultant? 11 A. I've listed the cases where I've done some 12 substantial work as in writing reports or being 13 deposed or testifying and my CV, and I think that's 14 about a couple of dozen, but I've not listed other 15 cases where I have been retained, maybe I read the 16 patent and then the case settled. So I'm guessing 17 if you counted everything maybe 50 times but I'm not 18 sure. 19 Q. And what is your consulting rate for this 20 matter? 21 A. 650 an hour. 22 Q. And that's your standard rate? 23 A. It depends. Sometimes I get recruited 24 through search firms, and since they tag on a fee I 25 reduce my rate a little bit to make it easier for	11 1 I have done extensive work and I have a bunch of 2 patents in that field. 3 And then finally I have multiple patents on 4 flash memory. That's also directly related -- 5 related to this technology. 6 And I would add that I was recently elected 7 a Fellow of the National Academy of Inventors for my 8 patents. 9 Q. And just to clarify, you understand that 10 the patent at issue in this IPR proceeding is US 11 Patent No. 10,868,031? 12 A. Yes. 13 Q. And when I refer to that as the '031 14 patent, you'll understand what I'm referring to? 15 A. Yes. 16 Q. What did you do to prepare for this 17 deposition today? 18 A. I reviewed the exhibits under the folder 19 labeled I think Micron exhibits. So that includes 20 the patent, my declaration, the Kim reference, the 21 Tessariol reference. So these are ones that I 22 reviewed extensively. But in my declaration you'll 23 see on page 13 we have a list of 23 exhibits and I 24 skimmed through all of them. I did not read 25 everything in detail. For example, there are
10 1 the clients. More recently I started charging 675 2 an hour, but in this case it's 650 an hour. 3 Q. In this particular matter does the 650 an 4 hour include any portion that is due to the search 5 firm? 6 A. No. In this case I was recruited directly 7 by Mr. Lang. 8 Q. How many patents do you have? 9 A. Those are listed in my CV. I believe 35. 10 Q. Do any of the patents with your -- bearing 11 your name have -- as an inventor -- strike that. 12 Among the patents that bear your name as an 13 inventor, do any of them relate to the technical 14 area of the '031 patent? 15 A. Many of them do. So I started my career at 16 Texas Instruments where I worked on full megabit 17 DRAMs, dynamic random access memory, using vertical 18 cells. Of course the patent here relates to another 19 type of memory. 20 I've also worked on polysilicon thin film 21 transistors which can be used in SRAMS, S-R-A-M, 22 static random access memory. I think that's 23 relevant to this case also because the 24 semi-conducting channel that these cells use is also 25 made out of polysilicon thin film transistors where	12 1 textbooks. I did not read those in detail. I 2 skimmed through some of those. 3 Q. I entered into the chat box the document 4 that has been already marked as Exhibit 1003 which 5 is the Declaration of Dr. Banerjee in support of the 6 Petition for IPR of the '031 patent. 7 Please let me know when you have that 8 downloaded. 9 A. Yeah, I have it. 10 Q. You recognize this Exhibit 1003 as your 11 declaration in this IPR proceeding? 12 A. Yes. 13 Q. And when you referred to your declaration 14 in your earlier response, this is the declaration 15 that you were referring to? 16 A. That's correct. 17 Q. Other than the documents listed -- strike 18 that. 19 Other than the -- the documents that you 20 mentioned in your prior answer, have you -- did you 21 review any other materials in preparation for this 22 deposition? 23 A. I don't think so, no. 24 Q. And in rendering your opinions in this 25 matter, did you review any other documents than

13 1 those listed in your declaration? 2 A. I don't recall doing so. I don't think 3 so. 4 Q. Can you please turn to the last page of 5 Exhibit 1003, your declaration? 6 A. Okay. 7 Q. That's your signature on the declaration? 8 A. Yes. 9 Q. And you reviewed your declaration before 10 signing it? 11 A. Yes. 12 Q. When you reviewed your declaration prior to 13 signing it, did you find it -- find any 14 inaccuracies? 15 A. Not that I recall. 16 Q. And so the declaration reflects your 17 opinions that you formulated -- formulated in this 18 matter? 19 A. To the best of my knowledge, yes. 20 Q. Is there any information that you requested 21 when preparing your declaration but were not 22 provided? 23 A. No. 24 Q. Did you review the IPR petition in 25 IPR2024-790 while preparing your declaration?	15 1 anticipate the claims of the '031 patent? 2 MR. LANG: Objection to form. 3 THE WITNESS: The summary of my opinions 4 are given in paragraph 39 of my declaration. And as 5 you can see, they're all one of three arguments of 6 the obviousness argument. 7 By MR. BONNY: 8 Q. And you did not render any opinions 9 regarding anticipation in this proceeding? 10 A. No, I don't think so. 11 Q. Several of the -- strike that. 12 One of the claim terms in the challenged 13 claims in this IPR for the '031 patent include the 14 term pillar support structure; is that right? 15 Strike that. Let me re-ask my question 16 because I misspoke. 17 Some of the challenged claims in this 18 proceeding include the term pillar support material; 19 correct? 20 A. Can you point me to a specific claim 21 element? I'm looking through it. 22 Q. Claim -- claim 4 of the '031 patent 23 includes the term pillar support material; 24 correct? 25 A. Yes, I see that now.
14 1 A. You mean the petition filed by Micron? 2 Q. That's right. 3 A. Yes, I did. 4 Q. As part of your analysis in this matter, 5 you analyzed certain claims of the '031 patent; 6 correct? 7 A. Yes. 8 Q. And you're aware of the difference between 9 anticipation and obviousness? 10 A. I'm not a lawyer but I have a layman's 11 understanding. 12 Q. What is your layman's understanding of 13 anticipation? 14 A. In this particular case I did not have any 15 anticipation arguments or obviousness arguments. 16 But as I discussed in the other case that we went 17 over on Wednesday, my layman's understanding is 18 anticipation is covered by I think one of two, where 19 obviousness is discovered by one of three. And 20 basically anticipation depends on a single piece of 21 prior art in terms of meeting the claim elements. 22 But once again, I'm not a lawyer so there may be 23 inaccuracies in that statement. 24 Q. But to clarify, in this particular IPR you 25 did not find that any of the prior art references	16 1 Q. What is your understanding of the term 2 "pillar support material?" 3 A. I'm looking at, for example, paragraph 156 4 of my declaration where we explain that Kim renders 5 this claim element obvious. Basically it means that 6 when you etch the sacrificial layers that we 7 subsequently filled with the word lines, the 8 conductive word lines, the whole structure can 9 mechanically collapse unless you have them supported 10 by these supporting pillars which are etched through 11 the staircase and then you fill them up with some 12 material which provides mechanical structural 13 support, so the staircase pattern which has been 14 etched off in terms of the sacrificial layers 15 doesn't mechanically collapse. 16 Q. How would a person of skill in the art 17 determine whether a material is a pillar support 18 material? 19 MR. LANG: Objection. Form. 20 THE WITNESS: If I look at paragraph 215 of 21 my declaration, we discuss this issue where we say 22 that different materials provide different levels of 23 structural support, and for a POSITA to determine 24 whether it does so or not, you look at the 25 mechanical and lasting properties of the support

17 1 materials as exemplified in terms of what is known 2 as a Bulk modulus and Young's modulus. These terms 3 are terms from the theory of elasticity of materials 4 and they are familiar then from my undergraduate 5 classes as well as in the context of my research. 6 So different materials behave differently. 7 For example, if you have dielectrics, they can be 8 brittle, and when you put stress on them, they hold 9 up to the stress until the so-called yield point at 10 which point they can fracture. On the other hand, 11 if you have metals, they can deform inelastically 12 without fracturing. And what the term inelastically 13 means is metals are so-called malleable and ductile 14 trills. Essentially what happens is you form 15 dislocations in the material but the whole structure 16 doesn't collapse. 17 A very good analogy would be think of 18 reinforced concrete. So the -- the concrete by 19 itself is a brittle material and that's why you 20 reinforce that with rebar, steel rebar. So that is 21 kind of the analog in this context. 22 By MR. BONNY: 23 Q. What is a Bulk modulus? 24 A. So in the theory of elasticity, you have 25 the relationship between what is called stress and	19 1 obviously don't want to reach that point. 2 Q. Does a pillar support material have a high 3 or a low Young's modulus? 4 A. That term is a material-dependent term. So 5 depending on the type of material that you are using 6 to fill up the dummy pillar holes, they have 7 different Young's moduli. And you can look them up, 8 you know, in all kinds of handbooks. 9 Q. What about if the material is a metal, does 10 a pillar support material that's a metal have a low 11 or high Young's modulus? 12 A. Once again, that is a very 13 material-dependent term. Different metals have 14 different Young's moduli. You have soft metals such 15 as aluminum, for example, versus harder metals such 16 as cobalt. So it's all dependent on what material 17 you're looking at. 18 Similarly in terms of insulators, such as 19 silicon dioxide versus silicon nitride, they have 20 different Young's moduli. I mean, I couldn't tell 21 you offhand without looking at textbooks which one 22 is higher or lower. 23 Q. Is that also true for Bulk modulus? 24 A. Yes. 25 Q. So is it accurate then that not all metals
18 1 strain. Stress is the force that you put on the 2 solid material while strain is the deformation of 3 the material. The percentage change of, for 4 example, the lattice constant divided by the 5 original lattice constant. 6 In the case of Bulk modulus, suppose I 7 squeeze it from all three directions with volumetric 8 compression, so the Bulk modulus gives you the 9 proportion at a constant between how much force I'm 10 applying in all four -- all three directions 11 compared to how much the material has been 12 compressed. 13 Q. And what is a Young's modulus? 14 A. A Young's modulus also means a similar 15 thing. It's a proportion at a constant between 16 stress and strain. So I don't recall exactly 17 whether in the case of Young's modulus it's one 18 dimensional stress versus one dimensional strain, 19 but I think that's not important. What is relevant 20 is all these terms are terms from theory of 21 elasticity which tells you how much material will 22 deform or strain in response to how much stress you 23 put on it. And then, as you keep increasing the 24 stress, at some point, what is known as a yield 25 point, things can fracture catastrophically so you	20 1 would qualify as a pillar support material? 2 A. No. That's also very context dependent. 3 So you have to tell me how much mechanical stress 4 you're putting on the structure and if that is below 5 or higher than the yield point of that particular 6 material. So the stress that I'm applying on the 7 structure is higher than the yield point, the 8 structure would collapse and I would say, yeah, that 9 material is not suitable. But on the other hand, if 10 the stress that I'm applying is below the yield 11 point of that material, it's a perfectly good 12 mechanical structure. 13 I'm not saying -- going back to my concrete 14 and rebar analogy where you make a skyscraper and 15 you can put in a lot of steel rods to increase the 16 mechanical strength and the skyscraper wouldn't 17 collapse, but if you put in fewer steel rods or 18 skinnier steel rods to build the skyscraper, the 19 force would exceed the yield point and the whole 20 structure would collapse. 21 Q. Other than Bulk modulus and Young's 22 modulus, are there any other criteria that you would 23 evaluate to determine whether material is a pillar 24 support material? 25 A. Yes.

21 1 Q. What else? 2 A. Well you'd have to look at this alternating 3 set of materials that are used to form the staircase 4 structure. So as deposited there tend to be two 5 different types of insulators, as an example, that 6 could be alternating yields of silicon dioxide and 7 silicon nitride but it could use other combinations 8 also. And then you would etch off one of those two 9 layers, those are the sacrificial layers, which is 10 then going to be subsequently filled with metal -- 11 highly conductive metal to make highly conductive 12 word lines. So I would look at exactly what 13 materials were being used and what the structure 14 properties of the material that's left after you do 15 the etch of the sacrificial metal -- material. 16 And then you also look at the etch process. 17 Again, do these etches of the sacrificial material 18 through what are called dry plasma base etches or 19 wet chemical etches and the forces that you put on 20 the structure are different in the two cases. So I 21 would consider all of those. And a POSITA would 22 know how to look at all of these. 23 And I will tell you what you do is you can 24 do, you know, test measurements and you can do a 25 cross-sectional imaging of the structure using	23 1 which then diffuse through what is called a 2 semi-stagnant boundary layer that forms between the 3 gas ambient and the substrate on which I'm doing the 4 deposition. 5 And then the final stage of the CVD action 6 is often capitalized with a surface of the substrate 7 itself. And all of this is relevant because with 8 CVD you end up getting a conformal deposition. And 9 the term conformal means you have some sort of a 10 mesa structure with maybe a cavity in part of the 11 mesa and I'm trying to fill up the cavity. The CVD 12 process would not only fill up the cavity but go on 13 top of the mesa and the sides of the mesa. That is 14 how CVD works. 15 Q. And is it right that CVD is sometimes used 16 in manufacturing memory devices? 17 A. Used extensively, yes. 18 Q. Can CVD be used for targeted deposition? 19 MR. LANG: Objection to form. 20 THE WITNESS: In some limited cases it can. 21 It's called -- so a subset of CVD is called epitaxy. 22 And what the term epitaxy refers to is not only am I 23 depositing a film, that film has a single crystal 24 structure as opposed to polycrystalline morphosis, 25 and for that you generally need a single crystal
22 1 things like scanning electron microscopy and that 2 will tell you if the structure had collapsed or not. 3 And accordingly you would, you know, tweak your 4 process. 5 Q. To do that analysis you would need to know 6 which specific materials are being considered? 7 A. Yes. Not only for the support materials 8 but also what's being etched and what's being left 9 behind, how it's being etched. And these are all 10 well known for a POSITA. 11 Q. In your declaration you offered some 12 opinions regarding CVD or chemical vapor deposition; 13 is that right? 14 A. Yes. 15 Q. What is CVD? 16 A. Throughout my 40-year career I have worked 17 on CVD as part of my research. It stands for 18 deposition processes for thin films where you flow 19 in different precursors and heat up the chamber 20 where the deposition is being done so that you get 21 some sort of a chemical reaction between the 22 precursors that I'm flowing in in the gas phase but 23 you don't want the reaction to go to completion 24 entirely in the gas phase. You have some 25 intermediate reaction byproducts that are formed	24 1 seed in the substrate to continue the single crystal 2 growth. And sometimes you can do something called 3 selective epitaxial growth which also I worked on. 4 In that case I did the targeted deposition. But the 5 vast majority of -- I mean, that is kind of hard to 6 achieve. You have to tweak things very carefully to 7 do that. But the vast majority of CVD processes are 8 not going to be targeted. But you have to give me 9 more details about the specific process you had in 10 mind. 11 By MR. BONNY: 12 Q. Are you familiar with masks during the CVD 13 process? 14 A. You could use masks, yes. 15 Q. And you can use masks to mask portions of 16 the device so that the CVD process does not deposit 17 material in those regions? 18 A. So once again the answer is context 19 dependent. You have to give me more details to 20 answer that definitively. 21 But, in general, you could use a mask to 22 block off deposition on the substrate in certain 23 regions with certain caveats. CVD processes are 24 generally done at an elevated temperature so the 25 mask that you choose has to be able to withstand

25 1 those deposition temperatures. So, for example, you 2 could not use a photo resist for this masking 3 purpose. And when you do the deposition with a mask 4 in certain regions, you still get deposition on top 5 of the mask, but then subsequently you have to then 6 etch off the mask and lift on the CVD deposition in 7 the mask region. So there are process steps that 8 are involved and everything is context dependent. 9 Q. Are there masks that can simply be lifted 10 off the device after the deposition step as opposed 11 to being etched away? 12 A. I mean you would have to give me -- you 13 would have to give me more specifics of the process 14 for me to answer that definitively. 15 Q. Are you not familiar with using that type 16 of mask for a CVD process? 17 A. I am. But I don't want to give a broad 18 answer that can be taken out of context. And I did 19 not offer any opinions on that in my declaration I 20 don't think. 21 Q. So you are aware that there are some masks 22 that can be used with a CVD process that do not need 23 to be etched away after and can be removed after the 24 deposition process? 25 A. Can you point me to my declaration where I	27 1 By MR. BONNY: 2 Q. When you say you don't want your answer to 3 be taken out of context, what other context are you 4 referring to that would be relevant? 5 MR. LANG: Objection to form. 6 THE WITNESS: That's a very broad question 7 so you will need to give me context to answer that 8 question also. 9 By MR. BONNY: 10 Q. If someone were depositing an insulator 11 using a CVD process and using a mask, the deposition 12 area would depend on the particular mask that's 13 used; correct? 14 MR. LANG: Objection to form. 15 THE WITNESS: If one were to use a mask to 16 do CVD, as I told you a few minutes earlier, the 17 deposition would generally happen in the openings in 18 the mask but then it also generally would deposit on 19 the top of the mask which would then, in general, 20 would have to be etched off lifting off the 21 deposition on top of the mask and leaving it on the 22 substrate only in the openings. But there is so 23 many variables in this that I can't give you a 24 clear-cut answer unless you give me more 25 specifics.
26 1 opine on that? I know I haven't. 2 Q. I'm simply asking about a topic relevant to 3 the context of CVD which you did opine on in your 4 declaration. 5 A. Okay. 6 Q. My question I'm asking is, are you aware 7 that there are some masks that can be used with a 8 CVD process that do not need to be etched away after 9 and can be removed after the deposition process? 10 A. Yes, I am. I can give you a broad answer, 11 but that is subject to caveat so I don't want you to 12 take my answer out of context. So, for example, 13 people sometimes put down metal masks with holes in 14 them and put that in contact with the substrate and 15 then you can do a deposition -- CVD deposition you 16 will only deposit in the holes and then you just 17 lift up the metal -- it's called a shadow mask. 18 I've done that kind of CVD also. But the specifics 19 depend very much on the context so I don't want my 20 answer to be taken out of context. 21 (Court Reporter clarification.) 22 MR. LANG: Yeah, I was. 23 Can you hear me now? 24 THE WITNESS: Yeah. 25 MR. LANG: Okay.	28 1 By MR. BONNY: 2 Q. When depositing an insulator using a CVD 3 process in the -- in the shadow mask, the deposition 4 area on the device would depend on the particular 5 shadow mask that's used; correct? 6 MR. LANG: Objection to form. 7 THE WITNESS: So, once again, you know, you 8 are not giving me enough context for the specifics, 9 but in broad terms the deposition would depend on 10 the details of the shadow mask, such as where the 11 openings are in the mask, but it would also depend 12 on the topography of the underlying substrate which 13 would then determine whether the shadow mask that 14 I'm putting down is in hard physical contact with 15 the substrate or the gaps. 16 So if you go back to the '031 patent, 17 hypothetically, when I have etched this mesa-type 18 structure with the staircases that we formed, and if 19 hypothetically I put down a metal shadow mask to 20 cover the mesa and then I did CVD, you still end up 21 getting CVD deposition around the mesa structure 22 because once the step on the mesa, there is going to 23 be a gap between the shadow mask and the substrate 24 and these molecules during CVD would be able to go 25 through that. So in that context a shadow mask

29 1 would not prevent deposition on the various sides of 2 the mesa. 3 By MR. BONNY: 4 Q. If using a mask that was deposited instead 5 of a shadow mask, that would prevent the deposition 6 in the masked portions of the memory device; 7 correct? 8 MR. LANG: Objection to form. 9 THE WITNESS: There is a lot of 10 hypotheticals in your question, but you can still 11 have a metal shadow mask that's placed on the mesa. 12 If you deposited a hard mask only on the sides to do 13 the deposition in the opening, maybe that would work 14 depending on the context once again, but I would not 15 see why a POSITA would want to do that. I mean, 16 that's contrary to the overall objectives of the 17 process which is to make these 3D NAND memory cells 18 the most simple way, the most cost-efficient way 19 with the highest yield. And what I mean by that -- 20 and, in fact, we have discussed that in my 21 declaration. 22 Let me get there. Just a second. Let me 23 research. I've discussed that issue in different 24 parts of my declaration, but I would like to draw 25 your attention to paragraph 112 as one example where	31 1 depth of focus where you have non-planar 2 topographies. 3 Furthermore, these metal bit lines are very 4 often made up of metal because you want highly 5 conductive bit lines so that you have low RC time 6 constants. So in that context, if one were to try 7 to pattern a hook parallel set of metal bit lines 8 going over a step, when you stop singling, do 9 patterning and etching of that, you can leave behind 10 these so-called metal filaments or stringers, add 11 those notches, and that would be catastrophic 12 because those metal stringers would be 13 short-circuits with the neighboring bit lines. You 14 do not want that. 15 And then finally, although I didn't express 16 it -- discuss that in my declaration, a POSITA would 17 know that when you make these memories, you don't 18 make a single memory chip, you have a whole bunch of 19 them. Maybe, I don't know, depending on the size of 20 the wafer and the size of the memory chip, hundreds 21 of these memories which generally have a rectangular 22 shape right next to each other with gaps in between. 23 So when you do the CVD deposition, you will have a 24 conformal deposition as I was discussing. And when 25 I'm trying to fill up the cavity in the staircase
30 1 we talk about this filling insulation -- insulating 2 layer 110 which is trying to fill up the cavity in 3 the staircase region. But as we discussed, that 4 deposition would be formed on the entire top surface 5 of the substrate and it would also cover the sides 6 of this mesa which is then planarized using 7 techniques such as chemical/mechanical polishing, 8 okay. 9 And as we discussed in 112, that's very 10 important because if you look at the entire 11 structure in the CAR region, for example in Figure 12 10, which is on page 63, that's a cell A region. 13 One, a POSITA would recognize that in this structure 14 you have an area of bit lines which are orthogonal 15 to the plane of the screen while you have an area of 16 word lines which are horizontal and you have a 17 memory cell I think the sections of bit lines and 18 word lines. 19 Now, why is that relevant? That's relevant 20 because when the bit lines go over the mesa, which 21 is in the direction -- in the Dub direction, so 22 closer to me or behind the screen, if you did not 23 have such a planarized surface, you would have 24 problems patterning those bit lines in terms of 25 topography and that is the so-called problem of	32 1 region, it will fill up the surrounding regions. 2 It's hard to describe that. 3 So in this context, if we look at Figure 4 10, the surrounding regions would be the region 5 closer to me or farther away in the depth direction, 6 keeping in mind that, you know, this Figure 10 is 7 just a cross-sectional view of a 3-dimensional 8 structure. And then you planarize the whole thing 9 to address this depth of focus issue and stringer 10 issue. 11 So, you know, a POSITA could decide to mask 12 off the gaps between chips to prevent deposition but 13 he or she would be shooting herself in the foot 14 because then you would end up with a stamp which, 15 you know, would lead to losses, it's additional 16 costs for a process that's going to be damaging to 17 you. So I cannot imagine a POSITA would be so 18 stupid as to try to do that. 19 Q. You understand that one of the prior art 20 references that you opine on in your declaration is 21 US Patent No. 10,381,369, or what you refer to as 22 Kim? 23 A. Yes. 24 Q. The Kim prior art reference does not 25 expressly show the edges of the alternating stack on

33 1 all four sides; is that correct? 2 MR. LANG: Objection to form. 3 THE WITNESS: I respectfully disagree. 4 By MR. BONNY: 5 Q. Which figure shows that? 6 A. If you can pull up Kim for me, I can give 7 you that. I believe it's Figure 1 but I want to be 8 certain. 9 Q. I've shared Exhibit 1001 which was 10 previously marked in this IPR. Please let me know 11 when you have that downloaded. 12 A. You gave me '031. I was asking for Kim. 13 Q. Oh, apologies. One moment. 14 All right. I have now shared what's been 15 previously marked as Exhibit 1005 which is US Patent 16 No. 10,381,369 to Kim. Let me know when you have 17 that downloaded, please. 18 A. Yes, I have it. I would like to draw your 19 attention to Figure 1 as we were discussing. So 20 this is a -- 21 Q. I just want to confirm. Exhibit 1005 that 22 I just shared, do you recognize that as the Kim 23 prior art reference that you opined on? 24 A. Yes. 25 Q. Thank you. Apologies for cutting you off.	35 1 back, on a wafer, which is a circular piece of 2 silicon, you would make -- and depending on the size 3 of the wafer and the size of these memory chips, you 4 know, hundreds of these memory chips which arrange 5 in a very regular fashion on the horizontal plane 6 with gaps between neighboring memory chips. You 7 obviously have to have a gap because after you make 8 the memory chips, you have to scribe them in 9 individual chips which are then packaged and sold. 10 So this narrow boundary that's shown in 11 Figure 1 between the outermost rectangle and the 12 inner rectangles represents a gap and then you do 13 the CVD to fill up these row DCR regions where the 14 staircase would be, you would fill up that narrow 15 boundary and then you would end up planarizing it 16 for the reasons that I mentioned earlier because now 17 when you made the bit lines which go up and down, 18 you want to be able to pattern those bit lines and 19 not have depth of focus issues. You don't want to 20 have stringers. 21 So it is abundantly clear to me that Kim 22 Figure 1 shows, you know, the surrounding regions 23 being covered with this dielectric, in fact, to a 24 greater extent than the '031 patent. That was 25 included in the '031. I believe all of the figures
34 1 Please continue. 2 A. So as I was telling you, I would like to 3 draw your attention to Figure 1 which is a plane 4 view of the memory cell. So in the middle we have 5 this rectangular regions marked CAR. I believe 6 that's cell area region. And then on either side 7 you have these so-called row DCR. I believe that 8 stands for row decoders. 9 So in this case the word lines would go 10 left to right and you would have these, you know, 11 conical memory cells pointing -- so this is a plane 12 view. So the conical memory cells would go into the 13 depths of the screen, if you will. And then at the 14 bottom you see C-o-l D-c-r, I believe that stands 15 for column decoder. In this case the bit lines 16 would go across the CAR region up and down and you 17 would have a whole area of those, okay. 18 And then if you look at the top, you will 19 see a boundary between the rectangles marked by CTR 20 or CAR. So that's the mesa where the memory area is 21 but then there is a -- a boundary, if you 22 will, between that and the outermost rectangle 23 which, you know, in this case shows the area that 24 could be devoted to one of these memory chips. 25 And as I was telling you a few minutes	36 1 in '031 are cross-sectional views. I do not recall 2 seeing a suitable plane view. 3 Going further -- I'm just getting to the 4 other figures of Kim. I could point you to Figure 5 18 of Kim, for example, which is an isometric view 6 of one of the memory chips. This is not a complete 7 view because this is trying to show you a 8 cross-section of the structure. 9 So, once again, as I fill up the cavity 10 with CVD, you would have a conformal deposition on 11 the two sides. You would work very hard not to have 12 deposition on the surrounding sides unless a POSITA 13 did something stupid by masking it off and then 14 shooting himself or herself in the foot. 15 Q. So is Figure 18 relevant to the embodiment 16 of Kim that you opined on in your declaration? 17 MR. LANG: Objection to form. 18 THE WITNESS: Let me look at my declaration 19 and see if -- I just did a search of my declaration, 20 Figure 18. I don't see that so it looks like I 21 didn't specifically refer to that figure. 22 By MR. BONNY: 23 Q. Would a person of skill have looked or 24 considered Figure 18 in understanding how Kim's 25 device is structured?

37 1 MR. LANG: Objection to form. 2 THE WITNESS: I mean, when you read any 3 patent, you read all the specifications, look at all 4 the figures, reach your opinion. And in many cases 5 there are multiple embodiments. I can't recall 6 offhand, you know, if Kim had multiple embodiments 7 and which one I referred to, but in a broad sense, 8 of course you look at everything to come to your 9 opinion. 10 By MR. BONNY: 11 Q. Would a person of skill also consider 12 Figure 24 in understanding the structure of Kim's 13 memory device? 14 MR. LANG: Objection to form. 15 THE WITNESS: Let me do a search of my 16 document -- of my declaration to see if I explicitly 17 referred to 24. 18 I don't see Figure 24 referenced in my 19 declaration so it looks like I did not explicitly 20 refer to it. But, you know, I reached my opinion 21 after reading Kim in its entirety. 22 By MR. BONNY: 23 Q. Is Figure 24 consistent with your 24 understanding of the structure of the memory device 25 that you opined on in your declaration?	39 1 Figure 1 of Kim, that figure does not actually show 2 or label specific materials or components within the 3 CAR region; correct? 4 A. I'm reading through the specifications 5 related to Figure 1 so just give me a second. 6 Yes. So Figure 1 is just a schematic view 7 as they describe in the specs without any details of 8 what the materials, but one would be able to infer 9 the types of materials Kim is talking about by 10 reading the rest of the specs. 11 Q. We've been going for about an hour. Do you 12 want to take a break, Dr. Banerjee? 13 A. Very much so. Thank you. 14 MR. BONNY: Let's go off the record. 15 THE VIDEOGRAPHER: Stand by. We are going 16 off the record. The time is 8:58. 17 (Recess.) 18 THE VIDEOGRAPHER: We are back on the 19 record. The time is 9:10. 20 By MR. BONNY: 21 Q. Dr. Banerjee, what is planarization? 22 A. The term planarization refers to making the 23 tops -- you start with a silicon wafer typically, 24 which is flat to begin with, but then you deposit 25 various kinds of films, you pattern and etch them
38 1 MR. LANG: Objection to form. 2 THE WITNESS: I don't think I analyzed this 3 in great detail in reaching my conclusions. But in 4 a broad sense, yes, I can see the cellular region 5 where the memory cells would be arranged in a 6 regular pattern. And then I see the CTR region, I 7 think Kim calls it the contact region so that is 8 where we would have the staircase. I can see that 9 it's been filled with dielectric -- I don't see the 10 label of the dielectric. And then I can see the 11 trenches, TR1 for example. 12 And I believe that's -- I mean, that is all 13 very common to separate the entire memory area into 14 what are called blocks or sub blocks. I believe 15 that's the reason for etching those strings here, 16 but I have not reviewed Figure 24 in great detail. 17 So all of my answers are subject to, you know, 18 caveats. 19 I mean, if you want me to, I can read that 20 section of Kim but I don't know want to, you know, 21 offer fresh opinions on the spot that have not been 22 discussed in my declaration. 23 By MR. BONNY: 24 Q. I would like to go back to Figure 1 25 actually which you mentioned a moment ago. For	40 1 and all of that, then you introduce topography on 2 the surface. By topography I mean you have hills 3 and valleys. 4 Now, very often people will deposit layers 5 that is then ground down mechanically using 6 something called chemical/mechanical polishing or 7 CMP, so that you have a flat top surface. And the 8 reason you want to do that is to address this depth 9 of focus issues during topography as an example, as 10 we were discussing before the break, and other 11 manufacturing challenges. 12 Q. Does the geometry of a planarized structure 13 in a memory device depend in part on the structure 14 that exists before the deposition? 15 A. Can you repeat that question, please? 16 Q. Does the geometry of a planarized structure 17 in a memory device depend in part on the structure 18 that exists before the deposition of the material 19 being planarized? 20 MR. LANG: Objection to form. 21 THE WITNESS: What exactly do you mean by 22 "the geometry of the planarized device?" 23 By MR. BONNY: 24 Q. So by geometry of the planarized device I'm 25 referring to the overall shape of the structure

41 1 after it's been planarized. 2 Does the geometry of the planarized 3 structure in the memory device depend in part on the 4 structure that exists below it before the deposition 5 of the structure that's planarized? 6 A. So when you form the structures of the 7 memory device through deposition of films and 8 patterning and etching them, you will have once 9 again protrusions and depressions and you may 10 have -- and you will have gaps between neighboring 11 memory chips, for example, as you were discussing 12 earlier, and then you deposit a filling layer where 13 you have an oxide dielectric on the entire wafer and 14 then you grind down everything using this technique 15 called chemical/mechanical polishing. And that will 16 then result in a planar surface over the entire 17 wafer that is then subject to do the next 18 lithographic step, patterning step. So when you do 19 planarization on a -- during processing, you 20 actually planarize not only the hills and valleys of 21 one chip but over the entire wafer. 22 Q. Could you please turn to paragraph 107 of 23 your declaration? 24 A. Okay. 25 Q. And at the end of paragraph 107 do you see	43 1 surface over the entire chip location. 2 Q. Insulating layer 110 has other structures 3 passing through the planarized top surface such as 4 channel structures; is that correct? 5 A. Yes. 6 Q. How is that accomplished during 7 manufacturing? 8 MR. LANG: Objection to form. 9 THE WITNESS: In general, it is 10 accomplished using what is called reactive-ion 11 etching, RIE. Let me see if I used that term 12 specifically. Yes, I did. 13 So, for example -- background. Yes. So in 14 paragraph 59 of my declaration we talk about how 15 etching would be done. It generally is done using a 16 reactive-ion etching which is a dry plasma-based 17 etch where you have an etch component which is an 18 isotropic. I have been doing this kind of research 19 for 40 years. I've been teaching the graduate 20 course about semiconductor fabrication using etching 21 for 40 years so I can, you know, get into great 22 details. 23 But in a broad sense, in reactive-ion 24 etching you have a plasma-based etch which is partly 25 chemical in nature which is selected between
42 1 you have an annotated copy of Figure 4B of Kim? 2 A. Yes. 3 Q. In that Figure 4B from your declaration, 4 insulating layer 110 is shaded in green; correct? 5 A. Give me the soft copy other than the hard. 6 Can you repeat the question, please? 7 Q. In Figure 4B of Kim in your declaration, 8 insulating layer 110 is shaded in green; correct? 9 A. That's correct. 10 Q. And insulating layer 110 has a planarized 11 top surface; is that right? 12 A. Well this is a cross-section view at a 13 specific location on the chip. So you really need 14 the view in the direction normal to the plane of the 15 screen. But as I've told you before, when you do 16 the planarization, you planarize the entire wafer 17 with multiple chip locations and all of that. So 18 based on that a POSITA would know that that would 19 also be planarized in the direction normal to the 20 plane of the screen as it's shown being planarized 21 in the horizontal direction in this particular 22 cross-sectional view. 23 Q. So insulating layer 110 is a -- has a 24 planarized top surface? 25 A. Yes, it should have a planarized top	44 1 different materials but also partly physical in 2 nature which is -- and that's what gives RIE this 3 isotropic etch. And that is generally what you want 4 in etching these conical deep holes in the structure 5 where the memory cells are made. 6 By MR. BONNY: 7 Q. That etching process is performed after the 8 deposition and planarization of insulating layer 9 110? 10 MR. LANG: Objection to form. 11 THE WITNESS: You are referring to Figure 12 4B, I presume, in this case? 13 By MR. BONNY: 14 Q. That's right, yes. 15 So in Figure 4B is the etching process that 16 forms the holds for the channel structures performed 17 after the deposition and planarization of insulating 18 layer 110? 19 A. Well, the channel structures are to the 20 left of the figure in the region marked CAR and that 21 is generally going to be done in this case in two 22 stages because it has a two stack memory structure 23 and that will be done prior to the deposition of 24 layer 110. 25 Q. And a portion of this structure is etched

45 1 after the deposition and planarization of insulating 2 layer 110; correct? 3 MR. LANG: Objection to form. 4 THE WITNESS: Would you repeat that 5 question, please? 6 By MR. BONNY: 7 Q. A portion of this channel structure -- 8 strike that. 9 A portion of the -- the hole for the 10 channel structure is etched after the deposition and 11 planarization of insulating layer 110; correct? 12 MR. LANG: Objection to form. 13 THE WITNESS: So there is different process 14 recipes used by different companies. So in many 15 cases what's done is these channel holes will be 16 filled with a sacrificial layer and then, you know, 17 after you do various etches, you may be etching off 18 the sacrificial layer and then filling it with the 19 storage -- charge storage layer and the 20 semi-conducting channel and all of that. 21 On the other hand, in the region marked 22 CPR, that's where the conductive word lines are 23 going to be formed through this gate replacement 24 process. And for that part of the structure you 25 have these interweaved layers of two different	47 1 MR. LANG: Same objection. 2 THE WITNESS: Depends on what you mean by 3 the final structure for 110. 4 By MR. BONNY: 5 Q. The final geometry of insulating layer 110 6 depends in part on the process -- on process steps 7 that happen after the deposition and planarization 8 of deposition -- insulating layer 110. 9 MR. LANG: Same objection. 10 THE WITNESS: It depends on what you mean 11 by final geometry. So you deposit 110, you 12 planarize it, and then the surface is planar. But 13 then when you etch these dummy holes, you do form 14 this conical cavities in 110. See, if that is what 15 you mean by the final structure, the final 16 geometry, yes. The final structure would depend on 17 process steps such as etched steps done after the 18 deposition of 110. 19 By MR. BONNY: 20 Q. What is a gate last manufacturing 21 process? 22 A. That's a term that's commonly used in the 23 field to make transistors. So the old way of making 24 transistors are MOSFETS, M-O-S-F-E-T-S, for us to 25 form on the channel a gate dielectric, which
46 1 dielectrics, one of which is a sacrificial layer 2 that is going to be etched off and the CVDs have to 3 be then refilled with metal. And during the process 4 you have to have this pillar support structure that 5 we were discussing earlier so that layer 110 would 6 have to be deposited prior to that. 7 By MR. BONNY: 8 Q. Is insulating layer 110 deposited before 9 forming the dummy holes in the right side of Figure 10 4B? 11 MR. LANG: Objection to form. 12 THE WITNESS: Yes. In this case, yes. 13 By MR. BONNY: 14 Q. So the final structure of the insulating 15 layer 110 depends in part on process steps that 16 happen after the deposition and planarization of 17 insulating layer 110? 18 MR. LANG: Objection to form. 19 THE WITNESS: Would you mind repeating the 20 question, please? 21 By MR. BONNY: 22 Q. The final structure of the insulating layer 23 110 depends in part on process steps that happen 24 after the deposition and planarization of insulating 25 layer 110?	48 1 historically would be internally grown oxide but in 2 more recent times it's an ALD, Deposited High-K Gate 3 Dielectric. 4 Then you pattern -- then you deposit a gate 5 electro material, you swap photography and etch to 6 form the gate, and then after you form the gate, you 7 form the sole strains on either side of the gate 8 through typically iron implementation and that is 9 done in multiple steps, in fact the MOSFET -- partly 10 in the MOSFET, for example. I don't want to go into 11 those details unnecessarily. So that is a gate 12 first process where one is using the gate itself as 13 a self-aligned mask to form the DocSourcing regions 14 on either side. And that is very important because 15 you want the gate to straddle the channel region 16 between the source and the drain without too much 17 oil for electrical reasons that, once again, we are 18 not going to get into. 19 With the gate last process, on the other 20 hand, you flip this order of the formation of the 21 gate and the source drains but you want still to 22 have this benefit of self-alignment. So there one 23 forms a so-called dummy gate which is patterned and 24 etched. Using the dummy gate in a self-aligned 25 fraction you form the source and the drain, then you

49 1 etch off the dummy gate and then you fill up that 2 cavity with a gate dielectric and then you refill 3 the thing with a gate material and very often you 4 then do CMP to planarize the structure. So when you 5 fill that, that is called a gate last process. 6 And that has been done here. We are not 7 forcing the planar transistors. These transistors 8 are vertical in the channel. So you form the 9 channel involving the charge storage layers, the 10 semiconductor channel and all that, then you etch 11 off the sacrificial layers in the staircase 12 structure forming cavities, and then you can very 13 often coat the cavity first with a high-K dielectric 14 in a conformal fashion. Then you fill up the rest 15 of the cavity with a metal such as one which can be 16 deposited by CVD. But, once again, the details 17 depend on who is making the product but -- but in 18 broad terms, that's what a gate last process is. 19 Q. When you say that has been done here, do 20 you mean that Kim uses a gate last manufacturing 21 process? 22 MR. LANG: Objection to form. 23 THE WITNESS: I don't know if Kim used the 24 term gate last. I can do a search. 25 A quick search under gate last are	51 1 a gate last process? 2 A. Yes. 3 MR. LANG: Objection to form. 4 THE WITNESS: And, in fact, that's very 5 commonly used for NAND manufacturing these days 6 because that's how you get low RC time constants of 7 your word lines. 8 By MR. BONNY: 9 Q. I think we may have talked over each other. 10 You said that, yes, Kim's device does use a gate 11 last process? 12 MR. LANG: Objection to form. 13 THE WITNESS: Yeah, I believe so based on 14 the specifications. He may not have used the 15 specific term gate last. 16 By MR. BONNY: 17 Q. What are the benefits of using a gate last 18 process? 19 A. So there was a second part of my answer. 20 So in the earlier versions of 3D NAND flash, one 21 would put down interleaved layers of a dielectric 22 with a highly doped polysilicon gate where the 23 polysilicon layers would act as your word lines and 24 there you would not have a gate last process. That 25 is your gate first process as we were discussing a
50 1 sometimes also called a replacement gate. 2 Apparently Kim doesn't use those terms. But let me 3 quickly skim through the specifications. I'm pretty 4 sure Kim does, but let me confirm that. 5 If you look at column 10 of Kim, between 6 lines 8 to 10, he is referring to Figures 3 and 7 6, insulating layers. And then it's talking about 8 the sacrificial layers HL1. So these are the terms 9 sacrificial layer would tell a POSITA that they are 10 talking about that gate last process. Let me go to 11 Figure 3 just to confirm that. 12 I guess Figure 6 is a better figure which 13 shows a cross-sectional view and they have two 14 interlinked types of dielectrics and that is 15 important because when you do these etches, you want 16 to do selective etches which would etch one material 17 much faster than the other and that's how you form 18 these cavities leaving the other insulating layer in 19 place which is going to be held up mechanically 20 through these pillar structures and then you fill up 21 those cavities with the replacement gate or the gate 22 last process. 23 By MR. BONNY: 24 Q. So based on the description of Kim's device 25 in the specification, it's clear to you that it uses	52 1 few minutes earlier. 2 The problem with that approach was, 3 although it's simpler in the sense that you don't 4 have to etch off a layer and then refill it 5 subsequently, the problem is even highly doped 6 polycrystalline silicon has a higher resistivity 7 than metal, and as a result, these word lines would 8 have a larger resistance and that, in turn, leads to 9 a higher RC time constant. And what the term means 10 is when I put electrical pulses during the read 11 operation, for example, those pulses would have to 12 travel down these word lines, kind of like 13 transmission lines, and they would be somewhat slow. 14 On the other hand, if you use the gate last 15 process where you etch off a sacrificial layer and 16 you refill that with a metal, that is going to have 17 a lower resistivity than highly doped polysilicon. 18 And by doing so in a gate last process, if you 19 reduce R, you reduce the RC time constants, and then 20 when you try to read the memory cells, the signals 21 would populate faster than the word line and you 22 would get a faster memory. That's why it's 23 preferred. 24 Q. How does the particular manufacturing 25 process, whether gate first or gate last, affect the

53 1 electrical properties of the final device? I'm just 2 not following that piece of it. 3 A. Okay. I don't think I have explicitly 4 opined on that in my declaration but I can tell you 5 from my general knowledge. 6 So in a gate first process, very often that 7 would be done with highly doped polycrystalline 8 silicon. So this is silicon which has single 9 crystal grains which are intersected with each 10 other. And when I'm doing the CVD deposition of the 11 this polycrystalline silicon, you could add an 12 n-type dopant using so phosphorus or arsenic, those 13 are the two most common n-type dopants. You are 14 making a so-called M-plus polysilicon gate or word 15 line. That is the gate first process. 16 The process of the gate last process, you 17 have this interleaved layers of two different 18 dielectrics, one of which is a sacrificial layer 19 where, after you deposited the interleaved 20 dielectric stack, you form these dummy pillars and 21 you put -- put this filler material so that the 22 interleaved stack would not collapse when you etch 23 off one of the sacrificial layers and then you 24 refill that with a metal. And the very common metal 25 that is used in this context is Tungsten which can	55 1 the bottom of 24 where that staircase extends in the 2 D1 direction? 3 A. Yes. 4 Q. You see there is no kind of space between 5 the staircase and the D1 direction and then going 6 below that to the substrate? 7 A. Yes. 8 Q. Now if you can turn to Figure 22. 9 A. Yes. 10 Q. You see that there is some space in the D1 11 direction? 12 MR. BONNY: Objection to form. 13 THE WITNESS: Yes, I see that. 14 By MR. LANG: 15 Q. And if you could go to Figure 18. 16 A. Yes. 17 Q. Do you see any space between the staircase 18 and the substrate in the D1 direction? 19 A. Yes, I do. 20 MR. LANG: No further questions. 21 MR. BONNY: Okay. If the videographer 22 could end the deposition. 23 THE VIDEOGRAPHER: Okay. This concludes 24 the deposition of Dr. Sanjay Banerjee. The time is 25 9:36.
54 1 be deposited very often with chemical deposition 2 using WF 6 constant hexafluoride. I'm giving you 3 specific examples. Different companies may use 4 different processes. 5 Q. Are there any other benefits to a gate last 6 process that you're aware of? 7 A. Yes. A company would make more money 8 because if a company has a product that operates 9 faster, it would sell more of those and to me that 10 is a goal of companies. 11 MR. BONNY: I have no further questions. 12 MR. LANG: Yeah, just one -- couple quick 13 questions. 14 EXAMINATION 15 By MR. LANG: 16 Q. Dr. Banerjee, can you pull up the Kim 17 reference again? 18 A. Yes. 19 Q. And go to Figure 24 or -- yeah, 24. 20 A. Okay. 21 Q. Now, you were asked if this had -- if you 22 considered this, and I believe you testified that 23 you considered the entire Kim reference? 24 A. Yes. 25 Q. Okay. Now, if you look at the -- kind of	56 1 (Proceedings concluded.) 2 ---o0o--- 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25

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CERTIFICATE OF STENOGRAPHIC REPORTER

I, BURGUNDY B. RYAN, a Certified Shorthand
Reporter, hereby certify that the witness in the
foregoing deposition,

SANJAY KUMAR BANERJEE, Ph.D.,
was by me duly sworn to tell the truth, the whole
truth, and nothing but the truth, in the
within-entitled cause; that said deposition was
taken at the time and place therein named; that the
testimony of said witness was stenographically
reported by me, a disinterested person, and was
thereafter transcribed into typewriting.

I further certify that I am not of counsel
or attorney for either or any of the parties to said
deposition, nor in any way interested in the outcome
of the cause named in said caption.

DATED: Thursday, January 2, 2025.


Burgundy B. Ryan, CSR No. 11373, RPR

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9:14, 19:9,	46:24, 47:7,	2:16	33:13, 33:25
24:9, 26:2,	47:17, 48:6,	aluminum	apparently
30:1, 39:9,	53:19	19:15	50:2
39:11, 43:14,	again	ambient	appeal
43:20, 50:7,	7:3, 14:22,	23:3	1:3, 5:16
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