

General review of issues and perspectives for advanced copper interconnections using air gap as ultra-low K material

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Abstract

The present paper deals with the different techniques investigated in the whole microelectronics community to integrate air cavities, usually known as air gaps, in-between copper lines for advanced interconnects. The different integration processes were split into two categories, i.e. (i) using a non-conformal CVD deposition inside patterned trenches and (ii) by removing a sacrificial material using a specific technological operation. Advantages and drawbacks of the different approaches will be discussed, including integration issues, manufacturability, and electrical performances. The aim of the paper is to sensitize the BEOL community on these specific approaches that now appear attractive considering the electrical performances required for 45 nm and below technological nodes.

Introduction

Due to the constant shrink of the critical dimensions in ULSI circuits in order to meet integration requirements, delay and crosstalk related to the interconnection part of the circuit become limiting factors for speed and logical performance. After integrating copper to reduce line resistance, it is necessary to isolate metal lines by ultra-low K (ULK) dielectrics currently characterized by low densities due to high proportion of randomly distributed nanopores. This approach is very expensive as it clearly requires new material development and integration at each technology node [1]. Moreover, the multilevel integration of ULK materials in ULSI CMOS circuits leads to several challenges at the process level (such as etch, strip, and chemical mechanical polishing (CMP)), in addition to integration reliability (e.g. leakage current, mechanical stability during multi-level interconnect fabrication and packaging, and thermal behavior). Furthermore, the presence of barriers and cap layers, that leads to increase the effective permittivity of the final dielectric stack, would be a limiting factor. Considering the ITRS roadmap for an effective constant dielectric lower than 2.5, the bulk ULK's dielectric constant

would be equal to 2 [2]. Although it is suggested in the roadmap that air-gap should be integrated when standard approach with ULK materials will not be workable, it could also be considered for an alternative approach to the development of new ULK dielectrics, allowing an unique technology for several CMOS nodes. Very low effective k values and consequently excellent propagation times and very low crosstalk levels obtained with air gaps have been already shown in literature [3-8].

The aim of this presentation is to give a global overview of the present efforts on air-gap integration. To simplify, we classified the different approaches into two main categories, i.e. (i) by taking advantage of the non-conformity of a CVD dielectric layer to create air cavities located inside trenches patterned between lines of a metallic level and (ii) by removing a sacrificial material during a specific technological operation for the construction of one or more metal levels.

Air gaps formation using non-conformal CVD

This approach, to our knowledge, is the most advanced solution in terms of integration and electrical results. Indeed, it has been first widely investigated for Al metallization combined with conventional dielectric material such as CVD deposited USG as this technique requires that trenches are initially formed between the metal lines before dielectric deposition [3-5]. However, since Cu interconnects integration led to new integration schemes including dual-damascene processes, an additional lithography/etching step to pattern the trenches [6-7,9] was required as illustrated in Fig. 1. Moreover, the trenches must be controlled in width and height so that the aspect ratio, defined as the ratio between the height and the width of the trenches, is above 1 as required for well-shaped cavities creation [3-5]. This is a key point to achieve air gaps integration as the shape of the air cavities (i.e. closure-point height, width, volume of the cavity) must be well controlled for any feature size so that any breakthrough into air gaps, potentially followed by some

metal intrusion, is avoided either during upper metal level etching or because of line/via-misalignment.



Figure 1: Standard technological sequence used to incorporate air gaps in a specific metal level, hereafter using non-conformal CVD technique. (i) Once the complete realization of a interconnect stack achieved, (ii) a specific lithography step is introduced to define air gap trenches in-between copper lines. (iii) Then a dielectric liner and a dielectric IMD are successfully deposited to create air cavities. (iv) After that, the interconnect stack is completed using a standard dual-damascene architecture (after [9]).

The main drawback of this technique for Cu interconnects is that an additional dedicated air gap lithography is necessary for each metal level. Moreover, air gaps must be introduced inside the narrowest spaces where the best electrical performances are required, thus making each air gap mask very expensive. However, simple mathematical solution can be used to design the additional mask deduced from metal level and to precisely define the areas where air cavities are required (i.e. dense areas).

This integration scheme should allow a sufficient mechanical stability of the interconnect module including air gap. Furthermore, temperature increase expected with those low thermal conduction materials is easily reduced using this technique [5].

Arnal et al. [6-7] investigated the formation and the optimization of SiO₂ air-gaps using Silane (SiH₄) and TEOS based precursors, and measured an effective dielectric constant to less than 1.7 despite some USG was let on the sidewall of the trenches before non-conformal CVD step. However, to address previously described integration difficulties, a sequential SiH₄/TEOS deposition process, based on step coverage properties of both precursors, was suggested. Combined with a SiN liner (K=7), reliability and electrical performance improvement were achieved: for instance especially for via-misalignment and leakage current. At the same time, no electromigration degradation was observed.

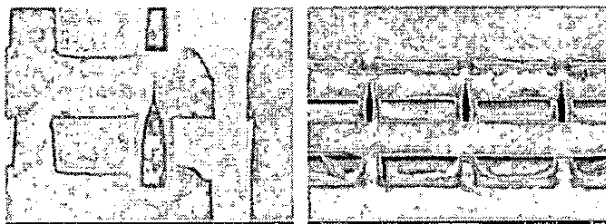


Figure 2: Examples of Cu interconnect modules integrating SiO₂ (left) and SiOC (right, after [8]) air gaps using non-conformal deposition technique.

More recently [9], the feasibility of air gaps built in bulk SiOC (K=2.9) using a dual damascene technique in association with SiC liner was demonstrated. In this case, to achieve all integration requirements and precisely control air gap morphology, the trench width was set on the air gap mask whatever the metal space. Hence, taking advantage of a constant aspect ratio, the air gap morphology was shown to

only depend on the step coverage properties of the CVD process, thus facilitating the integration of the SiOC air gaps.

To overcome cost issue of this approach, i.e. using an additional lithographic step at each metal level, blanket dielectric etch back technique (i.e. direct etching of trenches without Cu lines protection) is currently investigated as an alternative. Despite etching development is required, promising results showed a negligible degradation of Cu line resistance when trenches were directly etched inside USG. Nevertheless, introducing a self-aligned barrier on copper, such as CoWP deposited using an electroless process [10] could even prevent this effect. Furthermore, one could take advantage of a "mushroom" type shape of the metal layer to overcome via-misalignment issue: the as-formed capping being wider than the metal line, some dielectric remains on the sidewalls of the trenches after etching (Fig. 3) acting as a potential via landing pad. Besides, to limit trenches aspect ratio dispersion, metal tiles must be introduced for large metal spaces, preventing an additional dielectric CMP process, and thus imitating a design solution already introduced in interconnect modules to achieve more uniform thickness after metal CMP.

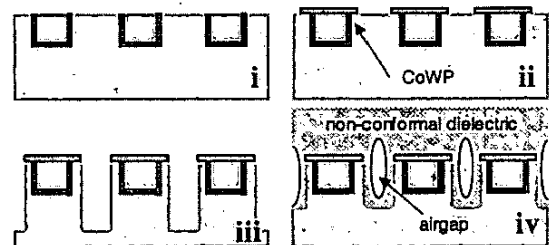


Figure 3: Schematic representation of air gaps formation using non-conformal CVD technique. (i) Once the realization of a metal level is completed, (ii) a self-aligned in CoWP is deposited on the copper that (iii) further protect the copper lines during direct etching of trenches. (iv) Then, air gaps are fabricated using a non-conformal CVD process. As the capping layer is wider than the metal line, this approach can overcome via-misalignment issues (Source: Motorola, Austin).

Air gaps formation using a sacrificial material

In this second approach, for the construction of one or more metal levels, a sacrificial material (SaM) is placed in-between the copper lines where air cavities are further required. In most cases, depending on the complexity of the technique, the interconnect stack consists of the superposition of this SaM as IMD and of a permanent material (PeM) at via level (or Intra-Level Dielectric, ILD). In a second step, once Cu lines have been formed and interconnect stack completed, the sacrificial material is removed during a specific technological operation (thermal or reactive plasma treatments, wet etching...). Whereas many different techniques were available in the literature (see for instance ref. 11) we took the arbitrary choice to focus this section on the different techniques investigated inside STMicroelectronics, Philips and Motorola, with only few references to some outside examples.

Anand et al. [12] presented a gas-dielectric interconnect process referred to as NURA, incorporated as both IMD and ILD. In this approach, a carbon-based layer is removed after

that an oxygen gas has diffused through a SiO₂ bridge layer and reacted with carbon under the bridge to form air gaps. The weakness of this approach is the lack of mechanical strength, as pointed out by Chen et al. [13], that suggested a modified version where some USG is let below the metal lines without completely addressing integration issues such as the incidence of a 450°C annealing in O₂ on metal and other material properties as pointed out by Kohl et al. [8]. However, this approach highlights some important points; for instance, it is suggested to remove the carbon-based SaM after a single O₂ exposure, i.e. once the stack is fully completed, thus achieving a good mechanical strength during specific integration steps such as metal CMP. Moreover, a permanent dielectric film can remain as ILD as the best electrical performances due to air gaps introduction are expected to occur at IMD level.

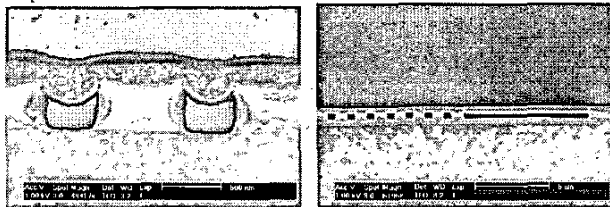


Figure 4: Air gaps obtained after a sacrificial polymer initially deposited in-between the Cu lines were removed during a thermal annealing in N₂ and residues out-diffused through (left) a SiLK layer and (right) a PhiLK layer (Source: Philips Research, Leuven).

Polymers as sacrificial materials have also been proposed using a porous overcoat as ILD [14]. This idea was investigated by Kohl et al. [8] who investigated the electrical performances of air gaps completed combining a polymer as IMD and SiO₂ as ILD. The temperature during the entire damascene integration process was kept no higher than 200°C, air gaps being created during the final N₂ thermal treatment at 425°C for 2 h. Despite promising electrical performances were obtained such as an effective dielectric constant of 2.17, the drawback of this approach is naturally the difficulty to implement a complete integration at 200°C. In parallel, investigations were carried out at Philips Research using SiLK as PeM that according to Kohl et al. [8] should decrease the effective dielectric constant below 2 with the same architecture.

This approach faces integration challenges such as the mechanical stability of the IMD after air gaps formation (some polymer liner collapse were observed for large inter line spaces, possibly due to the low modulus of SiLK) even if some improvements were obtained after SiLK was replaced by PhiLK, thus allowing wider air gaps to be obtained (see Fig. 4). Moreover, as the cure/heat treatment of the PeM occurs at 400°C, i.e. far above the decomposition limit of the SaM as previously discussed, the sacrificial material is removed at each metal level making viamisalignment issue a weakness point of the technique, unless a design solution is set or new sacrificial materials, with higher decomposition temperature, are developed.

Another solution is being investigated at Crolles2 Alliance and consists in successively depositing SiLK as

PeM and USG as a sacrificial layer. Since both materials are well-known and already integrated in Cu interconnects, no important process development was required to build the complete stack. In this approach, once the final multilevel interconnect module is completed, the sacrificial embedded USG layers are successively attacked and decomposed using a diluted HF solution that diffuses through the SiLK membranes on several levels. Moreover, one only cheap air gap mask with large open areas can be added to precisely control HF diffusion inside the multilevel interconnections and localize air gaps inside the dice, thus improving mechanical reliability during packaging of the interconnect module. Furthermore, as for most of the techniques using sacrificial material, integration of a self-aligned diffusion barrier on copper is required. Indeed, this is the only technique that makes easy the diffusion from the annealing ambient or liquid phase of the etchant as well as the out-diffusion of the reaction products.

Finally, we can underline that most of the specific steps and integration skills that are currently investigated for air gaps can be also considered for standard Cu integration schemes using porogen materials which porosity is stabilized only after the complete integration.

Conclusion

This review clearly evidences the multiple effort already done to achieve workable air gap solutions. For the remaining generations, the main features of these air gaps approaches, i.e. sacrificial material removal after partial or total integration, and dedicated architectures for reaction products diffusion, are more and more widely investigated.

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