

Extremely Low Keff (~ 1.9) Cu Interconnects with Air Gap Formed Using SiOC

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Abstract

Dual damascene Cu interconnects with Keff below 2.0 have been demonstrated for the first time. Air gaps between Cu lines were formed with a low K SiOC film in a carefully designed manner. CoWP cap layers were introduced to protect the Cu lines and to eliminate a dielectric liner layer. In addition, AGE (Air Gap Exclusion) was applied to solve crucial problems related to the air gaps. Keff of 1.9 was obtained at 65nm design rule, which surpassed by far ITRS target (2.5~2.8) for hp45. It was also confirmed that leakage current between lines was suppressed by the formation of the air gaps.

Introduction

With the shrinkage of devices, RC delay of interconnects becomes larger. So, the reduction of Keff has been strongly required.

To reduce Keff, the introduction of ELK materials has been investigated [1,2]. But the reduction of Keff below 2.4 is very difficult due to a series of integration issues.

On the other hand, the formation of air gaps between Cu lines is considered to be an alternative approach [3-5]. This approach had been at a standstill because it had crucial problems as follows.

- 1) Contact of vias and air gaps by misalignment
- 2) Degradation of planarity at large spaces

However, we have shown that these two problems can be solved by forming air gaps selectively, which accelerated to put this way in practical use [6].

In this paper, a new technology to realize Keff below 2.0 is proposed. Dual damascene Cu interconnects were successfully integrated with air gaps at 65nm design rule. Extremely low Keff of 1.9 was obtained. Its structure and other electrical characteristics are also reported.

Process Flow

Fig. 1 shows the process flow for this technology. At first, a SiOC film and a TEOS film are deposited as an ILD and an IMD. Next, Cu lines with Ta/TaN barrier layers are formed, and CoWP cap layers are selectively deposited on the Cu lines, as shown in Fig.1(a).

Then, a liner layer including a SiC based film is deposited on the TEOS film and the CoWP cap layers, and resist patterns are formed on the liner layer. The resist patterns are used to exclude air gaps from undesired regions such as wide spaces and peripheries of vias. This concept has been known as AGE (Air Gap Exclusion) [6].

After forming the resist patterns, the liner layer, the TEOS film and the SiOC film are partially etched to form gaps between the Cu lines. Hereafter, this step is referred as "gap etching".

Next, as shown in Fig. 5(d), a SiOC film is deposited and air gaps are formed between the Cu lines. The SiOC film is planarized by CMP. Finally, Cu interconnects having vias and lines are formed, as shown in Fig. 1(e).

In this technology, the CoWP cap layers act as hard masks in the gap etching and metal liners in the final structure. Thus, the damage to the Cu lines during the gap etching can be minimized, and a dielectric liner on the Cu lines can be eliminated to assure the advantage of the air gaps.

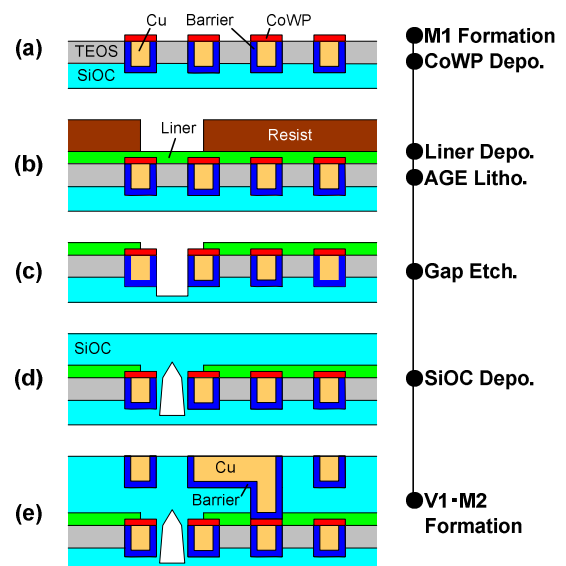


Fig. 1 Process sequence for this technology

Experimental

In order to prove the efficiency of this technology, M1-V1-M2 dual damascene Cu interconnects were fabricated at 65nm design rule with three processes shown in Fig.2.

Process	CoWP	Air Gap
A	NO	NO
B	YES	NO
C	YES	YES

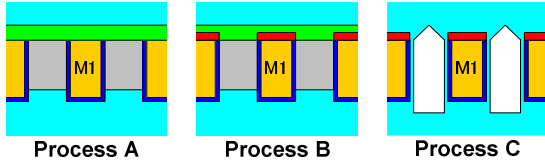


Fig. 2 Three processes tried in this work

Steps to form the air gaps were carefully examined and optimized. A SiOC film with K of 3.0 was used to form the air gaps.

Physical analyses such as SEM and TEM were carried out during and after the processes. The electrical characteristics were evaluated focusing on M1 and V1. Electromagnetic simulations were performed to calculate capacitance between lines.

Results and Discussion

1. Structural Analyses and Process Optimization

As a first step of the process optimization, the coverage of the SiOC film was evaluated. In this evaluation, trenches formed in dielectric films were used. Fig. 3 shows the cross-sectional SEM photograph of the SiOC film deposited on the trenches. It was revealed that the SiOC film used in this work has high bottom-coverage but low side-coverage. In order to make best use of this profile, the gap etching was tuned.

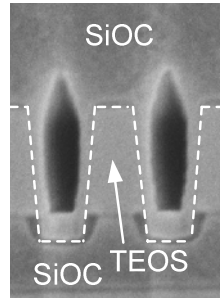


Fig. 3 Coverage of SiOC film

Fig. 4 shows the cross-sectional TEM photograph of Cu lines with an air gap. It is clear that the Cu lines were separated by the air gap with sufficient height. Moreover, the dielectric film on the sidewall of the Cu lines was so thin that the volume of the air gap was very large. The CoWP cap layers were left after the gap etching and there was no significant damage to the barrier layers. These results were obtained by the gap etching with carefully designed strategy.

As mentioned previously, AGE was fully applied in this technology. To check the effect of AGE, surface SEM observations of via chains were carried out after the gap etching. Fig. 5 shows an example of the results. Gaps can be seen at narrow spaces, but there were no gaps at wide spaces and the periphery of a via, showing that AGE worked well just as intended.

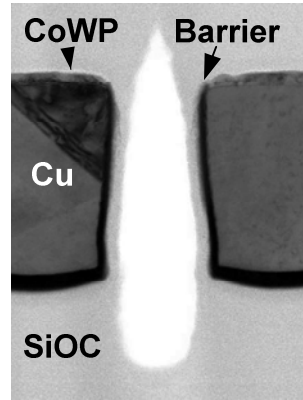


Fig. 4 Cu lines with Air Gap

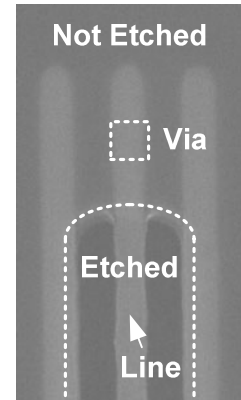


Fig. 5 Effect of AGE

2. Capacitance

Capacitance between lines is shown in Fig. 6 comparing process A and C. Fig. 6 includes observed values and values calculated from the simulations. Observed values in process C with the air gaps were significantly lower than those in process A without the air gaps. The variation of observed values was small especially in process C. The agreement between the observed values and the calculated values was fairly good. Extremely low Keff of 1.9 was obtained in process C.

Distributions of electric field strength are illustrated in Fig. 7. In process A, high electric field appeared around the area between Cu lines. However, an air gap with sufficient height covered entirely the high electric field region in process C. This is the reason why capacitance was drastically reduced in process C.

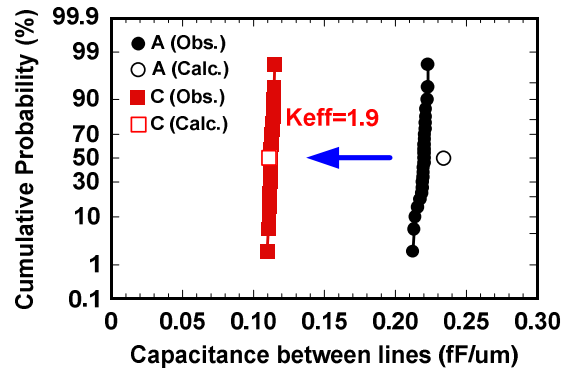


Fig. 6 Capacitance between lines in process A and C

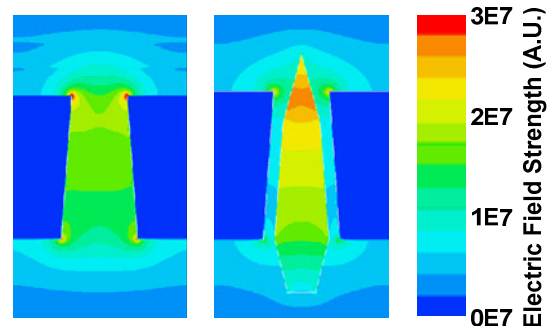


Fig. 7 Distributions of electric field strength in process A and C

3. Leakage Current

Fig. 8 compares leakage current between lines in the three processes. Process B with the CoWP cap layers gave higher leakage current than process A without the CoWP cap layers. On the other hand, process C with the CoWP cap layers and the air gaps gave lower leakage current than process A and B.

This phenomenon can be understood as follows. In process B, leakage paths were formed by the CoWP deposition between the Cu lines, as shown in Fig. 9(a) [7,8]. However, the leakage paths were removed by the gap etching in process C, as shown in Fig. 9(b). Furthermore, the interfaces between the liner layer and the TEOS film were replaced by the air gaps, as shown in Fig. 2. As a result, leakage current in process C became lower than that in process A and B.

Fig. 10 shows short defect density in the three processes. Defect density was very high in process B but it was significantly improved in process C. This trend can be also explained from the removal of the leakage paths by the gap etching.

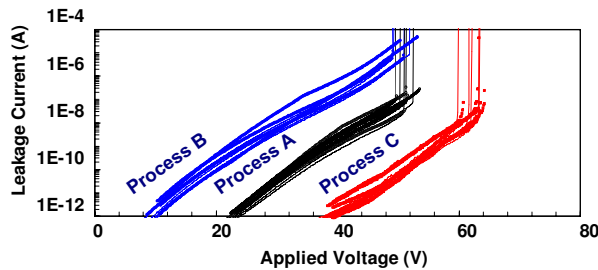


Fig. 8 Leakage current between lines in three processes

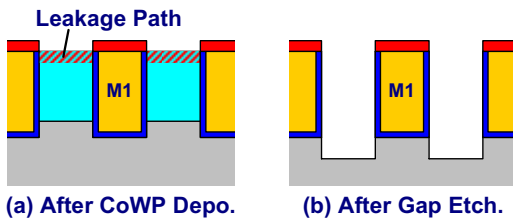


Fig. 9 Removal of leakage paths by gap etching

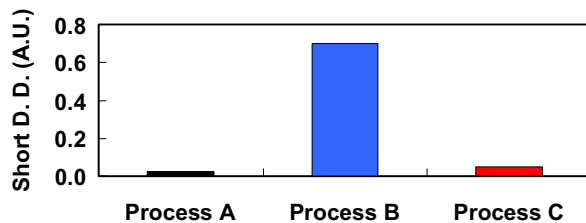


Fig. 10 Short defect density in three processes

4. Line and Via Resistance

Line resistance is plotted in Fig. 11 comparing the three processes. Process C gave the same resistance as that obtained from process A and B. This result indicates that the CoWP cap layers left after the gap etching had adequate barrier property, so that the interaction between the Cu lines and the SiOC film did not happen.

Fig.12 shows via chain resistance as a function of M1-V1 misalignment in process C. No degradation of yield could be found accompanied with the increase of M1-V1 misalignment. This result is quite reasonable because the contact of the vias and the air gaps could not happen due to AGE, as shown Fig. 5 [6,9].

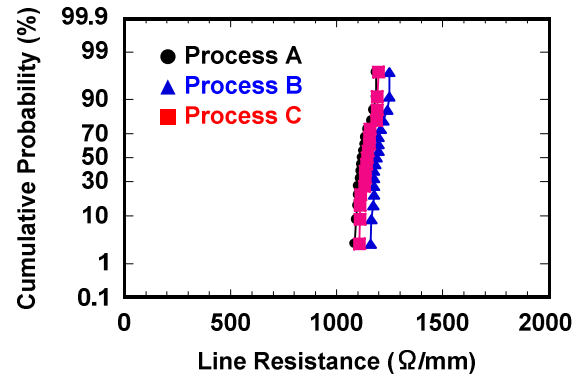


Fig. 11 Line resistance in three processes

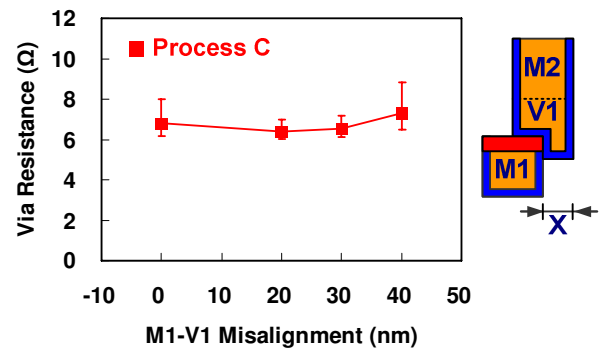


Fig. 12 Via resistance as function of M1-V1 misalignment in process C

Conclusion

A new technology to fabricate extremely low Keff dual damascene Cu interconnects has been established. The reduction of Keff was realized by forming air gaps with a low K SiOC film. CoWP cap layers were used to minimize the damage to the Cu lines and to eliminate a dielectric liner layer. Leakage current and defect density were reduced by integrating the CoWP cap layers and the air gaps. Keff of 1.9 was for the first time obtained successfully at 65nm design rule without the degradation of other electrical characteristics.

References

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