

Performance and reliability of airgaps for advanced BEOL Interconnects

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Abstract

In this paper we present new modeling and measured data to address detailed performance and reliability considerations of multi-level airgaps. Using finite element modeling, we analyzed the capacitance distributions in the airgaps while restricting openings in the cap layers for increased mechanical and electrical reliability. Despite this restriction, capacitance reductions can be maximized by expanding the gap in the low-k SiCOH dielectric underneath the cap, and by increasing gap depth. Relevant BEOL simulation, performance and reliability data has been obtained and will be presented in this context

Introduction

Airgap based interconnects have the potential to demonstrate k_{eff} values at or below 2.0. However, fabricating reliable and manufacturable airgap containing interconnects is far from trivial, especially as interconnect dimensions enter the nanoscale realm. Recently, we reported a potentially reliable and manufacturable airgap based wiring which was demonstrated on a 65nm production microprocessor (1). We achieved this using two techniques employing supra- and sub-lithographic templates, the latter of which uses a novel self-assembly approach.

In this publication, we will examine some of the performance and reliability trade-offs for the two airgap structures that were discussed by us in our previous publication (1). The goal is to design a high performance airgap structure without sacrificing any mechanical reliability.

Figure 1 shows the airgap made using the self assembly based integration scheme described in our previous publication (1). In this structure, the cap has 20 – 40 nm perforations in it and the cap itself stretches over the width and length of the underlying airgap. The Silicon Carbide based (SiCN) cap is compressively stressed and it is well known that as the gap width increases, the deflections which can drive cap buckling will increase (2). We will discuss the trade-offs associated with sustaining a large capacitance drop while at the same time ensuring that the structure remains mechanically stable.

Figure 2 shows the airgap made using the lithographic “optical” scheme described in our previous publication (1). In this approach, there are horizontal slots running through the cap material. These slots run the length of the gap. The gap itself is pinched off in the next level dielectric film. The performance and mechanical reliability challenges associated with this structure will also be discussed.

Results and Discussion

For the self-assembly airgap shown in figure 1, finite element simulations were carried out to calculate the capacitance of a given airgap structure as well as to assess the extent of cap buckling as a function of airgap width. In order

to account for the impact on the dielectric constant of the cap due to the gap formation induced perforations in it, standard correlations such as the Maxwell-Garnett approximation and

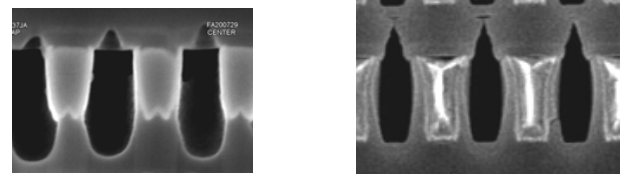


Fig. 1a: Self-Assembly Airgap Fig. 1b: Lithographic Airgap

the Bruggemann effective medium approximation (3) were used. These are analytical approximations that can be used to calculate an effective value for a macroscopic property such as the dielectric constant or the refractive index of a composite medium. For the SiCN cap with 33% void volume and an intrinsic dielectric constant (k) of 5.3, the Maxwell-Garnett and the Bruggemann approximations yield an effective k of 3.56 and 3.44 respectively. For all the capacitance simulations performed for the self-assembly based airgaps, we used a k value of 3.5.

Since the pore sizes of the block copolymer material are roughly 20 – 40nm (1), we observed that the pinch-off occurs very close to the top of the cap layer and that the height of the pinch-off point does not affect the capacitance in a substantial way. However, since this scheme uses a second cap deposition on top of the perforated SiCN film, it is necessary to account for the effect on the capacitance of the structure due to the re-deposited SiCN film on the sidewall. Thus, for a given block copolymer material, the only variables that affect the capacitance of the structure are the depth of the airgap and any potential re-deposition of the SiCN cap during the second cap dep. Figures 3a and 3b show the effect of re-deposited SiCN and increasing gap depth respectively. As can be seen from figures 3a and 3b, the overall capacitance drop for a gap which is nominally as deep as the trenches is about 35% and the effect of SiCN on the sidewall could result in a ~9% increase in total capacitance. Interestingly, while the capacitance does decrease with increasing gap depth, the gains seem to taper off beyond a certain depth.

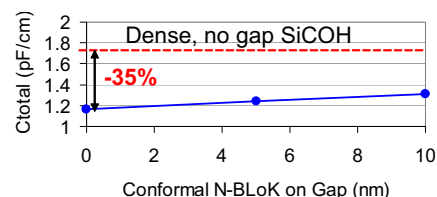


Fig. 3a: Effect of SiCN redeposition on gap Ctotal

As can be seen in figure 4, the measured capacitances on patterned multi-level hardware show that the reduction when compared to dense CVD SiCOH material is on the order of 33% which agrees well with the simulations.

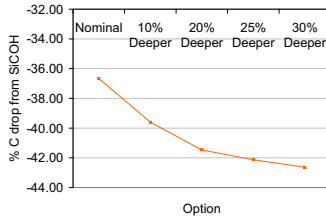


Fig. 3b: Effect of gap depth on Capacitance drop from SiCOH

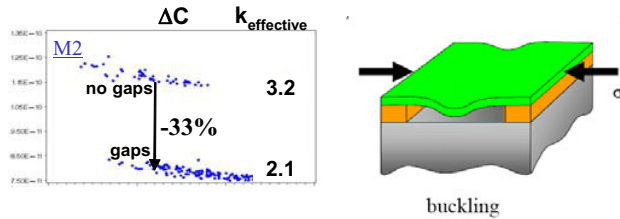


Fig. 4: Measured C drop from SiCOH Fig 5: Cap buckling

Figure 5 shows that the deflection of the compressively stressed SiCN cap increases as the gap width increases. Figure 6 shows that beyond a certain gap width the critical stress passes a threshold for buckling. Thus it is important to limit the gap width to below the critical threshold

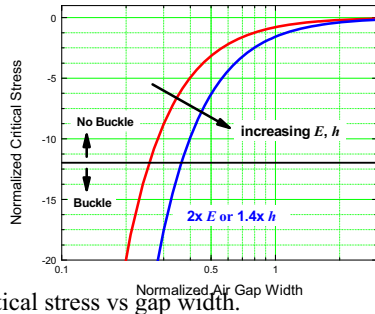


Fig. 6: Critical stress vs gap width.

for buckling. Fig. 6 shows that since buckling will not affect the minimum pitch features, they can be gapped thus preserving performance. Increasing the modulus or hardness of the cap delays onset of buckling as gap width increases.

For the optical gapping scheme (1), it is essential to limit the size of the airgap in the cap to ensure electrical and mechanical reliability. However, this affects the overall capacitance benefit that can be obtained. The other factors that affect the capacitance are the depth of the gap, the pinch-off height and the amount of sidewall re-deposition. Consequently, through appropriate optimization of these factors, it is still possible to get a large capacitance drop. As can be seen in figure 7, the depth of the airgap does have a significant effect

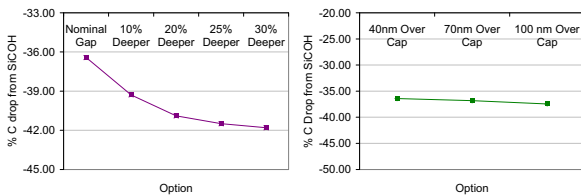


Figure 7: Effect of gap depth on capacitance drop

Figure 8: Effect of pinch-off height on capacitance drop

on the overall capacitance, with a majority of the benefit being realized when the gap is just 25% deeper than the trench.

However, figure 8 shows that increasing the pinch-off height does not significantly impact the performance. Finally, figure 9 shows that the sidewall re-deposition does indeed have a significant effect on the overall capacitance. However, despite limiting the size of gap in the cap, a large (~35%) capacitance drop can be obtained through appropriately minimizing the re-deposition. This is also readily realizable in practice as can be seen from figure 10.

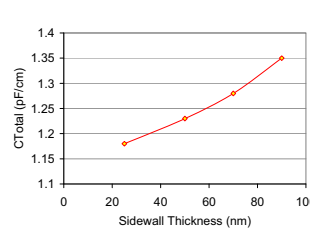


Fig. 9: Effect of sidewall re-deposition on Ctotal

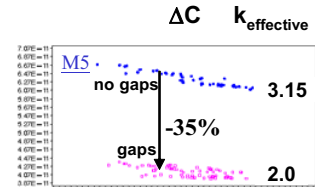


Fig 10: Measured C drop from SiCOH

Figure 11 shows that capacitance extractions can be performed by simulating the exact shape of the final airgap structure. The capacitance obtained from the structure in the simulation agrees very well with the measured capacitance which validates the models used to predict capacitance trends. Figure 12 shows that despite the presence of a pointed seam in the airgap structures, we can build multilevel airgaps without any cracking. These structures also passed stringent packaging tests including a 1000 hr DTC (-45 to +125 C) without any failures with 6 gapped levels in a production microprocessor (1).

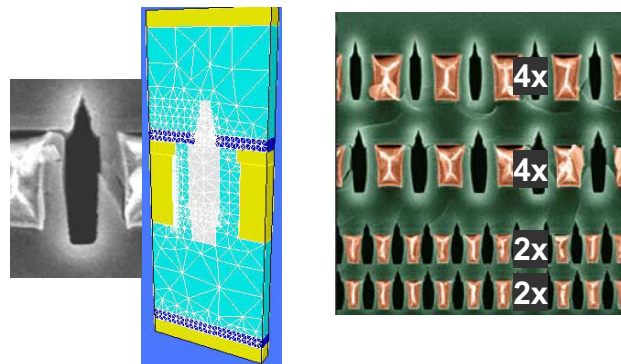


Fig. 11: Finite element simulation of Fig. 12: Multi-level gap shape for model/hardware validation

Conclusion

The studies presented here have shown that limiting the widest space that can be gapped and ensuring that the opening in the cap is small enough to allow for quick pinch-off, ensures that the self-assembly based airgap and the lithographic airgap structures are mechanically stable respectively. However, through careful optimization of the gap size and shape, it is still possible to realize a large capacitance drop of ~35% ($k_{eff} \sim 2.1$).

References: (1) S. Nitta *et. al.* Adv. Metal. Conf. 2007
(2) R. Daamen *et.al.*, Intl. Interconnect Tech. Con. 2005
(3) H. G. Tomkins, "A Users Guide to Ellipsometry" (Academic, New York, 1993)