

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,
Patent Owner

Case No.: IPR2024-00790
U.S. Patent No. 10,868,031
Issue Date: December 15, 2020

Title: MULTIPLE-STACK THREE-DIMENSIONAL MEMORY DEVICE
AND FABRICATION METHOD THEREOF

PETITIONER'S REPLY

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Exhibit	Description
1001	U.S. Patent No. 10,868,031 to Liu et al.
1002	File History of U.S. Patent No. 10,868,031 to Liu et al.
1003	Declaration of Dr. Sanjay Banerjee (“Banerjee”)
1004	<i>Curriculum Vitae</i> of Dr. Sanjay Banerjee
1005	U.S. Patent No. 10,381,369 to Kim et al. (“Kim”)
1006	U.S. Patent Publ. No. 2019/0081061 A1 to Tessariol et al. (“Tessariol”)
1007	Aritome, “NAND Flash Memory Technologies” (2016)
1008	Silvagni, “3D NAND Flash Based on Planar Cells,” Computers 2017
1009	Micheloni et al., “Inside Solid State Drives (SSDs)” (2 nd Ed. 2018)
1010	U.S. Patent No. 10,475,737 to Tang et al.
1011	U.S. Patent No. 10,559,583 to Park et al.
1012	U.S. Patent No. 9,768,186 to Shimabukuro et al.
1013	U.S. Patent No. 9,728,499 to Shimabukuro et al.
1014	U.S. Patent No. 9,299,641 to Sekar et al.
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1017	Minute Order, Dkt. No. 42, dated February 22, 2024 in <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC</i> , Case No. 3:23-cv-05792-RFL

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1018	Combined Civil and Criminal Federal Court Management Statistics (December 31, 2023), available at https://www.uscourts.gov/sites/default/files/data_tables/fcms_na_distcomparison1231.2023.pdf
1019	Docket from <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC</i> , Case No. 3:23-cv-05792-RFL
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1022	Sharpe, W.N., et al., “Mechanical Properties of MEMS Materials,” DARPA, AFRL-IF-RS-TR-2004-76 (March 2004)
1023	Wolf. S., et al., “Silicon Processing for the VLSI Era, Volume 1 – Process Technology, Chapter 15, Multilevel Interconnects for ULSI,” (2 nd Ed. 2000)
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1027	Wolf. S., et al., “Silicon Processing for the VLSI Era, Volume 1 – Process Technology,” (1 st Ed. 1986)
1028	Transcript of the deposition of Dr. Kelin Kuhn, dated March 28, 2025, in IPR2024-00789, concerning U.S. Patent No. 10,861,872
1029	U.S. Patent Publ. No. 2017/0148805 to Nishikawa et al. (“Nishikawa”)
1030	U.S. Patent Publ. No. 2017/0236746 to Yu et al. (“Yu”)

I. INTRODUCTION

YMTC admits that Kim and Tessariol disclose nearly every limitation of the challenged claims, including the unaligned channel sidewalls that the Examiner incorrectly found to be novel. YMTC, however, claims that these references do not disclose a filling structure “surrounding” the staircase structure. This argument fails because it erroneously construes “surrounding” to mean “encircling.” Even if this construction were correct (it is not), the argument still fails because YMTC ignores the prior art’s disclosure of CVD—a well-understood technique for depositing a conformal filling layer over the entire staircase structure.

YMTC also claims that these references do not disclose “pillar-support material,” even though they expressly disclose “support” pillars. This argument asks the Board to commit legal error by demanding more detail in the prior art than what the ’031 patent discloses and claims.

The Board should find all challenged claims unpatentable.

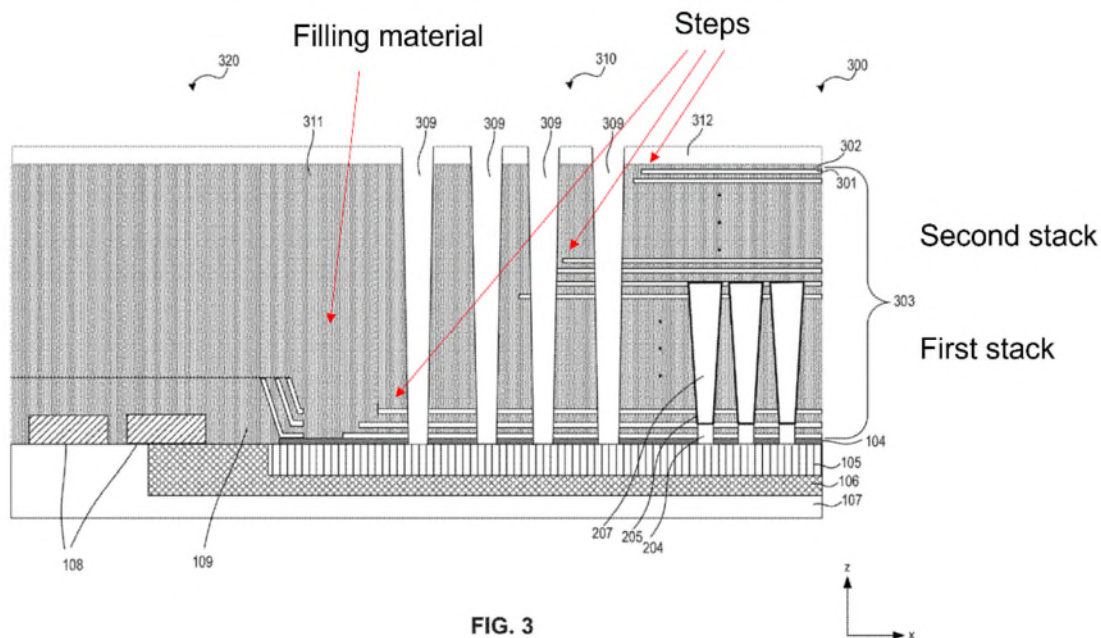
II. CLAIM CONSTRUCTION

The claims recite “a filling structure surrounding the multiple-stack staircase structure.” YMTC argues that the term “surrounding” means “encircling” or “all the way around (something).” POR, 14-19. YMTC’s expert, Dr. Kuhn, clarified that “encircling” does not necessarily mean “a contiguous structure that is connected all

the way around” the staircase but is broadly “akin to policemen surrounding a house,” even in a non-contiguous way. EX1026, 147:5-148:10.

YMTC’s interpretation is flatly inconsistent with the specification. EX1025 (“Banerjee-Reply”), ¶¶11-19; *see Phillips v. AWH Corp.*, 415 F.3d 1303, 1313 (Fed. Cir. 2005) (finding plain meaning is based on “the context of the entire patent”). The ’031 patent makes clear that “a filling structure surrounding the multiple-stack staircase structure” requires nothing more than a “filling structure” that “fill[s] [the] space formed by the formation of [the multiple-stack] staircase structure.” ’031, 13:11-38. Figure 3 shows “memory structure 300 ... formed by forming a two-stack staircase structure 303 from dielectric stack 203 [and] ***filling space formed by the formation of staircase structure 303 with a dielectric filling structure 311....***” *Id.*, 11:44-60, 12:65-13:64, 13:11-21.¹ More specifically, “after staircase structure 303 is formed,” “***a dielectric filling material can be deposited ... to fill in the space formed by the removal of the portions of dielectric stack 203:***”

¹ All emphases added unless otherwise noted.



Id., 13:36-59, Fig. 3 (annotated). This filling material “**can be deposited by any suitable deposition methods such as CVD.**” *Id.* Then, any “suitable planarization method (e.g., CMP...) can be performed to remove any excessive dielectric filling material overlying the topmost surface of staircase structure 303.” *Id.* The ’031 patent explains that **what remains after planarization of “the deposited dielectric filling material (e.g., over staircase structure 303 and isolation layer 109) [forms] dielectric filling structure 311 that surrounds staircase structure 303.”** *Id.*

In short, the ’031 patent consistently explains that a “filling structure” is deposited (via, e.g., CVD) to fill the “space formed by the formation of [the] staircase structure”—and, **by filling in the space**, the “filling structure ... surrounds” the staircase structure. Banerjee-Reply, ¶15; ’031, 11:44-60, 13:36-59, 19:41-49, 22:61-23:9, 24:26-38; EX1026, 97:21-101:14, 116:18-117:13.

Citing portions of the same disclosure, YMTC offers the conclusion that the “filling structure **therefore** surrounds/**encircles** the multiple-stack staircase structure **when it is deposited to the left, right, back, and front of the staircase structure.**” POR, 17. But the ’031 does not teach or illustrate the filling structure “deposited to,” e.g., the “back” and “front” (i.e., y-direction in Fig. 3) of the staircase. Banerjee-Reply, ¶16. The claims cannot require more than what the specification supports.

To the extent there is **any** support for depositing on all four sides of a staircase structure, it is that a POSITA would have known that “deposition” on all sides would occur when using well-known techniques, like CVD, for the reasons discussed below. Banerjee-Reply, ¶17; EX1026, 126:5-19, 159:13-160:8, 213:18-24; *Uber Techs., Inc. v. X One, Inc.*, 957 F.3d 1334, 1339 (Fed. Cir. 2020) (“The specification ... is entirely silent on how to [implement the technology], suggesting that a [POSITA] was more than capable of selecting between the known methods.”). Thus, if the Board adopts YMTC’s interpretation, it necessarily follows that Kim and Tessariol disclose (or at least render obvious) a “filling structure surrounding” the staircase structure because they expressly teach the same deposition techniques (e.g., CVD) that the ’031 patent uses to accomplish “surrounding” the staircase.

III. GROUND 1: INDEPENDENT CLAIM 1 AND DEPENDENT CLAIMS 2-4 ARE OBVIOUS OVER KIM

YMTC disputes only claim limitations [1.D] and [4.B]. POR, 23.

A. Claim 1

YMTC argues that Kim does not disclose or render obvious “a filling structure surrounding the multiple-stack staircase structure” because “Kim does not show” insulating material extending in the (a) “-D1 and +D1 directions” (i.e., front and back sides) and (b) “-D2 direction” (i.e., left side). POR, 23-45. As an initial matter, YMTC’s arguments fail because they ignore the basics of CVD and treat partial drawings of Kim’s memory device as if they were complete. Pet., 32-38; Banerjee-Reply, ¶¶18-22. Critically, Kim teaches that “filling insulation layer 110 may be ***formed on an entire top surface*** of the substrate 100 ***to cover*** the” stack structures, which include the staircase. Kim, 6:3-5, 9:53-58, 11:11-21. As the Board correctly found (ID, 15-17 (citing Kim, 10:17-20)), by forming an insulating material on the entire substrate (via, e.g., CVD) to cover the stack, the insulating material ***would necessarily encase the memory device*** and, thus, surround the staircase structure.

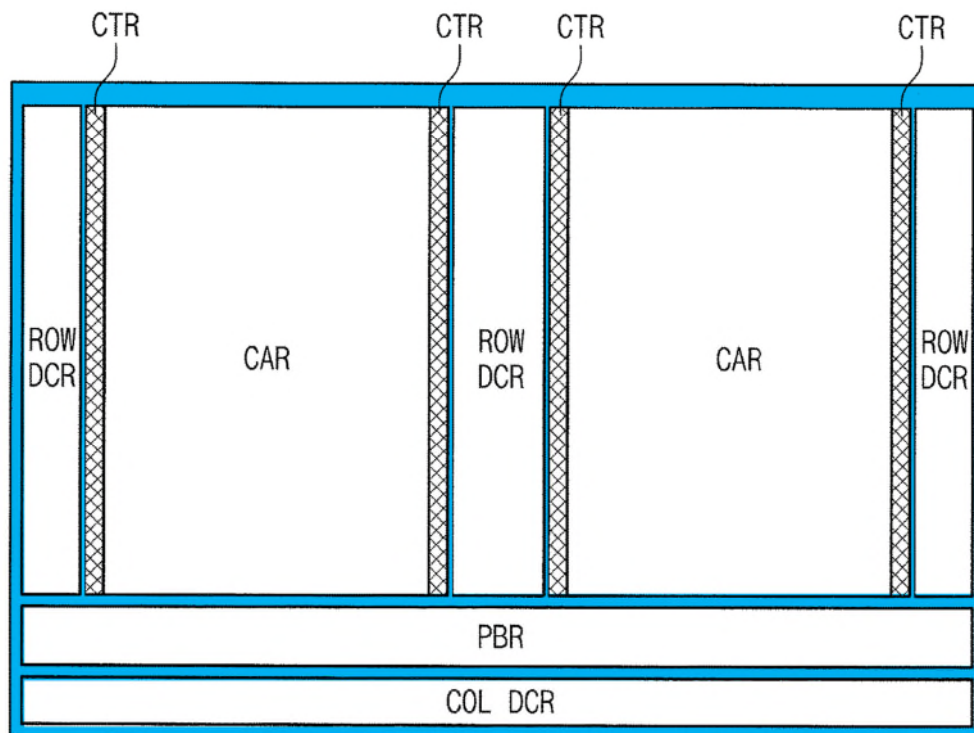
Indeed, a POSITA would have understood Kim’s teachings—i.e., depositing an insulating material to “cover” the substrate and memory device such that planarization is required—necessarily means that the “filling structure” would encase the memory device and, thus, would surround the staircase structure. As Dr. Banerjee explains, a POSITA would have understood the term “substrate” in Kim

includes the broader “wafer” on which the memory device sits (separated from other memory devices being fabricated on the wafer). Banerjee-Reply, ¶¶23-30 (citing EX1027); EX1026, 15:9-15. To electrically isolate the staircase after etching, one would commonly use CVD to deposit insulating material (as Kim teaches), which would cover the entire wafer with a uniform film of insulating material, including the side surfaces of any vertical structure (such as the staircase). Indeed, YMTC’s expert testified that “filling [techniques using] dielectric material [are] the mainstay of the semiconductor industry... There’s a myriad of options because it’s a very baseline foundational technology in the industry”—“assuming that it’s a *typical* conformal CVD process, *you’re going to get a blanket layer of CVD that’s across the entire wafer* ... following the topography of the wafer.” EX1026, 15:9-15, 32:9-33:9, 48:2-54:21, 65:6-21, 99:13-101:14, 106:10-19, 109:24-110:6, 111:23-112:8.

Ignoring how CVD (a “baseline foundational technology”) works, YMTC focuses on Kim’s figures (like Fig. 4A) to suggest, e.g., there is no room for filling material on the left-hand side or the front and back. POR, 24-31. But YMTC’s expert admitted that Figure 4A would have been understood to be a partial view. EX1026, 178:3-10, 181:19-182:5. What’s more, Kim discloses forming various regions on a substrate so as to leave room to deposit filling material that completely encircles the staircase regions (and, of course, fills the portions that the staircase formation removes). Banerjee-Reply, ¶¶31-33. Figure 1 is a top-down block

diagram that further illustrates various regions of Kim's memory device, including the CAR (cell array region) and CTR (connection region, i.e., staircase region):

FIG. 1

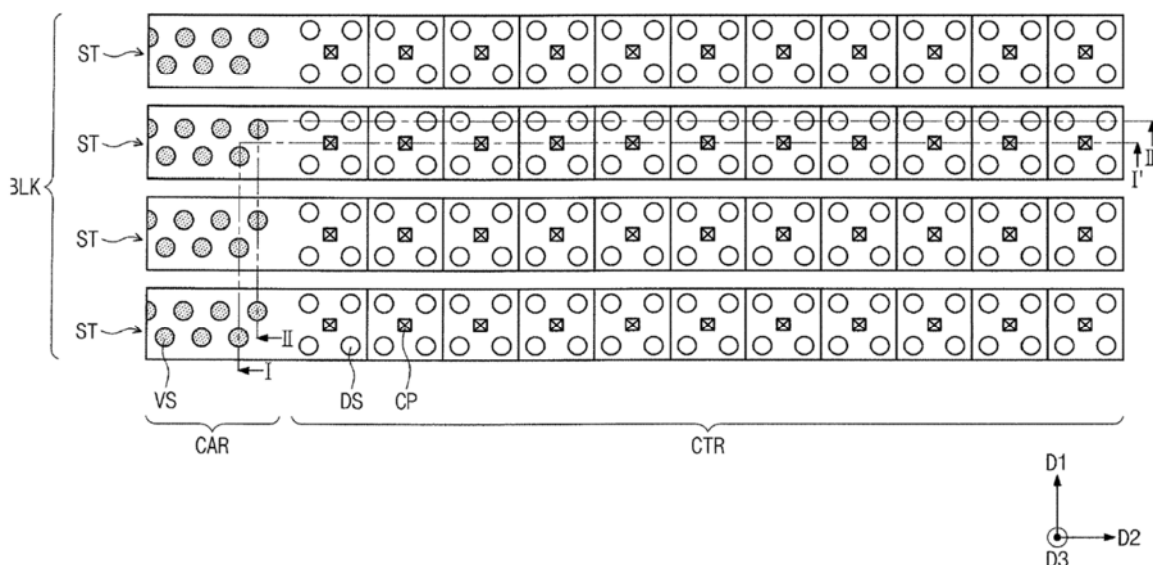


Kim, Fig. 1 (annotated), 4:59-67. As illustrated, the CAR and CTR regions—which embody stack structures—sit on a substrate (portions in blue) (which is part of the wafer, *see infra*).

The rest of Kim confirms that these regions do not extend to any substrate edge. Banerjee-Reply, ¶¶34-36. Specifically, Kim discloses “cell array block BLK may be disposed on the substrate 100.” Kim, 5:60-6:10. Block BLK can include several “stack structures ST, each of which includes ... vertically alternatively

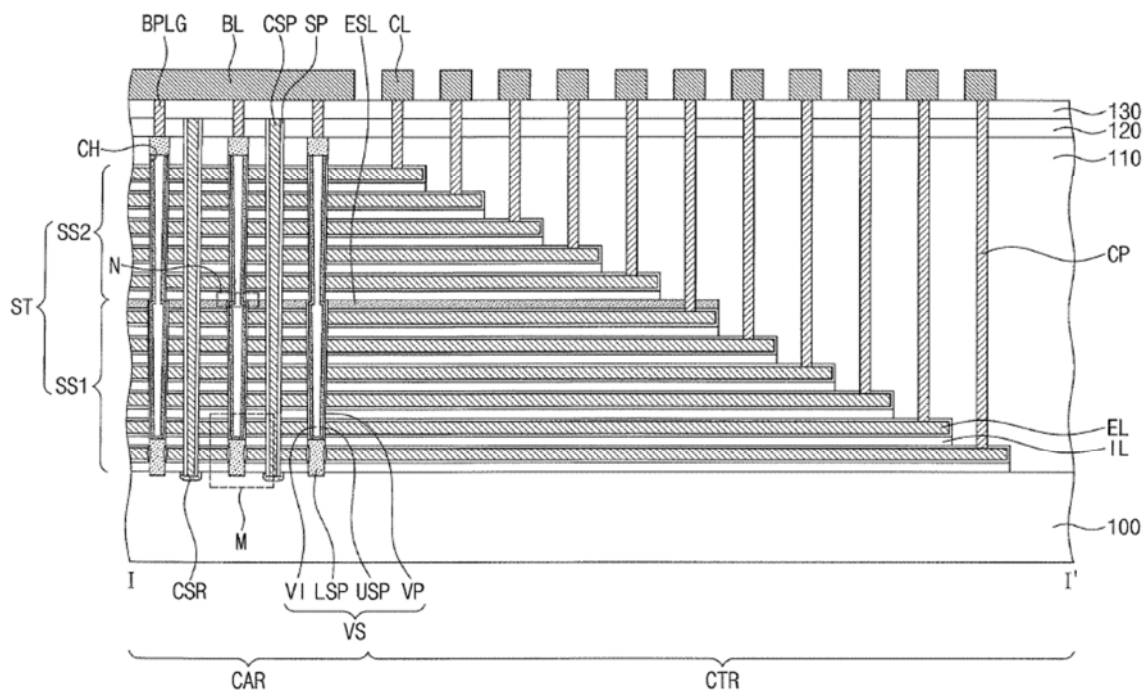
stacked” layers. *Id.* Figure 3 shows that stack structures “may extend from the” CAR region “onto the” CTR region “in a second direction D2,” where stack structures are “arranged in a first direction D1” and laterally spaced apart:

FIG. 3



Id., 5:60-6:10, Fig. 3; *see also id.*, 5:60-66 (referring to “mold structures” instead of “stack structures” for Fig. 3). Kim explains that a portion of the “stack structures” (in the CTR region) “may have a staircase structure.” *Id.*, 6:30-40. In other words, stack structures include both a “CAR” region and a “connection region CTR,” which includes the staircase. And consistent with Figure 1 and the discussion above, Figure 4A illustrates the right-hand side of such a layout with the CAR and CTR regions formed within (and not going beyond) the border of substrate 100:

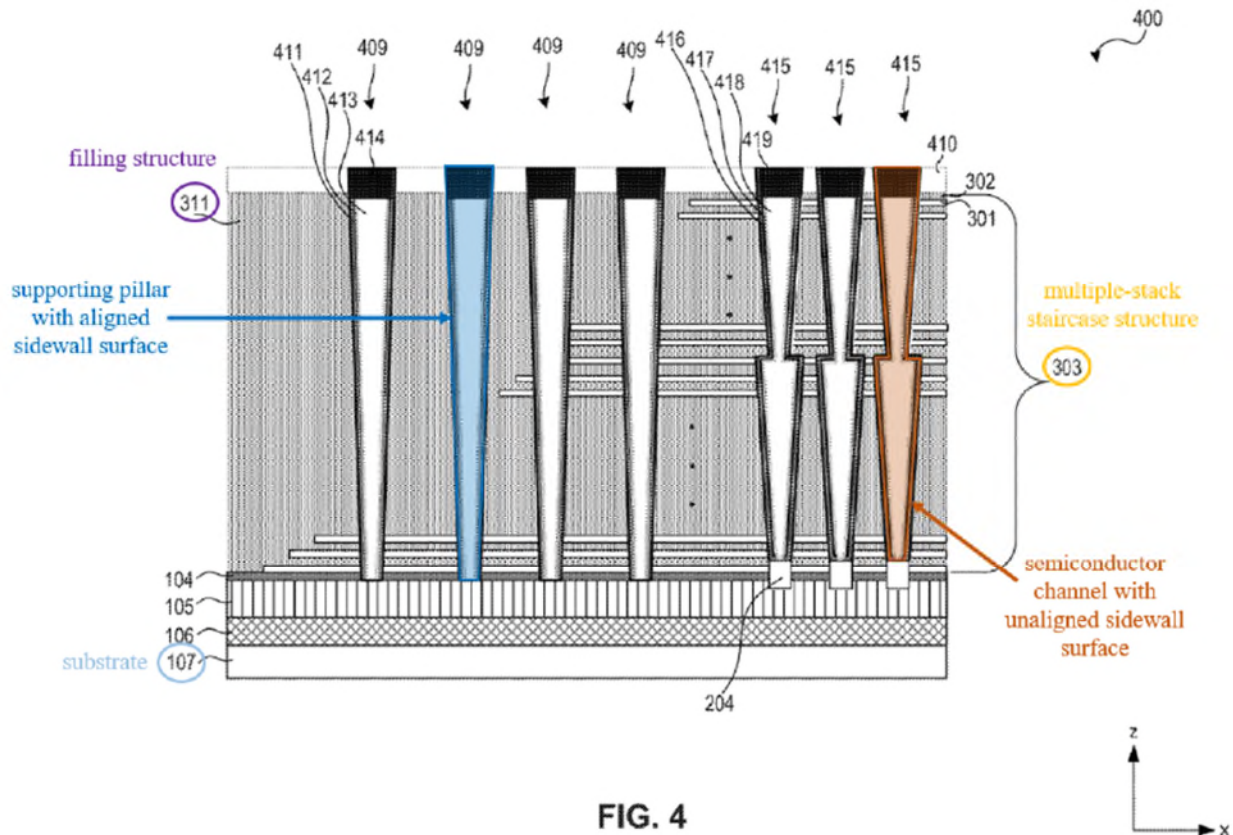
FIG. 4A



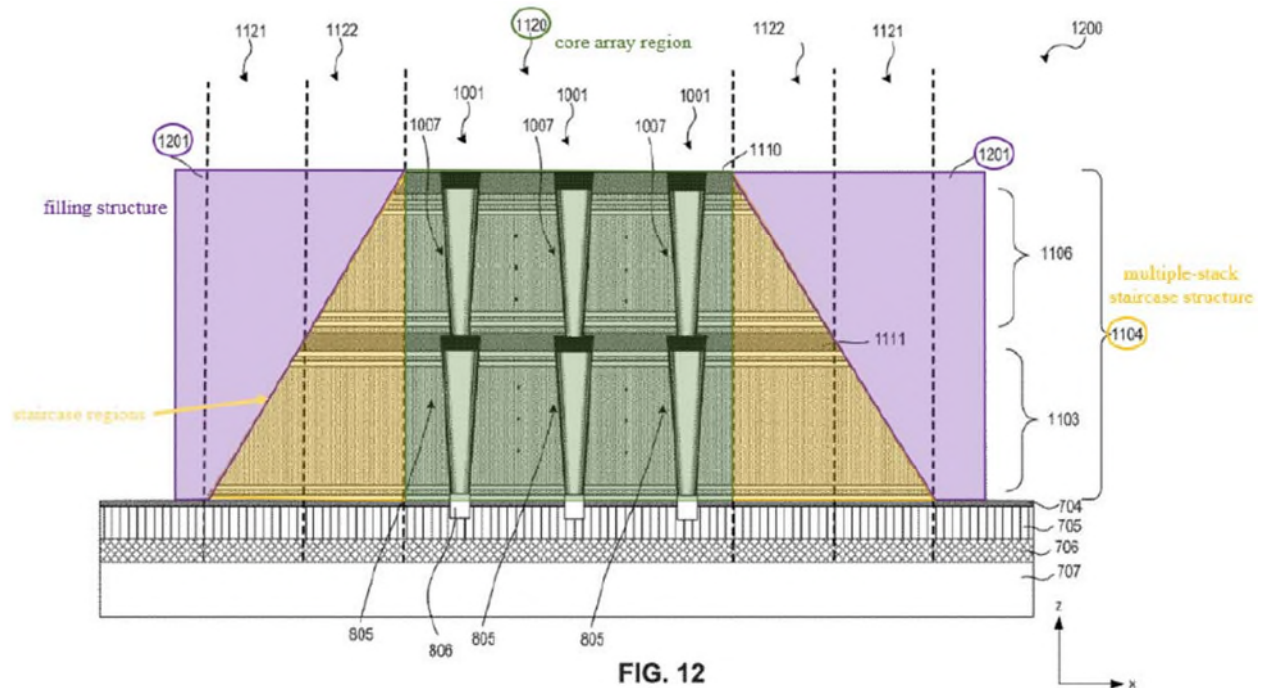
Id., Fig. 4A. Moreover, while Figure 4A shows a partial view of the device, it (and several other of Kim’s figures) “contain[] a 90-degree bend so” that it can illustrate “cross-section” of both “the array and staircase” (POR, 28 n.5). In other words, this 90-degree illustration shows how “insulation layer 110” extends in the D1 direction (e.g., flowing over multiple stack structures) and D2 direction (e.g., flowing over and past the outer edge of the staircase). Banerjee-Reply, ¶35. Moreover, Figure 1 and the above description all demonstrate that the substrate would extend beyond all sides of the memory device, leaving bare substrate bordering any region.

At bottom, ***regardless of what YMTC argues*** for this limitation, YMTC cannot rebut that Kim discloses the same type of “surrounding” that the ’031 patent

discloses. Banerjee-Reply, ¶¶37-39. In particular, when construing the term “surrounding,” YMTC argues that “Figs. 4 and 12 of the ’031 ... show that the multiple-stack staircase structure is encircled by the filling structure:”²



² YMTC’s expert contradicted this position, admitting Figures 4 and 12 **do not** alone show staircase structure “encircled by” filling structure. EX1026, 133:16-135:15.



POR, 15-17 (YMTC's Annotations). But these figures are indistinguishable from, e.g., Kim's Figures 1 and 4B:

FIG. 1

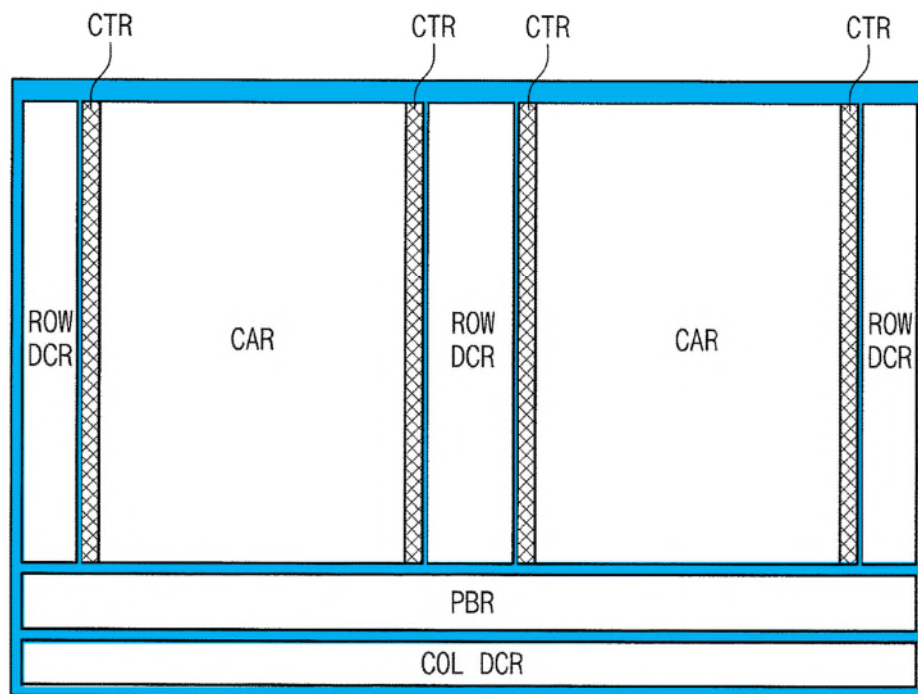
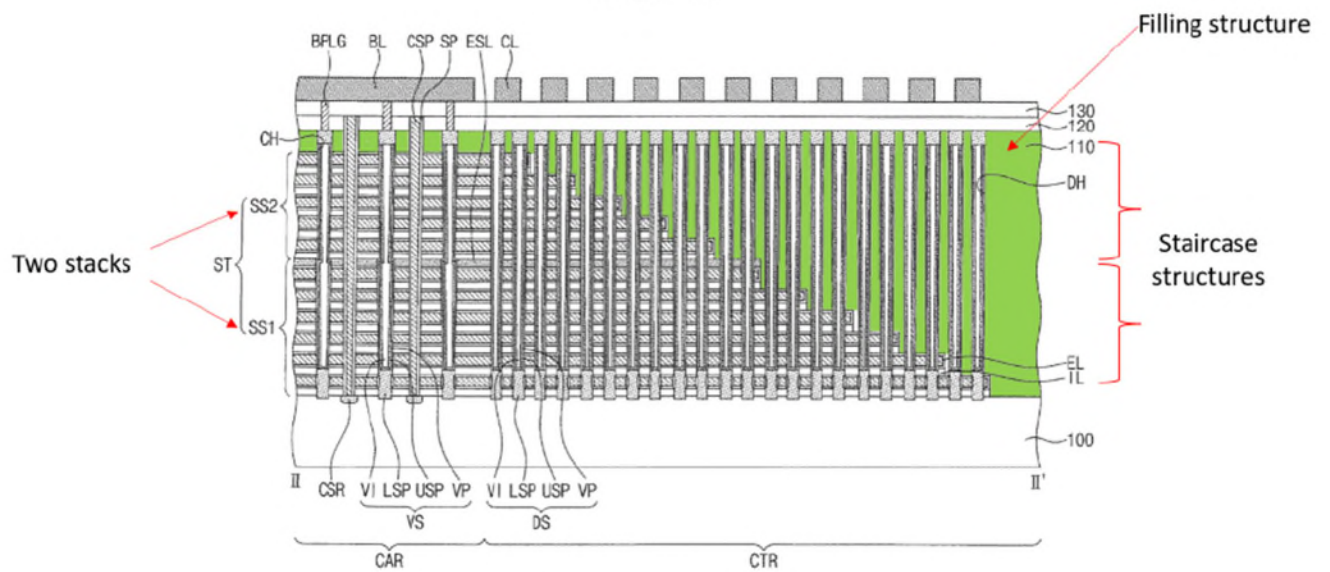


FIG. 4B



Kim, Figs. 1, 4B (annotated).

Similarly, YMTC cites 13:36-48 and 22:61-23:9 of the '031 patent to argue that the filling structure “encircles” the staircase. POR, 17. These passages disclose forming the filling structure using CVD and planarization. *Id.*; see EX1026, 116:2-117:13. Kim, too, discloses the same CVD and planarization. Kim, 9:53-58, 10:17-20. YMTC cannot credibly argue that the '031 patent describes a filling structure that “encircles” the staircase but Kim does not.³ Banerjee-Reply, ¶38.

1. Kim’s “Filling Structure” Extends in the “-D1 and +D1 Directions”

YMTC argues that cutting “trenches” into Kim’s memory devices means “that [insulation] layer 110 does not cover the side of the stack structures” in the D1 direction. POR, 27-30. This argument fails for several reasons.

First, YMTC improperly limits Kim to trench-only embodiments. Banerjee-Reply, ¶¶39-40. When describing “trenches,” Kim exclusively uses “permissive” language—e.g., “may be defined” or “may extend.” Kim, 12:9-19, 18:21-33; EX1026, 221:8-222:15. Thus, forming “trenches” is merely an optional

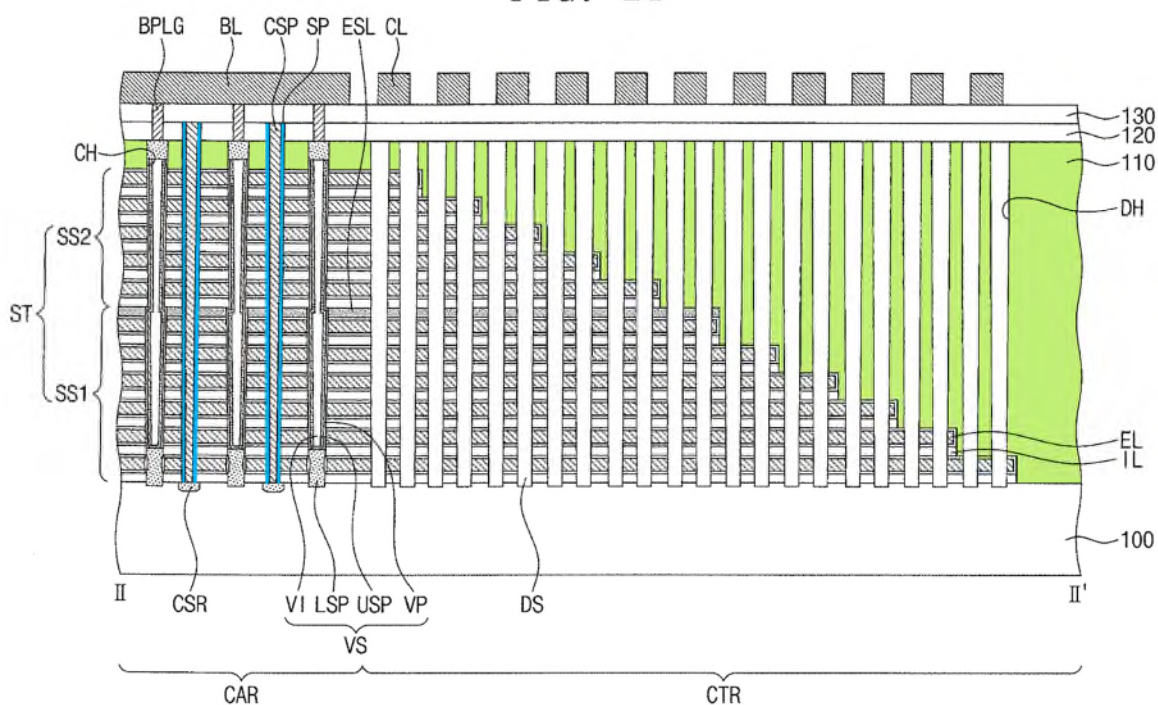
³ It would be legal error to require that the prior art expressly use the word “surrounding” in order to disclose limitation [1.D]. *Adasa Inc. v. Avery Dennison Corp.*, 55 F.4th 900, 910 (Fed. Cir. 2022) (a “reference need not disclose the elements in the very same terms [as] the [challenged] patent”).

embodiment. *AliveCor, Inc. v. Apple Inc.*, IPR2023-00948, Paper 30 (PTAB Jan. 7, 2025) at 45-46 (finding “the term ‘may’ is permissive”).

Second, even if Kim requires “trenches,” YMTC’s argument fails because, as explained above, Kim teaches that insulating material covers the entire substrate and encases the memory device. *See supra* §III.A. In other words, trenches cutting *internally* within a memory device are irrelevant to whether the filling structure surrounds the staircase structure, just like a fence surrounds a house even though it doesn’t cut through the house itself. Banerjee-Reply, ¶41.

Moreover, YMTC’s argument still fails because Kim’s trenches include an insulating liner that forms a filling structure (with, e.g., insulation layer 110) to surround the staircase. Banerjee-Reply, ¶41. After trenches are formed (*see* Figs. 12 and 13), Kim teaches that “[i]nsulating spacers SP” (blue, below) and “common source plug CSP *may be formed in each of the trenches:*”

FIG. 14



Kim, 12:9-35, Figs. 4A-4B, 14 (annotated). As shown, insulation layer 110 (**green**) encases the device, and insulating material (e.g., insulating spacers SP (**blue**)) is disposed on the walls within each trench. Banerjee-Reply, ¶41 (explaining insulation is necessary to prevent issues when using trenches for common source lines). Thus, even under YMTC’s requirement, the combination of insulation layer 110 and insulating spacers SP forms “a filling structure surrounding” the staircase.⁴

⁴ As the Board recognized (see ID, 24), the claimed “filling structure” can be one or more insulating materials so long as the combination that forms the filling structure “surround[s] the multiple-stack staircase structure.”

2. Kim’s “Filling Structure” Extends in the “-D2 Direction”

YMTC argues that “Kim does not show” a filling structure in the “-D2 direction” because insulation layer 110 “[is absent] to the left” and “no fundamental reason [exists]” prohibiting Kim’s figures from being “fabricated” as “drawn.” POR, 27. These arguments fail for several reasons. Banerjee-Reply, ¶¶42-49.

First, YMTC ignores Kim’s disclosure that CVD of insulating material covers the substrate. Banerjee-Reply, ¶43; *see supra* §III.A; Pet., 32-38.

Second, a POSITA would not have interpreted Kim’s Figures 3 and 4 as representing the full chip, for the reasons discussed above and shown in Figure 1. *Compare* Kim, Fig. 1 with Fig. 3; *see supra* §III.A; Banerjee-Reply, ¶¶42-45. Indeed, YMTC’s expert admitted that illustration techniques (e.g., “squiggly lines”) exist to indicate when a drawing “is intended as a fragment of a larger drawing.” EX1026, 172:12-17, 178:3-10, 181:19-182:5; Kim, 4:9-51, Figs. 3 (cutting off structures), 4A (including “squiggly lines”). And Kim does not include any disclosure that limits its “illustrative” drawings, nor does it teach that its memory devices abruptly end. *See* ID, 17.

Third, rather than grappling with what Kim actually discloses, YMTC speculates what “processing techniques” Kim *could* employ—such as “unfilled air-

gaps.”⁵ POR, 30-35. This argument is irrelevant because neither Kim, Tessariol, nor the '031 patent mentions, suggests, or illustrates “unfilled air-gaps.” Banerjee-Reply, ¶¶46-48; EX1026, 199:2-14, 256:3-5. Indeed, the “air-gap” documents that YMTC cites (and its expert identified in deposition) are further irrelevant because they are directed to creating air-gaps in “trenches” or between “interconnects,” whereas Kim teaches (1) depositing material in its optional trenches and between its components, and (2) *using “insulation layer 110” to encase the memory device.* Kim, 9:53-58, 10:17-20, 11:11-21, Fig. 1; EX1026, 65:6-11, 192:4-13 (admitting CVD was a filling technique used to electrically isolate staircases); Banerjee-Reply, ¶¶46-48. These documents also suggest that creating “air-gaps” was “very expensive” and required “additional dedicated air gap lithography.” EX2009, 2.

Finally, YMTC rehashes an argument made in its POPR that the Board should take the illustration of the memory device in Figure 24 as drawn. POR, 31-32. The Board correctly rejected this argument already. *See* ID, 14-15, 18. Apart from the reasons the Board raised, YMTC incorrectly points to “mask pattern MP3” as a “filling insulation layer,” coloring it purple, when MP3 is **not** a filling insulation layer. A POSITA would have understood that MP3 is used to etch/remove portions

⁵ A POSITA would not have understood that unfilled air-gaps would—or even practically could—cover the staircase structure. Banerjee-Reply ¶46.

of the stack and then MP3 *is removed* before, e.g., insulation layer 110 is deposited. See, e.g., Kim, 10:60-11:21, 18:7-33. In other words, the illustration of MP3 in Figure 24 has no bearing on what insulation layer 110 looks like. YMTC also ignores that Figure 24, *inter alia*, (1) is incomplete and “illustrative” of “a method [step] for manufacturing,” e.g., it fails to show memory channels (i.e., a critical part of 3D NAND); and (2) would be useless if it showed an “insulation layer” encasing the memory device (as Kim teaches) because you would be unable to view the underlying memory device features through the overlying deposited insulating material. Banerjee-Reply, ¶49.

3. Kim and the Knowledge of a POSITA Render This Limitation Obvious

The Petition demonstrates that Kim and the knowledge of a POSITA render limitation [1.D] obvious under both parties’ interpretations of “surrounding.” Pet., 35-38. YMTC’s responsive arguments all fail. Banerjee-Reply, ¶¶50-56.

First, YMTC mischaracterizes the Petition as arguing that each structure must extend symmetrically. POR, 36, 39-40. YMTC, for example, argues that “channel structures” extend “in the D3 direction but not in D1 or D2.” *Id.*, 36. This makes no sense. Each component of the device has a different purpose and structure, so whether a channel structure extends in one direction, as opposed to another direction, has no bearing on whether “insulation layer 110” extends in all directions and covers the substrate (as Kim teaches). Pet., 35; Banerjee-Reply, ¶¶51-52.

Second, YMTC misquotes Dr. Banerjee as stating Kim only discloses “filling material” on one side. POR, 37-38. In fact, his merely describes what partial Figure 10 illustrates on the right-hand side. Banerjee, ¶113; Banerjee-Reply, ¶53.

Third, YMTC contemplates edge cases of CVD that allegedly would result in the filling material not surrounding on all sides. POR, 37-38. But YMTC ignores that Kim expressly discloses a CVD technique that “may be ***formed on an entire top surface of the substrate 100 to cover the***” *stack structures*. Kim, 11:11-21; Banerjee-Reply, ¶54. In fact, YMTC’s expert testified that conformal CVD, which covers an entire structure on a wafer, was the “textbook method.” EX1026, 110:24-111:9. Not only does YMTC not cite anything in Kim that requires some sort of special CVD that allegedly would not cover the entire memory structure (apparently, “localized CVD” or “air-gap” techniques), but the mere possibility that some special, non-conformal CVD might exist does not render a limitation non-obvious. *See Intel Corp. v. Qualcomm Inc.*, 21 F.4th 784, 800 (Fed. Cir. 2021) (“It’s not necessary to show that a combination is ‘the *best* option, only that it be a *suitable* option.’”).

Fourth, YMTC argues Petitioner cannot use Park to show that using common source lines was obvious to isolate the staircase (Pet., 37) because “Kim does not reference Park” and Petitioner “does not propose combining Kim and Park” (POR, 42-44). But YMTC ignores that “non-prior art evidence of what was known”—like Park—can show “how [a POSITA] would have understood a prior art disclosure.”

Yeda Rsch. & Dev. Co. v. Mylan Pharms., Inc., 906 F.3d 1031, 1041 (Fed. Cir. 2018); Banerjee-Reply, ¶55. That is how Petitioner uses Park. Pet., 36-38.

Finally, YMTC fails to address the Petition’s showing that conformal CVD, which encases the entire structure, enables creating a beneficial top planar surface (which Kim teaches). Pet., 38; Banerjee-Reply, ¶56.

B. Claim 4

YMTC’s arguments attempt to distinguish the prior art by defining “pillar-support material” as having a “**required** stiffness and/or support function.” POR, 45-48. This interpretation is inconsistent with the specification. YMTC cites only a statement as to what material “*can be used* as the support material,” not what *must be used*. EX1026, 222:16-224:5; *see AliveCor*, Paper 30 at 45-46. YMTC ignores the ’031 patent’s explanation that “[a]ny **suitable pillar-filling materials**” can be deposited to “**form supporting pillars**.” ’031, 18:14-30; Banerjee-Reply, ¶¶57-58.

Using its improper interpretation of “pillar-support material,” YMTC then fixates on whether Kim expressly discloses this limitation. POR, 45-48. This misses the mark, however, because the Petition does not advance an anticipation argument. As explained, Kim discloses that the “dummy structures ... **may physically support** the stack structure” on the CTR region (Kim, 9:30-38) and may include a different “layer or component” than “the layer(s) or component(s) of ... the vertical structures” (Kim, 13:28-40; EX1026, 233:20-235:4). Given Kim’s teachings, it

would have been obvious to make Kim's dummy structures with a conductive core (which is different than Kim's channel structures) to "physically support" the stack. Pet., 42-44, 55-56; Banerjee-Reply, ¶59; *see Yeda*, 906 F.3d at 1041. In fact, YMTC's expert admitted that support pillars and their purposes were known in the art. EX1026, 79:2-12, 85:1-9, 91:10-23.

YMTC posits that this argument "jumps to [a] conclusion" without explaining the need or motivation. POR, 49. But YMTC ignores that Kim expressly discloses "support" pillars, and that the Petition explains why it would have been obvious "simply to use conductive vias [or] dummy vias" (which have a conductive core). Pet., 42-44, 55-56; Banerjee-Reply, ¶60. As explained, a POSITA would have been motivated to use conductive material in the support pillars because (1) "the process to form them would use the same process steps as the conductive vias," and (2) they "beneficially could serve two roles (support and interconnect) and reduce the need for additional structures." Pet., 55-56; Banerjee ¶¶156-157, 212-222.

YMTC next argues that "not all" materials have "the required stiffness and/or support function[s] to be considered a supporting material." POR, 10, 47-48, 53-54. But the Petition advances the known Tessariol conductive cores, and Tessariol describes their function as a supporting member. Pet., 55-56; Tessariol, [0041]. Moreover, other than pointing to the "Background" section (i.e., what was known in the art), YMTC's expert admitted that the '031 patent never explains what

“sufficient stiffness and/or support functions” means or how a POSITA would determine it. EX1026, 222:16-224:5, 227:19-229:12, 235:5-236:8. When a patent provides no implementation details, it is fair to conclude they are within the skill of a POSITA. Banerjee-Reply, ¶61; see *Lockwood v. Am. Airlines, Inc.*, 107 F.3d 1565, 1570 (Fed. Cir. 1997) (The patent-at-issue “does not disclose the level of detail that [PO] would have us require of the prior art”); *In re Epstein*, 32 F.3d 1559, 1567-68 (Fed. Cir. 1994) (same).

Relatedly, YMTC fixates on Dr. Banerjee’s discussion of elastic properties, arguing that he incorrectly correlated “conductivity [with] Young’s modulus.” POR, 50-54. But Dr. Banerjee never made such a restrictive correlation. Instead, he stated that elastic properties “determine the suitability of a material as [a] pillar.” Banerjee, ¶215; Banerjee-Reply, ¶¶62-63. Moreover, YMTC repeatedly mentions “stiffness” as a requirement (POR, 51-52), but, again, YMTC identifies no disclosure in the ’031 patent that shows “stiffness” is a requirement or what “stiffness” means. EX1026, 235:5-236:8, 237:4-8; see *Lockwood*, 107 F.3d at 1570; *In re Epstein*, 32 F.3d at 1567-68. Either way, even under YMTC’s interpretation, YMTC ignores Petitioner’s showing that a POSITA would have understood that the disclosed conductive cores provide, at least, “support functions.” Pet., 55-56.

Next, YMTC argues that modifying Kim “to use Tessariol’s conductive vias ... is unconvincing” because (a) the conductive vias “are specific to its unique

device,” and (b) “there is no circuitry under [Kim’s] array or ... staircase,” so “there is no need to create connections.” POR, 52-53. Point (a) improperly assumes bodily incorporation. Banerjee-Reply, ¶64. Conductive vias (dummy or operational) are not unique to Tessariol, and a POSITA readily understood how to employ such structures in 3D NAND devices before the ’031 priority date. *Id.* The Petition also explains in detail why a POSITA would have had a reasonable expectation of success when incorporating conductive vias. Pet., 55-56, 86-89; Banerjee ¶¶156-157, 212-222. Point (b) ignores Kim’s teachings. Banerjee-Reply, ¶65 (explaining same with citation to EX1029 and EX1030). Kim discloses peripheral circuitry on the substrate. Kim, 4:59-67, Fig. 1. As was well known, peripheral devices (whether under the array or within the base substrate) require vertical conductive vias, which YMTC’s expert admitted. EX1028, 80:9-82:9.

Finally, YMTC points to “issues of thermal expansion mismatch that would result” from using, e.g., “copper” and “silicon oxide” in the dummy structures. POR, 54-55. But YMTC’s expert admitted that the ’031 patent makes no mention of “thermal expansion mismatch” and explains nothing unpredictable about using “copper” and “silicon oxide” (*see* EX1026, 238:20-239:5)—indeed, the ’031 patent repeatedly suggests (and claims) this combination. ’031, 2:18-20, 25:4-21, claim 5; *see Lockwood*, 107 F.3d at 1570; *In re Epstein*, 32 F.3d at 1567-68. Moreover, as Dr. Banerjee explained, copper was a well-known metal used in semiconductor chips

and has “well-known structural and electrical characteristics.” Banerjee ¶¶157, 211; Banerjee-Reply, ¶66. In other words, a POSITA would have understood how to address any purported mismatch issues. *See Medichem, S.A. v. Rolabo, S.L.*, 437 F.3d 1157, 1165 (Fed. Cir. 2006) (finding the presence of disadvantages “does not necessarily obviate motivation to combine”).

IV. GROUND 2: INDEPENDENT CLAIM 1 AND DEPENDENT CLAIMS 2 AND 4-5 ARE OBVIOUS OVER TESSARIOL

YMTC disputes only claim limitations [1.D], [4.B], and [5.A]. POR, 55.

A. Claim 1

YMTC argues that Tessariol does not disclose or render obvious “a filling structure surrounding the multiple-stack staircase structure” because filling material allegedly is not “present at the ends” of the memory device in the D1 and D2 directions.⁶ POR, 56-64. This argument fails, however, because YMTC ignores the Petition’s showing that Tessariol’s CVD techniques would fully encase the memory structure. Pet., 66-71; Banerjee-Reply, ¶¶67-68; *see supra* §III.A.

Whether the Board considers the filling structure as “insulating material 48” or a combination of “insulating material 48,” “dielectric material 74,” and/or “insulation material 86,” Tessariol discloses insulating material that forms a filling

⁶ The Board invited Petitioner to develop its position as to whether Tessariol’s insulating materials “encase[] the entire stack structure.” ID, 25.

structure surrounding the staircase structure under both parties’ interpretations of “surrounding.” Pet., 66-71; Banerjee-Reply, ¶69.

Tessariol teaches that a “stair step structure is formed” by removing portions of the existing stack disposed on the substrate. Tessariol, [0034]-[0035], Fig. 1. Tessariol then discloses that “[a]n insulating material 48 ... is above” the staircase structure. *Id.* This insulating material, like all “materials” described in Tessariol, “may be formed using any suitable ... technique,” including CVD. *Id.*, [0063]; see *supra* §III.A (discussing deposition process). Thus, the portions of the stack removed to form the staircase are replaced with insulating material that forms the filling structure. Banerjee-Reply, ¶¶70-71.

Tessariol then teaches that “horizontally-elongated trenches 70” can be etched and “filled with dielectric material 74”—illustrated in Figure 11. Tessariol, [0043], [0063], Fig. 11. Finally, “[i]nsulator material 86” is deposited on top of the device so that it is “surrounding components 69, 82, 81, and 84”—illustrated in Figures 15-18. *Id.*, [0046], [0063]; Banerjee-Reply, ¶72.

In short, because each of these insulating materials may be formed using CVD—which would naturally fill spaces with insulating material (*see supra* §III.A), “insulating material 48,” “dielectric material 74,” and “insulator material 86” would naturally encase the memory structure. Banerjee-Reply, ¶¶69-76. Thus, “insulating material 48”—or the combination of “insulating material 48,” “dielectric material

74,” and/or “insulation material 86”—forms a filling structure surrounding the staircase structure because insulating material encases every portion of the staircase. *Id.* As the Petition demonstrates, this enables the planarization steps. Pet., 70.

YMTC argues that Tessariol’s figures “do not show the outer ends/sides of the device,” pointing to Figure 7. POR, 59-61. But YMTC fails to acknowledge that Figure 7, and others, illustrate only a “**portion**” of the disclosed substrate and memory device. Tessariol, [0008]-[0025]. And, as explained above, a POSITA would have understood that more than the illustrated “portion” exists and that the device sits on a much broader wafer—which is consistent with (1) Tessariol’s teachings and (2) the understanding that techniques like CVD would uniformly deposit insulating material on the substrate. Banerjee-Reply, ¶77; *see supra* §III.A.

YMTC next argues that (1) “Tessariol’s ‘dielectric material 74’ divides but does not surround” the staircase structure, (2) “Tessariol’s insulator material 86 ... covers only the top surface of the stacks,” and (3) the combination of insulating materials “does not” encase “the ends of Tessariol’s device in either the D1 or D2 direction.” POR, 59-64. But these arguments simply ignore how CVD of insulating materials would work in practice and ignore that the figures only illustrate a “portion” of the device. Banerjee-Reply, ¶78; *see supra* §III.A.

With respect to obviousness, YMTC rehashes the same arguments from Ground 1—including that “Dr. Banerjee ... incorrectly conflates planarizing with

surrounding,” that “there are a variety of well-known techniques for creating embedded air-gaps in planarized structures,” and that Tessariol/Kim “fail[] to teach [1.d] and therefore the combination” does not disclose it. POR, 63-64. But these arguments fail for the same reasons above. Banerjee-Reply, ¶79; *see supra* §III.A.

B. Claim 4

The Petition demonstrates that Tessariol discloses metals as “a pillar-support material.” Pet., 77-79, 83-85. YMTC counters that “Tessariol does not disclose the type of metal in its conductive core and does not disclose that the metal is a support material.” POR, 65-66. But YMTC ignores Tessariol’s teachings. Tessariol teaches that dummy structures can “*elevationally support[] the stack and prevent[] [it] from collapsing.*” Tessariol, [0041]; *see* Pet., 24-26, 77-79. These structures “comprise a conductive core ... and an insulative periphery,” and an example of a “conductive core” is “metal material.” Tessariol, [0038], [0049]. According to Tessariol, “metal material” can be “*an elemental metal.*” *Id.*, [0066]. A POSITA would have understood that “elemental metal” includes any well-known metal from the periodic table used in semiconductor memory fabrication. Banerjee-Reply, ¶80. In fact, YMTC’s expert admitted that “copper, cobalt, nickel, and aluminum” (which are identified as “pillar-support materials” examples in the ’031 patent) are “elemental metals.” EX1026, 238:4-10.

YMTC complains that Petitioner “does not argue that Tessariol’s metal has sufficient stiffness and/or support functions.” POR, 65-66. But, again, (a) YMTC’s argument is based on an improper interpretation of “pillar-support material”; (b) the ’031 patent does not explain what “stiffness and/or support functions” means or how to determine it; (c) Tessariol teaches that the dummy structures “support” the stack; and (d) Tessariol discloses exactly what the ’031 patent discloses. Banerjee-Reply, ¶¶80-81; *see Lockwood*, 107 F.3d at 1570; *In re Epstein*, 32 F.3d at 1567-68.

C. Claim 5

YMTC argues there is no motivation to use “copper, cobalt, nickel, [or] aluminum” in Tessariol’s dummy structures. POR, 66-67. This argument fails because Tessariol teaches that “metal material” includes any “elemental metal”—which a POSITA would have understood to include any one of the identified metals, and YMTC fails to dispute that a POSITA would have understood as much. Tessariol, [0066]; EX1026, 238:4-10. Moreover, even if showing a motivation were necessary, the Petition shows that at least copper was well-known and broadly used in this exact context. Pet., 86. YMTC merely argues copper has “diffusion and contamination issues” (POR, 66), but it cites no evidence and fails to dispute (1) copper was well-known and (2) the ’031 patent does not address these “issues.” Banerjee-Reply, ¶¶82-83; EX1026, 258:16-259:16; *see Medichem*, 437 F.3d at 1165; *Lockwood*, 107 F.3d at 1570; *In re Epstein*, 32 F.3d at 1567-68.

V. GROUND 3: DEPENDENT CLAIM 4 IS OBVIOUS OVER KIM IN VIEW OF TESSARIOL

For Ground 3, YMTC generally argues the same positions raised in response to Ground 1 (*compare* POR, 49-53 *with* 67-69), so the Board should reject YMTC's positions for the same reasons above. Pet., 86-89; Banerjee-Reply, ¶¶84-85. In addition to rehashing arguments, YMTC argues that adding a conductive core to Kim "would unnecessarily complicate the manufacturing process." POR, 68. But YMTC fails to identify what "unnecessary complicat[ion]" a conductive core would cause. In fact, YMTC completely ignores that Dr. Banerjee explained why adding a conductive core **would not** complicate the manufacturing process. Banerjee ¶218.

YMTC argues that there is no motivation to combine Tessariol's teaching of conductive cores with a conductive liner as Kim's dummy structures. POR, 68-69. But YMTC misses the point. Banerjee-Reply, ¶86. A POSITA would have employed a conductive core in Kim's dummy structure because, e.g., Tessariol and other prior art references teach the benefits of doing so. Pet., 55-56, 83-89; Banerjee ¶¶156-157, 212-222. And Kim expressly recognizes the need by teaching peripheral devices. Kim, 4:62-67.

Finally, YMTC accuses Petitioner of using "hindsight" (in Ground 3 and repeatedly elsewhere), citing *Nautilus Hyosung Inc. v. Diebold, Inc.*, IPR2016-00633, Paper 9 (PTAB Aug. 22, 2016). POR, 35, 48-49, 66, 69-70. *Nautilus* is inapposite. There, the petitioner argued that a component "**could** be added to"

another prior art system to satisfy a claim element. *Nautilus*, Paper 9 at 21-22. The PTAB rejected the combination, however, because the petitioner (a) did not explain what a POSITA would have done, and (b) cited only conclusory discussion of a purported advantage (i.e., an opinion without any “evidence” or “factual corroboration”). *Id.* Here, Petitioner does **not** base its obviousness argument on what “could be” done, and Dr. Banerjee provides ample evidence to support the combination. Pet., 86-89; Banerjee-Reply, ¶87. Further, as explained, Kim and Tessariol expressly teach “**support**” pillars, and YMTC’s expert admitted support pillars and their purposes were known. EX1026, 79:2-12, 85:1-9, 91:10-23.

VI. GROUND 4: INDEPENDENT CLAIM 1 AND DEPENDENT CLAIMS 2 AND 4-5 ARE OBVIOUS OVER TESSARIOL IN VIEW OF KIM

For Ground 4, YMTC generally rehashes arguments from other Grounds (POR, 70-72), so the Board should reject YMTC’s positions for the same reasons above. YMTC also argues that Petitioner’s stated motivation to use Kim’s fill techniques in Tessariol “to provide for” a planarized surface “is vague and conclusory because” Petitioner does not identify a “specific filling technique from Kim” or how a POSITA would have incorporated the technique. POR, 71. But YMTC simply ignores the Petition. It explained that Tessariol and Kim depict planar surfaces, and a POSITA would have used techniques—like “Kim’s fill techniques”

(e.g., CVD) that are “textbook”—to provide for a planarized surface.⁷ Pet., 90-96; Banerjee ¶231; Banerjee-Reply, ¶¶88-89; EX1026, 110:24-111:9; *see supra* §III.A.

VII. CONCLUSION

Petitioner respectfully requests that the Board enter a final written decision finding the Challenged Claims unpatentable.

⁷ The Board states that Ground 4 does not rely on Kim for limitation [1.D]. ID, 26. Ground 2 expressly discusses Kim (Pet., 70) and Ground 4 incorporates Kim’s teaching for [1.D] (Pet., 90-93). Ground 4 does not apply a separate claim mapping for [1.D], because it relies on the same Kim disclosures. *Id.*

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Dated: April 15, 2025

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CERTIFICATE OF COMPLIANCE

The undersigned certifies that the foregoing Petitioner's Reply complies with the type volume limitation in 37 C.F.R. § 42.24. According to the utilized word-processing system's word count, the petition—excluding the caption, table of contents, table of exhibits, mandatory notices, certificate of word count, and certificate of service—contains 5,545 words.

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CERTIFICATE OF SERVICE

The undersigned hereby confirms that the foregoing Petitioner's Reply and associated exhibits were caused to be served on April 15, 2024 via electronic mail, upon the following attorneys of record for the Patent Owner:

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