

1 UNITED STATES PATENT AND TRADEMARK OFFICE
2 BEFORE THE PATENT TRIAL AND APPEAL BOARD

3 Case No. IPR2024-00790
4 U.S. Patent No. 10,868,031

5 MICRON TECHNOLOGY, INC.,

6 Petitioner,

7 -vs-

8 YANGTZE MEMORY TECHNOLOGIES
9 COMPANY, LTD,

Patent Owner.

10 _____/

11
12
13 DEPOSITION OF
14 Kelin Kuhn

15 Monday, March 31, 2025
16 8:58 a.m. - 4:36 p.m.

17 Remote Location
18 Via Zoom Videoconference
19 All Parties Remote
20
21
22

23 Stenographically reported by:
24 Erica Field, RDR, CRR, CA-CSR, TX-CSR,
25 GA-CSR, WA-CSR, NM-CCR, IL-CSR, NJ-CCR,
FL-FPR, OR-CSR, NY Notary, FL Notary,
AK Notary, DC Notary
Job No. 978565

1 REALTIME VIDEOTAPED STENOGRAPHIC
2 DEPOSITION of KELIN KUHN, taken in the
3 above-entitled matter before ERICA
4 FIELD, RDR, CRR, California Certified
5 Shorthand Reporter (License No.
6 14515), Texas Certified Shorthand
7 Reporter (License No. 12724), Oregon
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19 Professional Reporter (License No.
20 1109), New York Notary, Florida
21 Notary, Alaska Notary, DC Notary taken
22 via remote videoconference on Monday,
23 March 31, 2025, commencing at 8:58
24 a.m.

25

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NO EXHIBITS MARKED

1 Thereupon,
2 the proceedings began at 8:58 a.m.:

3 MR. KENYON: Just for the
4 record, my name is Brooks Kenyan with
5 Orrick on behalf of petitioner Micron.

6 MR. CROSS: I'm Allen Cross with
7 Ropes & Gray on behalf of patent owner
8 YMTC.

9 Whereupon,

10 KELIN KUHN, PHD,
11 having been first duly sworn or affirmed, was
12 examined and testified as follows:

13 DIRECT EXAMINATION

14 BY MR. KENYON:

15 Q. Good morning, Dr. Kuhn.

16 A. Well, good morning.

17 Q. You've been deposed before,
18 correct?

19 A. That's correct.

20 Q. About how many times?

21 A. I'd have to look at my CV to
22 remember. It's on the order of 10-ish. I
23 think by the end of this round I may be
24 approaching 15.

25 Q. Okay. So I know you're familiar

1 with the process, but I do want to run
2 through a few things before we proceed.

3 So you understand you're under
4 oath today?

5 A. Yes, I do.

6 Q. If at any point I ask you question
7 and you do not understand what I'm asking,
8 will you let me know so that I can clarify it
9 for you?

10 A. Absolutely.

11 Q. Is there any reason why you cannot
12 answer fully and correctly today?

13 A. None that I'm aware of.

14 Should something come up, for
15 example, privilege or an NDA issue or
16 something like that, I'll make sure I alert
17 you.

18 Q. Okay. Other than the Zoom window,
19 do you have any other applications open on
20 your screen?

21 A. I do. What I have on my screen is
22 a folder with -- and I'll list what's in the
23 folder: It's the exhibits associated with
24 this action, my declaration, the patent
25 itself, and the prior art that I anticipate

1 we'll discuss.

2 I have nothing else open. Other
3 than Zoom, of course.

4 Q. And this action, you're referring
5 to IPR proceeding 2024-00790?

6 A. That's correct. And I'm going to
7 call it the '031 IPR, if that's okay with you.

8 Q. That works perfectly. I will call
9 it that as well.

10 And then you had mentioned a
11 declaration.

12 You're referring to the
13 declaration that you submitted in this IPR
14 proceeding?

15 A. Yes. And I have it as
16 Exhibit 2013, and it's a declaration that I
17 signed on the 21st day of January 2025.

18 Q. Okay. And then I think you
19 mentioned the patent as well; is that right?

20 A. Yes. And the patent I have, I
21 have as Exhibit 1001. It is U.S. Patent
22 10,868,031-B2 for Lu, and I'm just calling
23 that the '031 Patent.

24 Q. Perfect. And then the prior art,
25 which prior art do you have open?

1 A. I have in my folder, and let me
2 run through this, I have -- I'm going do it
3 by exhibit.

4 I have Exhibit 1005, which is,
5 turned sideways, 10,381,369-B2, Kim. I also
6 have, I haven't seen that in that form --
7 US 2019/0081061 A1 which is Tessariol.

8 Q. And is that Exhibit 1006?

9 A. That is Exhibit 1006, that's
10 correct.

11 Q. Okay. All right. Sounds good.
12 And then do you have any physical
13 documents in front of you today?

14 A. I just have an unmarked notepad
15 sitting off to one side should there become a
16 need to draw something during the deposition,
17 and then we can always scan that into the
18 record if necessary.

19 Q. Sounds good. Okay.

20 So the '031 Patent is directed to
21 3D NAND memory, right?

22 A. That's correct.

23 Q. And before July 2018, would a
24 person of ordinary skill in the art have
25 understood how to fabricate 3D NAND memory?

1 A. So I want to jump to the POSITA
2 definitions to answer this.

3 Q. Okay.

4 A. And give me a second here because
5 I need to open everything up and make it all
6 work.

7 Q. And you're referring to the POSITA
8 definitions in your declaration?

9 A. Yes. Because there is a slight
10 difference between a POSITA as I interpret it
11 and as Dr. Banerjee interprets it. And I do
12 want to make sure that we're all clear on
13 what a POSITA would know at the time of this
14 patent.

15 So I'm jumping to page -- sorry.
16 I'm jumping to Paragraph 65 of my
17 declaration.

18 Q. Okay. And before you do that, let
19 me go ahead and just share it --

20 A. Okay. That works.

21 Q. -- in the chat.

22 A. I will be -- yeah, I'll be using
23 my own version just in case the chat
24 collapses.

25 Q. Yeah, that's totally fine.

1 So I'm sharing right now what's
2 been marked Exhibit 2013 titled, Declaration
3 of Kelin Kuhn, PhD, In Support of Patent
4 Owner's Response, and it is dated January 21,
5 2025, on the front page.

6 Feel free to use your own copy,
7 but to the extent you can pull it -- well,
8 actually, do you mind pulling it up and
9 making sure that we're on the same page and
10 you recognize this document?

11 A. Sure. Now, when I went through
12 this a day or two ago, we had the interesting
13 problem that every time I downloaded one of
14 these things, it crashed my computer. So let
15 me --

16 Q. Well, that's not good.

17 A. Yeah, that's not good. Let me see
18 if it works this time.

19 Okay. And, yes, that's the same
20 declaration. It looks identical to mine.
21 And I will return to mine just in case
22 something goes wrong with it, the chat
23 version.

24 Q. Sounds good. So why don't we go
25 back to, I think you said, Paragraph 65?

1 A. Paragraph 65, yes. Because to
2 address the question of a POSITA's knowledge
3 at 2018, I think it's worth reviewing our
4 understanding of POSITA.

5 And in Paragraph 65, I'm going to
6 skip reading through the first sentence or
7 two and jump to: Understanding the claims of
8 the '031 Patent at the time of the invention
9 would have had at least a bachelor's degree
10 in electrical engineering, computer
11 engineering, or a similar discipline, along
12 with at least two years of professional
13 experience with semiconductor memory devices,
14 or an equivalent level of knowledge and
15 experience.

16 That's my version. Dr. Banerjee,
17 which is in Paragraph 66, is slightly
18 different. He also has a bachelor's degree
19 of science and electrical engineering, a
20 similar discipline, but he has along with two
21 to three years of professional experience
22 working with researching, designing, and/or
23 teaching monolithic 3D structures and NAND
24 memory devices or an equivalent knowledge
25 skill experience.

1 So there's a little bit of
2 difference between the two definitions with
3 regards to the amount of 3D structure and
4 NAND memory devices that a POSITA would have
5 had at the time of the patent.

6 With that in mind, do you want to
7 re-ask the question?

8 Q. Sure.

9 So before July 2018, would a
10 person of ordinary skill in the art have
11 understood how to fabricate 3D NAND memory
12 devices?

13 A. So the history of 3D NAND somewhat
14 begins in 2007 with Toshiba. My memory is --
15 and I may be wrong on the date -- that
16 Samsung introduced commercially the first 3D
17 NAND. My memory is 2012. Somewhere in the
18 2012 to 2013 time frame.

19 So by 2018, there was community
20 knowledge of 3D NAND. And whether it's
21 expressly described as in Dr. Banerjee's
22 POSITA definition, where he said a POSITA
23 would have been aware and generally
24 knowledgeable about 3D NAND structures, its
25 component parts, how it operates, and how

1 it's controlled, or indirectly, in my
2 definition of POSITA, as part of that two to
3 three years of experience.

4 I think it's fair to say using
5 either definition a POSITA would have been
6 aware of and generally knowledgeable about 3D
7 NAND structures, its components, how it
8 operates, and so on.

9 Q. And so I don't think you
10 said that it's fabrication.

11 Do you -- techniques to fabricate
12 these devices were known, correct?

13 A. So --

14 MR. CROSS: Objection to form.

15 THE WITNESS: My apologies. I'm
16 jumping in too fast and the
17 stenographer should be shouting at me.

18 A. Keep in mind -- and let me remind
19 myself again of the history. Gate-all-around
20 devices did not enter the community seriously
21 until, well, I'm going to say Toshiba 2007.

22 This is a highly competitive
23 business. And Samsung's 3D NAND flash
24 introduction was heralded with massive
25 interest by the entire community, including

1 the segment I worked in. And as is well
2 known in the art, details of fabrication are
3 kept very closely guarded. There is a huge
4 amount of money involved in this business.

5 And so I think we need to be
6 careful saying that a POSITA would have been
7 specifically familiar with fabrication
8 details. Banerjee, I think, has got the
9 right statement here, generally
10 knowledgeable. But given the competitive
11 nature of this business, the strong tendency
12 for manufacturers to be holding quiet key
13 information, I don't think a POSITA would
14 have been aware of every single little
15 fabrication detail.

16 It's not taught in school.
17 There's competitive advantage. It would not
18 be something that would be widely
19 disseminated.

20 BY MR. KENYON:

21 Q. Okay. But a general understanding
22 or knowledge as to how to fabricate these 3D
23 NAND devices was known at the time?

24 A. General knowledge, that's correct.

25 Q. Okay. So I wanted to walk through

1 the fabrication process of a 3D NAND memory
2 device, the general understanding of it, the
3 -- how it would be typically made.

4 I understand that you might not
5 know the technical details or the nuances
6 that a company like Samsung versus Toshiba
7 might use, but I did want to walk through
8 that process.

9 So you would typically start with
10 a silicon wafer, right?

11 MR. CROSS: Object to form.

12 A. Well, typically, all semiconductor
13 fabrication on silicon begins with a silicon
14 wafer. I cheerfully consider it like
15 plywood. It's where everything begins.

16 BY MR. KENYON:

17 Q. Okay. And memory devices are
18 rectangular in nature?

19 A. So I'm not sure how to answer that
20 question. Integrated circuits are built up
21 of layers.

22 There's a plan view looking down
23 on the integrated circuit. There's a
24 cross-section looking sideways on the
25 integrated circuit. There's a drawn design

1 database that has objects drawn in it that
2 will eventually be patterned. There's a
3 multiplicity of fabrication operations. What
4 -- and the wafers are round.

5 What do you mean -- what exact
6 element are you referring to as being
7 rectangular?

8 Q. Are 3D -- from a plan view, are
9 3D memory devices rectangular?

10 A. So from a plan view, what I have
11 seen is that the drawn database is generally
12 Manhattan. In other words, the drawn
13 database is rectangular boxes like the city
14 of Manhattan.

15 The fabricated parts, because of
16 the very small geometry, are typically
17 rounded by optical effects. So if you do a
18 cross-section from -- look at it from the
19 plan view, you don't see a bunch of squares,
20 you see a bunch of circles.

21 So the memory array as a whole,
22 the entirety of the product, is typically
23 square, you know, the die is typically
24 square, the wafer is typically round.

25 Did that answer your question?

1 Q. It did.

2 I guess I'm just trying to
3 understand, when fabricating 3D memory
4 devices on a wafer, are you able to use the
5 entire wafer?

6 A. Oh. That's an interesting
7 question.

8 And I'm going to say -- in
9 general, the wafer is generally round. The
10 die are generally square. And you can only
11 fit a certain number of square things inside
12 a round thing without having a certain number
13 of them halve or fall off the edge or
14 whatever.

15 There's something called a shot
16 map, which is, you know, you have a
17 lithography machine that shoots each of die
18 individually, a step and repeat machine it's
19 called, and there's a thing called a shot map
20 which shows how all the die, all the little
21 square die, fit into the round wafer in a way
22 that is typically repeatedly optimized to
23 improve yield.

24 Q. Okay. And how many memory devices
25 could you fabricate on a wafer at the time?

1 A. I have no idea. I would have to
2 go back and review that. Notices depends on
3 product. And my own experience, for example,
4 at Intel where memory devices were integrated
5 into microprocessors, we would make die as
6 big as a centimeter as a half and die as
7 small as a millimeter.

8 And how many of those you fit on a
9 wafer is obviously dependent on the size.
10 Little teeny ones you can pack in closer to
11 the edge. And how many of those die actually
12 work, that's the yield, which is normally a
13 closely guarded secret by the company that is
14 making these things.

15 Q. But in general, would you be
16 making more than a hundred on each wafer?

17 A. Depends on the size. You know, if
18 we want to pick a number for discussion, if
19 we take a hundred and then go do the math for
20 how large a wafer is and how much of an edge
21 bead we have, we can figure out the size of
22 the die.

23 Q. Well, is it closer to ten per
24 wafer or a hundred per wafer?

25 A. So my memories from Intel is that

1 product wafers in general had 100 to 200 die.
2 I have vivid memories of a Wi-Fi product that
3 had 1,200 die on the wafer that drove us all
4 mad because it went over a thousand.

5 I don't have any memories of
6 anything with five die on the wafer. But
7 again, it's kind of simple math. Die size is
8 a hotly debated topic. Once you know the die
9 size, you go back and set an edge ring that
10 you don't want to put the die outside and
11 then just do the math for how many fit.

12 Q. And how big of -- how big is that
13 edge ring typically?

14 A. That depends very much on the
15 technology capability. I have seen products
16 intentionally take die right up to the edge.

17 Because there's a place at the
18 edge where the wafer begins to bevel off.
19 And then there's another place at the edge
20 where the patterning and deposition makes a
21 little ring. And then you move in a little
22 further and you start to be able to fit die
23 in.

24 And I've seen products -- I told
25 you about my product with more than a

1 thousand die. I've seen products
2 intentionally patterned right up to the edge
3 just in the hope that some of those die would
4 work.

5 And I've seen other products where
6 an integration engineer spends hours and
7 hours and hours painstakingly readjusting the
8 shot map to make sure that every die is
9 perfectly placed with regards to the edge.

10 It's all kind of a yield thing.
11 You know, if you have extremely robust
12 products, you may run them closer to the
13 edge. If some product is very touchy, you
14 may be much more careful about exactly where
15 you place it.

16 Q. Okay. And so the edge ring is the
17 distance between the die and the edge of the
18 wafer?

19 A. So it sounds like you're
20 referencing an edge ring as a term of art,
21 and I'm just speaking more generally.

22 Wafers, in general, bevel off.
23 Wafers, in general, have a no-man zone at the
24 edge before the bevel. There's a place where
25 that first die can go in. And what those

1 areas are named depends very much on the
2 company and the technology and so on and so
3 forth.

4 And, you know, I don't want to,
5 you know, make a statement that could be
6 interpreted as defining edge ring when I'm
7 just speaking in broad terms.

8 Q. Got it.

9 And would you create any
10 separation between each of the die on the
11 wafer?

12 A. So typically, the die are removed
13 from the wafer using a dicing saw.
14 Amazingly, we don't use power lasers or
15 anything. It's just a saw.

16 The saw has a certain kerf just
17 like the saw blade in your shop. The --
18 there's a thing called the scribe line or the
19 die line or the die cut line or a myriad of
20 other names, but that's where the saw goes.
21 And that's a certain width that's determined
22 by the saw technology.

23 The existence of a slot between
24 the die to run the saw blade in means you
25 have an empty space on the wafer. And

1 engineers being what they are, they probably
2 put things in that space.

3 And at least at Intel, that space
4 was called the scribe line and we put stuff
5 in it. And then when the wafer went off to
6 be diced, the saw cuts through all that stuff
7 and all the die -- they don't fall out. The
8 die actually are on this sticky-backed thing
9 and they're picked up and go off and are
10 packaged and things happen to them.

11 Q. Got it.

12 What do you mean by you would put
13 stuff in it?

14 A. The die cut represents silicon
15 real estate. It also represented silicon
16 real estate that disappears at the end of the
17 process because you run the die over it.

18 But it represents useful real
19 estate and so people can put test structures
20 in there.

21 Q. To test future products?

22 A. To test the present product.

23 For example, let's say your TSMC
24 just for the moment and you build wafers for
25 sale for somebody and you've just run ten

1 wafers for customer so-and-so. Well,
2 customer so-and-so wants to know if those
3 wafers are good or not. And you have to
4 somehow test those wafers.

5 The moment you stick probe pads on
6 a wafer, that means you have to have a place
7 for those probe pads. And probe pads are
8 big. And so if you can put the probe pads
9 someplace else, that's kind of nice. And so
10 there is a sub-niche set of projects, which
11 is you put those test structures in the
12 scribe line where the dicing saw will go, and
13 there's a prober that goes in and tests these
14 structures in the scribe and they tell you if
15 the die is healthy via those test structures.

16 Now, they're not inside the die
17 themselves, so it's not like a product test
18 of the die. But let's say something bad
19 happened and the bottom half of the die
20 didn't get a shot map for some reason. Let's
21 pick something out of thin air.

22 Well, the probes that go down the
23 scribe line would immediately start to fail
24 in and the bad part of the wafer and that
25 would tell somebody something is wrong. And

1 the nice thing about this is doesn't use any
2 real estate that could go to product.

3 Scribe lines are pretty big
4 compared to product because the saw blade is
5 actually large compared to the size of a
6 transistor. And so you put all these nice
7 test structures in your scribe line and you
8 test them, and then you cut them out and
9 they're destroyed, and that has the
10 additional competitive advantage that all
11 your test results cannot be determined by
12 your competitors when they buy the products,
13 because you've got rid of the test
14 structures.

15 (Reporter clarification.)

16 BY MR. KENYON:

17 Q. And so even with these test
18 structures in the scribe lines, you would
19 still have separation between the different
20 devices that you have on the wafer, correct?

21 MR. CROSS: Objection to form.

22 A. So we're talking about die and
23 we're talking about the scribe lines between
24 die and we're talking about using those
25 scribe lines to cut out die.

1 Now, die themselves have other
2 structure inside. Are you talking about
3 die-to-die separation or are you talking
4 about stuff within the die itself?

5 BY MR. KENYON:

6 Q. Well, let's start with the
7 die-to-die separation.

8 A. And repeat your question?

9 Q. Okay. Is there any sort of
10 separation between die to die?

11 MR. CROSS: Objection to form.

12 A. There's the width of the scribe
13 line itself.

14 BY MR. KENYON:

15 Q. Okay. And then within the die
16 itself, is there any separation between each
17 of the structures?

18 A. So the outer perimeter of a die,
19 the very outer perimeter, not the devices
20 inside the die and not the memory and not the
21 sense amps and not the peripheral circuitry,
22 but the entire outside of the die typically
23 has a specialized structure sometimes called
24 a seal ring or an etch ring or something.

25 But the entire perimeter of the

1 die has a packaging-related sealing structure
2 that's kind of independent of everything that
3 goes on inside the die.

4 Q. Okay. And you mentioned the
5 memory inside the die.

6 Would there be separation between
7 the memory and other structures in the die?

8 A. Depends on the product
9 application. There are some types of
10 memories that put the memory array over the
11 peripheral circuits.

12 Q. But there are products in which
13 the memory has separation between itself and
14 other structures in the die?

15 MR. CROSS: Object to form.

16 A. So certainly, there exists
17 products where the memory is a block, and
18 there is block adjacent to it that something
19 else -- or could be another memory, it could
20 be a CPU, it could be something else, the
21 design of products uses, typically, blocks
22 of -- with different functionality.

23 And again, this is a very product
24 architecture thing, as I mentioned a minute
25 ago. There are products that pull out all

1 the peripheral circuitry underneath a memory
2 array. There's products that put the memory
3 array next to the peripheral circuitry.
4 There's products that have a memory array and
5 a CPU in the product. And so it goes.

6 BY MR. KENYON:

7 Q. Okay. Focusing on products that
8 are just the memory itself, so there's no CPU
9 as well, how would you go about -- what would
10 be the first step of fabricating that device
11 on the wafer?

12 MR. CROSS: Object to form.

13 A. So this, again, depends on the
14 specific fabrication process that's used.

15 As I mentioned, there are some
16 fabrication processes that put the circuitry
17 underneath the wafer, there are other
18 fabrication processes that put the circuitry
19 to the side, and so on and so forth.

20 At this point one thing that we
21 could do to help focus the conversation is, I
22 believe the -- the -- sorry, the '031 Patent
23 does show some of those underlying layers
24 with regards to steps prior to the memory
25 itself.

1 BY MR. KENYON:

2 Q. Okay. Well, I want to focus on
3 the fabrication of the memory itself, not the
4 underlying layers.

5 So what would be the first
6 fabrication step for the memory itself?

7 A. So now do we have a memory that
8 has the source underneath, or do we have a
9 memory that has the source on the top?

10 Q. Let's go with the source on the
11 top?

12 A. Okay. So then you're putting the
13 bit lines underneath?

14 Q. Well, what do you -- what would a
15 person of ordinary skill in the art
16 understand -- where would the -- where would
17 a person of ordinary skill in the art
18 understand the bit lines to go?

19 MR. CROSS: Object to form.

20 A. So that's going to sort of come
21 back to it depends on what architecture the
22 product is. There are products that have bit
23 lines underneath and there are products that
24 have bit lines on top.

25 And clearly, if you're going to be

1 fabricating a device with the bit lines
2 underneath, that's different than fabricating
3 a device with the bit lines on top.

4 BY MR. KENYON:

5 Q. Okay. So if the source is on the
6 top, where could you put the bit lines?

7 A. If the source is on the top, you
8 need to put the bit lines on the bottom
9 somewhere.

10 Q. Okay. And what would be the next
11 fabrication step after putting the bit lines
12 on the bottom?

13 A. Well, that's, again, going to
14 depend on the specific architecture. In
15 general, the bit lines are going to need to
16 connect to the channels. So you're going to
17 need to decide where the bit line is, where
18 the connection to the channel is, and where
19 the channels are.

20 Q. Okay. Maybe taking a step back.
21 Do we have a stack of alternating
22 layers fabricated yet?

23 A. So in a 3D -- oh, sorry. My bad.

24 MR. CROSS: Object to form.

25 A. So we have now moved from a

1 discussion of how we're building the device
2 with all the underlying material to a
3 discussion of the memory stack itself.

4 And the alternating layer business
5 is where the cells themselves would be
6 formed. The memory cells, the upper select
7 gates, the lower select gates, all of that is
8 this alternating stack thing.

9 BY MR. KENYON:

10 Q. And how would you form the
11 alternating stack?

12 A. This, again, depends on the
13 architecture of the memory. You have a
14 couple of choices. You can form the
15 alternating stack from insulators and
16 conductive layers.

17 So you have an insulating layer, a
18 polysilicon layer, an insulating layer, a
19 polysilicon layer, and so on all the way up.

20 You could form the stack from
21 alternating insulating and metal layers.
22 Insulating layer, metal, insulating layer,
23 metal, so on, and all the way up. It depends
24 on your architecture.

25 Q. Okay. Would each of these layers

1 span the entire wafer?

2 MR. CROSS: Object to form.

3 A. That has actually two answers
4 depending on the state of the process you're
5 at. We have to be a little careful here
6 whether you're describing the process as it
7 occurs or the final product.

8 Let me do --

9 BY MR. KENYON:

10 Q. The process as it -- go ahead.

11 A. Okay. Yeah, let me do a very
12 primitive example. Let's ignore all the
13 razzmatazz that's below the memory array and
14 let's come in and say we're going to an
15 insulator, a polysilicon layer, an insulator,
16 a polysilicon layer, and so on.

17 Those layers would likely be
18 deposited over the entire wafer and then
19 subsequently patterned. It's not the only
20 way to do it, but, in general, people put
21 those types of materials down in big sheets
22 and then pattern them later.

23 Q. Okay. And how would you deposit
24 each of the layers within that stack?

25 A. Again, this is an architectural

1 decision. There are an amazing number of
2 ways to do this. If you are, for example,
3 doing an insulator, metal, insulator, metal
4 stack, as an example, you might use a CVD
5 technique to do the insulator. You might, I
6 don't know, sputter or evaporate the metal.

7 There's lots of different ways to
8 do this.

9 Q. Okay. You had mentioned use a CVD
10 technique to do the insulator.

11 Is it any CVD technique?

12 A. There are a large variety of ways
13 to deposit insulators. Chemical vapor
14 deposition is one. You can actually sputter
15 insulators.

16 But there's a myriad of ways to do
17 this of, you know -- in my prior history, I
18 think I've used CVD, I've use HPCVD, LPCVD.

19 Since integrated circuits are
20 largely comprised of insulators and
21 conductors, you can imagine there's a large
22 number of ways to put both of these materials
23 down.

24 Q. Okay. I guess I was asking a
25 little bit of a different question. You had

1 mentioned a CVD technique.

2 And so I was wondering whether
3 there are more than one CVD techniques?

4 A. Yes. There is, you know, PECVD
5 and LPCVD and MOCVD and a whole acronym
6 forest of CVD techniques.

7 All CVD means is chemical vapor
8 deposition. And there's a myriad of ways to
9 do chemical vapor deposition.

10 Q. And the myriad of ways of doing
11 chemical vapor deposition can be used to
12 deposit the insulators within the stack?

13 MR. CROSS: Object to form.

14 A. So let me wind back the question a
15 bit so we're speaking the same thing.

16 We're talking about creating a
17 layered stack of oxide and conductors that
18 will eventually form a memory. And we're
19 talking about the various ways that one can
20 make those dielectrics. And I am laying CVD
21 on the table as one common way of depositing
22 a dielectric.

23 BY MR. KENYON:

24 Q. Correct.

25 A. Okay. So I may have lost the

1 question.

2 Do you want to re-ask the
3 question?

4 Q. Sure.

5 You had mentioned that there are a
6 myriad of CVD techniques, right?

7 A. Yes.

8 Q. Can you --

9 A. There's also non-CVD techniques.
10 I mean, you can do plasma enhanced CVD, you
11 can sputter, you can do ALD. There is --
12 there's a lot of different ways to deposit
13 materials.

14 Q. Okay. You just mentioned that
15 there are non-CVD techniques and then
16 mentioned plasma enhanced CVD.

17 Is plasma enhanced CVD not a CVD
18 technique?

19 A. So I apologize for misspeaking. I
20 perhaps should have said there's a variety of
21 suitable deposition methods, for example,
22 plasma enhanced CVD or sputtering or ALD.

23 I didn't mean to imply that PECVD
24 was not a CVD technique.

25 Q. Got it. Okay. So I kind of want

1 to get back to the fabrication process in
2 general. We're talking about a stack of
3 layers, dielectric and conductor layers, on
4 the wafer.

5 What's -- how would you -- what
6 would you do next in the fabrication process?

7 MR. CROSS: Object to form.

8 A. So again, that's an architectural
9 decision.

10 In general, if I am looking to
11 fabricate a 3D memory, and if we're more or
12 less after the step of doing the alternating
13 layers, there's a couple of different things
14 one could do: One could put the channels in;
15 one could put the staircase in; one could put
16 dummy structures in.

17 Again, the existence of multiple
18 layers does not constrain the architecture to
19 what happens next.

20 BY MR. KENYON:

21 Q. Okay. Why don't we go with
22 putting a staircase in.

23 How would you put a staircase in?

24 A. So putting a staircase in is,
25 again, perhaps not as easy as it sounds. And

1 the broad terms to put a staircase in -- and
2 let's agree for the moment what a staircase
3 is. A staircase is going to be a set of
4 steps where each step is a little bit shorter
5 in plan view than the adjacent step.

6 And I'm not trying to define the
7 term. I just want to make sure you and I
8 understand what we mean when we say
9 "staircase."

10 Is that what you mean or do you
11 mean something else?

12 Q. No, that -- we can go with that.

13 A. Okay. And perhaps maybe I should
14 make this simpler. I'm trying to avoid
15 accidentally defining staircase and causing
16 some long-term issues.

17 Can we just say it's kind of like
18 a staircase in a house and be good with that?

19 Q. Sure. That works.

20 A. Okay. So to make a staircase, you
21 have to make the risers just like in a house,
22 right. So you have to come and etch the
23 risers somehow. And there needs to be some
24 clever method that you etch the risers in the
25 staircase.

1 Q. Okay. And where would you form
2 the staircase?

3 MR. CROSS: Object to form.

4 A. You would form the staircase
5 wherever the architecture required it.

6 BY MR. KENYON:

7 Q. Where would a -- where could you
8 form a staircase?

9 MR. CROSS: Object to form.

10 A. So you could form a staircase on
11 any or all sides of your alternating layer
12 structure.

13 BY MR. KENYON:

14 Q. All four sides of the layer
15 structure?

16 A. You have an architectural choice.
17 You need the staircase to access what will
18 eventually be the gate lines to the
19 transistors, but it's an architectural choice
20 whether you have the staircase on one side,
21 two sides, three sides or four sides, or
22 whether you have the staircase partway on one
23 side or two or three or four.

24 Q. Okay. So why don't we stick with
25 one side of the stack. As I'm imagining this

1 memory device, I can kind of see in the z
2 direction the different layers of the stack
3 and the outline of the staircase. And in the
4 x direction, I can see the staircase
5 descending on the one side of the memory
6 device.

7 A. Okay. So --

8 Q. Where is the staircase --

9 A. Hang on.

10 Q. Go ahead.

11 A. Sorry. Why don't you ask your
12 question. I jumped in too soon.

13 Q. Where is the staircase located in
14 the y direction?

15 MR. CROSS: Object to form.

16 A. Can we -- we're starting to talk
17 about x and y. I would like to refer to a
18 drawing for x and y because at some point I'm
19 going to get them confused.

20 Do you have a sketch of your
21 alternating layer structure and where your
22 x's and y's are?

23 BY MR. KENYON:

24 Q. Sure. So why don't we go to
25 Paragraph 72 of your declaration.

1 A. All right. We -- I am on
2 Paragraph 72.

3 And we are probably going to be
4 discussing the illustration on Page 28 of the
5 '031 Patent?

6 Q. That's correct.

7 A. Sounds good. I have that up.

8 Q. Okay. So as I see in the y
9 direction, I can see the different layers
10 stacked on top of each other from the wafer
11 to the top of the device. And then in the x
12 direction, I can see the staircase descend.

13 Are you with me so far?

14 A. No. The z direction is vertical.
15 The x direction is to the right. I don't --
16 the y direction is in the page.

17 So I don't understand your comment
18 about the y direction.

19 Q. Well, I haven't mentioned the y
20 direction just yet.

21 A. Okay. So I must have missed --

22 MR. CROSS: Objection. For
23 clarification, I think you did start
24 the question discussing the y
25 direction.

1 MR. KENYON: Oh, I'm sorry. I
2 meant the z direction.

3 THE WITNESS: Okay. Why don't
4 we start the question all over.

5 MR. KENYON: Sure.

6 BY MR. KENYON:

7 Q. So looking at the figure on
8 Page 28, I can see in the z direction the
9 different layers stacked on top of each other
10 from the wafer to the top of the device. In
11 the x direction, I can see the staircase
12 descend away from the memory region.

13 Are you with me so far?

14 A. Yes, I am.

15 Q. Okay. And then, as you just
16 mentioned, the y direction goes through the
17 page?

18 A. That's correct.

19 Q. Where is the staircase located in
20 the y direction?

21 A. So we have an in general question
22 and we have a specific to '031 question.

23 Answering the in general question
24 first, the staircase is located wherever the
25 architecture required it. So, for example,

1 the staircase would -- could be located on
2 the right side as shown, on the left side as
3 shown, facing in to us as not shown, and
4 facing away from us as not shown. And it
5 could be other things too, but that is an
6 option.

7 And I used that option
8 specifically because it is my opinion that is
9 the option that is described in the '031
10 Patent with regards to their discussion in
11 relation to the x-y plane.

12 Q. Okay. So let's stick with the
13 general question for the moment.

14 If we're etching the staircase on
15 the right side of the stack, where is the
16 staircase located in the y direction in
17 relation to the stack?

18 MR. CROSS: Object to form.

19 A. So, again, this is an
20 architectural decision. If I rotate the
21 general case so that I'm facing the plan
22 view -- and I love using Mayan temple
23 pyramids as an example, by the way -- I could
24 etch stairs on each side and I could etch
25 stairs on the top and bottom so I could have

1 stairs on all sides.

2 And the stairs could be a segment
3 of the total side, they could extend the
4 entire length like a Mayan pyramid. But
5 you -- there's an architectural decision
6 could easily be made to have stairs on all
7 four sides.

8 BY MR. KENYON:

9 Q. Okay. And you had mentioned
10 extending the entire length.

11 What do you mean by that?

12 A. So when a -- it's always very
13 difficult to describe these structures using
14 only a cross-section. And so we use commonly
15 terminology like along the axis or in the
16 plane to try and differentiate between things
17 that are kind of linear and things that are,
18 you know, in two dimensions.

19 So in general, if I'm saying that
20 something is extending along the y-axis into
21 the page, I'm kind of talking about what's
22 happening along that single direction into
23 the page.

24 In contrast, if I'm talking about
25 something that's happening kind of in front

1 or behind me, I may be saying in the plane on
2 that -- of that feature, whatever it is.

3 So in this case what I'm saying is
4 that if one was flipping this and looking at
5 it in a planned view, you would be
6 potentially -- we're talking in the general
7 case -- you would be potentially extending
8 along the z-axis for one of your stairs; and
9 then in the back, along the negative x-axis
10 for a stair; then coming back along the
11 positive y-axis for a stair -- see if I got
12 this right -- and then coming across ways on
13 the positive x-axis for a stair.

14 Q. Okay. I think you --

15 A. I may have to do this again
16 because I think I may have screwed the
17 dimensions up.

18 Q. Maybe I missed the context that
19 you were providing. I thought -- or at least
20 I understood that what you were saying is
21 that the staircase would span the entire
22 length of the stack.

23 A. Not necessarily.

24 Q. So it could, though?

25 A. Again, this is an architectural

1 decision that's likely made for reasons
2 unrelated to the basic geometry.

3 For example, back to Mayan temple
4 pyramids for a moment, and, again, the human
5 example. People walk up to top of the Mayan
6 temple pyramid, they may not want to walk up
7 on the edges, and so the stairs may be
8 centered on the four sides.

9 I've certainly seen NAND
10 geometries where the stairs do not span an
11 entire side, they're a segment of the side.
12 So in this case and in a general case, we
13 could say, well, I have a Mayan temple
14 pyramid, I have staircases centered on the
15 plus and minus x-axis, and I have staircases
16 centered on the plus and minus y-axis, but it
17 doesn't necessarily extend all the way to the
18 edge.

19 Q. Okay. How would you pattern a
20 staircase that only spans a segment of the
21 memory device?

22 A. In your plan view design, there is
23 a box for your memory array and,
24 conceptually, a smaller box that's the active
25 part of the array.

1 And the mask for your etch is a
2 square box on all four sides of the array.
3 And then you pattern it and you do your
4 staircase etch using that box as a basis.

5 Q. And you would etch all the way
6 down to the substrate for those portions?

7 MR. CROSS: Object to form.

8 A. Okay. So again, this is an
9 architectural decision. And keep in mind,
10 staircase etches are a little more complex
11 than my simple example because I have to etch
12 a staircase, right?

13 So in the most primitive way, I
14 would need a mask to etch each stair. People
15 are smarter than that, and there's a variety
16 of more elegant techniques to etch every
17 stair that doesn't require having a hundred
18 masks if you have a hundred steps. Ignore
19 that for the moment.

20 Let's assume that we got plenty of
21 money and I have a mask to do each stair.
22 It's an architectural choice how far down I
23 go. For example, the bottom layer in my
24 multilayer stack may be an insulator and I
25 may elect to cut through it to the substrate.

1 I may elect to not cut through it to the
2 substrate. I may elect to leave buffer
3 layers at the bottom for one reason or
4 another. I may elect not to.

5 So these are architectural choices
6 that depend on the designer's goals.

7 BY MR. KENYON:

8 Q. Okay. Getting back to the
9 fabrication process, after you etch a
10 staircase, what's the next step?

11 MR. CROSS: Object to form.

12 A. So typically, after the staircase
13 is etched, there is some sort of a dielectric
14 fill process.

15 Now, there can be some order
16 reversals depending on the exact fabrication
17 sequence. But at some point or another, you
18 need to get contacts down to the staircase,
19 and the contacts need to be isolated in some
20 way.

21 And there's a variety of different
22 ways to do this, but in general, there's a
23 step to etch the staircase, and in general,
24 there's a step to fill, and then there's
25 subsequent patterning steps depending on what

1 people are trying to do.

2 BY MR. KENYON:

3 Q. What would the step to fill look
4 like?

5 MR. CROSS: Form.

6 A. I think the step to fill is
7 actually described -- or a typical step to
8 fill.

9 BY MR. KENYON:

10 Q. What are you looking at right now,
11 Dr. Kuhn?

12 A. I'm actually looking at my -- I'm
13 looking at the '872 Patent.

14 Q. Do you mean the '031?

15 A. I'm sorry. I'm looking --

16 Q. No worries. I know you're doing a
17 lot of these IPRs so it's fine.

18 So I'm actually trying to
19 understand what the fill step would look like
20 before July of 2018. So outside of the
21 context of the '031 Patent.

22 A. Okay. So if I -- if there is
23 generally a -- okay. So -- and why don't you
24 ask the question again. Because there's so
25 many different ways to answer it, I almost

1 don't know where to start.

2 Q. Before July 2018, what would the
3 step to fill look like?

4 MR. CROSS: Object to form.

5 A. Yeah, I don't know how to answer
6 that because there are so many different
7 technologies.

8 Do you have a specific example in
9 mind?

10 BY MR. KENYON:

11 Q. What examples come to mind for
12 you?

13 A. When you asked the question, every
14 possible way to fill a structure jumped into
15 my head, which wasn't helpful. Filling is a
16 very common thing in semiconductors.

17 Q. And you would be filling
18 dielectric material; is that right?

19 A. It depends on the architecture.
20 You typically do not want to fill a conductor
21 next to a staircase. But dielectric
22 materials are not your only choice.

23 Q. Okay. Maybe taking a step back.
24 What is the purpose of the fill
25 step?

1 MR. CROSS: Object to form.

2 A. Again, this depends on the
3 architecture.

4 Do you mean the purpose of the
5 fill step in general? Or the purpose of the
6 fill step in the '872 example -- or, sorry,
7 the '031 example?

8 BY MR. KENYON:

9 Q. So, in general, you had mentioned
10 earlier that you would etch a staircase and
11 then you would perform a step of filling or a
12 step to fill.

13 What is the purpose of that step?

14 A. So you typically want to be able
15 to create an isolation region so that the
16 staircases don't short against each other.
17 And then you want to be able to do subsequent
18 processing on that isolation region, for
19 example, for the staircase contacts.

20 Q. Why would the staircase -- or what
21 do you mean by the staircases don't short
22 against each other?

23 A. So each of the conductive lines in
24 the staircase -- now we've defined the
25 staircase as being created by a multiplicity

1 of layers. Each -- and the multiplicity of
2 layers are conductive lines separated by
3 isolating lines.

4 Each of those conductive lines
5 eventually ends up at a gate of a transistor.
6 And so ultimately, all those conductive lines
7 need to have a contact somewhere on the
8 product. And you don't want all the gate
9 lines shorted together or all your
10 transistors gates will be shorted together
11 and your product won't work.

12 Q. So if the gates are not isolated,
13 your product wouldn't work or might not work?

14 A. Let me put this the other way
15 around. If you short all your gates
16 together, your product will not work.

17 Q. Okay. And one way of performing
18 the step to fill is to fill the area with
19 dielectric material?

20 MR. CROSS: Object to form.

21 A. You can fill a layer -- one option
22 is to put a dielectric material in there.

23 BY MR. KENYON:

24 Q. And what would that process look
25 like?

1 MR. CROSS: Object to form.

2 A. That -- again, filling structures
3 with dielectric material is the mainstay of
4 the semiconductor industry. You have a lot
5 of choices. We've already talked about CVD
6 and its variants, and sputtering and its
7 variants, ALD and their variants. Filling
8 holes with a dielectric -- you could spin on
9 dielectrics, they're a liquid, and have them
10 dry, by the way.

11 There's a myriad of options
12 because it's a very baseline foundational
13 technology in the industry.

14 BY MR. KENYON:

15 Q. Okay. You mentioned at the
16 beginning of your answer, filling structures.

17 Do you mean isolation structures?

18 A. You know, I don't recall exactly
19 the terminology I used. It's possible I
20 misspoke. I may have meant filling
21 techniques because I recognized your question
22 as trying to describe all the ways you can
23 fill a hole with an insulator in the
24 industry.

25 And there's a lot of them. And I

1 ran through a couple that I was aware of, you
2 know, the CVD techniques, the sputtering
3 techniques, the various atomic layer
4 techniques, spin-on techniques where you put
5 a liquid on and it dries.

6 My intent was to list a series of
7 techniques because I believed that was the
8 tone of your question.

9 Q. Okay. Why don't we focus on CVD.

10 A. Okay.

11 Q. Can you walk me through the
12 process of filling the hole with CVD or using
13 the CVD process?

14 A. And which CVD did you have in
15 mind: MOCVD, LPCVD, HPCVD? What CVD is the
16 one you had in mind?

17 Q. What type of CVD would you use
18 typically before July 2018 to fill in a hole
19 to isolate the staircase structure?

20 MR. CROSS: Object to form.

21 A. So assuming I want to fill the
22 hole with a CVD process and assuming I want
23 to use -- and I'm going to restrict ourselves
24 to the moment to materials filling rather
25 than all the other ways you can fill just to

1 focus on that technique.

2 You would -- you could fill with a
3 CVD technique that put in a conformal film or
4 you could fill with a CVD technique that has
5 an intrinsic etch sputter capability, which
6 is much less conformal.

7 Those are the kind of two broad
8 classes. There's many ways to do it within
9 those classes, but in the creation of, for
10 example, a silicon dioxide fill, there's
11 usually some tension between conformality of
12 the fill and the ability to fill in a smooth
13 fashion.

14 And so on one side are the
15 techniques that don't have intrinsic etches
16 and the other side are the ones that do.

17 BY MR. KENYON:

18 Q. And what would the process look
19 like for conformal CVD?

20 A. So you would -- as one of several
21 examples, you would be using a CVD technique
22 and depositing a relatively thick film would
23 be one option. Another option would be
24 deposit a thinner film and do multiple
25 layers. You know, again, this is a

1 foundational technology.

2 But a conformal CVD film, you make
3 a dep and the dep is generally pretty thick
4 because it's like snow. It would lay over
5 the surface. Conformal means that it's the
6 same thickness no matter what it's doing, so
7 it lays over the surface like a blanket.

8 Q. And would the film form on the
9 entire wafer?

10 MR. CROSS: Object to form.

11 A. Well, in general, a CVD process is
12 done over the entire wafer surface, but
13 the -- if there's holes and valleys that will
14 go up over the val- -- I'm sorry, up over the
15 hills and down into the valleys, if you're
16 asking whether it covers -- whether it's
17 indirect contact with the substrate, not
18 necessarily.

19 Again, the best analogy is to a
20 blanket of snow. It's going to lie down over
21 the top of the structure that's preexisting.

22 BY MR. KENYON:

23 Q. And so it will cover any holes?

24 MR. CROSS: Object to form.

25 A. No. It's like a blanket of snow.

1 If you don't live in snow country, this may
2 be a bad analogy.

3 BY MR. KENYON:

4 Q. I live in Texas, so not really.

5 A. You live in Texas, okay. So let
6 me try another analogy.

7 Q. No, we can stick with snow, that's
8 fine --

9 (Reporter clarification.)

10 A. Let me try a more Texas analogy.
11 It's like thick grass over a field. It
12 follows the contours of the field. You know,
13 let's assume I could magic -- I'm Gandalf and
14 I could magically grow a thick layer of
15 grass, right?

16 So I'm sitting here on a golf
17 course and I wave my magic wand and I
18 conformly grow grass. It follows the
19 contours of the golf course. It doesn't fill
20 the holes. It follows the contours.

21 BY MR. KENYON:

22 Q. Okay. If it's following the
23 contours, would it necessarily fill in the
24 holes --

25 MR. CROSS: Object to form.

1 BY MR. KENYON:

2 Q. -- depending on --

3 A. No. And I need to be careful with
4 the word "necessarily" because I realize it
5 has a legal meaning that I'm not a lawyer
6 that I may be messing up on.

7 But it's a conformal film. It
8 will lay as a blanket. In some locations, if
9 the hole is of a suitable geometry, the
10 blanket will pinch on the top. And here's
11 where my glass analogy falls apart because
12 grass doesn't do this.

13 So if I have a big great hole, the
14 blanket comes over and follows the terrain
15 like grass. If I have a little tiny hole,
16 the blanket will come over and it won't work,
17 and I'll seal off and I'll get a -- an air
18 gap.

19 And so this is a size-dependent
20 thing, it's also a process-dependent thing,
21 and flow rates, and I am not a CVD expert.
22 But if you had one, they would give you a
23 long discussion on how you can control the
24 size of this void by exactly the parameters.

25 But it's a conformal deposition,

1 and under certain circumstances, you can make
2 a neat little void or an air gap.

3 Q. Using conformal CVD to fill --
4 strike that.

5 Using conformal CVD to deposit
6 dielectric material on a staircase structure
7 would create air gaps?

8 MR. CROSS: Object to form.

9 A. So if I use CVD and if I deposit a
10 CVD -- and I'm going to limit this to silicon
11 dioxide -- on a structure with staircases,
12 for example, all four sides, I will get a
13 conformal deposition unless I'm using a
14 special kind of CVD.

15 But let's just say it's a plain
16 and ordinary conformal CVD. I'll get a
17 thicker layer on the top that will -- the
18 same thickness will go down the sides, it
19 will go along whatever's next to it, it will
20 go whatever. It's a conformal deposition.

21 Now, if my staircase is teeny
22 tiny, just let us speculate on a teeny tiny
23 staircase, it may be that the deposition
24 cannot lay conformly down in the space and it
25 will pinch off and make an air gap.

1 And this is a geometry-dependent
2 thing. You can make of air gaps
3 intentionally. People are actually quite
4 good at this. You can make air gaps
5 accidentally. When you make air gaps
6 accidentally, they're usually called "voids."
7 When you make them intentionally, they're
8 usually called "air gaps."

9 BY MR. KENYON:

10 Q. And you mentioned teeny tiny
11 staircase.

12 Is that commonly used in -- before
13 July 2018?

14 MR. CROSS: Object to form.

15 A. So I perhaps was less technically
16 accurate with teeny tiny staircase than I
17 should have been.

18 Let me simplify this to pull the
19 staircase out for the moment and just talk
20 about holes, ignoring staircases for a
21 second, and just talk, for example, a line of
22 holes.

23 And so if I had a -- and we'll do
24 a -- do not really a hypothetical, but an
25 illustrative example. If I had a wafer with

1 holes of the same depth but different sizes,
2 so I had great big holes and smaller holes
3 and very small holes and nanometer size
4 holes, and if I did a conformal CVD
5 deposition over this wafer, which just has
6 holes in it now. In some cases, the
7 deposition will work its way down into the
8 hole and come back out leaving this -- and it
9 kind of looks like an upside down pillow.
10 There's still a hole but it's got some weird
11 ripples on the side.

12 And then as the holes got smaller,
13 all of a sudden I would be making a void in
14 the hole. And the hole would be -- from the
15 top, it would seem to be filled, but inside
16 would be a little void or a little air gap.

17 And the various dimensions here of
18 the holes and the various parameters of the
19 CVD can be altered so that, you know, certain
20 types of holes will always have the conformal
21 deposition and other types of holes will seal
22 over. And that's just an optimization thing
23 based upon the skill of the CVD module
24 expert.

25

1 BY MR. KENYON:

2 Q. Do voids cause issues?

3 A. It depends on whether you put them
4 in there intentionally or not. The
5 intentional use of voids as air gaps is well
6 established in the industry becoming
7 increasingly more well established.

8 They -- a happenstance where voids
9 become a yield issue is also a possibility.
10 As I mentioned earlier, if you put a void in
11 by accident and it causes a yield issue, you
12 could call it a void. If you put it on
13 purpose and it has a function in your
14 product, you call it an air gap.

15 Q. And when using -- strike that.

16 When creating an air gap, would
17 the memory device be exposed to the air?

18 MR. CROSS: Object to form.

19 A. This depends on the exact
20 processing. Air gap is a generic term used
21 to say that there's not a material in it.
22 You know, an air gap could have an inert gas
23 in it, nitrogen. Air gap could have vacuum
24 in it. An air gap could have air in it.

25 There's a number of process

1 options available for how to seal the air
2 gaps. Air gaps are often sealed at both
3 ends, and so, you know, the easiest way to do
4 it is just put nitrogen in the air gap as you
5 build it. But there's obviously many other
6 ways to do this.

7 BY MR. KENYON:

8 Q. When creating an air gap, would
9 the memory device be exposed?

10 A. Depends on how you create it.
11 Depends on what you're doing. It's -- again,
12 we're off into the intricacies of
13 architectural decisions.

14 Q. But issues would exist if it's
15 exposed?

16 A. So this is getting very
17 hypothetical. What is exposed? Is the
18 staircase exposed? Is the channel exposed?
19 Is the bit line exposed?

20 When you asked the question, you
21 said is the memory exposed. The memory has
22 got a lot of stuff in it.

23 Q. Why don't we go with the staircase
24 for now?

25 A. Okay.

1 MR. CROSS: Object to form.

2 A. And why don't you reprise the
3 question with staircase.

4 BY MR. KENYON:

5 Q. Well, why don't -- why don't we
6 take a step back.

7 Would you create an air gap to
8 isolate a staircase?

9 A. In general, I would create an air
10 gap to isolate objects from other objects.
11 And the reason I'm being a little more
12 precise is that the staircase involves a lot
13 of components. It's the staircase -- it's
14 elements in the staircase for the contacts,
15 dummy contacts, and so on and so forth. But
16 the use of an air gap to isolate object X
17 from object Y is certainly done in the art.

18 Q. Okay. I have a few more
19 questions, but why don't we -- it's been
20 about an hour.

21 Do you want to take a break now or
22 do you want to keep going?

23 A. I would like it take a break. I'm
24 a little cold.

25 (A brief recess was held from

1 1:08 p.m. to 1:19 p.m.)

2 BY MR. KENYON:

3 Q. Welcome back, Dr. Kuhn.

4 A. Good to see you again.

5 Q. So before the break, you mentioned
6 that a staircase involves a lot of
7 components.

8 Do you remember that?

9 A. Yes, I do.

10 Q. What components are you referring
11 to?

12 A. Well, the staircase has the
13 alternating layers of conductive and
14 nonconductive material.

15 The staircase may have intervening
16 layers that are thicker for purposes of --
17 various architectural purposes. The
18 staircase also must have some sort of contact
19 to the conductive layer of the alternating
20 layers because that's the function of the
21 staircase is to allow that contact.

22 The staircase may also have other
23 structures. It may have vias. It may have
24 support pillars. It may have the various
25 isolation structures. In addition to its

1 simple function of providing a staircase to
2 land a staircase contact, it often has a
3 number of other elements in it as well.

4 Q. Okay. Prior to -- well, strike
5 that.

6 I want to talk about the etching
7 of the alternating layers specifically.

8 A. Okay.

9 Q. You would etch the alternating
10 layers into a share -- staircase form before
11 creating any conductive vias, support
12 pillars, or any other components that you
13 mentioned, correct?

14 A. In general, yes.

15 Q. Okay. Directly after etching the
16 alternating layers into a staircase form,
17 what would -- would the next step be
18 isolating those layers?

19 A. Well, that depends on the process.
20 Sooner or later, you need to put a staircase
21 contact on those staircases. And sooner or
22 later, you need to decide how you are going
23 to keep those staircase contacts from
24 shorting each other. But the process may go
25 off and do other things after the staircase

1 etch.

2 Q. Before creating the context, would
3 you perform a fill step?

4 A. You certainly could perform a fill
5 step of some type.

6 Q. And one method of performing that
7 fill step is depositing dielectric material,
8 right?

9 A. Yes, one option to fill the area
10 near the staircase would be to put in a
11 dielectric filling material, that's correct.

12 Q. And the purpose of the fill step
13 is to isolate the alternating layers of the
14 staircase?

15 MR. CROSS: Object to form.

16 A. That is one of several purposes.
17 As I mentioned before, it's
18 generally bad if you short all your gates
19 against each other. But the isolating fill
20 may serve additional purposes depending on
21 the architecture.

22 BY MR. KENYON:

23 Q. What other purposes?

24 MR. CROSS: Object to form.

25 A. It depends on the architecture.

1 BY MR. KENYON:

2 Q. How so?

3 A. If you have an architecture where
4 you have peripheral circuitry under the array
5 and potentially under the staircase, you may
6 end up wishing to drill vias into the
7 staircase region to access that circuitry, in
8 which case you would have an additional
9 benefit of having those vias go through that
10 filling material and either providing a
11 structural support for drilling those vias or
12 providing isolation support.

13 Again, it's -- it depends on
14 exactly your architecture and what you have
15 in the staircase region in addition to
16 staircase contacts.

17 Q. Okay. Instead of depositing a
18 dielectric material, what other methods exist
19 to isolate the alternating layers in
20 staircase form?

21 MR. CROSS: Object to form.

22 A. So if we're talking about just the
23 staircase, not necessarily other parts of the
24 device, but just the steps themselves, so all
25 I'm talking about -- I'm not talking about

1 edges or corners or the sides or trenches or
2 anything like that, I'm talking about just
3 the risers on the staircase.

4 And, of course, in context here,
5 the risers on the staircase could be in a
6 very small region of the total staircase
7 area. So I'm just talking about the risers.

8 In general, you would have to have
9 some sort of insulating material on those
10 risers. There may be options that you might
11 be able to get away without it, but it would
12 generally be the case there would be some
13 sort of insulator there.

14 BY MR. KENYON:

15 Q. And you mentioned edges or corners
16 or the sides.

17 What do you mean by "edges"?

18 A. So when we had -- I'm
19 distinguishing the staircase -- so I'm
20 distinguishing the staircase itself with the
21 risers from regions in the part that may be
22 adjacent to the staircase that are facing in
23 a different direction.

24 Because I'm trying to distinguish
25 between, for example, if I have a staircase

1 and I elect to cut a trench through center of
2 that staircase, just as a what if, I have the
3 section with the risers, and I have a section
4 that now has a trench in it, and I may elect
5 to do two different things in the isolation
6 of those two items.

7 Q. What are the two different things?

8 A. I may elect to use a solid fill
9 material or I may elect to use some sort of
10 an air gap.

11 Q. And is the solid film material --
12 strike that.

13 When referring to a solid fill
14 material, are you talking about depositing a
15 material like a dielectric material?

16 A. So I'm referring to depositing a
17 nonconductive material.

18 Q. Okay. And when you said elect to
19 use some sort of an air gap, what are you
20 referring to?

21 A. When I'm saying air gap and when
22 I'm using the air gap technology in my --
23 both in my declaration and in this
24 deposition, I'm referring to a hole or void
25 or a gap where the primary isolation is not a

1 material.

2 It's vacuum or nitrogen or air, as
3 opposed to silicon dioxide or silicon nitride
4 or something of that nature. I'm
5 distinguishing between a gas or a vacuum from
6 a more solid material.

7 Q. What do you mean by the primary
8 isolation is not a material?

9 A. So if I have two -- let me make
10 this easy.

11 If I have two electrical boxes and
12 I have a positive voltage on one box and a
13 negative voltage on the other box, and if I
14 cut a trench between these two boxes, if I
15 place an air gap in that trench for
16 electrical isolation -- I'm going to have a
17 few other things in the trench. There's
18 going to be the seal at the top of the air
19 gap. There may be some residual material on
20 the side. But mostly, what's isolating my
21 side A from shorting to my side B is the
22 presence of the air gap.

23 Q. And when you say some residual
24 material on the side, what do you mean?

25 A. It may not be economically

1 feasible to clean out every little piece of
2 material on the side of an air gap. And so
3 the air gap itself may have some residual
4 material from fabrication, but the majority
5 of the isolation function is performed by the
6 gap, not by that material.

7 And this is just intended to be
8 specific to air gaps.

9 Q. And you would form air gaps in
10 trenches?

11 A. You certainly can form air gaps in
12 trenches, that's correct.

13 Q. Where else can you form air gaps?

14 A. Well, I would have to look into
15 that.

16 My experience has largely been air
17 gaps in trenches, but the technology has been
18 expanding rapidly in the past five to ten
19 years, and I have no good visibility today as
20 to the breadth of where people can put air
21 gaps.

22 Q. Speaking -- strike that.

23 Before July 2018, where else could
24 you put air gaps?

25 A. So you could put air gaps in any

1 place that you could reasonably expect to
2 fabricate those successfully.

3 Q. Before 20- -- strike that.

4 Before July 2018, where could
5 someone reasonably expect to fabricate
6 successfully air gaps?

7 A. Certainly before July 2018 there
8 was technology in place to fabricate air gaps
9 in trenches because people were using that
10 actively in products.

11 I don't have good visibility. I
12 haven't studied this. I haven't thought much
13 about this. I haven't seen the breadth of
14 what else people were doing prior to 2018.

15 I have personal experience with
16 people putting them in the back end of the
17 line as interconnect spacings, and I've seen
18 some efforts putting them in the front end of
19 the line for spacers and for other uses, but
20 I don't have broad visibility to the breadth
21 of air gap technology prior to 2018.

22 Q. You said "technology in place."

23 What did you mean by that?

24 A. Can you tell me the sentence back
25 and I'll explain it?

1 Q. Sure. You said: There was
2 technology in place to fabricate air gaps in
3 trenches because people were using that
4 actively in products.

5 What did you mean by technology in
6 place?

7 A. When I said technology in place, I
8 meant that people knew how to do this, that
9 it was not limited just to a student in a
10 laboratory, but that people were doing
11 this -- at least assessing it for
12 manufacturing.

13 Q. Okay. And before July 2018 --
14 strike that.

15 You then said: I have personal
16 experience with people putting them in the
17 back end of the line as interconnect
18 spacings.

19 A. That's correct.

20 Q. What do you mean by: Personal
21 experience with people putting them in the
22 back end of the line as interconnect spaces?

23 A. In the year or two before I
24 retired from Intel, there was significant
25 effort going on for replacing higher level

1 layers of ILD in the back end with air gaps.
2 And there's a huge competitive advantage to
3 be obtained by doing so. The back end of the
4 line is half the capacitance of a product.

5 Now, at that time I did not have
6 good visibility to which products were
7 running this, nor do I have good visibility
8 to Intel's product stream prior to 2014
9 because I retired in 2014.

10 But certainly the work I saw prior
11 to 2014 was not whether or not you could do
12 this, and it's not whether or not you could
13 do this on multiple layers, it was, you know,
14 how manufacturing compatible is this, how
15 many layers should we do this on, do we want
16 to do this on products, do we not want to do
17 this on products. You know, the technology
18 was at an advanced stage.

19 I don't have good visibility today
20 as to air gap usage in Intel's product streams
21 simply because I've been retired from the
22 company.

23 Q. Apart from using air gaps in
24 trenches, are you aware of any common use of
25 air gaps --

1 A. You mean --

2 Q. -- in the fabrication of 3D NAND
3 memory devices?

4 A. Well, one of your own references
5 does have an air gap in it, one of your prior
6 art references.

7 Q. What reference are you referring
8 to?

9 A. Well, let me see if I can figure
10 that out.

11 Your reference -- I have it as
12 Exhibit 1015. The patent number is -- ends
13 in '725. And the patent shows an air gap in
14 a 3D NAND device. It's shown expressly in
15 Figure 2T of the patent.

16 This is a patent you cited for
17 something else. And I noticed that there was
18 an air gap in it when I was reviewing it for
19 its original function.

20 Q. And you are referring to what's
21 labeled in Figure 2T as 228C?

22 A. That's correct.

23 Q. Okay.

24 A. And if you --

25 MR. CROSS: For clarification,

1 can you please upload the exhibit?

2 MR. KENYON: Sure.

3 MR. CROSS: Thanks.

4 MR. KENYON: I've added to the
5 chat Exhibit 1015, which is U.S.
6 Patent Number 11,244,725.

7 BY MR. KENYON:

8 Q. Do you recognize that document?

9 A. Let me look. That's it.

10 And I particularly --

11 Q. And --

12 A. Oh, I'm sorry, you go. I didn't
13 know if we were in a question or not.

14 Q. Go ahead.

15 A. I particularly draw your attention
16 to Column 10, Lines, oh, 57 to 60, which
17 describe the gate-slit openings being left as
18 an air gap.

19 Q. And where is the air gap located
20 in Figure 2T?

21 A. I suspect you don't mean on the
22 right side of the image. Do you mean in plan
23 view? It seems to be located in the gate
24 slit, the gate line slit.

25 Q. What is the gate line slit?

1 A. These are -- I could describe them
2 as trenches that run in this case in the --
3 in and out of the page direction.

4 Q. Okay. We can put that exhibit to
5 the side.

6 Earlier you said that you -- there
7 was significant effort going on for replacing
8 high level layers of -- the transcript says
9 ILD in the back end with air gaps.

10 Do you remember that?

11 A. Yes, I do.

12 Q. What do you mean by "significant
13 effort"?

14 A. Putting this in context, the back
15 end of the line, as I said, is half the
16 capacitance load of a product. The
17 capacitance in the back end of the line is
18 largely driven by the capacitance from metal
19 lines to each other, either adjacent or above
20 and below metal lines.

21 Historically, ILD, which stands
22 for interlayer dielectric, is used to
23 separate those metal lines. Interlayer
24 dielectrics, you probably heard people talk
25 about low-k technologies or low-k back ends

1 or low-k dielectrics. There's an effort to
2 drop the dielectric constant of those layers
3 as low as possible.

4 The problem is, is that there's a
5 bottom to this that's about 1.4 that's very
6 hard to get below for relative dielectric
7 constant. Air or nitrogen or vacuum or
8 whatever is around 1.

9 And so there has been a
10 longstanding effort to try and replace the
11 ILD with some sort of an air gap to be able
12 to get what would effectively be an enormous
13 improvement in the capacitance.

14 Q. And by effort, you mean research
15 efforts?

16 A. No, I mean development efforts.
17 And again, I don't have good visibility to
18 the product line. I am reluctant to say that
19 I know that Intel is selling air gaps in
20 products. I can't say that. I don't have
21 that knowledge in hand.

22 I would not be surprised based
23 upon the research and development activities
24 that were in place when I left Intel.

25 Q. Surprised that -- what do you mean

1 by surprised?

2 A. I would not be surprised if you
3 cut apart an Intel microprocessor today and
4 found air gaps in the back end of the line.

5 Q. Okay. Going back to the
6 components that you listed for the staircase,
7 you mentioned support pillars.

8 Do you remember that?

9 A. I do. I did, that's correct.

10 Q. What are "support pillars"?
11 And what are you looking for right
12 now?

13 A. Well, I'm doing two things. My
14 computer just crashed and I lost my patent.
15 So I am rebooting my screen to find my
16 patent.

17 And the second thing is I'm
18 reminding myself of this patent with regards
19 to support pillar.

20 Q. Okay.

21 A. Keep in mind that I'm having
22 multiple IPRs running at the same time and I
23 want to make sure I'm not misspeaking between
24 the various IPRs that are active.

25 Q. I understand. I'm actually asking

1 about outside of the context of the patent.

2 Before July 2018, what would you
3 have understood "support pillars" to be?

4 A. So I would understand a support
5 pillar to be a pillar that provides some sort
6 of mechanical support.

7 Q. And where would these pillars be
8 located?

9 MR. CROSS: Object to form.

10 A. So in answering the general
11 question, you'd locate the pillars anywhere
12 you needed support.

13 BY MR. KENYON:

14 Q. Could you locate the pillars in
15 the staircase region?

16 A. Well, certainly the '031 Patent is
17 doing so. It is --

18 Q. I'm --

19 A. -- discussing the use of the
20 support pillars in that region.

21 Q. So again, I'm trying to just
22 generally discuss support pillars outside the
23 context of the '031 Patent as to what a
24 person of ordinary skill in the art would
25 have understood support pillars to be before

1 July 2018?

2 A. So in general, not related to NAND
3 or staircases or anything of that nature?
4 Just in general.

5 Q. Sorry. Support pillars related to
6 3D NAND.

7 A. Okay.

8 MR. CROSS: Object to form.

9 A. Yeah.

10 BY MR. KENYON:

11 Q. Before July 2018, what would a
12 person of ordinary skill in the art
13 understand support pillars to be?

14 A. So at a general level, if someone
15 is saying support pillar without context, in
16 other words, what is the support pillar for,
17 it's understood to be a pillar with a certain
18 mechanical properties.

19 But keep in mind that in my own
20 experience, there are multiple broad uses for
21 the support pillars and they stem from
22 different root causes.

23 As a specific example, one very
24 common use of support pillars across all
25 product technologies is related to packaging

1 stress. When you take a die and put it in a
2 package, whether right side up or upside
3 down, you are subjecting that die to enormous
4 stresses and you can destroy, squish, more
5 simply, parts of the product.

6 And so there's a whole science of
7 support pillars that are related to the
8 packaging business or the packaging -- I
9 don't want to say business -- the packaging
10 step of the process.

11 There are also support pillars in
12 the 3D NAND world that are not packaging
13 related but are related to the nature of the
14 staircase architecture with certain kinds of
15 processing.

16 There's also support pillars that
17 are related to the edge of the
18 wafer -- sorry, the edge of the die. My
19 mistake. And we talked a little bit about
20 the stresses of die cutting, but we didn't go
21 very deeply into it.

22 So there's at least three ways you
23 can use a support pillar to deal with some
24 sort of mechanical stress in the part.

25 Q. Okay. I want to focus on the

1 second -- what did you call it -- reason. So
2 you mentioned support pillars in the 3D NAND
3 world that are not packaging related, but are
4 related to the nature of the staircase
5 architecture with certain kinds of
6 processing.

7 A. Yes, I said that.

8 Q. Before July 2018, would a person
9 of ordinary skill in the art have used
10 support pillars in the 3D NAND world related
11 to the nature of the staircase architecture?

12 MR. CROSS: Object to form.

13 A. Yeah, I'm not sure I can answer
14 that here because that would require me
15 looking extensively through the art just on
16 the topic of support pillars alone, and I
17 have not done that exercise.

18 BY MR. KENYON:

19 Q. You're not aware of using support
20 pillars in the staircase region of a 3D NAND
21 memory before July 2018?

22 MR. CROSS: Object to form.

23 A. It's a little more complicated
24 than that. Right here this second, I can't
25 sit down and list the patents that may talk

1 to support structures and their prior art
2 patents that may talk to support structures.
3 I just haven't done that study.

4 I certainly could do that study,
5 but I haven't been asked to do an extensive
6 study of the use of support pillars prior to
7 2018. I just don't have that information off
8 the top of my head.

9 BY MR. KENYON:

10 Q. Okay. Why don't we look at the
11 '031 Patent. I'm going to share it in the
12 chat.

13 So I've shared in the chat what's
14 been marked Exhibit 1001, which bears U.S.
15 Patent Number 10,868,031.

16 Do you recognize that document as
17 the patent at issue in this proceeding?

18 A. Let me take a look.

19 Yes, that's the patent at issue.

20 Q. I want to direct your attention to
21 Column 1, Lines 34 through 38.

22 And actually, before you read
23 those lines, Lines 34 through 38 are in the
24 background section of the '031 Patent; is
25 that right?

1 A. Okay. So I have '031 open. I
2 have Column 1 on the screen. I am looking at
3 Lines 33 to 37, give or take, and they are at
4 the end of the background session.

5 Q. Okay. And the '031 Patent says:
6 To form this multiple-stack memory device,
7 supporting pillars are used in the
8 fabrication process to provide mechanical
9 support and prevent pattern collapse.

10 Do you see that?

11 A. I do see that.

12 Q. Before July 2018, support pillars
13 were used in the fabrication process of
14 multiple-stack memory devices?

15 A. So the '031 Patent certainly has
16 the sentence in the background section that:
17 To form this multiple-stack memory device,
18 supporting pillars are used in the
19 fabrication process to provide mechanical
20 support and prevent pattern collapse.

21 That's correct.

22 Q. Are you a person of ordinary skill
23 in the art?

24 A. By both of the definitions given,
25 mine and Dr. Banerjee's, yes.

1 Q. Before July 2018, would a person
2 of ordinary skill in the art understand that
3 supporting pillars are used in the
4 fabrication process to provide mechanical
5 support and prevent pattern collapse?

6 A. So assuming information in the
7 background is accurately reflecting the prior
8 art, a POSITA in possession of this patent
9 would make that conclusion.

10 Q. Are you saying as a person of
11 ordinary skill in the art, you can't make
12 that determination without caveating that
13 that's what the '031 Patent says?

14 MR. CROSS: Object to form.

15 A. That was a very complicated
16 question. Let me back up a step.

17 Semiconductor history is
18 complicated. And the last handful of
19 questions you have been asking me specific
20 dates and specific times when people knew
21 specific things. And we've also had a
22 differentiation between whether they were
23 known in research and whether they were known
24 in manufacturing. And there is a difference.

25 So I have no problem at all saying

1 that the last three sentences or two
2 sentences of the background section indicate
3 that the '031 Patent establishes that these
4 things were used as prior art. That's a
5 little bit different than an entire study of
6 the art of supporting pillars.

7 BY MR. KENYON:

8 Q. So you made the distinction
9 between something that is known in research
10 versus known in manufacturing?

11 A. Well, technically, I think you did
12 earlier when we were talking about back end
13 of the line air gaps. You made that
14 distinction.

15 Q. Just reading a portion of your
16 answer, you stated that there is -- we also
17 have a differentiation whether they were
18 known in research and whether they were known
19 in manufacturing.

20 A. Yes, that's what I said. Because,
21 again, looking through a study of the past
22 work on supporting pillars is going to
23 require looking at the breadth of that
24 material.

25 Q. Sitting here today, you cannot

1 tell me one way or another whether supporting
2 pillars are used in the fabrication process
3 to provide mechanical support and prevent
4 pattern collapse of multiple stack memory
5 devices?

6 MR. CROSS: Object to form.

7 A. Well, of course, we can't. We're
8 talking about --

9 (Reporter clarification.)

10 BY MR. KENYON:

11 Q. Sitting here today, you cannot
12 tell me one way or another whether supporting
13 pillars are used in the fabrication process
14 to provide mechanical support and prevent
15 pattern collapse of multiple-stack memory
16 devices?

17 MR. CROSS: Object to form.

18 A. And my answer is: Yes, sitting
19 here today, supporting pillars are clearly
20 used to provide mechanical support for
21 pattern collapse in 3D memory. That's what
22 the '031 Patent is about.

23 BY MR. KENYON:

24 Q. Okay. I'm referring to before
25 July 2018.

1 A. Well --

2 MR. CROSS: Object to form.

3 BY MR. KENYON:

4 Q. Do you want me to read the
5 question again?

6 A. Yeah. The question initially did
7 not have before July 2018 in it, so...

8 Q. Sure. Let me add that.

9 Sitting here today, you cannot
10 tell me one way or another whether supporting
11 pillars were used before July 2018 in the
12 fabrication process to provide mechanical
13 support and prevent pattern collapse of
14 multiple-stack memory devices?

15 MR. CROSS: Object to form.

16 A. And so the answer is: Yes, they
17 were used prior to 2018. The patent itself
18 references prior art prior to 2018. But I
19 cannot tell you in detail the history of when
20 they were first used, who first used them,
21 and so on and so forth.

22 BY MR. KENYON:

23 Q. What materials would have
24 typically been used to create pillars that
25 provide mechanical support and prevent

1 pattern collapse before July 2018?

2 A. So that's two separate questions.

3 The first question is what
4 materials would be used in general, and the
5 second question is what materials would be
6 used prior to 2018.

7 And I'm going to concatenate those
8 two into the same question because I'm going
9 to assume that no new material fills appeared
10 after 2018.

11 So I'm going to also go down the
12 path of saying that if a pillar is used as a
13 support material or if it's a support pillar,
14 it needs to have the required stiffness to
15 meet the support function.

16 And just to cite to the patent
17 here, Column 18, Lines 27 and following: Any
18 suitable material was sufficient with
19 stiffness and/or support functions can be
20 used as the support material.

21 So I can then narrow this to say
22 that the support materials that would be
23 known in 2018, and thereafter as well, would
24 have materials with the required stiffness
25 and/or support function.

1 Q. What materials would a person of
2 ordinary skill in the art have used to meet
3 the required stiffness and/or support
4 function?

5 A. So this turns out to be a
6 complicated answer. The answer revolves
7 around assessing the important structural
8 characteristics.

9 Now, I do have in my declaration
10 at Paragraph 145 some analysis on this.
11 You'll notice the patent itself says that the
12 primary failure mode in the staircase is the
13 collapse mode, and there's a citation to 722
14 to 26.

15 There's other possible failure
16 modes. You can balloon things, you can crack
17 things. There's a whole variety of ways to
18 make things break in semiconductors. But the
19 collapse mode kind of narrows things down.

20 Now, at this point a POSITA has to
21 ask, well, what key parameters, key
22 mechanical parameters, would be needed to
23 determine a support pillar? And Dr. Banerjee
24 and I appear to be in agreement that Young's
25 modulus is not a bad start.

1 Now, it's an appropriate
2 high-level metric. There's -- you know, one
3 can get in a myriad of lower-level debates
4 about does Young's modulus reflect the
5 breadth of the alloys and compositions and
6 all of that.

7 But at a high level, a POSITA
8 would be using Young's modulus to select
9 appropriate pillar support materials.

10 Q. And so just so we're on the same
11 page, a POSITA would use Young's modulus
12 before July 2018 to select appropriate pillar
13 support materials?

14 A. That's what I said, but with a
15 narrowing that I'm not sure I intended.

16 A POSITA would be looking at the
17 spectrum of available materials and assessing
18 them based on their structural properties.
19 So far all we've talked about is as a support
20 material. And that one of the parameters,
21 and particularly a simple parameter that we
22 can discuss in this forum, would be Young's
23 modulus.

24 Q. But a person of ordinary skill in
25 the art would know how to choose materials to

1 create a support pillar, right?

2 A. Not necessarily. This is a
3 slightly different question. Keep in mind
4 that either by the definition of a POSITA
5 that I'm using and a definition of a POSITA
6 that Dr. Banerjee is using, the POSITA is not
7 deeply experienced in material science and in
8 the intricacies of structural mechanics.

9 If we go back to the POSITA
10 definition, and I'll just jump to that, she
11 says -- and I'll look at mine first and then
12 look at Dr. Banerjee's.

13 I have two years of professional
14 experience with semiconductor memory devices
15 or equivalent knowledge of level experience,
16 and Dr. Banerjee has about two years as well
17 but with monolithic 3D structures and NAND
18 memory devices.

19 The POSITA would have been aware
20 of and generally knowledgeable. Mechanical
21 stress in semiconductor devices is not
22 something that is part of a student's
23 teaching at the undergraduate level. It's
24 also not typically part of the first two to
25 three years of professional experience.

1 Structural analysis, the interplay
2 between structural forces and things like
3 conductivity, is outside the range of both of
4 our definitions of POSITA. A POSITA would
5 understand the analysis if presented to them,
6 but I think it's outside the range that a
7 POSITA would be able to do this type of a
8 choice on their own without the guidance of a
9 patent.

10 Q. What do you mean "the guidance of
11 a patent"?

12 A. Well, without the guidance of a
13 patent or without the guidance of prior
14 expertise in the company or without some form
15 of pathway as to what to do.

16 Q. Okay. I want to switch gears and
17 move to Column 13 of the '031 Patent.

18 A. Okay.

19 Q. And I want to first start with
20 Lines 36 to 41.

21 A. I'm at 36 through 41.

22 Q. Do you see that the '031 Patent
23 says: Further, a dielectric filling material
24 can be deposited after staircase structure
25 303 is formed to fill in the space formed by

1 the removal of the portions of dielectric
2 stack 203?

3 A. I see that.

4 Q. So the staircase structure is
5 formed by removing portions of the dielectric
6 stack?

7 MR. CROSS: Object to form.

8 A. So the patent's language says the
9 staircase regions are formed by removing
10 portions of the dielectric stack 203. I
11 believe I've read that correct. Hang on a
12 second.

13 Can you remind me of the column
14 again?

15 BY MR. KENYON:

16 Q. Column 13, starting on
17 lines -- sorry, Line 36.

18 A. So I guess I don't understand the
19 question. The patent says what it says.

20 Is the question -- yeah, why don't
21 you restate the question. I decided I don't
22 understand what I'm answering.

23 Q. Okay. Maybe I'll use the words
24 from the patent.

25 Staircase structure 303 is formed

1 by the removal of the portions of dielectric
2 stack 203?

3 A. Staircase structure 303 is formed
4 to fill in the space formed by removal of the
5 portions of dielectric stack 203, that's
6 correct.

7 MR. CROSS: Object to form.

8 BY MR. KENYON:

9 Q. Well, you added it to fill in the
10 space there.

11 A. That's the way the patent reads.

12 So let's start over here because I
13 may be misunderstanding the question or there
14 may have been a glitch in the electronics.

15 We are talking about Column 13, 35
16 to 37, and we're talking about the sentence:
17 Further, a dielectric filling material can be
18 deposited after staircase structure 303 is
19 formed to fill in the space formed by the
20 removal of the portions of dielectric stack
21 203.

22 Q. Correct.

23 A. So what's the question?

24 Q. I'm trying to understand what a
25 person of ordinary skill in the art would

1 read here and understand staircase structure
2 303 to be.

3 And so my question was: Staircase
4 structure 303 is formed by the removal of the
5 portions of dielectric stack 203, right?

6 A. That's correct.

7 Q. Okay. What does the '031 Patent
8 mean by "fill in the space"?

9 A. So I'd like to turn to the picture
10 that's associated with this. And I'm trying
11 to determine what picture that is so give me
12 a second here.

13 Q. What are you looking at right now?

14 A. I have the patent up. I am
15 looking here. I'm trying to tie this in with
16 the figure. We are now talking about details
17 of the formation of staircase structure 303
18 are described in Figures 7 through 12, so
19 that's the figures we're interested in.

20 And then what we have now is
21 the -- your statement: Further, a dielectric
22 filling material can be deposited after
23 staircase structure 303 is formed to fill in
24 the space formed by the removal of the
25 portions of dielectric stack 203.

1 And I'm working my way through
2 those figures to make sure that we're
3 comfortable with what is being precisely
4 referenced. And what I see is dielectric
5 filling structure 311 is deposited in the
6 periphery region 320 and core region 310 to
7 fill in the space formed by the removal of
8 the portions of dielectric stack 203.

9 And they -- I believe Figure 12 is
10 the most relevant figure. It doesn't quite
11 have the same numbering, and we're just going
12 to have to work our way through the slightly
13 different numbering than from what's written
14 in the patent.

15 So your question is basically, as
16 I see it, between Figure 11 and Figure 12 and
17 is regarding what is labeled 1201 in
18 Figure 12.

19 Is that correct? Is that where
20 you want me to go?

21 Q. My question was: What does the
22 '031 Patent mean by "fill in the space"?

23 A. So my understanding with this
24 discussion in Column 13 is that they're
25 referencing the space formed that's shown in

1 Figure 11 by the creation of the staircase
2 region with the material 1201 that is shown
3 in Figure 12.

4 Q. How would a person of ordinary
5 skill in the art fill that space?

6 A. So normally, some type of
7 deposition technique would be used. As we
8 discussed earlier, there would be the
9 potentials of a CVD deposition, sputtering,
10 there's some other types of deposition.

11 But it's clear from the language
12 "a dielectric filling material can be
13 deposited" that a deposition of some type is
14 suggested as, you know, perhaps opposed to
15 spin on or some other more complicated
16 technologies.

17 Q. You mentioned CVD.

18 How would you use chemical vapor
19 deposition to deposit dielectric filling
20 material to fill in the space?

21 A. You would put the wafer -- you
22 would create the staircase 1201 -- sorry.
23 You would create the staircase prior to 1201.
24 You would create the staircase as shown in
25 Figure 11.

1 And then you would put the wafer
2 in a CVD tool and do a deposition
3 sufficiently thick for the entire region to
4 have oxide in it, or whatever the dielectric
5 fill material is.

6 Q. And what is a CVD tool?

7 A. It is a piece of process equipment
8 that performs chemical vapor deposition.

9 Q. Okay. And you mentioned a
10 deposition sufficiently thick for the entire
11 region to have oxide in it.

12 A. Yes.

13 Q. What does "sufficiently thick"
14 mean?

15 A. So it's a conformal deposition.
16 Or if we're talking CVD specifically, it's a
17 conformal deposition, and you would need to
18 make sure that that area was filled all the
19 way to the top.

20 If we are referencing the sentence
21 further more -- or sorry: Further, a
22 dielectric filling material can be deposited
23 after the staircase structure is formed to
24 fill in this space, formed by removal of the
25 portions of the dielectric stack.

1 Then the implication of that one
2 sentence is that the dielectric fill material
3 needs to fill that space.

4 And since CVD is generally a
5 conformal deposition, the thickness needs to
6 be thick enough to fill that space.

7 Q. And when you say "conformal
8 deposition," are you referring to the same
9 conformal deposition that we discussed
10 earlier?

11 A. Yes. Conformal means that the
12 thickness is the same everywhere. So if I am
13 doing a conformal deposition of CVD to fill
14 the space, it has to be a thickness
15 sufficient to fill the space which will put
16 that same thickness on top of the core array
17 region.

18 Q. And we also discussed earlier how
19 the conformal deposition would occur on the
20 entire wafer.

21 Would that occur here as well?

22 MR. CROSS: Objection.

23 Mischaracterizes prior testimony.

24 A. So typically, in a manufacturing
25 operation, the -- a process step is

1 completed, in this case the space is created
2 by the removal of the portions of the
3 dielectric stack 203, then that entire wafer
4 is placed in the CVD tool.

5 And assuming it's a conformal
6 deposition and it's the correct kind of
7 CVD -- again, there's a myriad of ways to do
8 this -- but assuming that it's a typical
9 conformal CVD process, you're going to get a
10 blanket layer of CVD that's across the entire
11 wafer but is following the topography of the
12 wafer.

13 So it is on the wafer but is not
14 directly on the substrate.

15 BY MR. KENYON:

16 Q. Okay. And I've seen this in the
17 patent, the term "substrate."

18 Is the substrate -- what is the
19 relation between the term substrate and the
20 wafer?

21 A. Okay. That actually can get
22 contemplated because substrate and wafer can
23 end up having precise meanings in certain
24 patents. I'm going to give you a general
25 answer, but it's only a high level answer and

1 is not specific to any particular patent.

2 In general, a wafer is the
3 silicon -- typically silicon object that all
4 the processing is done on. It's, in modern
5 technology, a 12-inch disc that's a couple of
6 hundred microns thick.

7 The word "substrate" is variously
8 applied to the wafer itself or it can be
9 applied to layers within a preexisting
10 structure on the wafer or it can be applied
11 to a package or it can be applied to layers
12 in the package. Substrate is more
13 complicated.

14 In a very simple high-level usage,
15 substrate is often equated with wafer, but
16 they're not quite the same. Now, in response
17 to my question -- I'm sorry.

18 In response to your question, the
19 point I was making is that the conformal
20 deposition goes over all the existing
21 topography. It does not necessarily touch
22 the substrate. It does not necessarily touch
23 anything specifically.

24 It simply overlays whatever
25 existing topography is there at the time of

1 the CVD deposition.

2 Q. Okay. And going back to the CVD
3 tool, what does that tool look like?

4 MR. CROSS: Object to form.

5 A. So I have seen lots of CVD tools.
6 This is not something that can be described
7 in 30 seconds. I will give the general
8 answer CVD tools, particularly in
9 manufacturing, are large pieces of process
10 equipment.

11 They have gas lines plumbed into
12 them. They're typically made of stainless
13 steel. They have elaborate transport systems
14 to take wafers in and out. They have
15 elaborate ways of introducing gases and of
16 exhausting gases. They have appropriate
17 safety equipment. There's a whole science to
18 building CVD reactors which I'm peripherally
19 familiar with. I am not a module engineer.

20 So that's kind of a high-level
21 explanation of a CVD tool.

22 BY MR. KENYON:

23 Q. Where are the CVD gases plumbed
24 into the tool?

25 MR. CROSS: Object to form.

1 Object to also lacks foundation.

2 A. This is -- I -- again, I am not an
3 expert on CVD tool manufacturing technology.
4 And in all honesty, this is not an applied
5 materials patent. I don't have a lot of
6 personal information on the exact design and
7 engineering of CVD tools.

8 BY MR. KENYON:

9 Q. I'm just trying to understand how
10 the CVD process works, where the gases come
11 in, what occurs during the process.

12 A. Okay.

13 MR. CROSS: Objection to
14 relevance.

15 A. Yeah, I -- I can -- again, I'm not
16 a CVD expert. I'm process engineer and
17 device engineer. I can tell you what the
18 result of CVD is or the various results of
19 CVD, but I was not asked to do any detailed
20 work on CVD technology prior to this
21 deposition. I do not have a module
22 engineer's knowledge of CVD tool technology
23 at my fingertips.

24 BY MR. KENYON:

25 Q. Okay. I think we're about at the

1 hour mark. Do you want to take another break
2 or do you want to keep going?

3 A. I'd like to finish the CVD module
4 because it -- I want to get us to a clean
5 close on it and then let's take a break.

6 Q. Sure. I actually was going to
7 turn to the -- back to the patent.

8 A. Okay. Let's take a short break.

9 Q. Okay.

10 (A brief recess was held from
11 2:17 p.m. to 2:28 p.m.)

12 BY MR. KENYON:

13 Q. I wanted to direct your attention
14 to Column 13 of the '031 Patent, Lines 41
15 through 44. And let me know when you get
16 there.

17 A. I'm in Column 13, Lines -- 33
18 through 34, was that it?

19 Q. 41 through 44.

20 A. Oh, 41 through 44. Thank you.
21 I'm there.

22 Q. I apologize if I said anything
23 different.

24 A. Yeah, I may have just misheard.

25 Q. Okay. So the '031 Patent says: A

1 suitable planarization method (e.g., CMP
2 and/or recess etch) can be performed to
3 remove any excessive dielectric filling
4 material overlying the topmost surface of
5 staircase structure 303.

6 Do you see that?

7 A. I do.

8 Q. Okay. What does "CMP" stand for?

9 A. Chemical mechanical polish.

10 Q. Why is CMP a suitable
11 planarization method?

12 A. As we discussed earlier, CVD is a
13 conformal deposition technique, thus it
14 leaves a blanket of material everywhere, thus
15 there will be material on top of the array.

16 CMP is a very flattening technique
17 and can remove material that's on top of the
18 array without also removing material that's
19 on the staircase.

20 Q. And so when the patent says
21 "excessive dielectric filling material," is
22 it referring to the material that's on top of
23 the array?

24 A. The patent's exact language is:
25 Excessive dielectric material overlying the

1 topmost surface of the staircase structure.

2 And I would interpret that, and I
3 believe a POSITA would also interpret that,
4 to be specific to the material that is over
5 the staircase.

6 Q. And planarization would remove the
7 excessive dielectric filling material
8 overlying the topmost surface of the
9 staircase structure of 303?

10 A. That is the language in the patent
11 and that is also a common technique in the
12 art.

13 Q. Where would the dielectric
14 material terminate in the X direction?

15 A. So --

16 MR. CROSS: Objection to form.

17 Objection to lacks foundation.

18 A. So what figure are we discussing?

19 Are we still on Page 28 of my declaration

20 looking at the annotated version of

21 Figure 12?

22 BY MR. KENYON:

23 Q. So I want to focus on the
24 specification, the disclosure of the '031
25 Patent.

1 A. Okay.

2 Q. And we, before the break,
3 discussed a dielectric filling material can
4 be deposited, right?

5 A. Yes, we discussed that, that's
6 correct.

7 Q. And so I'm trying to understand
8 where that dielectric filling material is in
9 the X direction.

10 A. So your use of the word "X
11 direction" means that you are referencing a
12 figure. The Column 13 discussion following
13 35 is referencing Figures 7 through 12.

14 So I would propose that we discuss
15 the X direction in relation to Figure 12,
16 otherwise I have no idea which way it is.

17 Q. Sure. Why don't we -- let's go to
18 Figure 12.

19 A. So re-ask your question now that
20 we're both looking at Figure 12.

21 Q. Where would the dielectric filling
22 material terminate in the X direction?

23 MR. CROSS: Object to form.

24 A. Figure 12 shows it terminating
25 slightly inside the edges of the figure.

1 BY MR. KENYON:

2 Q. Okay. I'm trying to understand
3 what the disclosure of the '031 Patent
4 teaches, though.

5 MR. CROSS: Object to form.

6 A. So going back to Column 13: The
7 dielectric filling material is deposited
8 after the staircase structure is formed to
9 fill in the space formed by the removal of
10 the portions of dielectric stack 203. It's
11 deposited in the periphery region and the
12 core region to fill in the space formed by
13 the removal of the portions dielectric stack
14 203. The planarization method can be
15 performed to remove any excess dielectric
16 filling material overlying the topmost
17 service.

18 BY MR. KENYON:

19 Q. And before the break, you had
20 explained that one method of depositing the
21 dielectric filling material is using CVD?

22 A. Yes, I talked about CVD, that's
23 correct.

24 Q. And the process of using CVD would
25 deposit dielectric filling material across

1 the entire wafer?

2 A. So in general --

3 MR. CROSS: Object to form.

4 A. -- a CVD process, you put the
5 wafer in the CVD tool and you do a deposition
6 across the existing topography of the wafer.

7 BY MR. KENYON:

8 Q. Would the dielectric material
9 terminate at the end of the wafer?

10 MR. CROSS: Object to form.

11 A. So if we assume the dielectric
12 material has been polished with CMP as per
13 Lines 41 to 43, the excessive dielectric
14 filling material overlying the topmost
15 surface of the staircase structure has been
16 removed and we are left with the dielectric
17 filling structure 311 that surrounds the
18 staircase structure 303.

19 So the --

20 BY MR. KENYON:

21 Q. Okay.

22 A. -- edge of the wafer does not
23 appear anywhere in this discussion.

24 Q. Before planarization, would the
25 dielectric filling material deposited using

1 CVD terminate at the edge of the wafer?

2 MR. CROSS: Object to form.

3 A. So that is a question that is
4 extremely specific to the exact CVD
5 deposition. During our discussion so far, I
6 have been generically using the sort of
7 textbook, plain vanilla, conformal CVD, and
8 I've been answering the questions with that
9 textbook method.

10 There are a multiplicity of CVDs
11 available, and some of them are less
12 conformal. And so I can't say whether any
13 arbitrary CVD technique is going to do any
14 particular thing at the edge of the wafer. I
15 will also note that the patent itself does
16 not limit anything to CVD, but includes a
17 multiplicity of other techniques.

18 So I can't speak to what's going
19 on at the edge of the wafer either in general
20 or with reference to this patent because
21 there's many options.

22 BY MR. KENYON:

23 Q. What do you mean by "textbook,
24 plain vanilla, conformal CVD"?

25 A. So if you take a semiconductor

1 device class and you do the basic process
2 module in the class, they will typically
3 discuss CVD. They will sometimes discuss
4 some of the more -- the variant forms of CVD,
5 but the typical CVD that is described in an
6 undergraduate class is this type of conformal
7 CVD that I described in general earlier in my
8 deposition.

9 Q. Okay. We don't we go to Lines 44
10 through 48 of Column 13 in the '031 Patent.

11 A. Okay. I'm there.

12 Q. The '031 Patent says: The
13 remaining portion of the deposited dielectric
14 filling material (e.g., over staircase
15 structure 303 and isolation layer 109) can
16 form dielectric filling structure 311 that
17 surrounds staircase structure 303.

18 Do you see that?

19 A. I do see that.

20 Q. What does the '031 Patent mean by
21 "the remaining portion"?

22 A. So it appears to be clearly
23 defined in the parenthetical, "The remaining
24 portion of the deposited dielectric filling
25 material," and the "e.g." is an example: As

1 over staircase 303 and isolation layer 109.

2 So they provide an illustrative
3 example of where that would be.

4 Q. What does the '031 Patent mean by:
5 Can form dielectric filling structure 311?

6 A. Are you specifically requesting
7 about the emphasis on the phrase "can form"?

8 Q. Correct.

9 A. Well, I've not opined on that
10 exact phrase.

11 Q. Do you understand the formation of
12 dielectric filling structure to be a separate
13 step from the depositing of the filling
14 structure?

15 MR. CROSS: Object to form.

16 A. And I heard the question and it
17 did not click. So can you repeat that again?
18 BY MR. KENYON:

19 Q. Do you understand the formation of
20 dielectric filling structure to be a separate
21 step from the depositing of the filling
22 structure?

23 MR. CROSS: Object to form.

24 A. So are you asking in the sense of
25 a processed sequence where things are in

1 order or are you asking in the sense of a
2 patent claim that is describing a completed
3 structure?

4 BY MR. KENYON:

5 Q. A process sequence.

6 A. Okay. With that clarification,
7 could you repeat the question again?

8 Q. Do you understand the formation of
9 dielectric filling structure to be a separate
10 step from the depositing of the dielectric
11 filling structure?

12 MR. CROSS: Object to form.

13 A. So if we look at Column 13, the
14 various lines we've been working through, and
15 just for the record I'll remind everybody the
16 lines. We've been working through 35 and
17 thereafter. And these lines describe a
18 process sequence somewhat step by step.

19 They describe the -- they describe
20 the deposition of a dielectric filling
21 material after the formation of the staircase
22 structure. They describe where the material
23 is deposited in broad terms. They describe
24 the CMP to remove the excess filling
25 material. So those are, at least from the

1 process side, consecutive steps in the
2 process.

3 Q. So there's no separate step of
4 forming the dielectric filling structure?

5 MR. CROSS: Object to form.

6 A. So in general, when people are
7 speaking about a process flow, there are a
8 couple different ways of describing the
9 process flow.

10 One can say, for example -- and
11 I'll use some other layer in the process to
12 avoid confusion -- I am going to do an
13 implant, I am going to implant the wells, I
14 am going to put a gate dielectric on the
15 channel, I am going to form a polysilicon
16 gate over that, I am going to pattern it, and
17 so on and so forth, through 10 or 15 or 20
18 steps, and those 10 or 15 or 20 steps then
19 can also be described as I have formed a
20 transistor.

21 So I believe your question is
22 taking a phrase that is intended to describe
23 a multiplicity of steps which are contained
24 within the overall phrase.

25

1 BY MR. KENYON:

2 Q. Okay. Yeah, that's what I'm
3 trying to get at.

4 Is it a separate unique step or is
5 it a phrase that is describing a multiplicity
6 of steps disclosed in Column 13, Lines 36
7 through 48?

8 MR. CROSS: Object to form.

9 A. Okay. So I think I understand the
10 question. The question is -- and I'm going
11 to have you repeat the phrase so we can be
12 clear on this -- whether the phrase -- and
13 I'll have you say the exact
14 wording -- describes several different
15 process steps or one overall process step.

16 So remind me of the phrase again.

17 BY MR. KENYON:

18 Q. And can form dielectric filling
19 structure 311.

20 A. So I would consider the phrase
21 "and can form dielectric structure 311" as
22 summarizing the previous paragraph of
23 information, that information being the
24 deposition of the material, the polish of the
25 material, and so on and so forth.

1 Now, be aware that the patent does
2 say: Dielectric filling structure 311 is
3 deposited.

4 And then the patent says it's
5 polished to remove extra material, and then
6 it says it forms the dielectric filling
7 structure that surrounds the staircase.

8 So they are transitioning between
9 different meanings for that exact phrase as
10 the process is being described.

11 Did that make sense or do you want
12 me to say that again?

13 Q. No, it did. It did.

14 What part of this disclosure,
15 Lines 36 through 48 of Column 13 in the '031
16 Patent, causes the filling structure to
17 surround the staircase structure?

18 MR. CROSS: Object to form.

19 A. It's not the process sequence that
20 causes the dielectric filling structure to
21 surround the staircase structure. It's the
22 plan view layout that does that.

23 BY MR. KENYON:

24 Q. What do you mean "by plan view
25 layout"?

1 A. So in some sense -- and there's
2 exceptions to this. I'm speaking very
3 broadly.

4 In some sense, the process
5 describes what is happening in a cross
6 section. The layout describes what is
7 happening in the plan view. And so, for
8 example, if I only have cross-sections
9 available to me and I can't do top-down
10 patterning, I can only make a certain very
11 small set of structures.

12 It requires an associated
13 patterning process, which in many cases is an
14 implied patterning process, to make the
15 complete structure.

16 And as a specific example, if we
17 go to the '031 Patent -- and let me just pick
18 a picture arbitrarily. So I'm just going to
19 pick an unrelated picture just to make my
20 point.

21 In the '031 Patent in Figure 6,
22 there is one kind of a stepped channel
23 structure to the right in the figure and
24 another kind of unstepped support structure
25 to the left in the figure. Those are not the

1 same structures. They were not patterned the
2 same way.

3 But simply the process sequence
4 alone does not determine that in isolation.
5 There also is a patterning sequence and a
6 design that is required as well.

7 Q. Okay. So going back to Column 13,
8 Lines 36 through 48, is it your position that
9 reading Lines 36 through 48 does not tell a
10 person of ordinary skill in the art that the
11 filling structure surrounds the staircase
12 structure?

13 MR. CROSS: Object to form.

14 A. So I have two objections to
15 that -- at least two objections to that.

16 The first is that the language can
17 form dielectric fillings structure 311 that
18 surrounds the staircase structure indeed
19 indicates that the intent is to wrap -- to
20 surround the staircase structure.

21 The second point is that we can't
22 take this one little piece of the patent in
23 isolation. The patent describes in a number
24 of places, including in the pictures, the
25 more three-dimensional perception of this

1 structure. In particular, the way the
2 structure is oriented along the x-y and x-z
3 planes, which is important to understanding
4 the three-dimensional nature of the
5 surrounding relationship.

6 So, for example -- and I'm citing
7 here from my declaration in 72 -- we have
8 a -- places in the patent that say dielectric
9 pairs of different tiers can be etched to
10 form staircases extending along the x-y plane
11 and for staircase region 1121 and second
12 staircase region 1122 can each surround
13 memory structure 1100 along the x-y plane.

14 What's happening here is that the
15 specification is describing the directions
16 that are unseen in the simple cross-section
17 of Figure 12 that illuminates what it's doing
18 in the directions that we cannot immediately
19 see in that cross-section.

20 BY MR. KENYON:

21 Q. When you say the staircase
22 structure 1122 can each -- strike that.

23 When you say that the staircase
24 structure can surround the memory structure
25 along the x-y plane, what do you mean by

1 that?

2 A. Well, first, I'm not saying that.
3 The patent is saying that. That is
4 Column 22, Lines 30 and 32.

5 And the interpretation is that
6 along the x-y plane means that there is going
7 to be staircases on all four sides of this
8 object.

9 Q. And speaking about a specific
10 staircase on one side, is that staircase
11 coextensive with the memory region?

12 MR. CROSS: Object to form.

13 A. I don't know what the word
14 "coextensive" means. Can you rephrase that?

15 Wow. Hang on.

16 MR. KENYON: Are you okay?

17 THE WITNESS: My screen just
18 blanked. Give me a second.

19 MR. KENYON: Okay. Do you want
20 to go off the record?

21 THE WITNESS: No, I'm good. I'm
22 good. My computer just -- the screen
23 went black for some reason known only
24 to itself. I'm back.

25

1 BY MR. KENYON:

2 Q. Okay. So why don't -- I want to
3 get to the figures in a second and maybe it
4 will be easier with a figure in front of
5 us --

6 A. Okay.

7 Q. -- but the first objection that
8 you mentioned was that in Lines 36 through 48
9 of Column 13, it specifically states that
10 surround staircase structure 303.

11 A. That's correct, that's what I
12 said.

13 Q. Is it your position that that
14 phrase, surrounds staircase structure 303, is
15 the only disclosure in Lines 36 through 48
16 that tell a person of ordinary skill in the
17 art that the filling structure surrounds
18 staircase structure 303?

19 MR. CROSS: Object to form.

20 A. So your question is a little
21 confusing to me because you've asked what
22 part of that little section indicates to a
23 POSITA that the dielectric structure is
24 surrounding the staircase structure. And my
25 answer was, well, that phrase is in that

1 section at Lines 46 to 47.

2 So it's reasonably clear that the
3 dielectric filling structure 311 that
4 surrounds the staircase structure 303 is in
5 the patent text itself. If you're asking is
6 that the only place in the patent, no. The
7 patent describes in a variety of places,
8 which, you know, we can review my declaration
9 for those various places, but it describes
10 quite clearly that there's a staircase
11 structure in the x-y plane. So there's
12 staircases that a POSITA would interpret to
13 be on all four sides.

14 BY MR. KENYON:

15 Q. Okay. Why don't we move to
16 Lines 57 through 59 of Column 13.

17 A. Okay. I have 57 through 59
18 starting with "In some embodiments."

19 Q. Correct.

20 A. Am I correct?

21 Q. Correct.

22 So the '031 Patent says: In some
23 embodiments, dielectric filling structure 311
24 includes silicon oxide and is formed by CVD.

25 Do you see that?

1 A. I do see that.

2 Q. Okay. What does the '031 Patent
3 mean by the dielectric filling structure is
4 formed by CVD?

5 A. So in the art in general, there
6 are two broad classes of how we put materials
7 on a wafer. We can grow the materials, which
8 means that we are consuming the underlying
9 material to do so, or we can deposit the
10 materials, which means we're putting
11 something on top like painting.

12 Many of the technologies that
13 exist, for example, some of the high-pressure
14 CVD etch-dep-etch-dep-etch systems, etch and
15 dep at the same time, making it a little
16 ambiguous as to is this an etch, is this a
17 dep. It's not a growth, but what is this.

18 And so the word "formed" is often
19 used to avoid the intricacies of whether
20 something is a growth, a deposition, or some
21 dep-etch-dep process.

22 Q. And the filling structure formed
23 by CVD surrounds the staircase structure?

24 MR. CROSS: Object to form.

25 A. So if we're bouncing back to

1 Line 47, we have: Can form dielectric
2 filling structure 311 that surrounds the
3 staircase structure.

4 Line 57 is simply a description of
5 the materials: In some embodiments,
6 dielectric filling structure 311 includes
7 silicon oxide and is formed by CVD.

8 This seems to simply be an
9 expository sentence.

10 BY MR. KENYON:

11 Q. So dielectric filling structure
12 311 that surrounds the staircase structure
13 can be formed by CVD?

14 A. That's not what the patent reads.
15 I'm confused. Are you citing the patent?
16 The patent at Line 13 says: In the
17 embodiments, dielectric filling structure 311
18 includes silicon oxide and is formed by CVD.

19 Q. And so one method of forming
20 filling structure 311 is CVD, right?

21 A. That's correct. That's indicated
22 in Line 57.

23 Q. And filling structure 311
24 surrounds the staircase structure?

25 A. Filling structure 311 surrounds

1 the staircase structure, or more precisely,
2 if we jump back up to whatever line it is,
3 it -- dielectric filling structure 311 that
4 surrounds staircase structure 303.

5 Q. Does the '031 Patent explain how
6 to use CVD to form a dielectric filling
7 structure that surrounds the staircase
8 structure?

9 MR. CROSS: Object to form.

10 A. So the '031 Patent describes in
11 the section we've been reviewing, which is
12 Column 13, 36 to 65 or so, the various
13 process steps that -- the various process
14 steps that could be used to form an
15 embodiment that's displaying the dielectric
16 filling material surrounding 303.

17 But it is not explaining the
18 details of CVD because that is well
19 understood in the art.

20 BY MR. KENYON:

21 Q. Okay. Why don't we turn to
22 Figure 12.

23 A. Okay. I have Figure 12.

24 Q. So Figure 12 is an illustration of
25 a 3D NAND memory device, right?

1 A. So Figure 12 is an illustration of
2 part of a 3D NAND memory device, that's
3 correct.

4 Q. And Figure 12 shows filling
5 structure 1201, staircase structure 1104, and
6 core array region 1120?

7 A. All of that is correct, yes.

8 Q. So earlier I asked whether the
9 staircase structure was coextensive with the
10 memory array region.

11 Do you recall that?

12 A. You did. Yeah, and I had no idea
13 what coextensive meant.

14 Q. So why don't we focus on that
15 question now.

16 A. Okay.

17 Q. Is staircase structure 1104 the
18 same height in the z direction as core array
19 region 1120?

20 MR. CROSS: Object to form.

21 A. So this particular illustration
22 shows 104 to terminate equal in height with
23 1110. But as with many patent illustrations,
24 has no specific dimensionality involved with
25 it.

1 BY MR. KENYON:

2 Q. Based on the '031 Patent, do you
3 understand that staircase structure 1104 is
4 the same height in the z direction as core
5 array region 1120?

6 A. So the patent never actually says
7 that.

8 Can you -- I -- let me say this
9 more precisely. I don't believe the patent
10 says that.

11 Can you -- are you aware of a
12 place that you believe the patent says that?

13 Q. Well, maybe we can get at this a
14 different way.

15 In your declaration, you pointed
16 to Paragraph 72 earlier.

17 A. Okay.

18 Q. And why don't we go there and then
19 we can flip back to Figure 12.

20 A. Okay. I'm at 72.

21 Q. So in Paragraph 72, about halfway
22 down, you state that: The '031 makes clear
23 that the staircase regions (which have the
24 filling structure) also extend in the plus-y
25 and minus-y directions, and therefore

1 surround the memory structure.

2 Do you see that?

3 A. Yes, you read that correctly.

4 Q. What do you mean by "surround the
5 memory structure"?

6 A. So --

7 MR. CROSS: Object to form.

8 THE WITNESS: So, Allen, I
9 believe I went over your objection.

10 Do you want to object?

11 MR. CROSS: It's noted.

12 A. Okay. So do we want to have a
13 discussion about the meaning of the word
14 surround that I'm using, or do we want to
15 have a discussion about what the part looks
16 like three-dimensionally?

17 BY MR. KENYON:

18 Q. What the part looks like
19 three-dimensionally.

20 A. Okay. So my point, which I am
21 highlighting primarily in the latter part of
22 this paragraph is that there are a number of
23 citations in the patent, for example at 13:27
24 to 28: Dielectric pairs of different tiers
25 can be etched to form staircases extending

1 along the x-y plane.

2 And also at 22:30 to 32: First
3 staircase region 1121 and second staircase
4 region 1122 can each surround memory
5 structure 1100 along the x-y plane.

6 This use of "along the x-y plane"
7 is very indicative because it's different
8 than along the y direction or along the x
9 direction. It is indicative of a plane
10 relationship, which is suggestive to a POSITA
11 that this would be on all four sides or would
12 indicate to a POSITA it's on all four sides.

13 Q. Okay. And if we turn back to
14 Figure 12. And I'll let you get there.

15 A. Okay. I'm actually -- Figure 12,
16 I'm referencing Figure 12 that's in my report
17 on Page 28.

18 Q. Talk me through the -- where in
19 Figure 12 each of the staircases are.

20 A. So in Figure 12, we have a
21 staircase on the plus-x direction. We have a
22 staircase on the minus-x direction. And
23 those are both indicated in yellow.

24 We have a staircase -- and let me
25 see if I can get this right here. We have a

1 staircase in the plus-y direction, which is
2 away from us. And we have -- so it's the
3 staircase is stepping downwards on the side
4 we can't see into the page. And we have a
5 staircase in the minus-y direction, which is
6 facing toward us and is not seen because this
7 is a cross-section through the middle.

8 Q. Okay. Why don't we focus on the
9 staircase in the plus-X direction.

10 A. Okay. Which, just for clarity, is
11 the staircase in the right-hand side of the
12 image in Figure 12.

13 Q. Okay. You agree that the y
14 direction goes through the screen, correct,
15 of the page?

16 A. Yes. And I had a moment of
17 question as to which way it went, whether the
18 plus-y direction was into the page or out of
19 the page. I seem to remember x turns to y
20 and z goes up.

21 So I believe the y direction is
22 positive into the page and negative out of
23 the page.

24 Q. Okay. Where does the staircase
25 region on the right side of the core array

1 region stop in the positive-y direction?

2 A. It's unknown where that stops
3 because we do not have a clean top down. We
4 are -- we know from the language about x-y
5 plane that's repeated throughout the patent
6 and we know from the language surrounding
7 that there is intended to be a staircase on
8 the back and on the front.

9 But we don't have sufficient
10 information to know if the staircases are
11 relatively short things on each side of this
12 pyramid or longer things on each side of this
13 pyramid.

14 Q. So the '031 Patent does not
15 explain whether the staircase extends the
16 same length as the core array region?

17 MR. CROSS: Object to form.

18 BY MR. KENYON:

19 Q. In the y direction?

20 A. So the '031 Patent does not show a
21 top down -- a plan view that would clarify
22 precisely the extent of the -- the length, I
23 guess you would say, of the staircases.

24 Q. And so does Figure 12 show that
25 the staircase structure on the right side of

1 the core array region in the positive-x
2 direction is encircled by filling structure
3 1201?

4 A. So Figure 12 is a cross-section.
5 The encircling language arises from the
6 specification from the language that I cited
7 earlier about dielectric pairs can be etched
8 to form staircases extending along the x-y
9 plane.

10 Figure 12 is simply a
11 cross-section through one point of the y
12 plane, presumably at x equals zero -- sorry,
13 y equals zero, and does not give us details
14 as to what's going on either into the page or
15 out of the page.

16 Q. So looking at Figure 12, you
17 cannot determine one way or another whether
18 the staircase structure in the positive-x
19 direction is encircled by filling structure
20 1201?

21 MR. CROSS: Object to form.

22 A. So an assessment of a patent
23 will -- well, the specification and the
24 claims need to be looked at, and the figures
25 alone, particularly a single figure in

1 isolation, is typically not sufficient to
2 understand the scope of the patent.

3 Figure 12 in the absence of all
4 the other information in the specification,
5 it would be difficult to understand anything
6 other than what is actually shown in that
7 figure. It is the additional information,
8 the specification, that clarifies that there
9 is an x-y plane here and staircases extending
10 along both of those directions in the x-y
11 plane.

12 BY MR. KENYON:

13 Q. Okay. I want to get to the
14 specification portion that you're referring
15 to.

16 But first, when looking at
17 Figure 4.

18 A. Hang on.

19 Q. And I'll let you get there.

20 A. Let me find Figure 4. Give me a
21 second here.

22 So Figure 4, when I did whatever I
23 did to my screen, I apparently wiped it out,
24 so I loaded a new one.

25 Okay. So I am looking at

1 Figure 4.

2 Q. Okay. I want to ask the same
3 question.

4 So looking at Figure 4, you cannot
5 determine one way or another whether the
6 staircase structure is encircled by the
7 filling structure?

8 A. So Figure 4 is a -- not only a
9 cross-section in only one location, it's also
10 only one side. So Figure 4 contains even
11 less information than Figure 12. So Figure 4
12 would only tell us about, I'm going to call
13 it, the left-hand staircase. It would not
14 tell us about the right-hand staircase or the
15 back staircase or the front staircase.

16 Q. Okay. So why don't we turn to the
17 specification. And you mentioned that
18 there's additional information in the
19 specification that clarifies whether the
20 staircase structure is encircled by the
21 filling structure.

22 A. That's correct.

23 And I cite these in several places
24 in my declaration. I do want to point you to
25 Paragraph 49 where I cite: Which comprises

1 staircase regions that 'can each surround
2 memory structures along the x-y plane.

3 And that references to 13:44 to 48
4 and 22:30 to 32.

5 Q. If --

6 A. I also want to cite you to
7 Paragraph 72. And I've cited this before,
8 but this is the: Dielectric pairs of
9 different tiers can be etched to form
10 staircases extending along the x-y plane.
11 That's 13:27 to 28. And again, 22:30 to 32.

12 Q. If there are no staircase
13 structures in the y plane -- are you with me
14 so far?

15 A. So if there were no staircase
16 structures in the y plane. In other words,
17 my statement is just in broad terms, we
18 have -- if I look at Figure 12, we have a
19 right-hand staircase and a left-hand
20 staircase that is shown, and with regards to
21 my interpretation and the x-y plane, we have
22 a back staircase and a front staircase that
23 are not visible in the image.

24 Are we in agreement that that's
25 what I am proposing or --

1 Q. Correct.

2 A. -- opining on?

3 Q. Correct.

4 A. And so what you're saying is if I
5 don't have the front and back staircases,
6 that's your hypothetical?

7 Q. Correct.

8 A. Okay. So given that, what's the
9 question?

10 Q. Does filling structure 1201
11 surround staircase structure 1104?

12 MR. CROSS: Object to form.

13 A. So you're asking me that if I have
14 only two staircases, does the filling
15 structure surround, but we've not clarified
16 if there's other potential structures that
17 might also surround. In other words, a
18 filling structure surrounding could also
19 apply to structures that do not necessarily
20 have staircases immediately under them.
21 A possibility that Dr. Banerjee also
22 discusses.

23 So I would say that if we have
24 staircases only on the left and right but we
25 have no additional information, we don't know

1 if there's an existing -- the existence of a
2 surrounding layer.

3 BY MR. KENYON:

4 Q. So the existence of a surrounding
5 layer is based on having staircase structures
6 in the y plane, which you characterize as in
7 the back of the device and the front of the
8 device?

9 MR. CROSS: Object to form.

10 A. So if I look at the claims of the
11 patent, and I specifically look at Claim 1,
12 the language of the claim is a: Filling
13 structure surrounding the multiple stack
14 staircase structure.

15 That's the exact language in the
16 claims.

17 So omission of the front and back
18 staircase does not preclude that there is
19 some filling structure that's surrounding the
20 multiple-stack staircase structure. It's
21 just not quite as easy to explain as when
22 there's four structures.

23 BY MR. KENYON:

24 Q. If there's only staircase
25 structures on the left and right side of the

1 core array region, how would the filling
2 structures surround those staircase
3 structures?

4 MR. CROSS: Object to form.

5 A. So again, it depends on the
6 architecture. Let me back up and summarize
7 where we're at.

8 We have discussed my opinion that
9 the x-y description of one of the embodiments
10 of the patent indicates that surrounding is
11 intended on all sides of the structure with
12 regards that one embodiment. So a
13 surrounding is an A, a B, a C, a D. And I'm
14 using that embodiment as an example of that.

15 We have not yet had a discussion
16 as to whether structures can exist that may
17 have a surrounding filling structure around
18 the staircase region that may not exactly
19 look like that embodiment. But my response
20 would be, clearly, there are embodiments that
21 would exist that meet Claim 1 that may not be
22 precisely the same as the embodiment that I
23 am determining the use of the word
24 surrounding from.

25

1 BY MR. KENYON:

2 Q. And that's where -- really where
3 I'm getting at. I asked whether a person
4 of -- or whether you could understand that
5 the filling structure surrounds the staircase
6 structure in Figure 12, and I don't know the
7 exact language so I'm sure I'll get an
8 objection, but you characterized it as
9 Figure 12 is not enough to understand whether
10 the filling structure surrounds the staircase
11 structures.

12 MR. CROSS: Objection.

13 Mischaracterizes prior testimony.

14 A. I --

15 BY MR. KENYON:

16 Q. You then pointed me --

17 A. Well, I --

18 Q. You then pointed me to the column
19 -- you then pointed me to certain portions of
20 the specification.

21 A. Uh-huh.

22 Q. And I'm trying to understand why
23 those portions of the specification teach you
24 that the filling structure surrounds the
25 staircase structures.

1 A. Okay. That question -- so let me
2 make sure I'm answering -- the question, it
3 seems to have changed a little bit.

4 The question you're now asking is:
5 Why does 13:27 to 28 and 22:30 to 32 show
6 that the staircase is on all four sides? Is
7 that your question?

8 Q. No.

9 A. Okay.

10 Q. Why don't we go back to Figure 12.

11 A. Let's go back to Figure 12.

12 Q. Okay.

13 A. And what's your question with
14 Figure 12?

15 Q. So is it your opinion that
16 Figure 12 -- sorry. Strike that.

17 Looking at Figure 12, can you
18 determine whether filling structure 1201
19 encircles staircase structure 1104?

20 MR. CROSS: Objection. Asked
21 and answered.

22 A. And I will answer it again just
23 for clarity for the record.

24 Figure 12 in isolation without
25 reference to the specification or the claims

1 does not have sufficient information to
2 determine if the filling structure surrounds
3 the staircase region.

4 BY MR. KENYON:

5 Q. Okay. And what information do you
6 need to make that determination?

7 A. So you need some level of
8 two-dimensional information. And examples
9 include you need a topdown image or you need
10 language in the specification that contains
11 two-dimensional information or language in
12 the claims that contains two-dimensional
13 information.

14 Q. So let's go to the specification.

15 A. Okay.

16 Q. Could you please identify one
17 portion of the specification that explains to
18 you that filling structure 1201 surrounds
19 staircase structure 1104?

20 MR. CROSS: Object to form.

21 A. We can start at 22:30 to 32. And
22 the citation is: First staircase region 1121
23 and second staircase region 1122 can each
24 surround memory structure 1100 along the x-y
25 plane.

1 BY MR. KENYON:

2 Q. So this portion of the
3 specification does not mention filling
4 structure 1201, right?

5 A. It certainly mentions the first
6 staircase region and the second staircase
7 region, and it clarifies the two
8 dimensionality of the x-y plane.

9 Q. What do you understand "first
10 staircase region 1121" to mean?

11 MR. CROSS: Object to form.

12 A. So I understand first staircase
13 region 1121 to be that region that is
14 identified by 1121 in the figures.

15 BY MR. KENYON:

16 Q. Does first staircase region 1121
17 include both staircase structure 1104 and
18 filling structure 1201?

19 A. I believe you're making the subtle
20 point that the language in the patent
21 is -- the language that I am citing is
22 describing the staircase region rather than
23 the fill region.

24 And my contention is a POSITA
25 would recognize that the fill is on the

1 staircase, so the presence of staircase
2 regions in the x-y plane means that there are
3 fill regions in the x-y plane.

4 Q. What do you mean by "fill is on
5 the staircase"?

6 A. Well, let me go to the patent.
7 Hang on.

8 MR. CROSS: Brooks, we've been
9 going about an hour. Are we getting
10 close to a break?

11 MR. KENYON: Yeah, I mean, we
12 can break whenever. I -- it's unclear
13 based on her -- you know, her answers
14 whether I'm going to be done with this
15 module, but why don't we keep going
16 for five more minutes and then see
17 where we end up.

18 MR. CROSS: Okay. Thank you.

19 A. So I'm going to reference the same
20 place you referenced earlier for consistency,
21 and I'm going to reference this Column 13,
22 Lines 36 to -- I'm just going to say to 65
23 for the moment, which describes the
24 dielectric filling material being deposited
25 after the staircase structure 303 is formed.

1 And so I think the patent is clear
2 that the dielectric filling material is at
3 least associated with the staircase. So if
4 there are staircases on all four sides, there
5 is dielectric filling material on all four
6 sides as well.

7 BY MR. KENYON:

8 Q. The filling structure must
9 surround the staircase structure, though,
10 right?

11 A. Right.

12 Q. And so what I'm trying get at is
13 how do you know that the filling structure
14 surrounds a specific staircase structure of
15 the memory device?

16 MR. CROSS: Object to form.

17 A. This, I think, actually goes back
18 to what "surround" means because we wouldn't
19 be having this discussion if we agreed on
20 what surround meant.

21 BY MR. KENYON:

22 Q. Okay. Why don't -- that was
23 actually going to be the next thing that I
24 talk about, is going through your opinion of
25 surround. So why don't we stop, and then we

1 can pick that up after lunch.

2 A. That sounds great. Because the
3 way you're asking the questions here with
4 regards to the fill on the staircases really
5 points at a discrepancy on how we're
6 understanding surround. So this would be a
7 good point to stop and we can go debate
8 surround some more.

9 (A lunch recess was held from
10 3:26 p.m. to 4:15 p.m.)

11 BY MR. KENYON:

12 Q. All right. Welcome back,
13 Dr. Kuhn.

14 A. Same to you.

15 Q. Thank you.
16 Why don't we start with
17 Paragraph 70 of your declaration.

18 A. Uh-huh.

19 Q. Let me know when you're there.

20 A. I have Paragraph 70.

21 Q. In the first sentence you say:
22 The plain meaning of the surrounding is
23 encircling, right?

24 A. That's correct.

25 Q. And then a little further down in

1 Paragraph 70, you cite Exhibit 2003 and state
2 that this exhibit defines surround as: To
3 encircle on all sides of simultaneously.

4 A. That's correct.

5 Q. When looking at a staircase
6 structure, which sides of the staircase
7 structure does the filling structure need to
8 be on to surround the staircase structure?

9 A. So I do want to clarify one thing
10 with my definition that may be obvious, but I
11 want to avoid confusion.

12 I am not equating encircling with
13 there being a contiguous structure that is
14 connected all the way around. And the
15 example I will use -- I don't have all these
16 dictionary definitions in front of me, but I
17 believe one of them makes some comment about
18 policemen encircling a house. The
19 implication is not that the policemen are all
20 holding hands.

21 So I am not using the definition
22 of encircling that means completely
23 contiguous objects. I'm using a definition
24 where it is akin to policemen surrounding a
25 house.

1 With that in mind, the answer to
2 your question is the filling structure needs
3 to surround, as in the same sense of
4 encircle, to be on all sides of, but not
5 necessarily connecting.

6 So my interpretation of the word
7 "surround" in light of the specifications of
8 the patent is that it's on all sides, but
9 there's not a necessarily or there is not
10 required to be a continual connecting array.

11 Q. And so what sides are you
12 referring to?

13 A. The -- in general, the four sides
14 that we were talking about, Figure 12, it
15 would be the left and right side which are
16 shown, and the front and back side which are
17 not shown.

18 Q. And so just to be clear, looking
19 at Figure 12, it's your opinion that the
20 filling structure surrounds the staircase
21 structure in the positive-x direction on all
22 four sides?

23 MR. CROSS: Object to form.

24 A. Yeah, I would state that
25 differently since the positive-x direction is

1 only on one side.

2 I would say that the filling
3 structure surrounds the staircase structure
4 on the positive and negative-x and positive
5 and negative-y sides.

6 BY MR. KENYON:

7 Q. Okay. I want to focus on the
8 staircase structure on the positive-x side
9 and ignore any other staircase structure of
10 this memory device.

11 A. Okay.

12 Q. How is the staircase structure in
13 the positive-x direction surrounded on its
14 right side?

15 MR. CROSS: Object to form.

16 A. So we have talked about
17 surrounding in terms of objects -- of
18 multiple objects and multiple surrounding
19 features. Now we're eliminating it -- sorry,
20 we're limiting it to one of these objects and
21 still using the word surrounding. This is --
22 reminds me of the Zen paradox of listening to
23 one hand clapping.

24 BY MR. KENYON:

25 Q. Well, what do you understand the

1 claims to require?

2 A. So Claim 1 states: A filling
3 structure surrounding the multiple-stack
4 staircase structure.

5 Q. And so a portion of the
6 multiple-stack staircase structure is
7 illustrated in Figure 12 in the positive-x
8 direction --

9 MR. CROSS: Object to form.

10 BY MR. KENYON:

11 Q. -- of staircase structure 1104?

12 A. So let me try again on the point
13 of confusion.

14 The claim element requires a
15 filling structure surrounding the
16 multiple-stack staircase structure. It does
17 not specify that the filling structure needs
18 to be immediately adjacent, nor is that
19 consistent with the specification because
20 there's -- even if I limit myself to the
21 staircase on the right side in Figure 12, if
22 I'm only looking at that staircase, there's
23 no fill structure immediately to the left.
24 That's the array.

25 Q. So what portion of the filling

1 structure surrounds the staircase structure
2 in the positive X direction on its left side?

3 MR. CROSS: Object to form.

4 Sorry. For clarification, when
5 we say left and right side, are we
6 talking about on the figure or are we
7 talking about the staircase as you're
8 looking up it or down it?

9 MR. KENYON: We're talking about
10 the Figure 12. So the left side of
11 the staircase structure in the
12 positive-x direction of Figure 12.

13 A. Well, the -- okay. Now I'm even
14 more confused. Let's just spend a few
15 moments to make sure we're all talking about
16 the same thing.

17 There is a staircase structure on
18 the right-hand side, which is in yellow in
19 the Figure 12 on my Page 28. That staircase
20 structure has a left and right side when it
21 is in isolation.

22 There's also a staircase structure
23 on the left side of Figure 12 which is also
24 in yellow, and it also has a left and a right
25 side. And then I have opined that there are

1 staircase structures in and out of the page.

2 And so you are asking how -- I
3 believe you are asking how the fill on the
4 staircase structure on the right-hand side
5 and on the right-hand side of that staircase
6 structure is surrounding that one yellow box
7 on the right-hand side.

8 Is that what you're asking?

9 BY MR. KENYON:

10 Q. That's -- that's part of it. I
11 want to go through each of the -- each of its
12 sides to understand why you believe that the
13 term surround -- or sorry, that the staircase
14 structure on the right-hand side is
15 surrounded by filling structure.

16 A. Okay. Then let's do this one
17 question at a time and see if the answers
18 actually make sense.

19 Q. Okay. So when looking at the
20 staircase structure on the right-hand side of
21 the core array region, what portion of the
22 filling structure 1201 surrounds the
23 staircase structure on the right side of it?

24 A. So my initial answer to this,
25 before you added the last little caveat, was

1 that the filling structure on the left side,
2 right side, front, and back could be
3 considered to surround the staircase region
4 that's on the right side.

5 But then you said you can only
6 fill it on the right side and now I'm stuck
7 because I hear you asking how can a single
8 piece of the fill that's on a single side of
9 the structure surround the structure which
10 appears contradictory to me.

11 Q. I am trying to understand why you
12 believe that the staircase region in
13 Figure 12 is surrounded by filling structure.

14 MR. CROSS: Object to form.

15 A. And that one I can answer. I've
16 answered it in the previous pages as well and
17 in my declaration, but the filling structure
18 in -- sorry.

19 The staircases in Figure 12, given
20 the language along the x-y plane, the
21 staircases are -- on the right- and left-hand
22 side are illustrated in yellow on Page 28 and
23 there are staircases not shown in the image
24 on the front and back, and these staircases
25 have filling structures on them, which are

1 the purple in the image, 1201 in the image,
2 and so those -- that filling structure
3 surrounds that staircase structure.

4 BY MR. KENYON:

5 Q. Okay. When referring to the
6 staircase structures on the left and right
7 side of the core array region, what filling
8 structure surrounds those staircase
9 structures in the front and back?

10 A. So the filling structure on the
11 staircases on the front and back that are not
12 shown but are understood from the language in
13 the specification are part of the surrounding
14 structure.

15 Q. And so those filling structures
16 would be in a different x position than the
17 staircase --

18 A. Y position.

19 Q. Well, if --

20 A. Sorry. I didn't mean to
21 interrupt.

22 Q. Yeah, no, it's okay.

23 If your opinion is that there are
24 staircase structures on the front and back of
25 the core array region, then any fill

1 structure on those staircase structures would
2 be in a different x position compared to the
3 staircase structures on the left and right
4 side of the core array region?

5 A. I neither agree nor disagree
6 because I think you and I have a slightly
7 different mental picture of the geometry.
8 Let me repeat back what I am opining the
9 geometry to be.

10 There is a staircase on the left
11 and right in yellow in the picture on
12 Page 28. There is a staircase in the back
13 and front not shown in the picture but
14 implied in the specifications.

15 Each of those staircases has a
16 1201 layer on top of it, and thus that 1201
17 layer surrounds the staircases in an
18 encircling mode, not necessarily -- not
19 required to be contiguous.

20 So the answer to your question of
21 what is surrounding the staircase to the
22 right is the pieces of fill that are on all
23 four sides of the staircase to the right.

24 Q. Okay. Why don't we move to
25 Paragraph 73.

1 A. Okay.

2 Q. And in the last sentence -- I'll
3 let you get there.

4 A. I'm at Paragraph 73.

5 Q. Okay. In the last sentence, you
6 say: The filling structure therefore
7 surrounds/encircles the multiple-stack
8 staircase structure when it is deposited to
9 the left, right, back, and front of the
10 staircase structure.

11 Do you see that?

12 A. I do see that.

13 Q. What do you mean by: It is
14 deposited to the left, right, back, and front
15 of the staircase structure?

16 A. That's the same picture I'm trying
17 to describe from the cross-section in
18 Figure 12. I have a staircase structure on
19 the left and right, and I also have a
20 staircase structure on the front and back
21 that is not indicated clearly in the figure,
22 but is indicated in the specifications by the
23 use of this x-y plane language.

24 So if I were to visualize this
25 structure three-dimensionally, I have fill on

1 all four staircases. So I have the filling
2 structure encircling the multiple-stack
3 staircase structure because I have a fill
4 structure on the left, right, back, and front
5 of the staircase structures.

6 And the plural I'm using in the
7 moment to make it clear that there's a left,
8 right, front, and back staircase, which can
9 either be talked about as a staircase unit
10 with a left, right, front, and back, or
11 individual little pieces depending on what
12 makes it more clear.

13 Q. I might have misunderstood you,
14 but it sounds like what you were saying is
15 that the filling structure is deposited to
16 the left staircase structure, the right
17 staircase structure, the back staircase
18 structure, and the front staircase structure?

19 A. So we know from the specification
20 that the filling structure is, at minimum, on
21 the staircase. So if there are four
22 staircases, there are, at minimum, four
23 filling structures.

24 And so if I have a left staircase
25 and a right staircase and I have a front and

1 a back one, each one has associated with it a
2 fill-in structure.

3 Q. Okay. So I'm trying to focus in
4 on this deposited to the left, right, and
5 back of the staircase structure.

6 To me, deposited to the left,
7 right, back, and front of the staircase
8 structure signifies that you are depositing
9 something to the left, right, back, and front
10 of the staircase structure, not referring to
11 different staircase structures.

12 MR. CROSS: Objection to form.

13 BY MR. KENYON:

14 Q. Do you disagree?

15 A. Okay. That sentence is not a
16 quote. That sentence is what I am trying to
17 write to describe this structure.

18 And, again, I want to make clear
19 that we have two slightly different issues.
20 We have the issue of the dielectric filling
21 structure in general, which may or may not
22 have more elements than just that features
23 it's over the staircase. And we also have,
24 that is described very clearly in the
25 specification, the dielectric filling

1 structure that is over the staircase itself.

2 And so when we're talking about
3 how to interpret the claims, we can start
4 from the direction of saying where do we know
5 for sure there's dielectric fill structure.
6 And the answer is, well, we know for sure
7 it's over the staircase. It may be elsewhere
8 as well, but we know for sure it's over the
9 staircase.

10 And so if we have staircase on
11 four sides, we have dielectric structure on
12 four sides.

13 Q. Would a person of ordinary skill
14 in the art have understood that a single
15 deposition technique is capable of depositing
16 to the left, right, back, and front of the
17 staircase structure?

18 A. As we have discussed, a person of
19 ordinary skill in the art with two to three
20 years of experience -- and, again, I'm going
21 to just use Dr. Banerjee's POSITA definition
22 to, you know, avoid a debate there -- would
23 be -- would recognize that the staircase
24 filling operation is most likely done
25 simultaneously.

1 Now, obviously, there can be
2 different architectural requirements and so
3 on and so forth, but the simultaneous
4 deposition would be a typical way this would
5 be done.

6 So, yes, a POSITA as defined by
7 Dr. Banerjee would recognize this, in my
8 opinion.

9 Q. And I think you might have
10 suggested this, but there's no citation to
11 your sentence: The filling structure
12 therefore surrounds/encircles the
13 multiple-stack staircase structure when it is
14 deposited to the left, right, back, and front
15 of the staircase structure?

16 A. That sentence is my language and
17 it's my interpretation of the various
18 citations that appear in Paragraph 73 and
19 Paragraph 72 that describe the dielectric
20 filling material, where it's deposited, the
21 location of the staircases, and so on.

22 That's the summary of my opinion
23 of what this language means.

24 Q. If the memory device did not have
25 staircases on the front and back, would the

1 filling structure surround the staircase
2 structures of that memory device?

3 MR. CROSS: Objection. Form.

4 A. There's not enough information in
5 that question to answer it. As I said
6 before, the dielectric filling structure
7 includes that portion over the staircase but
8 may include other pieces as well. It's not
9 limited to that portion over staircase.

10 The reason I constructed my
11 analysis the way I did is because the patent
12 is extremely clear that the dielectric
13 filling material is at least over the
14 staircase. There may be other dielectric
15 filling structures present in any particular
16 design that augment this basic staircase
17 argument that you did not mention in your
18 question.

19 BY MR. KENYON:

20 Q. Do the claims require that
21 staircase structures exist on the from, back,
22 left, and right of the memory device?

23 A. The claims require two things.
24 And I'm just going to go to Claim 1. The
25 claims require: A multiple-stack staircase

1 structure comprising a plurality of staircase
2 structures stacked over the substrate -- I'll
3 skip all the details -- and requires a
4 filling structure surrounding the
5 multiple-stack staircase structure.

6 Q. Do the claims require the
7 staircase structure exists on the left,
8 right, back, and front of the memory device?

9 MR. CROSS: Objection. Asked
10 and answered.

11 A. The claims do not contain that
12 language.

13 BY MR. KENYON:

14 Q. So the claims could include or
15 could cover a memory device with staircase
16 structures on the left and right side, but
17 not on the back and front?

18 A. So any structure would need to be
19 compared against the claims themselves. And
20 I point to -- it would need to have a
21 multiple-stack staircase structure meeting
22 all the requirements of 1B. It would need to
23 have a filling structure surrounding the
24 multiple-stack staircase structure. And it
25 would need to have the semiconductor channel

1 and so on and so forth down the claims.

2 I point out that the filling
3 structure simply needs to be a filling
4 structure surrounding the multiple-stack
5 staircase structure. It is not specifically
6 limited to only have pieces over the
7 staircase structure.

8 Q. Okay. I'm trying to understand
9 when the stair- -- when the memory device
10 does not include staircase structures in the
11 front and back of the device and only
12 includes staircase structures on the left and
13 right side of it, what filling structure
14 surrounds the staircase structures?

15 MR. CROSS: Objection. Asked
16 and answered.

17 A. That's going to depend on the
18 design itself. You would need to look at the
19 design and see if there was a filling
20 structure that surrounded the staircase in
21 that particular design. It is not a
22 requirement. It's --

23 BY MR. KENYON:

24 Q. Okay. What portion --

25 A. The designs may have it, they may

1 not.

2 Q. What portion of the '031 Patent
3 explains to a person of ordinary skill in the
4 art that the filling structure surrounds the
5 staircase structure in this scenario?

6 MR. CROSS: Objection to form.

7 A. The claim itself states a filling
8 structure surrounding the multiple-stack
9 staircase structure.

10 BY MR. KENYON:

11 Q. I want to talk about the
12 specification.

13 Where in the specification?

14 MR. CROSS: Objection to form.

15 A. So are you asking me where in the
16 specification the exact language of the claim
17 is captured? Is that the question?

18 BY MR. KENYON:

19 Q. So for the past few questions, you
20 have been pointing to staircase structures on
21 the front, back, left, and right.

22 A. That's correct.

23 Q. Okay. Does the specification
24 explain how a filling structure surrounds the
25 staircase structure of a memory device if the

1 memory device comprises staircase structures
2 on the left and right side, but not the front
3 and back side?

4 MR. CROSS: Objection to form.

5 A. The specification in the patent
6 describes at some level of detail the
7 formation of the staircases, describes some
8 level of detail the formation of the filling
9 structures. It has the embodiment from which
10 I opined on the use of the word
11 "surrounding." It has other embodiments.

12 My understanding of the way
13 patents are interpreted is that the language
14 that matters is the precise language in the
15 claim. I am not saying that all embodiments
16 described by the '031 Patent have staircases
17 on all four sides.

18 I'm simply saying I used that
19 particular embodiment because it happened to
20 be clearer to validate my understanding of
21 the word "surrounding."

22 BY MR. KENYON:

23 Q. So you are basing your
24 understanding of surrounding on one
25 embodiment of the '031 Patent?

1 A. So I used that one embodiment of
2 the '031 Patent to confirm the understanding
3 of surrounding, which happened to also match
4 the plane and ordinary dictionary type
5 meaning.

6 Q. Can you point me to another
7 embodiment that does not include staircases
8 on all four sides?

9 A. I would have to go think about
10 that in some detail because I know which
11 embodiment has the staircases on all four
12 sides because it's the one I worked with to
13 get the language.

14 I can sort of answer it in a high
15 level way by saying it's the -- the
16 embodiments that do not specifically
17 reference the x and y plane geometry may be
18 embodiments that do not have staircases on
19 all four sides. But I'd have to sit and
20 think about it at some level of detail to get
21 all the right citations in the patent.

22 Q. Okay. What you haven't been able
23 to answer is how the filling structure
24 surrounds the staircase structure of a memory
25 device if the memory device comprises

1 staircase structures on the left and right
2 side but not the front and back sides?

3 MR. CROSS: Objection. Asked
4 and answered.

5 A. And I'm going to answer this one
6 more time in a different way and see if we
7 can bottom out on it.

8 The reason I can't answer that
9 question is it's too general. If you show me
10 a picture of a memory device that has
11 staircases on the left and right side, that
12 has other associated infrastructure
13 associated with the NAND flash, we can answer
14 that question in more detail.

15 But you're asking me how to answer
16 a question about the front and back of
17 something and not providing me any
18 information about the front and back. I
19 don't know if there's a dielectric fill
20 structure there or not.

21 The best answer I can give is if
22 you show me a topdown picture of something
23 with a staircase on the left and right, and
24 an obvious dielectric fill structure on the
25 top and bottom, then that would -- assuming

1 all the other claim limitations are met, that
2 would also meet the claim limitation.

3 BY MR. KENYON:

4 Q. Looking at Figure 12, Figure 12
5 does not illustrate staircase structures on
6 the front and back, right?

7 A. That's correct.

8 Q. And it is your position that
9 Figure 12 is illustrating a 3D device with
10 staircase structures on the front and back?

11 A. So my position is that the patent
12 in its discussion of Figure 12 permits an
13 embodiment with staircase structures on the
14 front and back.

15 Q. Okay. But Figure 12 does not
16 depict staircase structures on the front and
17 back?

18 MR. CROSS: Objection. Form.

19 A. Yes, we have discussed this
20 before.

21 Figure 12 in isolation is a simple
22 cross-section. It can't depict what is
23 either in front of or behind it. It just
24 can't do that. It doesn't have a topdown
25 associated with it.

1 I have stated and I have evidence
2 in my declaration that we've already worked
3 through that the '031 Patent describes an
4 embodiment which is in the x-y plane, so it
5 has staircases on all four sides, and I'm
6 using the existence of that embodiment to
7 clarify that my construction of surround is
8 the plain and ordinary meaning of having an
9 encircling of the fill structure, not
10 necessarily continuity of the fill structure.

11 BY MR. KENYON:

12 Q. Why don't we go to Paragraph 84.

13 A. Okay.

14 Q. And in -- I want to direct your
15 attention to the last sentence. You say: To
16 the extent that the ends of the device are
17 depicted or described in Tessariol, they
18 appear to be exposed.

19 Do you see that?

20 A. I see that.

21 Q. What do you mean by "they appear
22 to be exposed"?

23 A. I want to go to the figure in
24 Tessariol, and I believe it's Figure 17. I'm
25 picking Figure 17 largely because it's on

1 that same page of the declaration and we can
2 take a look at it.

3 If you'd like to reference another
4 figure, I can do that too. Are you okay with
5 Figure 17?

6 Q. Before we do that, why don't I
7 introduce Tessariol.

8 A. That's a good idea.

9 Q. For simplicity, I'm going to just
10 go ahead and share what's been marked both
11 Exhibit 1005 and Exhibit 1006.

12 Do you recognize Exhibit 1006 as
13 U.S. Patent Publication Number 2019/0081061,
14 which you referred to as Tessariol in your
15 declaration?

16 A. It's opening. Let me just confirm
17 that.

18 Do you want me to do 105 at the
19 same time?

20 Q. Why don't you stick with 106 first
21 and then I'll do 105.

22 A. By the way, how are you
23 pronouncing the name of this person? I have
24 no idea. I don't know this individual.

25 Q. I don't either. I've been

1 pronouncing it Tessariol.

2 A. Tessariol, I will go with that.

3 Q. Tessariol.

4 A. Okay. So Tessariol, I've opened
5 it, I've confirmed that's the same as the one
6 I have.

7 Q. Okay. Do you recognize
8 Exhibit 1005 as U.S. Patent Number 10,381,369
9 which you referred to as Kim in your
10 declaration?

11 A. Hang on. I just opened it.
12 And, yes, this looks like the 105
13 I have. I confirm that as Kim.

14 Q. Okay. So let's go back to
15 Paragraph 84.

16 A. And in particular, I think
17 Figure 17 above Photograph 84 that happens to
18 be annotated.

19 Q. Okay.

20 A. Why don't you ask the question
21 again for the record and I'll answer it.

22 Q. Why don't I start with the
23 statement in your declaration.

24 So you say: To the extent that
25 the ends of the device are depicted or

1 described in Tessariol, they appear to be
2 exposed.

3 Right?

4 A. That's correct.

5 Q. What you mean "they appear to be
6 exposed"?

7 A. The Figure 17 of Tessariol, which
8 will be the one I'll use for right now, has
9 the entire staircase structures inside the
10 confines of the figure, and you'll notice the
11 alternating layers just stop.

12 It's unclear whether they've
13 stopped because this is intended as a
14 fragment of a larger drawing, if that were
15 the case, people usually do little squiggly
16 lines; or if they've just stopped and are not
17 specified at all.

18 And that's why I've used the
19 language I used. Tessariol does not describe
20 either in the specifications or the claims
21 that the lateral ends of the stair step
22 materials are bordered. To the extent that
23 the ends of the device are depicted or
24 described, they appear to be exposed. And my
25 sort of caveat language there is because it

1 appears that they just are literally exposed.

2 There's no indication this is
3 inside a device or a -- you know, zoom in on
4 something. But that, I suppose, could be an
5 option.

6 Q. Okay. And how would you fabricate
7 exposed sides of a memory device?

8 MR. CROSS: Object to form.

9 A. At some point in the process you
10 put a mask on it and etch it.

11 BY MR. KENYON:

12 Q. Would there be any issues with
13 having sides of your memory device exposed?

14 A. As I mentioned earlier, it
15 is -- you don't want to short your gates
16 together. That's not quite the same thing as
17 you don't want to expose your gates. If you
18 etched -- let's just take Figure 17 for an
19 example.

20 If you etched all the way straight
21 down as indicated in Figure 17 and your
22 device just stopped there, there would need
23 to be some way to assure yourself that those
24 ends are not going to short together. It
25 could be as simple as an air gap structure.

1 This could be the edge of something that
2 never gets any further processing.

3 As long as the designer or the
4 architect can assure themselves that those
5 ends aren't going to short together, there
6 doesn't appear to be an issue for the device
7 functionality.

8 Q. Does Tessariol describe the ends
9 of the memory device as exposed?

10 A. Not that I recall.

11 Q. Okay. Why don't we go to
12 Paragraph 97.

13 MR. CROSS: That's Paragraph 97
14 of the declaration?

15 MR. KENYON: Correct.

16 A. I'm on Paragraph 97.

17 BY MR. KENYON:

18 Q. Okay.

19 A. I just want to make sure it is 97
20 because we've switched from Tessariol to Kim.

21 Q. The declaration. So Paragraph 97
22 of the declaration.

23 A. I'm there.

24 Q. Okay. In the second sentence you
25 say: Although, Kim states that insulation

1 layer 110 covers the entire top surface of
2 substrate 100, Kim does not disclose that the
3 substrate continues past the stack structure
4 in all four directions.

5 Do you see that?

6 A. I do.

7 Q. What do you mean by: Kim does not
8 disclose that the substrate continues past
9 the stack structure in all four directions?

10 A. Kim is a curiously limited patent
11 on describing directionality. Kim only
12 shows -- I'm going to call this the plus D1
13 direction. And I may need to find an
14 illustration to clarify that.

15 If you look at Kim Figure 3, which
16 I have on Page 40, Kim doesn't use x, y, and
17 z. It uses D1, D2, and D3. And I also do
18 want to point out that Kim does these very
19 strange cross-sections that have turns in
20 them. So some of these cross-sections that
21 we see in the images actually are not a
22 straight across the device, they have a turn
23 or multiple turns.

24 Anyway, my point is that Kim is
25 not showing what's happening in the plus and

1 minus D1 directions as well in the minus D2
2 direction.

3 More specifically, and right at
4 the beginning of page -- Paragraph 98, I
5 state: Kim does not show the insulation
6 layer 110 covering the side of the structure
7 in the plus and minus D1 directions, as well
8 as in the minus D2 direction.

9 Q. Going back to Paragraph 97, you
10 specifically say that Kim does not disclose
11 that the substrate continues past the stack
12 structure in all four directions.

13 MR. CROSS: Objection.

14 A. Let me -- yeah, let me check that
15 citation.

16 Yeah, so 9:53 to 56 says: The
17 filling insulation layer 110 may be disposed
18 on the substrate 100 and may cover the stack
19 structures ST. The filling insulation layer
20 110 may have a planarized top surface. A
21 vertical thickness of the filling insulation
22 layer 110 may increase as a horizontal
23 distance from the cell array.

24 So my point was that Kim does not
25 disclose anything in all four directions, not

1 necessarily that it's not disclosing the
2 substrate and it's disclosing other stuff as
3 well. It's simply talking about the
4 insulation layer in the single direction
5 that's shown in 4A.

6 BY MR. KENYON:

7 Q. We discussed earlier that memory
8 devices would have been fabricated on a
9 wafer, right?

10 A. That's correct.

11 Q. And you mentioned that typically
12 you would equate wafer and substrate, right?

13 MR. CROSS: Objection.

14 Mischaracterizes prior testimony.

15 A. So as I mentioned earlier, I
16 described a substrate in some -- sorry, I
17 described a wafer in some detail with regards
18 to it being, you know, 12 inches and so on
19 and so forth, and I also mentioned the
20 substrate may have a more different or subtle
21 meaning than wafer.

22 I don't want to repeat my entire
23 testimony of earlier because I thought quite
24 a bit about the question, and if I repeat it
25 again, I may not have the detail I did the

1 first time around.

2 BY MR. KENYON:

3 Q. Okay. Does Kim limit the
4 substrate to the stack structure?

5 MR. CROSS: Objection. Form.

6 A. Kim is fundamentally showing only
7 one part of the device. It's showing the
8 device in only one area, and it's not even
9 showing a clean cross-section because
10 Figure 4A is not across the device.

11 BY MR. KENYON:

12 Q. Okay. Does Kim limit the
13 substrate to the stack structure?

14 MR. CROSS: Objection. Form.

15 BY MR. KENYON:

16 Q. Can you describe what you're
17 looking at?

18 A. I'm looking through Kim because
19 your question is not clear to me. And so I'm
20 looking through Kim to see if the word
21 "substrate" is used in an unexpected way.

22 Q. Okay. How about we do this.

23 For this sentence use cite
24 Column 9, Lines 53 through 56, right?

25 A. I believe so. Let me double-check

1 that. And I actually read those to you, I
2 believe.

3 Q. Right?

4 A. Yes. So, yes, I cite 53 through
5 96, and, yes, I read that to you.

6 Q. Okay. Do you mind going to
7 Column 9, Lines 53 through 56?

8 A. Sure. Would you like me to read
9 them? I'm there.

10 Q. No, I'll have a question. Let me
11 know when you're there.

12 A. I'm there.

13 Q. This portion of Kim does not limit
14 the substrate to the stack structure, right?

15 MR. CROSS: Objection. Form.

16 A. So 53 to 57 describes that the
17 filling insulation layer 110 may be disposed
18 on the substrate 100 and may cover the stack
19 structures, ST. The filling insulation layer
20 110 may have a planarized top surface. A
21 vertical thickness of the filling insulation
22 layer 110 may increase as a horizontal
23 distance from the cell array.

24 So that section is describing the
25 little piece that is more or less shown in

1 Figure 4A.

2 BY MR. KENYON:

3 Q. But this portion of Kim does not
4 limit the substrate to the stack structure,
5 right?

6 MR. CROSS: Objection to form.

7 BY MR. KENYON:

8 Q. It's a yes-or-no question.

9 A. What do you mean by "limit the
10 substrate to the stack structure"?

11 Let me ask this another way. When
12 you say "limit the substrate to the stack
13 structure," are you saying that this section
14 of Kim does not say that the substrate can
15 only be under the stack structure?

16 Q. I am asking what you understand
17 substrate to mean in Kim?

18 MR. CROSS: Objection. Form.

19 A. Okay. So I'm going to go to
20 Column 10 of Kim. So Column 10 says:
21 Referring to Figs 3 and 6 --

22 (Reporter clarification.)

23 A. I'll repeat that just for the
24 record. I'll start over.

25 Referring to Figs 3 and 6,

1 insulating layers, IL, and first sacrificial
2 layers, HL1, may be vertically and
3 alternately stacked on an entire top surface
4 of substrate 100 to form a lower mold
5 structure, MT1.

6 The substrate 100 may include a
7 cell array region, CAR, and a connection
8 region, CTR. An etch stop layer, ESL, may be
9 formed on the uppermost one of the first
10 sacrificial layers, HL1. For example, the
11 substrate 100 may be a silicon substrate, a
12 germanium substrate, or a silicon germanium
13 substrate.

14 My conclusion from this is that,
15 at minimum, the substrate 100 needs to
16 include the cell array region and the
17 connection region.

18 BY MR. KENYON:

19 Q. Okay. And does Kim limit the
20 substrate to the cell array region in the
21 connection region?

22 MR. CROSS: Objection. Form.

23 A. So I've looked through Kim, and
24 exclusive of the claims, which do have the
25 word substrate embedded in the claims, and

1 might be more complex, the specification does
2 not appear to limit it to the core and cell
3 region. More specifically, the language is:
4 May include a cell region CAR and a
5 connection region CTR.

6 BY MR. KENYON:

7 Q. Okay. Why don't we move on. I
8 want to point you to paragraph 98.

9 A. I'm there.

10 Q. I think it's the last four lines
11 of this paragraph, you say: Even if the
12 assumption is made that Kim is adjacent to
13 another (undisclosed) structure, and thus
14 requires some intervening isolation to that
15 structure, there are a variety of common
16 semiconductor processing techniques to
17 produce an exposed (unfilled) edge between
18 the disclosed structure and other adjacent
19 structures.

20 Do you see that?

21 A. I do.

22 Q. What do you mean by "adjacent
23 structures"?

24 A. So Kim is only showing one half of
25 staircase region. Or let me -- sorry, that

1 didn't come out right. Let me rephrase.

2 Kim is showing a cross-section
3 that only shows a staircase region on one
4 side. Kim does not disclose a staircase
5 region elsewhere. Kim does not have any
6 language suggesting a staircase region is in
7 front or back either as the '031 Patent has.

8 All the information in Kim that
9 I've seen says it's disclosing a one-sided
10 staircase. So for this question of
11 surrounding, the question is what's on the
12 other side.

13 So as we talked about with
14 Tessariol, the other side could be an exposed
15 unfilled edge that faces into something else.
16 It could face into an array facing the other
17 direction. It could face into the end of the
18 die. It could face into undisclosed other
19 objects.

20 But if there is the need for
21 isolation between this one-sided Kim
22 structure and something else, that doesn't
23 say that that isolation must be a piece of
24 fill material or include a piece of fill
25 material.

1 Q. But the isolation could be a piece
2 of fill material, right?

3 A. It could, but it's not required to
4 be.

5 Q. What do you mean by "exposed
6 unfilled edge"?

7 A. What I mean is, let's make the
8 assumption that Kim -- and I'm just going to
9 simplify it -- Kim is a memory block that has
10 a staircase on one side and just stops. That
11 staircase accesses all the core that's -- I'm
12 going to put the staircase on the right. The
13 staircase accesses all the core that's to the
14 left. And then the array just stops.

15 Well, you need to isolate it
16 somehow from everything else, but you could
17 isolate it with simply a trench. And by
18 that, I mean an exposed unfilled edge between
19 the disclosed structure and other adjacent
20 structures. I am saying that there could be
21 a gap or trench that's simply a hole between
22 the disclosed structure and other adjacent
23 structures.

24 Q. Would the exposed edge of the
25 structure be exposed to the air?

1 A. Depends on how you make it.

2 As I mentioned before, they are
3 air gap technologies that can leave that edge
4 unfilled. But that doesn't necessarily mean
5 it's exposed to air. It could be exposed to
6 nitrogen.

7 Q. But it would still be exposed to
8 the air, nitrogen, whatever is inside the air
9 gap?

10 A. Whatever you design to be inside
11 the air gap.

12 Keep in mind that exposure to air
13 typically has concerns with regards to
14 contamination. You could always put a gas in
15 there that would mitigate those concerns.

16 Q. What gas would mitigate those
17 concerns?

18 A. Nitrogen.

19 Q. How would you insert the nitrogen
20 gas into that air gap?

21 A. If the air gap is sealed, you
22 simply put nitrogen in the chamber prior to
23 the sealing step.

24 Q. Is that an additional step to
25 everything else?

1 A. Probably not.

2 MR. CROSS: Objection. Form.

3 A. Obviously, it depends on which
4 particular fabrication tech you're using.
5 But keep in mind air is generally unwanted in
6 semiconductor processes. So most tool suites
7 exclude air as standard practice.

8 When I say "air," I probably
9 should be more precise and say inert gas.

10 BY MR. KENYON:

11 Q. Is it standard practice to include
12 nitrogen?

13 A. Many inert gases are used.
14 Nitrogen is common because it's cheap. It's
15 not the only one.

16 Q. Let's go to Paragraph 100. And
17 let me know when you're there.

18 A. I'm there.

19 Q. I want to talk about the last
20 sentence.

21 A. Okay.

22 Q. So in the last sentence, you say:
23 The presence of the trenches on the sides of
24 the stack structure shows that Kim's
25 insulation layer does not have to extend to

1 the 'other three sides of the structure.

2 Do you see that?

3 A. I see that.

4 Q. What do you mean by that?

5 A. I believe that I'm citing Banerjee
6 on that.

7 Q. You're quoting --

8 A. The Kim discloses filling material
9 on the outer edge of where the staircase
10 ends. That's a quote from Banerjee.

11 MR. CROSS: Objection.

12 Mischaracterizes prior testimony.

13 BY MR. KENYON:

14 Q. I'm specifically asking about the
15 unquoted portion. The preference of the
16 trenches on the sides of the stack structure
17 shows that Kim's insulation layer does not
18 have to extend to the other three sides of
19 the structure.

20 MR. CROSS: Objection.

21 Mischaracterizes prior testimony.

22 A. So I'd like to turn your attention
23 to Page 43.

24 BY MR. KENYON:

25 Q. Sure.

1 A. And that may clarify this little
2 bit of confusion.

3 Q. I'm there.

4 A. Yeah. There's an annotated
5 Figure 4 on Page 43 that's got purple where
6 the insulating layers are. Purple is layer
7 110.

8 The way Kim describes the process
9 and is illustrated in Figure 24 of Kim is
10 that there are trenches cut through the
11 insulating layer after it is present that are
12 existing in, in this case, the D1 direction.
13 So the trenches go in the D2 direction, but
14 the line of trenches progresses down the D1
15 direction.

16 Those trenches clearly are not
17 filled. There is insulating material above
18 the staircase, but there's no insulating
19 material between the trenches because they've
20 already been -- they've been cut after the
21 material is present. They've been cut after
22 110 is present.

23 And now if we loop back to my
24 previous comment, there's no requirement that
25 additional fill material be put in those

1 trenches. There's a variety of other ways to
2 potentially fill those trenches, and that is
3 not described in Kim.

4 Q. If the trenches were filled with
5 insulation material, it is your position that
6 going back to Paragraph 100, that the
7 presence of the trenches on the sides of the
8 stack structure show that Kim's insulation
9 layer does not extend -- does not have to
10 extend to the other three sides of the
11 structure?

12 MR. CROSS: Objection. Form.

13 A. Okay. That's complicated. Let me
14 answer it in a slightly different way.

15 In the way Kim discloses its
16 information, Kim Figure 24 is clear that the
17 filling insulation layer 110, which is purple
18 in my picture on Page 43, is not on three of
19 the four sides. It is not on minus D2, plus
20 D1, and minus D1. So it's only on the plus
21 D2 side.

22 Now, I am first contending there's
23 no requirement that that hole be filled again
24 with insulating material. As I said before,
25 there are others ways to manage slots without

1 filling them with an insulating material such
2 as silicon dioxide.

3 But even if I, for the sake of the
4 argument, say, well, let's fill them with
5 insulating material, it still hasn't resolved
6 what's in the direction of negative D2.
7 Negative D2 is just not specified.

8 Q. Okay. I think we're at a one-hour
9 mark again. Do you want to take a break, or
10 do you want to keep going?

11 A. Yes, I do. I was just about to
12 request a break.

13 Q. Okay. Perfect timing then.
14 (A brief recess was held from
15 5:15 p.m. to 5:24 p.m.)

16 BY MR. KENYON:

17 Q. All right. Let's go to
18 Paragraph 101. Let me know when you're
19 there.

20 A. I'm at 101.

21 Q. Okay. In the sentence starting
22 with "Even assuming," I think it's the second
23 or the third sentence, you say: It is not
24 necessarily the case that an insulating layer
25 would be used to provide that electrical

1 isolation.

2 Do you see that?

3 A. I see that.

4 Q. What electrical isolation are you
5 referring to?

6 A. So I'm going to refer to
7 Figure 24, which is on the subsequent page.
8 And I'm doing this to remind us that the
9 minus D2 direction is to the left in the
10 figure. So the right in the figure, the plus
11 D2 direction is where the staircases are.
12 The minus D2 direction, it just stops.
13 There's no staircase. There's no information
14 given there.

15 So my point in Paragraph 101 is
16 that in the minus D2 direction, Kim doesn't
17 show insulating layer 110. It doesn't
18 actually show anything. Now, should there be
19 some adjacent structure to which electrical
20 isolation was needed, for example, it was not
21 uncommon in the art to mirror image the array
22 should there been an array facing the other
23 direction, and there would -- needed to be
24 electrical isolation between the two, you
25 don't need to put an insulating layer in

1 there. There's other options.

2 And that's what I meant by that
3 phrase.

4 Q. Okay. But one technique to
5 provide electrical isolation is using an
6 insulating layer?

7 A. That is one of several techniques,
8 that's correct.

9 Q. And you can deposit the insulating
10 layer using CVD?

11 A. You could deposit an insulating
12 layer using CVD. That is one technique to
13 provide an insulation or isolating layer.

14 Q. Why don't we go to Paragraph 107.

15 A. I'm there.

16 Q. You say: Planarized top surface
17 does not necessarily mean that the stack is
18 encased on all sides.

19 Do you see that?

20 A. I do.

21 Q. What do you mean by that "does not
22 necessarily mean"?

23 A. Dr. Banerjee in his declaration
24 appears to be confusing the existence of a
25 planarized top surface with the idea that

1 something is encased on all sides. These are
2 not the same thing.

3 The fact that the top of something
4 is flat does not give you any information on
5 the cross-section. The cross-section may not
6 be flat. It may have holes in it. It may be
7 structured in a variety of ways.

8 Q. Could a person of ordinary skill
9 in the art understand that a planarized top
10 surface means that the stack is encased on
11 all sides?

12 MR. CROSS: Objection. Form.

13 A. I may have misheard the question.
14 Why don't you restate it.

15 BY MR. KENYON:

16 Q. Could a person of ordinary skill
17 in the art understand that a planarized top
18 surface means that the stack is encased on
19 all sides?

20 MR. CROSS: Objection. Form.

21 A. A POSITA would well understand
22 that a planarized top surface means the top
23 surface is planarized. It bears no
24 information about what's happening underneath
25 the surface.

1 BY MR. KENYON:

2 Q. Okay. Why don't we go to
3 Paragraph 109.

4 A. I'm there.

5 Q. In the second sentence, you say:
6 There is no requirement in the art that the
7 electrical separation be implemented by
8 filling with an insulation material.

9 Do you see that?

10 A. I see that.

11 Q. And the electrical separation that
12 you were referring to is electrically
13 separating one plane of memory from an
14 adjacent plane of memory?

15 A. No, it is broader than that. I'm
16 simply saying that what is going on in the
17 minus D2 direction of Kim is simply not
18 specified at all.

19 And I'm presenting the
20 hypothetical that if there were something
21 over there, and as we well know, products are
22 formed of many different blocks, if there's
23 something over there we care about and if we
24 want to do electrical separation to that
25 something, we don't necessarily have to use a

1 fill -- we don't necessarily have to fill the
2 slot between the two with an insulating
3 material. We could use an air gap or other
4 technologies.

5 Q. But you would agree that
6 electrical separation can be implemented by
7 filling the space with an insulating
8 material?

9 MR. CROSS: Objection. Form.

10 A. So I certainly agree that filling
11 a space between two objects is one way to
12 provide electrical isolation. An air gap
13 would be another way.

14 BY MR. KENYON:

15 Q. Okay. Let's go to the last
16 sentence of the same paragraph because it
17 starts talking about air gaps.

18 A. Yes.

19 Q. Let me know when you're there.

20 A. The sentence beginning with
21 "thus"?

22 Q. Correct.

23 A. Yes, I'm there.

24 Q. So you say: There are a wide
25 variety of techniques available in the art

1 for creating air gaps, .

2 And then you list certain
3 techniques.

4 A. That's correct.

5 Q. Is that accurate? Okay.

6 Other than the techniques listed,
7 are there any other techniques for creating
8 air gaps?

9 A. Well, I'm sure there are. I
10 happened to list techniques that I was
11 familiar with.

12 Q. Are these techniques common for
13 electrically isolating staircase structures?

14 MR. CROSS: Objection. Form.

15 A. So these specific techniques that
16 I listed here are more oriented to the
17 problem in this section, which is Kim's minus
18 D2 direction. I recall that this 109
19 paragraph is all in a section on Kim. The
20 paragraph that I believe begins talking about
21 the minus D2 direction of Kim -- sorry, that
22 was the paragraph before.

23 And then I come into describing
24 several of the possible techniques that you
25 could put an air gap between the minus D2

1 direction of Kim and a potential adjacent
2 structure.

3 BY MR. KENYON:

4 Q. In the -- and the last example is
5 embedding an air gap during processing of the
6 memory structure.

7 Do you see that?

8 A. I see that.

9 Q. What do you mean by embedding an
10 air gap?

11 A. Well, a good example was that
12 patent that we reviewed earlier where I
13 believe Figure 2L showed an embedded air gap
14 in a memory structure. I was unaware of that
15 patent when I wrote this sentence, but that
16 patent would have been a nice reference right
17 here.

18 Q. And that's embedding an air gap in
19 a trench?

20 A. It was an -- embedding an air gap
21 in a gate line slit.

22 Q. What is a -- strike that.

23 Is a gate line slit a trench?

24 A. A gate line slit could be
25 considered a trench. It is a common object

1 in the manufacturing of memory devices such
2 as 3D NAND flash.

3 Q. Why do you say it's a common
4 object?

5 A. I believe your original question
6 asked if these were used commonly. I may
7 have misheard.

8 Q. Well, I think you were referring
9 to a gate line slit?

10 A. Yes, I was.

11 Q. Or were you referring -- as a
12 common object?

13 A. So why don't you ask the question
14 again because I may have misunderstood --

15 Q. Sure.

16 A. -- where you were going.

17 Q. So you say it's a common object in
18 the manufacturing of memory devices such as
19 3D NAND flash. I'm just trying to understand
20 what "it" is in that sentence.

21 A. Oh, my apologies.

22 What I meant was the gate line
23 slit is a common object in the manufacture of
24 3D NAND flash. It's not some super
25 specialized structure.

1 Q. Got it.

2 What portion of the '031 Patent
3 teaches embedding air gaps to electrically
4 isolate staircase structures?

5 MR. CROSS: Objection. Form.

6 A. The '031 Patent does not speak
7 specifically to air gaps. The '031 Patent in
8 general is describing a structure, not a
9 process technology. It's not a method
10 patent.

11 BY MR. KENYON:

12 Q. Does Kim teach embedding air gaps
13 to electrically isolate staircase structures?

14 A. I don't recall.

15 Q. Why don't we go to Paragraph 110.

16 A. I'm there.

17 Q. You say in the first sentence,
18 this is about halfway through: There is a
19 common technique for creating an embedded air
20 gap which takes advantage of the
21 nonconformity of a CVD dielectric layer to
22 create air cavities located inside trenches.

23 Do you see that?

24 A. I do.

25 Q. So this technique creates air

1 cavities located inside trenches?

2 A. That's correct.

3 Q. What do you mean by "common
4 technique"?

5 A. So let me put this sentence in
6 context.

7 One of Dr. Banerjee's points was
8 that the simple disclosure of CVD immediately
9 creates the oxide encasing an object. And I
10 disagree with Dr. Banerjee's point. I
11 disagree that simply evoking CVD immediately
12 says that there is an oxide encased
13 structure.

14 And as one example, I gave this
15 particular technique which is use of a CVD
16 layer to create air cavities located inside
17 of trenches. I haven't done a huge study for
18 what's the most common way to create air
19 gaps. My personal sense is that CVD is
20 pretty common.

21 But my main point is this
22 technique is reasonably well-known, it uses
23 CVD, and it refutes Dr. Banerjee's point.

24 Q. Do you cite any other technique
25 for creating an embedded air gap that's not

1 located inside of trenches?

2 MR. CROSS: Objection. Form.

3 A. I don't recall if I did. But the
4 main places I cited this was with regards to
5 either Kim, where I was addressing a very
6 specific situation in the minus D2 direction,
7 and with regards to this Banerjee CVD
8 observation which I simply disagreed with and
9 wanted to get a nice clean reference to
10 refute that.

11 BY MR. KENYON:

12 Q. What does the process look like of
13 creating air cavities located inside
14 trenches?

15 MR. CROSS: Objection. Form.

16 A. First, that depends on the
17 process. I have multiple citations in here
18 that describe different ways of creating air
19 gaps. There's not only one way to do that.
20 In fact, somewhere in here I have a picture
21 on Page 47 of a self-assembled air gap
22 technique.

23 I also talk in 112 about
24 alternative techniques other than the ones I
25 talked about earlier like CVD techniques and

1 whatnot.

2 BY MR. KENYON:

3 Q. And so you're referring to
4 Exhibits 2009, 2010, and 2012?

5 A. At minimum, I'm referring to 2009,
6 2010, and 2012. There may be additional
7 exhibits, but those are the ones cited here.

8 Q. Why don't we go to Paragraph 111.

9 A. I'm there.

10 Q. In the first sentence, it's about
11 halfway through again. You say: Neither the
12 use of CVD nor the use of CMP necessarily
13 results in an isolation structure filled with
14 silicon dioxide or silicon nitride.

15 Do you see that?

16 A. I do.

17 MR. CROSS: Objection.

18 Mischaracterizes prior testimony.

19 BY MR. KENYON:

20 Q. What is an "isolation structure"?

21 A. So in the usage I have here where
22 I was not intending to define the term, but
23 simply attempt to describe something in a
24 general way, I'm meaning some structure that
25 provides electrical isolation between one

1 object and another.

2 Q. And the use of CVD could result in
3 an isolation structure filled with silicon
4 dioxide, right?

5 A. So there are certainly examples
6 described in the patents where CVD is used to
7 fill a structure and provide isolation. It's
8 not the only way to do that.

9 Q. Okay. Let's go to Paragraph 112.
10 First sentence you say: The use
11 of air gaps is a widely-researched area due
12 to the importance of capacitance reduction in
13 modern semiconductor technologies.

14 Do you see that?

15 A. I do.

16 Q. What do you mean by a
17 "widely-researched area"?

18 A. So in modern semiconductor
19 technologies, the dimensions decrease each
20 generation, and I'm sure you're well aware.
21 What this means is that the spacing between
22 things decreases each generation. The
23 spacing between things is what generates
24 capacitance.

25 30 years ago, people didn't worry

1 about most capacitances because they were
2 very small. In modern technologies, every
3 single one, every single wire, every single
4 conductive element has a capacitance to all
5 the adjacent elements, including ones that
6 may be not immediately adjacent but further
7 away.

8 So this is a huge issue because it
9 limits the speed and power of the modern
10 device. As a consequence, the hunt for how
11 to make capacitance lower is an incredibly
12 important economic driver for product
13 development.

14 And as I mentioned in earlier
15 testimony, the use of a fill material whose
16 dielectric constant or relative dielectric
17 constant can't go lower than 1.3 is a barrier
18 to dropping the capacitance even further.

19 And so as geometries have gotten
20 smaller, as the demands for product
21 applications continue to get more aggressive,
22 people are trying very hard to drop those
23 capacitance even further, and one of many
24 paths, but one of the very exciting paths, is
25 to simply get rid of the fill material and

1 leave just a hole there.

2 And one can debate whether the
3 hole is filled with a vacuum or nitrogen or
4 argon or whatever, but it's not filled with a
5 solid material.

6 Q. Were air gaps widely used in
7 semiconductor fabrication before July 2018?

8 A. They were certainly used.

9 Q. Were they used in commercial
10 manufacturing before July 2018?

11 A. I believe so. I can't cite to a
12 specific product simply because I've not
13 referenced that.

14 As I mentioned earlier, in work at
15 Intel, I was well aware that these things
16 were being worked on in 2013 and '14. I
17 simply don't have good knowledge of what was
18 going on in 2018 to say, well, products such
19 and so used these things.

20 Q. What do you mean "worked on"?

21 A. I mean that research and
22 development teams were running silicon wafers
23 in the factory on product material and
24 getting yield off of them.

25 Q. In the last sentence of

1 Paragraph 112, you mention a self-assembly
2 technique.

3 Do you see that?

4 A. I do.

5 Q. What do you mean by "self-assembly
6 technique"?

7 A. That is the name that the authors
8 of Exhibit 2012 called their technique. I'd
9 have to review the exhibit to remind myself
10 of the exact processing methodology they were
11 using.

12 Q. Is this technique directed to
13 creating air gaps for back end of line
14 interconnects?

15 A. Well, the picture certainly
16 suggests that.

17 Q. Why don't I provide you with 2012
18 so that you can confirm.

19 A. It is going to be in the chat?

20 Q. Yes.

21 A. Okay. I see it.

22 Q. I've entered into the chat what's
23 been marked Exhibit 2012 --

24 A. Okay. I have it. I have it open.
25 And I'm reminding myself of it.

1 MR. CROSS: Dr. Kuhn, just as a
2 reminder not to speak over Brooks.

3 BY MR. KENYON:

4 Q. So Exhibit 2012 is titled:
5 Performance and Reliability of Air Gaps for
6 Advanced BEOL Interconnects.

7 A. I see that.

8 Q. Do you recognize this document?

9 A. I do.

10 Q. What is "BEOL"?

11 A. Back end of the line.

12 Q. So this exhibit is directed to
13 creating air gaps for back end of line
14 interconnects?

15 A. That's correct.

16 Q. Was this technique commonly used
17 in -- or before July 2018?

18 A. So, first, let me check the date
19 of the paper.

20 So I can't answer that because I
21 don't know IBM's history on the use of this
22 technique and their products.

23 Q. Okay. Does Kim teach air gap for
24 back end of line interconnects?

25 A. Not to my knowledge.

1 Q. And regardless of what technique
2 you might use to create air gaps, does Kim
3 illustrate any air gaps in its figures?

4 A. If we're talking about the minus
5 D2 direction in Kim's Figure 24, it
6 illustrates nothing.

7 Q. I'm asking whether any figure of
8 Kim illustrates an embedded air gap.

9 A. Not that I recall.

10 Q. Going back to Paragraph 112, in
11 the second sentence you mentioned trade-offs.
12 Do you see that?

13 A. I see that.

14 Q. What do you mean by "trade-offs"?

15 A. As I mentioned earlier, the
16 development and manufacturing of modern
17 back-end processes is very complex. The
18 geometries are tight. The product demands
19 are large.

20 And experienced engineers spend
21 many years of their lives trying to, bluntly,
22 make everybody happy. To get the capacitance
23 down so that the designers are happy, to keep
24 the part from failing so that the yield and
25 reliability community are happy, to make the

1 manufacturing straightforward and cheap so
2 that the finance guys are happy. And all of
3 those challenges have to be balanced to
4 deliver a successful product.

5 Q. And what trade-offs exist?

6 MR. CROSS: Objection. Form.

7 A. Okay. That's a complex question.
8 I'll give a few examples, but, you know,
9 that's many people's day job for years on
10 end.

11 As I mentioned earlier,
12 capacitance is part of CB^2 dynamic
13 power. The lower your capacitance, the
14 better your power or the better your power
15 reduction, the more efficient your product.
16 Let me say that.

17 The question of reliability, if
18 you make things too tight or don't use enough
19 materials or put them under too high voltages
20 in order to make your product perform better,
21 you can have your product fail early.

22 If you are not mindful about how
23 you design your product and it has process
24 limitations embedded in it, you will have low
25 yield. There is a multiplicity of choices,

1 materials choices, process choices, and
2 layout choices that all have to play together
3 to successfully deliver a product, and none
4 of them are easy.

5 BY MR. KENYON:

6 Q. Okay. And you mentioned
7 reliability.

8 Are there any reliability issues
9 with embedding air gaps?

10 MR. CROSS: Objection.

11 A. There are reliability issues with
12 every process technology known. I haven't
13 done an extensive study on the reliability of
14 air gaps, but every single thing we do in the
15 process has certain reliability issues that
16 need to be understood.

17 BY MR. KENYON:

18 Q. Okay. Why don't we go to
19 Paragraph 124 of your declaration.

20 A. I'm at 124.

21 Q. In the second sentence, you say:
22 However, this description of the deposition
23 process does not acknowledge that CVD
24 deposition does not necessarily fill all
25 structures, and moreover, it can be

1 architected to not fill specific structures.

2 Do you see that?

3 A. I do.

4 Q. What do you mean by "it can be
5 architected to not fill specific structures"?

6 A. So that answer to that is actually
7 the next sentence: As I discussed earlier,
8 one of several methods to create air gaps in
9 trenches is taking advantage of the
10 nonconformity of a CVD dielectric layer to
11 create air cavities located inside trenches.

12 The reason I bring this up
13 here -- let me finish this one --

14 Q. Yeah, sorry.

15 A. -- because it's relevant to the
16 first part of the paragraph.

17 Dr. Banerjee expressly says that
18 it's an isotropic process leading to
19 deposition on all sides except the bottom
20 surface which is blocked. And he implies
21 that it's always completely filled with that
22 sentence.

23 And I disagree with that, and I
24 put out as an example the use of this
25 non-conformity of the CVD dielectric layer to

1 make air cavities, which is almost exactly
2 the opposite of what Dr. Banerjee is
3 describing.

4 Q. Okay. So when you state it can be
5 architected to not fill specific structures,
6 you are referring to creating air gaps and
7 trenches?

8 MR. CROSS: Objection. Form.
9 Mischaracterizes the prior testimony.

10 A. In this particular paragraph, I am
11 using air gaps as a way of illustrating that
12 Dr. Banerjee's statement is, in my opinion,
13 incorrect.

14 This particular paragraph is not
15 really using air gaps to describe
16 alternatives to creating insulation regions.
17 It's simply saying Dr. Banerjee made the
18 following statement, I disagree with that
19 statement, and by the way, I just gave you an
20 example of how to create air gaps that's
21 directly in conflict with Dr. Banerjee's
22 statement.

23 BY MR. KENYON:

24 Q. You agree, though, that CVD
25 deposition could fill all structures?

1 A. Actually, no.

2 MR. CROSS: Objection.

3 A. Having spent years using CVD like
4 techniques to fill STI very early in my
5 career, there are structures that CVD just
6 plain won't fill.

7 BY MR. KENYON:

8 Q. Well --

9 MR. CROSS: Dr. Kuhn, please
10 allow a little bit of time for me to
11 get in my objections.

12 THE WITNESS: My apologies.

13 BY MR. KENYON:

14 Q. Well, when referring to the
15 staircase structure of a memory device, would
16 you agree that a CVD deposition wouldn't
17 necessarily -- sorry. Strike that.

18 When referring to the staircase
19 structure of a memory device, would you agree
20 that the CVD deposition could fill the space
21 covering the staircase structure?

22 A. So the '031 Patent describes CVD
23 as one of the alternatives for a filling
24 structure above the staircase. So yes.

25 Q. Okay. Why don't we move to

1 Paragraph 129. And I want to direct you to
2 the last sentence. Let me know when you're
3 there.

4 A. I'm at the last sentence.

5 Q. Okay. You say: Simply put, Kim
6 and the '031 show different memory devices
7 with a different staircase design.

8 Do you see that?

9 A. I do.

10 Q. What do you mean by "different
11 staircase design"?

12 A. If you look at the beginning of
13 129 and the picture above, the first issue is
14 that Kim's stack -- Kim's staircase, I'm
15 saying this in a slightly different way,
16 extends only in the plus D2 direction.
17 There's no staircase in the D1 direction and
18 no staircase in the minus D1 direction.

19 Note also that alone is different
20 from what is described in the '031 Patent.
21 But note also that Kim's structure as
22 described above has these trenches that are
23 cut through the insulation layer after the
24 insulation layer is fabricated.

25 Q. Okay. I want to -- I want to --

1 putting the trenches aside because I want to
2 focus on the staircase design.

3 A. Okay.

4 Q. Is it your opinion that the
5 staircase design in Kim is different because
6 it does not disclose a staircase in the minus
7 D1 and plus D1 directions?

8 MR. CROSS: Objection. Form.

9 A. Keep in mind that Paragraph 129 is
10 directly responding to a petitioner's
11 statement that Kim's device is symmetric or
12 needs to be symmetric or requires symmetry.

13 And what I'm saying in this
14 paragraph is that Kim's device is not
15 symmetric. It only extends in one direction.
16 And '031 is showing a device which is
17 symmetric, which is shown as having both a
18 left and a right direction, and is described
19 as extending along the x-y plane.

20 So with this regard, these are two
21 different devices.

22 BY MR. KENYON:

23 Q. If Kim disclosed that a staircase
24 structure was etched on the left side of
25 this -- the memory device, the right side,

1 the front and the back, would it be the same
2 staircase design as the '031 Patent?

3 MR. CROSS: Objection to form.

4 A. If Kim modified the '031 -- sorry.

5 If Kim modified the structure to
6 look like what is disclosed and described in
7 the '031 Patent, then it would indeed be the
8 same as the '031 Patent.

9 BY MR. KENYON:

10 Q. I'm not sure you've answered my
11 question.

12 The last sentence of Paragraph 129
13 says that Kim in the '031 showed different
14 memory devices with a different staircase
15 design.

16 A. That's correct.

17 Q. Walk me through the differences
18 between Kim's staircase design and the '031
19 Patent staircase design.

20 MR. CROSS: Objection. Form.

21 A. So as I stated in 129, Kim's stack
22 structure extends in the D2 direction, does
23 not extend in the D1 direction, and it does
24 not extend in the minus D2 direction. That
25 differs from the '031 structure.

1 As a secondary point, which I
2 explained in 130, Kim discloses these
3 trenches that are formed after the filling of
4 insulation layer 110 such that the trench
5 openings and subsequent features divide the
6 stack into blocks, and those features are not
7 further described. The trenches are simply
8 left exposed.

9 So 132 actually may directly
10 address this question, which is even if it
11 were obvious to extend the insulating layer
12 110 in all directions, which I think is your
13 first question, is if there were staircases
14 on all four sides, there's still the issue
15 that in view of the trenches, Kim does not
16 disclose or render obvious that the stack
17 structures encircled by the filling
18 insulation 110.

19 BY MR. KENYON:

20 Q. So putting the trenches aside, if
21 Kim disclosed staircase structures on all
22 four sides, there would be no differences
23 between the staircase design in Kim and the
24 staircase design in the '031 Patent?

25 MR. CROSS: Objection. Form.

1 A. So first, I would -- that's a very
2 odd way to phrase the question. I would need
3 to look through Kim and see if there's other
4 or subtle differences. But in some sense, I
5 hear you saying that if the two most
6 distinguishing features between Kim and the
7 '031 Patent were magically removed, would
8 then Kim look more like the '031 Patent?
9 Well, sure, if we remove the two biggest
10 differences, it would sure look more like it.
11 Whether it looked exactly like it, I'd need
12 to go through Kim and look at it in more
13 detail.

14 BY MR. KENYON:

15 Q. Well, when you said in
16 Paragraph 129 that Kim in the '031 showed
17 different memory devices with a different
18 staircase design, I assumed you had something
19 in mind, right?

20 MR. CROSS: Objection. Form.

21 A. Yes, I had in mind that Kim is a
22 one-sided structure with trenches.

23 BY MR. KENYON:

24 Q. Okay. If Kim's stack structure
25 extended in the positive D2 direction, the

1 minus D2 direction, the plus D -- positive D1
2 direction, and the minus D1 direction, how
3 would its staircase design be different from
4 the '031 Patent staircase design?

5 MR. CROSS: Objection. Form.

6 A. Okay. So I'm going to start this
7 with the same answer I gave before.

8 What you're doing is creating a
9 hypothetical where you're removing from
10 consideration the two most significant
11 differences between the structure. And now
12 we're doing an analysis for features that are
13 perhaps less significant in the overall
14 question.

15 I do point out that Kim, as one of
16 many additional features, does not disclose
17 this double-decker stack that is disclosed in
18 the '031 Patent. I haven't looked at this in
19 detail, but off the top of my head, I don't
20 think Kim is disclosing the same type of
21 channel architecture or the same type of
22 pillar architecture or the multiplicity of
23 other things that are in the claims of '031
24 that we haven't discussed in detail on this
25 proceeding.

1 BY MR. KENYON:

2 Q. I'm trying to focus on the
3 staircase structure itself.

4 And so you've stated that there
5 are two significant differences, right?

6 A. I started this by saying there are
7 two differences that I'm highlighting as
8 significant between Kim and '031. One of
9 those differences is it's a one-sided
10 staircase. The other difference is that it
11 has these trenches. And this is all with
12 regards to the question of the isolation
13 region surrounding.

14 Clearly, Kim has a number of other
15 differences if we go claim by claim in
16 comparison with the '031 Patent. I have just
17 not gone through that detailed description in
18 this particular IPR.

19 Q. Are you done or did you
20 have anymore?

21 A. I think I'm done.

22 Q. I'm sorry. Okay. So you don't
23 provide any of those opinions in your
24 declaration?

25 MR. CROSS: Objection. Form.

1 A. I'm not opining in my declaration
2 on the hypothetical that if I made Kim
3 staircases on all four sides and if I removed
4 Kim's trenches, what are the differences now
5 between Kim and '031. I have not done that
6 analysis in this declaration.

7 BY MR. KENYON:

8 Q. Okay. Why don't we go to
9 Paragraph 131. And let me know when you're
10 there.

11 A. I'm there.

12 Q. You say: As depicted below, the
13 trenches TR are formed between the mold
14 structures MT used to form the steps.

15 Do you see that?

16 A. I do see that.

17 Q. And as support, you cite
18 Column 12, Lines 15 through 19 in Kim?

19 A. That's correct.

20 Q. Let's go to Kim Column 12,
21 Lines 15 through 19.

22 A. Hang on.

23 Q. Just let me know when you're there
24 and I will ask you a question.

25 A. Okay. I'm here.

1 Q. Kim does not use the phrase "are
2 formed," correct?

3 A. I believe it -- hang on. Kim
4 12:15 to 19, Kim uses the phrase "may be
5 formed" at the top of this. And at 15
6 to -- 15 to 19, I'll just cite it: A trench
7 TR may be defined between the mold structures
8 MT adjacent to each other. The trenches TR
9 may expose portions of the substrate. The
10 trenches may extend in parallel to the mold
11 structures MT in the second direction D2.

12 Q. So Kim does not use the phrase
13 "are formed" in Lines 15 through 19?

14 A. The phrase "are formed" does not
15 appear in Lines 15 through 19.

16 Q. Okay. Why don't we go to
17 Paragraph 141.

18 A. I have Paragraph 141.

19 Q. Okay. And I'm going to direct you
20 to the second to last sentence, so it's the
21 next page.

22 Let me know when you're there.

23 A. I'm there.

24 Q. Okay. You say: For this reason,
25 a material must have sufficient stiffness

1 and/or support functions to be considered as
2 a supporting material.

3 Do you see that?

4 A. I see that.

5 Q. And as support, you cite
6 Column 18, Lines 26 through 28?

7 A. That's correct.

8 Q. And that's in the '031 Patent?

9 A. That's in the '031 Patent.

10 Let me pull that up so we can look
11 at that together.

12 Q. Great. That was going to be my
13 next question.

14 A. Okay. 18:26 to 28.

15 Q. And when you're there, I'll ask my
16 question.

17 A. Okay. Hang on a second. I'm
18 still paging through.

19 Okay. I'm there.

20 Q. In Column 18, Lines 26 through 28,
21 the '031 patent does not use the phrase "must
22 have," right?

23 A. That was not the question I
24 expected so you're going to have to repeat
25 that so I can look.

1 Q. In Column 18, Lines 26 through 28,
2 the '031 Patent does not use the phrase "must
3 have," right?

4 A. Column 18, 26 through 30, the
5 phrase "must have" is not used.

6 Q. And it does say: Sufficient
7 stiffness and/or support functions.

8 Right?

9 A. It does.

10 Q. What does the '031 Patent mean by
11 "sufficient"?

12 A. So as I describe and, in fact,
13 this paragraph we're in, the material must
14 have sufficient -- and, I agree, must have is
15 not in the patent itself -- but in order to
16 be a supporting material, if it does not have
17 sufficient stiffness and/or support functions
18 to be considered a supporting material,
19 presumably it's not a supporting material
20 anymore.

21 So the must is somewhat implied in
22 the nature of significant stiffness and/or
23 support functions to be considered as a
24 supporting material.

25 Q. So the question that was pending

1 was: What does the '031 Patent mean by
2 sufficient?

3 So let's start there.

4 A. Okay. So the '031 Patent does
5 describe -- and I may need to hunt through
6 this -- does describe the importance of the
7 support -- mechanical support materials. And
8 in particular, I reference my own
9 Paragraph 141 where the '031 Patent is
10 describing the need to provide mechanical
11 support and prevent pattern collapse.

12 And that is 123 to 25 and 33 to
13 36, which we may want to look at first.

14 Q. Okay. Why don't we go there and
15 then I'll ask a question once you get there.

16 A. So the first place I'm going to go
17 is, hang on, 123 to 25.

18 Q. Go ahead.

19 A. And I'm not finding a clean cite
20 at 123 to 125, but I am at 133 to 136. So
21 let me read that one: To form this
22 multiple-stack memory device, supporting
23 pillars are used in the fabrication process
24 to provide mechanical support and prevent
25 pattern collapse.

1 Q. And what you just read is in the
2 background section of the '031 Patent?

3 A. It is in the background section,
4 but continuing in the summary, there are a
5 multiplicity of references to the supporting
6 pillar and what it's doing and how it's
7 operating.

8 Q. Okay. Why don't we go back to
9 Column 18, Lines 26 to 28.

10 A. I'm there. I'm there.

11 Q. Okay. What does the '031 Patent
12 mean by "sufficient"?

13 A. So my opinion as a POSITA would
14 read this as sufficient to not permit pattern
15 collapse or layer collapse.

16 Q. And does sufficient modify
17 stiffness or -- strike that.

18 Does sufficient modify stiffness
19 and support functions or just stiffness?

20 A. So if I go back to the problem
21 statement, from an engineering perspective
22 and from the perspective of a POSITA, the
23 problem statement is what is at the end of
24 that background section, which is: Provide
25 mechanical support and prevent pattern

1 collapse.

2 So then, if we look back to this
3 language here, we have significant stiffness
4 and/or support functions. And I would map
5 that to the problem statement that's earlier,
6 which is to -- and let me cite that
7 again -- to provide mechanical support and
8 prevent pattern collapse.

9 So those two materials'
10 properties, if I may say so, are mapped to
11 the desire to prevent the issues that are
12 described in the background section.

13 Q. What does the '031 Patent mean by
14 "stiffness"?

15 A. So stiffness is not quite a term
16 of art. Stiffness is usually mapped to
17 engineering metrics such as, for example,
18 Young's modulus.

19 Q. Does the '031 Patent explain what
20 stiffness means?

21 A. The '031 Patent does not explain
22 what stiffness means, but Dr. Banerjee
23 specifically mentions that he is using
24 Young's modulus as the primary metric for
25 stiffness, and I'm in agreement with that.

1 Q. Okay. And does the '031 Patent
2 explain what stiffness is sufficient?

3 A. Given the introductory background
4 sentence about pattern collapse and given a
5 POSITA's general knowledge that pattern
6 collapse is bad, the understanding would be
7 sufficiently stiff to not permit pattern
8 collapse and presumably not have yield or
9 reliability issues.

10 Q. What does the '031 Patent mean by
11 "support functions"?

12 A. Again, I think that goes back to
13 that sentence in the background that is
14 referencing mechanical support and prevent
15 pattern collapse.

16 Q. Does the '031 Patent provide any
17 other disclosure regarding support functions?

18 A. In the sense of -- this is a
19 clarification question.

20 In the sense of using the term or
21 in the sense of giving more detail on what
22 the support function is?

23 Q. What the support function means?

24 MR. CROSS: Objection. Form.

25 A. So support function is used

1 primarily in this one location at the patent
2 at 18, but, again, I point back to the
3 background section that is discussing the
4 known issue of pattern collapse and known
5 issues with mechanical support, particularly
6 in the staircase.

7 As the background section reads,
8 the problem arises because there's channel
9 holes in the stack, but there's no channel
10 holes out on the staircase. And so the
11 staircase is poorly supported resulting in
12 the structural issues.

13 BY MR. KENYON:

14 Q. In the next sentence of
15 Paragraph 141, you say that: Supported
16 materials, for example, can include copper,
17 cobalt, nickel, and aluminum.

18 Do you see that?

19 A. Hang on a second. I'm in the
20 patent.

21 Yes.

22 Q. And those examples come from the
23 '031 Patent?

24 A. Yes.

25 Q. What other materials would a

1 person of ordinary skill in the art consider
2 to be supporting materials?

3 A. So we have an interesting issue
4 here with how much a person of ordinary skill
5 in the art would know about the details of
6 mechanical support of semiconductor
7 structures. At the two- to three-year
8 experience level, bachelor in science in
9 engineering or appropriate level, a POSITA
10 would be familiar with Young's modulus, would
11 likely have had some level of understanding
12 of basic mechanics, but probably would not be
13 aware of the extensive detailed, technical
14 body of work that's been done in mechanical
15 support in semiconductors.

16 Q. Can we go to Claim 4 of the '031
17 Patent.

18 Sorry to keep jumping back and
19 forth between your declaration and the '031
20 Patent.

21 A. It's okay. Let me find Claim 4.
22 I have Claim 4.

23 Q. And Claim 4 requires a pillar
24 support material; is that right?

25 A. That's correct.

1 Q. Is it your position that the term
2 "a pillar support material" must have
3 sufficient stiffness and/or support
4 functions?

5 A. That's my position from the way
6 the patent has connected the pillar support
7 material to the stiffness and support
8 functions and to this pattern collapse issue
9 in the background section.

10 Q. And to go back to -- and, again,
11 sorry for jumping around -- but Column 18,
12 Lines 26 through 30.

13 A. Okay. I'm there.

14 Q. This is at least part of the
15 disclosure in the '031 Patent where -- or
16 what -- that supports your position that
17 connects pillar support material to stiffness
18 and support functions?

19 MR. CROSS: Objection. Form.

20 A. So I am referencing several
21 locations for my pillar support analysis.
22 This is one of them. The background section
23 describing the mechanical support and
24 collapse issues is another one.

25

1 BY MR. KENYON:

2 Q. And based on this portion of the
3 '031 Patent and the background section, is it
4 your position that a person of ordinary skill
5 in the art may not be able to identify a
6 pillar support material?

7 MR. CROSS: Objection.

8 Mischaracterizes prior testimony.

9 A. I believe the starting point for
10 this is you asked me if a POSITA would be
11 able to pick out, without any additional
12 information, a correct pillar support
13 material, and my response was a POSITA at
14 either Dr. Banerjee's definition or my
15 definition probably does not have the
16 extensive background required to select such
17 a material.

18 They could do a preliminary
19 analysis as I include in this report, but
20 they probably do not have the extensive
21 knowledge of all of the variety of materials
22 and manufacturing conditions that are
23 available.

24 So I think my testimony is that it
25 would not be -- a POSITA would not be able to

1 pick a material based on their own knowledge
2 without some additional guidance either from
3 a patent or a publication or information
4 within their own organization.

5 MR. KENYON: Okay. I think
6 we're getting pretty close to an hour.
7 Do you want to go ahead and stop here?

8 THE WITNESS: Yeah, I do. This
9 is a good stopping place. I also
10 noticed it was about an hour. And
11 perhaps more importantly, I noticed my
12 tea was empty.

13 MR. KENYON: Okay.

14 (A brief recess was held from
15 6:23 p.m. to 6:36 p.m.)

16 BY MR. KENYON:

17 Q. All right. I'd like to direct you
18 to Paragraph 143.

19 A. I'm there.

20 Q. In the sentence starting with
21 "rather," it's about halfway down --

22 A. I see that.

23 Q. -- you say: Kim's dummy
24 structures are formed of a single layer,
25 e.g., a silicone oxide layer, a silicon

1 nitride layer, a silicon oxynitride layer, or
2 a polysilicon layer.

3 Do you see that?

4 A. I see that.

5 Q. And you cite Column 13, Lines 33
6 through 36 in Kim for this statement?

7 A. Okay. I'm pulling that up.

8 Q. You cite Column 13, Lines 33
9 through 36; is that right?

10 A. I do cite that and I'm pulling
11 that up. Okay. I have that on the screen.

12 Q. Kim does not use the phrase "are
13 formed," correct?

14 A. Okay. That's correct. The quote
15 following the "are formed of a single layer
16 e.g.," that quote begins "formed of single
17 layer e.g.," it begins on Line 34 and then it
18 continues to match the quote all the way
19 down.

20 Q. And so prior to the word "formed,"
21 Kim actually says "may be formed"?

22 A. Let me check. 33. The entire
23 sentence is: The dummy pattern of the dummy
24 structures -- sorry. Let me do that again.

25 The dummy pattern of the dummy

1 structure DS may be formed of a single layer,
2 e.g., a silicon oxide layer, a silicon
3 nitride layer, a silicon oxynitride layer, or
4 a polysilicon layer.

5 Q. Let's switch back to your
6 declaration and turn to Paragraph 144.

7 A. I'm there.

8 Q. After the word "because," right
9 through the middle of Paragraph 144, you say:
10 Not all conductive (typically metal) cores
11 have the required stiffness and/or support
12 function to be considered a supporting
13 material.

14 Do you see that?

15 A. I see that.

16 Q. You do not cite the '031 Patent
17 for this statement, right?

18 A. I do not. This is an analysis.
19 I'm doing an extension.

20 Q. The '031 Patent does not use the
21 phrase "required stiffness and/or support
22 function," right?

23 A. That's correct. It uses simply
24 stiffness and/or support function.

25 Q. Does the '031 Patent explain how a

1 person of ordinary skill in the art would
2 determine which conductive cores have, as you
3 state, required stiffness and/or support
4 function?

5 A. The '031 Patent does not go into
6 detail on the technical analysis for
7 determining the required stiffness and/or
8 support function.

9 Q. Okay. Why don't we go to
10 Paragraph 151 of your declaration, and I want
11 to point you to Footnote 7.

12 A. I'm on 151, Footnote 7.

13 Q. In this footnote you say: The
14 '031 explains that the pillar support
15 material are metals such as copper, cobalt,
16 nickel, and aluminum.

17 Do you see that?

18 A. I see that.

19 Q. And you cite Column, 18 Lines 28
20 through 30 of the '031 Patent for this
21 statement?

22 A. That's correct. And we can check
23 those if you wish.

24 Q. Why don't we go there.

25 A. So that's 18. It's the last

1 sentence: For example, the support material
2 can include one or more of copper, cobalt,
3 nickel, and aluminum.

4 Q. So the '031 Patent does not use
5 the phrase "the pillar support material are
6 metals," correct?

7 A. It does not use that exact phrase,
8 that's correct.

9 Q. What does the '031 Patent mean by
10 "one or more"?

11 A. The '031 Patent does not explain
12 in detail what one or more means. But in the
13 context of the larger art, one or more of
14 copper, cobalt, nickel, and aluminum would
15 suggest either an alloy or a multilayer
16 structure.

17 Q. And what is an "alloy"?

18 A. An alloy is the combination of two
19 or more metals.

20 Q. And did you use the phrase
21 "multilayer structure"?

22 A. I did use that phrase, that's
23 correct.

24 Q. What do you mean by that?

25 A. It is not uncommon in the

1 semiconductor industry to layer materials on
2 top of each other to achieve particular
3 goals.

4 Q. And copper, cobalt, nickel, and
5 aluminum are not alloys in and of themselves?

6 A. Copper, cobalt, nickel, and
7 aluminum are elements.

8 Q. When you say "elements," you mean
9 elemental metals on the periodic table?

10 A. Yes.

11 Q. Let's go to Paragraph 172 of your
12 declaration. Sorry.

13 A. I'm looking. Yeah, I'm on 172.

14 Q. So in the first sentence, you
15 argue that: Petitioner and Dr. Banerjee
16 ignore significant issues of thermal
17 expansion mismatch.

18 Do you see that?

19 A. I see that.

20 Q. Does the '031 Patent mention
21 thermal expansion mismatch?

22 A. I don't believe it describes
23 thermal expansion mismatch.

24 Q. So it also does not explain how a
25 person of ordinary skill in the art would

1 consider thermal expansion mismatch when
2 choosing what material to use?

3 A. The patent does not describe that.
4 I do point out that that information is known
5 in the art.

6 Q. Why don't we go to Paragraph 184.

7 A. I'm at 184.

8 Q. You say Figures 6 and 7 of
9 Tessariol show that the staircase structure
10 is covered by insulating material 48, right?

11 A. Yeah, the first sentence is: As
12 shown in Tessariol's Figures 6 and 7, the
13 steps are covered by insulating material 48
14 from above and divided into stadiums by
15 landings 35 in the D2 direction.

16 Q. What do you mean by "cover by"?
17 Sorry, strike that.

18 What do you mean by "covered by"?

19 A. Well, as described and depicted in
20 Tessariol, 48 is above and -- is certainly
21 above and may be in direct contact with the
22 staircase.

23 Q. How would you deposit insulating
24 material 48?

25 MR. CROSS: Objection. Form.

1 A. How would I personally deposit it?

2 BY MR. KENYON:

3 Q. Sorry. How would a person of
4 ordinary skill in the art deposit insulating
5 48?

6 MR. CROSS: Objection. Form.

7 A. I don't believe Tessariol actually
8 provides guidance on this. Give me a second
9 to go figure that out.

10 I don't believe Tessariol provides
11 guidance. If we go to the broader community,
12 this would be somewhat the same type of list
13 we discussed in the '031 Patent: CVD
14 technologies, sputter technologies, ALD
15 technologies, and so on.

16 BY MR. KENYON:

17 Q. So one option would be conformal
18 CVD deposition?

19 A. That is a common technique that us
20 used in the art.

21 Q. Why does insulating material 48
22 not surround the staircase structure?

23 MR. CROSS: Objection. Form.

24 A. So there is no depiction or
25 description of the encircling activity for

1 the encircling property that is required for
2 surround.

3 BY MR. KENYON:

4 Q. What do you mean by the
5 "encircling activity"?

6 A. So as we discussed earlier, when
7 we talked about my claim construction or my
8 discussion of the word "surrounding," and I'm
9 not trying to reconstrue surrounding, by the
10 way. My point was it has a plain and
11 ordinary meaning. The plain and ordinary
12 meaning is encircling, and Tessariol is not
13 illustrating the material 48 encircling the
14 staircase region.

15 Q. Why not?

16 MR. CROSS: Objection. Form.

17 A. So let me turn this around. It
18 seems obvious to me it's not, so can you tell
19 me why you think it is encircling?

20 BY MR. KENYON:

21 Q. So why don't I rephrase the
22 question.

23 Does insulating material 48 cover
24 the staircase structures in Tessariol?

25 MR. CROSS: Objection. Form.

1 A. So each block of insulating
2 material 48 covers a different piece of the
3 staircase structure, but there is no
4 indication that I can see that any of these
5 blocks or that these blocks in combination
6 encircle the staircase.

7 BY MR. KENYON:

8 Q. Which staircase are we referring
9 to?

10 A. Any interpretation of the
11 staircase that is consistent with the '031
12 description, a filling structure surrounding
13 the multiple-stack staircase. I don't see
14 any place in Tessariol where a filling
15 structure is surrounding a multiple-stack
16 staircase.

17 Q. If we go to Page 77 of your
18 declaration, you annotate --

19 A. I'm actually on Page 77.

20 Q. Okay. You annotate Figure 6 of
21 Tessariol, right?

22 A. I do.

23 Q. If insulating material 48 is
24 deposited using conformal CVD deposition,
25 would it surround the staircase structures

1 34, 36, and 38?

2 A. No.

3 Q. Why not?

4 A. I see no place in this picture
5 that meets the condition of a filling
6 structure surrounding the multiple-stack
7 staircase structure. If you have an
8 alternate position, it would be good to draw
9 it and we can talk about it, but I don't see
10 that. I don't see any surrounding of the
11 multiple-stack staircase structure in this
12 image.

13 Q. Why don't we start with the
14 deposition of insulating material 48.

15 If insulating material 48 is
16 deposited using conformal CVD deposition,
17 would it look like Figure 6 or would there be
18 excessive dielectric material above the
19 staircase structures?

20 MR. CROSS: Objection. Form.

21 A. I'm not sure it matters as to what
22 it looks like initially. The patent is
23 describing it looking like Figure 6 when
24 you're all done.

25

1 BY MR. KENYON:

2 Q. When looking at Figure 6, does
3 insulating material 48 surround the staircase
4 structures in the D2 direction?

5 MR. CROSS: Objection. Form.

6 A. No.

7 BY MR. KENYON:

8 Q. Why not?

9 A. Because it does not meet the
10 definition of "surround" that we have
11 discussed with regards to encircling.

12 Q. What is it missing --

13 MR. CROSS: Objection.

14 BY MR. KENYON:

15 Q. -- in your mind as to why it's not
16 meeting the definition of "surround"?

17 MR. CROSS: Objection. Form.

18 A. So the encircling nature has not
19 been demonstrated, and the filling structure
20 surrounding the multiple-stack staircase
21 structure hasn't been demonstrated.

22 BY MR. KENYON:

23 Q. So you're using the word
24 "surrounding" to explain why it's not
25 surrounding.

1 I'm trying to understand
2 what -- why is the filling structure 48 not
3 surrounding the staircase structures 34, 36,
4 and 38 in the D2 direction?

5 MR. CROSS: Objection. Asked
6 and answered.

7 A. So I'm not using surrounding to
8 redefine surrounding. I am using the word
9 "encircling" as an alternative to
10 surrounding. And I see no place that this is
11 encircling.

12 If Dr. Banerjee or the petitioner
13 believed that this was encircling, there
14 should be a clear picture of why it's
15 encircling. And there's two conditions that
16 need to be met with regards this: The
17 surrounding needs to be clarified and the
18 multiple-stack staircase needs to be
19 clarified. And I don't see that here in
20 either of those limitations.

21 BY MR. KENYON:

22 Q. What do you mean by "the
23 surrounding needs to be clarified"?

24 A. So what you're doing is you're
25 having me look at Figure 6 and you're saying,

1 well, tell me why it's surrounding -- sorry,
2 why it is not surrounding, and I'm saying,
3 well, it's not encircling. There's no part
4 of Figure 6 that I see that's encircling.

5 If there is a belief that there is
6 an encircling characterization of this, then
7 I need a picture of it. Encircling means
8 something. It means on all sides of. Now,
9 we can talk about things being continuous or
10 whatever, but right at the moment, none of
11 these three structures are on all sides of
12 any of the individual staircases, much less a
13 multiple stack staircase.

14 Q. What sides are these three
15 structures on?

16 MR. CROSS: Objection. Form.

17 A. So that's --

18 MR. CROSS: Sorry.

19 Objection. Lacks foundation.

20 A. That's a hard question to answer
21 for two reasons. First is, the left and
22 right side of this structure just end. So
23 the ends of the structure aren't clear. If
24 we look at the staircases that are within the
25 structure, the staircases have two sides as

1 depicted in Figure 6, but they do not have
2 two sides with regards the contacts. And
3 give me a second here because I want to
4 illustrate another figure.

5 Hang on. I may have to pull it
6 out of the patent.

7 BY MR. KENYON:

8 Q. And what are you looking at right
9 now?

10 A. I'm looking at Tessariol, which I
11 can't pronounce correctly, and I'm looking
12 for a particular figure. And then I'm going
13 to take you to the part in my declaration
14 where I have that figure because I didn't
15 remember where it was.

16 Page 34.

17 Q. Of Tessariol or your declaration?

18 A. Page 34 of my declaration. And
19 I'm actually going to Fig 17 annotated as
20 sitting above my Paragraph 84.

21 Q. Okay.

22 A. So what we have here is Tessariol
23 has, and in this particular figure, has this
24 same stadium-style architecture and has
25 contacts only on one side. So in this

1 figure, you asked me, I believe, about the
2 left-hand side of the staircase; am I
3 correct?

4 Q. Sure. Why don't we stick with the
5 left-hand side for now.

6 A. Okay. Well, the left-hand side of
7 the staircase hasn't got any contacts on it,
8 so it's not active.

9 Q. Okay. And what about the
10 right-hand side?

11 A. Only the right-hand side of the
12 staircase is active. And I don't see any way
13 that this part of the staircase could be
14 interpreted as surrounding, if nothing else,
15 because 48 is broken into two pieces.

16 Q. What do you mean it's broken into
17 two pieces?

18 MR. CROSS: Objection to form.

19 A. If you look to the left-hand side,
20 there is four contacts on the upper part of
21 the staircase. If you look to the right-hand
22 side, there's four contacts on the lower part
23 of the staircase.

24 And if you look at the claim
25 language for '031, it's a filling structure

1 surrounding the multiple-stack staircase
2 structure. Well, you have two stadiums of 48
3 and I don't see how that fits the limitation
4 of filling structures surrounding the
5 multiple-stack staircase structure.

6 BY MR. KENYON:

7 Q. Talk me through that determination
8 as to why it does not fit the limitation.

9 MR. CROSS: Objection. Form.

10 A. So the filling structure
11 surrounding the multiple-stack staircase
12 structure needs to surround the staircase
13 structure and encircle it.

14 My opinion, which I did not opine
15 in the declaration, but my opinion looking at
16 this picture is this does not meet that
17 condition.

18 Q. So what sides of stair step
19 structure 36 are not encircled by filling
20 structure 48?

21 A. The staircase structure itself is
22 not encircled by 48.

23 Q. It's not encircled on any side?

24 A. It's not encircled --

25 MR. CROSS: Objection to form.

1 THE WITNESS: Sorry. I didn't
2 mean to interrupt you.

3 MR. CROSS: Go ahead.

4 A. The staircase structure here in
5 Figure 17 that we're discussing does not meet
6 a filling structure surrounding the
7 multiple-stack staircase structure.

8 If you folks think it does, then
9 you need to show how it is surrounding and
10 how it is surrounding the multiple-stack
11 staircase structure, and I see no place in
12 Dr. Banerjee's report or your petition where
13 you've done that.

14 BY MR. KENYON:

15 Q. I'm trying to understand what
16 sides of stair step structure 36 --

17 MR. CROSS: Objection. Asked
18 and answered.

19 BY MR. KENYON:

20 Q. -- are surrounded by filling
21 structure 48.

22 You cannot determine -- you cannot
23 tell me which sides are not -- are
24 surrounded?

25 MR. CROSS: Objection. Asked

1 and answered.

2 A. I've answered this question a
3 couple of times. And I realize my answer is
4 not satisfying you, but I have no other way
5 to answer this question other than what I've
6 opined in the report and what I've seen in
7 response to what Dr. Banerjee and the
8 petitioner has said.

9 The question you've asked is
10 outside of that scope.

11 BY MR. KENYON:

12 Q. So you cannot tell me which sides
13 of staircase structure 36 are not surrounded
14 by filling structure 48?

15 MR. CROSS: Objection. Form.

16 A. And that's correct, I cannot tell
17 you that because I cannot apply a surrounded
18 definition to this figure, period.

19 BY MR. KENYON:

20 Q. Why won't we go to Paragraph 185
21 of your declaration.

22 A. Okay. I'm at 185.

23 Q. So you say: Tessariol's
24 dielectric material 74 divides but does not
25 surround Tessariol's steps.

1 A. That's correct.

2 Q. Do you see that?

3 A. That's correct.

4 Q. What do you mean by that?

5 A. So Figure 11 is a topdown view of
6 Tessariol. You can see 74 is running
7 horizontal in the page with regards to
8 Figure 11. You can also see that this is
9 incomplete. This is some undefined piece of
10 the array, and we don't know what happens
11 above or below the array.

12 So the first problem is the
13 structure 74 only go in one direction. So
14 there is no indication that they extend in
15 the other direction. But there's a trench
16 present in the D1 direction. These things
17 going along the D2 direction, but there's no
18 discussion in Tessariol that there's some
19 other trench going the other way.

20 And moreover, Tessariol is really
21 not disclosing what's happening outside of
22 this range. Tessariol is not disclosing that
23 the stack is encircled in either direction
24 largely because it's not disclosing where the
25 end of this thing is.

1 Q. Could dielectric material 74 be
2 deposited using conformal CVD deposition?

3 A. I would assume dielectric
4 materials could be deposited using a variety
5 of different processed technologies.

6 Q. Let's go to Paragraph 189.

7 A. I'm there.

8 Q. You say: Tessariol's 'insulator
9 material 86' covers but does not surround
10 Tessariol's steps.

11 A. That's correct.

12 Q. Do you see that?

13 What do you mean by that?

14 A. So if you look at the figure on
15 the following page, the annotated figure on
16 the following page, that happens to be an
17 amalgam -- not an amalgam -- it happens to be
18 the simultaneous presentations of Figure 17
19 and 18. And these are actually annotated by
20 you guys, annotated by the petitioner. And
21 what you're pointing to is dielectric
22 structure 86 which is on top of everything.

23 And I think there's no debate that
24 dielectric structure 86 is covering the
25 entire area under discussion, but it's not

1 surrounding or encircling the staircase
2 structure. It's higher up. I agree that
3 it's surrounding a number of components that
4 are embedded in it, but it's above the
5 staircase structure.

6 Q. But you agree that insulator
7 material 86 could be deposited using
8 conformal CVD deposition?

9 A. I certainly agree that conformal
10 CVD deposition is one of many possible
11 techniques.

12 Q. I want to go to Paragraph 196.

13 A. Okay. I'm there.

14 Q. In the last sentence, you mention
15 that: There are a variety of well-known
16 techniques for creating embedded air gaps in
17 planarized structures.

18 A. That's correct.

19 Q. Do you see that?

20 A. Yep.

21 Q. And are those the techniques we
22 discussed earlier?

23 A. Yes.

24 Q. What you mean by "well-known"?

25 A. I mean these are techniques that

1 were published in the literature that may
2 appear in patents that have a high likelihood
3 of being in products.

4 Q. But you do not cite any
5 documentation or papers that show that
6 creating embedded air gaps occurs in
7 products?

8 A. Be aware that companies typically
9 are very cautious about publishing any
10 technique that gives them competitive
11 advantage. The lack of publications of
12 something in a product does not mean they're
13 not there.

14 Now, obviously, you can do reverse
15 engineering, you can do extensive analysis to
16 see what is in the product, but that is a
17 level of analysis that I have not done for
18 this project.

19 Q. So you do not cite any
20 documentation or papers that show that
21 creating embedded air gaps occurs in
22 products?

23 A. So I cited the papers that we
24 discussed earlier, and I also pointed out
25 that an air gap is disclosed in one of, I

1 believe, Micron's patents. If Micron is
2 patenting it, presumably they're doing it.

3 Q. Does Tessariol mention any
4 technique for creating embedded air gaps?

5 A. I don't believe so.

6 Q. Let's go to Paragraph 211.

7 A. Hang on a second.

8 I'm at Paragraph 211.

9 Q. So in the first sentence, you say:
10 While petitioner cites a reference that
11 discloses that copper was well-known, it is
12 also well known that copper poses significant
13 diffusion and contamination issues in the
14 processing of transistors and memory cells.

15 Do you see that?

16 A. I see that.

17 Q. So copper was a well-known
18 material used in semiconductor manufacturing?

19 A. So the transition to copper in the
20 back end of the line in 130 nanometers by
21 Intel and the earlier transition to copper by
22 IBM -- and I forgot what year it was, I
23 should know -- was a major change in the art
24 for exactly this concern.

25 Copper is an extraordinarily fast

1 diffuser and will kill transistors.

2 Q. And when did Intel implement
3 copper in the back of -- end of line?

4 A. 130 nanometers, give me a second
5 to figure the date on that. Probably early
6 2000s. I'd have to look that up.

7 Q. And then you mentioned copper by
8 IBM.

9 When did that occur?

10 A. That I would have to Google. I
11 have forgotten.

12 Q. Is it before July of 2018?

13 A. Yes.

14 Q. Would a person of ordinary skill
15 in the art understand how to address
16 diffusion and contamination issues that
17 copper poses?

18 A. Probably not.

19 Q. Why not?

20 A. Keep in mind that it took massive
21 efforts on the part of industry over a
22 multitude of years to figure out how to
23 manage copper diffusion.

24 The key issue here is the close
25 presence of copper to the transistors itself.

1 I do notice that the two patents that the
2 petitioner and Dr. Banerjee cite, which is
3 Patent '641 and Patent '725, neither one
4 places the copper near the memory cell.

5 In the case of '725, the copper is
6 above the cell. In the case of '641, the
7 copper is kind of a thermal pipe off to one
8 side.

9 While the community understands
10 through extensive effort some of the
11 techniques used to mitigate copper diffusion,
12 these are very difficult and complex
13 techniques that would not necessarily be
14 known to a POSITA with only a bachelor's
15 degree and two years of practical experience.

16 Q. The '031 Patent identifies copper
17 as an example of a pillar support material,
18 right?

19 A. It does.

20 Q. Does the '031 Patent explain how a
21 person of ordinary skill in the art would
22 address diffusion and contamination issues
23 with copper?

24 A. It does not, but I do point out
25 that the listing of copper in the '031 Patent

1 gives a POSITA an indication that copper is
2 successful in that location.

3 One of the important points here,
4 in copper as a whole, is how far the copper
5 is from the actual transistor. And the '031
6 Patent with regards to the copper is focused
7 on a location that is out on the staircase.

8 Q. Okay. And the '031 Patent does
9 not explain how a person of ordinary skill in
10 the art would address any sort of diffusion
11 and contamination issues with respect to any
12 material, right?

13 A. It is assumed that a patent is
14 enabled, and thus, it is assumed that the
15 core materials listed in the patent will work
16 in the location that's described.

17 Q. Okay.

18 MR. KENYON: No further
19 questions.

20 MR. CROSS: Why don't we take a
21 15-minute break. I'll take a look at
22 my notes and come back.

23 (A brief recess was held from
24 7:14 p.m. to 7:30 p.m.)

25 CROSS-EXAMINATION

1 BY MR. CROSS:

2 Q. Hi, Dr. Kuhn. If you don't mind,
3 can we turn to Exhibit 1001.

4 A. And just to clarify, that's the
5 patent itself. And where would you like me
6 to go?

7 Q. If you can go to the Column 1.
8 Do you remember Mr. Kenyon asking
9 you about the language that appears at
10 Column 1, Lines 34 through 36?

11 A. I do.

12 Q. Does any of that language mention
13 forming supporting pillars through the
14 multiple-stack staircase structure?

15 MR. KENYON: Objection. Form.

16 A. No. The language, itself, simply
17 says: To form this multiple-stack memory
18 device, supporting pillars are used in the
19 fabrication process to provide mechanical
20 support and prevent pattern collapse.

21 It's not that specific.

22 BY MR. CROSS:

23 Q. And does this part of the
24 background section mention forming supporting
25 pillars through the filling structure?

1 A. It does not --

2 MR. KENYON: Objection. Form.

3 A. No, it does not.

4 BY MR. CROSS:

5 Q. And we can turn to Column 6,
6 Lines 17 through 25.

7 A. I'm here.

8 Q. That first sentence does not
9 inform you how the patent uses the term
10 "substrate"?

11 A. Yes, it does, and I will read the
12 sentence for the record.

13 As used herein, the term
14 "substrate" refers to a material onto which
15 subsequent material layers are added. The
16 substrate itself can be patterned. Materials
17 added on top of the substrate can be
18 patterned or remain unpatterned.

19 Q. And is this your understanding
20 that you applied when analyzing the patents
21 in the prior art?

22 MR. KENYON: Objection. Form.

23 A. Yes.

24 BY MR. CROSS:

25 Q. If we could turn to Column 22,

1 Lines 27 through 32.

2 A. Sorry. Repeat that?

3 Q. You can turn to Column 22,

4 Lines 27 through 32.

5 A. 22:27 to 32.

6 Q. That's right.

7 A. I'm there.

8 Q. Does the '031 explain that the
9 first staircase region and the second
10 staircase region on Figure 11 surround memory
11 structure 1100 along the x-y plane?

12 A. Yes, it does.

13 MR. KENYON: Objection. Form.

14 A. The language there is first
15 staircase region 1121 and second staircase
16 region 1122 can each surround memory
17 structure 1100 along the x-y plane.

18 BY MR. CROSS:

19 Q. And uses the word "surround"
20 expressly, correct?

21 A. That's correct.

22 Q. And that's to describe this
23 particular configuration, correct?

24 A. That's correct.

25 Q. Are you aware of whether the '031

1 Patent ever described a memory device with
2 staircase regions along only one axis as
3 surrounding the memory device?

4 MR. KENYON: Objection. Form.

5 A. I'm not aware of that location or
6 that reference.

7 BY MR. CROSS:

8 Q. Okay. If we could turn to
9 Exhibit 1005, which is Kim.

10 A. Uh-huh. I'm in Kim.

11 Q. Okay. Please turn to Figure 4A.
12 Sorry, I have to turn to Figure 4A.

13 A. I have Figure 4A up.

14 Q. Can you identify the word lines in
15 this figure?

16 A. Yes, I can. They're the
17 horizontal lines throughout the figure and
18 they're the cross-etched ones.

19 Q. Okay. And does each of these word
20 lines in the staircase region have a contact?

21 A. Yes, it does.

22 Q. If that's the case, is there any
23 reason to have any other staircase regions
24 with word line contacts to these word lines?

25 A. No, it's not.

1 MR. KENYON: Objection. Form.
2 Leading.

3 A. Okay. But let me address the
4 question.

5 The staircase as identified in
6 Figure 4A has a contact on every single one
7 of the gates. And that means that there is
8 no need to have an additional staircase
9 anywhere else.

10 BY MR. CROSS:

11 Q. If we can turn to Exhibit 1015.

12 A. Okay.

13 Q. Do you recall discussing this
14 patent with Mr. Kenyon?

15 A. Yes. Yes, I do.

16 Q. Who is the applicant of this
17 patent?

18 A. Micron.

19 Q. Okay. And at indicator 63, can
20 you tell me what the continuation -- strike
21 that.

22 Indicator 63, does this patent
23 continue from an earlier patent?

24 A. It does indeed. It's continuation
25 of Application Number 13,450,299 filed on

1 April 18, 2012, which is now Patent
2 10,504,596.

3 MR. CROSS: Thank you.

4 No further questions.

5 MR. KENYON: No further
6 questions.

7 (Thereupon, the proceedings
8 concluded at 4:36 p.m.)
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CERTIFICATE OF REPORTER

UNITED STATES PATENT AND TRADEMARK OFFICE)
PATENT TRIAL AND APPEAL BOARD)

I, ERICA FIELD, RDR, CRR, certify that I
was authorized to and did stenographically
report the deposition of KELIN KUHN, pages 1
through 265; that a review of the transcript
was not requested; and that the transcript is
a true and complete record of my stenographic
notes.

I further certify that I am not a
relative, employee, attorney, or counsel of
any of the parties, nor am I a relative or
employee of any of the parties' attorney or
counsel connected with the action, nor am I
financially interested in the action.

DATED this 2nd day of April, 2025.



Erica Field, RDR, CRR