

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,

Petitioner,

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,

Patent Owner.

Case No.: IPR2024-00790
U.S. Patent No. 10,868,031

PATENT OWNER'S SUR-REPLY

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LIST OF EXHIBITS

Exhibit	Description
Ex. 2001	New Oxford American Dictionary, 3 rd Ed., 2010
Ex. 2002	The American Heritage® College Dictionary, 3 rd Ed., 2000
Ex. 2003	Webster’s II New College Dictionary, 3 rd Ed., 2005
Ex. 2004	Merriam-Webster’s Dictionary and Thesaurus, 5 th Printing, 2014
Ex. 2005	Declaration of Jonathan Bradford
Ex. 2006	Deposition Transcript of Dr. Banerjee
Ex. 2007	Micron’s Preliminary Claim Constructions (District Court)
Ex. 2008	Plaintiff’s Proposed Claim Constructions (District Court)
Ex. 2009	Gosset, “General review of issues and perspectives for advanced copper interconnections using air-gaps as ultra-low K material” (2003)
Ex. 2010	Harada, “Extremely Low Keff (1.9) Cu Interconnects with Air Gap Formed Using SiOC” (2007)
Ex. 2011	Ashby, Michael, “Materials Selection in Mechanical Design, Chapter 4, Material Property Charts” (4 th Ed. 2011)
Ex. 2012	Nitta, “Performance and reliability of airgaps for advanced BEOL Interconnects” (2008)
Ex. 2013	January 17, 2025, Declaration of Dr. Kuhn (“Kuhn”)
Ex. 2014	Electrical Conductivity, Wolfram Research
Ex. 2015	Young’s Modulus, Wolfram Research
Ex. 2016	Thermal Expansion Coefficients, Wolfram Research

LIST OF ABBREVIATIONS

Abbreviation	Term
'031	U.S. Pat. No. 10,868,031
'031FH	File History of U.S. Pat. No. 10,868,031
Board or PTAB	Patent Trial and Appeal Board
Challenged Claims	'031 patent, Claims 1-5
DI	Decision Granting Institution for <i>Inter Partes</i> Review of U.S. Patent No. 10,868,031 (IPR2024-00790, Paper 9)
Kim	U.S. Patent No. 10,381,369
Office or USPTO	U.S. Patent and Trademark Office
Parallel district court litigation	<i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc.</i> , NDCA-3:23-cv-05792 (N.D. Cal.)
Patent Owner or PO	Yangtze Memory Technologies Co. Ltd.
Petition or Pet.	Petition for <i>Inter Partes</i> Review of U.S. Patent No. 10,868,031 (IPR2024-00790, Paper 1)
Petitioner	Micron Technology, Inc.
POR	Patent Owner Response for <i>Inter Partes</i> Review of U.S. Patent No. 10,868,031 (IPR2024-00790, Paper 12)
POSITA	Person of ordinary skill in the art
Reply	Petitioner's Reply for <i>Inter Partes</i> Review of U.S. Patent No. 10,868,031 (IPR2024-00790, Paper 14)
Tessariol	U.S. Patent Publication No. 2019/0081061

I. INTRODUCTION

Petitioner's Reply fails to address the issues raised in the POR, misunderstands the prior art, and misrepresents PO's positions. In addition, the Reply introduces new arguments, which are not only flawed in logic and fact, but also should be rejected as Petitioner is not allowed to broaden its case beyond the original Petition. 37 C.F.R. § 42.23(b); *Henny Penny Corp. v. Frymaster LLC*, 938 F.3d 1324, 1330-31 (Fed. Cir. 2019) (rejecting attempts to broaden the petition's ground in its reply). The validity of all Challenged Claims should be upheld.

The Board should continue to apply its preliminary construction construing "surrounding" to mean "encircling." Petitioner fails to address PO's and the Board's support for the construction, which is consistent with the plain meaning of the term in light of the intrinsic evidence. POR, 15-17; DI, 8, 11.

Under that construction, the two references relied on in the Grounds (Kim and Tessariol) do not disclose or render obvious "a filling structure surrounding the multiple-stack staircase structure," as claim 1 requires. At most, Kim teaches that insulating material (the alleged filling structure) covers the top and one side. Of the remaining three sides, trenches are subsequently formed on two sides to remove the alleged filling structure, and the third side is never shown or described. Tessariol's disclosures fail for similar reasons as it does not describe or show the cited insulating materials as encircling the staircase.

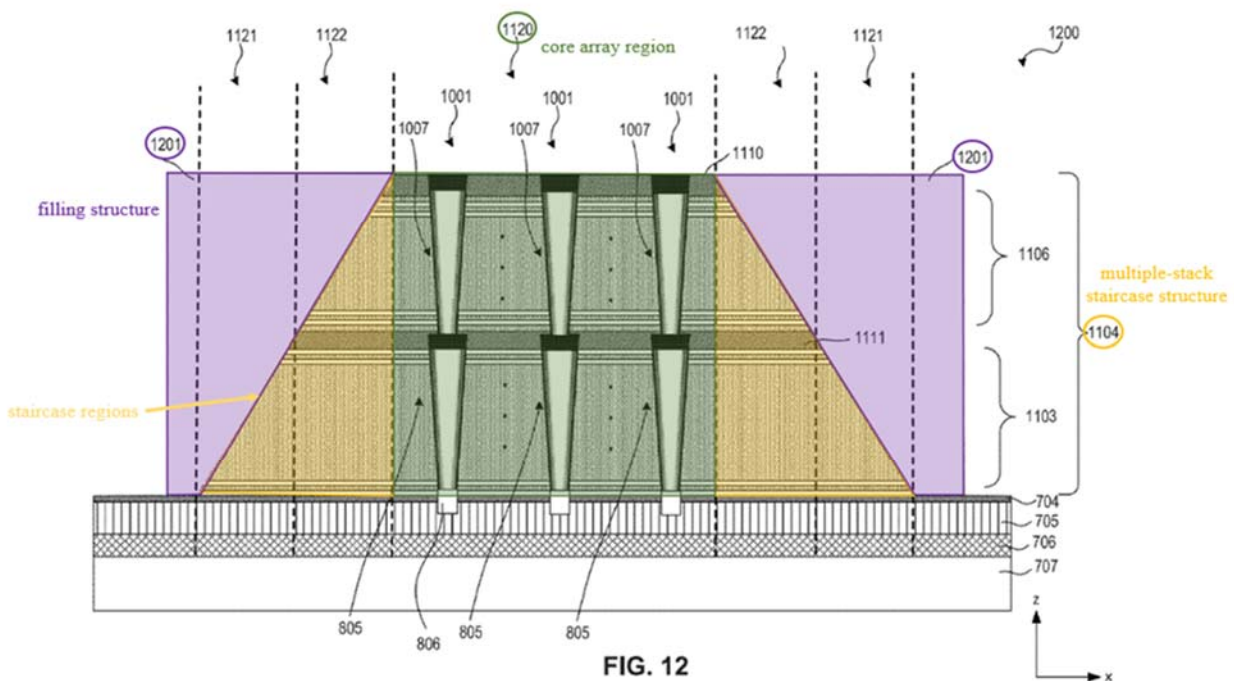
Furthermore, neither Kim nor Tessariol discloses or renders obvious “a supporting pillar [that] is filled with ... a pillar-support material surrounded by the insulating material,” as claim 4 requires. Kim does not even disclose a conductive core, and Petitioner’s hindsight-based obviousness arguments for both references are flawed.

II. “SURROUNDING” MEANS “ENCIRCLING”

The Board should sustain its preliminary construction of “surrounding” to mean all the way around (something)—in other words, encircling. DI, 11-12; POR, 14-19. As explained in the POR and the DI, dictionary definitions confirm this plain meaning, claim 1 uses “surrounding” instead of narrower alternatives such as “covering” or the concept of being “between” two structures, and the ’031 specification describes the filing structure extending in the x-y plane—thus encircling in all directions along the x-y plane. POR, 15-17; DI, 8, 11. Petitioner ignores this key evidence and does not even propose its own construction.

Petitioner instead argues that the specification does not support “encircling” because it allegedly “does not teach or illustrate the filling structure ‘deposited to,’ e.g., the ‘back’ and ‘front’ (i.e., the y-direction in Fig. 3) of the staircase” (Reply, 2-4), but again, Petitioner ignores the cited evidence. For example, as depicted below, the staircase structure that is surrounded extends in the +x and -x directions. In addition, the staircase structure extends in +y and -y directions (into and out of the

page), thus forming “*staircases extending along the x-y plane*” (’031, 13:27-28) and showing staircases surround the stack. The filling structure “fill[s] [the] space formed by the formation of the staircase structure” and thus surrounds the staircase structure. ’031, 13:13-17.



’031 Patent, Fig. 12 (annotated); POR 15-17. Petitioner does not address the above disclosures. The fact that the filling structure is “deposited” to fill the space formed by the formation of the staircase structure, as noted by Petitioner (Reply, 3), does not diminish the fact that the specification further taught to “surround” the staircase structure in the x-y plane.

Finally, Petitioner argues that if there is any support for PO’s construction, it must have been known in the art to use such techniques (Reply 4), but PO’s

construction doesn't rely on these supposedly known techniques. And as further discussed below, in contrast to the '031, the cited art does not teach "surround[ing]" or depositing material on all sides. In short, the very claim construction evidence that Petitioner ignores is not present in the cited art, and thus Petitioner's misguided attempt to link the two separate issues fails.

III. GROUND 1: KIM (CLAIMS 1-4)

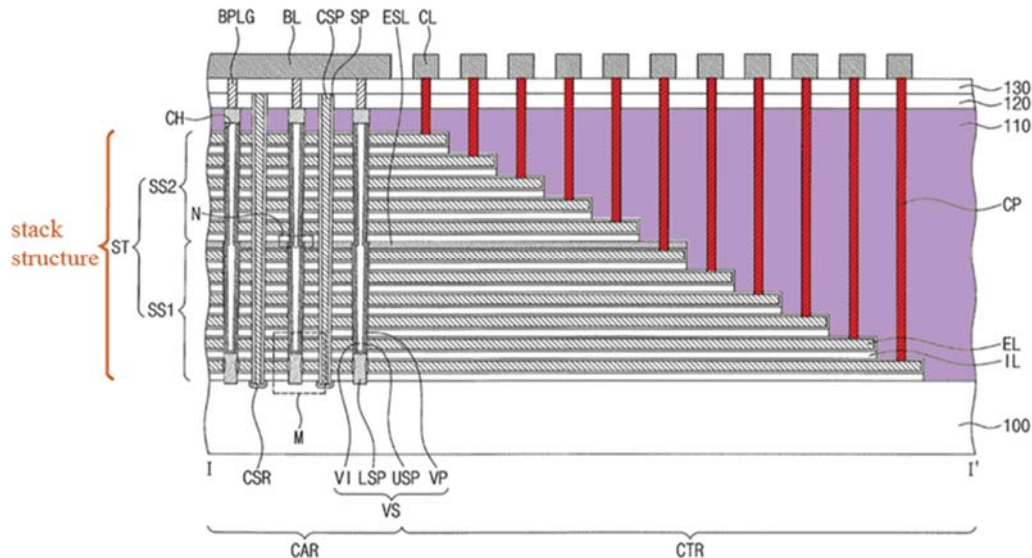
Kim fails to disclose or render obvious the Challenged Claims at least because, under the proper construction of "surrounding" as "encircling" (§II), Kim fails to disclose or render obvious limitation [1.d] of the sole challenged independent claim. Kim also does not disclose or render obvious a "supporting pillar" with a "pillar-support material," as required by dependent claim 4.

A. Independent Claim 1: Kim Does Not Disclose or Render Obvious That Its Filling Insulation Layer "Surrounds" the Stack Structure

Kim does not disclose or renders obvious "a filling structure surrounding the multiple-stack staircase structure," because, at most, Kim teaches that its **filling insulation layer 110** (the alleged filling structure) covers the top and one side of its stack structure (as shown in Fig. 4A below), but does not "surround" or encircle the stack structure. Instead, Kim discloses that at least two sides of the stack structure are instead cut by trenches formed after the insulation material has already been deposited (the +D1 and -D1 directions), and a third side (the -D2 direction) is simply

not shown or described in Kim. Neither Petitioner's original arguments nor its improperly-introduced new arguments cure Kim's deficiencies.

FIG. 4A



Kim, Fig. 4A (annotated); *see also* Kim, Fig. 4B.

1. The Board Did Not Already Find that Kim’s Filling Insulation Layer “Surrounds” the Stack Structure

Petitioner begins by misrepresenting the Board’s finding at institution, falsely asserting that “[a]s the Board correctly found (DI, 15-17 (citing Kim, 10:17-20)), by forming an insulating material on the entire substrate (via, e.g., CVD) to cover the stack, the insulating material **would necessarily encase the memory device** and, thus, surround the staircase structure” (emphasis original). Reply, 5. The Board made no such finding and never stated that the material would “necessarily” surround the staircase structure. Instead, the Board in its preliminary analysis under the

reasonable likelihood standard noted that PO's pre-institution arguments, which had not yet been supported by Dr. Kuhn, were not from the vantage point of a POSITA. DI, 17-18. Now, however, Dr. Kuhn has explained why the usage of CVD does not necessitate an isotropic deposition and a full encasing of the device—because, for example, it was common to use CVD to create air-gaps—and does not disclose or render obvious a filling structure “surrounding” a multiple stack staircase structure. Kuhn, ¶¶110-112, 124-126. In addition, the Board did not yet have an opportunity consider the additional arguments raised in the POR.

Contrary to Petitioner's suggestion (Reply, 5-6), Dr. Kuhn never stated that CVD necessarily results in coverage of the entire surface of the substrate, and instead testified why it does not. For example, Dr. Kuhn testified that CVD is also used to leave air-gaps intentionally. Ex. 1026, 57:3-58:8 (discussing creating air-gaps), 58:23-59:24 (discussing creating holes varying sizes with voids inside), 60:1-14 (discussing air-gap creating as an established practice), 211:17-212:3 (disagreeing with Dr. Banerjee about CVD being an isotropic process leading to deposition on all sides). Dr. Kuhn also identified the use of air-gaps in 3D NAND technology in one of Petitioner's exhibits. Ex. 1026, 74:4-76:5 (discussing Ex. 1015, 10:57-59, which reads: “The gate-slit openings 228A can be left as an air-gap or filled with various types of dielectric material, such as, for example, silicon dioxide.”).

Even in the testimony Petitioner quotes, Dr. Kuhn was referring only to a “*conformal* CVD process,” which was “*assuming it’s a conformal deposition*” and “assuming...it’s the correct kind of CVD—again, *there’s a myriad of ways to do this*” (emphasis added). Ex. 1026, 101:5-12. Even then, in that specific use of CVD among many, Dr. Kuhn merely acknowledged that it would create a blanket layer across the wafer—not that the deposited layer would surround the staircase structure. That would still depend, for example, on the topography and structures surrounding the other sides prior to CVD, which Kim does not show. As a result, contrary to Petitioner’s assertions, a teaching of CVD by itself does not teach a surrounding filling structure, and Kim’s disclosure of CVD does not disclose a filling structure “surrounding” a multiple-stack staircase structure.

Finally, even if CVD were used in the manner argued by Petitioner, this argument further ignores the trenches that are formed on two sides after the insulation layer is deposited, which prevent the insulation layer from “surrounding” the stack structures. See *infra* §III.A.4; POR, 27-30.

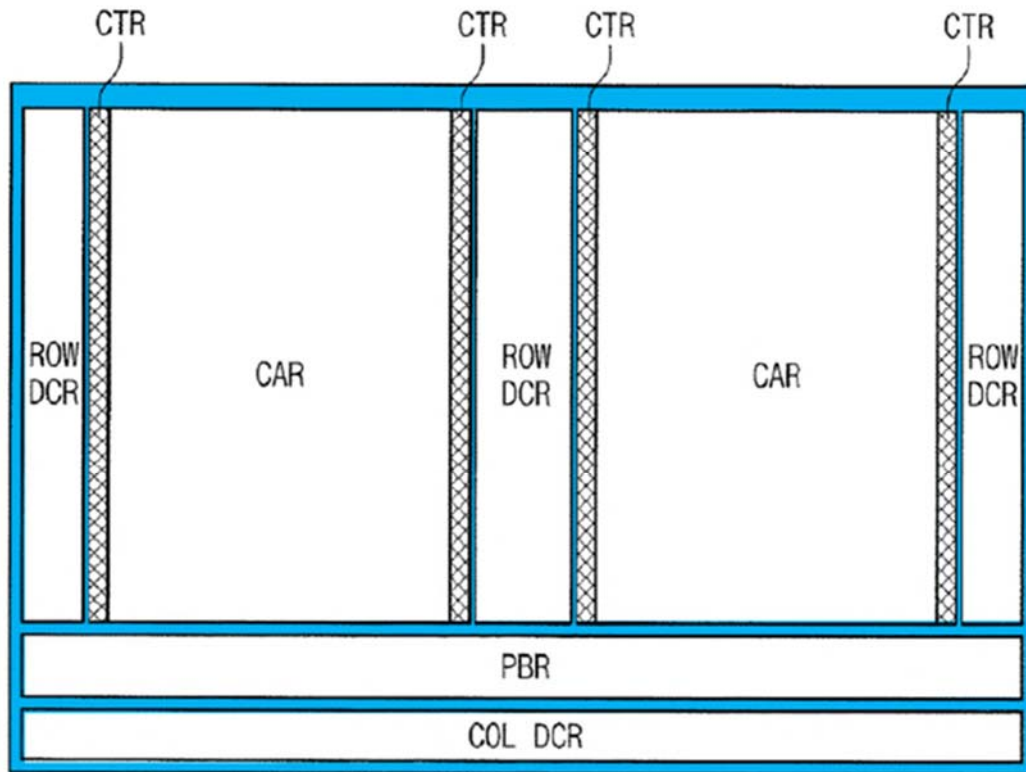
2. Petitioner’s New Figure 1 Argument Similarly Fails

Petitioner next introduces an improper new claim mapping on reply by referencing Kim’s Fig. 1 for the first time and asserting that it shows “forming various regions on a substrate so as to leave room to deposit filling material that completely encircles the staircase regions” (Reply, 6-7). As an initial matter, this is

an improper new argument that should have been “presented earlier” in the Petition. *See Ariosa Diagnostics v. Verinata Health Inc.* 805 F.3d 1359, 1364 (Fed. Cir. 2015); PTAB Consolidated Trial Practice Guide 2019, at 73. The claim mapping presented in the Petition does not rely on the blue-shaded areas in Fig. 1 (reproduced below from Reply, 7) as the alleged filling structure. Compare, *e.g.*, Petition, 32-38 and Reply, 7. PO’s expert was not given an opportunity to address this new argument as new evidence is not permitted in the Sur-Reply. 37 C.F.R. §42.23(b). Regardless, Petitioner’s new argument does not show filling structure surrounding the multiple-stack staircase structure.

The likely reason Petitioner did not rely on Figure 1 before is that it shows a “schematic block diagram,” depicting general regions of the device, as opposed to the “plan view” or “cross-sectional view” figures (Kim, 4:18-48), which are intended to show the structure and spatial relationships of various elements. Indeed, Fig. 1 does not label the blue-shaded region or otherwise indicate that it is a structure in the actual device (in contrast, other regions like the CAR and CTR are labeled).

FIG. 1



Kim, Fig. 1 (annotated by Petitioner at Reply, 7). Fig. 1 also does not label the substrate or provide any indication that Petitioner's blue-shaded region is the substrate on which the filling insulation layer is formed. Instead, Kim first describes "substrate 100" in connection with Fig. 3, which is a "plan view" as opposed to a "schematic block diagram." Kim, 4:18-20, 5:53-55. As such, the blue-shaded region in Fig. 1 does not teach what Petitioner asserts.

Based on its assertion that the CAR and CTR regions do not extend to any substrate edge (Reply, 7-9), Petitioner argues that there necessarily would be bare

substrate bordering any region and implies that the bare substrate would be covered by the filling structure (Reply, 7-9), but even assuming there are there are adjacent regions that require isolation in the +D1 and –D1 directions (perpendicular to Fig. 4A), or the –D2 direction (to the left in Fig. 4A), Kim does not teach a filling structure for that isolation. POR, 25-31. As explained in the POR, there are multiple reasons that Kim does not show the insulation layer covering the side of the staircase structure in those directions. For example, Kim teaches trench cuts through the staircase in the +D1 and –D1 directions. POR, 27; Kuhn, ¶¶99-100. Second, Kim does not show the structure in the –D2 direction and multiple semiconductor processes produce an unfilled edge. POR, 27; Kuhn, ¶101. Kim’s specification provides limited information about the “filling insulation layer,” which does not support Petitioner’s argument that it must surround the stack—instead it says only that the layer “cover[s]” the stack on top. Kim, 9:53-58, 11:11-15.

3. Petitioner’s Attempt to Analogize the ’031’s Disclosures to Kim’s Ignores Key Distinctions

Petitioner incorrectly asserts that “Kim discloses the same type of ‘surrounding’ that the ’031 patent discloses” (Reply, 9-10). As discussed in §II, the ’031 discloses, specifically, that the filling structure “*surrounds*” the staircase structure, and that the staircase structure extends all four directions in the x-y plane. POR, 15-17. In contrast, Kim teaches only that its filling insulation layer that it is

disposed or *formed on* some structures to *cover* them, not that the filling insulation layer *surrounds* anything, and Kim has a different staircase structure, which does not surround the stack in the x-y plane. Petitioner wrongly asserts that PO relies solely on Figures 4 and 12 of the '031 to show “surrounding” (Reply, 10-13), but the POR and §II above instead rely on the combination of Figs. 4 and 12 with express disclosures in the specification regarding the x-y plane. POR, 15-17. As Dr. Kuhn testified, with “***It is the additional information, the specification, that clarifies that there is an x-y plane here and staircases extending along both of those directions in the x-y plane.***” Ex. 1026, 134:3-11. Thus, Petitioner’s attempt to conflate these two different issues fails.

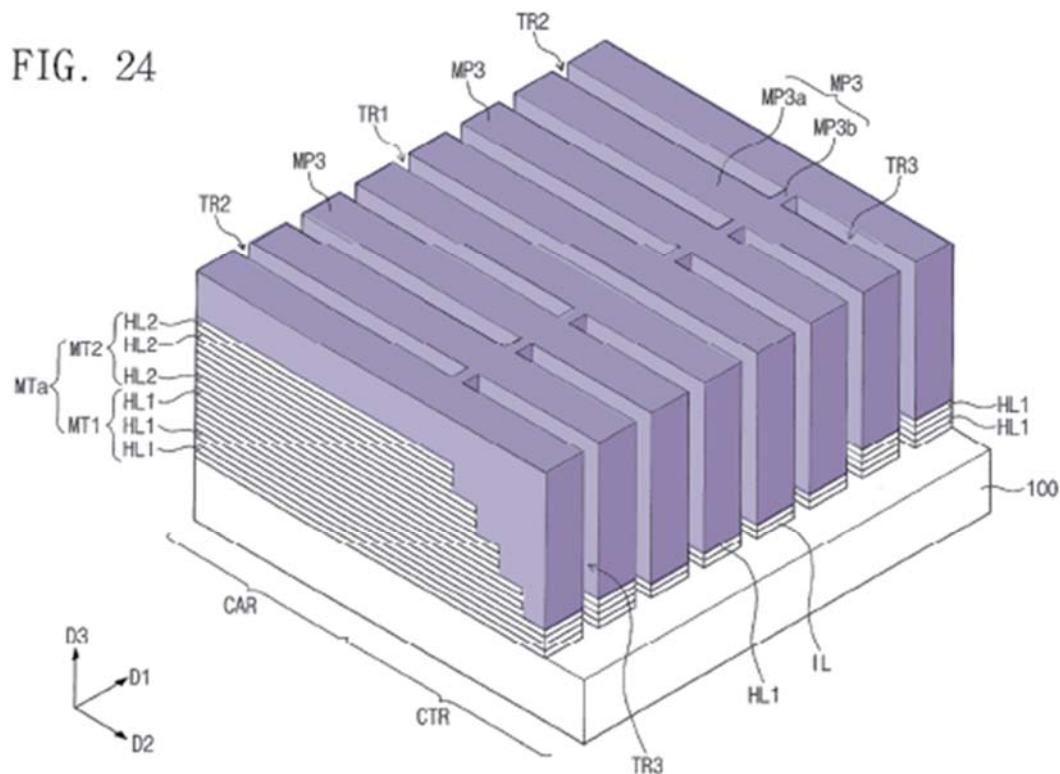
Petitioner’s attempt to equate Kim’s disclosures to '031 quotations regarding CVD and planarization (Reply, 13) fail for similar reasons. Unlike Kim, the '031 teaches “surrounding” (*e.g.*, 13:44-48), and that the staircase structure extends in the x-y plane (*e.g.*, 13:27-28). Petitioner repeatedly ignores these differences between Kim and the '031. Petitioner asserts it would be error to require the prior art to “use the word ‘surrounding’” (Reply, 13), but PO has never argued that Kim must use that word. Rather, Kim fails to disclose or render obvious the concept that is claimed regardless of the particular terminology that is used.

4. Kim's Trenches Further Demonstrate That the Filling Insulation Layer Does Not "Surround" the Stack Structure

As explained in the POR, Kim's filling insulation layer fails to extend in the -D1 and +D1 directions, because it is cut by trenches. POR, 27-30. In response, Petitioner asserts that "forming 'trenches' is merely an optional embodiment" since Kim uses the word "may" (Reply, 13-14), but Kim never describes the device without them—all of Kim's disclosed embodiments, including the embodiment relied upon by Petitioner, include trenches. Moreover, the word "may" is used throughout Kim to describe virtually all of Kim's teachings (it is used 368 times) and thus could not mean that any component that is described with the word "may" is optional. Petitioner also asserts that "even if Kim requires 'trenches,' [...] Kim teaches that insulating material covers the entire substrate and encases the memory device." Reply, 14. However, as PO explained, trenches are "formed after the insulating layer has been deposited, cut across the entire length (Fig. 3) and height (Fig. 13) of the staircase region, forming an intervening opening on at least two sides of the stack structure" (POR, 27-28 (citing Kim, 18:21-33)). As a result, even if the insulating material covers the entire substrate, trenches are formed afterwards and "expose portions of the substrate." Kim, 12:9-18.

This is further illustrated in Kim's Figure 24, which provides a three-dimensional view of another embodiment in Kim. POR, 31-32. The purple

highlighted “MP3” structure provides an illustration of what the insulation layer looks like after the opening of the trenches.



Kim, Fig. 24 (annotated by PO at POR, 31). Contrary to Petitioner’s assertion, PO does not ask the Board to take Kim’s Figure 24 “as drawn” (Reply, 17-18). While the filling structure may in fact reach the substrate on one side (as PO acknowledged at POR, 31-32), it nevertheless does not surround the stack structure, at least due to the trenches that disrupt it along the +D2 edge.

Because Petitioner realizes Kim’s trenches prevent its filling insulation layer from surrounding the staircase structure, it now relies on a new element to meet the limitation—asserting that “Kim’s trenches include an insulating liner that forms a

filling structure” (Reply, 14-15). Petitioner’s late attempt to raise a new argument based on a new combination of elements should be rejected as improper. Furthermore, Petitioner fails to show how the new mapping would encircle the stack. For example, Petitioner does not address what happens at the ends of the trenches. Also, this would raise the issue of whether the two components can be combined to meet the claimed “filling structure,” which Petitioner fails to address. Petitioner’s assertion that “the Board recognized ... that the claimed ‘filling structure’ can be one or more insulating materials” (Reply, 15 n.4 (citing DI, 24 from the Tessariol analysis)) is false, as the Board made no such determination. Rather the Board in the cited analysis found that “Petitioner does not adequately describe what parts or sections of the staircase structure dielectric material is deposited ‘around’” and “it is not clear that insulator material 86 ‘encases the entire stack structure.’” DI, 24-25.

5. Kim Does Not Disclose a Filling Insulation Layer in the -D2 Direction

As shown above in Figure 4A, Kim does not depict or describe the chip’s structure in the -D2 direction and in particular whether there is a filling insulation layer on that side. See POR, 30-31. While PO agrees with Petitioner that Kim’s Figures 3 and 4 do not “represent[] the full chip” (Reply, 16), the issue is whether Kim teaches an insulating layer is also present in the -D2 direction—it does not. Nothing in Kim’s teachings suggests that the insulating layer covers the -D2 side,

and other options (*e.g.*, an air-gap) were commonly practiced (Ex. 1026, 74:4-76:5; Ex. 1015, 10:57-59). POR 30-31. Alternatively, to the extent the stack structure extends to the substrate edge on that side, the insulating layer would be unable to surround it. Petitioner argues that an air-gap would not have been obvious to a POSITA (Reply, 16-17), but that is not accurate nor is it the proper test. Petitioner has the burden to show that Kim either inherently discloses or renders obvious the limitation—both parties appear to agree it is not expressly taught.

6. Kim Does Not Render Obvious That Its Filling Insulation Layer “Surrounds” the Stack Structure

Kim also does not render obvious a filling structure that “surrounds” the stack structure—the obviousness arguments in the Petition, which are based on CVD and allegedly desirable symmetry, are inconsistent with the trenches discussed above and ignore that Kim’s device is intentionally asymmetrical. POR, 35-42. Petitioner asserts that “YMTC mischaracterizes the Petition as arguing that each structure must extend symmetrically” (Reply, 18), but it was Petitioner’s arguments that were based on symmetry. For example, the Petition asserted that “it would have been understood by a POSITA, and certainly obvious, that the filling material would extend to the outer edge in the other directions.” Pet. 35; *see also* Ex. 1003, ¶113 (Dr. Banerjee arguing for “a symmetric device, which is generally desirable”). Thus, it appears that Petitioner is withdrawing its argument that having the filling material

extend in all four planar directions would have been motivated to create “a symmetric device.”

Next, Petitioner misrepresents PO’s position as “contemplat[ing] edge cases of CVD” (Reply, 19), while it is Petitioner who only contemplates one possible result of CVD deposition out of many—driven by a hindsight desire to read on the claims: covering and surrounding everything on all sides. Kim itself discloses that CVD is used to form small, localized structures (11:63-12:1) and insulating layers and sacrificial layers (12:17-21), which do not cover the entire surface of the substrate. It is Petitioner’s burden to show that Kim’s teachings would have rendered obvious an insulating layer that surrounds Kim’s stack—a task at which Petitioner has consistently failed. Petitioner again selectively quotes from Dr. Kuhn’s testimony, from a mostly irrelevant discussion about the edge of the wafer and not the edge of the memory stack (Reply, 19). During that discussion, Dr. Kuhn in fact stated: “There are ***a multiplicity of CVDs available***, and some of them are less conformal. And so I can't say whether any arbitrary CVD technique is going to do any particular thing at the edge of the wafer.” Ex. 1026, 111:10-14. Dr. Kuhn also stated that what happens at the edge of the wafer is product-dependent. Ex. 1026, 20:11-15 (“[I]f you have extremely robust products, you may run them closer to the edge. If some product is very touchy, you may be much more careful about exactly where you place it.”). Furthermore, Dr. Kuhn explained that the “empty

space” between the die on a wafer can be used to host various structures, such as “test structures.” Ex. 1026, 21:23-4.

Petitioner attempts to defend its reliance on the separate Park reference (which teaches “using common source lines...to isolate the staircase”) as showing “what was known” (Reply, 19-20), but Petitioner still fails to establish that it would have been obvious for a POSITA to use that technique in Kim. POR, 43. The Petition merely pointed to Park’s common source lines and asserted that “Kim would have been understood to disclose (or at least render obvious)” these same components, and cited conclusory expert testimony. Pet. 36-38. Even if a component is “known” to a POSITA, it does not mean that a POSITA would have found it obvious to use the same component specifically in Kim’s device.

Lastly, Petitioner again asserts that PO fails to address the Petition’s reliance on conformal CVD (Reply, 20), but PO has repeatedly addressed these assertions and has shown that Kim merely teaches CVD, which does not by itself render the “surrounding” limitation obvious. POR, 37-39.

B. Claim 4: Kim Does Not Disclose or Render Obvious That “the Supporting Pillar Is Filled with...a Pillar-Support Material Surrounded by the Insulating Material”

Petitioner’s argument that Kim’s dummy structures include a conductive core that is a “supporting material” fails because Kim does not even disclose a conductive

core, let alone disclose or render obvious one that is a “pillar-support material.” POR 45-55.

Petitioner has not shown that Kim’s device needs or would even benefit from additional supporting structures. POR, 49; Kuhn, ¶155. Petitioner’s argument that “support pillars...were known in the art” and “physically support” the stack (Reply, 20-21) and its related reliance on Dr. Kuhn’s testimony (Ex. 1026, 233:20-235:4) miss the point. Without a reason to include or modify structures to provide further support than Kim’s dummy structures already provide, a POSITA would have had no motivation to complicate Kim’s manufacturing flow by introducing new materials and fabrication steps for no identified benefit.

While the ’031 discloses that “[a]ny suitable pillar-filling materials” can be deposited to “form supporting pillars” (Reply, 20), Petitioner ignores that the ’031 clarifies that this means “[a]ny suitable material **with sufficient stiffness and/or support functions** can be used as the support material.” ’031, 18:26-28. Petitioner asserts that “YMTC’s expert admitted that the ’031 patent never explains what ‘sufficient stiffness and/or support functions’ means or how a POSITA would determine it” (Reply, 21-22), but that does not mean that a POSITA would have been unable to understand the term in light of the ’031 or how to apply it—nor does Petitioner assert otherwise.

Petitioner's only attempt at explaining how a POSITA would have selected a material to modify Kim's dummy structures was its reliance on Dr. Banerjee's testimony regarding elastic properties of metals. *See* Pet. 87; Banerjee, ¶215. As explained in the POR, however, metals do not necessarily have a higher Young's modulus than insulators, and there is no correlation between conductivity and material stiffness. POR 50-54; Kuhn, ¶¶156-163. Unable to rebut these points, Petitioner accuses PO of "fixat[ing]" on that issue (Reply, 22), but does not otherwise defend it—tacitly admitting that Dr. Banerjee's discussion of elastic properties was flawed all along.

Petitioner's reliance on Tessariol's conductive vias fails because (1) Tessariol does not disclose the type of metal, and thus whether it is a pillar support material, and (2) Petitioner fails to show that Kim would benefit from additional interconnects. POR, 52-53. Petitioner fails to address the first point. As to the second, Petitioner asserts that "Kim discloses peripheral circuitry" and that these "require vertical conductive vias, which YMTC's expert admitted" (Reply, 22-23), but Dr. Kuhn did not admit that "peripheral devices **require** vertical conductive vias." Dr. Kuhn simply explained, in a different context (indeed, a different IPR), that a vertical conductive via **can** be used to connect to peripheral devices. Ex., 1028, 80:9-82:9.

Moreover, a purported showing that a POSITA would have known about conductive vias (from Tessariol) does nothing to show that a POSITA would have

turned Kim’s dummy structures, in particular, into conductive vias. Dr. Banerjee in his new declaration provides examples of vertical vias from new references (Ex. 1025, ¶65), but Kim does not disclose any circuitry under the memory array or the staircase that would need connections. Kuhn, ¶169. Moreover, Petitioner’s new examples only show vias that are **beyond** the staircase region (“peripheral device region 200” in Ex. 1029 and “through-peripheral-stack region 500” in Ex. 1030). Thus, this evidence is irrelevant to whether a POSITA would have modified **Kim’s dummy structures**, which are **in the staircase region**, to turn them into conductive vias. Dummy structures and conductive vias are distinct, and whereas the former are placed in the staircase region to support the stack (Ex. 1026, 79:2-6), the latter are placed where connections between the upper layers and lower layers are needed (Ex. 1026, 66:3-12).

Lastly, regarding thermal expansion mismatch, Petitioner’s assertion that “the ’031 patent makes no mention of ‘thermal expansion mismatch’ and explains nothing unpredictable about using ‘copper’ and ‘silicon oxide’” (Reply, 23-24) is misplaced. The fact that the ’031 was able to solve a problem does not negate the problem itself or suggest that a POSITA would have found that particular solution obvious.

IV. GROUND 2: TESSARIOL (CLAIMS 1-2, 4-5)

Tessariol fails to disclose or render obvious the Challenged Claims at least because, under the proper construction of “surrounding” as encircling (§II), Tessariol fails to disclose or render obvious limitation [1.d] of the sole challenged independent claim. Tessariol also does not disclose or renders obvious a “supporting pillar” with a “pillar-support material,” as required by dependent claim 4, which comprises copper, cobalt, nickel, or aluminum, as required by dependent claim 5.

A. Independent Claim 1: Tessariol Does Not Disclose or Render Obvious That Its Alleged Filling Structures “Surround” Its Steps

Petitioner argues that PO “ignor[ed] the Petition’s showing that Tessariol’s CVD techniques would fully encase the memory structure” (Reply, 24), but neither Petitioner nor Dr. Banerjee quoted Tessariol’s single mention of “chemical vapor deposition” ([0063]) before their Reply. Nonetheless, this new argument merely rehashes the same flawed analysis discussed above for Kim, where PO already refuted Petitioner’s similar arguments. POR, 56-64. Similar to its approach with Kim, Petitioner makes an unsupported leap from a mere mention of CVD to “fully encas[ing] the memory structure” and surrounding the stack. Reply, 24. As explained above and in the POR (POR 56-64), mere disclosure of CVD does not disclose or render obvious the limitation.

A POSITA would not have understood or found obvious that Tessariol's stack would have been encased by a dielectric material. POR, 56-64. For example, none of Tessariol's dielectric components Petitioner points to, alone or in combination, encircle the stack. POR, 57-63. Furthermore, the entirety of Tessariol's teachings about CVD is a generic reference within a list of fabrication techniques. Tessariol, [0063]. From this, Petitioner jumps to the conclusion that Tessariol's device would have been encased as a result of CVD, in a specific way that would allegedly satisfy limitation [1.d]. The Board has rightfully questioned these assertions (DI, 24-25) and PO has repeatedly explained why they are incorrect (POR, 56-64).

Petitioner accuses PO of "fail[ing] to acknowledge that Figure 7, and others, illustrate only a '**portion**' of the disclosed substrate and memory device" (Reply, 26), but this statement and the subsequent analysis attempts to refute arguments that PO has not made. PO's arguments have not been based on any assumption that Tessariol's figures show the entire device.

Lastly, Petitioner argues that PO's arguments with respect to obviousness fail for the same reasons as in Ground 1 (Reply, 26-27), but Petitioner's obviousness arguments are once again based on Tessariol's aforementioned single mention of CVD. As discussed in Ground 1, there are many ways to deposit materials using CVD, and Petitioner has failed to show that a POSITA would have found it obvious

to use CVD in a specific manner that would result in filling structures “surrounding” Tessariol’s steps. POR, 64-65.

B. Claims 4-5: Tessariol Does Not Disclose That “the Supporting Pillar Is Filled with...a Pillar-Support Material Surrounded by the Insulating Material”

Petitioner’s reliance on Tessariol’s dummy structures (Pet., 83-84) fails because Tessariol does not disclose or render obvious that the conductive core is a “pillar-support material” as required by claim 4.

Petitioner acknowledges that Tessariol does not provide examples for the “metal material” of its dummy structures beyond the fact that it can be an “elemental metal.” Reply, 27. But claim 4 requires a “pillar-support material,” which requires a material with “sufficient stiffness and/or support functions.” ’031, 18:26-28. Petitioner has never shown why Tessariol’s unspecified metal has these functions or why it would have been obvious to use a material that does. POR, 65-66. Petitioner is wrong that “Tessariol discloses exactly what the ’031 patent discloses” (Reply, 28)—while the ’031 discloses the properties of “pillar-support materials” and gives examples of such materials, Tessariol never does so.

Because Tessariol’s teachings fall short, Petitioner attempts to backtrack from the “sufficient stiffness and/or support functions” requirement. Reply, 28. Until now, Petitioner embraced this requirement by arguing that material properties, *e.g.*, Young modulus, “determine the suitability of a material as the pillar.” Ex. 1003, ¶215; Pet.

84-88. Petitioner cannot now complain about phrases from the specification it previously had no problem understanding.

Regarding claim 5, Petitioner asserts any “elemental metal” satisfies the limitation of “copper, cobalt, nickel, or aluminum,” but that is clearly not the case. For example, mercury is an elemental metal, but is not even in its solid state at room temperature. Therefore, Petitioner needed to show why a POSITA would have been motivated or found it obvious to use a particular material in Tessariol’s dummy structures, which it did not. For example, Petitioner does not even attempt to address the issues PO raised about, *e.g.*, copper. Instead, it merely reasserts (Reply, 28) that copper was “well-known,” which is not the test for obviousness. Petitioner is also wrong that the ’031 does not discuss these issues, as discussed above. Finally, as before, the fact that the ’031 solved a problem does not negate the problem itself or suggest that a particular solution would have been obvious.

V. GROUND 3: KIM IN VIEW OF TESSARIOL (CLAIM 4)

Kim in view of Tessariol fails to render obvious claim 4. First, Ground 3 relies on Kim only for claim 1, and fails for the same reasons as Ground 1. POR, 67. Second, as explained in the POR, a POSITA would not have applied Tessariol’s “conductive core” teachings to Kim’s dummy structures. POR, 68-70.

Petitioner incorrectly asserts that PO “ignores” Dr. Banerjee’s explanation of why “adding a conductive core” to Kim’s dummy structures “would not complicate

the manufacturing process.” Reply, 29. This is false, as PO and Dr. Kuhn addressed Dr. Banerjee’s arguments (POR, 68-69; Kuhn, ¶¶218-219). Petitioner cites Paragraph 218 of Dr. Banerjee’s first declaration, where he argued that “Kim’s fabrication process already employs such structures that extend through the stack, namely, a common source line [CSR]” (Reply, 29 (citing Ex. 1003, ¶218)), but this argument fails because Kim’s CSR is not analogous to a dummy structure with a conductive core. Unlike Kim’s dummy structures, Kim’s CSR (1) is a long extensive structure, (2) is not disclosed as connected to peripheral circuitry, and (3) does not include a conductive core (it includes a doped semiconductor). Kim, 6:11-22 (“*The common source regions CSR may be arranged in the first direction D1. The common source regions CSR may be **doped with dopants** and may have a second conductivity type.*”). Thus, the unrelated CSR does not rebut Dr. Kuhn’s explanation that adding a conductive core to the dummy structures complicates the manufacturing process, which Petitioner fails to address.

Petitioner argues that using a conductive core in Kim’s dummy structure would provide support and interconnection for peripheral devices (Reply, 29; Pet. 87-88), but Petitioner again fails to identify (1) a need for additional support beyond what Kim’s dummy structures already provide, and (2) any peripheral devices under the array that would require interconnection. POR 52-53, 68-69. Tessariol’s device might benefit from a conductive core, but not Kim’s device. POR, 67-70; Kuhn,

¶222. As a result, without a sufficient showing of motivation to combine, Petitioner's Ground 3 fails.

VI. GROUND 4: TESSARIOL IN VIEW OF KIM (CLAIMS 1-2, 4-5)

Tessariol in view of Kim fails to render obvious claims 1-2, 4-5. A POSITA would not have applied Kim's filling material techniques to Tessariol's stack to meet claim 1. POR, 70-71. Petitioner continues to provide only vague and conclusory statements regarding the desirability of a "planarized surface" in Tessariol (Pet. 92; Reply, 30-31), which PO has already addressed (POR, 71). Without explaining how using planarization (which relates to obtaining planar top surfaces and not surrounding) in Tessariol fixes Tessariol's deficiency in showing limitation [1.d] ("surrounding"), these comments are insufficient. Even if a POSITA applied Kim's "planarization" technique to Tessariol, as Petitioner suggests, this would result in filling structure with a planar surface, which does not teach a filling structure surrounding the stack.

Lastly, Petitioner disputes the Board's observation that Ground 4 does not rely on Kim for limitation [1.D] (Reply, 31 n.7 (citing DI, 26)), but because Petitioner uses the same mapping in Ground 4 as it uses in Ground 2 (a Tessariol-only ground), the Board is correct that Ground 4 does not rely on Kim for [1.D]. Regardless, without addressing how using planarization would fix Tessariol's deficiency in showing limitation [1.d], Ground 4 fails.

VII. CONCLUSION

Petitioner has failed to demonstrate by a preponderance of the evidence that any of the Challenged Claims of the '031 are anticipated or obvious. Accordingly, the Board should uphold the validity of all Challenged Claims.

Dated: May 27, 2025 Respectfully submitted,

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CERTIFICATE OF SERVICE

The undersigned certifies that the foregoing PATENT OWNER'S SUR-REPLY was served in its entirety by filing through the Patent Trial and Appeal Case Tracking System (P-TACTS), as well as providing a courtesy copy via e-mail to the following attorneys of record for Petitioner listed below:

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