Patent Owner's Demonstrative Slides

Micron Technology, Inc. v. Yangtze Memory Technologies Company, Ltd.

***Inter Partes* Review of**

U.S. Patent No. 10,868,031

July 31, 2025

IPR2024-00790
Patent Trial and Appeal Board
United States Patent and Trademark Office

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I. Introduction

Table of Abbreviations

Abbreviation	Description
’031	U.S. Pat. No. 10,863,031 (Ex. 1001)
Banerjee	Declaration of Dr. Sanjay Banerjee (Ex. 1003)
Banerjee II	Reply Declaration of Dr. Sanjay Banerjee (Ex. 1025)
Challenged Claims	’031, Claims 1-5
Kim	U.S. Patent No. 10,381,369 (Ex. 1005)
Kuhn	Declaration of Dr. Kelin Kuhn (Ex. 2013)
Office	U.S. Patent and Trademark Office
Parallel District Court Litigation	*Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc.*, NDCA-3-23-cv-05792 (N.D. Cal.)
Patent Owner	Yangtze Memory Technologies Co. Ltd.
Petition or Pet.	Petition (Pap. 1)
Petitioner	Micron Technology, Inc.
POSITA	Person of ordinary skill in the art
POR	Patent Owner’s Response (Pap. 12)
Reply	Petitioner’s Reply (Pap. 14)
POSR	Patent Owner’s Sur-reply (Pap. 17)
Tessariol	U.S. Patent Publication No. 2019/0081061

All citations within quotations omitted herein, and emphasis added unless otherwise indicated

'031, Claim 1

- Claim 1 of the '031 recites:

[1.Pre] 1. A memory device, comprising:

[1.A] a substrate;

[1.B] a multiple-stack staircase structure comprising a plurality of staircase structures stacked over the substrate,

[1.C] wherein each of the plurality of staircase structures comprises a plurality of conductor layers, wherein each of the plurality of conductor layers is located between two insulating layers;

[1.D] ***a filling structure surrounding the multiple-stack staircase structure***;

[1.E] a semiconductor channel extending through the multiplestack staircase structure, wherein the semiconductor channel comprises unaligned sidewall surfaces; and

[1.F] a supporting pillar extending through at least one of the multiple-stack staircase structure and the filling structure, wherein the supporting pillar comprises aligned sidewall surfaces.

’031, Claims 4-5

4. The memory device of claim 2, wherein:

the supporting pillar and the semiconductor channel are filled with different filling layers; and

the supporting pillar is filled with at least one of an insulating material and a pillar-support material surrounded by the insulating material, and the semiconductor channel is filled with at least one of a charge trapping film, a semiconductor channel film, and a dielectric core.

5. The memory device of claim 4, wherein the insulating material comprises silicon oxide and the pillar-support material comprises at least one of copper, cobalt, nickel, and aluminum.

Grounds

Claims	Ground
’031, Claims 1-4	Kim Obviousness
’031, Claim 1-2 and 4-5	Tessariol Obviousness
‘031, Claim 4	Kim in view of Tessariol Obviousness
‘031, Claims 1-2 and 4-5	Tessariol in view of Kim Obviousness

Pet. 8.

Disputed Issues

Issue	Slides
"Surrounding" Limitation (All Challenged Claims) ▪ **Claim Construction** ▪ **Ground 1 (Kim)**: Kim Does Not Disclose or Render Obvious That Its Filling Insulation Layer "Surrounds" the Stack Structure (Limitation [1.d]) ▪ **Ground 2 (Tessariol)**: Tessariol Does Not Disclose or Render Obvious That Its Alleged Filling Structures "Surround" Its Steps (Limitation [1.d]) ▪ **Ground 4 (Tessariol in view of Kim)**: Tessariol in View of Kim Fails for the Same Reasons as Ground 2, and a POSITA Would Not Have Been Motivated to Combine Tessariol and Kim (Limitation [1.d])	Slides 8-34
"Pillar-Support Material Surrounded by the Insulating Material" Limitation (Claims 4-5) ▪ **Ground 1 (Kim)**: Kim Does Not Disclose or Render Obvious That "the Supporting Pillar Is Filled with…a Pillar-Support Material Surrounded by the Insulating Material" (claim 4) ▪ **Ground 2 (Tessariol)**: Tessariol Does Not Disclose That "the Supporting Pillar Is Filled with…a Pillar-Support Material Surrounded by the Insulating Material" (claims 4-5) ▪ **Ground 3 (Kim in view of Tessariol)**: A POSITA Would Not Have Applied Tessariol's "Conductive Core" Teachings to Kim's Dummy Structures (claim 4) ▪ **Ground 4 (Tessariol in view of Kim)**: Tessariol in View of Kim Fails for the Same Reasons as Ground 2 (claims 4-5)	Slides 35-53

II. “Surrounding” Limitation

Limitation [1.D] Requires a Filling Structure "Surrounding" the Multiple-Stack Staircase Structure

[1.B] a multiple-stack staircase structure comprising a plurality of staircase structures stacked over the substrate,

[1.C] wherein each of the plurality of staircase structures comprises a plurality of conductor layers, wherein each of the plurality of conductor layers is located between two insulating layers;

[1.D] ***a filling structure surrounding the multiple-stack staircase structure***;

The Term "Surrounding" in the '031 Patent Means to Be All the Way Around (Something)—Encircling

- The plain meaning of "surrounding" is "encircling"

> **Surround**: "be all around (someone or something); … ***encircle*** (someone or something) so as to cut off communication or escape"

Ex. 2001 (New Oxford American Dictionary (2010)); POR 15; Kuhn, ¶70.

> **Surround**: "***encircle***"

Ex. 2002 (American Heritage College (2000)); POR 15; Kuhn, ¶70.

> **Surround**: "to ***encircle*** on all sides of simultaneously"

Ex. 2003 (Webster's II New College (2005)); POR 15; Kuhn, ¶70.

> **Surround**: "to enclose on all sides : ***ENCIRCLE***"

Ex. 2004 (Merriam-Webster's Dictionary and Thesaurus (2014)); POR 15; Kuhn, ¶70.

- Claim 1 uses the term "surrounding" instead of narrower alternatives, such as "covering" or the concept of being "between" two structures:

> "a filling structure ***surrounding*** the multiple-stack staircase structure;"

POR 15; Kuhn, ¶71.

The '031 Specification Supports Construing "Surrounding" as "Encircling"

- Figure 12 shows that the multiple-stack staircase structure is encircled by the filling structure **in the -x and +x directions**:

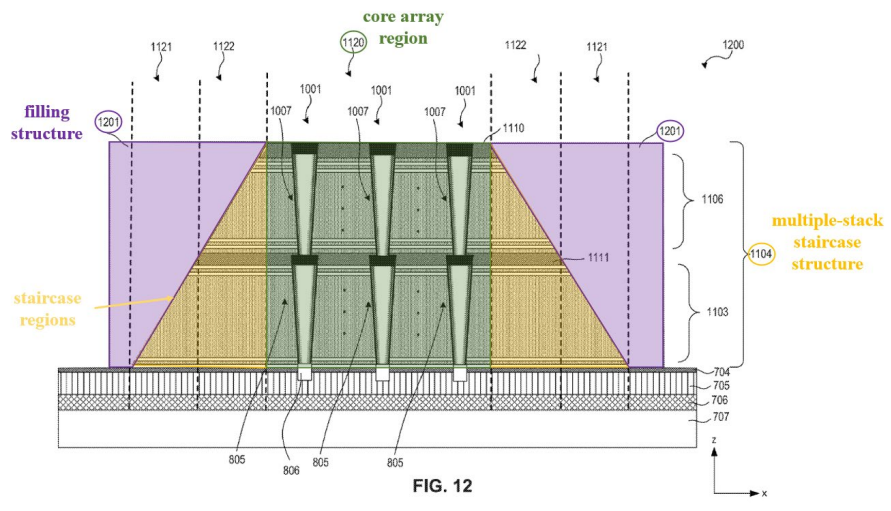


FIG. 12

'031, Fig. 12 ("first staircase region 1121" and "second staircase region 1122" are shown to extend in the +x and –x directions), Fig. 4; POR 15-17; Kuhn, ¶72.

- The specification explains that the staircase regions, which have the filing structure, **also extend in the +y and -y directions**, and therefore "surround" the multiple-stack staircase structure:

"Dielectric pairs of different tiers can be etched to ***form staircases extending along the x-y plane***."

'031, 13:27-28; POR 15-16; Kuhn, ¶72.

"First staircase region 1121 and second staircase region 1122 can each ***surround memory structure 1100 along the x-y plane***."

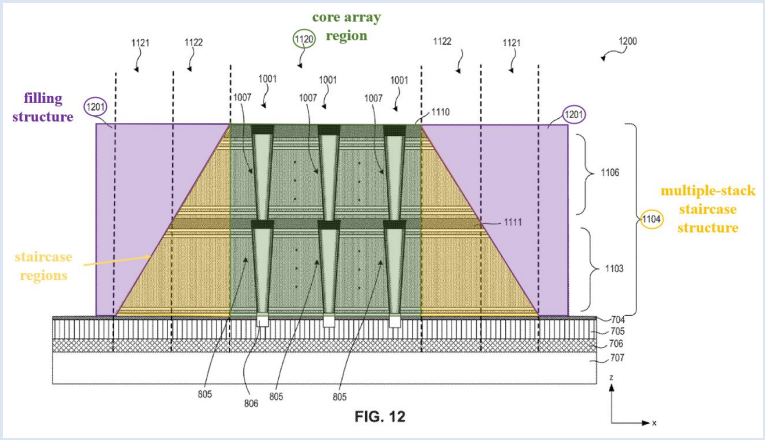
'031, 22:30-32; POR 15-16; Kuhn, ¶72.

The '031 Specification Supports Construing "Surrounding" as "Encircling"

- After the patterning of the staircase regions, the filling structure is deposited to fill the space surrounding the staircase structure (the left, right, back, and front):

"Further, ***a dielectric filling material can be deposited after staircase structure 303 is formed to fill in the space formed by the removal of the portions of dielectric stack 203***. Dielectric filling structure 311 is deposited in periphery region 320 and core region 310 to fill in the space formed by the removal of the portions of dielectric stack 203."

'031, 13:36-48; POR 17; Kuhn, ¶73.



'031, Fig. 12, Fig. 4; POR 15-17; Kuhn, ¶72.

- The '031 uses the term "surrounding" consistently as "encircling" in multiple other instances:

"In some embodiments, the supporting pillar is filled with at least one of an insulating material and a pillar-support material ***surrounded by the insulating material***."

'031, 2:12-14; POR 18; Kuhn, ¶74.

"Charge trapping film 416 can also include a storage unit layer (memory layer) over and ***surrounded by the block dielectric layers*** for trapping charges and forming a plurality of charge storage regions along the z axis. Charge trapping film 416 can also include a tunneling layer (e.g., tunneling dielectric) over and ***surrounded by the memory layer***."

031, 15:49-57; POR 18; Kuhn, ¶74.

"Surrounding" in the '031 Patent Means "Encircling"

Petitioner argues: "But the ***'031 does not teach*** or illustrate the filling structure 'deposited to,' e.g., the 'back' and 'front' (i.e., ***y-direction*** in Fig. 3) of the staircase."

Reply 4.

- But Petitioner ignores the cited evidence of staircases that extend along the x-y plane to "surround" the memory structure:

"Dielectric pairs of different tiers can be etched to ***form staircases extending along the x-y plane***."

'031, 13:27-28; POR 15-16, POSR 2-3; Kuhn, ¶72.

"First staircase region 1121 and second staircase region 1122 can each ***surround memory structure 1100 along the x-y plane***."

'031, 22:30-32; POR 15-16; Kuhn, ¶72.

- The filling structure thus surrounds the staircase structure:

"[M]emory structure 300 can be formed by forming a two-stack staircase structure 303 from dielectric stack 203, ***filling space formed by the formation of staircase structure 303 with a dielectric filling structure 311***."

'031, 13:13-17; POSR 3.

Ground 1 (Kim): Kim Fails to Disclose or Render Obvious That Its Filling Insulation Layer "Surrounds" the Stack Structure

- Kim does not disclose that its filling insulation layer "surrounds" the stack structure
  - Kim's disclosure that insulation layer 110 may be disposed "on the substrate" and may "cover" the stack structures ***merely teaches that insulation layer 110 is on one side*** POR 25-27.
  - Kim teaches trenches are formed after the insulation layer 110, which prevents the previously deposited insulation layer from "surrounding" the stack structures in the ***+D1 and -D1 direction*** POR 27-30; POSR 12-14.
  - Kim ***does not show*** insulating layer 110 in the ***-D2 direction*** POR 30-31; POSR 14-15.
  - Kim never discloses that the insulation layer 110 fills all voids, and there are a wide variety of techniques in the art for creating ***unfilled air-gaps*** POR 32-34; POSR 5-7.
  - Petitioner's arguments regarding a ***planarized top surface do not account for subsequent processing steps (e.g., trenches)*** POR 35.
  - Petitioner's improper new claim mapping based on Kim's Figure 1 does not show filling structure surrounding the staircase structure POSR 7-10.

Ground 1 (Kim): Kim Fails to Disclose or Render Obvious That Its Filling Insulation Layer "Surrounds" the Stack Structure

- Kim does not render obvious that its filling insulation layer "surrounds" the stack structure
  - Petitioner's argument that a structure that extends in one direction would also extend in a perpendicular direction is ***inconsistent with the evidence (e.g., trenches)*** POR 36-37.
  - Dr. Banerjee's reliance on CVD fails to acknowledge that the ***process creates air-gaps*** POR 37-39; POSR 16-17.
  - Dr. Banerjee's reliance on a general desire for symmetry ignores that ***Kim's device is intentionally asymmetrical*** POR 39-42; POSR 15-16.
  - Park does not explain how Kim "would have been understood"; ***simply because a component is "known" does not mean that it would have been obvious to use*** POR 42-44; POSR 17.
  - Insulating liners in combination with filling insulating layer 110 still would not render obvious surrounding the stack structure because ***Kim's device in the -D2 direction is not depicted or described*** POR 44.

Ground 1 (Kim): Kim Fails to Disclose That Its Filling Insulation Layer "Surrounds" the Stack Structure

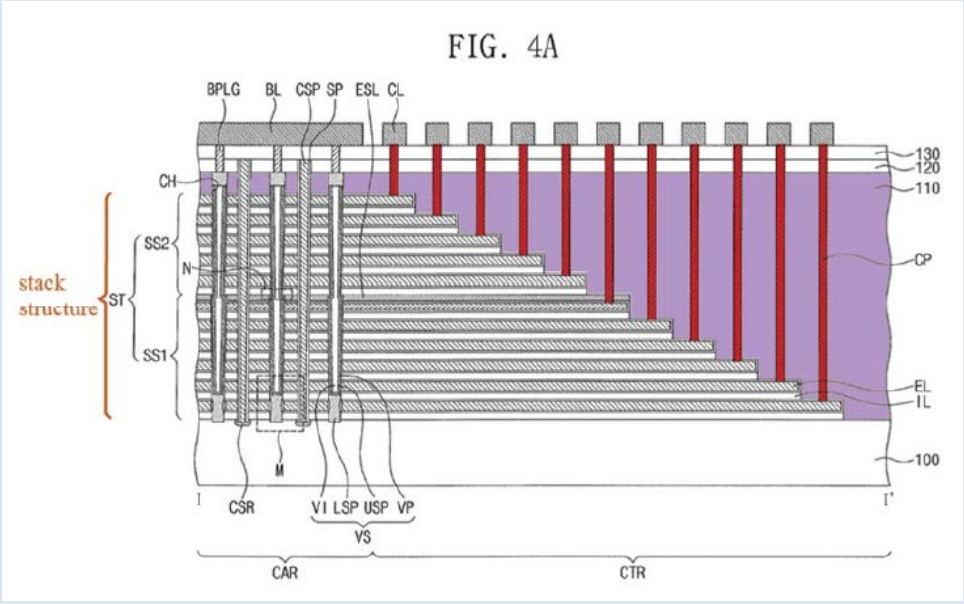
Petitioner argues: "Kim discloses a 'filling insulating layer 110' that 'may be disposed on the substrate 100 and may cover the stack structures ST.'"

Pet. 32.

- But Kim's disclosure ***merely teaches that the stack structures may be covered by the insulation layer 110 and is on one side***

Kim: "The filling ***insulation layer 110 may be disposed on the substrate 100 and may cover the stack structures ST***. The filling insulation layer 110 may have a planarized top surface."

Kim, 9:53-56; Kuhn, ¶¶96-97; POR 25-27.



Kim, Fig. 4A; Kuhn, ¶¶96-97; POR 26.

Ground 1 (Kim): Kim Fails to Disclose That Its Filling Insulation Layer "Surrounds" the Stack Structure

- Kim teaches that ***trenches*** are formed after the insulation layer 110, which prevents the previously deposited insulation layer from "surrounding" the stack structures in the ***+D1 and -D1 direction***

Kim: "Referring to FIGS. 3 and 13, a first interlayer insulating layer 120 may be formed on the filling insulation layer 110. ***The first interlayer insulating layer 120 and the mold structure MT may be patterned to form a plurality of mold structures MT laterally spaced apart from each other***. The mold structures MT may extend in the second direction D2 and may be arranged in the first direction D1. ***A trench TR may be defined between the mold structures MT adjacent to each other. The trenches TR may expose portions of the substrate 100***."

Kim, 12:9-18; 18:21-33; Kuhn, ¶¶99-100; POR 27-30; POSR 12-14.

FIG. 3

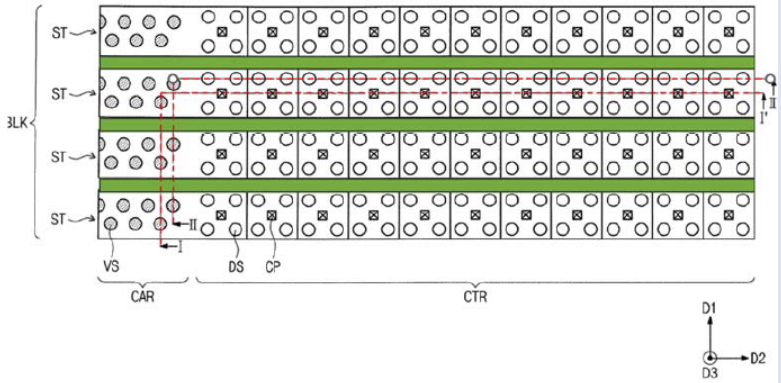
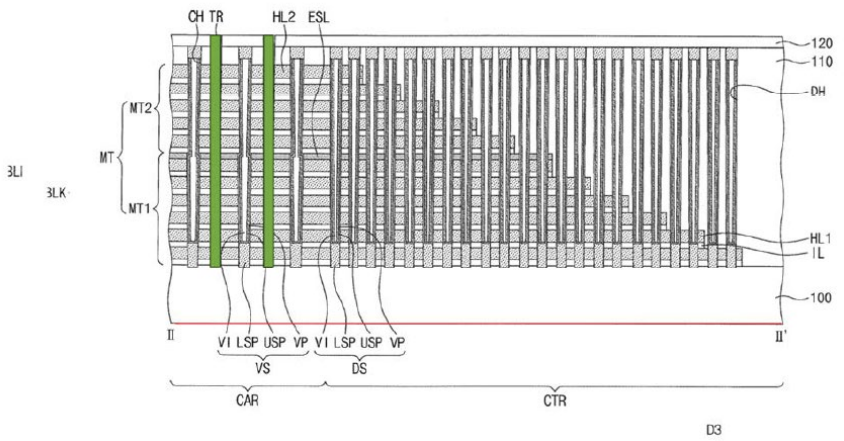


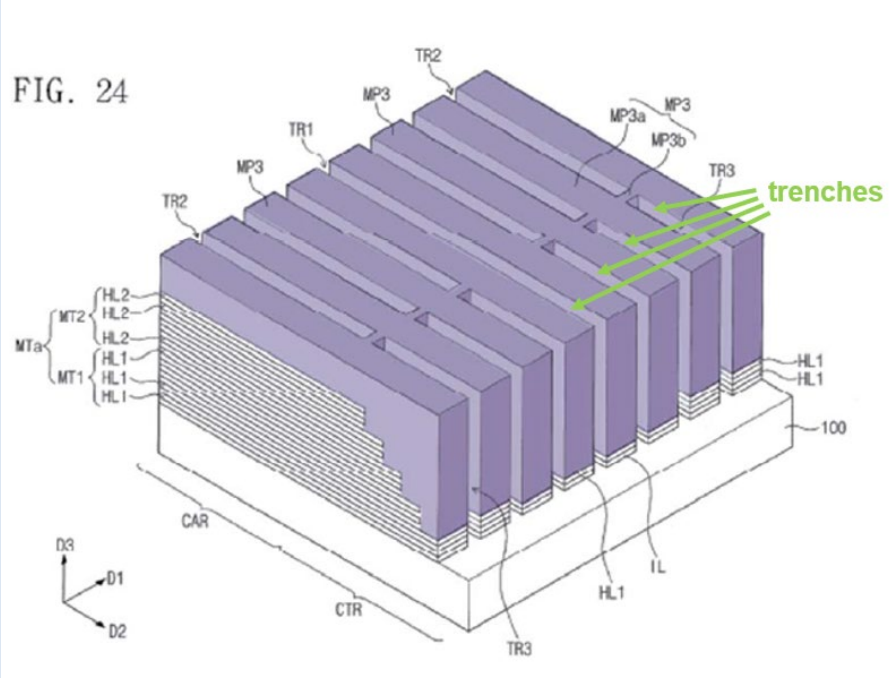
FIG. 13



Kim, Figs. 3, 13; Kuhn, ¶¶99-100; POR 27-30.

Ground 1 (Kim): Kim Fails to Disclose That Its Filling Insulation Layer "Surrounds" the Stack Structure

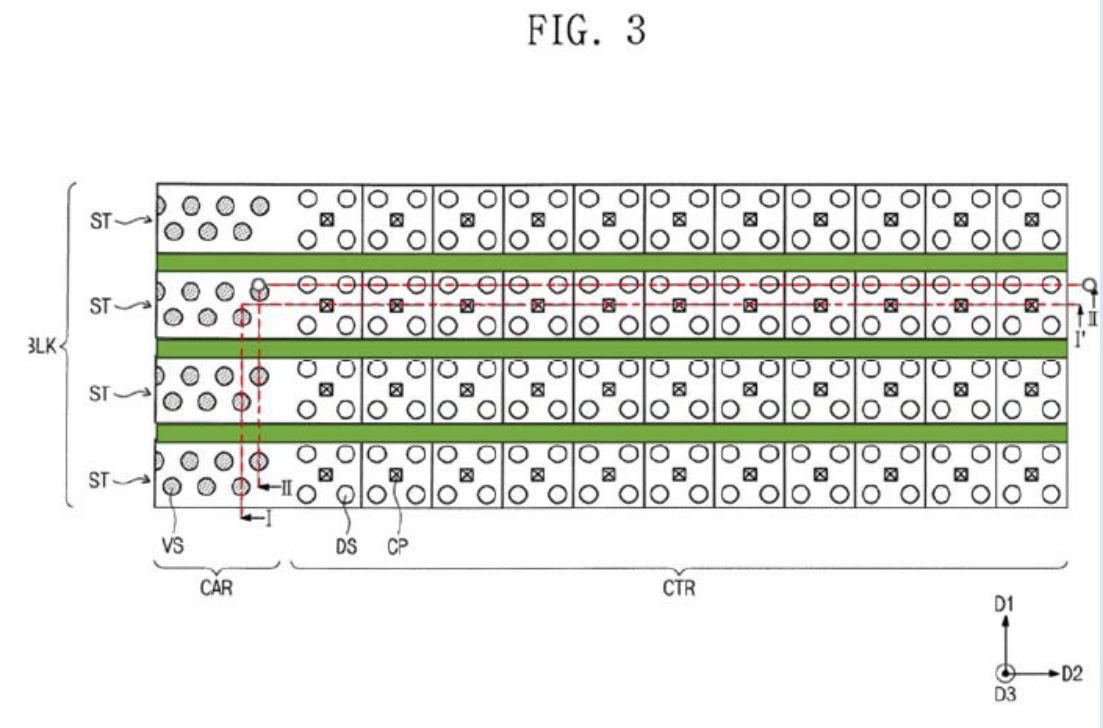
- Kim's Figure 24 illustrates what the **insulation layer** looks like after opening the trenches, confirming that the filling structure does not surround the stack structure due to the trenches



Kim, Fig. 24; POSR 12-13; Kuhn, ¶¶102-103; POR 31-32.

Ground 1 (Kim): Kim Fails to Disclose That Its Filling Insulation Layer "Surrounds" the Stack Structure

- Kim ***does not depict or describe*** insulating layer 110 in the ***-D2 direction***



Kim, Fig. 3; Kuhn, ¶101; POR 30-31; POSR 14-15.

Ground 1 (Kim): Kim Fails to Disclose That Its Filling Insulation Layer "Surrounds" the Stack Structure

Petitioner argues: "Because Kim discloses depositing the filling insulating layer onto "substrate 100" to cover the stacks and ***planarizing the material on the top surface***, this ***means that the filling material will encase*** the memory device.'"

Pet. 35.

- But Petitioner's arguments regarding a ***planarized top surface do not account for subsequent processing steps, e.g., trenches in Figs. 3 and 13, which are formed through the entire staircase structure***

FIG. 3

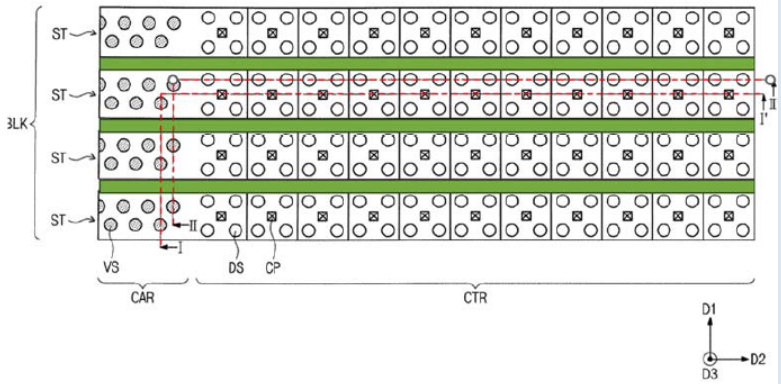
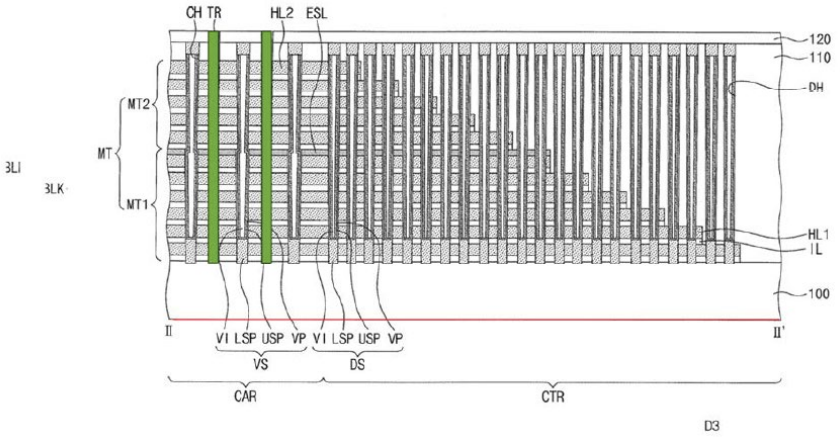


FIG. 13



Kim, Figs. 3, 13; Kuhn, ¶¶113-115; POR 35.

Ground 1 (Kim): Kim Fails to Disclose That Its Filling Insulation Layer "Surrounds" the Stack Structure

Petitioner argues: "As shown in Figure 10 below, after forming the staircase region, Kim further discloses forming insulation layer 110 ***to fill all voids***. Kim, 11:10-21.'"

Pet. 33.

- But again, Petitioner ignores subsequent processing steps, e.g., trenches (see slide 20)
- Kim never discloses that the insulation layer 110 fills all voids
- Kim instead discloses that CVD is used to form small, localized structures and insulating layers and sacrificial layers, which do not cover the entire surface of the substrate

Kim: "A vertical insulating layer VP and an upper semiconductor pattern USP may be formed to sequentially cover an inner side wall of each of the channel and dummy holes CH and DH. ***Each of the vertical insulating layer VP and the upper semiconductor pattern USP may be formed using an ALD process and a CVD process***."

Kim, 11:63-12:1; POSR 16.

Kim: "***The insulating layers IL, the first sacrificial layers HL1, and the etch stop layer ESL may be deposited using a thermal chemical vapor deposition (thermal CVD) process, a plasma-enhanced CVD process, a physical CVD process***, and/or an atomic layer deposition (ALD) process."

Kim, 10 :17-21; POSR 16.

Kuhn, ¶¶105-106; POR 32-34; POSR 5-7.

Ground 1 (Kim): Kim Fails to Disclose That Its Filling Insulation Layer "Surrounds" the Stack Structure

Petitioner argues in Reply: "[A] POSITA would have understood Kim's teachings—i.e., depositing an insulating material to "cover" the substrate and memory device such that planarization is required—***necessarily means that the "filling structure" would encase the memory device*** and, thus, would surround the staircase structure. … To electrically isolate the staircase after etching, ***one would commonly use CVD*** to deposit insulating material (as Kim teaches), ***which would cover the entire wafer with a uniform film of insulating material***, including the side surfaces of any vertical structure (such as the staircase)"

Reply 5-6; *see also* Pet. 35.

- But there are a wide variety of techniques in the art for creating ***unfilled air-gaps*** that do not involve insulation material, e.g., using the non-conformity of a CVD dielectric layer

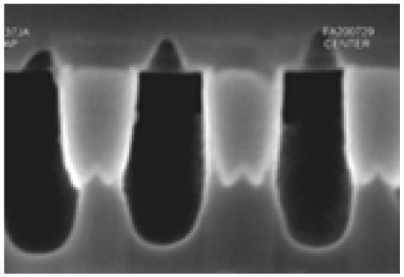


Fig. 1a: Self-Assembly Airgap

Ex. 2012, 191; Kuhn, ¶¶109-112; POR 32-34; POSR 5-7; *see also* Ex. 2009, 65, Fig. 1; Ex. 2010, 141-142.

- Dr. Kuhn also identified the use of air-gaps in 3D NAND technology in one of Petitioner's own exhibits:

Goda: "The gate-slit openings 228A can be left as an air-gap or filled with various types of dielectric material, such as, for example, silicon dioxide."

Ex. 1015, 10:57-59; Ex. 1026, 74:4-76:5; POSR 6.

Ground 1 (Kim): Kim Fails to Disclose That Its Filling Insulation Layer "Surrounds" the Stack Structure

Petitioner argues in Reply: "[A] POSITA would have understood Kim's teachings—i.e., depositing an insulating material to "cover" the substrate and memory device such that planarization is required—***necessarily means that the "filling structure" would encase the memory device*** and, thus, would surround the staircase structure. … To electrically isolate the staircase after etching, ***one would commonly use CVD to*** deposit insulating material (as Kim teaches), ***which would cover the entire wafer with a uniform film of insulating material***, including the side surfaces of any vertical structure (such as the staircase)"

Reply 5-6; *see also* Pet. 35.

- As Dr. Kuhn explains, it was common to use CVD to create air-gaps:

Dr. Kuhn: "These examples, which illustrate the creation of air-gaps in semiconductor devices using both CVD and CMP, clearly indicate that ***neither the use of CVD nor the use of CMP necessarily results in an isolation structure filled with silicon dioxide or silicon nitride***."

Kuhn, ¶¶110-112; POR 32-34; POSR 6; *see also* Ex. 2012, 191; Ex. 2009, 65, Fig. 1; Ex. 2010, 141-142.

Dr. Kuhn: "However, this description of the deposition process does not acknowledge that ***CVD deposition does not necessarily fill all structures***, and moreover, it can be architected to not fill specific structures. As I discussed earlier, ***one of several methods to create air-gaps in trenches is "taking advantage of the non-conformity of a CVD dielectric layer*** to create air cavities located inside trenches" a situation almost the opposite of what Dr. Banerjee has described."

Kuhn, ¶124; Ex. 2009, 65; POR 37-38.

- During her deposition, Dr. Kuhn did not agree that CVD necessarily results in coverage of the entire surface of the substrate, and rather discussed creating air-gaps:

Dr. Kuhn: "And this is a geometry-dependent thing. You can make of air gaps intentionally. People are actually quite good at this. You can make air gaps accidentally. When you make air gaps accidentally, they're usually called 'voids.' When you make them intentionally, they're usually called 'air gaps.'"

Ex. 1026, 57:5-58:8; POSR 6.

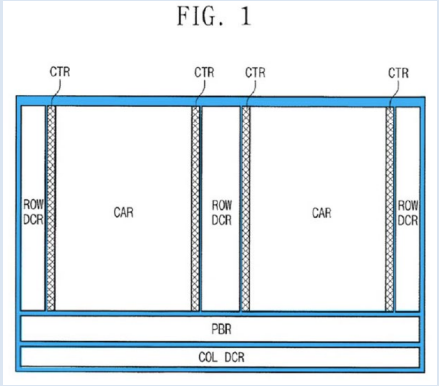
Ground 1 (Kim): Kim Fails to Disclose That Its Filling Insulation Layer "Surrounds" the Stack Structure

Petitioner argues in Reply: "What's more, ***Kim discloses forming various regions on a substrate so as to leave room to deposit filling material that completely encircles the staircase regions*** (and, of course, fills the portions that the staircase formation removes). Banerjee-Reply, ¶¶31-33. ***Figure 1*** is a top-down block diagram that further illustrates various regions of Kim's memory device, including the CAR (cell array region) and CTR (connection region, i.e., staircase region): … ***As illustrated, the CAR and CTR regions—which embody stack structures—sit on a substrate (portions in blue)*** (which is part of the wafer, see infra)."

Reply 6-7.

- But Petitioner's reliance on Kim Figure 1 is an **improper new claim mapping** on reply—the Petition did not rely on the blue-shaded areas in Figure 1

POSR 7-8; compare, e.g., Petition, 32-38 and Reply, 7; *Ariosa Diagnostics v. Verinata Health Inc.* 805 F.3d 1359, 1364 (Fed. Cir. 2015); PTAB Consolidated Trial Practice Guide 2019, at 7.



Kim, Fig. 1 (annotated by Petitioner).

- Regardless, unlike later figures, Kim's Figure 1 is a "schematic block diagram" that does not show the substrate, let alone a filling structure surrounding the staircase

Kim: "***FIG. 1 is a schematic block diagram*** illustrating a three-dimensional (3D) semiconductor memory device according to some embodiments of the inventive concepts."

Kim: "***Referring to FIGS. 3, 4A, 4B, 5A, 5B, and 5C, a substrate 100 may be provided***. The substrate 100 may include a cell array region CAR and a connection region CTR."

Kim, 4:18-20, 5:53-55, Figs. 1, 3; POSR 8-10.

- Petitioner's new mapping once again ignores that Kim teaches trenches that cut through the staircase

POSR 9-10.

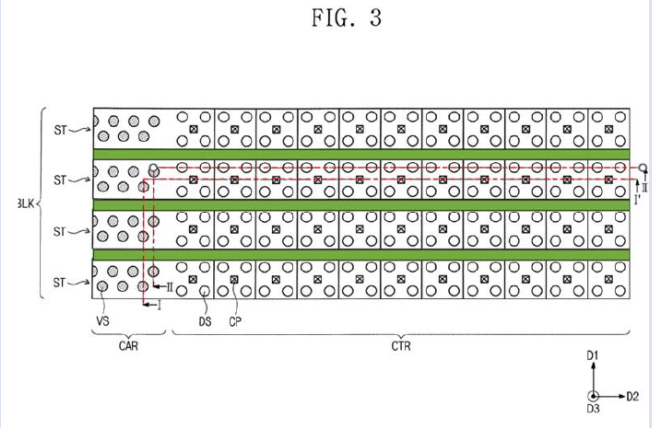
Ground 1 (Kim): Kim Fails to Render Obvious That Its Filling Insulation Layer "Surrounds" the Stack Structure

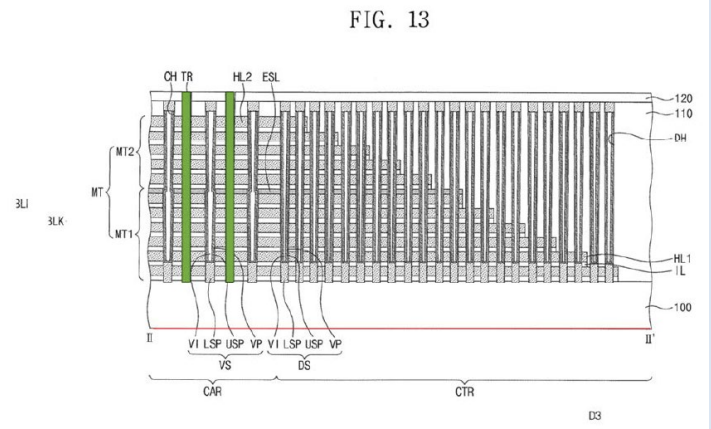
Petitioner argues: Petitioner argues: "[I]n Figure 10 above, Kim discloses filling material on the outer edge of where the staircase region ends (e.g., all the way to the right). Thus, consistent with this filling pattern, ***it would have been understood by a POSITA, and certainly obvious, that the filling material would extend to the outer edge in the other directions***, namely, on the other three sides of the structure. Banerjee, ¶ 112."

Pet. 35.

- But Petitioner's argument that a structure that extends in one direction would also extend in a perpendicular direction is inconsistent with the evidence (e.g., trenches)

POR 36-37; Kuhn, ¶119.





Kim, Figs. 3, 13; Kuhn, ¶¶119, 99-100; POR 36, 27-30.

- In addition, many of Kim's components extend in one direction and not others (e.g., channel structures, dummy structures, contact plugs, common source regions)

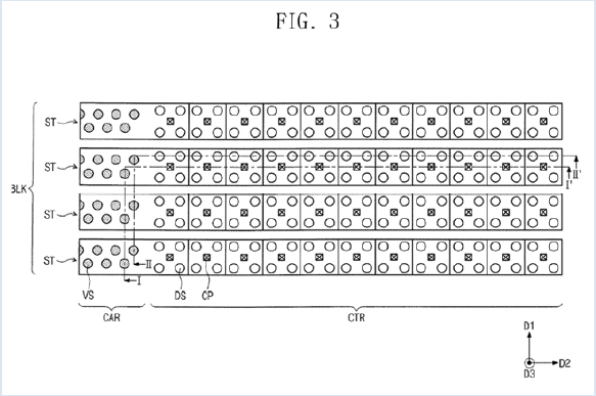
POR 36; Kuhn, ¶¶119-120.

Ground 1 (Kim): Kim Fails to Render Obvious That Its Filling Insulation Layer "Surrounds" the Stack Structure

Dr. Banerjee argues: "***[H]aving uniform filling material on all sides would make for a symmetric device***, which is generally desirable.'"

Ex. 1003, ¶ 113; Pet. 35.

- But **Kim's device is intentionally asymmetrical**, for example Kim's device is different in the D1 and D2 directions:



POR 39-42; Kuhn, ¶¶127-128; POSR 15-16.

- Petitioner's only response is to argue symmetry is not required, but Petitioner tried to support its understanding of Kim by relying on purported symmetry

Petitioner: "***YMTC mischaracterizes the Petition as arguing that each structure must extend symmetrically***"

Reply 18; POSR 15-16.

Ground 1 (Kim): Kim Fails to Render Obvious That Its Filling Insulation Layer "Surrounds" the Stack Structure

Petitioner (citing a different reference, Park) argues: "It was well known that with such a block arrangement, a common technique was to isolate the blocks with, e.g., common source lines 102…. Thus, ***Kim would have been understood to disclose (or at least render obvious) that additional insulating material (filling structure) would exist that encases the array and staircase portions***, resulting in a filling structure on all sides of the staircase structures."

Pet. 36-37 (citing Ex. 1011 (U.S. Pat. No. 10,559,583 to Park), Fig. 3).

- But the teachings of ***Park*** do not explain how ***Kim*** "would have been understood."

Dr. Kuhn: "Kim does not reference Park, Petitioner does not propose combining Kim and Park, and Petitioner does not argue or establish that Park's teachings are the only way to implement Kim's teachings such that it is how Kim "would have been understood.""

Kuhn, ¶134; POR 42-44.

- The argument that such a component is "known" does not mean that a POSITA would have found it obvious to use the component in ***Kim***

PTAB: "[A]n understanding that something '***could*** be applied to the problem at hand' ***does not establish that it would have been obvious to do so*** at the time the [] invention was made."

Costco Wholesale Corp. v. Robert Bosch LLC, IPR2016-00035, Paper 23 at 8 (PTAB Aug. 12, 2016); POSR 17; POR 42-44.

- To the extent that Petitioner's argument is that the insulating liners of the common source in combination with the filling insulation layer 110 show the filling structure of the '031, this combination of elements still fails to render obvious surrounding the stack structure:
  - Kim's device in the -D2 direction is neither depicted nor described
  - Petitioner has not shown that it would have been obvious to surround the stack structure on that side for at least the reasons discussed above

POR 44; Kuhn, ¶137.

Ground 2 (Tessariol): Tessariol Fails to Disclose a Filing Structure That "Surrounds" the Stack Structure

Petitioner argues: "[A]s shown in Figure 6 below, Tessariol discloses that "[a]n ***insulating material 48*** (e.g., silicon dioxide and/or silicon nitride) ***is above steps 40-47***." Tessariol, [0034]."

Pet. 66-67 (citing Tessariol, [0034], Fig. 6).

- But Tessariol's "insulating material 48" covers and does not ***surround*** Tessariol's steps:

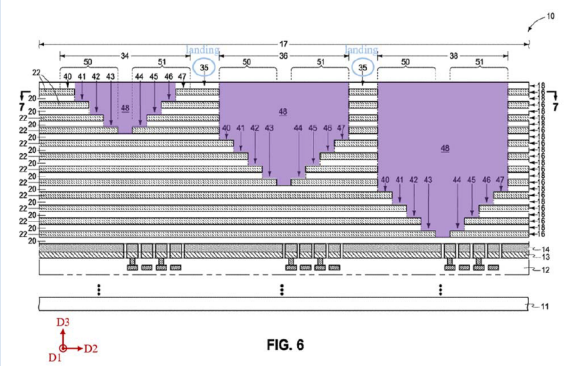


FIG. 6

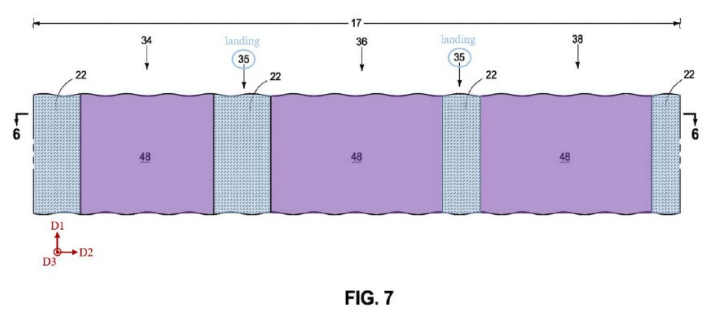


FIG. 7

Tessariol, Figs. 6, 7; POR 57-59; Kuhn, ¶¶182-184.

Tessariol: "An ***insulating material*** 48 (e.g., silicon dioxide and/or silicon nitride) ***is above steps*** 40-47."

Tessariol, [0034]; POR 57; Kuhn, ¶182.

Tessariol: "[T]he stair step structure comprising ***insulating material above the steps.***"

Tessariol, Claims 1, 8, 16; POR 57; Kuhn, ¶182.

- Dr. Banerjee acknowledges that Tessariol does not show the outer ends/sides of the device (i.e., in the D1 and D2 directions in Fig. 7):

Dr. Banerjee: "[T]he figures in Tessariol do not show the outer ends/sides of the device."

Banerjee, ¶184; POR 59; Kuhn, ¶184.

Ground 2 (Tessariol): Tessariol Fails to Disclose a Filing Structure That "Surrounds" the Stack Structure

Petitioner argues: "Tessariol additionally discloses the deposition of "***dielectric material 74" around the staircase structures***. Tessariol, [0043]."

Pet. 67-68 (citing Tessariol, [0043], Fig. 11).

- But Tessariol's "dielectric material 74" ***divides*** and does not ***surround*** Tessariol's steps:

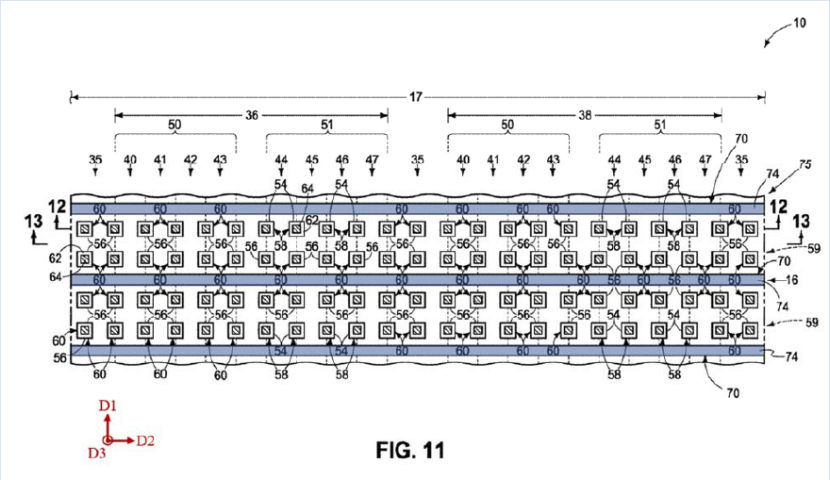


FIG. 11

Tessariol: "For example in the depicted embodiment, and referring to FIGS. 11-13, ***horizontally-elongated trenches 70 (e.g., stack slots) have been formed*** to extend elevationally into vertically-alternating tiers 16, 18. … Then, ***trenches 70 have been filled with dielectric material 74***."

Tessariol, [0041], [0043]; POR 60; Kuhn, ¶186.

- Tessariol does not disclose or suggest that these "horizontally-elongated" trenches are present at the other ends.

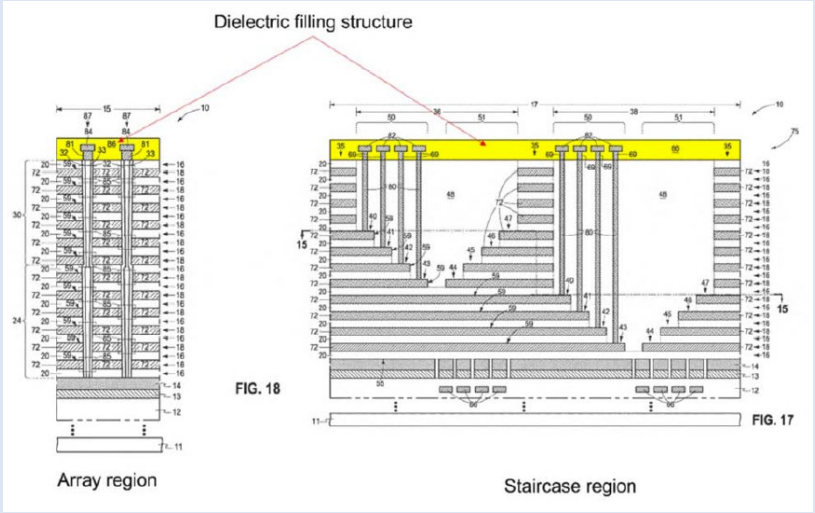
Tessariol, [0041], [0043]; POR 61; Kuhn, ¶187.

Ground 2 (Tessariol): Tessariol Fails to Disclose a Filing Structure That "Surrounds" the Stack Structure

Petitioner argues: "Tessariol ***discloses an additional dielectric filling structure (86)***. Tessariol, [0046] ("Insulator material 86 (e.g., silicon nitride and/or silicon dioxide) is shown surrounding components 69, 82, 81, and 84."). As shown in the below figures, this encases the entire stack structure to provide a region for metal layer connections to the lower layers:"

Pet. 68-69 (citing Tessariol, [0046], Figs. 17-18).

- But Tessariol's "insulator material 86" ***covers*** and does not ***surround*** Tessariol's steps:



Tessariol, Figs. 17-18 (annotated by Petitioner, Pet. 69); POR 61-63; Kuhn, ¶¶189-193.

- While Tessariol discloses that "[i]nsulator material 86 … is shown surrounding components [conductive extensions] 69, [interconnect lines] 82, [conductive extensions] 81, and [conductive lines] 84" (Ex. 1006, [0046]), ***these components are above the stacks, as seen in the figures above***.

POR 62; Kuhn, ¶192; Tessariol, [0046].

Ground 2 (Tessariol): Tessariol Fails to Render Obvious a Filing Structure That "Surrounds" the Stack Structure

Dr. Banerjee: "Based on the knowledge of a POSITA as reflected, e.g., in the Kim reference, ***a POSITA would have understood, or at least found obvious, that Tessariol's "dielectric material 74" and "insulator material 86***" is like Kim's "filling insulating layer 110," and "may be disposed on the substrate 100 and ***may cover" the entire stack structure, and "may have a planarized top surface***." … [S]uch filling insulators are understood to surround the stack structures to create a planar surface for the upper-level metal layer. Ex. 1023, 14."

Banerjee, ¶183 (citing Ex. 1023, 14); Pet. 70.

- But Dr. Banerjee incorrectly conflates ***planarizing*** with ***surrounding***

POR, 63; Banerjee, ¶183; Kuhn, ¶195.

- The cited exhibit (Ex. 1024) is about ***planarization***, and does not include teachings about "***encas[ing] all sides*** of the memory device," as Dr. Banerjee alleges

Ex. 1024, 14; POR 63; Kuhn, ¶195.

Dr. Kuhn: "Planarizing simply refers to making the uppermost layer flat and does not suggest that there is filling material on the sides of the staircase structure in Tessariol."

Kuhn, ¶196; POR 63.

- Additionally, there are a variety of well-known techniques for ***creating embedded air-gaps in planarized structures*** (see slides 22-23), and so it is incorrect to assume that filling material would be on the sides of Tessariol that are not depicted or described.

POR 63; Kuhn, ¶197.

Ground 2 (Tessariol): Tessariol Fails to Render Obvious a Filing Structure That "Surrounds" the Stack Structure

Petitioner argues in Reply: "YMTC ignores the Petition's showing that ***Tessariol's CVD techniques would fully encase the memory structure***"

Reply 24.

- But this is a new argument—neither Petitioner nor Dr. Banerjee quoted Tessariol's single mention of "chemical vapor deposition" ([0063]) before their Reply

POSR 21; Reply 24.

- Regardless, Petitioner makes an unsupported leap from a mere mention of CVD to "fully encas[ing] the memory structure" and surrounding the stack

POSR 21-22; Reply 24.

- As already explained for Kim (slide 23), mere disclosure of CVD does not disclose or render obvious the limitation

POSR 21-22.

Ground 2 (Tessariol): Tessariol Fails to Render Obvious a Filing Structure That "Surrounds" the Stack Structure

Petitioner argues: "Tessariol discloses, or at least renders obvious, ***a filling structure (e.g., insulating material 48, dielectric material 74, and insulator material 86) surrounding the multiple-stack staircase structure*** (e.g., first stack 24 and second stack 30, having staircase regions, e.g., 34, 36, 38 or a two-staircase variation)."

Pet. 70-71.

- But even the combination of these elements fails to surround the stack structure, as ***Tessariol does not teach or suggest an insulator material at the ends of Tessariol's device in either the D1 or D2 direction*** in any of the figures or in the specification

POR, 64; Kuhn, ¶200; POSR 22.

Ground 4 (Tessariol in View of Kim): Tessariol in View of Kim Fails to Render Obvious a Filing Structure That "Surrounds" the Stack Structure

Petitioner argues: "Ground 2 uses Kim to show the knowledge of a POSITA in three areas: … (2) for limitation [1.D], that filling techniques to encase the 3D structure were conventional and routine to employ…. ***To the extent that PO were to argue that Ground 2 must expressly include Kim*** to consider Kim's teachings (which would be incorrect, because an obviousness ground always considers the knowledge of a POSITA), ***Ground 4 combines Tessariol and Kim***."

Pet. 90.

- However, ***the Petition does not raise any new arguments as to limitation [1.d]*** ("a filling structure surrounding the multiple-stack staircase structure")

POR 70-71; Pet. 90-96 (addressing only limitations [1.b], [1.f], and [1.h]); Kuhn, ¶228.

- As explained for Ground 2 (Tessariol), Petitioner fails to show that limitation [1.d] is disclosed or rendered obvious by Tessariol

POR 71; Kuhn, ¶229.

- Even if a POSITA applied Kim's "planarization" technique to Tessariol, as Petitioner suggests, this would result in filling structure with a planar surface, which does not teach a filling structure surrounding the stack

POSR 26.

- Furthermore, a POSITA would not have been motivated to combine Tessariol and Kim:

Dr. Kuhn: "Petitioner's statement that "a POSITA would have been motivated to consider Kim's fill techniques to provide for the planarized surface" is vague because ***the motivation to combine does not state which specific filling technique from Kim would be incorporated into Tessariol and how that incorporation would be executed such that limitation [1.d] would be rendered obvious***."

Kuhn, ¶¶230-231; POR 71.

Dr. Kuhn: "Furthermore, ***Petitioner does not explain why a POSITA would be motivated to combine Tessariol and Kim simply because they both disclose planarized surfaces***."

Kuhn, ¶232; POR 71.

III. “Pillar-Support Material Surrounded by the Insulating Material” Limitation

Claim 4 Requires That the Supporting Pillar Is Filled With at Least One of an Insulating Material and a Pillar-Support Material Surrounded by the Insulating Material

[4] The memory device of Claim 2, wherein:

the supporting pillar and the semiconductor channel are filled with different filling layers; and

the supporting pillar is filled with at least one of an insulating material and a pillar-support material surrounded by the insulating material, and the semiconductor channel is filled with at least one of a charge trapping film, a semiconductor channel film, and a dielectric core.

[5] The memory device of Claim 4, wherein the insulating material comprises silicon oxide and the pillar-support material comprises at least one of copper, cobalt, nickel, and aluminum.

Ground 1 (Kim): Kim Fails to Disclose That "the Supporting Pillar Is Filled with … a Pillar-Support Material Surrounded by the Insulating Material"

Petitioner argues: "Kim discloses embodiments wherein the ***dummy structure DS*** is different than the channel structures. Kim, 13:28-33."

Pet. 55-56.

- But Kim's dummy structures are ***single layer structures*** that do not map to this element

POR 46; Kuhn, ¶143.

- Kim discloses two possible relationships between its dummy structures (the alleged "supporting pillar") and vertical channel structures (the alleged "semiconductor channels"), neither of which satisfies claim 4
  - Claim 4 requires that "the supporting pillar and the semiconductor channel ***are filled with different filling layers" and*** that "the supporting pillar is filled with … ***a pillar-support material*** surrounded by the insulating material."

POR 46-48; Kuhn, ¶149.

- ***First, Kim's disclosure that the dummy structures may be identical to the vertical channel structures does not disclose Claim 4***
  - Claim 4 requires that the "supporting pillars [allegedly Kim's dummy structures] and the semiconductor channel [allegedly Kim's vertical channels] are ***filled with different filling layers***."

Kim: "In some embodiments, each of the dummy structures DS may include a vertical insulating layer VP, an upper semiconductor pattern USP, a lower semiconductor pattern LSP, and a filling insulation pattern VI, like the vertical structure VS (i.e., ***the vertical dummy structures and the vertical channel structures may include the identical layers*** in some embodiments)."

Kim, 9:31-37, 11:49-53; POR 46-48; Kuhn, ¶¶149-150.

Ground 1 (Kim): Kim Fails to Disclose That "the Supporting Pillar Is Filled with … a Pillar-Support Material Surrounded by the Insulating Material"

Petitioner argues: "Kim discloses embodiments wherein the ***dummy structure DS*** is different than the channel structures. Kim, 13:28-33."

Pet. 55-56.

- But Kim's dummy structures are ***single layer structures*** that do not map to this element

POR 46; Kuhn, ¶143.

- Kim discloses two possible relationships between its dummy structures (the alleged "supporting pillar") and vertical channel structures (the alleged "semiconductor channels"), neither of which satisfies claim 4
  - Claim 4 requires that "the supporting pillar and the semiconductor channel ***are filled with different filling layers" and*** that "the supporting pillar is filled with … ***a pillar-support material*** surrounded by the insulating material."

POR 46-48; Kuhn, ¶149.

- ***Second, Kim's disclosure that the dummy structures and vertical channel structures are made from different materials does not disclose Claim 4***
  - This is because for these structures Kim discloses only ***insulator/semiconductor material 11—silicon oxide, silicon nitride, silicon oxynitride, polysilicon—which cannot be used to form a "conductive core" (Petitioner's claim mapping is based on a conductive core being a pillar-support material)***

Kim: "A layer or component of ***each of the dummy structures DS may be different from the layer(s) or component(s) of each of the vertical structures VS***, unlike the embodiment described above with reference to FIG. 4B.."

Kim, 13:29-33; POR 46-48; Kuhn, ¶¶149, 151; Pet. 55-56.

Kim: "The dummy pattern of the dummy structure DS may be formed of a single layer, e.g., ***a silicon oxide layer, a silicon nitride layer, a silicon oxynitride layer, or a poly-silicon layer***."

Kim, 13:33-36; POR 47; Kuhn, ¶151.

Ground 1 (Kim): Kim Fails to Disclose That "the Supporting Pillar Is Filled with … a Pillar-Support Material Surrounded by the Insulating Material"

Petitioner argues: "Given the knowledge of a POSITA, a POSITA would have understood that ***Kim's dummy structures could have been made with a conductive core*** (the supporting material) and insulating liner. Banerjee, ¶ 156 (citing Ex. 1012)"

Pet. 55-56.

- But this argument is not based on any disclosure of a conductive core in ***Kim***

POR 48; Kuhn, ¶142.

- As Petitioner appears to acknowledge, ***Kim does not disclose a conductive core in the cited dummy structures***

POR 48; Pet. 55-56.

- Kim instead discloses that its dummy structures are formed of materials that are not conductive cores

Kim: "The dummy pattern of the dummy structure DS may be formed of a single layer, e.g., ***a silicon oxide layer, a silicon nitride layer, a silicon oxynitride layer, or a poly-silicon layer***."

Kim, 13:33-36; POR 48; Kuhn, ¶143.

Ground 1 (Kim): Kim Fails to Render Obvious That "the Supporting Pillar Is Filled with … a Pillar-Support Material Surrounded by the Insulating Material"

Petitioner argues: "Given the knowledge of a POSITA, a POSITA would have understood that ***Kim's dummy structures could have been made with a conductive core*** (the supporting material) and insulating liner. Banerjee, ¶ 156 (citing Ex. 1012)"

Pet. 55-56.

- ***But Petitioner does not explain why a POSITA would have been motivated to use a conductive core.***

POR 49; Pet. 55-56; Kuhn, ¶154.

- Petitioner has not shown that Kim's device needs or would even benefit from additional supporting structures

Federal Circuit: "[***It does not] suffice[] for obviousness that a variation of the prior art would predictably work, but requires consideration of whether***, in light of factors such as 'design incentives and other market forces,' ***the hypothetical skilled artisan would recognize the potential benefits and pursue the variation***."

Belden Inc. v. Berk-Tek LLC, 805 F.3d 1064, 1075 (Fed. Cir. 2015); POR 49; Kuhn, ¶155; POSR 18.

- Petitioner has not identified a reason to include or modify structures to provide further support than Kim's dummy structures already provide

POSR 18.

Ground 1 (Kim): Kim Fails to Render Obvious That "the Supporting Pillar Is Filled with … a Pillar-Support Material Surrounded by the Insulating Material"

Dr. Banerjee: "[T]he mechanical support provided by a material is determined by its ***elastic properties such as the bulk modulus and Young's modulus***. … Many metals such as Al and Cu tend to deform inelastically without fracturing because they are malleable and ductile. One the other hand, dielectrics such as silicon dioxide and silicon nitride are brittle, and fracture once the yield point is exceeded. ***These properties determine the suitability of a material as the pillar***."

Banerjee, ¶215.

- Dr. Banerjee asserts that it would have been obvious to include a ***metal core***, but ***there is no correlation between electrical conductivity and Young's modulus***.

Dr. Kuhn: "There are some materials (such as indium) with ***very good conductivity and poor Young's modulus*** (11 GPa), some materials (such as copper) with ***very good conductivity and moderate Young's modulus*** (130 GPa), and some materials such as iridium with ***very good conductivity and excellent Young's modulus*** (528 GPa)."

Kuhn, ¶157; POR 50; POSR 19.

- Dr. Banerjee asserts that it would have been obvious to include a metal core, but ***there is no correlation between electrical conductivity and Young's modulus***.

Non-metals	Metals
Glass: 64 GPa, 74 GPa and 100 GPa	Aluminum: 70 GPa
Polysilicon: 150 GPa	Copper: 130 GPa
Silicon nitride: 250 GPa	Cobalt: 209 GPa
	Nickel: 200 GPa

Kuhn, ¶160; POR 50-51; Ex. 1021; Ex. 1022.

Dr. Kuhn: "[T]he Young's modulus for silicon nitride is greater than the Young's modulus for all four metals, the Young's modulus of polysilicon is roughly midway in value for the four metals (and very close to that of copper), and the Young's modulus of "glass" is in a range between aluminum and copper"

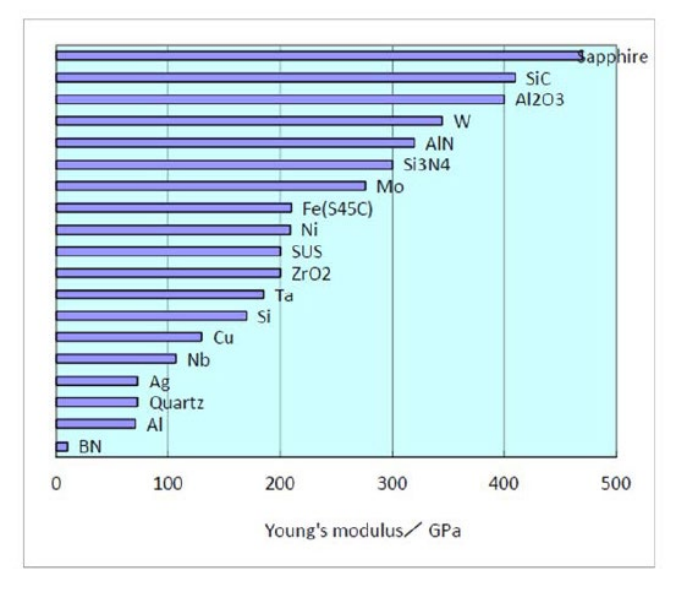
Kuhn, ¶160; POR 50-51.

Ground 1 (Kim): Kim Fails to Render Obvious That "the Supporting Pillar Is Filled with … a Pillar-Support Material Surrounded by the Insulating Material"

Dr. Banerjee: "[T]he mechanical support provided by a material is determined by its ***elastic properties such as the bulk modulus and Young's modulus***. … Many metals such as Al and Cu tend to deform inelastically without fracturing because they are malleable and ductile. One the other hand, dielectrics such as silicon dioxide and silicon nitride are brittle, and fracture once the yield point is exceeded. ***These properties determine the suitability of a material as the pillar***."

Banerjee, ¶215.

- In addition, the chart in Petitioner's own source shows that ***conductors (Al, W) and insulators (BN, Al2O3) can both be positioned at low and high ends of the Young modulus chart***:



Ex. 1021; Kuhn, ¶¶161-163; POR 51-52.

A "Pillar-Support Material" Must Have Sufficient Stiffness and/or Support Functions

Petitioner argues in Reply: "YMTC's arguments attempt to distinguish the prior art by defining "pillar-support material" as having a "***required*** stiffness and/or support function." POR, 45-48. ***This interpretation is inconsistent with the specification***. YMTC cites only a statement as to what material "*can be used* as the support material," not what *must be used*."

Reply 20; *see also* Reply 28.

- Petitioner ignores that the '031 patent clarifies that "[a]ny suitable pillar-filling materials" means "[a]ny suitable material with sufficient stiffness and/or support functions can be used as the support material":

'031 Patent: "***Any suitable material with sufficient stiffness and/or support functions can be used as the support material.***"

'031, 18:26-28; POSR 18, 23-24.

- Petitioner's expert agrees with the "sufficient stiffness and/or support functions" requirement:

Dr. Banerjee: "***[T]he mechanical support provided by a material is determined by its elastic properties such as the bulk modulus and Young's modulus***. … Many metals such as Al and Cu tend to deform inelastically without fracturing because they are malleable and ductile. One the other hand, dielectrics such as silicon dioxide and silicon nitride are brittle, and fracture once the yield point is exceeded. ***These properties determine the suitability of a material as the pillar***."

Banerjee, ¶215; POSR 23-24.

Ground 1 (Kim): Kim Fails to Render Obvious That "the Supporting Pillar Is Filled with … a Pillar-Support Material Surrounded by the Insulating Material"

Petitioner argues: "***Tessariol discloses that supporting pillars may be either conductive vias or dummy versions of the conductive vias***. Tessariol, [0037], [0038], [0041]. Accordingly, ***it would have been obvious simply to use conductive vias or dummy vias*** (which have an insulating liner and conductive core), and this would have been beneficial because the process to form them would use the same process steps as the conductive vias."

Pet. 55-56.

- But ***Tessariol does not disclose the type of metal***, and a "conductive core" by itself is not necessarily a pillar-support material (slides 41-43)

POR 52-53; Kuhn, ¶166; POSR 19.

- Dr. Banerjee's conclusion that using Tessariol's conductive vias in Kim would provide support and interconnect functions completely ***disregards the fact that Kim does not need or even benefit from additional interconnecting structures***

Dr. Kuhn: "***Kim does not disclose any circuitry (either transistors or interconnects) under the memory array or the staircase 13. If there is no circuitry under the array or the staircase, there is no need to create connections to that circuitry***. As such, Kim has no clear motivation to make the dummy structures conductive for an interconnect function."

Kuhn, ¶¶169-170; POR 52-53; POSR 19-20.

- The new vias cited in the Reply are beyond the staircase region, and thus are irrelevant

POSR 20; Ex. 1029 ("peripheral device region 200"); Ex. 1030 ("through-peripheral-stack region 500").

- The other exhibit Petitioner cites (Ex. 1012) does not include information about elastic properties that show pillar-supporting capabilities and, like Tessariol, ***merely mentions pillars with metal cores***

Ex. 1012 (U.S. Patent No. 9,768,186): "The core material 111 may comprise any suitable electrically conductive material, such as a metal material (e.g., a metal or metal alloy, including a metal nitride or metal silicide) or a doped semiconductor material."

Ex. 1012, 4:60-5:12; Kuhn, ¶171; POR 53-54.

Ground 1 (Kim): Kim Fails to Render Obvious That "the Supporting Pillar Is Filled with … a Pillar-Support Material Surrounded by the Insulating Material"

- Petitioner and Dr. Banerjee ignore ***significant issues of thermal expansion mismatch*** that would result from their proposed modification of Kim

> **Dr. Kuhn**: "All materials have a thermal expansion coefficient, which indicates the amount a material will expand over a given temperature change. ***If two adjacent materials are subjected to high temperature, as routinely occurs in semiconductor manufacturing, differences in the thermal expansion coefficient between these materials can cause stress and lead to structural damage such as dislocations or cracks***."

Kuhn, ¶172; POR 54-55.

- The only metal Petitioner proposes using for the conductive core, anywhere in its Petition, is copper (for Ground 2, Pet. 86), which ***has a significantly different thermal expansion coefficient than Kim's insulating materials***

> **Dr. Kuhn**: "[C]opper has a thermal expansion coefficient of 16.6, and silicon oxide has a coefficient of 0.64. During subsequent processing, such an anneal or metal deposition step, ***the structure of copper surrounding by an insulating liner would likely lead to cracking***."

Kuhn, ¶172 (citing Ex. 1021, 3, 9; Ex. 1023 (discussing high temperatures for various processing steps)); POR 54-55.

Ground 2 (Tessariol): Tessariol Fails to Disclose or Render Obvious That "the Supporting Pillar Is Filled with … a Pillar-Support Material Surrounded by the Insulating Material"

Petitioner argues: "Tessariol discloses this limitation. Specifically, "***the dummy structures may individual [sic] comprise a conductive core*** (e.g., 64) and an insulative periphery (e.g., 62)." Tessariol, [0049]. Here, ***the pillar-support material is the conductive core***, which is surrounded by the insulating liner. Id."

Pet. 84.

- Petitioner's argument that Tessariol discloses claim 4 appears to rest solely on the argument that Tessariol's conductive core is a "pillar support material" because the material is a metal

POR 65; Kuhn, ¶205.

- However, not all metals are pillar support materials (slides 41-43)

POR 65; Kuhn, ¶205.

- ***Tessariol does not disclose the type of metal in its conductive core and does not disclose that the metal is a support material***

Tessariol: "The dummy structures may individually be conductive top-to-bottom through the vertically-alternating tiers. The operative conductive vias and the dummy structures may individually be of the same peripheral size and peripheral shape. The operative conductive vias and ***the dummy structures may individual comprise a conductive core (e.g., 64)*** and an insulative periphery (e.g., 62)."

Tessariol, [0049]; POR 65; Kuhn, ¶206.

- Petition provides almost no analysis for this limitation
  - Petitioner does ***not*** argue that Tessariol's metal has ***sufficient stiffness and/or support functions***
  - Petitioner does ***not*** argue that Tessariol's conductive core has a ***supporting function***

POR 65-66; Kuhn, ¶¶208-209; POSR 23-24.

Ground 2 (Tessariol): Tessariol Fails to Disclose or Render Obvious That "the Supporting Pillar Is Filled with … a Pillar-Support Material Surrounded by the Insulating Material"

Petitioner argues: "[*A] POSITA would have understood that by disclosing that the conductive core can be a "metal material," Tessariol discloses that the pillar-support material may be one of "copper, cobalt, nickel, and aluminum."* Tessariol discloses that the dummy structures and metal vias may be the same material. Tessariol, [0038]."

Pet. 86.

- But Petitioner merely quotes the claim language and fails to provide any motivation for using any of those materials in Tessariol's dummy structures, which is improper

Federal Circuit: "*[T]here must be a motivation to make the combination* and a reasonable expectation that such a combination would be successful, otherwise a skilled artisan would not arrive at the claimed combination."

Belden Inc. v. Berk-Tek LLC, 805 F.3d 1064, 1075 (Fed. Cir. 2015); POR 66-67; Kuhn, ¶210.

Federal Circuit: "T*o draw on hindsight knowledge of the patented invention, when the prior art does not contain or suggest that knowledge, is to use the invention as a template for its own reconstruction—an illogical and inappropriate process by which to determine patentability*."

Sensonics, Inc. v. Aerosonic Corp., 81 F.3d 1566, 1570 (Fed. Cir. 1996); POR 66-67; Kuhn, ¶210.

Petitioner argues in Reply: "*According to Tessariol, "metal material" can be "an elemental metal."* *Id*., [0066]. A POSITA would have understood that *"elemental metal" includes any well-known metal from the periodic table used in semiconductor memory fabrication.* Banerjee-Reply, ¶80."

Reply 27.

- But Claim 4 requires a "pillar-support material," which requires a material with "***sufficient stiffness and/or support functions***" (see slides 41-43)
- Petitioner has never shown why Tessariol's unspecified metal has these functions or why it would have been obvious to use a material that does

POSR 23.

Ground 2 (Tessariol): Tessariol Fails to Disclose or Render Obvious That "the Supporting Pillar Is Filled with … a Pillar-Support Material Surrounded by the Insulating Material"

Petitioner argues: "***Copper, a metal material, was a well-known interconnect material***, including in 3D NAND devices. Ex. 1014 (U.S. Pat. No. 9,299,641), 2:32-43 (copper interconnects); Ex. 1015 (U.S. Pat. No. 11,244,725), 11:36-44 (copper interconnects); Banerjee, ¶ 211."

Pet. 86.

- But whether copper was "well-known" is not the test for obviousness

POSR 24.

- Petitioner needed to show ***why*** a POSITA would have been motivated or found it obvious to use a particular material in Tessariol's dummy structures, which it did not

POSR 24; POR 66-67; Kuhn, ¶211.

- Petitioner does not address that copper poses significant diffusion and contamination issues:

Dr. Kuhn: "While Petitioner cites a reference that discloses that copper was well-known, ***it is also well known that copper poses significant diffusion and contamination issues*** in the processing of transistors and memory cells and Petitioner does not explain how a POSITA would have been motivated or found it obvious to use copper (with all its attendant risks) in Tessariol's dummy structures."

Kuhn, ¶211; POR 66-67.

Ground 2 (Tessariol): Tessariol Fails to Disclose or Render Obvious That "the Supporting Pillar Is Filled with … a Pillar-Support Material Surrounded by the Insulating Material"

Petitioner argues in Reply: "***Tessariol discloses exactly what the '031 patent discloses***."

Reply 28.

- But unlike Tessariol, the '031 patent discloses the properties of "pillar-support materials" and gives examples of such materials:

'031 Patent: "Any suitable material with ***sufficient stiffness and/or support functions*** can be used as the support material. For example, the support material ***can include one or more of copper, cobalt, nickel, and aluminum***. "

'031, 18:26-30; POSR 23.

Ground 3 (Kim in View of Tessariol): Kim in View of Tessariol Fails to Render Obvious That "the Supporting Pillar Is Filled with … a Pillar-Support Material Surrounded by the Insulating Material"

Petitioner argues: "Ground 1 uses Tessariol to show that the use of such dummy structures was well known to a POSITA. Id. ***Ground 3 expressly combines Kim with Tessariol to demonstrate the same point***: Kim in view of Tessariol would ***render obvious employing a conductive core*** and insulating liner as the dummy pillars in Kim."

Pet. 86-88.

- But as explained for Ground 2, ***Tessariol does not disclose or render obvious limitation [1.d]*** (slides 46-49), and so the combination of Kim in view of Tessariol fails to cure the deficiencies in Kim

POR 67; Kuhn, ¶¶213-215.

- Petitioner again ***fails to show that a POSITA would have been motivated to make this proposed modification***:
  - ***First***, Petitioner has not shown that Kim's device needs or would even benefit from additional supporting structures (slide 44)
  - ***Second***, Kim has a PNC architecture with no transistors or circuitry under the array or the staircase, and therefore has no need to make its dummy structures conductive for an interconnect function (slide 44)
  - ***Third***, contrary to Petitioner's assertion, metals do not always provide better support than insulators (slide 41-43)
  - ***Fourth***, a POSITA would not be incentivized to add a conductive core to Kim because that would unnecessarily complicate the manufacturing process
  - ***Fifth***, Petitioner does not explain why a difference in the material in Kim's dummy and channel structures would prompt a POSITA to incorporate Tessariol's conductive vias into Kim's structure

POR 68-69; POSR; 24-26; Kuhn, ¶¶216-222.

Ground 3 (Kim in View of Tessariol): Kim in View of Tessariol Fails to Render Obvious That "the Supporting Pillar Is Filled with … a Pillar-Support Material Surrounded by the Insulating Material"

Petitioner argues in Reply: "[A] conductive core ***would not complicate the manufacturing process***. Banerjee ¶218."

Reply 29.

Dr. Kuhn: "[A] POSITA would not be incentivized to add a conductive core to Kim because that ***would unnecessarily complicate the manufacturing process***."

Kuhn, ¶219; POR 68.

Dr. Banerjee: "[T]he support pillars described in Tessariol include both an insulating liner and a conductive core. ***Kim's fabrication process already employs such structures that extend through the stack, namely, a common source line***."

Banerjee, ¶218.

- But Kim's common source line (CSR) is not analogous to a dummy structure with a conductive core, because unlike the dummy structures, the CSR:
  - (1) is a long extensive structure
  - (2) is not disclosed as connected to peripheral circuitry
  - (3) does not include a conductive core (it includes a doped semiconductor)

POSR 24-25.

Kim: "***The common source regions CSR may be arranged in the first direction D1***. The common source regions CSR may be ***doped with dopants*** and may have a second conductivity type."

Kim, 6:11-22; POSR 25.

Dr. Banerjee: "***[I]t would have been obvious simply to use conductive vias (which have an insulating liner and conductive core) in Kim's dummy structures***, and this would have been beneficial because ***the process to form them would use the same process steps as the conductive vias***."

Banerjee, ¶¶157, 216.

- But this makes little sense, because Kim does not disclose anything about forming conductive vias and, thus, there is no "same process steps as the conductive vias" in the reference

POR 69; Kuhn, ¶221.

Ground 3 (Kim in View of Tessariol): Kim in View of Tessariol Fails to Render Obvious That "the Supporting Pillar Is Filled with … a Pillar-Support Material Surrounded by the Insulating Material"

Petitioner argues: "***Kim expressly recites that the dummy structures need not be the same material as the channel structures***. Kim, 13:28-33. This would have motivated a POSITA to consider other types of support pillars, and Tessariol provides such other types."

Pet. 87-88.

- But Petitioner does not explain why a difference in the material in Kim's dummy and channel structures would prompt a POSITA to incorporate Tessariol's conductive vias into Kim's structure

POR 68-69; Kuhn, ¶220.

Ground 4 (Tessariol in View of Kim): Tessariol in View of Kim Fails to Render Obvious That "the Supporting Pillar Is Filled with … a Pillar-Support Material Surrounded by the Insulating Material"

Petitioner argues: "Ground 2 demonstrates that claims 1, 2, and 4-5 are obvious in view of Tessariol and the knowledge of a POSITA. Ground 2 uses Kim to show the knowledge of a POSITA in three areas: (1) for limitation [1.B], … , (2) for limitation [1.D], … , and (4) for limitation [1.H],…. ***For all other limitations, Ground 4 relies on the same disclosures as Ground 2. Thus, the sections below only address limitations [1.B], [1.F], and [1.H]***."

Pet. 87-88.

- Thus, ***Tessariol in view of Kim fails to disclose these claims for the same reasons explained in Grounds 1 and 2***

POR 72; Kuhn, ¶¶234-235.