

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,

Petitioner

v.

YANGTZE MEMORY TECHNOLOGIES CO., LTD.

Patent Owner.

IPR2024-00790

Patent 10,868,031 B2

Record of Oral Hearing

Held: July 31, 2025

Before JO-ANNE M. KOKOSKI, KIMBERLY McGRAW, and
MICHAEL T. CYGAN, Administrative Patent Judges.

APPEARANCES:

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P-R-O-C-E-E-D-I-N-G-S

1:05 p.m.

JUDGE KOKOSKI: Good afternoon. Today we will hear arguments in IPR 2024-00790, concerning U.S. Patent number 10,868,031. I'm Judge Kokoski, and I'm joined today by Judge McGraw and Judge Cygan. Let's start with appearances, beginning with Petitioner.

MR. LANG: Good afternoon again, Your Honors. Jason Lang, counsel for Micron, with me is -- Micron representative.

JUDGE KOKOSKI: Thank you, welcome. Patent Owner?

MR. DAVIS: Good afternoon, Your Honors, for day three. James Davis for the Patent Owner. Along with me is Mr. Bonny, Allen Cross, Andrew Radsch, all from Ropes & Gray, and with us as well is Daniel Chang from YMTC.

JUDGE KOKOSKI: Okay, welcome, or welcome back, as the case may be. Before we begin, I'd just like to remind you again that we each have a copy of the demonstratives, but please, during your argument, try to identify the slide, that's particularly useful for Judge McGraw, who cannot see the screen in the room.

JUDGE MCGRAW: Thank you.

JUDGE KOKOSKI: As set forth in our hearing order, each party has 60 minutes to present their arguments. Petitioner will proceed first, may reserve time for rebuttal. How much time would you like to reserve?

Mr. LANG: 15 minutes, Your Honor.

1 JUDGE KOKOSKI: 15 minutes? Okay, Patent Owner will then
2 have 60 minutes to present their case and may also reserve time for a
3 surrebuttal. How much time would you like to reserve?

4 MR. DAVIS: 15 minutes, Your Honor.

5 JUDGE KOKOSKI: 15 minutes.

6 MR. DAVIS: Thank you.

7 JUDGE KOKOSKI: Okay. Petitioner, you can proceed when you're
8 ready.

9 MR. LANG: Well, again, good afternoon. I'd like to start with
10 turning to slide 4, just an overview of the grounds. There are four grounds,
11 but there's two primary references, Kim, we argue claims 1 through 4 are
12 obvious over Kim. For claim 4, we do rely on Tessariol, Exhibit 1012, as
13 the knowledge of a POSITA, and there's a separate ground, Kim, in view of
14 Tessariol, which is very similar, it just expressly combines Tessariol with
15 Kim. The arguments against that are -- there's an argument that the filling
16 structure does not surround the multi-stack staircase structure, and there's an
17 argument regarding the pillar.

18 The Tessariol ground, the arguments are very similar, except there's
19 also claim 5 challenged, which, there's a separate argument relating to
20 copper that I'll get into. Turning to slide 6, I just want to take a step back
21 here and note, the point of alleged novelty in this patent was this idea of
22 having unaligned channel structure, where you have basically two sub-
23 channels. That's not at issue here today. What you'll see is at issue is
24 known prior art elements operating according to their established functions.

1 And we cite, quite frequently, *Uber* and *Intel/Qualcomm*, and I'll get into
2 that a bit later.

3 I also want to point out the filling structure here, I'll get into here, it's
4 a small claim construction issue relating to that, but the first issue we're
5 going to be talking about is filling structure, whether it surrounds this multi-
6 stack staircase structure. That's shown there, and Patent Owner's
7 annotations in purple on the right. Also, to the left, you see a supporting
8 pillar in light blue.

9 Turning to slide 8, now, what's the description of how you make this
10 filling structure? Any suitable dielectric material, any suitable deposition
11 method, CVD, such as CVD. You basically deposit it and you planarize it,
12 such as with CMP. Very dearth disclosure. Turning to slide 9, the same is
13 true with the pillar. Indeed, the pillar is described in the background section
14 of the '031 Patent. Any suitable filling material. In some embodiments, you
15 can have an insulating liner and it can be made with metal. Any suitable
16 material with sufficient stiffness and support. Again, a very dearth
17 disclosure.

18 Turning to slide 11 -- that's better. So, the filling structure surrounds
19 this multi-stack staircase. The multi-stack staircase is this dual deck
20 structure that has a staircase structure to it. So, skipping to slide 12, the
21 petition had established that Kim has this dual deck multi-stack staircase
22 structure. There's no dispute on that. Further, turning to slide 13, the
23 petition established that, indeed, the fill material 110 surrounds all sides.

24 JUDGE KOKOSKI: Counsel, can I just stop you there? How are
25 you construing "surround" for purposes of these arguments?

1 MR. LANG: We have applied “surround” to be all sides. I’ll make a
2 couple minor points on that, and I can do that right now. The two points I
3 would make -- I read the Board’s construction, I read Patent Owner’s
4 construction, that it does not require surround on the top. And, of course,
5 the reason for that is, as Patent Owner annotates itself there, there’s no
6 purple on top. Indeed, in other figures of the ‘031 patent, the pillars and the
7 channel structures extend up through the top, and of course, that is the case
8 because this is a memory. It’s not a wireless memory, connections need to
9 be made to it.

10 The second point I would like to make is to Dr. Kuhn’s testimony, and
11 I’m turning to slide 19. Here’s what Dr. Kuhn said, this is Patent Owner’s
12 expert. She wanted to clarify a point. She says, I’m not equating encircling
13 with there being a contiguous structure that is connected all the way around.
14 I don’t have all these dictionary definitions in front of me, but I believe one
15 of them makes some comment about policemen encircling a house. Not that
16 the policemen are all holding hands. So, she’s saying that it doesn’t require
17 a continuous structure, it needs to surround on all sides, but she’s -- I think
18 she’s recognizing the fact that this is a memory, things have to make
19 connections. We talked about surrounding two days ago, it doesn’t
20 necessarily require a continuous structure. Indeed, it can disclose a
21 continuous structure all around, but I would say that is not necessary.

22 So, I want to -- and I’ll talk a lot, I’m on slide 15 now, but what the
23 petition pointed to importantly, is if you see that right arrow there, the
24 staircase structure ends at that point. But yet, the filling material 110
25 continues. It continues past the staircase structure. And Dr. Banerjee

1 describes, in his first declaration, none of the CVD stuff is new. That's his
2 first declaration, that what would be understood by this coverage language,
3 that it covers a substrate, is a CVD -- typical CVD deposition discusses the
4 pressure of the gas, how it basically conforms to all of the structures on the
5 substrate and the wafer, and I'll get into that shortly.

6 The Board instituted -- they preliminarily construed encircling to be
7 all around something. And again, the only points I would make, Kim clearly
8 discloses it all around. Even Patent Owner, their expert doesn't say it needs
9 to be contiguous. Kim is contiguous, and there's certainly no requirement
10 that it has to surround on the top, otherwise you'd have an encased memory
11 that can't communicate with the outside world.

12 So I'll jump to slide -- and I will make one further point, Your
13 Honors, on slide 22. I feel like there was some confusion in the briefing,
14 and there may be to this day. The point we were trying to make with the XY
15 plane, if you look at slide 22, in the purple that Patent Owner annotated. So,
16 to the right is the X plane, and behind the page, or in front of the page,
17 would be the Y. So you basically have an XY filling material on one side,
18 XY filling material on the other side, and those are two XY planes. And all
19 we were trying to make the point in the briefing was, yeah, there are two XY
20 planes on each side, and that's one example that they've given of
21 surrounding. But I will submit that these are minor issues in view of Kim
22 disclosing it fully encircling. And I want to focus my time on that.

23 And before I do that, I think it's important to discuss Kim's express
24 disclosures, the knowledge of a POSITA a bit, and then we'll get into Patent
25 Owner's specific arguments. So, turning to slide 25, Kim does disclose

1 CVD. In this example, he's talking about insulating layers. Those are the
2 big, long layers that form the stack, but the point is, is that -- the larger point
3 is, is that the disclosures, the filling insulation layer may be disposed on the
4 substrate and cover the stack. Then you will planarize it. I'll get into the
5 import of that. Indeed, it says again, filling insulation layer 110 may be
6 formed on an entire top surface of the substrate to cover the mold structure.
7 So, you're not just putting in a mold structure, it's going over the whole
8 substrate, and there's more.

9 Turning to slide 26, when it describes forming this, they basically say
10 that there's this block, BLK. Okay? That includes the stack structure, the
11 staircase, all of that. They say, that may be disposed on the substrate. Now,
12 after you put that block on a substrate, it describes forming on the entire top
13 surface of the substrate, the filling structure. So, you've got something on
14 the substrate and then all over the substrate, and the stack structure, you're
15 covering it. So you cover it all sides, and the figures make that very clear.
16 And let me jump to slide 28 on the figures.

17 So again, on Figure 4A on the left, you see the stack structure stop,
18 but to the right of it is still filling, the filling material. This is Kim's, what
19 both parties agree is a 90-degree angle, rotated angle. So when I look at that
20 light green on the right part of these figures, I have a cross section of that
21 light green. And notably, you see where Figure 3, you see where that
22 structure ends, and 4A you see where it ends. The insulating layer is all the
23 way to the right of it. So when it's saying you cover the substrate, indeed
24 you are putting it all over the stack, past the stack, onto the substrate. It has
25 a 90-degree bend, so in that light green, or light blue it may be, I have a

1 cross section of that on the left. And I still see the 110 on top. So, that is
2 just going to the point where its's covering the whole thing, it includes the
3 substrate, so it goes beyond the device.

4 And, going back to slide 27, Patent Owner continues to say, Kim's
5 specification provides limited information about filling insulation layer. It
6 says only that it covers the stack on top. I do not see how you can square
7 that with Figure 4A that shows 110 directly on the substrate. There's no
8 way to square Patent Owner's argument with sitting there, looking right
9 there, seeing 110 on the substrate. It does not just cover the top. Kim says it
10 three or four different times.

11 Turning to slide 29, everything's consistent with this. Figure 1, Patent
12 Owner points out it's a schematic. Indeed, it is, but just like all the other
13 descriptions, what it represents is that you're laying out these blocks, you're
14 laying out these modules, onto a substrate. Okay? And the insulation layer
15 then is going not just on top, it's covering all sides and it continues onto the
16 substrate. Turning to slide 30, I think this is important, Your Honors. It just
17 further confirms how a POSITA would understand Kim. Dr. Kuhn's
18 testimony is consistent with this. How are these devices really made? I
19 haven't held a wafer in five or six years, but, you know, these are, you
20 know, a foot or something, and about like this. And that's what's shown in
21 the picture above pattern. And each one of these memory devices are on that
22 wafer, there may be 100 of them. And, when they're talking about the CVD
23 deposition covering the substrate, it's covering the whole wafer. So you've
24 got all these devices on there, you're putting the CVD down, and it's just
25 covering everything.

1 Turning to slide 31, Dr. Banerjee explained this. This notion of
2 covering, it's a basic CVD technique. It's been known textbook material for
3 decades. Dr. Banerjee explained it with respect to Exhibit 1027. What you
4 see there is structures that kind of go up and down, but the CVD -- he
5 discusses the gas pressures, what causes this, it's often referred to as
6 conformal deposition. The CVD deposition lays this dielectric all over, and
7 it just conforms to the topology of the wafer. Again, the hundreds of devices
8 on the wafers, all of those structures, it just conforms and puts a layer of
9 dielectric that just follows the topology of all of the structures. It's shown
10 here in 1027.

11 And Dr. Banerjee further explained the point about planarization. So,
12 if you look at this figure from 1027, he cites, I believe it's Exhibit 1014, and
13 you read through those sections. When you're depositing the CVD, you
14 know, it's going to conform to that structure. So if you want to planarize it,
15 what do you have to do? You just keep depositing, keep depositing, and it's
16 going to look like this still at the top, and then you can planarize it because
17 you build it all up enough where you can planarize it. And that's what these
18 references are showing.

19 Turning to slide 32. And look, Dr. Kuhn's testimony is consistent
20 with this. When we asked her about conformal deposition, she said, you
21 know, space is created by removing, what have you, parts of the dielectric
22 stack, and then in a typical conformal CVD process. Again, you look at how
23 the '031 patent described this. These processes have been being done for
24 decades. She describes it as a blanket of CVD that's across the entire wafer.
25 Again, she agrees with this. The substrate is actually just over the whole

1 wafer, but it is following the topology of the wafer. That means all of the
2 structures it's covering.

3 Turning to slide 33, now, let me get into their specific arguments with
4 that context, if I may. They bring up a first argument about, where there's
5 trenches. And I will submit that fails for at least three reasons. And I want
6 to go over, actually, the second reason first. Even if we were to assume
7 these trenches were in here. These trenches are internal structures, okay?
8 And how do we know that? And we see -- I'm pointing to one here in this
9 figure, in this light blue and -- now, it is sticking out of the top, I've already
10 talked about that, but we know it's internal -- we'll go to slide 28, because
11 you see, these are the trenches before they're filled, between the ST stacks.
12 Where do they stop? And the patent describes it, they're a trench built
13 through the stack, okay? So, they stop at the end of that stack, on the right.
14 But, what's to the right of it? More insulation fill 110. So this is nothing
15 but a -- if you imagine that, like, a top-down view, you have your structure,
16 your 110, and internal to that, you're making a trench on the inside of this.
17 110 is still surrounding that trench, and that right side is going to look
18 exactly like the left side of this device because you are covering the
19 substrate. So, this trench is no different than a channel structure that's inside
20 the memory array. There are staircase contacts that are inside, that a
21 structure -- that there is something inside my house does not mean that it's
22 not encircled by police.

23 So, skipping back to slide 32, the trenches are optional, too. He
24 pointed out that the specification said you may have trenches, they said,
25 well, Kim uses "may" a lot. I would submit "may" is still a permissive

1 word, but more importantly, when you look at the context, what Kim is
2 saying is that this is an option to create a multi-block or multi-sub block
3 architecture. So you could just have this one stack structure or you could
4 split it into four sub-blocks -- four blocks, what have you, architecture. So
5 it's clearly an optional architecture. Internal structure is optional.

6 Third, they have an insulating liner. So, to the extent that they're
7 saying that these are some type of air gaps, that is not the case. They are not
8 air gaps, okay? A fourth reason it fails, they do not stick out of the stack.
9 They are not air gaps, if that's what Patent Owner is saying. They are
10 internal structures, but even if they did, their own expert said encircling
11 doesn't require a continuous structure. So, trench argument fails. Well, they
12 say --

13 JUDGE McGRAW: Excuse me, if you don't mind, could you go
14 back to slide 34? Figure 14. Where is the D direction? Is that horizontal,
15 left to right?

16 MR. LANG: This is a 90-degree -- so, I believe the D direction -- let
17 me go to an earlier figure to explain. So, the right side of that picture
18 correlates to the green there. So you would be looking at a cross section
19 with the D and the -- going to the right. But --

20 JUDGE McGRAW: And so patent -- oh, go ahead, I'm sorry.

21 MR. LANG: Yeah, but when you're looking at the left-hand side of
22 the figure, the D direction actually goes in that -- you would be looking on
23 the D1 direction, would be right and left.

24 JUDGE McGRAW: So Patent Owner's argument is that, in Figure 3,
25 the D2 direction goes left and right, and their argument is that Petitioner has

1 not shown that there is insulating material to the left of the staircase
2 structure, is that correct?

3 MR. LANG: That's one argument they make, and that's what I will
4 address right now.

5 JUDGE MCGRAW: Okay, thank you. I don't mean to throw you off
6 of your --

7 MR. LANG: No, no, not a --

8 JUDGE MCGRAW: -- your -- as long as you cover it.

9 MR. LANG: Not a problem, please ask me what you will. Yes, the
10 second argument is that -- yeah, I think you're getting to this, I'm sorry I
11 didn't pick up quicker on it, is in this minus two D direction, which, going
12 back here, would be to the left of this picture. And they make this argument
13 because, I guess, they say, well, you can't see it. I mean, it really reminds
14 me of that old saying, you know, you're in the forest and the tree falls down
15 but you have your eyes closed, you hear it, you look, and there's a tree, did
16 the tree fall down? Yeah. Kim is clear that he's not showing the complete
17 figures, and in fact their expert finally agreed with that, they agreed with
18 that. And so, you come down to -- it comes back to, what does Kim
19 disclose? The filling insulation layer may be formed on an entire top surface
20 of the substrate. So, that's to the right of the structure is the substrate, to the
21 left of the structure is the substrate. So indeed, it does cover it and go all the
22 way, just like the right-hand side. In fact, when it's on a wafer, it's even
23 more clear. This is one chip in a whole wafer, that thing is covering the
24 whole wafer. So, absolutely, it covers it.

1 I think -- they bring up this notion of air gap. And I'm not sure I've
2 fully understood these arguments, because if they're talking about an air gap
3 in a trench, again, that's the internal structure. If my house is encircled by
4 police, and I have an air gap in my house, it's still encircled by police. I'm
5 not sure if they're saying that maybe there's an air gap on the left-hand side
6 or some exposed air gap somewhere, but the trenches are internal and,
7 regardless, air gap is completely irrelevant to this ground. We asked your
8 expert, does Kim disclose anything about air gap? I don't recall. Okay?
9 She would have recalled if there was something there, and there's never
10 been any citations to Kim to discuss air gap. In fact, Dr. Kuhn said the
11 names for air gap was well known, they were air gap or buoyed void if it
12 was accidental. Don't see those words in Kim. Okay? Kim discloses the
13 opposite, fill the deposition to cover the substrate.

14 Indeed, turning to slide 37, they cite Exhibit 1015. Well, that says
15 you can do an air gap or fill it with dielectric material. What does Kim
16 disclose? Filling the trench with dielectric -- okay? So, it's the opposite of
17 air gap. In fact, Patent Owner's evidence 2009 says, well, the main
18 drawback is you need the special lithography for it. It's very expensive.
19 And this goes back to the point where Dr. Banerjee explained with the
20 symmetry of the device, when Kim is saying you just cover the whole thing,
21 and that, you know, after all, it's an insulation layer. You're insulating it,
22 you're electrically isolating it, you don't need any more manufacturing
23 steps, because you just put it all over it. What do they say? Well, you could
24 use these very special lithography or very expensive techniques to do it
25 instead, but this isn't an inherency case, so these arguments are irrelevant.

1 Now, then they bring up, turning to slide 38, Your Honors, this
2 argument about Figure 24, that we never relied on, in a different
3 embodiment. And I just have to make a few points about it. Okay, we
4 didn't rely on it, relates to alternative embodiment. They keep saying this
5 purple is the filling structure. Not so. It's called MP3. It stands, not
6 surprisingly for, mask pattern three. They're illustrating a technique to form
7 a trench, okay? Now, we know that the filling structure is not shown
8 because there is filling structure above the steps where they're showing a
9 mask and step. More importantly, as I talked about in Figure 4, you
10 remember the insulation layer 110 extends beyond those steps. You
11 remember, it extends beyond those steps. There's no filling insulation
12 material even shown here. So, it's irrelevant for --

13 JUDGE McGRAW: So when you say the filling material extends
14 beyond the step, do you mean it extends to the left side?

15 MR. LANG: All sides. All sides. Let me jump back to the figure,
16 Figure 4. So, this is just showing half the device, okay? You see in --

17 JUDGE McGRAW: Figure 14 or Figure 4?

18 MR. LANG: Both of them. Neither of them show the full device.
19 Okay? And to the right, you do see the right full side of the device, and you
20 see the light green, which is the filling material, that extends past the stack
21 structure, and it goes all the way up. And it's on every side, because what
22 does it mean to cover the substrate? that's what you see on the right. The
23 filling material is on the substrate to the right of the stack structure. It is to
24 the left, as well, because it says you cover the whole substrate, you cover the
25 whole mold structure, which is this multi-deck staircase structure.

1 And at bottom, you look at the '031 Patent, turning to slide 39, in the
2 Kim, they disclose the exact same thing. It's a dielectric filling material that
3 you deposit, that you planarize, and Kim, in fact's, disclosures are even
4 more clear than the '031, because it says you cover the whole substrate.
5 Now --

6 JUDGE MCGRAW: If you could go back, again, to slide 39? Where
7 does the staircase structure end of the left side? Is that shown in Figure 4B,
8 or not?

9 MR. LANG: No, it's not shown.

10 JUDGE MCGRAW: Okay.

11 MR. LANG: So, what I want to stress is, it says that you cover the
12 stack structure. It says that you cover the substrate. What does that mean?
13 That is shown on the right. The filling material goes over past the stack
14 structure onto the substrate. Therefore, what you see on the right is going to
15 be around every edge, every side. You cover the whole substrate.

16 JUDGE CYGAN: Counselor, how do we know what's on the left-
17 hand side in Kim?

18 MR. LANG: It describes it, that it's a memory device with the
19 various regions. I mean, we could go back to Figure 1, slide 29. So -- and
20 they have various pictures to how they lay this out, but there's going to be
21 the entire device, schematically. And so, you're going to have -- what
22 they're showing is a staircase on the right, and you're showing the cell
23 region on the left on those figures, and a cell region is going to complete.
24 They say that you put the block down, the block is a whole memory device.

1 The left part of the block, which is just a continuation of the memory cells,
2 it's just not shown.

3 JUDGE CYGAN: So, how do we know that it's not just a single
4 staircase?

5 MR. LANG: Well, the claim only requires that you surround the
6 multi-stack staircase structure. So, the multi-stack staircase structure, going
7 back to the petition, the multi-stack staircase structure has to be two
8 structures, each with a staircase region. And they've never argued that the
9 claim requires, you know, a staircase structure on all four sides. So they
10 would have laid that argument, if that's what you're getting to. The claim --
11 and I'll go back to the claim. There we go. The multi-stack staircase
12 structure comprising a plurality of staircase structures stacked over the
13 substrate. And the petition explains this, the staircase structure, it includes a
14 deck in which part of that deck has a staircase. So, you're not surrounding
15 the staircase, you're surrounding this whole unit.

16 JUDGE CYGAN: So, which is your multiple staircase structure,
17 then?

18 MR. LANG: They've never argued against this. Each one of those is
19 formed separately. The bottom one's formed, it has a staircase structure,
20 that's ST. See ST1? That's the first staircase structure, and on the right is
21 the staircase part of it. And then on top, they build an ST2, and on the right
22 is another staircase built on top of that.

23 JUDGE CYGAN: So, are you contending that just two of those
24 together are the multiple staircase structure?

25 MR. LANG: Yes, and that's never been disputed.

1 JUDGE CYGAN: And to be surrounded, it has to be surrounded on
2 all four sides, is that correct?

3 MR. LANG: That's what the Board preliminary construed. We'd
4 have --

5 JUDGE CYGAN: So, how do we know that's surrounding it on the
6 left hand side?

7 MR. LANG: Because it's -- I've got to go back to this language
8 again. The block. The block may include the staircase structures, ST.
9 That's the ST. That's the whole kit and caboodle, the whole structure, okay?
10 So, it's put on the substrate, and then you cover the whole thing. You cover
11 the whole thing because it says you cover the substrate. You cover the entire
12 top surface of the substrate. What does that look like? When you cover the
13 whole top surface of the substrate, you're not just covering the stack
14 structure ST. It goes beyond that, substrate 100, you're covering past the
15 structure.

16 JUDGE CYGAN: I guess my question is if on the left side there's no
17 staircase on the left and it just ends at the same point that the substrate ends,
18 then there would be no insulation on the left-hand side.

19 MR. LANG: That's not correct, because your substrate on the left,
20 and you're saying you're covering the whole substrate.

21 JUDGE CYGAN: How do we know the substrate extends past the
22 stack on the left?

23 MR. LANG: Well, for one, because these things are put on a wafer.
24 And she -- Dr. Kuhn agrees with -- well, I've got to find that. There you see
25 it, number one. B, it says if you dispose this on the substrate, not like on the

1 edge of the substrate. And two, it says that it covers the substrate. So it has
2 to be substrate over there to cover. Three, as Dr. Banerjee explained, the
3 whole point of this is you're isolating it. Fourth, the way that conformal
4 CVD deposition works, it doesn't even matter if there's not substrate over
5 there, because you're in a bit, you're on a wafer, your CVD is coming down,
6 and it's conforming to every structure on that wafer. So, even if you wanted
7 to say that thing was on an edge, even Dr. Kuhn testified, across the entire
8 wafer, topology of the wafer. So, anything on that wafer, it goes onto. So, it
9 can be on the edge, and it conforms to that edge.

10 JUDGE CYGAN: Is Figure 1 a semi-conductor memory device, or is
11 it a single wafer?

12 MR. LANG: This is a schematic of one device that would be built on
13 a wafer.

14 JUDGE CYGAN: How do we know it's a single wafer?

15 MR. LANG: No, I said that's a schematic of one device that would be
16 built on a wafer. How do we know that? Both experts testified that's how
17 all of this is done. And Your Honor, to kind of address your question, we
18 also argued obviousness. And what Dr. Banerjee explained is that you
19 would want to make this symmetrical, why? So you have that insulation to
20 the right. Okay? You're going to do the same thing on the left, because
21 then you isolate the whole thing and you don't need any extra manufacturing
22 steps. What Patent Owner has said is, well, you could do some type of air
23 gap. Okay? This isn't an inherency case, it's saying you're covering the
24 whole substrate. It's certainly at least obvious that you're doing that on the
25 left in view of Kim's expressed language. Dr. Banerjee did not testify that

1 the filling material, turning to slide 43, would be on one side. He said it
2 would similarly extend to the outer edges of the device as well.

3 So, where this really comes down to is, Kim is saying that you cover
4 the whole substrate and they have come up with this air gap stuff that's
5 found nowhere in Kim. The mere possibility that something might exist,
6 other than covering it all, even though Kim says cover it all, does not defeat
7 obvious. And with the remaining time I have left, I want to briefly cover the
8 remaining issues.

9 With respect to claim 4, I want to summarize the evidence. Kim
10 discloses a support pillar. Petition all explains this slideshow. It supports
11 the stack during the replacement gate process. Okay? Tessariol, Exhibit
12 112, cite support structures that support the stack during the gate
13 replacement process. Kim, in fact, says, you could use a different material
14 than the channel structure. So, right there, a POSITA and under the
15 *Intel/Qualcomm* case knows that a pillar, such as Tessariol, or Exhibit 112,
16 is a suitable option. Why? Because it supports the stack during the gate
17 replacement process. I would submit, under *Intel/Qualcomm*, that's enough
18 there. What's more, they've argued -- just to back up, that it wouldn't be
19 obvious to use a metal pillar in Kim. But again, the metal pillar provides the
20 exact same support function.

21 JUDGE CYGAN: Counselor, in Ground 1, are you arguing that
22 Tessariol provides evidence that those two are equivalents in the art, for the
23 same purpose?

24 MR. LANG: Yeah, they both say they support the stack during the
25 gate replacement process.

1 JUDGE CYGAN: Doesn't Tessariol just teach those as two different
2 options for its device, or does it teach that, in general, a person of ordinary
3 skill in the art would recognize that they're equivalent to that purpose?

4 MR. LANG: Well, we've combined it expressly with Tessariol, but
5 we've also cited Exhibit 112. That, too, is a support pillar that says it
6 supports the stack, and what the *Uber* case we cited tells you, if you look at
7 the '031 description, the Tessariol description, these dearth descriptions,
8 then that means that the POSITA certainly understood that these were
9 predictable prior art elements that have established functions. And
10 absolutely, Tessariol, even the '031 patent and Dr. Kuhn admitted, said it
11 didn't give any type of guidance on how to determine the sufficient stiffness
12 or, you know, support. The patent just says sufficient support and gives a
13 couple examples of that. Okay? Tessariol discloses the same thing, Exhibit
14 112 disclosed the same thing.

15 JUDGE CYGAN: But in Tessariol, does it teach that a person of
16 ordinary skill in the art would recognize these to have the same properties,
17 or does it just teach that, in Tessariol, there's two different alternatives?
18 Does it teach them as being equivalent alternatives, is what I'm getting at?

19 MR. LANG: Yes, because -- well, Tessariol has an added advantage,
20 because you can make the same one, it can be a support or it can be a via and
21 support. So you get this via potential. Okay? But, the support function is
22 equivalent, because it supports the stack during the gate replacement
23 process. So, yes. And Exhibit 112 says the same thing.

24 JUDGE CYGAN: So, because Tessariol describes using both of
25 them, essentially for the same purpose, that's teaching that generally one of

1 ordinary skill in the art would recognize these can always be used as
2 equivalents?

3 MR. LANG: They would recognize, certainly, that a metal support
4 can be used to support the stack during gate replacements process. Tessariol
5 expressly says that. Exhibit 1012 does too. You know, equivalent, I mean,
6 one's made out of dielectric, one's made out of metal. The Tessariol one has
7 the advantage, in that respect. That's one thing we pointed to.

8 And I just want to briefly touch on their argument, you know, well,
9 there could be thermal expansion issues. The '031 patent says nothing about
10 that. Dr. Kuhn said it's known in the art. Thermal expansion, we've cited,
11 many references, a copper interconnect. If there's a thermal expansion issue,
12 they've been used for decades. A POSITA -- you know, you look at the
13 *Uber* case again, these details are within the knowledge of a POSITA,
14 because the '031 patent doesn't describe them. Does the '031 patent, to get
15 into your question, Your Honor, describe, like, what's this required stiffness
16 or support function? No, it doesn't provide any detail on that. These are --
17 again, the supporting pillar was in the background of the '031 patent.

18 I did point out an added function. In the point here, we talked about
19 Tessariol a couple days ago, but the point here is Tessariol is saying not only
20 can you use this to support the stack during a gate replacement process, but
21 you could actually use it as a via as well. And Kim discloses peripheral
22 circuitry. Patent Owner says, well, it's not under the array. Well, where is it
23 then? It's either going to be under the array or on the main substrate. In
24 either case, like Tessariol discloses, you need a via for it.

1 I want to just, with the two or three minutes, bring up one point about
2 Tessariol, that really all the arguments that they've made, it just comes down
3 to the same analysis that I gave you. From the very beginning -- and I will
4 say, let me find the slide, slide 61. From the very beginning, Dr. Banerjee
5 explained that Tessariol would be understood just as Kim's language
6 covering the substrate. And so, when you're laying down these various --
7 going back to slide 54, when you're laying down all these dielectric
8 materials, they're being formed all over the substrate. This is on a wafer,
9 they're being formed all over the wafer slash substrate and it's building up
10 all around. And so just the natural, conventional CVD, as Dr. Banerjee
11 explained, what we're looking at is a stack of word lines and dielectric
12 layers. You have to electrically isolate that, encase that, and these are the
13 same techniques a POSITA would recognize that Kim is applying, and they
14 fully surround on all sides. So, with that, I'll -- if there's no more questions,
15 I'll save my remaining time.

16 JUDGE MCGRAW: Actually, I did have some questions, and I think
17 we can extend your rebuttal, perhaps, because of all the questions. I think,
18 first, I'd like to address the -- what I think we're calling the left side of the
19 stack structure. In order for a filling structure to surround the multi-stack
20 staircase structure, does the filling structure have to physically touch the
21 staircase structure?

22 MR. LANG: I would say no. I mean, going back to Dr. Kuhn, the
23 Patent Owner's expert, she gave the example of encircling as police around
24 your house. They may not be touching your house, but I think it doesn't
25 matter, because in Kim, and as Tessariol understood, that this deposition

1 layer -- both Dr. Banerjee and Dr. Kuhn explained this the same way. When
2 you put down a dielectric layer like that, it conforms to the topology of the
3 structures on the wafer. So, if I have anything on the left-hand side, that
4 dielectric is going to go over it just like that and cover it, and it is absolutely
5 going to touch it, and that's what electrically isolates the structure, Your
6 Honor.

7 JUDGE McGRAW: Okay. I think the issue that I was having with
8 that argument is, we cannot see, or we haven't seen what is actually on the
9 left side of the stack structure. So, if there was something in between the
10 stack structure and the filling structure, whatever that may be, and you
11 require the filling structure to touch the stack structure, then it would be
12 possible that claim limitation was not met.

13 MR. LANG: I would say, number one, Kim doesn't describe
14 anything there. He describes the stack structure and then putting the
15 dielectric to cover that and cover the substrate. So, there's not anything
16 between them, he doesn't describe that.

17 JUDGE McGRAW: Okay. And then the second issue was just --
18 maybe you could do this when you come back, on your rebuttal, is just to
19 point out where in the record there is support for Kim wanting to use a via
20 that is able to be conductive. I know you had a slide up, but you didn't point
21 out the slide number, and I want to make sure I can find all of that evidence
22 in the record.

23 MR. LANG: Oh, yeah.

24 JUDGE McGRAW: I believe it was slide 50.

1 MR. LANG: Yeah, so Kim -- on slide 50, Your Honor, and I
2 apologize for not saying the slide number. On slide 50, what we see on the
3 left is a quote from Kim. And Kim says -- he refers to this peripheral circuit
4 region may include row decoder regions, DCR, a page buffer, column
5 decoder, COL. So that is kind of your peripheral circuitry. And Dr.
6 Banerjee explained, with citations to references, you know, where is that
7 found? You build those transistors -- you really have two options. One, in
8 the base substrate there, Patent Owner says that Kim doesn't disclose the
9 substrate underneath, so you would just build them -- that's the transistor
10 right there, on the left of the figure that Dr. Banerjee's illustrating, and you
11 would put that right there. And then you would need to draw conductive
12 vias down to it. That's certainly a suitable option to implement that
13 peripheral circuitry.

14 Kim also, in the schematic of Figure 1, shows that region. In Figure 1
15 of Kim, Kim simply does not show it in the figures, because he's focused on
16 the, you know, staircase and stack structure itself.

17 JUDGE McGRAW: And that was cited in the reply, not the petition,
18 correct?

19 MR. LANG: Yes, and that was responsive to the idea that we always
20 said that a benefit of Tessariol in a petition with this dual role, and they said
21 there was no need for it, and we rebutted that.

22 JUDGE McGRAW: Thank you.

23 MR. LANG: Thank you, Your Honors.

24 JUDGE KOKOSKI: Thank you. Patent Owner, you can begin when
25 you're ready.

1 MR. DAVIS: Yes, Your Honor. Just one moment while I set up my
2 laptop, thank you. May it please the Board. I'd like to begin by addressing
3 a few of the Board's questions that were asked. The issue of claim
4 construction came up a couple times. It seems like the parties are somewhat
5 reaching an agreement on that. It seems like both parties agree that surround
6 means encircle, or all the way around, as the Board had construed it, that it
7 does not require being on the top, and that the Board doesn't need -- reach
8 the issue of whether it has to be continuous. The question also was just
9 asked by Judge McGraw, as well, as to whether it has to touch all the way
10 around, and our position is no, it does not need to touch all the way around.
11 And I apologize, I should have introduced what each person will be
12 handling. I'll be handling, as I've been indicating, the surround issues. Mr.
13 Bonny will handle the pillar support issues.

14 The next set of issues that the panel's questions raised were really
15 what Patent Owner has been focusing on with respect to Kim. The Patent
16 Owner really has failed to -- excuse me, the Petitioner has failed to show or
17 even demonstrate that it would have been obvious as to what's happening on
18 the other side, as we've been referring to, on the left side, or frankly, even on
19 the other three sides of what's shown in Kim. For example, in Kim Figure
20 4B, which I have up here on the screen. This is page 32 of the petition. But,
21 in addition to that lack of disclosure in the Kim reference, Petitioner's
22 arguments, really importantly -- Your Honor, if you want to start the timer?
23 Yep. Alright, thanks.

24 JUDGE KOKOSKI: Thank you for pointing that out.

1 MR. DAVIS: Thank you. Importantly, Petitioner's arguments simply
2 ignore all of the subsequent processing steps that would need to take place
3 and do take place, even assuming that CVD blanketed everything as
4 Petitioner is now arguing. And a lot of the flaws in Petitioner's arguments
5 that they're making now are actually illustrated by the petition and the trial
6 grounds that they've put forward. And so, I do want to walk through their
7 arguments there and explain how they're undercutting the arguments that
8 Petitioner now is trying to ride through to final written decision, having
9 changed them in its reply.

10 The petition starts out -- and this is on page 32 of the petition, with an
11 argument under its original construction or interpretation of what surround
12 was, which meant just something covering, something on top. And so they
13 rely on Figure 4B, to start off with, pointing to Element 110, which is on the
14 right-hand side of Figure 4B, and explaining, look, that's covering at least a
15 part of the staircase structure. They then go on to argue that the -- and
16 actually, let me hit pause there on a second, they don't try to address what's
17 happening, as we've been referring to on the left side, or into the page, or
18 out of the page, they're just referring to what's being covered, what's shown
19 there as Element 110. And we agree that Element 110 does extend to cover
20 part of the substrate as shown in Figure 4B there to the right, not the left, of
21 that figure. Petitioner goes on and --

22 JUDGE CYGAN: Counselor?

23 MR. DAVIS: Excuse me. Oh, please.

24 JUDGE CYGAN: Question for you. They're not just relying on
25 Figure 4, correct? They're relying on a much broader description in Kim.

1 MR. DAVIS: Completely agree, Your Honor, and I think they pivot
2 to that in just a moment. So if they start off with just this narrow argument
3 about Figure 4B, and they then -- and this is just what I was getting to, Your
4 Honor, on page 34, they recognize to the extent that PO, Patent Owner,
5 argues that surrounding requires the dielectric filling structure to be on all
6 sides. They knew this was an issue, they knew they weren't satisfying it
7 when they started out with Kim, and they say they raise three arguments for
8 why Kim discloses it, or at least renders it obvious. And I want to step
9 through each of those three arguments, and Your Honor, I think that might
10 be what you're referring to, is how they're trying to refer to a broader
11 disclosure in the Kim reference.

12 JUDGE CYGAN: Actually, what I was looking at was the description
13 right above Figure 4B.

14 MR. DAVIS: On page 32, Your Honor?

15 JUDGE CYGAN: Yes, on page 32. So Petitioner quotes Kim,
16 disclosure of the filling insulating layer may be exposed on the substrate,
17 and they cover the stack structures ST. Why isn't that sufficiently meeting
18 the claim limitation?

19 MR. DAVIS: Your Honor, simply because that language itself just
20 says it's covering it. It's on top, and as we just talked about for purposes of
21 claim construction, I think the parties are in agreement, when we're talking
22 about surrounding, we're looking at what's on the sides, and that's what this
23 figure and that argument doesn't satisfy. And the Petitioner recognizes that,
24 because they then go on to make obviousness arguments to the extent that it
25 needs to be on all sides.

1 JUDGE CYGAN: But certainly, at least, it's covering the substrate.
2 So, if it's covering the stack structures, isn't it a reasonable interpretation of
3 Kim to say that wherever there's a stack structure, it's being covered by the
4 filling insulating layer, which is also disposed on the substrate? So it would
5 extend everywhere you have a stack structure to cover it and extend all the
6 way down the substrate so it would cover it completely?

7 MR. DAVIS: I think there's at least two problems with that, Your
8 Honor. The first is, we're focused on the sides of the devices, not the
9 surface of the substrate or the surface of the stack structure. The second
10 problem with that argument --

11 JUDGE CYGAN: Well, before we move to the second problem, if
12 you're covering the stack structures and you're covering the substrate, and
13 the stack structures are extending in the steps down to the substrate, and if
14 it's illustrated on 4B that that insulating layer is a mask that's covering the
15 entirety of it, so it's not some sort of special insulating layer that is sort of
16 hitting, I guess, the stripes of it, but it's just this mass that goes all the way
17 down, then you're covering all of the stack structures. At what point are you
18 not surrounding it? With that broader description, and not going to left,
19 right, forward, backwards.

20 MR. DAVIS: Your Honor, because, as Your Honor pointed out in
21 your questions before, while there is a staircase structure on the right side,
22 there isn't disclosure of what is actually happening on the other three sides.
23 And so, it's not clear if that's the end of the substrate, if that goes into other
24 circuitry, or anything else. So, it's never disclosed that you're going to have

1 an edge that will then allow for CVD to fill that other area in, and thus
2 completely encircle that stack structure as is required. I --

3 JUDGE CYGAN: And this was the question I asked your
4 counterpart, and his response to it was, the experts agree it's a single
5 substrate wafer. In Figure 1, if you look at Figure 1, there's other
6 components around it, if you look at the extra exhibits, it shows that those
7 components are sort of the wiring breakouts, those wiring breakouts would
8 be understood to be on the same substrate. So, if you have a single wafer,
9 and the single wafer is also being covered by the filling insulating layer
10 because it's disposed on the substrate and that substrate is the whole
11 underlying portion, at what part are you missing a side?

12 MR. DAVIS: And this is the -- I mentioned before, Your Honor,
13 there's two responses. Can I -- I think if I get to the second, I might answer
14 your question on it. It's the subsequent processing steps. So, if you look
15 here, even -- and I'll zoom in on Figure 4B. So, Element 110, you see how
16 it's buried among several other pieces that are then layered on top of that,
17 there's Element 120, 130, there's trenches that are subsequently dug.
18 There's a lot of additional processing steps that are performed. So, what
19 Petitioner is arguing is that maybe at one point, CVD is applied such that
20 you would deposit Element 110. And what Petitioner would have this Board
21 then say is, everything freezes, it stops, no additional processing is
22 performed, no additional etching is performed, no additional cutting away of
23 that Element 110. What they need to show is that at the end of the day,
24 when you have a fully created memory device, that Element 110 continues
25 to, even if it did at one point, continues to encircle the entire stack structure.

1 And this is actually illustrated if we turn to their slide 30. They
2 reference the CVD process, and we don't disagree that this is the basic CVD
3 process that takes place, but they ignore what's depicted on the right side of
4 their own slide. You see the oxidize, diffuse, implant evaporate, deposit
5 step, that's where it -- whatever is being deposited gets deposited, and
6 they're saying it's deposited everywhere. But what happens after that? The
7 very next step, a mask is applied to create a pattern. What happens after
8 that? Etching is applied. Etching is removing pieces of what you just
9 deposited. So even if, at one point, Element 110 was deposited everywhere
10 and encircled, they need to show that it wasn't then subsequently etched
11 away and removed.

12 And we actually know from their subsequent arguments in the petition
13 that it is removed, that there's a lot of additional processing that takes place
14 exposing the sides of this, and we see an illustration of that -- this is in the
15 petition at pages 36 to 37. Their argument is these are all memory blocks.
16 And you can actually see the labeling of block on Figure 3, there in the
17 middle of page 36 of their petition. And what they're saying is, there are
18 trenches that are cut, top to bottom, left to right, as is depicted from the top-
19 down view, that expose sides of the stack. That additional processing takes
20 place all over the entire structure of whatever the wafer is. For example,
21 Your Honor was referred to -- excuse me, Figure 1 of Kim, which is just one
22 slide prior to where I was, slide 29.

23 So, just to zoom in on that figure, there's additional processing to
24 create the row decoders on the left and the right, or the PBR on the bottom,
25 or the column decoders. All that additional processing would be removing

1 Element 110 if it was even deposited there, such that even if it was at one
2 point encircling the stack structure, they need to show that it was there and
3 stayed there the entire time. They haven't done that.

4 JUDGE CYGAN: So, the issue is really revolving around whether or
5 not the additional processing has removed this sort of encapsulation, this
6 surrounding material. And your point is that Petitioner has not shown
7 whether or not Figure 1 is a finished device in which there has been some
8 processing which has removed it. For example, because there's nothing in
9 Kim which really says anything about the processing of the other features.

10 MR. DAVIS: It does not, Your Honor.

11 JUDGE CYGAN: So your contention is that the existence of those
12 other features makes it unclear whether or not the surrounding material has
13 been removed from the substrate?

14 MR. DAVIS: Just simple failure of proof, Your Honor. They don't
15 even attempt to address it. Their whole argument is, look, CVD was
16 performed at one point, and that's it. We can sit down, we're done. They
17 don't even attempt to address any of the subsequent processing that would
18 have to take place. And you can even look just at Figure 4B, which we've
19 been looking at, right? You see a bunch of different processes that then take
20 place on top of 110. We see the additional trenches, and you can see kind of
21 from a cross sectional standpoint in Figure 4B, you see them in Figure 3,
22 which is on page 36 of the petition, these trenches cutting all the way
23 through.

24 Petitioner even points to the Park reference, which is separate from
25 Kim, and says all right, well, these common source lines, these are all cut all

1 the way through, this is what would exist in the Kim reference as well. You
2 saw Petitioner making arguments that, well, Element 110 might still be out
3 there somewhere, we even see these common source signs extending
4 beyond, as you can see in the upper right hand corner, for example, of Figure
5 3 from Park, extending beyond where that staircase structure would be.
6 These are just one failure of proof after another. They're just waving their
7 hands and saying well, CVD's applied, and we're done. And it just simply
8 doesn't meet their burden here. Your Honor, unless there's any further
9 questions on that, I will pass the podium to -- Your Honors, any further
10 questions, otherwise I'll pass the podium to Mr. Bonny. Thank you.

11 MR. BONNY: Your Honors, I will address the second set of issues
12 which is the pillar support material surrounded by the insulating material
13 limitation. As you know, claim 4 requires that the supporting pillar is filled
14 with at least one layer of an insulating material and a pillar support material
15 surrounded by the insulating material. The relevant portion here for the
16 proceeding, however, is just the portion that recites a pillar of support
17 material surrounded by the insulating material, and that's because that's the
18 portion of the claim that Petitioner mapped the art to in its petition. And so,
19 I'll address Grounds 1 through 4, primarily focusing on Grounds 1 and 2
20 because even though there are four grounds, there are really two references
21 here, Kim and Tessariol.

22 At a high level, just to preview what I'll be arguing, all of the
23 references use, or all of the arguments, rather, use Tessariol's conductive
24 core. Kim, even for Ground 1, they cite Tessariol for that ground. At a high
25 level, what Petitioner has failed to show is multiple steps that are required in

1 the obviousness analysis. First, Petitioner has failed to show that a person of
2 skill would have been motivated to use a particular material of the
3 conductive core, and furthermore, for Kim, that a person of skill would have
4 added a conductive core, and the second, they failed to show that any of
5 those such materials is a pillar of support material.

6 So turning to slide 39, jumping ahead actually a few slides to slide 39,
7 starting with Kim. Petitioner's argument for Kim involves modifying Kim's
8 dummy structures to include a conductive core. The first problem is that
9 Kim never actually discloses using a conductive core, and as I'll explain,
10 they haven't shown that it would have been obvious to modify Kim to
11 include a conductive core. And that's really where the issues lie here, is in
12 that explanation as to why a person of skill would have added that core to
13 Kim's device.

14 They've made a couple of arguments, and they cite Tessariol and one
15 other reference to show a conductive core, but what Petitioner has failed to
16 do here is showing that a person of skill would have actually added that
17 conductive core to Kim's device. I'll touch on the arguments that Petitioner
18 raised in his presentation as well as a couple issues that he either chose not
19 to or didn't have time to get to. First, there's the argument that there's a
20 beneficial support function, and that's something that counsel touched on in
21 his presentation, but the issue here is that Kim already has support structures
22 that already provide support without a conductive core. And in fact, you
23 heard counsel for Petitioner say that they're equivalent. But if that's the
24 case, if they're providing an equivalent support function, then what's the

1 motivation for adding that conductive core to Kim's device? Kim already,
2 by his own admission, already provides that same support function.

3 He then also said that there's an additional benefit, and this is jumping
4 ahead now to slide 44. There's an additional benefit of an interconnect
5 function, but Kim also has no need for an interconnect function in the
6 relevant location, and that location piece of it is the key part that Petitioner
7 does not address. As Dr. Kuhn explained, and this is here on slide 44, Kim
8 doesn't disclose any circuitry, either transistors or interconnects under the
9 memory array in the staircase region where these dummy structures in Kim
10 are located. And because of that, if there's no circuitry under the dummy
11 structures, there's simply no reason to use those dummy structures as an
12 interconnect, because there's nothing for them to connect to.

13 And in Petitioner's presentation, he brought up this figure, so
14 switching over to Patent Owner's demonstratives, I believe it's slide 50. I'm
15 sorry, Petitioner's demonstratives, slide 50. He pointed to the left side of
16 Figure 1, but that's not the right part of the device. Those peripheral circuit,
17 that's the peripheral circuit region, it's not in the staircase region. It's not
18 where these dummy structures are located, and so this doesn't show that
19 there would be any need or benefit from adding those interconnects in the
20 actually relevant location, which is the location of Kim's dummy structures.

21 There was a third argument, in the papers at least, that a conductive
22 core would use the same process as the conductive vias. This is also
23 switching back to Patent Owner's slide 44, you can see this on the top here,
24 past the part that's -- in red, they say that this would have been beneficial
25 because the process to form them would use the same process steps as the

1 conductive vias. It's not clear, to us at least, what they're referring to when
2 they say 'the' conductive vias. If they're talking about Kim, Kim doesn't
3 explain a process for forming the conductive vias, so there's no same
4 process steps, and therefore no benefit in that scenario. If they're talking
5 about Tessariol structures, that doesn't show a reason to modify Kim.
6 There's no benefit to using Tessariol's process, if anything, that further
7 complicates the manufacturing process, because you're adding a process
8 that's in Tessariol and not in Kim. So that doesn't show a benefit for
9 modifying the Kim reference.

10 The other issue -- turning back to slide 41, that I want to -- sorry,
11 actually before that, sticking with slide 45. There's also an issue that Dr.
12 Kuhn discussed about thermal expansion mismatch that was not addressed
13 by Petitioner in the petition analysis. And that issue specifically is, when
14 you have different materials next to each other, and in particular when
15 you're extending through the full height of the stack like you are with these
16 dummy structures, you need to be thinking about this thermal expansion
17 coefficient issue, because for example during the gate replacement process,
18 you have a high-heat process that results in thermal expansion, and if there's
19 a mismatch between those coefficients, that leads to cracking and can
20 damage the device.

21 And this wasn't addressed in part because for the longest time in the
22 petition, they don't even address or mention a specific material, but then
23 when they finally in Ground 2 come around to discussing copper, that
24 material actually has significant thermal expansion potential issues, because
25 it's thermal expansion coefficient is different from Kim's insulating

1 materials. And as Dr. Kuhn explained, you have a coefficient of 16.6 for
2 copper versus .64 for silicon oxide. So it's a huge difference, and something
3 that Dr. Banerjee did not address in his analysis.

4 Briefly turning back to slide 41, the Board doesn't even need to reach
5 this issue because they haven't shown that there would be a motivation to
6 add a support structure, an additional support structure, rather, in Kim's
7 device. But even apart from that, there's also this issue of the material
8 properties of the metals, which Dr. Banerjee discusses in his declaration as
9 being something that determines the suitability of the material as a pillar.
10 But then, for most of their petition and most of his declaration, they're just
11 analyzing metals generally rather than specific materials. And specifically,
12 they address metal cores as a group, and the problem with that analysis is
13 that metals as a group do not have a specific or even a trend regarding their
14 material properties. It's all over the place. And there are non-metals that
15 have better and worse -- Young's modulus, for example, then metals. And
16 so simply saying that you would use a metal, a metal core as Petitioner
17 argues, doesn't necessarily show that it would be a so-called pillar support
18 material.

19 JUDGE CYGAN: Counselor, all of the materials that are mentioned
20 in the '031 Patent are suitable materials, correct?

21 MR. BONNY: That's correct, yes. We're not disputing whether
22 those materials are pillar support materials, that makes it clear that they are.
23 And the issue with, for example, Petitioner's reliance on copper, is that they
24 haven't shown a person of skill would have been motivated to use that
25 material in Kim's device, or when I will get to it, in Tessariol's device.

1 So I'll turn to Ground 2 now, and there's a lot of overlap with the
2 issues here because, as I mentioned before, Petitioner cited Tessariol for
3 Ground 1 as well, even though it's ultimately a Kim ground. But in Ground
4 2, there's a lot of those same issues. As a background for this, Tessariol
5 doesn't say what kind of metal is in the device. It has a conductive core, but
6 it doesn't say what kind of metal is in the device. And I don't believe he got
7 to it in his presentation, but if you look at their demonstratives, one of the
8 main pieces of information they're relying on in Tessariol is paragraph 41, I
9 think it is, and that's the paragraph that talks about the dummy structures
10 performing a support function.

11 And I just wanted to address that before moving on, and the issue
12 there is that Tessariol doesn't say that the core is a support material. It's
13 talking about the dummy structure, and at most it's saying that the dummy
14 structure provides support. The dummy structures have an insulated
15 periphery, as they refer to it, even in the situation where it has a conductive
16 core. And as Dr. Kuhn explained, those materials, insulating materials,
17 often have better support materials than many metals. And so, even if the
18 Board were to conclude that Tessariol's dummy structures are support
19 structures, that doesn't necessarily mean that the core material is a pillar
20 support material, and Petitioner hasn't done the analysis to show that the
21 core would be a pillar support material.

22 JUDGE KOKOSKI: Counsel, do we need to construe what pillar
23 support material is?

24 MR. BONNY: The Board doesn't have to reach that issue, and
25 there's been a bit of briefing on that but it's not something that has been

1 addressed in detail. And the reason why the Board doesn't need to reach
2 that is because the main dispute is not over whether certain materials are
3 support materials. The main dispute is that Petitioner hasn't shown that it
4 would have been obvious to use any particular material, its analysis is based
5 on general categories of conductive cores, or elemental metals I think is how
6 they refer to it at one point, which isn't sufficient, because again, those can
7 just span a huge spectrum and they haven't shown that any particular metal
8 will be used.

9 They do eventually discuss copper by citing to other references, but
10 when they finally do address, when Petitioner finally starts discussing other
11 metals, it doesn't show that a person of skill would have been motivated to
12 modify the reference to use that particular metal. And in fact, as I will get
13 into in more detail, at one point they actually quote the claim language for
14 the metals they would use, which is textbook hindsight. And it's word for
15 word quoting the language of claim, I believe it's 5, where it's listing the
16 metals that the '031 Patent discloses.

17 I'll actually address that a bit more now in the context of slide 47.
18 And so, Petitioner, you can see here, at the top, they argue that Tessariol
19 discloses that the pillar support material may be one of copper, cobalt,
20 nickel, and aluminum. That's the claim language. It's textbook hindsight,
21 they're not citing Tessariol or even another reference for that. They're using
22 the claims as a roadmap, and as the Federal Circuit has held, that's
23 inappropriate. And of course, you know, the way to guard against this is to
24 require a motivation to make the combination, but for the reasons I've
25 explained, Petitioner hasn't provided that motivation.

1 One last point I want to address for Ground 2, they argue that copper
2 was a well-known interconnect material, and Petitioner cites a couple
3 references for that. Two points here. One, that's not the test for
4 obviousness. They needed to show motivation to use copper specifically in
5 Tessariol's conductive core, which they haven't done. And even if they had
6 shown -- I'm sorry, what I meant to say is, the references that they cite
7 relating to teaching copper for interconnects doesn't necessarily show even
8 that it was well known or obvious to use copper for support structures,
9 which has been a key difference, because Tessariol's conductive core
10 extends the full height of the device and through all the way through the
11 stack after the device layer. When you get to the device layer at the bottom,
12 that's where you have to start worrying about things like diffusion and
13 contamination from copper, because that's where the device structures are.

14 You also have to start worrying about thermal expansion mismatch
15 during the gate replacement process, as I talked about before. And so, a
16 reference that simply talks about using copper for interconnects, for
17 example, on a higher layer of the device, doesn't necessarily show that it
18 was even known or desirable to use that material for the pillar support
19 structure that extends the full height of the device. And there's -- I'll skip
20 over Grounds 3 and 4 unless there are questions on those, because they
21 essentially rely on -- or are deficient for the same reasons. There's a couple
22 additional motivation issues in our briefing and on the slides related to
23 Ground 3, but unless there are no further questions we'll reserve the
24 remaining time for rebuttal.

1 JUDGE KOKOSKI: Thank you very much. Petitioner, we're going
2 to restore some of your rebuttal time back to you from the questions, we'll
3 then give you 12 minutes for your rebuttal.

4 MR. LANG: Thank you, Your Honor.

5 JUDGE KOKOSKI: And you can start when you're ready.

6 MR. LANG: Having a computer issue here. There we go. Okay,
7 Your Honors, I'm ready. I'm just going to briefly touch on the cover issue.
8 Again, I've been here for three days and they're saying, you know, you can't
9 just rely on figures, and then they're just relying on figures because it's
10 missing, you can't see the other half. What we do know from the figures in
11 the specification is that when it says cover is that it goes -- and it says it goes
12 onto the substrate, it covers the substrate. What we do know is what that
13 right arrow shows us, it shows that it covers the edge, it keeps going onto the
14 substrate. This idea that CVD doesn't cover both sides, that's incorrect. Dr.
15 Kuhn, Dr. Banerjee, the exhibits that Dr. Banerjee showed, it follows the
16 topology, so it follows the edges. And the figures show an example of that.

17 Ironically, they say that there's extra processing done. What extra
18 processing? Look at Figure 4B on the right. Your Honors, I'm on slide 39, I
19 apologize. You put all the channel structures through, you put stuff on top,
20 there's degreed filling structure still there. Kim doesn't say any of it's
21 removed. As we all talked about, things go through the top and the trenches
22 are inside, as I demonstrated earlier.

23 JUDGE CYGAN: Counselor, just to sort of refocus that issue, so are
24 you contending that by the time we see Figure 4B it's a memory device that
25 meets at least the preamble limitation?

1 MR. LANG: I mean, I would say I don't know what would be left to
2 do. There's the deadline on top, and to your question, Figure 1 is a complete
3 memory device. So, I don't know what's exactly remaining to be done, and
4 Figure 1 is a complete device. All right.

5 So, I want to focus on these issues of claim 4 and 5. Claim 4 to start,
6 there's no mention of a metal in here, type of metal. This idea that you
7 know, you've got to disclose a type of metal to disclose claim 4 is false. It
8 doesn't identify a type of metal, okay? That's number one. Number two. I
9 ask the court to look at the *Intel* case number one that says it's not necessary
10 to show the best option, only the suitable option. Predictable use of prior art
11 elements, according to their established function, that is a classic *KSR*.
12 We're not modifying, we're not taking some structure in Kim and modifying
13 it. The supporting pillar was a well-known predictable use of a prior art
14 element according to established function. What is that established function
15 here? Supporting the stack during the gate replacement process. That's what
16 Kim does, that's what Tessariol does, that's what Exhibit 112 does.

17 Does the '031 Patent even describe how stiff it has to be? You asked
18 a question, Your Honor, if we should construe that term. And the answer to
19 that question is no, and the *Uber* case says why. The *Uber* case says, when
20 you have a description like that, which Dr. Kuhn admitted, there's no details
21 on how you determine that in a patent. The *Uber* case tells you that safe to
22 assume a POSITA knows how to implement those details. Indeed, why is
23 that safe to assume? It's in the background section of the '031 Patent.
24 That's how Tessariol treats it. That's how Exhibit 112 treats it, okay?

1 Thermal expansion. They got up and talked about thermal expansion.
2 Let me go to that slide, slide 49, I believe. Dr. Kuhn. So, the '031 Patent
3 also does not explain how a person of ordinary skill in the art would
4 consider a thermal expansion mismatch when choosing what metal to use.
5 The patent does not describe that. Huh, why? I do point out that the
6 information is known in the art. Their own expert, it's not in the '031 Patent,
7 and their expert is saying because it is known how to be dealt with. Indeed,
8 we cite all of these references using copper. The copper issue was dealt with
9 for 20 years. As *Uber* says, safe to assume a POSITA understood this, Dr.
10 Kuhn in fact said it herself. The case that they're citing -- and what they're
11 trying to do is, they said oh, we're converting this pillar and we're changing
12 this pillar in Kim. No, we're talking a known element with a predictable
13 use. And what *Intel/Qualcomm* says is that it is obvious when there's
14 another known element that has that same established function, okay?

15 On top of that, we do provide a motivation and a few points on that.
16 They had said -- and I do want to go to -- and Tessariol is just clear. I'm
17 sorry, I'm at slide 48. Such tiers being elementally supported and
18 preventing from collapsing within the array portion by a transition metal.
19 Okay. By both dummy support structures and operative vias within the
20 staircase structure. No other way to read that. And it's not surprising that
21 both of them support the stack, because they're made at the same time, the
22 exact same way. This notion that the conductive core doesn't do the
23 supporting, well, if you look at claim 4, Your Honor, it says itself -- I'm on
24 slide 45. The supporting pillar is filled with at least one of the insulating
25 liner and a pillar support material. Okay?

1 So, what this claim is getting at is to the examples of its patent, where
2 you'd have an insulating liner and you would have a, they give a couple
3 examples of metal, like copper. And -- well, what's doing the support?
4 Presumably this patent is enabled, and what's doing the support? They say
5 it's just the insulating liner. Well, then I guess copper's not a pillar support
6 material if it's just insulating liner? The argument doesn't make any sense,
7 okay? And Tessariol, at Exhibit 1012, both of them are clear, you have a
8 thick metal core. Dr. Banerjee in fact explained why that's a support
9 material.

10 All of these arguments that they brought up about modulus, the Young
11 modulus, he said that was one factor. You can look at his declaration. He
12 said that was one factor, and they tried to suggest it was the only factor, and
13 then they go off on some tangent about it. This really comes back to this
14 *Uber* case, though. I would urge Your Honors. And the benefits of it, they
15 bring up this notion about, well the peripherals, and the peripheral. I think
16 they back off of yeah, it has peripheral circuitry. It's somewhere. They're
17 saying it's not underneath the array. Well, the picture I showed Your
18 Honors had it on the substrate. Okay, that's where it's going to be.

19 And the point of it is, they're saying that well, so what? You're
20 making vias over there, that's the peripheral. You need them in the staircase
21 as well. My point -- let me go to a figure. I'm on slide 39. The point of it
22 is, as Tessariol teaches, that you've got those dummy channels all in that
23 staircase region, okay? Now the point is, peripheral, Tessariol somewhere
24 has some additional peripheral logic. Figure 1 kind of shows that as well.
25 And you can make all of those dummies and the vias at the same time with

1 the same process. So you get a two for one. Instead of just doing one
2 process to make your dummies and then separately making your vias, now
3 you're doing them all the same time, the same way, in one process step.
4 That's the benefit. The fact that some of them are in the peripheral is of no
5 moment. In fact, that right most dummy that Kim is showing on the Figure
6 4B, that's not even through the staircase contact. That's what they're
7 considering peripheral.

8 JUDGE McGRAW: This is Judge McGraw. Just to clarify, you're
9 saying that it's an advantage to make the dummy structures using the
10 conductive material core, conductive core, because it's more efficient?
11 Because then you would just use the same process?

12 MR. LANG: When you're --

13 JUDGE McGRAW: Go ahead.

14 MR. LANG: Oh, I'm sorry, Your Honor, please finish.

15 JUDGE McGRAW: My question is directed to exactly why is it more
16 efficient to create Kim's dummy structures using the conductive core
17 material? Explain that part to me. I'm not quite sure I believe you. Please
18 convince me why.

19 MR. LANG: So, Tessariol, Your Honor -- I'm looking at slide 50.
20 Tessariol has what is called peripheral circuitry. Those are the basic, you
21 know, transistors, logic, every memory has it. It's called peripheral because
22 usually it's on one side of the stack, as shown here. And in those transistors
23 are going to be either on that substrate or on a substrate below. In either
24 case, as Tessariol shows, you need to make a connection down to that
25 transistor. That is what Exhibit 1029 is showing. That connection cannot be

1 a dielectric core that goes down there. You need an insulating liner and a
2 conductive core. You need that conductive core to make an electrical
3 coupling, electrical connection to that element through the stack. That is
4 precisely why Tessariol has vias and dummy vias.

5 The benefit is, now you're making your dummy support structure.
6 You're making your vias all at the same time. You need those conductive
7 vias in Kim, and voila, here they are. I would also say that at bottom, not
8 only are you getting this benefit, it is a suitable option under
9 *Intel/Qualcomm*. These are well known elements, it's in the background
10 section of the '031 Patent, that are being used for their established functions.
11 Tessariol says, my pillar supports the stack. That is what Kim is using, a
12 support pillar to support the stack during RG, replacement gate process.

13 JUDGE KOKOSKI: Okay. You are out of time, I think. Unless
14 Judge McGraw had any follow up on her question, and I'm thinking she
15 does not?

16 JDUGE McGRAW: No, thank you very much.

17 JUDGE KOKOSKI: Okay. Thank you so much for your argument.

18 MR. LANG: Well, I really thank you for your attention today.

19 JUDGE KOKOSKI: Patent Owner, we think you have 30 minutes
20 left. So of course, after you're done setting up, feel free to begin when
21 you're ready.

22 MR. DAVIS: I hope to use nowhere near that. May it please the
23 Board. I do want to point out just generally, Petitioner has really no
24 response to the failure of proof, the problem they have with respect to the
25 problem that goes across all of their grounds. They're relying on a CVD

1 process that takes place very early on in the formation of this overall
2 memory device, this Element 110 that you have depicted here on their slide
3 28. As you can even see on slide 28, layered on top of that there's Element
4 120, there's Element 130, there's additional lines layered on top of that,
5 even, there's further trenches that are then dug. You heard about their
6 arguments regarding the common source line from Park. All of these
7 removing whatever material was applied before, even if there was CVD.

8 And we see their arguments on Figure 1, it actually further
9 accentuates the problem -- this is on slide 29. Right below that memory
10 region you have the page buffer region, the PBR. Whatever was there, even
11 if there was something that was deposited there, or even if Element 110 was
12 there at one point in time, it was removed with the formation of the PBR.
13 And you have the next problem on slide 29 -- excuse me, slide 30.

14 No response to how the CVD process works. As you can see, in that
15 CVD process, even when you do the process of CVD, you deposit whatever
16 material it is, say it's Element 110, you then mask, you then etch, you
17 remove. And that repeats over and over and over again with each
18 subsequent step. So even if there might have been Element 110 blanketing
19 the surface at one point, there's no even argument or showing, there's no
20 proof of the obviousness or express disclosure that it would remain there and
21 surround the stack structure. Unless there's any further questions, your
22 Honor, I'll pass the podium to Mr. Bonny.

23 JUDGE KOKOSKI: I do have one question. Can you just point out
24 to me, it's probably on a slide, but can you just point out to me where you
25 made the subsequent processing arguments in your briefing?

1 MR. DAVIS: Yes Your Honor, that was really throughout our
2 briefing. So an aspect of that, Your Honor, was the trench piece, right? We
3 were arguing the entire time that these subsequent trenches are formed -- and
4 I could point Your Honors just to those pages, but that really flows
5 throughout our arguments on this.

6 JUDGE KOKOSKI: Okay. I think that does clear it up. I do have
7 one other question then, following up on that. Are these the trenches that
8 Kim says may include trenches, or is this a different trench? And if Kim
9 does say 'may include,' wouldn't that mean that it does not need to include
10 the trenches?

11 MR. DAVIS: Your Honor, I think Petitioner's arguments belie that
12 position as well. If we look at the -- so, these are, to answer your questions
13 directly, these are the trenches, I think, that they describe as may be
14 included, and those are trenches that are inside of the block. You see that
15 here depicted on Figure 3, this is on page 36 of their petition. Those are
16 what are described as may include. But what they then go on to explain, and
17 this is on Figure 2, just above Figure 3, is between each of those blocks you
18 need to have a source line that is able to access them. And they explain this
19 in the context of Park. they explain those source lines are trenches that cut
20 all the way through, stem to stern, the entire memory array, again dividing
21 that -- this is on the top of page 37 of their petition. In addition to that, Your
22 Honor, if we go back to their argument on the Figure 1, this is on slide 29 of
23 Petitioner's exhibits. You have the PBR that's also on one side of this
24 memory array that would have eliminated whatever was deposited there
25 before at some earlier processing step.

1 JUDGE KOKOSKI: Thank you.

2 MR. DAVIS: Thank you.

3 MR. BONNY: Your Honors, on the pillar support material issue I just
4 have three points that I'd like to explain that -- get at points that Petitioner
5 raised in his rebuttal. First, Petitioner asserted that the claims don't identify
6 a type of material, or specifically claim 4, but that's misunderstanding the
7 issue here. The claim does recite a pillar support material. Tessariol, on the
8 other hand, never discloses anywhere that its conductive core is a pillar
9 support material. So that's the disconnect, and that's why Petitioner needed
10 to explain and do the analysis to show that there would be a particular
11 material that a person of skill would have been motivated to use in Tessariol
12 that would have met that requirement.

13 Petitioner also argued again that the use of copper was well known,
14 and that this is just taking something that's known for its known purpose.
15 The problem, however, is that even Petitioner's own references, as I
16 explained before, that discuss copper, which are not Kim or Tessariol, it's
17 other secondary references that aren't part of the ground, that even those
18 references do not address using copper for a pillar support structure. And
19 that's the key issue. That doesn't show that it was well known to use copper
20 for the particular purpose just because it was known to use copper
21 somewhere in the memory device, or in semiconductor devices generally.

22 JUDGE CYGAN: Can I take you back to your first point?

23 MR. BONNY: Yes, Your Honor.

24 JUDGE CYGAN: Tessariol's lack of support for showing that it
25 supports it. You're kind of pointing to language in paragraph 41 of

1 Tessariol, which seems to indicate that during the gate replacement step the
2 tiers are being supported and prevented from collapsing by the demi-support
3 structures and the operative conductive -- so, what is missing in that
4 paragraph?

5 MR. BONNY: Yeah, Your Honor, this actually goes back to the point
6 that I mentioned in the opening, which was that in paragraph 41, there's no
7 disclosure that it's the core that provides that support function. And as I
8 explained, Dr. Kuhn explained that the insulating materials, like the
9 insulating periphery of this demi structure, when it has the conductive core
10 there's still an insulating periphery, those insulating materials often have
11 better support function than many metals. And so, it's not enough -- they
12 basically just assume that the core is what's providing the support function
13 in Tessariol, and Tessariol says nothing of the sort. That's the issue.

14 And the final point that I wanted to raise is just Petitioner's attempt to
15 rehabilitate some of his motivations. First, the need for vias. You can look
16 directly at the figure that Petitioner relied on. Those periphery structures are
17 not under the staircase. It's clear cut. Just because there's periphery circuits
18 elsewhere does not mean that there would be a need to add them or to use
19 them in the staircase region. And with respect to the same process issue,
20 that there would be a benefit for using the same process that's used to form
21 vias, at best that just shows that the modification wouldn't further
22 complicate the process, at best. It doesn't show that there's a benefit.
23 Because if you're already using that process, you're not gaining anything by
24 using that process elsewhere, it just means you're not making it more

1 complicated. So, it doesn't actually motivate the combination or the
2 modification that Petitioner is proposing.

3 JUDGE MCGRAW: What about an argument that it's just another
4 process that's equally suitable?

5 MR. BONNY: Yes Your Honor, even if that was the case, it still
6 doesn't address why a person of skill would have used that process or used
7 that structure for the other device. It's really just going to, at best,
8 reasonable expectation of success or the issue of whether you're
9 complicating the device and the manufacturing process, but it doesn't show
10 that there's any gain, anything that would motivate that modification,
11 because there's no benefit. You've just shown that okay, you can do it for
12 some unknown reason and you aren't complicating the process, but why?
13 Why is a person of skill going to do that? Why isn't it going to add that
14 core? And that's the thing that's missing.

15 JUDGE CYGAN: Does there need to be a benefit if they're known
16 alternatives in the art?

17 MR. BONNY: Well, respectfully Your Honor, as I was discussing
18 earlier, the issue is Petitioner hasn't even shown that it's known. So it hasn't
19 cleared that threshold or hurdle of showing that these materials were known
20 to be used for this specific purpose. If there's no other questions, we'll yield
21 the remaining time back to the Board.

22 JUDGE KOKOSKI: Okay. Thank you very much. I'd just like to
23 thank the parties here today and all week for your preparation in your
24 presentations. It's been very helpful to us for all of the cases. We appreciate
25 your attendance and all the work that everyone on your teams have done.

1 With that, this case is now submitted to the panel for determination and
2 preparation of the final written decision, and we are adjourned.

3 (Whereupon, the above-entitled matter went off the record at
4 2:59 p.m.)

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