

UNITED STATES PATENT AND TRADEMARK OFFICE

---

BEFORE THE PATENT TRIAL AND APPEAL BOARD

---

MICRON TECHNOLOGY, INC.,

Petitioner,

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,

Patent Owner.

---

Case No. IPR2024-00790

U.S. Patent No. 10,868,031

---

**PATENT OWNER'S NOTICE OF APPEAL**

Director of the United States Patent and Trademark Office  
c/o Office of the General Counsel  
United States Patent and Trademark Office  
P.O. Box 1450  
Alexandria, VA 22313-1450

Pursuant to 35 U.S.C. §§ 141, 142, and 319, and 37 C.F.R. §§ 90.2-90.3, notice is hereby given that Patent Owner Yangtze Memory Technologies Company, Ltd. (“Patent Owner”) appeals to the United States Court of Appeals for the Federal Circuit from the Final Written Decision of the Patent Trial and Appeal Board (“Board”) entered October 23, 2025 (Paper 29) in IPR2024-00790, and from all underlying orders, decisions, rulings, and opinions decided adversely to Patent Owner regarding this *inter partes* review of U.S. Patent No. 10,868,031 (“the ‘031 patent”). A copy of the Final Written Decision is attached.

In accordance with 37 C.F.R. § 90.2(a)(3)(ii), Patent Owner further indicates that the issues on appeal include, but are not limited to, the following: (1) the Board’s determination that claims 1-3 of the ‘031 patent have been shown to be unpatentable; (2) the Board’s determination that Petitioner has demonstrated by a preponderance of the evidence that claims 1-3 of the ‘031 patent are unpatentable under 5 U.S.C. § 103; (3) the Board’s consideration of the expert testimony, prior art, and other evidence in the record; (4) the Board’s factual findings, conclusions of law or other determinations supporting or related to those issues; as well as (5)

all other issues decided adversely to Patent Owner in any orders, decisions, rulings, and opinions.

Pursuant to 35 U.S.C. § 142 and 37 C.F.R. § 90.2(a), this Notice is being filed with the Director of the United States Patent and Trademark Office, and a copy of this Notice is being concurrently filed with the Patent Trial and Appeal Board. In addition, a copy of this Notice and the required docketing fees are being filed with the Clerk's Office for the United States Court of Appeals for the Federal Circuit via CM/ECF.

Dated: November 5, 2025

By: /Andrew Radsch/  
Andrew Radsch  
Admitted *Pro Hac Vice*  
Counsel for Patent Owner

**CERTIFICATE OF SERVICE**

The undersigned hereby certifies that, on November 5, 2025, the foregoing PATENT OWNER'S NOTICE OF APPEAL was:

- (1) electronically filed through PTACTS
- (2) filed by Express Mail to The Director of the United States Patent and

Trademark Office at the following address:

Director of the United States Patent and Trademark Office  
c/o Office of the General Counsel  
United States Patent and Trademark Office  
P.O. Box 1450  
Alexandria, VA 22313-1450

- (3) filed in the U.S. Court of Appeals for the Federal Circuit using the Court's CM/ECF filing system and pay.gov to pay the filing fee electronically

- (4) provided a courtesy copy via electronic mail to the following attorneys of record for the Petitioner listed below:

| <b>Lead Counsel</b>                                                                                                                                                                                                                                                         | <b>Back-Up Counsel</b>                                                                                                                                                                                                               |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Jeremy Jason Lang<br>Registration No. 73,604<br>( <a href="mailto:jlang@orrick.com">jlang@orrick.com</a> )<br><br>Postal & Hand-Delivery Address:<br>Orrick, Herrington & Sutcliffe LLP<br>1000 Marsh Road<br>Menlo Park, CA 94025-1015<br>T: 650-614-7400; F: 650-614-7401 | Jared Bobrow<br>Admitted <i>Pro Hac Vice</i><br>( <a href="mailto:jbobrow@orrick.com">jbobrow@orrick.com</a> )<br><br>K. Patrick Herman<br>Registration No. 75,018<br>( <a href="mailto:pherman@orrick.com">pherman@orrick.com</a> ) |

|                                                                                                                                                                                                                                                                                                              |  |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--|
| <a href="mailto:PTABDocketJJL2@orrick.com">PTABDocketJJL2@orrick.com</a><br><a href="mailto:P52PTABDocket@orrick.com">P52PTABDocket@orrick.com</a><br><a href="mailto:PTABDocketJ3B3@orrick.com">PTABDocketJ3B3@orrick.com</a><br><a href="mailto:micron-ymtc_ohs@orrick.com">micron-ymtc_ohs@orrick.com</a> |  |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--|

Dated: November 5, 2025

By: /Jonathan Bradford/  
Name: Jonathan Bradford  
**ROPES & GRAY LLP**

UNITED STATES PATENT AND TRADEMARK OFFICE

---

BEFORE THE PATENT TRIAL AND APPEAL BOARD

---

MICRON TECHNOLOGY, INC.,  
Petitioner,

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,  
Patent Owner.

---

IPR2024-00790  
Patent 10,868,031 B2

---

Before JO-ANNE M. KOKOSKI, KIMBERLY McGRAW, and  
MICHAEL T. CYGAN, *Administrative Patent Judges*.

KOKOSKI, *Administrative Patent Judge*.

JUDGMENT  
Final Written Decision  
Determining Some Challenged Claims Unpatentable  
35 U.S.C. § 318(a)

## I. INTRODUCTION

We have jurisdiction to conduct this *inter partes* review under 35 U.S.C. § 6 and issue this Final Written Decision pursuant to 35 U.S.C. § 318(a). For the reasons that follow, we determine that Micron Technology, Inc. (“Petitioner”) shows by a preponderance of the evidence that claims 1–3 of U.S. Patent No. 10,868,031 B2 (“the ’031 patent,” Ex. 1001) are unpatentable and does not show by a preponderance of the evidence that claims 4 and 5 of the ’031 patent are unpatentable.

### A. *Procedural Background*

Petitioner filed a Petition to institute an *inter partes* review of claims 1–5 (the “challenged claims”) of the ’031 patent. Paper 1 (“Pet.”). Yangtze Memory Technologies Company, Ltd. (“Patent Owner”) filed a Preliminary Response. Paper 8. Pursuant to 35 U.S.C. § 314(a), we instituted an *inter partes* review of claims 1–5 on the grounds advanced in the Petition. Paper 9 (“Institution Decision” or “Dec.”), 6, 26–27. After institution of trial, Patent Owner filed a Patent Owner Response (“PO Resp.,” Paper 12), Petitioner filed a Reply (“Pet. Reply,” Paper 14), and Patent Owner filed a Sur-reply (“PO Sur-reply,” Paper 17).

We held an oral hearing on July 31, 2025, and a transcript is included in the record. Paper 25.

### B. *Real Parties in Interest*

Petitioner identifies “Micron Technology Inc. and its subsidiaries, including Micron Consumer Products Group LLC” as the real parties in interest. Pet. 6. Patent Owner identifies itself as the real party in interest. Paper 4 (Mandatory Notice), 2.

*C. Related Matters*

The parties indicate that the '031 patent is asserted in *Yangtze Memory Techs. Co., Ltd. v. Micron Tech. Inc.*, Case No. 3:23-cv-05792-RFL (N.D. Cal.). Pet. 6–7; Paper 4, 2.

*D. The '031 Patent*

The '031 patent, titled “Multiple-Stack Three-Dimensional Memory Device and Fabrication Method Thereof,” relates to “structures and methods for forming a 3D memory device.” Ex. 1001, code (54), 8:63–64. The Specification teaches that “multiple dielectric stacks or multiple stacks of dielectric pairs (e.g., sacrificial material layer/insulating material layer pairs) are formed sequentially along a direction perpendicular to the surface of a substrate.” *Id.* at 7:25–28. The lower dielectric stack closest to the top surface of the substrate is formed first, sub-channel holes and sub-pillar holes are formed therein, and a patterning process is performed to form a staircase structure (e.g., the lower staircase structure). *Id.* at 7:31–37. An upper staircase structure is formed over the lower staircase structure, with sub-channel holes and sub-pillar holes that align and join with the sub-channel holes and sub-pillar holes in the lower staircase structure. *Id.* at 7:37–44. The upper staircase structure and the lower staircase structure form a multi-stack staircase structure, with the adjoining sub-channel holes and sub-pillar holes “filled with suitable materials to form semiconductor channels and supporting pillars, respectively.” *Id.* at 7:44–49. The supporting pillars “can include one or more connection portion formed by the adjoining sub-pillar holes,” and “[t]he sidewall can thus have unaligned (or disjointed) surfaces at the connection portions.” *Id.* at 8:35–41.

Figure 3 is reproduced below.

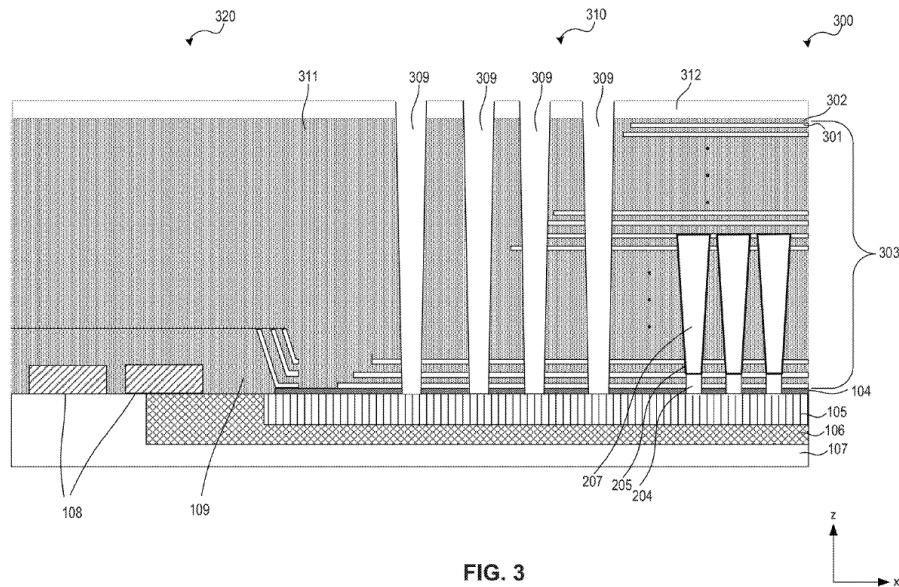


Figure 3 is an illustration of a cross-sectional view of a 3D memory device at a stage of the fabrication process. Ex. 1001, 5:24–26. Memory structure 300 includes two-stack staircase structure 303, dielectric filling structure 311, and plurality of pillar holes 309. *Id.* at 13:11–17. The '031 patent explains that “[d]ielectric filling structure 311 is deposited in periphery region 320 and core region 310 to fill in the space” created by removing portions of the dielectric stack to form staircase structure 303. *Id.* at 13:36–41. A suitable planarization method “can be performed to remove any excessive dielectric filling material overlying the topmost surface of staircase structure 303,” and “[t]he remaining portion of the deposited dielectric filling material (e.g., over staircase structure 303 and isolation layer 109) can form dielectric filling structure 311 that surrounds staircase structure 303.” *Id.* at 13:41–48.

Figure 4 is reproduced below.

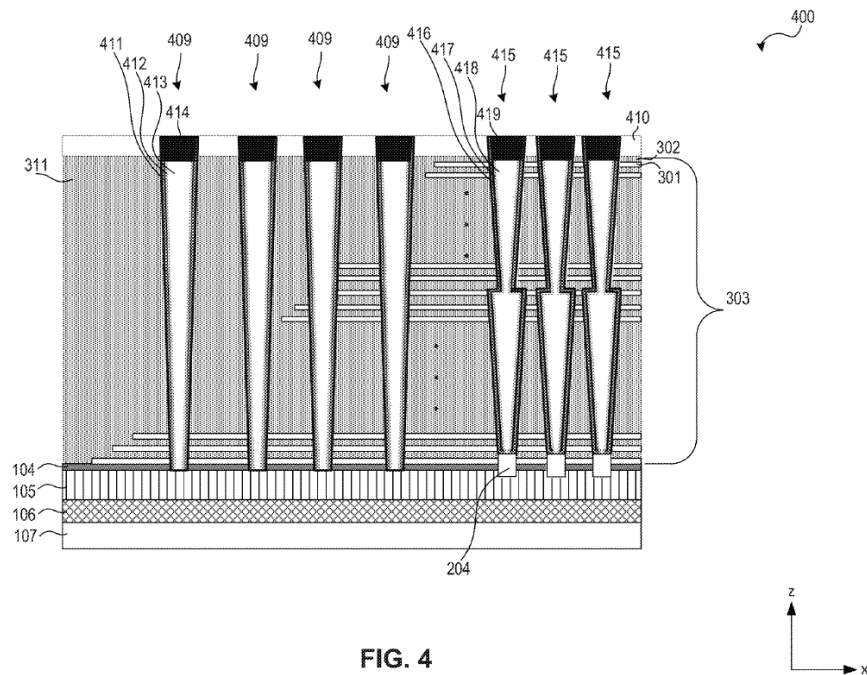


Figure 4 illustrates memory structure 400 formed based on memory structure 300 depicted in Figure 3 above. Ex. 1001, 14:35–36. “[M]emory structure 400 can be formed by forming a plurality of second sub-channel holes over first sub-channel holes 205 [shown in Figure 3], filling the first and second sub-channel holes and pillar holes 309 to form semiconductor channels 415 and supporting pillars 409” along with “drain regions 419 over semiconductor channels 415 and dummy drain regions 404 over supporting pillars 409.” *Id.* at 14:37–43.

#### *E. Challenged Claims*

Petitioner challenges claims 1–5 of the ’031 patent. Claim 1, the only independent claim challenged, is illustrative of the claimed subject matter and is reproduced below.

1. [1.PRE] A memory device, comprising:  
[1.A] a substrate;

- [1.B] a multiple-stack staircase structure comprising a plurality of staircase structures stacked over the substrate, [1.C] wherein each of the plurality of staircase structures comprises a plurality of conductive layers, wherein each of the plurality of conductor layers is located between two insulating layers;
- [1.D] a filling structure surrounding the multiple-stack staircase structure;
- [1.E] a semiconductor channel extending through the multiple-stack staircase structure, [1.F] wherein the semiconductor channel comprises unaligned sidewall surfaces; and
- [1.G] a supporting pillar extending through at least one of the multiple-stack supporting structure and the filling structure, [1.H] wherein the supporting pillar comprises aligned sidewall surfaces.

Ex. 1001, 26:15–32 (bracketed material added).

*F. Asserted Grounds*

Petitioner asserts that claims 1–5 would have been unpatentable on the following grounds:

| <b>Claim(s) Challenged</b> | <b>35 U.S.C. §</b> | <b>Reference(s)/Basis</b> |
|----------------------------|--------------------|---------------------------|
| 1–4                        | 103 <sup>1</sup>   | Kim <sup>2</sup>          |
| 1, 2, 4, 5                 | 103                | Tessariol <sup>3</sup>    |
| 4                          | 103                | Kim, Tessariol            |
| 1, 2, 4, 5                 | 103                | Tessariol, Kim            |

---

<sup>1</sup> The Leahy-Smith America Invents Act (“AIA”), Pub. L. No. 112–29, 125 Stat. 284 (2011), revised 35 U.S.C. §§ 102 and 103 effective March 16, 2013. Because the ’031 patent has an effective filing date after March 16, 2013 (Ex. 1001, codes (22), (63)), we refer to the AIA version of Sections 102 and 103.

<sup>2</sup> Kim, US 10,381,369 B2, issued Aug. 13, 2019 (Ex. 1005).

<sup>3</sup> Tessariol, US 2019/0081061 A1, published Mar. 14, 2019 (Ex. 1006).

Pet. 8. Petitioner relies on the Declarations of Sanjay Banerjee, Ph. D. (Ex. 1003; Ex. 1025). Patent Owner relies on the Declaration of Kelin Kuhn, Ph.D. (Ex. 2007).

## II. ANALYSIS

### *A. Level of Ordinary Skill in the Art*

Petitioner contends that a person of ordinary skill in the art (“POSITA”) would have had “a bachelor of science degree in electrical engineering or a similar discipline” with “2–3 years of professional experience working with (*e.g.*, researching, designing, or teaching) monolithic 3D structures and NAND memory devices,” or “an equivalent level of skill, knowledge, and experience (*e.g.*, an advanced degree may replace some of the professional experience).” Pet. 22–23. Petitioner further contends that a “POSITA would have been aware of and generally knowledgeable about 3D NAND’s structure, its component parts, how it operates, and how it is controlled.” *Id.* at 23 (citing Ex. 1003 ¶¶ 41–44). Patent Owner states that it does not object to the definition of a POSITA proffered by Petitioner. PO Resp. 13–14 (citing Pet. 22).

In the Institution Decision, we adopted the assessment offered by Petitioner. Dec. 7. Because Petitioner’s definition of the level of skill in the art is consistent with the ’031 patent and the asserted prior art, we maintain it for purposes of this Final Written Decision. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir 2001).

### *B. Claim Construction*

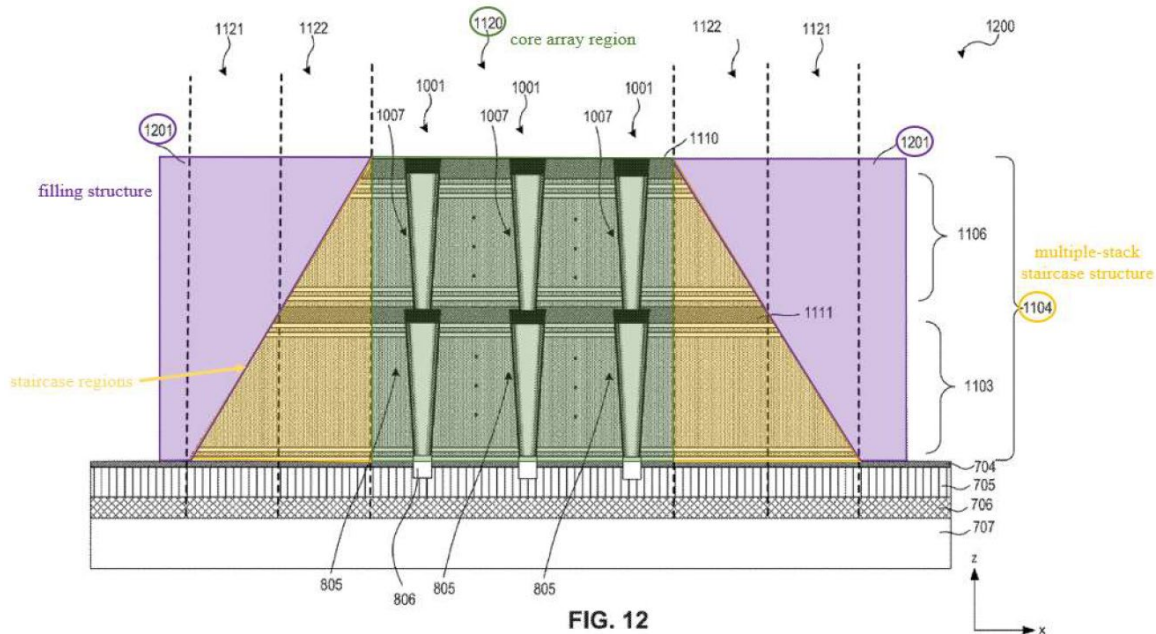
We construe each claim “in accordance with the ordinary and customary meaning of such claim as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent.” 37 C.F.R. § 42.100(b). Under this standard, claim terms are generally given their plain

and ordinary meaning as would have been understood by a person of ordinary skill in the art at the time of the invention and in the context of the entire patent disclosure. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1313 (Fed. Cir. 2005) (en banc). Only those terms in controversy need to be construed, and only to the extent necessary to resolve the controversy. *Realtime Data LLC v. Iancu*, 912 F.3d 1368, 1375 (Fed. Cir. 2019).

Petitioner contends that “the terms of the ’031 Patent’s claims do not require further construction and can be afforded their plain and ordinary meaning.” Pet. 22 (citing Ex. 1003 ¶¶ 76–77). Patent Owner proposes a construction for the term “surrounding” in claim 1. PO Resp. 14–19.

1. “*surrounding*”

In the Institution Decision, we preliminarily construed “surrounding” to mean “encircling” or “to be all the way around (something).” Dec. 11–12. Patent Owner agrees with this preliminary construction, contending that it “is both consistent with the plain and ordinary meaning of the term and supported by the intrinsic evidence.” PO Resp. 14. Patent Owner provides an annotated version of the ’031 patent’s Figure 12 (reproduced below) to illustrate its contentions.



*Id.* at 15–16. Annotated Figure 12 is an illustration of a cross-sectional view of a 3D memory device described in the '031 patent, with Patent Owner's addition of purple shading to area 1201, labeled "filling structure," yellow shading to component 1104, labeled "multiple-stack staircase structure," and green shading to area 1120, labeled "core array." *Id.* After noting that "Fig. 12 has labels provided for x and z directions, and the y direction is perpendicular to both directions and points into the page," Patent Owner contends that "staircase regions ('first staircase region 1121' and 'second staircase region 1122') are shown to extend in the +x and -x directions" and "[t]he '031 [patent] makes clear that the staircase regions also extend in the +y and -y directions, and therefore 'surround' the memory structure." *Id.* at 15–16 and n.3 (citing Ex. 1001, 13:27–28, 22:30–32; Ex. 2007 ¶ 72).

Patent Owner also contends that the '031 patent "uses the term 'surrounding' consistently as 'encircling' in multiple other instances." *Id.* at 18 (citing Ex. 1001, 2:12–14, 15:49–57, 3:31–35, 4:13–17, 18:25–26; Ex. 2007 ¶ 74). Patent Owner additionally cites to several dictionary

definitions to support its contention that this is the plain meaning of “surrounding,” and contends that “[t]he claims use the term ‘surrounding’ instead of narrower alternatives, such as ‘covering’ or the concept of being ‘between’ two structures.” *Id.* at 15 (citing Exs. 2001–2004; Ex. 2007 ¶ 70).

Petitioner argues that Patent Owner’s “interpretation is flatly inconsistent with the specification.” Pet. Reply 2 (citing Ex. 1025 ¶¶ 11–19; *Phillips*, 415 F.3d at 1313). Petitioner asserts that the ’031 patent “makes clear that ‘a filling structure surrounding the multiple-stack staircase structure’ requires nothing more than a ‘filling structure’ that ‘fill[s] [the] space formed by the formation of [the multiple-stack] staircase structure.’” *Id.* (citing Ex. 1001, 13:11–38) (alterations in original). According to Petitioner, “the ’031 patent consistently explains that a ‘filling structure’ is deposited (via, e.g., CVD) to fill the ‘space formed by the formation of [the] staircase structure’—and, by filling in the space, the ‘filling structure . . . surrounds’ the staircase structure.” *Id.* at 3 (citing Ex. 1025 ¶ 15; Ex. 1001, 11:44–60, 13:36–59, 19:41–49, 22:61–23:9, 24:26–38; Ex. 1026, 97:21–101:14, 116:18–117:13) (alterations in original, emphasis omitted). Petitioner argues that the ’031 patent “does not teach or illustrate the filling structure ‘deposited to,’ e.g., the ‘back’ and ‘front’ (i.e., y-direction in Fig. 3) of the staircase,” and “[t]he claims cannot require more than what the specification supports.” *Id.* at 4 (citing Ex. 1025 ¶ 16).

We begin our analysis with the language of claims. *Phillips*, 415 F.3d at 1312; *see also SuperGuide Corp. v. DirecTV Enterprises, Inc.*, 358 F.3d 870, 874–875 (Fed. Cir. 2004) (“There is a ‘heavy presumption’ that the terms used in the claims ‘mean what they say and have the ordinary meaning that would be attributed to those words by persons skilled in the relevant art.’”). Claim 1 recites, in relevant part, “a filling structure

surrounding the multiple-stack staircase structure.” Ex. 1001, 26:24–25. The plain language of the claim does not address the relationship between the filling structure and the multiple-stack staircase structure other than requiring that the filling structure “surround” the multiple-stack staircase structure.

We turn next to the specification. *Phillips*, 415 F.3d at 1315; *see also SuperGuide*, 358 F.3d at 875 (“We review the patent’s written description and drawings to confirm that the patentee’s own use of the disputed term is consistent with the meaning given to it by the court.”). The ’031 patent teaches that dielectric pairs of different tiers are etched to form staircases extending along the x-y plane. Ex. 1001, 13:27–28. As described above (§ I.D, *supra*), dielectric filling structure 311 is formed by depositing a dielectric filling material to fill the space remaining after portions of dielectric stack 203 are removed to form staircase structure 303. *Id.* at 13:36–41; *see also id.* at 22:63–65 (“Memory structure 1200 can be formed by forming dielectric filling structure 1201 to fill the space formed by the removal of portions of dielectric stack 1003.”) The ’031 patent then teaches that excess dielectric filling material overlying the topmost surface of staircase structure 303 is removed using a suitable planarization method. *Id.* at 13:41–44; *see also* 22:67–23:5 (performing a planarization process to remove excess dielectric filling structure 1201 over the top surface of memory structure 1200). According to the ’031 patent, the portion of the deposited dielectric filling material that remains “over staircase structure 303 and isolation layer 109” forms “dielectric filling structure 311 that *surrounds* staircase structure 303.” *Id.* at 13:44–48 (emphasis added); *see also id.* at 1:56–58 (stating in “some embodiments, the memory device also includes a filling structure surrounding the multiple-stack staircase structure”).

These disclosures in the '031 patent indicate that the staircase structure is etched along the x-, y-, and z-axes, and the dielectric filling structure fills the spaces in the x-, y-, and z-directions created when the staircase structure is etched. Because the excess portion of the dielectric filling structure overlying the top of the staircase structure is removed, what remains is dielectric filling structure in the spaces around the staircase structure in the x-, y-, and z-planes. In this way, the '031 patent teaches that the dielectric filling structure surrounds, i.e., is all around or encircles, the staircase structure.

This understanding of “surround” is consistent with the way “surround” is used in the '031 patent and with the plain and ordinary meaning of “surround.” *See, e.g.*, 2:12–14 (“the supporting pillar is filled with at least one of an insulating material and a pillar-support material surrounded by the insulating material”), 10:25–29 (periphery region 120 “can surround core region 110” and “can also be under core region 110, depending on the type of the memory device”), 15:49–53 (“Charge trapping film 416 can also include a storage unit layer (memory layer) over and surrounded by the block dielectric layers for trapping charges and forming a plurality of charge storage regions along the z axis.”), 18:25–26 (“In some embodiments, the insulating liner/spacer layer surrounds the support material.”); Ex. 2001, 3 (New Oxford American Dictionary defining “surround” as “to be all around (someone or something)”); Ex. 2002, 3 (The American Heritage College Dictionary defining “surround” as “to extend on all sides simultaneously; encircle”); Ex. 2003, 3 (Webster’s II New College Dictionary defining “surround” as “to encircle on all sides of simultaneously”); Ex. 2004, 3 (Merriam-Webster’s Dictionary and Thesaurus defining “surround” as “to enclose on all sides”).

We disagree with Petitioner that the '031 patent “does not teach or illustrate the filling structure ‘deposited to’ e.g., the ‘back’ and ‘front’ (i.e., the y-direction in Fig. 3) of the staircase.” Pet. Reply 4. As discussed, the '031 patent teaches that the staircase structures extend along the x-y plane. *See* Ex. 1001, 13:27–28. The '031 patent defines “staircase structure” as “a structure having stepped surfaces,” and defines “stepped surfaces” as

a set of surfaces that include at least two horizontal surfaces (e.g., along x-y plane) and at least two (e.g., first and second) vertical surfaces (e.g., along the z axis) such that each horizontal surface is adjoined to a first vertical surface that extends upward from a first edge of the horizontal surface, and is adjoined to a second vertical surface that extends downward from a second edge of the horizontal surface.

*Id.* at 9:39–49. Consequently, the dielectric filling material that is deposited into the space formed by creating the staircase structure will be over the stepped surfaces that comprise the staircase structure, including surfaces along the x-y plane and along the z-axis. *See also id.* at Fig. 12; Ex. 2013 ¶ 72 (Dr. Kuhn explaining that the staircase regions in Figure 12 extend in the +x and -x directions, and the Specification teaches that the staircase regions also extend in the +y and -y directions) (citing Ex. 1001, 13:27–28, 22:30–32).

For these reasons, we determine that “surrounding” as used in claim 1 of the '031 patent means “all around” or “encircling.”

*C. Ground 1: Asserted Obviousness over Kim*

Petitioner contends that claims 1–4 would have been obvious over Kim. Pet. 27–56.



common source plug CSP and stack structures ST. *Id.* at 6:27–29. Vertical structures VS are provided in each of channel holes CH and “may penetrate each of the stack structures ST on the cell array region CAR.” *Id.* at 7:4–8. Vertical structure VS includes vertical insulating layer VP, upper semiconductor pattern USP, lower semiconductor pattern LSP, and filling insulation pattern VI. *Id.* at 7:16–19. “The filling insulation layer 110 may be disposed on the substrate 100 and may cover the stack structure ST.” *Id.* at 9:53–54.

Kim teaches that “[p]lanar areas of the electrodes EL on the connection region CTR may increase sequentially as a distance from the top surface of the substrate 100 in the third direction D3 increases,” and the lowest electrode EL of stack structure ST “may have the largest planar area,” while the uppermost electrode EL of stack structure ST “may have the smallest planar area.” Ex. 1005, 6:63–7:3.

## 2. *Claim 1*

Petitioner contends that Kim teaches all of the limitations of claim 1. Pet. 27–47. For example, Petitioner contends Kim teaches “a substrate” (substrate 100), “a multiple-stack staircase structure comprising a plurality of staircase structures stacked over the substrate” (stack structure ST including lower substrate SS1 and upper substrate SS2), “each of the plurality of staircase structures comprises a plurality of conductor layers, wherein each of the plurality of conductor layers is located between two insulating layers” (electrode layers EL and insulating layers IL), and “a semiconductor channel extending through the multiple-stack staircase structure” (vertical structure VS extending through stack structure ST). *Id.* at 27–31 (citing Ex. 1005, 5:60–6:1, 6:30–35, 6:41–63, 9:11–13, 9:39–41, 10:8–16, 10:50–59, 13:41–50, Figs. 4B, 12; Ex. 1003 ¶¶ 97, 99–106), 38–39

(citing Ex. 1005, 1:42–45, 5:1–3, 5:37–39, 7:15–24, Fig. 4B; Ex. 1003 ¶¶ 118–119).

With respect to limitation [1.D] (“a filling structure surrounding the multiple-stack staircase structure”), Petitioner contends that “Kim discloses a ‘filling insulating layer 110’ that ‘may be disposed on the substrate 100 and may cover the stack structures ST. The filling insulation layer 100 may have a planarized top surface.’” Pet. 32 (citing Ex. 1005, 9:53–56). Petitioner further contends that “after forming the staircase structures, the insulating layer 110 fills the voids.” *Id.* (citing Ex. 1005, 10:60–11:21, Figs. 9, 10).

Patent Owner responds that “Kim’s insulation material does not surround the stack structure because it is disclosed as only covering the top and one side of the structure.” PO Resp. 24–25. Patent Owner argues that Kim “merely teaches that the stack structure may be covered by the filling insulation layer [110] (i.e., the material is on top) and is on one side, but it never says that the insulating layer surrounds the stack structure.” *Id.* at 25–26 (citing Pet. 32; Ex. 1005, 9:53–56; Ex. 2013 ¶ 96) (emphasis omitted). Patent Owner also argues that Kim does not suggest that filling insulation layer 110 covers the sides of the structure in the -D1, +D1, and -D2 directions. *Id.* at 26–27 (citing Ex. 2013 ¶ 97). In particular, Patent Owner argues that trenches formed in the +D2 and -D2 directions after fabrication of filling insulation layer 110 prevent filling insulation layer 110 from “surrounding” the stack structures as required by limitation [1.D]. *Id.* at 27–30. Patent Owner further argues that Kim does not show filling insulation layer 110 in the -D2 direction. *Id.* at 30–32.

After considering the complete record, we are persuaded that Petitioner sufficiently establishes that Kim teaches limitation [1.D]. As set

forth above, we construe “surrounding” to mean “all around” or “encircling.” *See* § II.B.1, *supra*. Kim teaches that “filling insulation layer 110 may be formed on *an entire top surface* of the substrate 100 to cover the mold structure MT.” Ex. 1005, 11:11–13 (emphasis added); *see also* 9:53–54 (“The filling insulation layer 110 may be disposed on the substrate 100 and may cover the stack structures ST.”). Prior to this step, mold structure MT is formed by vertically and alternately stacking insulation layers on the substrate, and mold structure MT is formed into a staircase structure. *Id.* at 10:8–11, 10:50–55, 10:60–63. Because Kim teaches that mold structure MT is formed on the surface of the substrate, and filling insulation layer 110 is formed on an entire top surface of the substrate, it follows that filling insulation layer 110 is also formed on the structures already present on the substrate, including the staircase structure in mold structure MT. *See, e.g.*, Ex. 1003 ¶ 112. In other words, because Kim teaches depositing filling insulation layer 110 on the entire top surface *of the substrate*, a POSITA would have understood that the filling material was deposited to the outer edges of the substrate and not to just a portion of the substrate. As a result, a POSITA would have understood that Kim’s filling insulation layer 110 would extend around the staircase structure.

This is partially depicted in Kim's Figure 10, reproduced below.

FIG. 10

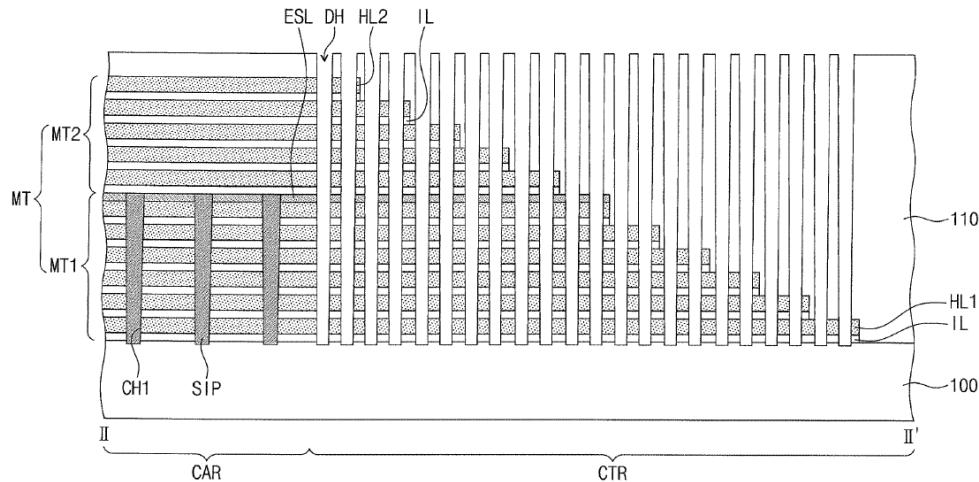


Figure 10 is a cross-sectional view of a 3D semiconductor device during the manufacturing process. Ex. 1005, 4:29–32. Figure 10 shows that filling insulation layer 110 covers the top and right side of mold structure MT, as well as the portion of substrate 100 that extends out from the bottom step of mold structure MT. *Id.* at Fig. 10; *see id.* at Figs. 4A, 4B. Dr. Banerjee persuasively explains that this figure does not depict all of the areas of the semiconductor device upon which the filling material was deposited:

[A]s shown in Fig. 10 above, Kim discloses filling material on the outer edge of where the staircase region ends (*e.g.*, on the far-right side of the figure). Consistent with the filling pattern, a POSITA would have understood, and certainly found it obvious, that the filling material would similarly extend to the other outer edges of the memory device as well, not just the right side (*viz.*, the filling material would be present on all sides/edges of the memory device). This is consistent with traditional semiconductor fabrication processing and chip design techniques. PECVD (Plasma-Enhanced Chemical Vapor Deposition), which is often used for this purpose, is an isotropic process leading to deposition on all sides, except the bottom surface which is blocked. No extra manufacturing steps would

be needed to accomplish this result, and having uniform filling material on all sides would make for a symmetric device, which is generally desirable.

Ex. 1003 ¶ 113; *see also* Ex. 1035 ¶¶ 23–30 (Dr. Banerjee explaining the fabrication process).

We have considered Patent Owner’s arguments that Kim does not teach filling material that surrounds the staircase structure, and find them unavailing. For example, Patent Owner argues that “there is no depiction of insulating layer 110 to the left of the staircase structure.” PO Resp. 30. But Kim’s Figures 4A, 4B, and 10, which show filling insulation layer 110 on the top and one side of the staircase structure, do not depict the left side of the staircase structure. *See* Ex. 1005, Figs. 4A, 4B, 10; Ex. 1003 ¶¶ 44–45. In particular, Figures 4A and 4B are cross-sectional views taken along lines I-I’ of the 3D semiconductor memory device depicted in Figure 3, and Figure 10 is a cross-sectional view taken along lines II-II’ in Figure 3. *Id.* at 4:18–22, 4:29–32, Figs. 3, 4A, 4B, 10. Because these figures do not depict the left side of the staircase structure, it follows that the figures would not depict what layers or structures are present on the left side of the staircase structure, including the presence of filling insulation layer 110. Thus, that there is no depiction of insulating layer 110 to the left of the staircase structure in these figures is not evidence that there is no filling insulation layer 110 to the left of the staircase structure; nor does it preclude a finding that Kim’s insulating layer 110 surrounds the staircase structure as recited in limitation [1.D].

We also disagree that the trenches described in Kim prevent filling insulation layer 110 from “surrounding” the stack structures. *See* PO Resp. 27–30. Kim teaches that “[a] trench TR may be defined between the

mold structures MT adjacent to each other. The trenches TR may expose portions of the substrate 100. The trenches TR may extend in parallel to the mold structures MT in the second direction D2.” Ex. 1005, 12:15–19. Kim also teaches that “[i]nsulating spacers SP and a common source plug CSP may be formed in each of the trenches TR.” *Id.* at 12:30–31. While subsequent processing may result in the creation of structures in filling insulation layer 110, filling insulation layer 110 still is encircling mold structures MT, because “surrounding” does not require complete continuity.

Patent Owner does not address Petitioner’s specific contentions with respect to the other limitations of claim 1. *See* PO Resp. We reviewed Petitioner’s contentions for all the elements of independent claim 1, as well as the supporting evidence. Pet. 27–47. Based on the record before us, we are persuaded that Petitioner’s discussion of the particular structures in Kim, and the explanations in the Banerjee Declarations, shows that Kim teaches all of the limitations of claim 1. Accordingly, we determine that Petitioner shows, by a preponderance of the evidence, that claim 1 would have been obvious over the teachings of Kim.

### 3. *Claims 2 and 3*

Claim 2 depends from claim 1, and adds limitations related to the multi-stack staircase structure and the supporting pillar. Ex. 1001, 26:33–39. Claim 3 depends from claim 2, and add limitations related to the supporting pillar and the semiconductor channel. *Id.* at 26:40–45. Patent Owner does not address Petitioner’s specific contentions with respect to the limitations of dependent claims 2 and 3. *See* PO Resp. We reviewed Petitioner’s contentions for all the elements of claims 2 and 3, as well as the supporting evidence. Pet. 47–55. Based on the record before us, we are persuaded that Petitioner’s discussion of the particular structures in Kim, and

the explanations in the Banerjee Declarations, shows that Kim teaches all of the limitations of dependent claims 2 and 3. Accordingly, we determine that Petitioner shows, by a preponderance of the evidence, that claims 2 and 3 would have been obvious over the teachings of Kim.

4. *Claim 4*

Claim 4 depends from claim 2, and further recites:

the supporting pillar and the semiconductor channel are filled with different filling layers; and

the supporting pillar is filled with at least one of an insulating material and a pillar-support material surrounded by the insulating material, and the semiconductor channel is filled with at least one of a charge trapping film, a semiconductor channel film, and a dielectric core.

Ex. 1001, 26:46–54. Petitioner identifies Kim’s dummy structures DS as the recited “supporting pillar” and Kim’s vertical structures VS as the recited “semiconductor channel.” Pet. 42–47. Petitioner points to Kim’s teaching that “[a] layer or component of each of the dummy structures may be different from the layer(s) or component(s) of each of the vertical structures VS” as disclosing the “the supporting pillar and the semiconductor channel are filled with different filling layers” limitation of claim 4. *Id.* at 55 (citing Ex. 1005, 13:28–33).

With respect to the “the supporting pillar is filled with at least one of an insulating material and a pillar-support material surrounded by the insulating material” limitation of claim 4, Petitioner contends that “a POSITA would have understood that Kim’s dummy structures could have been made with a conductive core (the supporting material) and insulating liner.” Pet. 55–56 (citing Ex. 1003 ¶ 156). Petitioner contends that Tessariol teaches that supporting pillars can be conductive vias or dummy

versions of the conductive vias, and “it would have been obvious simply to use conductive vias or dummy vias (which have an insulating liner and conductive core), and this would have been beneficial because the process to form them would use the same process steps as the conductive vias.” *Id.* at 56 (citing Ex. 1003 ¶ 157).

Patent Owner argues that, for dummy structures and vertical structures “Kim discloses only insulator/semiconductor material—silicon oxide, silicon nitride, silicon oxynitride, polysilicon—which cannot be used to form a ‘conductive core,’ i.e., the type of core upon which Petitioner bases its argument.” PO Resp. 47 (citing Ex. 1005, 13:33–36; Ex. 2013 ¶ 151) (footnote and internal citation omitted). Patent Owner also argues that Petitioner does not show “that Kim’s device needs or would even benefit from additional supporting structures.” *Id.* at 49 (citing Ex. 2013 ¶ 155; *Belden Inc. v. Berk-Tek LLC*, 805 F.3d 1064, 1075 (Fed. Cir. 2015)).

After reviewing the parties’ arguments and evidence, we are not persuaded that Petitioner shows that Kim teaches “the supporting pillar is filled with at least one of an insulating material and a pillar support material surrounded by an insulating material” as recited in claim 4.

Kim teaches that “dummy structures DS may physically support the stack structure ST on the connection region CTR.” Ex. 1005, 9:30–31. Kim also teaches that “[i]n some embodiments, each of the dummy structures DS may include a vertical insulating layer VP, an upper semiconductor pattern USP, a lower semiconductor pattern LSP, and a filling insulation pattern VI.” *Id.* at 9:31–35. Kim further teaches that upper semiconductor pattern USP and lower semiconductor pattern LSP “may include silicon (Si), germanium (Ge), or a mixture thereof and may have crystal structures different from each other. *Id.* at 7:54–57. Kim describes other embodiments

wherein dummy structures DS include a dummy pattern that may be formed of a silicon oxide layer, a silicon nitride layer, a silicon oxynitride layer, or a poly-silicon layer. *Id.* at 13:28–36. Accordingly, by its express disclosures, Kim teaches that dummy structures DS provide support for the stack structure and also identifies a number of materials from which dummy structures DS can be formed.

In light of these disclosures in Kim, neither Petitioner nor Dr. Banerjee adequately explains why a POSITA would have been motivated to make dummy structures DS with a conductive core as Petitioner proposes. In an obviousness analysis, some kind of reason must be shown as to why a POSITA would have thought of combining or modifying the prior art to achieve the patented invention. *See Innogenetics, N.V. v. Abbott Labs.*, 512 F.3d 1363, 1374 (Fed. Cir. 2008). Here, Petitioner offers only the general proposition that pillar support structures comprising electrically conductive material were known in the art, but this does not provide a reason why a POSITA would have been motivated to modify Kim’s dummy structures. Pet. 55–56; Ex. 1003 ¶¶ 156–157. Petitioner’s arguments and Dr. Banerjee’s testimony with respect to the modification of Kim leaves an analytical gap that does not apprise us of why a POSITA would have modified Kim’s dummy structures to include a conductive core as the pillar-support material recited in claim 4.

Instead, Petitioner attempts to imbue a POSITA with the knowledge of the claimed invention, when no prior art reference, references of record, or other evidence conveys or suggests that knowledge. Petitioner’s argument that a POSITA would have modified Kim in this way appears to be premised on Petitioner’s knowledge of the ’031 patent disclosure. This is improper hindsight reasoning. Petitioner needed to explain sufficiently what

would have led a person of ordinary skill in the art at the time of the invention to consider modifying Kim’s dummy structures to include a conductive core. Petitioner fails to provide such an explanation. *See W.L. Gore & Assoc., Inc. v. Garlock, Inc.*, 721 F.2d 1540, 1553 (Fed. Cir. 1983) (In an obviousness analysis, we must “cast the mind back to the time the invention was made” and “occupy the mind of one skilled in the art who is presented only with the references, and who is normally guided by the then-accepted wisdom in the art.”).

For these reasons, after considering Petitioner’s and Patent Owner’s positions, as well as their supporting evidence, we are not persuaded that Petitioner demonstrate that Kim teaches or suggests “the supporting pillar is filled with at least one of an insulating material and a pillar-support material surrounded by the insulating material” as required by claim 4.

#### 5. *Conclusion*

Having reviewed the parties’ arguments and evidence, we are persuaded that Petitioner shows by a preponderance of the evidence, that claims 1–3 of the ’031 patent would have been obvious over the teachings in Kim, but does not show by a preponderance of the evidence that claim 4 would have been obvious over the teachings of Kim.

#### D. *Ground 2: Asserted Obviousness over Tessariol*

Petitioner contends that claims 1, 2, 4, and 5 would have been obvious over Tessariol. Pet. 57–86.

##### 1. *Overview of Tessariol*

Tessariol is directed “to devices, to methods used in forming a circuit structure, and to methods used in forming an array of elevationally-extending transistors and a circuit structure adjacent thereto.” Ex. 1006 ¶ 1.

Tessariol teaches construction 10 comprises base substrate 11 and various materials formed elevationally over base substrate 11. *Id.* ¶ 27.

Figure 6 is reproduced below.

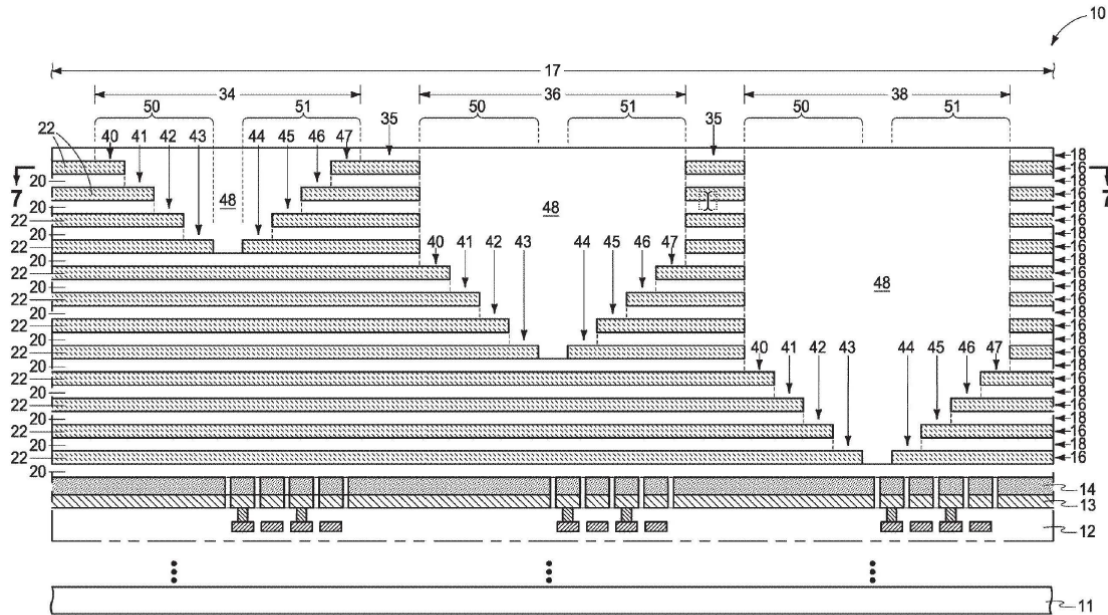


**FIG. 6**

Figure 6 is a diagrammatical cross-sectional view of a portion of the substrate construction in process as described in Tessariol. Ex. 1006 ¶ 13. Vertically-alternating tiers 16 and 18 of different composition first and second materials 20 and 22 are formed above substrate 11. *Id.* ¶ 29. Stair step structures 34, 36, and 38 individually comprise steps 40–47 and are separated from one another by an elevationally-outer landing 35. *Id.* ¶ 34. Insulating material 48 is above steps 40–47 in each of stair step structures 34, 36, and 38.

FIG. 9

Figure 9 is a diagrammatic cross-sectional view of a portion of a substrate construction in process as described in Tessariol. *Id.* ¶ 16. Dummy-structure openings 56 and via openings 54 are formed through insulating material 48 and vertically-alternating tiers 16 and 18. *Id.* ¶ 37. Operative conductive vias 58 are formed within via openings 54, and dummy structures 60 are formed within dummy-structure openings 56. *Id.* ¶ 38. Operative conductive vias 58 and dummy structures 60 comprise insulative lining 62 and conductive core 64. *Id.* Some alternate ones of operative conductive vias 58 are directly electrically coupled to individual conductive lines 66 through source material 14, conductive material 13, and conductive vias 67, and other alternate ones of operative conductive vias 58 are directly electrically coupled to individual conductive lines 66 through materials 14 and 13 to be directly against individual conductive lines 66. *Id.* ¶ 39.

2. *Claim 1*

Petitioner contends that Tessariol teaches all of the limitations of claim 1. Pet. 57–81. For example, Petitioner contends Tessariol teaches “a substrate” (base substrate 11), “a multiple-stack staircase structure comprising a plurality of staircase structures stacked over the substrate” (first stack 24 and second stack 30, having staircase regions, e.g., 34, 36, 38), “each of the plurality of staircase structures comprises a plurality of conductor layers, wherein each of the plurality of conductor layers is located between two insulating layers” (tiers 18 composed of second material 22 and tiers 16 composed of first material 20), and “a semiconductor channel extending through the multiple-stack staircase structure” (within channel opening 26, a transistor material 32). *Id.* at 57–66, 71–72 (and evidence cited therein).

With respect to limitation [1.D] (“a filling structure surrounding the multiple-stack staircase structure”), Petitioner contends that Tessariol teaches that insulating material 48 (e.g., silicon dioxide and/or silicon nitride) is above steps 40–47, and “additionally discloses the deposition of ‘dielectric material 74’ around the staircase structures,” which “may extend through the array region.” Pet. 66–68 (citing Ex. 1006 ¶¶ 34, 43, Figs. 6, 11). Petitioner also contends that Tessariol’s insulator material 86 that surrounds components 69, 81, 82, and 84 is a dielectric filling structure that “encases the entire stack structure to provide a region for metal layer connections to the lower layers.” *Id.* at 68–69 (citing Ex. 1006 ¶ 46, Figs. 17, 18; Ex. 1003 ¶¶ 179–181).

Patent Owner argues that “none of the features identified by Petitioner, either individually or in combination, surrounds Tessariol’s steps.” PO Resp. 56. In particular, Patent Owner argues that insulating

material 48 covers the steps from above. *Id.* at 57–59. Patent Owner argues that dielectric material 74 divides, but does not surround, Tessariol’s steps. *Id.* at 59–61. And Patent Owner argues that insulator material 86 only covers the tops of the stacks. *Id.* at 61–63.

As set forth above, we construe “surrounding” to mean “all around” or “encircling.” *See* § II.B.1, *supra*. Thus, Petitioner must show that Tessariol’s insulating material 48, dielectric material 74, and insulation material 68 encircle, or are all around, Tessariol’s staircase structures. *Harmonic Inc. v. Avid Tech. Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016) (stating that it is Petitioner’s burden to show with particularity why a challenged claim is unpatentable); *see also* 37 C.F.R. § 42.104(b)(4) (A petition “must specify where each element is found in the prior art patents or printed publications relied upon.”). After reviewing the complete trial record, we are not persuaded that Petitioner has done so.

Tessariol teaches that “insulating material 48 (e.g., silicon dioxide and/or silicon nitride) is above steps 40–47,” indicating that it covers the tops of the steps. Ex. 1006 ¶ 34; *see also id.* at claim 1 (“the stair step structure comprising insulating material above the steps”), Figs. 6, 7. Tessariol teaches that dielectric material 74 fills trenches 70, and trenches 70 are “horizontally-elongated” and “formed to extend elevationally into vertically-alternating tiers 16, 18.” *Id.* ¶¶ 41, 43. Tessariol teaches that insulator material 86 “surround[s] components 69, 82, 81, and 84.” *Id.* ¶ 46. With respect to components 69, 81, 82, and 84, Tessariol teaches:

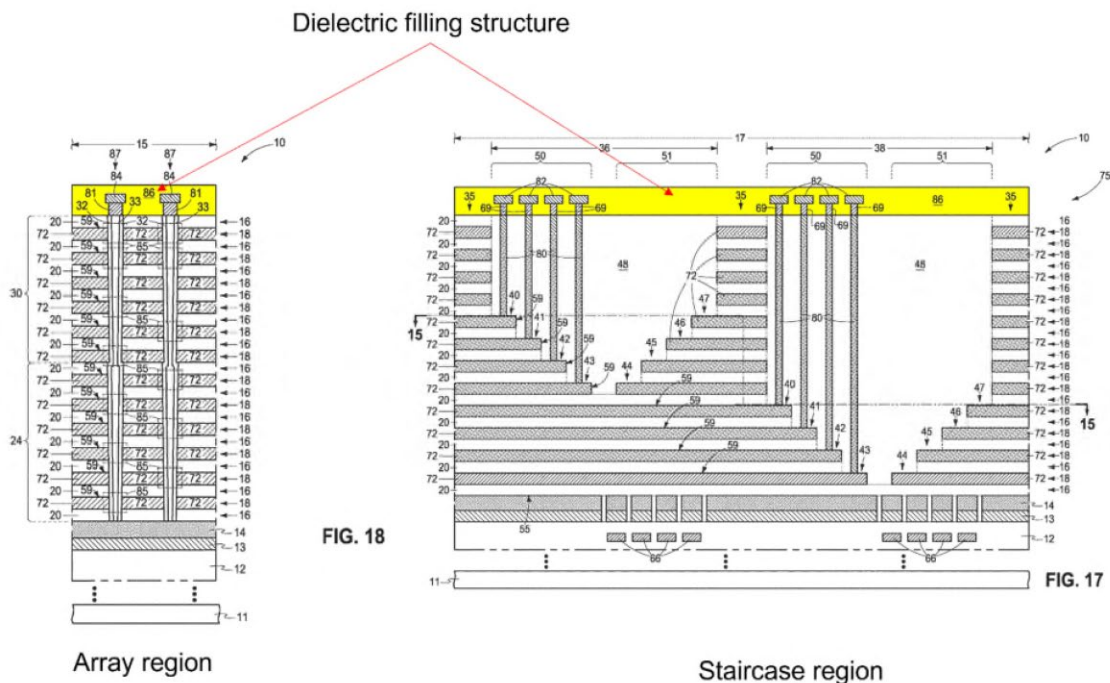
Interconnect lines 82 have been formed above stair step structures 36 and 38 and individually directly electrically couple together different individual conducting vias 80 to different individual operative conductive vias 58 through conductive extensions 69. . . . Strings 87 of transistors 85 may

connect with individual conductive lines 84 through conductive extensions 81.

*Id.* Components 69, 81, 82, and 84 are above the stacks. *See* Ex. 1006, Figs. 17, 18; Pet. 69; Ex. 2013 ¶ 189.

Given these disclosures in Tessariol, neither Petitioner nor Dr. Banerjee adequately explains how insulating material 48, dielectric material 74, and insulator material 86 encircles, or is all around, the staircase structures. For example, Petitioner argues that dielectric material 74 is deposited around the staircase structure, but does not adequately explain what parts or sections of the staircase structure dielectric material 74, which is within trenches 70, is deposited around. *See, e.g.,* Pet. 67–68 (citing Ex. 1006 ¶ 43, Fig. 11); ; Ex. 1003 ¶ 180; *see also* Ex. 1006 ¶ 43, Fig. 11 (depicting dielectric material 74 only in trenches 70)

Similarly, Petitioner contends that insulating material 86 “encases the entire stack structure,” and provides annotated versions of Tessariol’s Figures 17 and 18, reproduced below, to illustrate.



Pet. 68–70 (citing Ex. 1006 ¶ 46, Figs. 17, 18; Ex. 1003 ¶ 184). Figure 17 (right) is a view of a processing step shown in Figure 15 (not pictured) taken through line 17-17 in Figure 15, and Figure 18 (left) is a cross-sectional view of a portion of the substrate construction commensurate with the processing in Figure 14. Ex. 1006 ¶¶ 24–25. Petitioner’s annotations include highlighting insulating material 86 yellow and labeling the highlighted region “Dielectric filling structure,” and identifying Figure 17 as the “Staircase region” and Figure 18 as the “Array region.” Pet. 69. Annotated Figures 17 and 18 show insulating material 86 layered on top of insulating material 48, which itself only covers the steps. It is not clear from annotated Figures 17 and 18, and Petitioner and Dr. Banerjee do not explain, how insulating material 86 (located above the staircase) “encases” the entire stack structure. In particular, Petitioner fails to show that Tessariol discloses or suggest an insulator material at the ends of Tessariol’s device in either the D1 or D2 direction. *See* Ex. 2013 ¶ 200. Thus, unlike Petitioner’s showing for Kim, Petitioner does not sufficiently show that Tessariol’s insulating material 48, dielectric material 74, or insulator material 86, either alone or in combination, are deposited in such a way as to surround the staircase structure.

Petitioner also argues:

A POSITA would have understood, or at least found obvious, that as taught by Kim, Tessariol’s “dielectric material 74” and “insulator material 86” is like Kim’s “filling insulating layer 110” that “may be disposed on the substrate 100 and may cover” the entire stack structure, and “may have a planarized top surface.” This electrically isolates the structure and was a conventional, routine insulating technique. This step would encase all sides of the device, like Kim. And [it] provide[s] the planarized surface for the interface between the upper-level metal layers for interconnects.

Pet. 70 (citing Ex. 1005, 9:53–56, 11:11–21; Ex. 1003 ¶ 183) (internal citations omitted). But Petitioner’s arguments and Dr. Banerjee’s testimony that it would have been obvious to modify Tessariol are largely conclusory and are not persuasive on the present record. *See id.* at 69–71; Ex. 1003 ¶ 183. Petitioner’s argument that electrically isolating the structure in this way “was a conventional, routine insulating technique” appears to be nothing more than a statement that a POSITA could have made the proposed modification. Obviousness, however, “concerns whether a skilled artisan not only *could have made* but *would have been motivated to make* the combinations or modifications of prior art to arrive at the claimed invention.” *Belden*, 805 F.3d at 1073 (citing *InTouch Techs., Inc. v. VGO Commc’ns, Inc.*, 751 F.3d 1327, 1352 (Fed. Cir. 2014)).

For these reasons, after considering Petitioner’s and Patent Owner’s positions, as well as their supporting evidence, we are not persuaded that Petitioner sufficiently demonstrates that Tessariol teaches or suggests “a filling structure surrounding the multiple-stack staircase structure” recited in claim 1. Accordingly, we determine that Petitioner does not show, by a preponderance of the evidence, that claim 1 would have been obvious over the teachings of Tessariol.

### 3. Claims 2, 4, and 5

Petitioner also contends that Tessariol teaches or suggests all of the limitations of claims 2, 4, and 5. Pet. 81–86. Claims 2, 4, and 5 depend, directly or indirectly, from claim 1, and therefore include the “a filling structure surrounding the multiple-stack staircase structure” limitation of claim 1. Ex. 1001, 26:33–39, 26:46–58. Thus, for the same reasons given above with respect to Petitioner’s challenge of claim 1, we also conclude

that Petitioner does not demonstrate by a preponderance of the evidence that claims 2, 4, and 5 would have been obvious over the teachings of Tessariol.

*E. Ground 3: Asserted Obviousness over Kim and Tessariol*

Petitioner contends that claim 4 would have been obvious over the combined teachings of Kim and Tessariol. Pet. 86–89. Petitioner asserts:

Ground 1 demonstrates that in view of Kim’s disclosures and the knowledge of a POSITA, claim 4 is unpatentable at least because it would have been obvious to a POSITA to employ dummy pillars with a conductive core and insulating liner as Kim’s dummy structures (“supporting pillars”). Ground 1 uses Tessariol to show that the use of such dummy structures was well known to a POSITA. Ground 3 expressly combines Kim with Tessariol to demonstrate the same point: Kim in view of Tessariol would render obvious employing a conductive core and insulating liner as the dummy pillars in Kim.

*Id.* at 86–87 (internal citations omitted).

Petitioner’s arguments with respect to Ground 3 are substantially similar to those discussed above with respect to claim 4 in Ground 1. For example, Petitioner contends that “a POSITA would have been motivated to employ Tessariol’s teaching of conductive cores with a conductive liner as Kim’s dummy structures (‘supporting pillars’)” because Tessariol describes pillars that provide the same stack support function as Kim. Pet. 87 (citing Ex. 1005, 9:30–31; Ex. 1006 ¶ 41; Ex. 1003 ¶ 214). Petitioner contends that Kim teaches that the dummy structures need not be the same material as the channel structures, and Tessariol provides other types of support pillars. *Id.* at 87–88 (citing Ex. 1005, 13:28–33; Ex. 1006 ¶¶ 37, 38, 41; Ex. 1003 ¶ 216). These arguments are not persuasive for the reasons set forth above with respect to our analysis of Petitioner’s challenge of claim 4 in Ground 1. § II.C.4, *supra*.

Petitioner further contends that “Kim’s dummy pillars include various thin layers, which unlike the solid metal core of Tessariol’s vias, are an inferior support member, and the overall structure provides less support than Tessariol’s metal core.” Pet. 87 (citing Ex. 1012, 4:60–5:12; Ex. 1003 ¶ 215). To support this contention, Petitioner cites to U.S. Patent No. 9,768,186 B2, issued Sept. 19, 2017 (“the ’186 patent,” Ex. 1012). Although the ’186 patent does describe pillar-shaped support members that include “any suitable electrically conductive material, such as a metal material . . . or a doped semiconductor material,” it does not discuss other materials that can be used as a support member, or their abilities to provide suitable support. Ex. 1012, 4:63–5:5. Furthermore, Dr. Kuhn testifies that “not all conductive (typically metal) cores have the required stiffness and/or support function to be considered a supporting material.” Ex. 2013 ¶ 144. In that regard, Dr. Kuhn explains that “Young’s modulus (the measure of how much a material will deform when a load is placed on it, or more simply the slope of a stress versus strain plot) is often used as a high-level metric for ‘collapse’ of these ‘pillar support’ materials.” *Id.* ¶ 145. Dr. Kuhn further explains that

there is no apparent correlation between electrical conductivity and Young’s modulus. There are some materials (such as indium) with very good conductivity and poor Young’s modulus (11 GPa), some materials (such as copper) with very good conductivity and moderate Young’s modulus (130 GPa), and some materials such as iridium with very good conductivity and excellent Young’s modulus (528 GPa).

*Id.* ¶ 148. Dr. Kuhn testifies that this “demonstrates both that conductivity cannot be taken as a predictor of Young’s modulus, and that conductivity is not an appropriate measure for determining materials suitable for structural support.” *Id.* (footnote omitted); *see also id.* ¶¶ 158–163. Thus, we are not

persuaded that the '186 patent supports Petitioner's contention that Kim's dummy structures provide inferior support.

Petitioner also contends that “[a] POSITA would have understood that using active conductive vias as supporting pillars in Kim would be advantageous because they enable a dual-role function: the pillar would provide both a support function and an interconnect function.” Pet. 88 (citing Ex. 1003 ¶ 217). As Dr. Kuhn notes, however, “Kim does not disclose any circuitry (either transistors or interconnects) under the memory array or the staircase” and, “[i]f there is no circuitry under the array or the staircase, there is no need to create connections to that circuitry.” Ex. 2013 ¶ 169; *see also id.* ¶ 167 (“Tessariol’s conductive vias are specific to its unique device and cannot be simply incorporated into Kim’s memory device without sufficient explanation and motivation for doing so.”). Petitioner and Dr. Banerjee do not sufficiently explain why a POSITA would have been motivated to incorporate active conductive vias as supporting pillars in Kim if Kim does not suggest a need for, or the desirability of, an interconnect function.

For these reasons and the reasons set forth in Section II.C.4 above, after considering Petitioner’s and Patent Owner’s positions, as well as their supporting evidence, we are not persuaded that Petitioner demonstrates that the combination of Kim and Tessariol teaches or suggests “the supporting pillar is filled with at least one of an insulating material and a pillar-support material surrounded by the insulating material” as required by claim 4. Accordingly, we determine that Petitioner does not show, by a preponderance of the evidence, that claim 4 would have been obvious over the combined teachings of Kim and Tessariol.

*F. Ground 4: Asserted Obviousness over Tessariol and Kim*

Petitioner contends that claims 1, 2, 4, and 5 would have been obvious over the combined teachings of Tessariol and Kim. Pet. 90–96. In the proposed combination, Petitioner relies on its arguments in Ground 2 that Tessariol discloses all of the limitations of these claims except for limitations [1.B], [1.F], and [1.H] of claim 1, which Petitioner contends Kim discloses. *Id.* at 90, 94–96. As set forth above in our analysis of Ground 2, we are not persuaded that Petitioner sufficiently demonstrates that Tessariol teaches or suggests limitation [1.D] (“a filling structure surrounding the multiple-stack staircase structure”). See § II.D.2, *supra*. Petitioner does not rely on Kim to remedy this deficiency in Tessariol. Pet. 90, 94–96. Accordingly, for the same reasons given above with respect to Petitioner’s challenge of claim 1 in Ground 2 (§ II.D.2, *supra*), we conclude that Petitioner does not demonstrate by a preponderance of the evidence that claim 1, and claims 2, 4, and 5 that depend, directly or indirectly therefrom, would have been obvious over the combined teachings of Tessariol and Kim.

### III. CONCLUSION<sup>4</sup>

After reviewing the record and weighing the evidence offered by both parties, we determine that Petitioner shows, by a preponderance of the

---

<sup>4</sup> Should Patent Owner wish to pursue amendment of the challenged claims in a reissue or reexamination proceeding subsequent to the issuance of this decision, we draw Patent Owner’s attention to the April 2019 *Notice Regarding Options for Amendments by Patent Owner Through Reissue or Reexamination During a Pending AIA Trial Proceeding*. See 84 Fed. Reg. 16,654 (Apr. 22, 2019). If Patent Owner chooses to file a reissue application or a request for reexamination of the challenged patent, we remind Patent Owner of its continuing obligation to notify the Board of any such related matters in updated mandatory notices. See 37 C.F.R. § 42.8(a)(3), (b)(2).

evidence, that claims 1–3 of the '031 patent are unpatentable, and does not show by a preponderance of the evidence that claims 4 and 5 of the '031 patent are unpatentable.

In summary:

| <b>Claims</b>              | <b>35<br/>U.S.C.<br/>§</b> | <b>Reference(s)/Basis</b> | <b>Claims<br/>Shown<br/>Unpatentable</b> | <b>Claims<br/>Not shown<br/>Unpatentable</b> |
|----------------------------|----------------------------|---------------------------|------------------------------------------|----------------------------------------------|
| 1–4                        | 103                        | Kim                       | 1–3                                      | 4                                            |
| 1, 2, 4, 5                 | 103                        | Tessariol                 |                                          | 1, 2, 4, 5                                   |
| 4                          | 103                        | Kim, Tessariol            |                                          | 4                                            |
| 1, 2, 4, 5                 | 103                        | Tessariol, Kim            |                                          | 1, 2, 4, 5                                   |
| <b>Overall<br/>Outcome</b> |                            |                           | 1–3                                      | 4, 5                                         |

#### IV. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that Petitioner has established by a preponderance of the evidence that claims 1–3 of the '031 patent are unpatentable;

FUTHER ORDERED that Petitioner has not established by a preponderance of the evidence that claims 4 and 5 of the '031 patent are unpatentable; and

FURTHER ORDERED that, because this is a Final Written Decision, parties to the proceeding seeking judicial review of the Decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

IPR2024-00790  
Patent 10,868,031 B2

For PETITIONER:

Jeremy Jason Lang  
K. Patrick Herman  
ORRICK, HERRINGTON & SUTCLIFFE LLP  
jlang@orrick.com  
pherman@orrick.com  
ptabdocketjl2@orrick.com

For PATENT OWNER:

Christopher M. Bonny  
Andrew T. Radsch  
Allen S. Cross  
ROPES & GRAY LLP  
Christopher.Bonny@ropesgray.com  
Andrew.Radsch@ropesgray.com  
Allen.Cross@ropesgray.com