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Invention Name: Through-array Contacts (TACs) for Three-Dimensional memory devices

Re-Examination
Requested by: Yangtze Memory Technologies Co., Ltd.

Re-Examination Protocol

(No. 283889)

☐ According to the comments of the aforementioned review decision, the rejection decision made by the State Intellectual Property Office on ____Month ____Day, ____Year is revoked, and the original review department shall continue the approval process.

☒ Maintain the rejection decision made by the National Intellectual Property Administration on July 21, 2,020.

☐ Upon review, the rejection decision made by the National Intellectual Property Administration on ____Month ____Day, ____Year is revoked.

In accordance with the provisions of Paragraph 2 of Article 41 of the Patent Law, if the re-examination requestor is dissatisfied with this decision, it may file a lawsuit with the Beijing Intellectual Property Court within 3 months from the date of receipt of this notice.

☒ Enclosed: Body Page of the Decision, 15 pages (body starts from Page 2).

Team Leader: Ling Yufei Lead Reviewer: Huang Lina, Reviewer: Li Yuan

Reexamination and Invalidation Department, the Patent Office



National Intellectual Property Administration

National Intellectual Property Administration

Decision of Reexamination Request (No. 283889)

Case number	No. 1F353287
Decision Day	November 25, 2021
Invention Name	Through-array Contacts (TACs) for Three-Dimensional Memory Devices
International classification number	H01L27/11565, H01L27/11573, H01L27/11578, H01L23/48
Reexamination Requestor	Applicant Yangtze Memory Technologies Co., Ltd.
Application No.	201880000655.5
Application Date	May 03, 2018
Public Day	December 21, 2018
Reexamination Request Date	September 27, 2020
Legal basis	Article 22, Paragraph 3 of the Patent Law
Key Points of the Decision: If the technical solution of a claim has a distinguishing technical feature compared to a Reference Document that is the closest to the prior art, and the distinguishing technical feature belongs to the common knowledge in the field, it is obvious that a person skilled in the art can obtain the distinguishing technical feature based on the Reference Document and the common knowledge in the field, then the claim does not involve creativity.	



I. Cause of Case

This re-examination request relates to the PCT invention patent application with application number 201880000655.5 and titled “Through Array Contacts (TAC) for Three-dimensional Memory Devices” (hereinafter referred to as “the application”). The applicant of the application is Yangtze Memory Technologies Co., Ltd., the application date is May 3, 2018, the date of entering the national phase is June 14, 2018, and the public date is December 21, 2018.

Upon substantial review, the Substantial Review Department of the National Intellectual Property Administration issued a rejection decision on July 21, 2020, and rejected the application on the ground that Claims 1-32 do not possess the creativity as specified in Article 22, Paragraph 3 of the Patent Law. The text on which the rejection decision is based is: Claims 1 to 32 submitted on July 6, 2020; Pages 1 to 27 of the Specification, which was modified in accordance with Article 28 or 41 of the PCT treaty; Pages 1 to 15 of the drawings attached to the Specification, the summary of the Specification and the drawings for the summary in the Chinese translation of the original application document submitted when entering the Chinese national phase on June 14, 2018.

The content of the claims to which the rejection decision is directed is as follows:

- “1. A three-dimensional (3D) memory device, comprising:
a semiconductor substrate;
an alternative stacked layer disposed on the semiconductor substrate;
a dielectric structure, which is on the isolation area of the semiconductor substrate and extends extending vertically through the alternative stacked layer, wherein the dielectric structure abuts a vertical sidewall surface of the alternative stacked layer and the dielectric structure is formed of a dielectric material;
at least two through-array contacts each extending perpendicularly through the dielectric structure and one of the isolation areas; and
one or more channel structures extending perpendicularly through the alternative stacked layer.
2. The three-dimensional (3D) memory device of Claim 1, further comprising:
an epitaxial layer formed between each of the one or more channel structures and the semiconductor substrate;
an etch stop plug disposed on each of the one or more channel structures;
a ladder structure disposed in the alternative stacked layer; and
one or more contact layers disposed on the at least two through-array contacts, the one or more channel structures, and the one or more crevice structures.
3. The three-dimensional (3D) memory device of Claim 1, wherein the dielectric structure abuts a sidewall surface of the at least two through-array contacts.
4. The three-dimensional (3D) memory device of Claim 1 or 2, wherein the 3D memory device is a NAND 3D memory device.
5. The three-dimensional (3D) memory device of Claim 1, wherein the alternative stacked layer comprise alternating pairs of dielectric layers and conductor layers.
6. The three-dimensional (3D) memory device of Claim 5, wherein the dielectric layer comprises silicon oxide and the conductor layer comprises metal.
7. The three-dimensional (3D) memory device of Claim 5, wherein the conductor layer comprises a word line.
8. The three-dimensional (3D) memory device of Claim 1 or 3, wherein the dielectric material is silicon oxide.



9. The three-dimensional (3D) memory device of Claim 1 or 3, wherein the dielectric structure comprises an oxide.

10. The three-dimensional (3D) memory device of Claim 1, wherein the dielectric structure defines a through-array contact area within the 3D memory device.

11. The three-dimensional (3D) memory device of Claim 1, wherein the dielectric structure has a footprint equal to or smaller than the isolation area.

12. A method for forming a 3D memory device, the method comprising:

shaping a isolation structure on a substrate;

providing an alternating dielectric stack layer on the substrate, the alternating dielectric stack layer comprising a first and second pair of dielectric layers, the second dielectric layer being different from the first dielectric layer [in the pair];

forming a channel structure extending vertically in the alternating dielectric stack layer;

forming an opening in the alternating dielectric stack layer, wherein the opening exposes the isolation structure;

filling the opening with a dielectric layer to form a dielectric structure as a through-array contact area of the 3D memory device;

removing portions of the dielectric structure and the isolation structure until the substrate is exposed to form through-array contact openings extending perpendicularly through the dielectric structure and the isolation structure; and

filling the through-array contact opening with a conductor to form a through-array contact structure in the through-array contact area, wherein the through-array contact structure contacts the substrate;

The method further comprises: forming an alternating conductor/dielectric stack layer based on an alternating dielectric stack layer;

wherein the dielectric structure abuts the vertical sidewall surface of the alternative stacked layer.

13. The method of Claim 12, wherein, prior to forming the through-array contact opening, the method further comprises:

forming a crevice opening extending vertically in the alternating dielectric stack layer, wherein the crevice opening exposes a doped area of the substrate;

replacing the second dielectric layer with a conductor layer through one or more crevice openings to convert the alternating dielectric stack layer to an alternating dielectric/conductor stack layer; and

filling the one or more crevice openings with conductors to form one or more crevice structures extending vertically in the alternating dielectric/conductor stack layer.

14. The method of Claim 12, wherein prior to forming the channel structure, a pruning etch process is performed to form a ladder structure in the alternating dielectric stack layer.

15. The method of Claim 12, wherein removing portions of the alternating dielectric stack layer comprises performing a dry etch process.

16. The method of Claim 12, wherein filling the opening with the dielectric layer comprises depositing the dielectric layer using a chemical vapor deposition, plasma-enhanced chemical vapor deposition, or physical vapor deposition process.

17. The method of Claim 12, wherein filling the opening with the dielectric layer comprises forming an oxide.



18. The method of Claim 12, wherein filling the opening with the dielectric layer comprises forming silicon oxide.
19. The method of Claim 12, wherein the first dielectric layer comprises an oxide and the second dielectric layer comprises a nitride.
20. The method of Claim 12, wherein the first dielectric layer comprises silicon oxide and the second dielectric layer comprises silicon nitride.
21. A method for forming a 3D memory device, the method comprising:
- providing an alternating dielectric stack layer on a substrate, wherein the alternating dielectric stack layer comprises a first and second pair of dielectric layers, the second dielectric layer being different from the first dielectric layer [in the pair];
 - forming a channel structure extending perpendicularly through the alternating dielectric layer;
 - etching the alternating dielectric stack layer to form an opening that exposes the isolation area in the substrate;
 - filling the opening with a dielectric layer to form a dielectric structure as a through-array contact area, wherein the through-array contact area is equal to or smaller than the isolation area;
 - etching through the dielectric structure and the isolation area to form a through-array contact opening exposing the substrate; and
 - filling the through-array contact opening with a conductor to form a through-array contact structure in the through-array contact area;
- The method further comprises: forming an alternating conductor/dielectric stack layer based on the alternating dielectric stack layer;
- The dielectric structure abuts the vertical sidewall surface of the alternative stacked layer.
22. The method of Claim 21, further comprising:
- forming a crevice opening extending perpendicularly through the alternating dielectric layer, wherein the crevice opening exposes a doped region of the substrate;
 - replacing the second dielectric layer with a conductor layer through the crevice opening to convert the alternating dielectric stack layer into an alternating dielectric/conductor stack layer;
 - filling the crevice opening with a conductor to form a crevice structure;
 - forming a ladder structure in the alternating dielectric stack layer, wherein the ladder structure comprises a hierarchy;
 - forming word line contacts on each of the levels of the ladder structure;
 - forming local contacts over the channel structure and the crevice structure; and
 - forming one or more contact layers over the local contacts, each word line, and each through-array contact structure.
23. The method of Claim 21, wherein the first dielectric layer comprises silicon oxide and the second dielectric layer comprises silicon nitride.
24. The method of Claim 21, wherein forming the opening in the alternating dielectric stack layer comprises performing a dry etch process.
25. The method of Claim 21, wherein the dielectric structure comprises silicon oxide.



26. The method of Claim 22, wherein the alternating dielectric/conductor stack layer abuts a sidewall of the dielectric structure.

27. The method of Claim 21, wherein the dielectric structure abuts a sidewall surface of each through-array contact structure.

28. A three-dimensional (3D) memory device, comprising:
a substrate having an isolation structure;
an alternating conductor/dielectric stack layer disposed on the substrate;
a dielectric structure on the isolation structure and extending vertically through the alternating conductor/dielectric stack layer, wherein the dielectric structure abuts a vertical sidewall surface of the alternating conductor/dielectric stack layer and the dielectric structure is formed of a dielectric material;
a channel structure extending vertically through the alternating conductor/dielectric stack layer; and
at least two through-array contacts each extending perpendicularly through the dielectric structure and one isolation structure in the isolation areas.

29. The three-dimensional (3D) memory device of Claim 28, further comprising:
a ladder structure disposed in the alternating conductor/dielectric stack layer, wherein the ladder structure comprises a hierarchy, having a conductor layer on each level;
a word line contact disposed on each conductor layer of the stepped structure; and
local contacts disposed on each channel structure and crevice structure.

30. The three-dimensional (3D) memory device of Claim 28, wherein the dielectric structure abuts the sidewall of each through-array contact.

31. The three-dimensional (3D) memory device of Claim 28, wherein the dielectric structure comprises a through-array contact area of the 3D memory device.

32. The three-dimensional (3D) memory device of Claim 28, further comprising:
an etch stop plug inserted between each local contact and each channel structure; and
an epitaxial layer disposed between each channel structure and the substrate.”

The rejection decision references the following comparison documents:

Reference Document 2: US2017179026A1, public date: June 22, 2017.

In the rejection decision, it was pointed out that: 1) Compared with the content disclosed in Reference Document 2, the technical solution requested for protection in Claim 1 distinguishes the following technical features: a dielectric structure on an isolation area of the semiconductor substrate, at least two through-array contacts extending perpendicularly through one of a plurality of isolation areas, wherein the isolation area is buried in the semiconductor substrate, and wherein a lower end of the through-array contact is formed in the isolation area and in contact with the semiconductor substrate. The above distinguishing technical characteristics belong to common knowledge in the art. Therefore, Claim 1 does not possess the creativity as specified in Paragraph 3 of Article 22 of the Patent Law. 2) The additional features of Claims 2-11 are disclosed by Reference Document 2, or belong to common knowledge in the art. Therefore, Claims 2-11 do not possess the creativity specified in Article 22, Paragraph 3 of the Patent Law. 3) Compared with the content disclosed in Reference Document 2, the technical solution requested for protection in Claim 12 distinguishes the following technical features: the opening exposing the isolation structure, removing portions of the isolation structure until the substrate is exposed to form a through-array contact opening extending perpendicularly through the dielectric structure and the isolation structure, the through-array contact structure contacting the substrate; wherein the isolation area is buried in the semiconductor substrate, and wherein a lower end of the through-array contact is formed in the isolation area and in contact with the semiconductor substrate. The above distinguishing technical characteristics belong to common knowledge in the art. Therefore, Claim 12 does not possess the creativity as specified in Article 22, Paragraph 3 of the Patent Law. 4) The additional features of Claims 13-20 are disclosed by Reference Document 2, or belong to common knowledge in the art. Therefore, Claims 13-20 do not possess creativity as prescribed in Article 22, Paragraph 3 of the Patent Law. 5) Compared with the content disclosed in Reference



Document 2, the technical solution requested for protection of Claim 21 distinguishes the following technical characteristics: the opening exposing the isolation structure, the through-array contact area being equal to or smaller than the isolation area, etching through the isolation area to form a through-array contact opening exposing the substrate; wherein the isolation area is buried in the semiconductor substrate, and wherein a lower end of the through-array contact is formed in the isolation area and in contact with the semiconductor substrate. The above distinguishing technical characteristics belong to common knowledge in the art. Therefore, Claim 21 does not possess creativity as prescribed in Article 22, Paragraph 3 of the Patent Law. 6) The additional features of Claims 22-27 are disclosed in Reference Document 2. Therefore, Claims 22-27 do not possess the creativity as specified in Article 22, Paragraph 3 of the Patent Law. 7) Compared with the content disclosed in Reference Document 2, the technical solution claimed in Claim 28 is distinguished by: a dielectric structure on an isolation area of the semiconductor substrate, at least two through-array contacts extending perpendicularly through one of a plurality of isolation areas; wherein the isolation area is buried in the semiconductor substrate, and wherein a lower end of the through-array contacts is formed in the isolation area and in contact with the semiconductor substrate. The above distinguishing technical characteristics belong to common knowledge in the art. Therefore, Claim 28 does not possess creativity as prescribed in Article 22, Paragraph 3 of the Patent Law. 8) The additional features of Claims 29-32 are disclosed by Reference Document 2, or belong to common knowledge in the art. Therefore, Claims 29-32 do not possess creativity as prescribed in Article 22, Paragraph 3 of the Patent Law.

The Applicant (hereinafter referred to as the re-examination requestor) is dissatisfied with the aforementioned rejection decision. On September 27, 2020, it submitted a request for re-examination to the National Intellectual Property Administration, and did not amend the application document. The re-examination requestor believes that: Reference Document 2 does not disclose the feature of “the dielectric structure abuts a vertical sidewall surface of the alternative stacked layer,” and the dielectric structure 430 in Reference Document 2 abuts a ladder structure of the alternative stacked layer rather than a vertical sidewall surface of the alternative stacked layer. Therefore, Claims 1-32 of the Present Application involves creativity.

After passing the formality review, the National Intellectual Property Administration accepted the re-examination request in accordance with the law on October 12, 2020, and forwarded it to the substantive review department for pre-examination.

The substantive review department maintained the rejection decision in the pre-review opinion.

Subsequently, the National Intellectual Property Administration established a panel to hear this case.

On April 22, 2021, the panel issued a re-examination notice to the requestor, stating that: (1) The combination of Claims 1 to 32 with respect to Reference Document 2 and common knowledge in the art does not possess the creativity as specified in Paragraph 3 of Article 22 of the Patent Law; (2) Regarding the re-examination request made by the re-examination requestor, the panel believed that: FIG. 17E of Reference Document 2 clearly discloses that the through-hole area 400 of the through-memory hierarchy can be disposed immediately adjacent to the memory array area 100. The alternative stacked layers 132/146 and 232/246 are located in the memory array area 100 and the dielectric structure 430 is located in the through-hole area 400 of the through-memory hierarchy. As the through-hole structure 488 of the through-memory hierarchy extends perpendicularly through the dielectric structure 430 and is electrically connected with the peripheral device of the lower layer, the formation of a vertical interconnection between the memory array device and peripheral device in the storage series adjoining region can be achieved. On the basis of the above technical content disclosed in Reference Document 2, the opening is etched at the location abutting the alternative stacked layer, so that the dielectric structure abuts the vertical sidewall surface of the alternative stacked layer, which is easy to think of and can be achieved by those skilled in the art. This is only a conventional technical means in the art and does not require creative work.

The Reexamination Requestor submitted the Statement of Opinion on June 4, 2021 and did not amend the application documents. The re-examination requestor believes that: (1) Reference Document 2 sets the dielectric structure in the step area, occupying the position of the word line contacts, making adjusting the position of the word line contacts very difficult, resulting in wasted storage unit and more complex read and write circuit design. The present



application moves the dielectric structure to a certain position. Although the position of the NAND string contacts and the crevice structure contacts is still extruded, it allows greater freedom for adjusting the position of these contacts. The technical problems existing in Reference Document 2 and the technical means for solving the technical problems are first discovered by the re-examination requestor and are not common knowledge in the art. (2)Reference Document 2 does not disclose the feature of “dielectric structure on an isolation area of the semiconductor substrate and extends vertically through the alternative stacked layer”, the portion in contact with the TAC in Reference Document 2 is a contact in the interconnected metal layer, the TAC structure having no relationship with the substrate. The present application omits the interconnected metal layer, reduces structural complexity, simplifies the process, reduces cost, and improves good yield.

On July 30, 2021, the panel issued a notice of change of members of the panel to the re-examination requestor. If the re-examination requestor fails to reply within the time limit, it shall be deemed that there is no request for avoidance.

On the basis of the above procedures, the panel believes that the facts of this case have been clear and a review decision can be made in accordance with the law.

II. Reason for decision

1. Identification of documents

The re-examination requestor did not modify the application documents when making the re-examination request and replying to the re-examination notice. The documents on which this re-examination request is based is the same as the documents on which the rejection decision and the re-examination notice are addressed, i.e.: Claims 1 to 32 submitted on July 6, 2020; Pages 1 to 27 of the Specification, which was modified in accordance with Article 28 or 41 of the PCT treaty; Pages 1 to 15 of the drawings attached to the Specification, the summary of the Specification and the drawings for the summary in the Chinese translation of the original application document submitted when entering the Chinese national phase on June 14, 2018..

2. Regarding Article 22, Paragraph 3 of the Patent Law

Article 22, Paragraph 3 of the Patent Law stipulates that: Creativity means that the invention has prominent substantive features and significant advancements compared to the prior art, and the utility model has substantive features and advancements.

If the technical solution of a claim has a distinguishing technical feature compared to a Reference Document that is the closest to the prior art, and the distinguishing technical feature belongs to the common knowledge in the field, it is obvious that a person skilled in the art can obtain the distinguishing technical feature based on the Reference Document and the common knowledge in the field, then the claim does not involve creativity.

The Reference Documents cited by the decision for this re-examination request are the same as the Reference Documents used by the rejection decision and the re-examination notice, i.e.:

Reference Document 2: US2017179026A1, public date: June 22, 2017.

2.1. Claim 1 requests protection of a three-dimensional (3D) memory device. Reference Document 2 discloses a three-dimensional memory device comprising the following technical features (see Paragraphs [0162]-[0389] of the Specification, Figs. 1A-76): Refer to Paragraphs [0162]-[0260] of the Specification and Figs. 1A-17F for details, and the three-dimensional memory device comprises: substrate semiconductor layer 10 (equivalent to a semiconductor substrate); alternative stacked layers 132/146 and 232/246 disposed on the substrate semiconductor layer 10; dielectric structure 430, which is disposed on the isolation area of the substrate semiconductor layer 10 (the removed portion of the substrate semiconductor layer 10 is filled with dielectric material, which is equivalent to the isolation area of the substrate) and extends perpendicularly through the alternative stacked layers, and the dielectric structure 430 is formed of a dielectric material; Referring to FIG. 17E, the through-hole 400 of the through-memory hierarchy is disposed immediately adjacent to the memory array area 100, the dielectric structure 430 is located in each through-hole 400 of the through-memory hierarchy, and alternative stacked layers 132/146 and 232/246 are located in each memory array area 100; at least two through-hole structure 488 of the through-memory hierarchy (equivalent to through-array contacts), each of the at least two through-hole structure 488 of the through-memory hierarchy extends perpendicularly

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04/2019 In the case of an electronic application, the relevant documents shall be submitted electronically through the electronic patent application system. Unless otherwise specified, documents submitted in other forms such as paper forms are considered not submitted.



through the dielectric structure 430 and a plurality of isolation areas (see Figs 11A-12B and relevant paragraphs of the Specification, each through-hole 400 of the through-memory hierarchy is etched to form an opening 769 and filled with dielectric material, forming one of the multiple isolation areas correspondingly; one or more memory stack structure 55 (corresponding to a channel structure), which extends perpendicularly through the alternative stacked layer.

Compared with the content disclosed in Reference Document 2, the technical solution claimed in Claim 1 is distinguished by: The dielectric structure abuts the vertical sidewall surface of the alternative stacked layer. Based on the aforementioned distinguishing technical features, the technical problem actually solved by Claim 1 is: How to form a vertical interconnection between the storage array device and peripheral device in storage series adjoining region. However, Fig. 17E of Reference Document 2 has clearly disclosed that the through-hole region 400 of the through memory hierarchy may be disposed immediately adjacent to the memory array region 100, the dielectric structure 430 is located in the through-hole region 400 of the through memory hierarchy, and the alternative stacked layers 132/146 and 232/246 are located in the memory array region 100, thereby enabling the formation of a vertical interconnection between the storage array device and peripheral device in the storage series adjoining region. On the basis of the above technical content disclosed in Reference Document 2, the opening is etched at the location abutting the alternative stacked layer, so that the dielectric structure abuts the vertical sidewall surface of the alternative stacked layer, which is easy to arrive and achieved by those skilled in the art, and is a conventional technical means in the art.

Therefore, it is obvious to those skilled in the art that the technical solution claimed by Claim 1 is obtained based on Reference Document 2 in combination with conventional means in the art. Claim 1 does not have prominent substantive features and does not possess creativity as prescribed in Article 22, Paragraph 3 of the Patent Law.

2.2. Claims 2-11 directly or indirectly further define Claim 1. Reference Document 2 also specifically discloses the following technical features (see Paragraphs [0162]-[0260] of the Specification and Figures 1A-17F):

1) For Claim 2, Reference Document 2 discloses a base channel portion 11 (equivalent to an epitaxial layer) formed between each of the one or more memory stack structures 55 and the substrate semiconductor layer 10; a polysilicon drain region 63 (equivalent to an etch stop plug) disposed on each of the one or more memory stack structures 55; a ladder structure disposed in the alternative stacked layer; and one or more contact layers 108, 103, 101 disposed on the at least two through-hole structures 488 of the through memory hierarchy, the one or more memory stack structures 55, and one or more contact through-hole structures 76 (equivalent to a gap structure);

2) For Claim 3, Reference Document 2 discloses that the dielectric structure 430 abuts the sidewall surfaces of the at least two through-hole structures 488 of the through-memory hierarchy;

3) For Claim 4, Reference Document 2 discloses that the three-dimensional memory device is a three-dimensional NAND memory device;



4) For Claims 5-7, Reference Document 2 discloses alternative stacked layers include dielectric layers 132, 232 and conductor layers 146, 246; the dielectric layer including silicon oxide, the conductor layer including metal; and the conductor layer including wordlines.

5) For Claims 8-9, Reference Document 2 discloses that the dielectric material is silicon oxide, and the dielectric structure 430 includes oxide;

6) For Claim 10, Reference Document 2 discloses that the dielectric structure 430 defines a through-array contact area within the three-dimensional memory device;

7) For Claim 11, Reference Document 2 discloses that the dielectric structure 430 is equal to the footprint of the isolation area. Furthermore, forming the dielectric structure into a footprint smaller than the isolation area is a conventional technical means in the art.

Therefore, where the claims referenced do not possess creativity, Claims 2-11 do not possess creativity as prescribed in Article 22, Paragraph 3 of the Patent Law either.

2.3. Claim 12 requests protection for a method of forming a 3D memory device. Reference Document 2 discloses a method for forming a three-dimensional memory device comprising the following technical features (see paragraphs [0162]-[0389] of the Specification, Figs. 1A-76): Refer to Paragraphs [0162]-[0260] of the Specification and Figs. 1A-17F for details, and the method comprises: Alternating dielectric stack layers are provided on the substrate semiconductor layer 10 (equivalent to the substrate). The alternating dielectric stack layer includes the first and second pair of dielectric layers 132/142 and 232/242, in which the second dielectric layer 142 and 242 are different from the first dielectric layer 132 and 232; a memory stack structure 55 (equivalent to a channel structure) extending perpendicularly in the alternating dielectric stack layers is formed; Opening 769 is formed in the alternating dielectric stack layers, passing through the substrate semiconductor layer 10; the opening 769 is filled with dielectric layers to form dielectric structure 430 as through-array contact area of the three-dimensional memory device; remove a portion of the dielectric structure 430 until it penetrates the substrate semiconductor layer 10 to form a through-array contact opening extending perpendicularly through the dielectric structure 430; fill the through-array contact opening with a conductor to form a through-hole structure 488 of the through memory hierarchy (equivalent to a through array contact structure) in the through array contact area. The through-hole structure 488 of the through memory hierarchy penetrates the substrate semiconductor layer 10 and contacts the underlying peripheral component; the method also include: Alternating conductor/dielectric stack layers 146/132, 246/232 are formed based on alternating dielectric stack layers; referring to FIG. 17E, through-hole region 400 of the through memory hierarchy is disposed adjacent to memory array region 100, dielectric structures 430 is located in each through-hole region 400 of the through memory hierarchy, and alternating stack layers are located in each memory array region 100.

Compared with the content disclosed in Reference Document 2, the technical solution claimed in Claim 12 is distinguished by: (1) forming a partition structure on the substrate, opening to expose the partition structure; removing a portion of the partition structure to expose the substrate, the through array contact opening extends through the partition structure so that the through array contact structure is in contact with the substrate; and (2) the dielectric structure abutting a vertical sidewall surface of the alternative stacked layer. Based on the aforementioned distinguishing technical features (1) and (2), the technical problem actually solved by Claim 12 is: How to realize device isolation on the substrate and how to form a vertical interconnection between the storage array device and peripheral device in storage series adjoining region. However, for distinguishing technical feature (1), Reference Document 2 is a monolithic three-dimensional memory device that forms a storage array directly on the peripheral device wafer, so the through-array contact structure contacts the underlying peripheral device through the substrate semiconductor layer 10, thereby enabling vertical interconnection between the storage array device and the peripheral device. For another conventional memory device structure, which is a non-monolithic three-dimensional memory device (storage array device and peripheral device are independently manufactured on different substrates, and then both are bonded), in order to achieve device isolation on the substrate of the storage array device, an isolation structure is first formed on the substrate, followed by forming a through-array contact structure on the opening above the



isolation structure, and the through-array contact structure extends through the isolation structure and contacts the substrate, which is a conventional technical means in the art without creative work. For distinguishing technical features (2), the Fig.17E of Reference Document 2 has clearly disclosed that the through-hole region 400 of the through memory hierarchy may be provided immediately adjacent to the memory array region 100, the dielectric structure 430 is located in the through-hole region 400 of the through memory hierarchy, and the alternating stacking layers 132/146 and 232/246 are located in the memory array region 100, thereby enabling the formation of vertical interconnections between the storage array device and peripheral device in the storage series adjoining region. On the basis of the above technical content disclosed in Reference Document 2, the opening is etched at the location abutting the alternative stacked layer, so that the dielectric structure abuts the vertical sidewall surface of the alternative stacked layer, which is easy to arrive and can be achieved by those skilled in the art, and is also a conventional technical means in the art.

Therefore, it is obvious to those skilled in the art to obtain the technical solution claimed by Claim 12 based on Reference Document 2 in combination with conventional means in the art. Claim 12 does not have prominent substantive features and does not possess creativity as prescribed in Article 22, Paragraph 3 of the Patent Law.

2.4. Claims 13-20 further define Claim 12, respectively. Reference Document 2 also specifically discloses the following technical features (see Paragraphs [0162]-[0260] of the Specification and Figures 1A-17F):

1) For Claim 13, Reference Document 2 discloses that before forming the through-array contact opening, the method further comprises: forming a rear side contact channel 79 (equivalent to a crevice opening) extending vertically in the alternating dielectric stack layers 132/142, 232/242, the rear side contact channel 79 exposing a doped region 61 of the substrate semiconductor layer 10; replacing the second dielectric layer 142 and 242 with a conductor layer through the one or more rear side contact channels 79 to convert the alternating dielectric stack layers 132/142 and 232/242 into alternating dielectric/conductor stack layers 132/146 and 232/246; filling the one or more rear side contact channels 79 with a conductor to form one or more contact through-hole structures 76 (equivalent to crevice structures) extending vertically in the alternating dielectric/conductor stack layers 132/146 and 232/246;

2) For Claim 14, Reference Document 2 discloses that prior to forming the memory stack structure 55, a pruning and etching process is performed to form a ladder structure in the alternating dielectric stack layers 132/142, 232/242 (see Figure 3 and related paragraphs of the Specification);

3) For Claim 15, Reference Document 2 discloses portions of alternating dielectric stack layers 132/142, 232/242 removed by anisotropic etching. In addition, dry etching process is a conventional technical means in the art;

4) For Claim 16, Reference Document 2 discloses that filling the opening 769 with a dielectric layer comprises depositing the dielectric layer by conformal deposition, non-conformal deposition in combination with a backflow material, or spin coating, etc. In addition, chemical vapor deposition, plasma-enhanced chemical vapor deposition, or physical vapor deposition processes are conventional technical means in the art;

5) For Claims 17-18, Reference Document 2 discloses that filling the opening 769 with a dielectric layer comprises forming silicon oxide;

6) For claims 19-20, Reference Document 2 discloses that the first dielectric layer 132, 232 includes silicon oxide and the second dielectric layer 142, 242 includes silicon nitride.

Therefore, where the claims referenced do not possess creativity, claims 13-20 do not possess creativity as prescribed in Article 22, Paragraph 3 of the Patent Law either.

2.5. Claim 21 requests protection for a method of forming a 3D memory device. Reference Document 2 discloses a method for forming a three-dimensional memory device comprising the following technical features (see paragraphs



[0162]-[0389] of the Specification, Figures 1A-76): Refer to Paragraphs [0162]-[0260] of the Specification and Figs. 1A-17F for details, and the method comprises: Alternating dielectric stack layers are provided on the substrate semiconductor layer 10 (equivalent to the substrate). The alternating dielectric stack layers include a first and second dielectric layer pair 132/142 and 232/242. The second dielectric layer 142 and 242 are different from the first dielectric layer 132 and 232; forming a memory stack structure 55 (equivalent to a channel structure) extending perpendicularly through the alternating dielectric stack layers; etching the alternating dielectric stack layer to form openings 769, which penetrate the substrate semiconductor layer 10; opening 769 is filled with a dielectric layer to form a dielectric structure 430 as a through-array contact area of the three-dimensional memory device; the portion passing through the dielectric structure 430 is etched to form a through-array contact opening that passes through the substrate semiconductor layer 10; fill the through-array contact opening with a conductor to form a through-hole structure 488 (equivalent to a through-array contact structure) of the through-memory hierarchy in the through-array contact area; the method further includes: Alternating conductor/dielectric stack layers 146/132 and 246/232 are formed based on alternating dielectric stack layers; referring to FIG. 17E, through-hole region 400 of the through-memory hierarchy is disposed adjacent to memory array region 100, dielectric structure 430 is located in each through-hole region 400 of the through-memory hierarchy, and alternating stack layers are located in each memory array region 100.

Compared with the content disclosed in Reference Document 2, the technical solution claimed in Claim 21 is characterized by: (1) the opening exposes a isolation area in the substrate, and the through array contact opening passes through the isolation area and exposes the substrate; the through array contact area is equal to or smaller than the isolation area; and (2) the dielectric structure abuts a vertical sidewall surface of the alternative stacked layer. Based on the aforementioned distinguishing technical features (1) and (2), the technical problem actually solved by Claim 21 is: How to realize device isolation on the substrate and how to form a vertical interconnection between the storage array device and peripheral device in the storage series adjoining region. However, for distinguishing technical feature (1), Reference Document 2 is a monolithic three-dimensional memory device that forms a storage array directly on the peripheral device wafer, so the through-array contact structure contacts the underlying peripheral device through the substrate semiconductor layer 10, thereby enabling vertical interconnection between the storage array device and the peripheral device. For another conventional memory device structure, which is a non-monolithic three-dimensional memory device (storage array device and peripheral device are independently manufactured on different substrates, and then both are bonded), in order to achieve device isolation on the substrate of the storage array device, an isolation structure is first formed on the substrate, followed by forming a through-array contact structure on the opening above the isolation structure, and the through-array contact structure extends through the isolation structure and contacts the substrate, which is a conventional technical means in the art without creative work. As for making the through-array contact area equal to or smaller than the isolation area, this is a common technical method in the art. For distinguishing technical features (2), Fig. 17E of Reference Document 2 has clearly disclosed that the through-hole region 400 of the through memory hierarchy may be provided immediately adjacent to the memory array region 100, the dielectric structure 430 is located in the through-hole region 400 of the through memory hierarchy, and the alternating stacking layers 132/146 and 232/246 are located in the memory array region 100, thereby enabling the formation of vertical interconnection between the storage array device and peripheral device in the storage series adjoining region. On the basis of the above technical content disclosed in Reference Document 2, the opening is etched at the location abutting the alternative stacked layer, so that the dielectric structure abuts the vertical sidewall surface of the alternative stacked layer, which is easily conceivable and can be achieved by those skilled in the art, and is also a conventional technical means in the art.

Therefore, it is obvious to those skilled in the art that the technical solution claimed by Claim 21 is obtained based on Reference Document 2 in combination with conventional means in the art. Claim 21 does not have prominent substantive features and does not possess creativity as prescribed in Article 22, Paragraph 3 of the Patent Law.

2.6. Claims 22-27 directly or indirectly further define Claim 21. Reference Document 2 also specifically discloses the following technical features (see Paragraphs [0162]-[0260] of the Specification and Figures 1A-17F):



1) For Claim 22, Reference Document 2 discloses how to form a backside contact channel 79 (equivalent to a crevice opening) vertically extending through the alternating dielectric stack layers 132/142, 232/242, the backside contact channel 79 exposing the doped area 61 of the substrate semiconductor layer 10; replacing the second dielectric layer 142, 242 with a conductor layer through the backside contact channel 79 to convert the alternating dielectric stack layers 132/142, 232/242 into alternating dielectric/conductor layer 132/146 and 232/246; The backside contact trench 79 is filled with a conductor to form a contact through-hole structure 76 (equivalent to a crevice structure); a ladder structure is formed in the alternating dielectric stack layers 132/142, 232/242, and the ladder structure includes levels; a word line contact through hole structure 86 (equivalent to a word line contact) is formed on each level of the ladder structure; a drain contact through-hole structure 88 and a source through-hole structure 91 (equivalent to a local contacts) are formed on the memory stack structure 55 and the contact through-hole structure 76; one or more contact layers 108, 103, 101 are formed on the drain contact through-hole structure 88, source through-hole structure 91, each word line contact through-hole structure 86 (i.e., each word line) and each through-hole structure 488 of the through memory hierarchy;

2) For Claim 23, Reference Document 2 discloses that the first dielectric layers 132 and 232 comprises silicon oxide and the second dielectric layers 142 and 242 comprise silicon nitride;

3) For Claim 24, Reference Document 2 discloses the formation of an opening 769 in alternating dielectric stack layers 132/142 and 232/242 by anisotropic etching. In addition, dry etching process is a conventional technical means in the art;

4) For Claim 25, Reference Document 2 discloses that dielectric structure 430 includes silicon oxide;

5) For Claim 26, Reference Document 2 discloses that the through-hole region 400 of the through memory hierarchy may be disposed immediately adjacent to the memory array region 100 (Fig. 17E), the dielectric structure 430 is located in the through-hole region 400 of the through memory hierarchy, and the alternating stacking layers 132/146 and 232/246 are located in the memory array region 100, thereby enabling the formation of a vertical interconnection between the storage array device and peripheral device in the storage series adjoining region. Based on the above technical content disclosed in Reference Document 2, an opening is etched at the position abutting the alternative stacked layer, so that the alternative stacked layer abuts a sidewall of the dielectric structure, which is easily conceivable and can be achieved by those skilled in the art and is a conventional technical means in the art;

6) For Claim 27, Reference Document 2 discloses that the dielectric structure 430 abuts a sidewall surface of each through-hole structure 488 of the through-memory hierarchy.

Therefore, where the claims referenced do not possess creativity, Claims 22-27 do not possess creativity as prescribed in Article 22, Paragraph 3 of the Patent Law either.

2.7. Claim 28 requests protection of a three-dimensional (3D) memory device. Reference Document 2 discloses a three-dimensional memory component comprising the following technical features (see Paragraphs [0162]-[0389] of the Specification, Figs. 1A-76): Refer to Paragraphs [0162]-[0260] of the Specification and Figs. 1A-17F for details, and the three-dimensional memory component comprises: a substrate semiconductor layer 10 (equivalent to a semiconductor substrate), having a barrier structure (the portion of the substrate semiconductor layer 10 being removed is filled with dielectric material, the portion is equivalent to a isolation structure of the substrate); alternating conductor/dielectric stack layers 146/132 disposed on the substrate semiconductor layer 10, 246/232 ; a dielectric structure 430, on the isolation structure of the substrate semiconductor layer 10 and extending vertically through the alternating conductor/dielectric stack layer 146/132, 246/232, the dielectric structure 430 is formed from a dielectric



material; Referring to Fig. 17E, the through-hole region 400 of the through memory hierarchy is disposed adjacent to the memory array region 100, the dielectric structure 430 is located in each through-hole region 400 of the through memory hierarchy, while the alternating conductor/dielectric stack layers 146/132 and 246/232 are located in each memory array region 100; a memory stack structure 55 (equivalent to a channel structure) extends perpendicularly through the alternating conductor/dielectric stack layer 146/132 and 246/232 ; at least two through-hole structures 488 (equivalent to through array contacts) of the through memory hierarchy; the at least two through-hole structures 488 of the through memory hierarchy extend perpendicularly through the dielectric structure 430 and one of a plurality of isolation areas (see Figures 11A-12B and related paragraphs of the Specification; opening 769 is etched and the dielectric material is filled in each through-hole region 400 of the through memory hierarchy, thus correspondingly forming one of a plurality of isolation areas).

Compared with the content disclosed in Reference Document 2, the technical solution claimed by Claim 28 distinguishes the following technical features: The dielectric structure abuts the vertical sidewall surface of the alternative stacked layer. Based on the aforementioned distinguishing technical features, the technical problem actually solved by Claim 28 is: How to form a vertical interconnection between the storage array device and peripheral device in storage series adjoining region. However, Fig. 17E of Reference Document 2 has clearly disclosed that the through-hole region 400 of the through memory hierarchy may be disposed immediately adjacent to the memory array region 100, the dielectric structure 430 is located in the through-hole region 400 of the through memory hierarchy, and the alternating stack layers 132/146 and 232/246 are located in the memory array region 100, thereby enabling the formation of a vertical interconnection between the storage array device and peripheral device in the storage series adjoining region. On the basis of the above technical content disclosed in Reference Document 2, the opening is etched at the location abutting the alternative stacked layer, so that the dielectric structure abuts the vertical side wall surface of the alternative stacked layer, which is easy to think of and can be achieved by those skilled in the art, and is a conventional technical means in the art.

Therefore, it is obvious to those skilled in the art to obtain the technical solution claimed by Claim 28 based on Reference Document 2 in combination with conventional means in the art. Claim 28 does not have prominent substantive features and does not possess creativity as prescribed in Article 22, Paragraph 3 of the Patent Law either.

2.8. Claims 29-32 further define Claim 28, respectively. Reference Document 2 also specifically discloses the following technical features (see Paragraphs [0162]-[0260] of the Specification and Figures 1A-17F):

1) For Claim 29, Reference Document 2 discloses a ladder structure disposed in said alternating conductor/dielectric stack layers 146/132 and 246/232, said ladder structure comprising levels; conductor layers 146, 246 are formed on each level; a word line contact through-hole structure 86 (equivalent to a word contact) disposed on each conductor layer of said ladder structure; a drain contact through-hole structure 88, a source through-hole structure 91 (equivalent to a local contact) disposed on each memory stack structure 55 (equivalent to a channel structure) and a contact through-hole structure 76 (equivalent to a crevice structure);

2) For Claim 30, Reference Document 2 discloses that the dielectric structure 430 abuts the sidewall of each through-hole structure 488 in the through memory hierarchy;

3) For Claim 31, Reference Document 2 discloses that the dielectric structure 430 includes a through-array contact area of the three-dimensional memory device;

4) For Claim 32, Reference Document 2 discloses a polysilicon drain region 63 (equivalent to an etch stop plug) inserted between each drain contact through-hole structure 88 and each memory stack structure 55; a base channel portion 11 (equivalent to an epitaxial layer) disposed between each memory stack structure 55 and the substrate semiconductor layer 10.

Therefore, where the claims referenced do not have creativity, Claims 29-32 do not have creativity prescribed in Article 22, Paragraph 3 of the Patent Law either.



3. Comments on the opinions of the Re-examination Requestor

With regard to the opinions stated by the requestor in replying to the re-examination notice, the panel believes that: For (1), first, the claims of the application define “vertical sidewall surfaces in which the dielectric structure abuts the alternative stacked layer”, which can reflect neither the positional relationship between the dielectric structure and the ladder structure, nor the positional relationship between the dielectric structure and the memory array area. Secondly, Figs. 17E and 17F of Reference Document 2 show that the through-hole region 400 of the through memory hierarchy is disposed adjacent to the memory array region 100, the dielectric structure 430 is located in each through-hole region 400 of the through memory hierarchy, and the alternating stacking layers 132/146 and 232/246 are located in each memory array region 100. The through-hole structure 488 of the through memory hierarchy extends perpendicularly through the dielectric structure 430 and is electrically connected with the peripheral device of the lower layer, thereby enabling the formation of a vertical interconnection between the storage array device and peripheral device in the storage series adjoining region. Based on the above technical content disclosed in Reference Document 2, when the opening is etched in the area 400 adjoining the alternative stacked layer to form the dielectric structure 430, such that the dielectric structure adjoins the vertical side wall surface of the alternative stacked layer, which is easy to think of and can be achieved by those skilled in the art, which is only a conventional technical means in the art and does not require creative labor. For (2), referring to FIGS. 1A-17F, the alternative stacked layers 132/146 and 232/246 in Reference Document 2 are grown on the semiconductor layer 10, the semiconductor layer 10 may be considered a growth substrate or a growth substrate layer, equivalent to the semiconductor substrate in the present application. The portion of the semiconductor layer 10 corresponding to the through-hole region 400 of the through-memory hierarchy is removed and filled with dielectric material, and this portion is equivalent to an isolation area of the substrate. The dielectric structure 430 is on the isolation area of semiconductor layer 10 and extends vertically through the alternating stacked layers.. Accordingly, Reference Document 2 has disclosed the “isolation area of the semiconductor substrate” and the “isolation structure” in claims 1-11 and 28-32 of the present application, as well as the characteristic “dielectric structure, which is in the isolation area of the semiconductor substrate” and extends vertically through the alternating stacked layers”. As for “the parts in contact with the TAC in Reference Document 2 are contacts in the interconnection metal layer, and the TAC structure has no relationship with the substrate”, the present application involves independently making memory array device and peripheral device on different substrates, and then bonding the two non-monolithic three-dimensional memory devices to provide vertical interconnection between the memory array device and peripheral device. Reference Document 2 involves a monolithic three-dimensional memory device that forms a storage array directly on the peripheral device wafer, and the TAC penetrates the semiconductor layer 10 to make contact with the peripheral device in the lower layer, and can also realize vertical interconnection between the memory array device and the peripheral device.

In summary, the re-examination requestor’s statement of opinion is not persuasive and will not be accepted by the panel.

Based on the above facts and reasons, the panel of this case made the following review decision in accordance with the law.

III. Decision

The rejection decision of the National Intellectual Property Administration on July 21, 2020 is maintained.

If the review decision of the re-examination request is dissatisfactory, the re-examination requestor may file a petition with the Beijing Intellectual Property Court within three months from the date of receipt of the review decision for this re-examination request in accordance with the provisions of Article 41, Paragraph 2 of the Patent Law.

Team Leader: Ling Yufei

Lead Reviewer: Huang Lina



Reviewer: Li Yuan

Reexamination and Invalidation Department, the Patent Office

200912 paper application, please send a reply to: Re-Examination and Invalidation Department, the Patent Office of the National Intellectual Property Administration, No. 6 West Tucheng Road, Jimenqiao, Haidian District, Beijing 100088

04/2019 In the case of an electronic application, the relevant documents shall be submitted electronically through the electronic patent application system. Unless otherwise specified, documents submitted in other forms such as paper shall be deemed not submitted.



March 25, 2024

Certification

Translator's Declaration:

I, Meihua Shi, hereby declare:

That I possess advanced knowledge of the Chinese and English languages.

My qualifications are as follows: I have obtained master's degree from both China and United States and have been translating documents for over 20 years. I am competent to translate from Simplified Chinese to English.

The attached Chinese into English translation has been translated by me and to the best of my knowledge and belief, it is a true and accurate translation of:

CN109075169A, Reexamination Decision dated November 25, 2021

I understand that willful false statement and link are punishable by fine or imprisonment, or both (18 U.S.C. 1001) and may jeopardize the validity of the application or any patent issuing thereon. I declare under the penalty of the perjury that all statements made herein of my own knowledge are true and all statements made on information and belief are believed to be true.

Meihua Shi

Meihua Shi

Sworn to before me this
March 25, 2024

WPO

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