

BALL GRID ARRAY TECHNOLOGY

Edited by
JOHN H. LAU

Electronics

As the trend toward higher input/output, higher performance, and higher board-manufacturing yield continues, Ball Grid Array (BGA) becomes the package of choice. This book is a one-stop guide to state-of-the-art BGA technology. For professionals active in BGA research and development, those who wish to master BGA problem-solving methods, and those who must choose a cost-effective design and high-yield manufacturing process for their interconnect systems, here is a timely summary of progress in all aspects of this fascinating field. It meets the reference needs of design, material, process, equipment, manufacturing, quality control, product assurance, reliability, component, packaging, vendor, marketing, and system engineers, and technical managers working in electronic packaging and interconnection.

This book offers contributions from a wide array of experts who address areas covering the most advanced research and solutions in BGA today. With this volume you will develop a practical understanding of the economic, design, material, process, equipment, quality, and reliability issues of BGA. Among other aspects of this diverse field, you will find covered:

- Design, materials, and processing of substrates for CBGA, PBGA, and TBGA packages. Also, the routing of PCB for BGA packages is considered.
- Key considerations of materials, processes, and equipment for the assembling of CBGA, PBGA, and TBGA packages.
- Key considerations of placement, process compliance, yield, factory handling, and moisture for PCB assembling of CBGAs, PBGAs, and TBGAs.
- Test-socket of BGAs, and inspection and rework of BGA PCB assemblies.
- BGA industry infrastructure and electronics packaging glossary.

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Ball Grid Array Technology

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To my daughter Judy (who helped to design the book cover) and my wife Teresa for their love, consideration, and patience in allowing me to work on many weekends for this private project. Their simple belief that I am making my small contribution to humanity was a strong motivation for me, and to them I dedicate my efforts on this book.

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Preface

Ball Grid Array (BGA) is not just an emerging technology—it is quickly becoming the package of choice. The last few years have witnessed an explosive growth in the research and development efforts devoted to Ceramic BGAs (CBGA), Plastic BGAs (PBGA), and Tape Automated Bonding (TAB) BGAs (TBGA) as a direct result of the limitations of Fine-Pitch Surface Mount Technology (FPT) and Pin Grid Array (PGA) technology. The BGA technology offers many advantages over FPT and PGA. The most prominently stated benefits of BGA are: reduced coplanarity problems (no leads); reduced placement problems (self-centering); reduced paste printing problems (bridging); reduced handling issues (no damaged leads); lower profile (smaller size); better electrical performance; better thermal performance; better package yield; better board assembly yield; higher interconnect density; cavity-up or -down options; multilayer interconnect options; higher I/Os for a given footprint; shorter wire bonds; easier to extend to multichip modules; and faster design-to-production cycle time.

However, as with any new technology, BGA is not without its problems. In the development of BGA, the following issues must be noted and understood in order to obtain its full benefits: the infrastructure of FPT and PGA is well established; BGA expertise is not commonly available; rework methods are more difficult; solder joint reliability is more critical; BGA availability is limited; BGA testability is not well established; BGA standardization is just starting; BGA assembly inspection is more difficult; BGA cost is higher at low volume; and PBGA cracking has been reported during reflow.

We are now beginning to obtain useful insight and understanding of the economic, design, material, process, equipment, manufacturing, quality, and reliability issues of BGAs. The important BGA parameters such as the Integrated Circuits (ICs), substrates, packaging, routing capabilities, thermal and electrical management, assembly processes, reliability, inspection, rework, test, burn-in, and infrastructure have

been studied by many experts. Their results have already been disclosed in diverse journals or, more incidentally, in the proceedings of many conferences, symposia, and workshops whose primary emphasis is material science or electronic packaging and interconnection. Consequently, there is no single source of information devoted to the state of the art of BGA technology. This book aims to remedy this deficiency and to present, in one volume, a timely summary of progress in all aspects of this fascinating field.

This book covers the three most popular BGA technologies (CBGA, PBGA, and TBGA), and the sequence of this book is basically following the BGA processes. A brief introduction to BGA technologies is presented in Chapter 1.

The book's next two chapters present BGA substrate technologies. In Chapter 2, Richard Sigliano describes ceramic technology and its applications to CBGAs. The merits as well as demerits of plastic technology and its applications to PBGAs are discussed by Osamu Fujikawa and Motoji Kato (Chapter 3).

The advantages in packaging and assembly with BGAs can be offset by the difficulties created in Printed Circuit Board (PCB) routing. The BGA package needs to be carefully chosen with PCB routing in mind. In Chapter 4, Patrick Hession examines the impact of PCB layout on the use of BGAs.

The next four chapters of this book present the CBGA technology. In Chapter 5, Thomas Caulfield, Marie Cole, Frank Cappel, Jeff Zitz, and Joseph Benenati present the design, material, and process of CBGA package carriers. Key considerations of materials, processes, and equipment for assembling CBGAs on PCB are discussed in Chapter 6 by Donald Banks, Karl Hoebener, and Puligandla Viswanadham. In Chapter 7, Yung-Cheng Lee, Jay Liu, Robert Tsai, and Jeffrey Zitz present some specific thermal and electrical characteristics of CBGA assemblies. Chapter 8, by Yifan Guo and John Corbin, provides the mechanical behavior and the reliability of the CBGA assemblies.

The next five chapters present the PBGA technology. In Chapter 9, Robert Marrs presents the design, material, and process of PBGA package carriers. Key considerations of placement, process compliance, yields, factory handling, moisture, and repair for assembling PBGAs on PCB are discussed in Chapter 10 by Bill Mullen, Allen Hertz, Barry Miles, and Robert Darveaux. The electrical and thermal issues of PBGA assemblies are discussed by Phil Rogren (from the vendors' perspective) in Chapter 11, and by David Walshak and Hassan Hashemi (from the users' perspective) in Chapter 12. Extensive data, analytical techniques, and a generalized methodology for PBGA solder joint reliability assessment are provided by Robert Darveaux, Kingshuk Banerji, Andrew Mawer, and Glenn Dody (Chapter 13).

By combining most of the advantages of C4 (Controlled Collapse Chip Connection) technology and TAB technology, IBM was the first to develop the TBGA technology. In Chapter 14, the design, material, and process of TBGA package carriers, and the electrical and thermal issues of TBGA assemblies are discussed by Chin-Ching Huang and Ahmad Hamzehdoost.

The next three chapters present the inspection and rework of BGA assemblies, and the test-socket of BGAs. In Chapter 15, John Adams discusses the nondestructive and automated process test of BGA PCB assemblies with x-ray techniques. Key considerations of the BGA PCB assembly rework process and equipment are presented by Tom Chung and Paul Mescher (Chapter 16). In Chapter 17, Christopher Schmolze presents the material, hardware, and contact issues of BGA burn-in sockets.

The last two chapters present two very important subjects for BGA technology readers. In Chapter 18, E. Jan Vardaman describes the current BGA industry infrastructure (i.e., the relationship and interaction between users and suppliers of the package). In Chapter 19, Ronald Gedney presents, arguably, the most complete glossary in print for electronics packaging.

Some duplication of material between chapters is necessary if each chapter is to offer the reader all the information essential for understanding the subject matter. An attempt has been made to provide a degree of uniformity in perspectives, but diverse views on certain aspects of BGAs are a reality. I hope that their inclusion here is seen as an unvarnished reflection of the state of the art and a useful feature of the book.

For whom is this book intended? Undoubtedly it will be of interest to three groups of specialists: (1) those who are active or intend to become active in research and development of BGAs; (2) those who have encountered practical BGA problems and wish to understand and learn more methods of solving such problems; and (3) those who have to choose a high-performance and cost-effective packaging technique for their interconnect system.

I hope this book will serve as a valuable source of reference to all those faced with the challenging problems created by the ever-more-expanding use of BGAs in electronics packaging and interconnection. I also hope that it will aid in stimulating further research and development on ICs, substrates, solder bumping, wire bonding, TAB, fine-line-and-space high-density low-cost PCB, chip attachment, encapsulant and underfill epoxy, flux, printing, placement, mass reflow, cleaning, inspection, rework, testing, electrical and thermal managements, reliability, equipment, material, process, and design, and more sound use of BGA technologies in either single-chip or multichip packaging applications.

The organizations that learn how to design and manufacture BGAs in their interconnect systems have the potential to make major advances in electronics packaging and to gain great benefits in cost, performance, quality, size, and weight. It is our hope that the information presented in this book may assist in removing roadblocks, avoiding unnecessary false starts, and accelerating design, material, and process development of these technologies. The BGA technologies are limited only by the business constraints, ingenuity, and imagination of engineers, visionless managements, and infrastructures.

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adventure and a privilege, and I learned a lot about Ball Grid Array and other electronic packaging technologies from them. Their brief technical biographies are presented at the end of this book.

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Thermal and Electrical Performance Management in Plastic Ball Grid Array Packages from the Vendor's Perspective

Phil Rogren

11.1 Introduction

The focus of this chapter is a discussion of the electrical and thermal issues that we as manufacturers see around the BGA format. Before jumping straight into the technical issues, however, I think that it is relevant to talk a bit about the author's perspective on the development of the BGA market and infrastructure, and the position that BGAs will assume in the semiconductor packaging hierarchy. While this discussion is from the perspective of the vendor of BGA packages, it is also from the unique perspective of the author.

11.1.1 Package suppliers perspective

The author's experience is in supplying high-performance, cost-effective packages for semiconductors. The company has been working with packages incorporating a multilayer laminate substrate and with molded package bodies for more than six years. The early work was with Plastic Pin Grid Arrays (PPGA), Plastic Leaded Chip Carriers (PLCC) and Plastic Quad Flat Packs (PQFP). As a natural extension of the technology, the company began working with area array packages, other than PGAs, about 4 years ago. Early work with what were called Land Grid Arrays (LGA) led directly to what we have called Solder Grid Arrays (SGA), which are essentially the current Ball Grid Array (BGA) package.

The author's perspective is unique in several ways. First, the company is among the smallest of the BGA suppliers and as a result, is

focused on the niche markets, particularly those applications that require high lead count with high electrical and thermal performance. We also thrive on applications that require relatively low production volumes of customized packages that take advantage of our flexibility. Last, we are ardent supporters of the concept of laminate-based molded packaging for the optimum combination of performance and cost. Because of the emphasis on high-performance and highly customized packages, the company probably has exposure to a wider range of packages than the other suppliers of plastic ball grid array packages.

From our work to date, we are convinced that the BGA will become a viable semiconductor package. We feel that the format is particularly well-suited to the portion of the market that we serve because there is no other format that is as cost-effective or easy to use in the over-208-lead range. Particularly above 300 leads, there is really no other viable format for surface mount, and the PGA becomes an expensive and cumbersome format for through-hole assembly.

The thermal and electrical performance of the format, as we will discuss here, is on a par with anything else available on the market. Probably the most universally important performance measurement is assembly yields, and that is the feature that is most striking about BGAs. Standard surface mount packages have taken us through a progression of tighter lead pitches and more delicate leads. BGAs promise a rare opportunity to make the task of board assembly easier and improve their yields at the same time. Not only can BGAs increase yield while eliminating rework, but they can do it with equipment and processes that have much wider process windows than the industry has seen in many years.

The author does not believe that BGAs will become a major factor for devices with fewer than 208 leads because of the additional cost of the laminate substrate. However, it is possible that the cost advantages of small QFP will be washed out by higher assembly yields and lower costs for equipment used to place BGAs. Our experience to date suggests that there is very little difference in yield expectations between the smallest BGAs and those with 400 or more leads. The current expectation is that a process yielding less than 50 DPM on a package basis is a good starting point for a new process. Normal levels of process refinement will push those levels to less than 5 DPM.

One of the features that makes the BGA format so attractive to a supplier of custom packaging solutions is the relatively low expense involved in tooling for a custom package. While high-volume production tooling is still quite expensive, the tooling costs required to produce anything over a few thousand parts can be amortized over the production run with minimal pain.

11.1.2 Thermal and electrical performance management in plastic BGAs

Performance, like beauty, is in the eye of the beholder. As designers and suppliers of semiconductor packages, we tend to focus on the properties of the package alone, in isolation from the environment in which it will be used. That is not to say that the package manufacturer is totally insensitive to the needs of the end user. We are simply more preoccupied with the things that we can have a direct influence on than with performance influences of the final application environment. That is also not to say that what we perceive as improved performance does not yield a performance improvement to the end user. The real issue is the relative magnitude and importance of the performance features of a given package at the system level. Unfortunately, every system benefits differently from the built-in performance of the package. Consequently, the system designer/manufacturer has to evaluate the performance of a package in the light of his own system environment. The objective of this chapter is to give the user of PBGAs the information they need to evaluate the package performance in their applications.

Thermal. The good news with respect to thermal management is that semiconductor devices are becoming more efficient every day. The thermal energy dissipated by each junction is being pushed lower and lower, despite increases in clock rates. The bad news is that higher levels of integration and smaller design rule geometries are increasing the number of “transistors” per chip and squeezing them into the same size, or even smaller chips. On top of generally increasing power densities, bigger chips are being squeezed into smaller packages (ball grid arrays are a perfect example) and the volume of the systems is being reduced (sub-notebook computers for example). All the while, active cooling systems like fans are virtually being legislated out of existence. The bottom line is increased demand for thermal management at all levels.

The challenge for plastic ball grid arrays is the same as for any other package type. The package must move the heat to the outside of the case where it can be moved out of the system environment. By virtue of their second-level interconnect method, PBGAs have some advantages over other surface mount packages in terms of thermal transfer from the surface of the die to the outside of the package. The problem is that the primary thermal transfer mechanism from a PLCC or QFP is a combination of conduction and convection. In the standard PBGA, the primary thermal transfer mechanism is pure conduction. Depending on the construction of the PCB on which the packages are mounted and the general environment of the system, the leaded packages, with higher thermal resistance from junction to case (θ_{JC}) values, may exhibit lower thermal resistance from junction to ambient.

As with most package types, there are enhancements that can be incorporated in PBGA packages to improve the thermal conductivity between the junction and case. In virtually all cases, reducing thermal resistance to the outside of the package also reduced thermal resistance to ambient. Again, the degree to which θ_{JA} is improved when θ_{JC} is improved is largely dependent upon system design. As package suppliers, our objective is to minimize the thermal resistance of the package and to do whatever is possible to maximize the thermal coupling between the outside of the package and the next level of thermal transport.

Electrical. Electrical performance of the semiconductor packages translates more directly to performance at the system level than does thermal performance. Generally, electrical performance of the PC board can be designed to match or exceed the performance of the package without going to extreme measures. The miniaturization that increases power density and causes major thermal problems for systems designers can actually have a positive effect on electrical performance. As the components are brought closer together, propagation delay and parasitic affects are reduced. Increased clock rates places more demand on the PCB design but the design and manufacturing technologies are fully capable of matching the package performance.

Electrical performance in PBGAs is highly dependent upon the design and construction of the specific package. Perhaps more than any other packaging type, PBGA designs address a wide range of price and performance objectives. When compared with the other available surface mount package types, PBGAs have the dubious honor of both the worst and best electrical performance. As with thermal performance, the second-level interconnect method (the solder balls) have electrical performance advantages over the leads of PLCCs or QFPs. The area array of the PBGA leads also reduces the straight line distance from the bond pad in the die to the interconnect to the PC board. The problem is that there are no straight lines in the package and as the conductor length deviates from the minimum possible, the inductance of the signal traces increases and the general electrical performance decreases. The conductor length is greatly influenced by the basic construction of a specific PBGA design. The design and basic construction options are the predominant factors affecting electrical performance in PBGAs and those issues will be addressed in detail.

11.2 Thermal Performance Management

11.2.1 Thermal transfer basics

From the package supplier's perspective, thermal management is strictly a matter of moving heat from the surface of the die to the out-

side of the package. Thermal transfer within conventional semiconductor packages is almost exclusively via conduction. Convection is a factor only in cavity-style packages and typically plays an insignificant role. Thermal transfer via radiation does occur in all packages but the contribution under practical conditions is totally insignificant to any practical application.

Consequently, our success in moving heat from the die to the package surface is dependent upon the thermal conductivity of the materials that go into the package and upon how those materials are used in the package. In the case of PBGAs, the basic materials and designs are well-defined. In general, those basic materials and the ways in which they are combined to produce PBGA packages do not lend themselves to high thermal performance. Fortunately, there are avenues for increasing the thermal performance significantly by altering the designs slightly and using additional, more thermally conductive materials.

To say that the materials are key to thermal performance is an understatement. The materials that affect the thermal performance of a PBGA package are listed in Table 11.1 along with their relative thermal conductivities. The actual thermal conductivities of these and other common materials are listed in Table 11.2 for your reference. The point is that there is a difference of more than four orders of magnitude among the materials that affect the thermal performance of the package.

In most electronic systems, moving heat away from the outside of the packages is effected via convection. Whether forced or natural convection, and regardless of the fluid medium, modeling and predicting convection cooling is an extremely complex problem involving fluid dynamics, thermal conductivities, and thermal capacities. The fluid dynamics part of the equation is typically so complex that it can only be predicted by comparison to measurements of very similar systems. Fortunately for the package supplier, that problem is out of our hands, left to the system designer to solve.

Conduction mode thermal resistance is an almost perfect analog to electrical resistance, right down to changes in resistivity with changes

TABLE 11.1 Relative Thermal Conductivity of Package Materials

Copper	15,000
Gold	12,000
Silicon	3,000
Sn 63 Solder	1,900
Die Attach Epoxy	190
Mold Compound	22
BT Laminate	7
Air	1

TABLE 11.2 Thermal Conductivity of Various Materials (Watt/Cm°C)

Diamond	5.9
Silver	4.3
Copper	4.0
Gold	3.2
Beryllium oxide	2.5
Aluminum	2.4
Tungsten	1.8
W85/Cu15	1.7
Lead frame	1.6
Silicon carbide	.90
Iron	.84
Silicon	.80
Platinum	.73
Tin	.66
96% aluminum oxide	.35
Die attach epoxy	.05
Mold compound	.006
Laminate substrate	.002
Hydrogen	.002
Air	.0003
Steam	.0002

in temperature of the conducting medium. As such, models are relatively easy to build. The basic equation that applies to conductive heat transfer across a material of uniform composition and cross section is

$$q = -kA \frac{dt}{dx}$$

where q = heat conduction in the x direction
 A = cross-sectional area normal to heat flow
 dt/dx = temperature gradient in x direction
 k = thermal conductivity of conducting medium

In any practical application, the situation is more complex than this simple case, but most cases can be estimated closely enough for practical purposes. In the case of semiconductor packages, there are three issues that make the problem more complex. First is the stack-up of several different materials between the heat source and the outside of the package. Second, the heat source is confined to the surface of the die and will be conducted in all directions. This problem is exacerbated by the fact that in many cases, the die surface is not a uniform heat source but that most of the thermal energy will come from one or two hot spots. In addition to layers of different materials normal to the heat flow, there are also areas of highly different thermal conductivity that lay parallel to the heat flow. The problem of layers of different material in the heat path is a relatively simple one. The illustration in Fig. 11.1

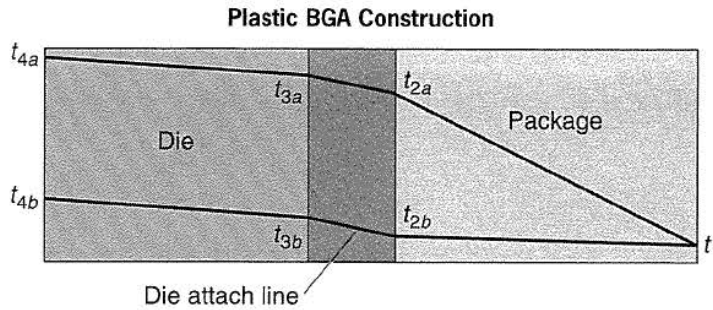


Figure 11.1 The delta t across the material drives the heat flow out of the package. Unfortunately, the objective is to keep the temperature of the die, and thus, the delta t low. The only way to have both is to keep the thermal resistance as low as possible in all materials.

shows schematically the stack-up of die, die attach, and package. t_1 is the temperature of the outside of the package. t_{2a} and t_{2b} are the temperatures at the interfaces between the die-attach material and the package. The difference in those two temperatures illustrates the problem of high thermal resistance in the package. The thermal resistance of the die is represented by the temperature increase between t_3 and t_4 . The delta t across the die is virtually the same along both lines a and b . The same is true across the die attach line, from t_3 to t_2 .

In the multilayer case, the heat flow across all of the layers is equal; therefore we can write

$$q = k_a A \frac{t_1 - t_2}{\Delta x_a} = k_b A \frac{t_2 - t_3}{\Delta x_b} = k_c A \frac{t_3 - t_4}{\Delta x_c}$$

These equalities can be rewritten to express the temperature across each layer.

$$t_1 - t_2 = q \frac{\Delta x_a}{k_a A}$$

$$t_2 - t_3 = q \frac{\Delta x_b}{k_b A}$$

$$t_3 - t_4 = q \frac{\Delta x_c}{k_c A}$$

Unfortunately, real-world thermal transfer problems are never as simple as flat plates with the heat source on one side and an infinite heat sink on the other side. Even multiple-layer models are very simple when compared to real applications. Semiconductor packages are obviously no exception. In virtually all cases, the heat source—the junctions on the surface of the die—are completely surrounded by the materials that make up the package. If you draw a line from the junction to the outside of the package, it may cross a single, homogeneous

layer, or it could cross half a dozen different material layers. The very simplest situation is that of a standard molded plastic package, illustrated in Fig. 11.2.

In the molded package, the heat source on the top of the die has a direct path to the outside through the mold compound. In addition, there is a path to the backside of the package, which goes through the die itself, the die-attach line, the die-attach flag, and then through the mold compound on the back of the package. Those are the physically shortest paths, but because of the high thermal resistance of the mold material, they do not represent the primary thermal path. Most of the thermal energy moves out of the package through the leads. It is easy to understand why the longer path along the lead is the shorter thermal path, but it is a complex task to model the coupling between the die and the leads. There are two major thermal connections between the two. One is through the wire bonds and the other is through the die and die attach line, into the die attach flag, and then across the mold compound between the flag and the lead fingers.

Modeling the thermal transmission of the bond wires is fairly simple. They really look like long, flat plates, and for all practical purposes, they are wrapped in a perfect thermal insulator since gold wire is more than 500 times more thermally conductive than the mold compound. Modeling the path through the back of the die is much more complicated. Essentially, there are a number of thermal resistances in series between the heat source(s) and the lead fingers. Each resistance can be determined and the series resistance calculated. The problem is that none of these physical regions resembles a flat plate. In all cases the cross section of the region is constantly changing as you move along the path of the heat flow. In some cases the direction of heat flow is not clear from casual observation. The only way to determine the thermal transfer with any degree of accuracy is through the application of some form of finite element analysis.

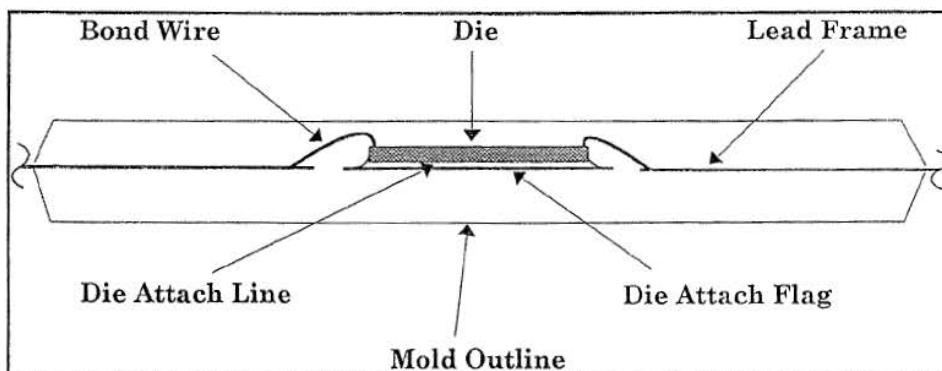


Figure 11.2 Standard molded QFP.

In cases where the heat source is well-defined and the surrounding material is uniform in composition, simple relaxation models can be constructed that yield reasonable results. In most cases the problems are complex enough that a real solution is not practical without sophisticated thermal analysis software.

The good news about thermal analysis of the package itself is that the hard parts can often be ignored. We have learned empirically that devices dumping a watt or a little more will perform well in a standard molded package. We also know that as the die and package get larger, they will transfer more power to the outside of the package. The result is an imperial set of practical power levels for each package family. The difficult situations come as the application approaches those assumed limits.

For high-power applications, those well beyond the limits of standard packages, the problem of predicting the overall thermal performance of the package is actually simplified. In order to go from one or two watts to 6 to 10 watts coming out of a plastic package, the thermal path must be radically improved. Typically those improvements are effected by replacing mold compound with high thermal conductivity material. In the case of plastic packages, that material is usually copper. For all packaging designs, adding a good thermal conductor reduces the primary thermal path to a flat plate model. While this enhanced thermal path is only one of several parallel paths to the outside of the package, it has a very low resistance relative to the others and thus dominates the thermal performance of the package. In most applications, the contribution of the secondary paths are swamped out by variations in the application environment and can be ignored.

The role of the package. Thermally, the role of the package is to move the heat dissipated by the active elements on the surface of the die to the outside of the package and then to transfer it to the next level of thermal conductor. The role of the package designer, with respect to thermal management, is to ensure that a sufficient thermal path exists to remove the power that the chip dissipates.

11.2.2 Package construction

Plastic ball grid arrays are available in two basic configurations. The most common and most basic package is a thin PC board with the die on one side and the solder balls on the other. The body of the package and the protection for the die is a transfer molded structure on the side of the substrate opposite the balls. This basic configuration goes by the Motorola trade name OMPAC[®],* which stands for Over Molded Pad

* OMPAC is a registered trademark of Motorola, Inc.

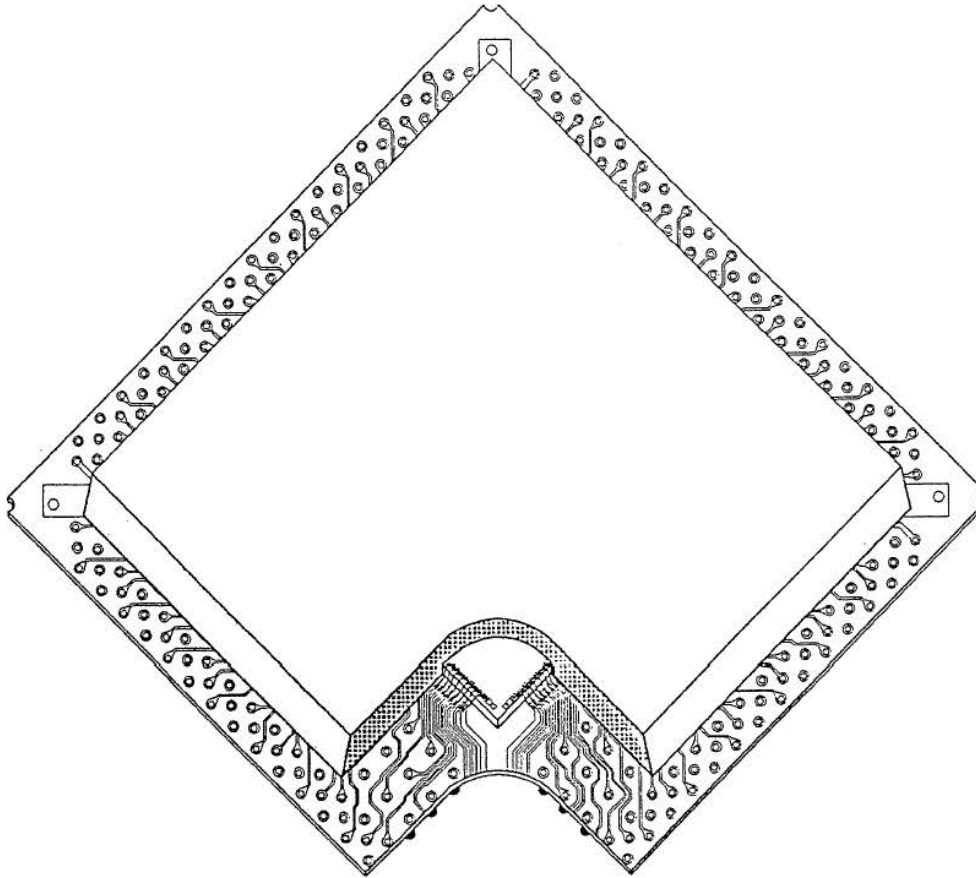


Figure 11.3 Cut-out of an OMPAC-style package.

Array Carrier. Figure 11.3 illustrates the construction of the basic OMPAC style package. In the basic configuration, the OMPAC style package is slightly superior in terms of thermal transfer to an equivalent-sized PQFP. It is important to note that the improved performance is in thermal resistance between junction and case (θ_{jc}). The improved performance is the result of the relatively shorter thermal path between the die and the balls on the back of the package. The primary heat sink in OMPAC style of package is the PC board to which they are attached. The equivalent QFP delivers its heat to the leads at the edge of the package, which in turn pass it to the air around the package. The relative efficiency of these two thermal paths depends upon the construction of the PC board and the quality of the airflow around the packages. The result is that even though the PBGA has a lower θ_{jc} , the thermal resistance between the junction and the final heat sink may be higher because of the way it couples to that heat sink.

There are a number of variations to the OMPAC construction but the only one that has any real effect on thermal management is the addi-

tion of thermal vias through the substrate under the die. Again, this enhancement delivers the heat primarily to the PC board. If the board is not capable of moving the heat away from the package, the thermal vias will be of little value even though they reduce the θ_{jc} significantly.

The pure OMPAC style package is the PBGA standard and the equivalent of the standard, lead-frame-based molded plastic QFP. It is appropriate for the majority of semiconductor devices and is the most economical of PBGA designs. All of the other designs address higher performance applications and much smaller markets. As with enhancements to most products, the enhancement comes at a certain cost. Consequently, the higher thermal performance PBGAs are finding acceptance where there is a need to dissipate more than about 2 watts. There are essentially three approaches to improving the thermal performance of a PBGA as illustrated in Fig. 11.4. The simplest is to put thermal vias through the substrate from the back of the die to the back of the package. A thermal via is simply a hole through the substrate that is plated with copper. Electrical vias can serve as thermal vias. The only real difference between the two is that thermal vias are employed in arrays that place as much copper as possible in the area of the array. The effectiveness of thermal vias is dependent upon the area of copper in the array and is inversely proportional to the thickness of the substrate.

As mentioned previously, this approach can be effective if the PC board to which the package is attached is capable of transferring the heat away from the package. In applications where the heat can be moved away from the package, thermal vias can take PBGA thermal performance from the 1- to 2-watt range to the 3- to 4-watt range.

The next step up in thermal performance enhancements for PBGAs is copper planes in the substrate that spread the heat over the entire area of the package. Typically, thermally conductive planes are used in conjunction with thermal vias. As with thermal vias, thermal planes can and most commonly do act as electrical planes as well. The difference between thermal and electrical planes is that copper planes included for electrical reasons perform their duty very well at thicknesses of .0007 to .0014 in. While a 1.4-mil-thick copper plane is of some help, the typical thickness for a thermal plane is between 4 and 8 mils. The primary thermal path in a package with thermal planes is parallel to the surface of the plane, through the solder balls, and into the PC board. Unlike the thermal via approach, thermal planes also enhance the secondary thermal path through the mold compound to the top of the package.

While the basic construction of a package with thermal planes is the same as the basic OMPAC style, the substrate is significantly different. Basic OMPAC has a metallized layer on the top and bottom surface of the substrate only. To incorporate thermal planes, it is necessary to

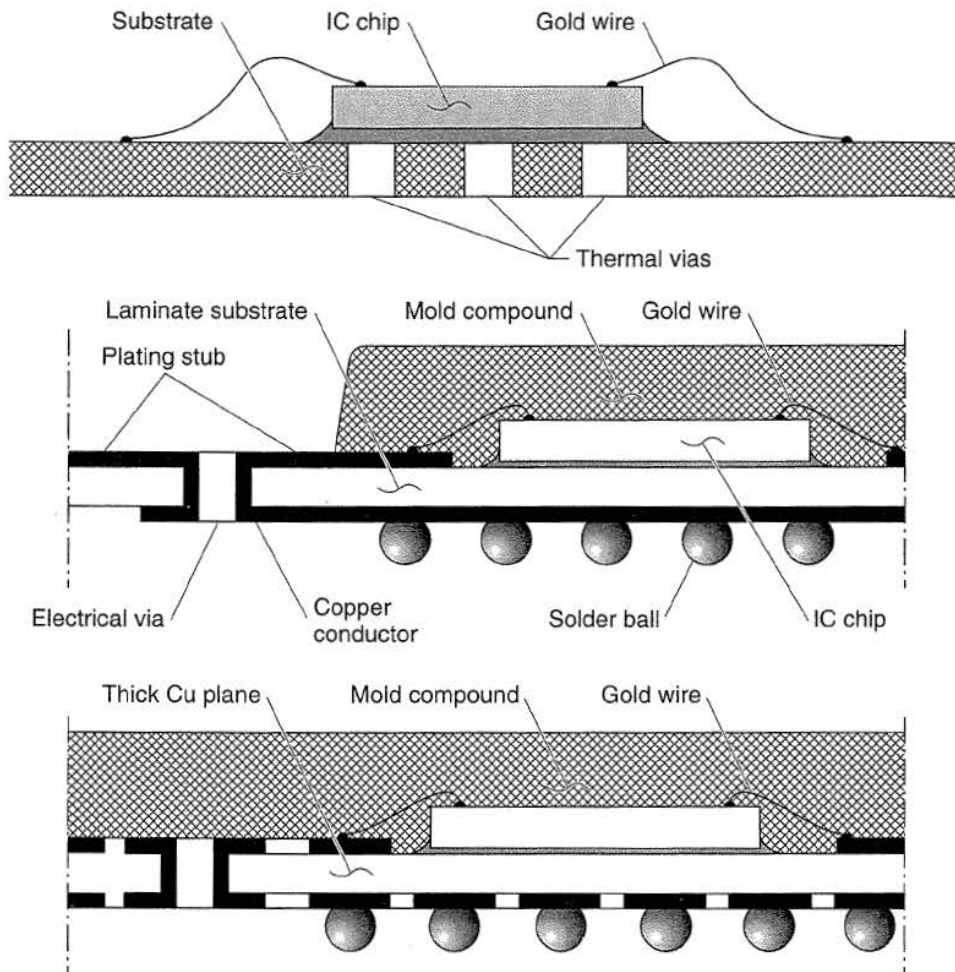


Figure 11.4 Three thermal-enhanced PBGAs.

have more than just the two layers of metal. The added complexity of a multilayer substrate typically yields electrical as well as thermal benefits, but it also increases the cost of the package.

For the maximum in thermal performance, the configuration of the PBGA package is changed considerably. The package is constructed with the die attached directly to a copper slug which forms most of the top surface of the package. The substrate is also attached to the copper slug and forms a cavity around the die. The balls are attached to the surface of the substrate opposite the copper slug and they form a depopulated array around the cavity. Figure 11.5 illustrates the typical construction of what Hestia calls a *high-performance solder grid array*. Aside from the copper heat spreader, the most interesting feature is the cavity-style substrate. In order to provide room for the wire bonds, the wire-bond ledge must be set well below the ball surface of the substrate. This construction dictated the use of a multilayer substrate and

as such, electrical performance of these packages can be significantly improved over standard PBGAs. The cost also increases.

The price for the improvement in thermal performance is modest and the price/performance ratio is extremely low when compared to ceramic multilayer with Copper/Tungsten heat spreaders. The thermal performance of this style of package, as represented by θ_{jc} , is dependent upon the size of the heat source and the size of the heat spreader. In the smallest practical sizes for this construction, around 100 balls, θ_{jc} should be less than $4^{\circ}\text{C}/\text{W}$. With packages designed to house die more than 15 mm sq. and heat spreaders in the range of 37 mm sq., θ_{jc} can go to less than $0.15^{\circ}\text{C}/\text{W}$. This is really the area where the package supplier and the system manufacturer can interrupt the performance differently. While the package supplier is likely to see this package as capable of dissipating more than 300 watts with a 50°C delta above ambient, the systems designer may see it as stretching to deal with 7 watts. The difference in perspective is a function of how each sees the transfer of heat from the package to ambient. As packages suppliers, we know that the systems guys can run these things in liquid nitrogen if something gets too hot. Unfortunately, the systems designer wants to make the system as small and as quiet as possible and cooling systems are incompatible with those objectives.

The real story on laminate packages with copper heat spreaders is that their θ_{jc} is lower than a multilayer ceramic package with the same size copper tungsten heat spreader for a fraction of the cost. They do have the same problems as any thermally enhanced package. The thermal enhancement can only move the heat from the die to the back of the package. There must be some provision made to thermally couple the package to the final heat sink, and the efficiency of that path dictates the practical efficiency of the package.

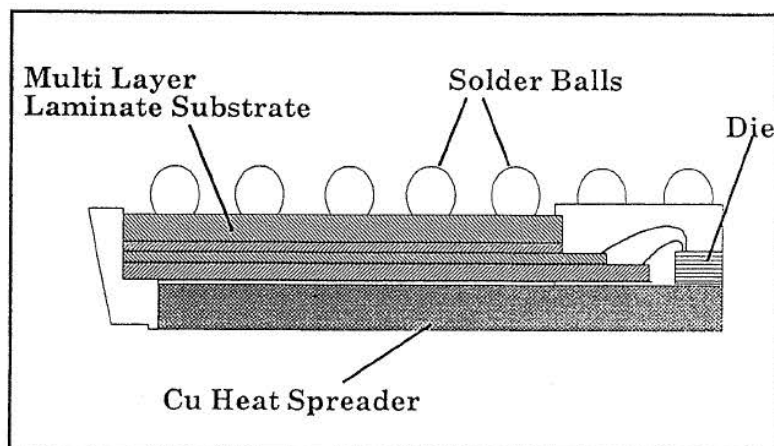


Figure 11.5 High-performance solder grid array.

External augmentation. One way to improve the transfer of thermal energy from the package to the air inside the system enclosure is to increase the area of the package. One of the simplest ways of doing that is to add a heat sink to the back of the package. These devices, which are available in many different configurations and materials, can improve the performance of any package. The real improvement is a function of the θ_j of the package, the attachment of the heat sink to the package and the efficiency of the heat sink itself. One of the most common types is illustrated in Fig. 11.6.

While external heat sinks offer a quick and easy way to increase the thermal efficiency of any package, the PBGA format offers a few challenges that are not issues in other form factors. The most notable problem is with the balls themselves. During the reflow of a PBGA, the solder ball melts completely. In most cases, the weight of the packages literally floats on the ball of molten solder. The advantage with this system is that the surface tension of the molten solder pulls the package into the alignment with the metal pattern on the PC board that produces the lowest cumulative surface tension among all the balls. By definition, this is the best possible alignment of package to board. Adding a copper heat spreader to the package can compromise its ability to float. Each ball can support just so much weight before collapsing into contact with its neighbor. External heat sinks are typically heav-

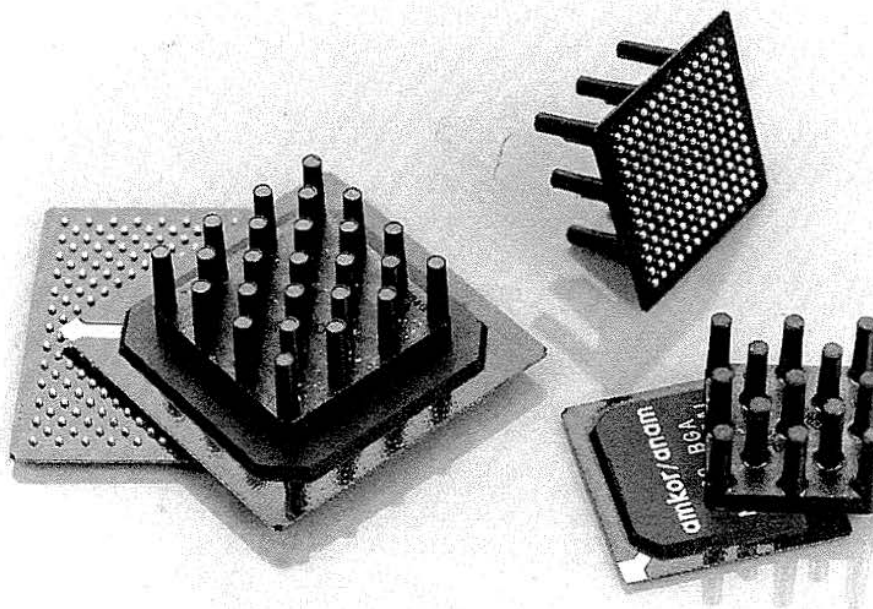


Figure 11.6 Examples of heat sinks for OMPAC® style plastic ball grid arrays. (Photo courtesy of Wakefield Engineering.)

ier than integral heat spreaders and in most cases would catastrophically collapse the solder balls. The solutions are fairly straight forward but do compromise some of the advantages of the PBGA form factor. First, standoffs can be molded into the package to prevent the added weight from collapsing the balls. The standoff, however, can prevent the package from being pulled to best alignment by the surface tension of the solder. The other solution is to attach the heat sink after the package has been reflowed to the PC board. Probably not the most elegant solution from a manufacturing perspective, but effective.

11.3 Electrical Performance Management

11.3.1 Vendor vs. end-user perspective

As with thermal performance, the real electrical performance contribution of a semiconductor package is influenced by its environment. The electrical environment of a package is primarily the board to which it is directly attached. Increasing the performance of the board typically involves adding wiring layers to the board and designing the interconnect to maximize performance. Along with performance, cost is also increased. However, in contrast to the measures necessary to improve the thermal environment, the monetary cost is low and there is virtually no change to the outline and components of the system when the PC board is optimized for electrical performance. In addition, electrical performance improvements in the PC board can be effected for virtually any system whereas thermal improvements require physical attributes which can be impossible to provide for some applications.

The bottom line is that high electrical performance in the package is much more likely to be translated into equivalent performance at the system level. Consequently, the perspective of the package supplied and the system designed are much more closely aligned.

11.3.2 Basic electrical requirements

The basic electrical features in semiconductor packages are conductive paths between the chip and the outside world and insulating separations between the conductive paths. The conductive paths between the chip I/O and the outside world must be of low enough resistance to maintain required voltage levels in the signal. For most packages, this is not a problem. For PBGAs with robust copper conductors, low resistance traces are unavoidable, and ultra low resistance is easy to design in.

Resistance between adjacent conductors is a slightly more complicated issue. With most high-speed digital devices, resistances in the range of a 10^6 ohm are all that are required for proper device function. No package makers worth their salt would consider shipping a

package with resistances that low. The problem comes when very high isolation resistance is required. It is not uncommon to see leakage currents specified at less than 1 nA at 100 volts, or $10^{11}\Omega$ on multilayer ceramic packages. There are very few devices that really require that level of electrical isolation but there are a few. Laminate-based packages are certainly capable of that level of isolation when they are dry, but in real systems, that is probably not the case. One of the biggest problems with PBGA packages is that both the laminate substrate and the mold compound absorb moisture, which, among other things, reduces the resistivity of both those materials. The degree to which this is a problem is primarily dependent upon the device. In most applications, we do not see excessive leakage current as a failure mode until the package has been exposed to pressure cooker conditions (121°C, 100 percent relative humidity and 2 atmospheres pressure) for more than 168 hours. Even then the condition can be reversed simply by baking the component dry. The point is that semiconductor devices that operate with current levels in the pico amp range may not be candidates for PBGA packages, or plastic packages in general. Higher power devices should not experience any problem.

11.3.3 Noise problems in semiconductor packages

All commercially available packaging solutions for semiconductor devices meet the basic requirements for low resistance in the conductors and high resistivity in the dielectric materials. The more pressing issue with the electrical performance in semiconductor packages is electrical noise, and there are three major sources of noise in a semiconductor package: (1) coupling of signals between nearby conductors due to parasitic capacitance and inductance, (2) voltage bounce generated by transient currents in inductive elements, and (3) reflections from impedance discontinuities in the conductive elements.

Noise associated with capacitive and inductive coupling is more commonly known as *crosstalk*. Capacitive crosstalk is a function of the dielectric constant of the package insulating materials and of the separation between conductors. Reducing the dielectric constant and increasing the separation of conductors reduces capacitive coupling. Unfortunately, the dielectric constant of the insulating materials is defined to a narrow range by the materials applicable to a given package type. The physical separation of conductors is a design issue, but largely constrained by the die and the form factor of the package. There is, however, more latitude to influence capacitive-coupled noise with design than with materials selection. Increasing the number of conductive layers provides more design flexibility to both space conductors farther apart and to isolate

traces that are particularly sensitive to capacitive coupling. Inductive crosstalk is largely a design problem in most packages but is influenced by the magnetic permeability of the conductors and the other materials in the package. Again, increasing the number of metal layers and providing flexibility to vary dielectric thicknesses provides the latitude necessary to reduce inductive coupling by design.

For packages housing high-speed digital circuits, induced voltage in the ground circuit (or ground bounce) is a problem of at least equal magnitude to crosstalk. Ground bounce—or for that matter, supply voltage bounce—is caused when many outputs switch simultaneously causing a current surge in the ground or supply circuit. The induced voltage is a function of the self-inductance of the circuit and the rate of change in the current pulse. The voltage potential, that can be calculated by the equation

$$v = L \frac{di}{dt}$$

appears as noise on the inputs and outputs of the IC and thus reduces the noise margin. The voltage “bounce” can be reduced by reducing the rate of change in the switching current, but that implies slowing down the chip. For all practical purposes, voltage bounce must be controlled by reducing the self-inductance in the power and ground circuits. This is accomplished by avoiding materials with high magnetic permeability and by design. Increasing the number of metal layers is particularly important in controlling inductance. The easiest way to reduce self-inductance is to increase the area of the current path while minimizing the length of the current path. The result is that wherever practical, power and ground circuits are actually planes that, as completely as possible, cover the entire area of a metal layer.

The problem of reflections from impedance mismatches is really two problems. The first is signals reflected from physical discontinuities in the package. The most problematic of these in most cases are the traces used to plate the exposed metalization on laminate-based and cofire ceramic packages. In virtually all cases, these traces simply end at the edge of the package and reflect a large portion of the signal incident upon them back into the circuit and to the input of the chip. The impact of these reflected signals increases as the clock rate increases and, again, appears as noise at the inputs and outputs of the chip.

The second part of the problem with reflections from impedance mismatches is probably more important in most cases. In order for the signal to be passed from one circuit element to the next, the characteristic impedance of the two elements must match as closely as possible. To the degree that the impedance of a transmission line and the inputs of the chip do not match, the signal is reflected back into

the input circuitry. While this reflection appears as noise in the circuit, the more important issue is the reduced transfer of the signal onto and off of the chip. To complicate the problem, characteristic input impedances of the various semiconductor devices range from around 50 to 110 Ω . Impedance in semiconductor packages is primarily a function of capacitance and inductance, which really gets back to dielectric constant, magnetic permeability, and design. In most package types, magnetic permeability is not an issue and dielectric constant is closely dictated by the packaging type. That leaves only design as a major impedance variable. However, with design, it is possible to vary capacitance, inductance, and resistance over a wide range. This is particularly true when multiple conductive layers are available to the designer.

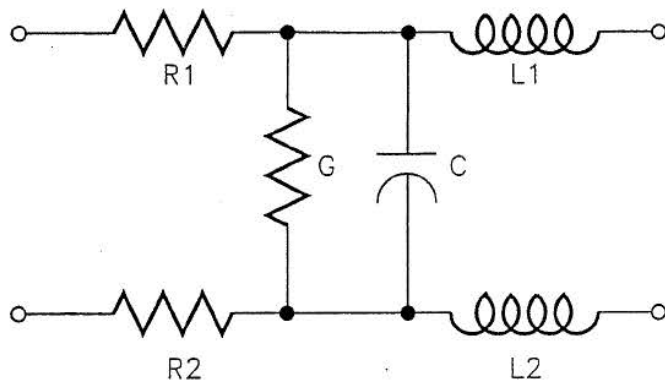
Figure 11.7 is the equivalent circuit for a finite length of the typical transmission lines on all semiconductor packages. The value of G , the conductance between the two legs of the transmission line and R , the resistance of each leg are insignificant in most applications and can be neglected. Figure 11.8 shows the equivalent circuit as it appears without considering R and G . This network is terminated with an impedance that represents the impedance of an infinite number of sections exactly like the section under consideration. Z_0 is the characteristic impedance of the line, Z_1 is the distributed reactive impedance of the section, and Z_2 is the capacitive reactance of the section. Without going into the mathematics, the characteristic impedance of a transmission line is primarily dependent on the ratio of the distributed inductance and capacitance in the line. That allows the line to be characterized by looking at the lumped values of capacitance and inductance for a finite section of the line according to the equation

$$Z_0 = \sqrt{\frac{L}{C}}$$

What is not obvious from any of the basic discussion of factors influencing impedance is the effect of the inherent geometries of the processes and how they interact with the basic materials parameters.

11.3.4 The role of the package in electrical performance

The role of the packages is to deliver the functionality of the chip to the rest of the system with as little degradation as possible. Having said that, the implication is that the package does damage to the intrinsic performance of the chip. The implication is accurate. The chip is capable of significantly better performance before any electrical or mechanical connections are made to it. Unfortunately, the chip is of virtually no practical value in that state.



- $L1$ —Inductance of the top conductor.
 $L2$ —Inductance of the bottom conductor.
 $R1$ —Resistance of top conductor.
 $R2$ —Resistance of bottom conductor.
 G —Conductance between conductors.
 C —Capacitance between conductors.

Figure 11.7 Equivalent circuit for a finite-length transmission line of an IC.

In addition to acting as the electrical interface to the rest of the system, the package provides a translation of geometries from those of the chip to those of the real world and to provide mechanical and environmental protection. In all packages, the space translation is a performance problem. The mechanical protection features may or may not impose significant performance limitations, depending upon the design.

The degree to which the performance of the chip is degraded can be reduced by the package design. In keeping with the natural laws of economics, the simplest (and therefore least expensive) designs do the most damage to performance. The performance of the chip can be preserved with careful design of the package. The problem is that these

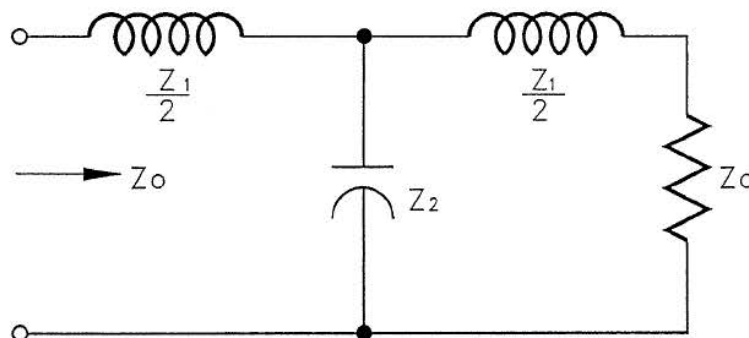


Figure 11.8 Equivalent circuit without R and G .

designs are more complex mechanically and thus more expensive. Fortunately, the majority of chips can deliver adequate performance with the simplest of packages. The question of electrical performance, then, only becomes an issue for the fastest or most sensitive devices.

11.3.5 The materials set

Plastic ball grid array packages are blessed with a good basic materials set. Table 11.3 lists the basic properties of those materials. First of all, the electrical properties of all the materials are good. The electrical conductivity of the copper conductor material is among the highest available. The dielectric properties of both the glass/epoxy substrates and the mold material are favorable with dielectric constants in the range of 4. The mechanical attributes of the materials and the processes used to produce laminate substrates lend themselves to advantageous geometries in both the conductors and the dielectric structures. The practical conductor pitches, down to around 100 μm , are well-suited to translate the fine geometries of the chip and the first-level interconnect to the courser geometries of the PC board. Those natural geometries, combined with the basic electrical properties, allow for the easy design of transmission lines with characteristic impedance that match to most semiconductor devices.

The range of geometries possible and practical in laminate manufacturing processes bring more to the party than just the ability to do the space transformation from the die to the PC board. The combination of those natural geometries and the basic electrical properties allows for the easy design of transmission lines with characteristic impedances that match to most semiconductor devices. Practical dielectric thicknesses for PBGA substrates range from .002 to .020 in. Minimum conductor width is in the range of .002 in and there is no maximum except for the width of the substrate. Using conductor designs with maximum width of .020 in, it is possible to achieve impedance values from 2 or 3 Ω to 110 Ω . While neither the range nor the absolute impedance numbers are unique to laminate substrates, there is no other packaging type that has a materials set that allows those numbers to be achieved so easily.

TABLE 11.3 Electrical Properties of Laminate Materials

Sheet resistivity	1 m Ω /Sq.
Dielectric constant	4.2
Impedance	20 to 100 Ω
Propagation delay	70 pS/Inch
Minimum conductor pitch	.004"
Dielectric thickness range	.002" to .030"

Plastic ball grid arrays are still in the industry-acceptance portion of their life cycle, and as such, there continues to be significant evaluation and development done of materials, processes, and designs. The current basis for PBGA packages is a substrate made of Bismalimide Triazene (BT) epoxy and E glass. The primary purpose for choosing this material is its high glass transition temperature at a moderate cost premium over FR-4. The high T_g , in the range of 190°C , is necessary to withstand the thermal exposure associated with thermosonic bonding and transfer molding. As an added benefit, the BT board has a lower dielectric constant than FR-4 at around 4.1.

The current conductor is copper laminate. In standard designs, the copper is $\frac{1}{2}$ oz/sq. ft, or about $17.5\text{ }\mu\text{m}$ thick. At that thickness, the conductors exhibit a sheet resistivity of around $1\text{ m}\Omega/\text{sq}$. The mold compound that complete current PBGA designs is one of several that are also used for standard molded packages. Typically these materials have dielectric constants from about 3.7 to 4.4.

11.3.6 Package construction

The advantages of the materials set are analogous to having good genes. You may be genetically predisposed to live to a ripe old age, but you can always find a way to squander your advantage and die young. In the case of PBGAs, the problem is that the most natural design for economical packages is close to the worst case for electrical performance. The most basic PBGA conductor design is illustrated in Fig. 11.9. Essentially, the conductor traces are routed from the edge of the die to the outer edge of the package, through vias to the backside of the package, and then to a solder ball location. This design makes it virtually impossible to avoid doubling the conductor over on itself, separated only by the thickness of the substrate. The result is very high mutual- and self-inductance in the traces. Generally, the individual conductors in PBGAs of this design can be expected to have self-inductance that is higher than in the conductors of a QFP of comparable lead count. Even with this problem, the standard OMPAC[®] design is adequate for most semiconductor devices and applications.

Where improved electrical performance is required, there are changes in the package construction and design that allow the package designer to take full advantage of the properties of the materials set. The biggest problem with the OMPAC[®] design is the fact that the conductors transition from the top to the bottom of the substrate only at the extreme outside edge of the substrate. This design eliminates the possibility of mold material leaking through vias since there are none in the molded area. It is also mechanically logical since the traces must be routed to the edges to be tied to the electrolytic plating bus. By rout-

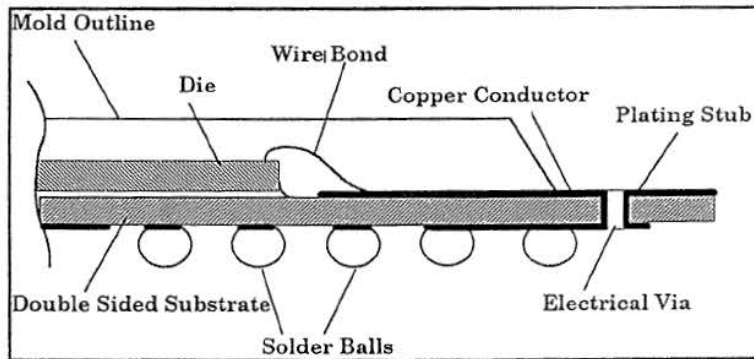


Figure 11.9 OMPAC conductor configuration.

ing the traces to vias under the molded area, and designing for the shortest possible conductor lengths, much of the self-inductance of the trace can be eliminated. With shortened traces, the inductance of the leads in a PBGA would typically be less than in the leads of a standard QFP with the same lead count. Unfortunately, the extension of the traces for plating—from the vias to the edge of the substrate—still adds capacitance and inductance and is a source of reflected noise from the stubbed-off end of the conductor. The only way to eliminate the plating stubs is to eliminate electrolytic plating of the conductors. Since the standard conductor material is essentially pure copper, either the material must be changed, or the surface of the copper must somehow be treated to be compatible with the gold thermosonic bonding processes. At this point, the most practical way to provide that surface without plating stubs is by electroless plating of gold on the copper conductors.

Once we eliminate the plating traces and provide for vias under the molded area of the package, the next step in improving the performance of the package is to increase the number of wiring layers. As the number of wiring layers increases, there are several performance-enhancing features that can be incorporated in the package. For practical purposes, wiring layers are added two at a time. Effectively, a four-metal layer board is made by sandwiching a layer of epoxy/glass laminate material, with no metallization, between two double-sided boards. With four metallized layers to work with, there is room for two layers for signals and two layers for low-inductance power and ground planes. Further increasing the number of available metal layers increases the flexibility to design precise transmission lines and to add even more complex power-distribution systems to isolate sensitive portions of the circuit.

The multilayer PBGA construction is basically equivalent to multilayer ceramic package construction in concept and in the feature

geometries. The big difference is in the properties of the two materials sets. The resistivity of the tungsten conductors of cofire ceramic is an order of magnitude higher than the copper in the multilayer laminate, and the dielectric constant of the ceramic is two times that of BT epoxy/glass. The result is that laminate-based multilayer substrates can be implemented in fewer layers than is possible in cofire ceramic multilayer.

11.3.7 Electrical advantages of BGAs vs. other surface mount packages

BGAs do have one inherent electrical performance advantage over other surface mount packages. That advantage lies in the interface between the package substrate and the PC board: the solder balls themselves. When compared to the leads of a QFP or a PLCC, the solder balls are short, they are relatively large in area, and they are widely spaced. The result is an electrical connection of significantly lower inductance than with the leads of other surface mount packages.

In addition to the lower lead inductance, the average length of the package conductors is much shorter in a BGA than in a QFP. Shortening the conductor does reduce the capacitance, inductance, and the total time of flight for the signal. Unfortunately, this is one of the areas where the package supplier and the system designer are likely to see this performance advantage differently. In cases where the footprint of a BGA package is the same size or larger than an equivalent QFP, reduced package conductor length does not translate into an overall shorter distance for the signal to travel. The only real effect in those cases is to move the signal path more to the PC board. Depending upon the PC board design, that may improve or degrade the electrical performance.

For high-lead-count, multilayer BGAs, not only is the average package conductor length less than the equivalent QFP's, but the maximum conductor length is also lower. BGAs become more area efficient than QFPs at around 100 leads. As the I/O count goes up the area efficiency advantage of the BGA increases. The 304 QFP occupies 1849 sq. mm as opposed to 625 sq. mm for the 324 BGA with 1.27-mm ball pitch. That translates to a real reduction in trace length and, therefore, to propagation delay between system components.

It probably comes as no surprise to anyone that increasing the performance of PBGAs increases their cost. Since cost is also a real performance attribute, it is necessary to weigh the cost against the benefit of high-performance packages. In most cases, the price for enhanced performance in PBGAs will be lower than for other packages types with the same lead counts. The primary reason for the lower cost is the smaller size of the PBGA. To build a QFP that is elec-

trically equivalent to a PBGA with a four-layer board, the QFP will have to have a wiring system that is very similar to the PBGA. In fact, the most practical option is to use essentially the same board in the QFP as is used in the PBGA. The only difference is the size. Looking again at the comparison of the 304 QFP to the 324 PBGA, the substrate for the QFP would be in the range of 38 mm sq. as opposed to 25 mm sq. for the PBGA. The direct area ratio of QFP to PBGA is 2.3:1. If you extend the comparison to less area-efficient formats such as PGAs, the area ratios become even larger. Again looking at the 300 lead-count range, a standard PGA would occupy at least 3.4 times the space of a PBGA, and in a more practical configuration, the ratio is closer to 5:1.

The bottom line is that increasing the electrical performance of a BGS does increase the cost, but that the incremental cost for increased performance is less in the PBGA format than it is for other formats. Additionally, most high-performance PBGAs have greater potential to increase the system performance than the other formats simply because of their smaller size and therefore shorter conductor paths. It is also important to consider that the smaller BGA footprint also reduces the size of the system board, yielding both electrical performance and cost improvements.

11.3.8 Electrical modeling and high-performance design

Having come to the point of understanding that PBGAs are endowed with a materials set that lends itself to high electrical performance, and that there is sufficient latitude in the construction of the packages to take advantage of the materials set, the focus goes to design. Intrinsically, plastic ball grid array packages have all of the advantages of other package formats based on a laminate substrate and have shed some of the limitations by growing smaller than their cousins. The general design features are similar to those used in laminate-based QFPs, PLCCs, and PGAs. To tune the designs to optimum performance, we need careful evaluation and measurement of actual packages. To this point, we do not have sufficient data to model PBGA's electrical performance to the degree that we will ultimately need.

We can, however, take what we have learned from other packages and from our early work with PBGAs and postulate a number of rather solid rules for PBGA design. The issues of crosstalk are the same as with most other package types. The one advantage that PBGAs have is that their leads are generally shorter—and thus couple less energy—both through capacitance and inductance, into their neighbors. The keys to low crosstalk are to minimize the length of parallel conductors and to space them as far apart as possible. Reducing voltage bounce in

either power supply or ground circuitry is a matter of lowering the inductance of the circuits. In most cases this is accomplished by increasing the number of pins dedicated to each circuit and distributing those pins around the package to equalize current in each. All of the pins for a given circuit are shorted together to a plane that occupies as much as possible of one metal layer. In many cases, a few signal lines are more sensitive to noise than most and need special treatment. In these cases it is often desirable to split power and ground planes into quiet and noisy planes. The quiet planes are reserved for the few extra-sensitive signals, and the less-sensitive lines connect to the noisy planes. Even though these planes are connected to common power and ground sources somewhere on the PC board, moving that unification closer to the power supply can significantly reduce the noise apparent at the chip.

One of the problems with the leaded surface mount packages is that the parasitics of the leads are both unfavorable and essentially fixed for a given package configuration. The inductance of a solder ball is variable within a narrow range, but is typically less than one-third that of the gull wing lead of a QFP. More importantly, the capacitance, and therefore the impedance of the leads can be varied significantly by varying the spacing of the balls. While there are effectively six different pitches approved by JEDEC, it is not generally practical or desirable to change the ball pitch to modify the impedance of a few signal traces. Instead, JEDEC, and the configuration flexibility built into the ball grid format, allow the removal of individual balls to increase individual ball spacing and thus reduce the capacitance. By using this design approach and controlling the size of the solder ball it is possible to adjust the impedance of the solder ball connection from around 20 to 50 Ω without much difficulty. Increasing the impedance to the 100 Ω range is possible but causes significantly more disruption of the ball pattern.

11.4 Summary

Plastic ball grid array packages offer an array of options in construction and design that allows the format to be competitive with any other in terms of electrical and thermal performance. Thermally, the standard PBGA package has a shorter thermal path to the PC board than any other package type. To be useful, the PC board needs to be of a construction that will absorb and dissipate the thermal energy transferred through the balls. Moving to more complex packages, there are a number of features that can be added to PBGA packages that can move their thermal performance into competition with the very best of semiconductor packages. The beginning step is to add thermal vias that can

improve the thermal performance by 20 to 40 percent depending upon the substrate and the exact configuration of the package. Internal copper planes can spread the heat out, over the full area of the package and move the heat to both the top and bottom of the package. Typically, thermal planes will improve the thermal dissipation capabilities of a package by 50 percent. The real big improvement comes when the back of the package is replaced by a copper plane. This requires making the package a cavity-down design and, necessarily, increases the size of the package. The pay-back for the larger package is a package that is a thermal transfer champion. Actual performance depends on both the package and die size, but θ_{jc} values less than 0.2°C/W are possible in real-world packages. θ_{ja} values for these packages can be less than 1°C/W .

Electrically, the PBGA package benefits from a very good materials set. The conductor is nearly pure copper and has a design sheet resistance of $1\text{ m}\Omega/\text{sq}$. The dielectric constant of both the substrate dielectric and the mold compound are in the range of 4. The relationship between these basic values and the natural manufacturing geometries of the laminate production processes allow for very easy design of transmission lines that match the impedance of virtually all semiconductor logic types. The combination of these attributes and the flexibility to tailor the package for the chip to a greater degree than in any other surface mount format makes the plastic ball grid array package an unsurpassed electrical performer.

The combination of electrical and thermal performance options in plastic ball grid arrays will make them one of the most useful surface mount packages introduced to date.

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Thermal and Electrical Management of Plastic BGA Packages—A User's Perspective

David B. Walshak, Jr. and Hassan Hashemi

12.1 Introduction

One of the attributes generally listed by proponents of ball grid array (BGA) packages is their perceived improved thermal performance over conventional quad flat pack (QFP) and pin grid array (PGA) packages. However, these improvements can only be achieved through a system-level approach to thermal performance. Plastic BGAs are similar in construction to plastic pin grid array (PPGA) packages except that where pins are located on a PGA, solder balls are attached on a BGA. Therefore, many of the thermal performance characteristics of BGAs are similar to PPGAs. Due to the shorter traces provided by its fine-line laminate base and to the lack of long pins, the electrical performance of a BGA is generally better than that of the best PPGA.

This chapter describes the important factors affecting the thermal and electrical performance of plastic BGA packages that have been reported in the literature. Wherever possible, comparisons with similar conventional packages are presented. Since this package type is still relatively new to the industry, only a small number of studies have been conducted and published, but the BGA package is currently being scrutinized by a large number of packaging designers and users.¹

12.2 Thermal Management of Plastic BGA Packages

12.2.1 Introduction

Three common types of BGA packages are currently being studied: plastic, ceramic, and tape. The plastic BGAs can be manufactured

more cheaply, but the cheapest of these packages inherently have the poorest thermal characteristics—which may be completely acceptable for many low-power applications. For this reason, when faced with putting a high-performance chip (or chipset) in BGA format, designers have typically pursued ceramic or tape BGAs. Several enhancements have been conceptualized for plastic BGAs to improve their thermal performance and consequently expand their power-operating window. Thermally enhanced plastic BGAs (EBGAs) are also being investigated as a lower-cost alternative in moderate- to high-performance applications. The EBGA packages will be discussed in Sec. 12.2.3, while the thermal aspects of ceramic BGAs and tape BGAs are discussed in other chapters.

In certain “borderline” situations the cost savings of plastic overmolded BGAs must be weighed against the performance attributes of both ceramic and tape BGAs. Just as different package types are compared to obtain the optimum match, the mix of enhancement options provides a large variety of selections, each option with its own cost penalty or benefit. The effects of utilizing some of these performance enhancements should be thoroughly studied to determine the impact on overall system performance and cost.

A schematic showing the major heat-flow paths in a typical BGA package is provided in Fig. 12.1 and a simple one-dimensional electrical analogy to the thermal problem is shown in Fig. 12.2. While the thermal analysis problem is a three-dimensional one, this 1-D schematic shows the associations between the significant factors in the system. The thermal resistances in Fig. 12.2 are discussed in detail later in this section.

The factors affecting thermal performance of the plastic BGA packages may be divided into three main categories, although there is some overlap: materials variables, geometric variables, and environmental variables. Each of these categories is described below, including the important factors for each area.

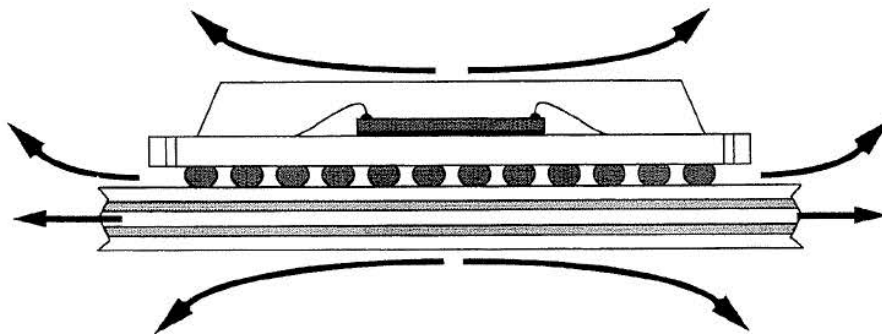


Figure 12.1 Schematic of major heat-flow paths in a typical BGA package.

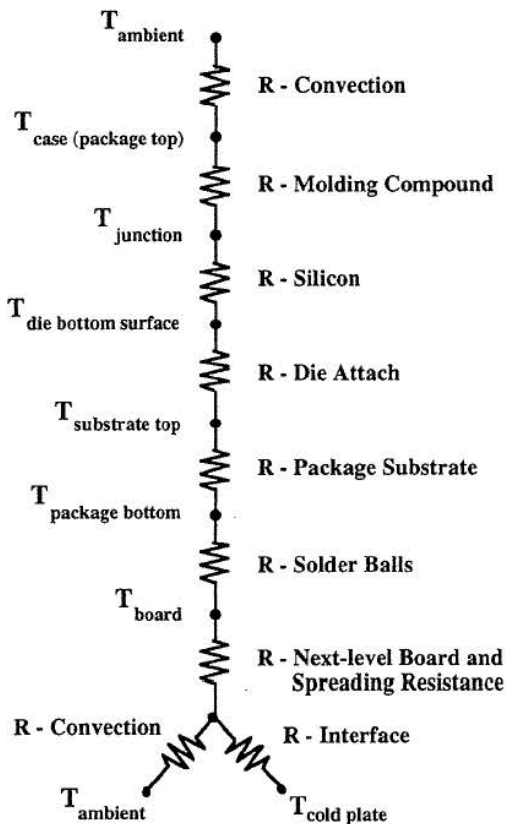


Figure 12.2 One-dimensional electrical analogy to the thermal problem.

12.2.2 Materials variables

From a thermal management perspective, the three major materials variables include the molding compound, the die-attach material, and the substrate dielectric material.

The molding compound completely surrounds the chip, providing mechanical protection as well as a surface for marking the package. Typically, the molding compound is in direct contact with the surface of the chip, although, in some cases, an encapsulation layer may be utilized prior to the overmolding operation. This encapsulation layer (typically either silicon gel or an epoxy) can act as a mechanical stress buffer and can provide additional corrosion protection. Unfortunately, from a thermal point of view, the molding compound thickness over the die surface is typically on the order of 15 to 25 mils, providing a relatively high thermal-resistance path to the top surface of the package. For this reason, most of the attention placed on thermal performance of standard plastic BGAs has been directed toward improving the thermal paths through the package to the external board. One study has been published showing that the mold compound thermal conductivity is of small importance

relative to other packaging variables.² Of course, if an extended-surface heat exchanger were added to the top of an overmolded BGA package, the thermal conductivity of the molding compound (or more correctly, the thermal resistance from the chip surface to the top surface of the package) would be of tantamount importance.

With the current emphasis on through-the-board thermal enhancement, the selection of die-attach material is critical. When thermal vias are incorporated in the package substrate, this material directly couples the silicon chip to the die-attach pad at the top of the thermal via stacks. From a 1-D perspective, the thermal resistance across this layer is directly proportional to the thickness and inversely proportional to the thermal conductivity of the die-attach material. Typically, a silver-filled epoxy is used for the die attach with a thermal conductivity of around 1.9 W/m·K with die-attach layer thicknesses ranging from 1 to 2 mils.

The thermal conductivity of the substrate dielectric material is secondary in importance relative to several design-related variables that are discussed in Sec. 12.2.3. Most plastic BGA users are using a modified polyimide resin-glass (bismaleimide triazine, or BT) as the core for the substrate, while others use polyimide. The thermal conductivities for these materials vary from 0.21 W/m·K for BT to 0.155 W/m·K for polyimide.

12.2.3 Geometric variables

Using materials which are optimized for thermal performance is only one of the tools that package designers have at their disposal. In fact, design-related factors can have an even larger effect on thermal performance than materials-related variables. Several design enhancements have been incorporated into plastic BGAs to improve thermal performance. Some of these enhancements are related to the package substrate design, while others involve making a heat spreader integral to the package. The package designer must observe the thermal performance from a system-level point of view in making intelligent decisions related to package design optimization.

Package size. The “standard” plastic BGA utilizes a double-sided substrate with plated-through-hole vias located around the perimeter of the package for routing the I/O from the chip to the solder balls on the bottom of the package (see Fig. 12.3). This molded plastic package configuration, often referred to as the OMPAC (Over-molded Pad Array Carrier), provides a low-cost, easy-to-manufacture package which is more than adequate for low thermal-performance applications (i.e., less than one watt).

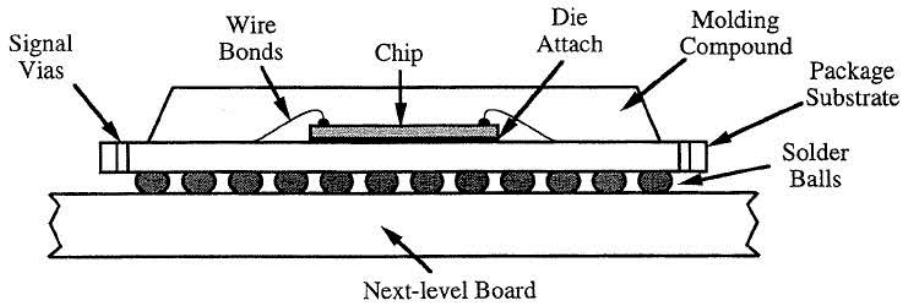


Figure 12.3 Standard plastic BGA package (or OMPAC).

Values quoted for junction-to-ambient thermal resistance, θ_{ja} , for plastic BGAs with no thermal enhancements are presented in Table 12.1. With the package mounted onto a low thermal conductivity board³ (i.e., no thermal vias, no heat-spreading layers, and with a minimum number of traces) and with no forced airflow (i.e., in a natural convection environment) the values for θ_{ja} ranged from 52 to 74°C/W depending on package size. With 1 m/sec forced airflow, the thermal resistances ranged from 38 to 57°C/W. The relationship between θ_{ja} and package size is shown in Fig. 12.4.

Along these same lines for a given size package, a package with a larger chip will exhibit a better perceived thermal performance compared to the package containing a smaller chip. The thermal conduc-

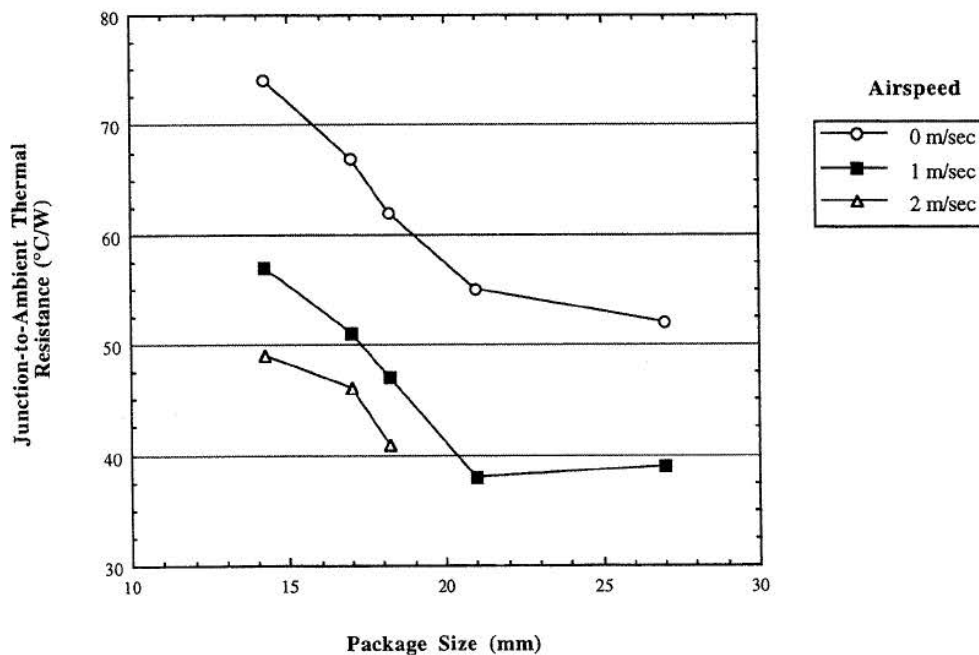


Figure 12.4 Relationship between package size and θ_{ja} for different airspeeds.

TABLE 12.1 Package Comparison of Standard Plastic BGAs with No Internal Thermal Enhancements

Package description	Package size (mm)	Junction-to-ambient thermal resistance, θ_{ja} , ($^{\circ}\text{C}/\text{W}$)		
		Natural convection	Forced convection	
			0 m/sec	1 m/sec 2 m/sec
68 OMPAC ⁴	14.2	74	57	49
86 OMPAC ⁴		67	51	46
106 OMPAC ⁴	18.23	62	47	41
169 BGA ⁵	21	55	38	
225 BGA ⁶	27	52	39	

tivity of the silicon is so much larger than that of the molding compound (149.6 versus 0.7 W/m·K, respectively) or most of the other materials in the package that, from a global perspective, the temperature of the chip will appear much higher and quite uniform relative to the temperature distribution throughout the rest of the package. For two different size chips dissipating the same amount of power, the larger chip will have a lower heat flux (in watts per unit area) than the smaller chip. The larger chip can also provide some of the benefits of a heat spreader because of the higher thermal conductivity of the silicon. In summary, a BGA containing a larger chip will thermally outperform an identical BGA containing a smaller chip.

Thermal test data may also be skewed by power dissipation, especially at low airflows where the buoyancy effect of natural convection is the major heat-transfer driver. Depending upon package design, next-level board layout, and airspeed, the thermal resistance measurements may vary by up to 28 percent simply because of the different powers being dissipated within the package.

The BGA substrate also presents a platform on which more than one chip can be interconnected, providing an overmolded multichip module. The electrical, assembly, and cost benefits of multichip modules have been well-documented. The thermal benefits with a multiple chip BGA are also pertinent due to the heat-spreading attributes inherent in the package simply by having multiple heat sources within the same package.²

In summary, if system-level space allows it, one method of improving thermal performance of BGAs is to increase the package size. A larger package will generally accommodate more solder balls to help spread the heat to the next-level board as well as a larger surface area for improved convective heat transfer. In many situations, the constraints are such that it is the engineer's job to minimize both the size and cost parameters. In fact, smaller package size is a primary reason why

BGAs are being considered for use. For this reason, an alternative to enlarging the package must be pursued.

Package substrate design. The major emphasis on improving thermal performance for plastic PGAs has been on improving the through-the-substrate heat transfer. Two parallel design approaches have been used to optimize through-substrate thermal conduction: using either thermal vias or heat-spreading planes.

When dealing with laminate substrates, thermal vias are simply plated through-holes in the substrate which happen to be located underneath the chip (see Fig. 12.5). In general, the thermal vias are tied together with a rather large copper land on both the top and bottom surfaces of the substrate. The copper land on the top side of the substrate is also used as the die-attach pad. Although the cross-sectional area of copper from the thermal vias is relatively small, the difference in thermal conductivities between the copper and the dielectric is quite large (i.e., 389 W/m·K for copper versus 0.21 W/m·K for BT). Thus, the effective through-substrate thermal conductivity can be dramatically improved by utilizing thermal vias.

The design of the thermal vias can obviously affect the effective through-substrate thermal conductivity underneath the substrate. Compaq has used 0.300-mm (12-mil) diameter thermal vias for two plastic BGA packages considered.⁷ A modeling study was conducted at MCC on these two packages to determine the dependence of through-substrate effective thermal conductivity on several parameters: via pitch, via diameter, and plating thickness.⁸ The net result of this study is that increasing the amount of copper in the cross-section of the via array increases the effective through-substrate thermal conductivity. For example, an array of 12-mil diameter vias on 60-mil pitch plated with ½-oz copper, the predicted through-substrate effective thermal conductivity in the thermal via region is approximately 1.75 W/m·K versus 0.21 W/m·K for BT without thermal vias—an improvement of 833 percent.

The thermal vias aid in getting heat from the top surface to the bottom of the substrate, but, used alone, only in the region directly underneath the chip. In this case, the solder balls directly under the chip must trans-

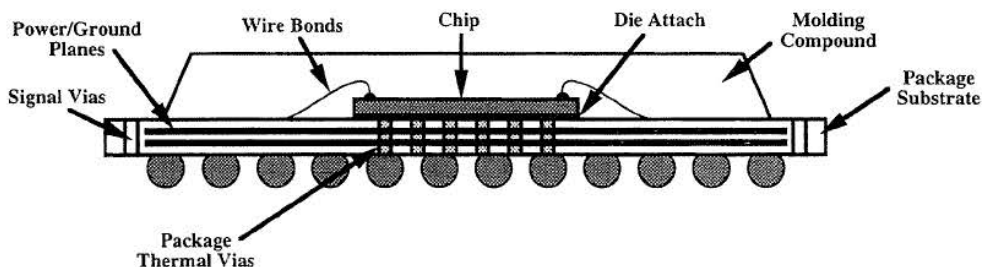


Figure 12.5 Plastic BGA with internal thermal vias and heat-spreading layers.

fer most of the heat to the next-level board. To efficiently utilize the benefits of thermal vias, some method of spreading heat throughout the package must be used.

With an internal heat-spreading layer incorporated into the package substrate, heat can be spread over a larger portion of the package area (see Fig. 12.5). This heat-spreading layer is usually a ground plane that is nearly solid and provides a low-resistance path across the package area. For best results, the thermal vias should be connected directly to the heat-spreading layer. The net effect of tying the thermal vias to this ground plane is that it improves the thermal coupling to the next-level board through the solder balls and also improves the convective heat transfer from the top surface of the package.

These additional layers can be added to the package substrate without significantly increasing the overall package cost. These layers can be used for power, ground, or additional signal planes and can provide opportunities for improved electrical, thermal, and routing characteristics.⁹ The thermal vias occupy a section of the substrate that would normally be used for routing purposes. Again, the system-level tradeoffs must be analyzed to determine the appropriate direction to proceed.

The thermal management strategy currently being used by Compaq is to route all power and ground traces into the center of the package to connect with the thermal vias. This also puts performance-dependent pads on the perimeter of the array, thereby shortening the electrical paths to the next-level board and reducing electrical parasitics.⁷

Thermally enhanced plastic BGAs. Each of the above variables described varying degrees of subtle changes to package design and materials relative to overmolded plastic BGAs. Another approach that has been used to improve the thermal performance of plastic BGAs is similar to incorporating a copper slug in plastic PGAs. This package is usually considered a “cavity-down” BGA or enhanced BGA (EBGA) as opposed to the traditional overmolded plastic BGA. In this approach, the interconnect substrate has a hollow center and usually has multiple tiers to facilitate wire bonding and routing (see Fig. 12.6). Usually the copper slug is adhesively attached to the backside of the substrate, and solder or other electrical connections are made to ensure proper grounding. The chip is then placed in the cavity followed by a die-attach cure cycle. After the wire bonds are formed, the chip is either over-coated or a lid is affixed for mechanical protection. With this package, the bond pad array is not a continuous array, but has omissions in the region occupied by the chip and lid (i.e., the package only has solder balls under the package substrate).

Since the major heat path is through the slug, thermal vias in the substrate are not necessary with this package. From a thermal man-

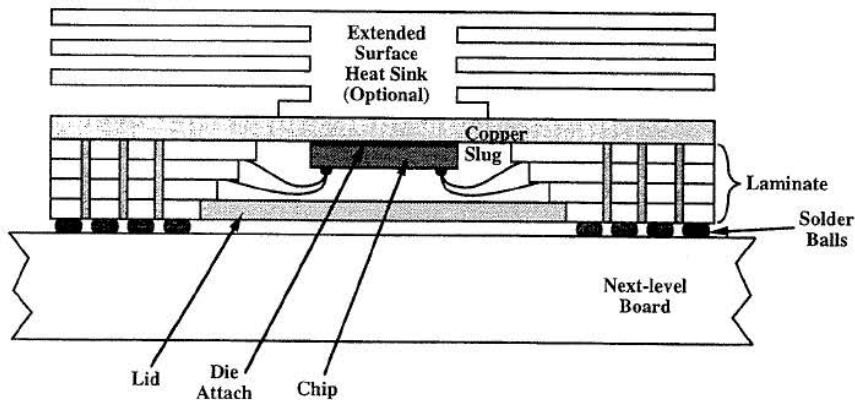


Figure 12.6 Thermally enhanced ball grid array package (EBGA).

agement perspective, if the package is to be used without a heat sink, the slug should be made as large as possible. This ensures good heat spreading for the package and also provides a larger surface area which enables more efficient convective heat transfer. The EBGA package also allows for a heat sink to be attached to the package top with a relatively low junction-to-case thermal resistance path.

Unfortunately, very little thermal work has been published regarding these enhanced BGA packages. Figure 12.7 shows some results generated by Amkor comparing a 169-I/O BGA in different package configurations. The thermal resistances show the dramatic potential of this thermally enhanced package.⁵

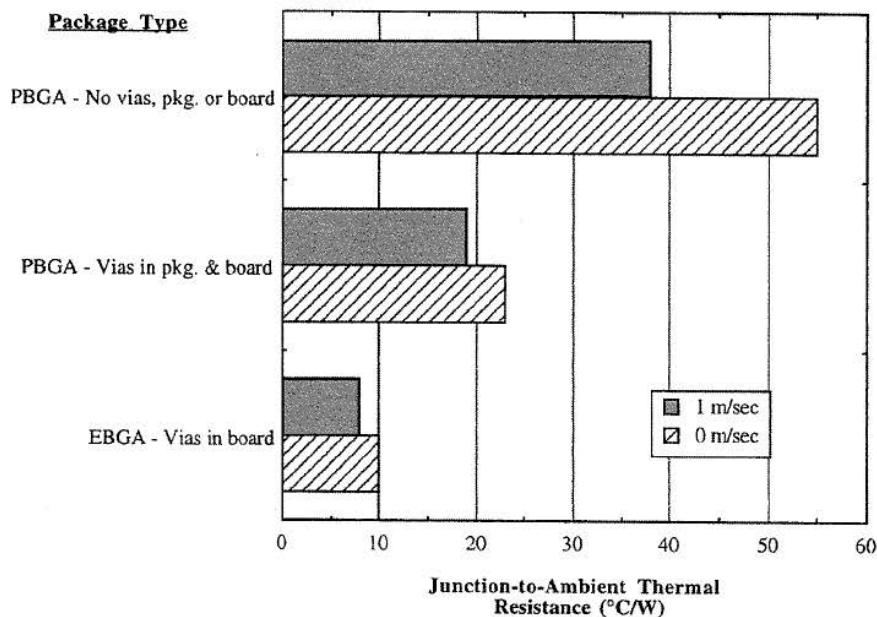


Figure 12.7 Comparison of two different PBGAs with an EBGA at 0 and 1 m/sec airflow.

12.2.4 Environmental variables

While most thermal testing is performed in controlled, specified environments, the application- or system-level environment is where the thermal performance of any package is most critical. The degree to which the operating environment can have an effect on the perceived thermal performance of BGA packages is presented and the major factors are identified in this section.

System-level cooling approach. Several options are available for the packaging engineer to remove heat from a package. Usually, these cooling decisions are made at the system level and are specified to the device engineers as requirements. The optimum design of a BGA package for any situation will depend upon which system-level cooling strategy is to be employed.

In many consumer, telecommunication, and portable products, system power, size, and/or noise restrictions prevent forced-air convection from being utilized as a cooling method. In this situation, the heat must be either removed from the package by conduction or by natural convection from the package and board surface.

Natural, or free, convection is a result of the motion of air due to density changes arising from the heating process. As the air in proximity to a hot surface heats up, its density decreases. This change in density imposes buoyancy forces on the air, resulting in upward movement of the air.¹⁰ Even so, this movement of air is typically much less than 0.25 m/sec. Thus, the major vehicle for cooling these products requires conducting the heat to the outside surface of the product.

In contrast, the power dissipated in many workstations and other computer applications requires some form of forced convection to cool the electronics. Typical airspeeds used in these applications range from 0.25 m/sec up to 3 m/sec. To improve the heat transfer from an electronic package, a heat sink may be attached to the top surface of the package with a high thermal conductivity material, usually either a metal-filled epoxy or an adhesive film. The enhanced BGAs with their copper slugs are the most likely candidates for utilizing a heat sink.

External board design. Since the most efficient thermal path for a BGA package is through the substrate to the next-level board, another method for removing the heat from the package is by optimizing the conduction path to this next-level board.

The effective thermal conductivity of the next-level board can have a dramatic effect on the package thermal resistance.¹¹ The design of the next-level board can be modified in many ways to improve the thermal performance of BGAs. As mentioned previously, several designers have used thermal vias in the package substrate to provide a lower thermal

resistance path through the substrate. These thermal vias are usually located underneath the chip and many times are shorted to either the power or ground planes in the substrate. The solder balls in the center of these packages are typically connected to these package thermal vias. For best results, the mating bond pads on the next-level board should be connected to thermal vias in the board, which are in turn connected to power or ground planes in the board.

Using the next-level board's ground plane is an excellent method for cooling BGAs. System-level designers may find it best to place the BGA packages close to the edge of the next-level board so that heat can be carried away easily.¹² In comparing the presence or absence of ground planes in the next-level board, Compaq has reported thermal-resistance improvements of up to a factor of two by having a ground plane. An additional ground plane tended to reduce the thermal resistance measurements by another 5°C/W.⁷

Again, the package designer must balance improvements in thermal performance with overall system benefits and costs. For example, it may be easy to aggressively assign too many solder balls to power or ground for better thermal coupling to the next-level board. Unfortunately, this action can also limit the number of solder balls available for the I/O. Another concern for the designer is to ensure that not too many closely spaced packages are dependent on the system (or next-level board) ground plane to provide heat conduction away from these packages. Although this potential problem should be manageable in most situations, it must be evaluated at the system level and could affect the overall cooling strategy.

12.3 Electrical Management of Plastic BGAs

12.3.1 Introduction

The electrical performance issues for plastic ball grid array (PBGA) packages are discussed in this section. First the electrical parameters that affect the package performance are briefly reviewed, and then the typical values of these parameters for conventional PBGAs and enhanced BGAs are listed. Some comparisons between quad flat package (QFP) and pin grid array (PGA) electrical performance specifications and BGAs are also included in these discussions.

Many concerns about BGAs have been raised regarding package reliability and thermal performance, but even less published data is available regarding the electrical performance of these packages. However, the simplicity of the conventional single-layer OMPAC-like BGAs allows one to use back-of-the-envelope closed-form equations to arrive at first-order electrical parameters. In the meanwhile, the construction of enhanced BGAs is very similar to cavity-down plastic pin grid arrays

(PPGAs) and there have been numerous publications on their electrical performance. The main difference between enhanced BGAs and PPGAs is that the 3-mm pins are replaced with 0.8-mm to 0.9-mm solder bumps.

As mentioned earlier in Sec. 12.2 there are several configurations of PBGAs. The first-level interconnection between the chip(s) and the BGA substrate can be direct-chip attached (DCA), tape automated bonded (TAB), or wire-bonded. The overall performance in this case is dependent on the overall net length, conductor geometry, and the location of current return path. For example, in the simplistic OMPAC-like layout, the conductor traces are routed to the periphery of the top layer and through a host of through-hole connections for connection to the redistribution bottom layer. A typical net from the IC chip to the next layer interconnect board (see Fig. 12.8) consists of a wire bond, substrate conductive trace (top-layer), through-hole via, redistribution conductor layer, and the solder bump. In the enhanced face-up configuration, a pair of power and ground planes could be designed into the interconnect substrate to allow for lower inductance net and more controlled signal propagation characteristics.

12.3.2 Electrical analysis methodology

The electrical analysis of a package needs to be addressed from a system's point of view to fully appreciate its performance effects. However, in this chapter, a very simplistic approach has been taken to discuss the typical electrical parameters of PBGA packages. While the methodologies may vary, these characteristics are derived from the same fundamental set of circuit parameters (i.e., resistance, inductance, capacitance—*RLC*). Separate measurements or modeling techniques may be used to indepen-

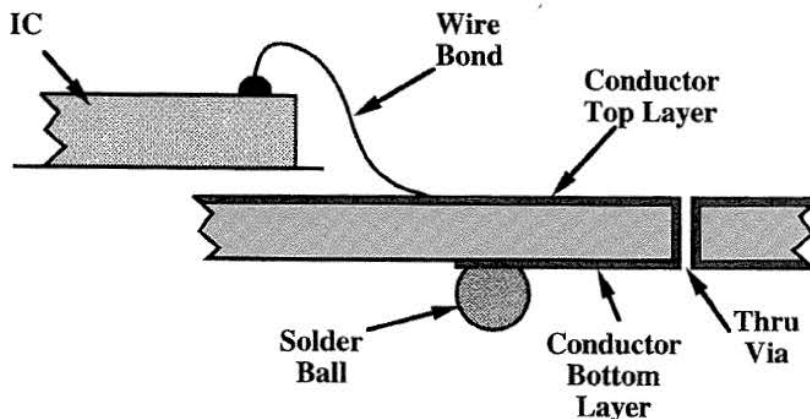


Figure 12.8 A typical net connection in a PBGA which consists of a wire-bond connection from an IC to the BGA substrate, the conductive trace along the substrate, and the solder ball.

dently confirm the listed data. The PBGA package performance needs to be studied from two points of view: signal fidelity and power distribution integrity. Signal fidelity is analyzed in the context of propagation delay and crosstalk noise, while power distribution integrity is discussed from inductance of power network and how it can be minimized in a PBGA design.

Three electrical parameters—resistance, capacitance, and inductance—are always present in packaging and interconnect systems. Resistances can cause DC drops on signal lines and contribute to RC charging delays, both of which are unwanted effects. Resistances, however, often help to dampen unwanted noise in systems. Capacitance is the primary cause of delays in packaging and interconnect systems. Capacitive loading of signal lines is decreased by reducing net lengths. Finally, inductance contributes to switching noise and time-of-flight delays in packaging systems. These basic circuit parameters define the signal fidelity in a BGA package and contribute to the overall power distribution integrity. The definitions for each term affecting the electrical performance of a typical plastic BGA package follow, and the predicted values of these parameters for a 225 I/O BGA are summarized in Table 12.2.

Propagation delay. Propagation delay is the time delay for a signal edge to propagate along a given length of interconnect, measured at the 50 percent signal transition level. In digital signal transmission applications, propagation delay is perhaps the most significant composite characteristic. Many factors contribute to the propagation delay of a signal along a trace. Different components to the propagation

TABLE 12.2 Typical Package Features and Electrical Parameters Comparing a 225-I/O BGA with a 208-I/O QFP Package²

Attribute	225 I/O BGA	208 I/O QFP
Size (mm ²)	27 × 27	31 × 31
Pitch of out lead (mm)	1.5	0.5
Shortest lead (mm)	6.8	10.2
Longest lead (mm)	22.5	13.7
Smallest L (nH)	3.3 to 5.8	6.3 to 7.1
Largest L (nH)	10 to 11.2	8.9 to 9.8
Inductive coupling (K_L)	0.12 to 0.25	0.68 to 0.70
Z_0 (Ω)	60 to 85	—
Delay (psec)	5.02 to 9.07	9 to 14.5
Capacitance (pF)	1.28 to 1.31	1.61 to 2.38
R_{DC} (m Ω)	20 to 24	70 to 80
ΔI -noise (mV)	550	730
Crosstalk (mV)	90	510

NOTE: This data corresponds to the packages only and no chip-to-package interconnect data is included.

delay, ranked in decreasing order of their importance, are time of flight, RC charging, and delays associated with noise (including reflections, crosstalk, and switching noise). The packaging delay depends not only on the length of the nets but also the distribution of loads on the nets, the size of the loads, and the characteristics of the circuits driving the nets. Finally, the signal delay varies as a function of frequency—at slower frequencies the RC charging delays dominate, and at high frequencies the time of flight ($\sqrt{LC}$) dominates the delay.¹³ The speed of signal propagation is inversely proportional to the square root of the dielectric constant (ϵ_r) of the dielectric medium. For typical laminate materials used in PBGA substrates (with $3.5 < \epsilon_r < 4.9$) a delay of 62 to 74 psec/cm is expected.

Crosstalk. Crosstalk is defined as the coupled noise from active lines onto quiet lines due to mutual capacitive and inductive coupling. Crosstalk increases as the distance between lines (pitch) decreases, the distance between the lines and their circuit return path (ground plane, for example) increases, and the length of their close proximity (coupled length) increases. Coupled transient analysis of transmission lines can be used to simulate the crosstalk noise. Capacitive coupling ($K_C = -C_m/C_s$) and inductive coupling ($K_L = L_m/L_s$) between adjacent lines add at the driving end and subtract at the far end of the line. C_m and L_m are the mutual capacitance and mutual inductance between adjacent leads, respectively. Likewise, C_s and L_s are the self-capacitance and self-inductance of an active signal line, respectively. A low dielectric constant material is desired for reducing the effective crosstalk in a PBGA package. Alternatively, inclusion of a ground trace between adjacent signal lines reduces the crosstalk by approximately 50 percent. Critical nets can be designed in a stripline format by taking advantage of an internal power or ground plane. This allows PBGA packages to be used for very high end applications which demand low crosstalk.

Switching noise. A switching event causes current change in the supply network which delivers energy to the chip. When this transient current is passed through a power distribution network, a noise voltage is produced, which is referred to as switching, or delta-I, noise. Power distribution systems represent a source of coupling between the circuits that depend on characteristic impedance of the distribution system. The magnitude of the noise voltage depends on the current slew rate and the amount of inductance in the current path as shown in Eq. (12.1). The duration of the noise disturbance depends primarily on the impedance of the power distribution network. Switching noise limits the achievable system performance and can induce a number of significant problems in digital systems if it is not handled correctly.

The transient noise generated by simultaneous switching of n output drivers is expressed by

$$\delta v = \frac{L n \delta i}{\delta t} \quad (12.1)$$

where δv = amplitude of noise

L = inductance of interconnect

δi = current demand per driver at the time of switching

δt = rise (fall) time of the signal

Switching (or ΔI) noise for conventional PBGAs is approximately 10 percent of the swing voltage. Conventional single-layer PBGAs inherently have some long routing paths which result in highly inductive traces. In this case, the allocation of power and ground pads is essential to minimize the overall net (trace) length which would in turn allow small switching noise voltage in the power distribution network.

First-level interconnect concerns. The first-level interconnect between an IC and the PBGA substrate is generally through gold-wire bonding. However, solder flip-chip bonded parts are also used in ≤ 169 I/O BGA packages. Flip-chip bonding offers the shortest interconnect lengths and highest signal fidelity. The mutual coupling between the interconnects is small due to very short electrical paths. Typical solder bumps may be 150 to 200 μm in diameter. Wire bonds introduce a transmission discontinuity for the signals traversing the integrated circuit boundary. The inductance of thin wires, of diameter 0.025 to 0.032 mm (0.001 to 0.00125 inches) and length 1.9 to 2.5 mm (0.075 to 0.100 inches), is on the order of 2 nH. Wire bonding can be performed down to a wiring pitch of 0.1 mm (0.0045 inches). The inductive mutual coupling between the wires is significant (1 nH cumulative mutual inductance and 1 pF of mutual capacitance). The inductance terms scale logarithmically with distance, so their coupling values do not drop very rapidly as one moves away from a signal line. It is necessary to have ground wires placed among every few signal wires in order to keep the crosstalk within reasonable bounds.

Effect of BGA design on electrical performance. The electrical parameters of a 225 I/O BGA package are given in Table 12.2. In the single-layer implementation of a BGA (e.g., Motorola OMPAC design), a metal layer for routing is located on both the top and bottom sides of the substrate. These two metal layers are electrically connected through vias at the perimeter of the substrate and there are no metal layers inside the substrate. There usually is a die attach pad that may have a host of thermal vias connecting it to the bottom layer of the substrate.

Inductance of a package may be the single biggest factor affecting the overall performance of a BGA package, especially in a high-frequency (≥ 50 MHz) system. High-frequency inductance measurement of a 225 I/O OMPAC shows that the longest trace has an inductance of nearly 11 nH, and the shortest trace's inductance is 1 nH with ≈ 51 percent of all the traces having an inductance of ≤ 6 nH.

12.3.3 PBGA Performance Comparison versus QFP

The results of a comparison between a 208-lead quad flat package (QFP) and a 225-I/O PBGA are presented in Table 12.2.² Neither the QFP nor the PBGA in this study has any type of electrical enhancement such as built-in voltage planes in the package structure. The data in Table 12.2 shows that the PBGA has a smaller per unit inductance than the corresponding QFP package.

The BGA package, even in its simplest configuration (i.e., single-layer OMPAC), exhibits very favorable electrical performance specifications. Due to the circuit structure of the conducting traces (see Fig. 12.9), each conductive trace is partly routed on the top side and partly routed on the bottom side of the substrate. Therefore, the two segments of the same trace have close coupling.

The overall inductance of a given trace is determined by Eq. (12.2):

$$L_{tot} = L_1 + L_2 - 2M_{12} + L_{VIA} \quad (12.2)$$

where L_1 corresponds to the inductance of the top-layer conductor, L_2 is the inductance of the bottom-layer conductor, M_{12} refers to the mutual coupling between the two segments, and L_{VIA} is the inductance of the through-hole via.

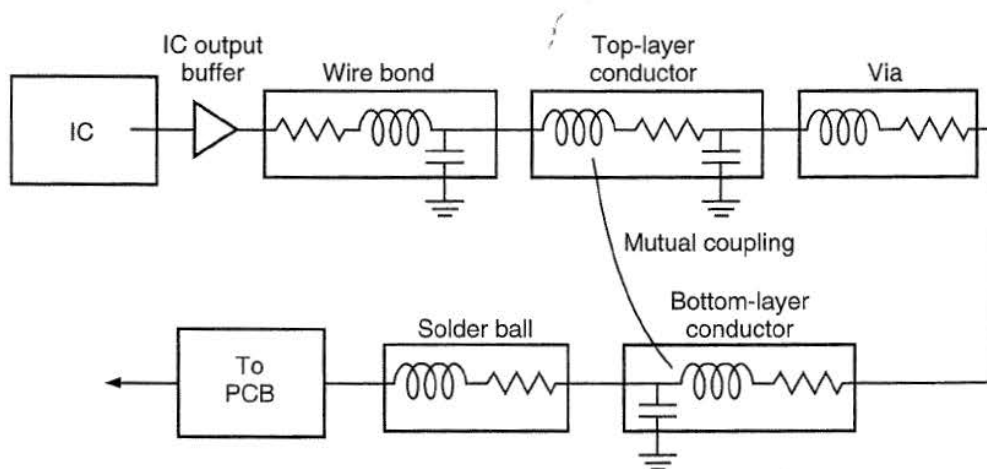


Figure 12.9 An equivalent circuit model corresponding to a typical net in the PBGA illustrated in Fig. 12.8.

In an outgoing signal, the current flows outward along the top-layer conductor, and flows inward along the bottom-layer conductor. Due to opposing magnetic fields generated by the two different current flows, the overall conductor inductance is reduced. The stronger the coupling between the top-layer conductor and the bottom-layer conductor, the larger the M_{12} term [Eq. (12.2)] and the smaller the L_{tot} term will be. Motorola has shown that if the traces were to be simply routed directly from a bonding pad on the top layer through a via to the bottom layer and routed to the solder bump, the overall net length would be one-third of the conventional routing and the inductance would be less than one-fourth the inductance in the conventional case.¹⁵

Mutual inductive coupling between adjacent lines is primarily a function of geometry, but it is also affected by the magnetic fields due to nearby signals. The coupling between the top-layer component of one signal trace and the bottom-layer component of another signal trace causes opposing magnetic fields that partially reduce the coupling between adjacent traces on the same layer. The manufacturable substrate design rules also dictate the routing limitations between the solder pads, thus minimizing the number of adjacent traces running in parallel with one another, which effectively reduces the overall coupling length.

In cavity-up (chip face-up) BGA configurations with built-in power and ground planes, the signal routing on the top layer to a periphery and redistribution on the bottom layer may not change. However, the electrical parasitics are substantially different due to the presence of such voltage planes. Referring to Eq. (12.2), the self-inductance terms L_1 and L_2 are much smaller (microstrip line or buried microstrip line with a solder mask) as the current return path is across a very low-inductance plane. Compaq has reported that the loop inductance of the ground or power path in a 225-I/O BGA package with built-in planes is 130 to 170 pH, respectively.⁹

In the enhanced BGA configurations, a through-hole via is placed near a bonding pad routing the signal through a very short path from the IC to the solder bump. In this case, the overall net inductance is reduced simply by shortening the net length. BGA packages with 300 to 500 I/O are under considerations that are geared for 100- to 200-MHz computing applications. The enhanced BGA packages with solder balls on 1.27-mm or 1.5-mm pitch simply allow multiple voltage and signal planes to be laminated in a donut-shaped laminate structure where all the traces are routed in a controlled-impedance manner. For the very high end processors with sub-nanosecond edge rates, the ball pitch of 1.27 mm is being used to minimize the overall substrate size. This way the microstrip or stripline structures are very short and package parasitics are minimized. When 32- or 64-bit wide drivers

switch simultaneously and cause significant switching noise problems, the low inductance of the enhanced BGAs simply minimizes these effects.

12.4 Summary

Overmolded plastic BGAs are being touted as a low-cost, easy-to-manufacture, and easy-to-implement package. With no additional cost-related requirements, they fit very well in many low-power, high-I/O applications. As device engineers explore using these packages for their high-performance applications, the thermal limitations of these overmolded BGAs are quickly encountered.

With little cost penalty, users of plastic BGA packages have been able to substantially increase the thermal performance of this class of packages by optimizing the package and next-level board design. Package modifications include the intelligent design of vias and power and ground planes to serve as centralized thermal vias with heat-spreading layers. By coupling a BGA with thermal vias to a next-level board that also has thermal vias and heat-spreading layers, additional improvement is made to the overall thermal performance.

Another approach is being investigated that dramatically improves thermal performance. By incorporating a copper slug into the package and mounting the chip directly to this slug, the thermal resistance from the chip to the outside of the package is minimized. These enhanced BGAs should be able to dramatically increase the power capabilities of this class of package, especially with the addition of a heat sink.

Of course, each of these package improvements comes with a cost increase, which must be considered early in the product-design cycle.

In general, the electrical performance of PBGA packages, like any other semiconductor package type, needs to be studied from a system point of view. The PBGA construction allows the use of this family of semiconductor packaging from the low-end consumer electronics to the very high-end computing machines with 100- to 200-MHz processors. In an isolated one-to-one comparison, a single-layer PBGA has similar or better performance than a comparable leadcount QFP. The packaging technology choice has a very strong effect on delay and noise, and simulation and modeling are needed to accurately predict the performance of a PBGA in a system. Nevertheless, the PBGA electrical performance can be improved significantly by optimizing the layout of the module with the intent of shortening the overall trace length. PBGAs with built-in power and ground planes have better electrical performance than conventional single-layer PBGAs and, to maximize their performance, the signal routing should be optimized. Finally, the

enhanced BGA packages with solder balls on 1-mm or 1.27-mm pitch are suitable packaging options for advanced personal computers and workstation applications.

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