

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,

Petitioner,

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,

Patent Owner.

Case No.: IPR2024-00791
U.S. Patent No. 10,937,806

**PATENT OWNER'S RESPONSE
UNDER 37 C.F.R. § 42.120**

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TABLE OF AUTHORITIES

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LIST OF EXHIBITS

Exhibit	Description
Ex. 2001	Joint Claim Construction Statement
Ex. 2002	Micron’s Preliminary Claim Constructions
Ex. 2003	YMTC’s Proposed Claim Constructions
Ex. 2004	February 19, 2025, Declaration of Dr. Yang (“Yang”)
Ex. 2005	File History of U.S. Patent No. 10,658,378 B2 to Tao et al.
Ex. 2006	Deposition Transcript of Dr. Lee
Ex. 2007	U.S. Patent No. 10,559,583 B2 to Park et al. (“Park”)

LIST OF ABBREVIATIONS

Abbreviation	Term
'806	U.S. Pat. No. 10,937,806
'806FH	File History of U.S. Pat. No. 10,937,806
'378	U.S. Pat. No. 10,658,378
Challenged Claims	Ex. 1001, Claims 8-9, 11-12
DI	Decision Granting Institution for <i>Inter Partes</i> Review of U.S. Patent No. 10,937,806 (IPR2024-00791, Paper 11)
Office	U.S. Patent and Trademark Office
Petition or Pet.	Petition for <i>Inter Partes</i> Review of U.S. Patent No. 10,937,806 (IPR2024-00791, Paper 1)
Parallel district court litigation	<i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc.</i> , NDCA-3-23-cv-05792 (N.D. Cal.)
Patent Owner or PO	Yangtze Memory Technologies Co. Ltd.
Petitioner	Micron Technology, Inc.
POSITA	Person of ordinary skill in the art
Toyama	U.S. Patent Publication No. 2017/0179026

I. INTRODUCTION

The references in Petitioner’s Grounds fail to disclose or render obvious the Challenged Claims of U.S. Patent No. 10,937,806 (“’806,” Ex. 1001). The first and second Grounds rely on two embodiments of the same reference and fail to disclose or render obvious at least limitation [8.g]: “a through array contact (TAC) region formed between the first and second channel regions, wherein the TAC region comprises a plurality of through array contacts (TACs) extending vertically through the dielectric structure.” The remaining Challenged Claims (9 and 11-12) depend from claim 8. The third Ground attempts to combine the two embodiments in Grounds 1 and 2, but fails to show that a POSITA would have made such a combination. The first and third Grounds additionally fail to disclose or render obvious “a plurality of non-electrically functional channel structures surrounding the TAC region” as required by limitation [8.h].

The ’806 is directed to a novel three-dimensional (3D) memory device having through array contacts (TACs) and methods related to manufacturing such a device. As memory cells are scaled down and the density of memory cells increases, it becomes challenging to collect and route signals to the peripheral circuitry efficiently. The ’806 provides a solution by forming TACs in a dedicated region where they provide vertical interconnects to the peripheral devices. ’806, 1:24-36, 2:24-26, 5:52-56, 11:8-14, 19:59-64. By forming this TAC region within a dedicated

dielectric structure, the '806 simplifies the fabrication process, improving yield and lowering costs. The '806 also improves performance by locating the TAC region between two channel regions of a memory device. '806, Figs. 1A-B, 2, Claim 8.

The '806 introduced a 3D memory device in which TACs “extend vertically through” the “dielectric structure,” which hosts a “TAC region” that is between “first and second channel regions” of the memory device. '806, Abstract, 10:62-64, Figs. 1A-B, 2, Claim 8. The claimed invention recites “a dielectric structure extending vertically through the alternating conductor/dielectric layer stack,” “first and second channel regions comprising first and second pluralities of channel structures, respectively,” and “a through array contact (TAC) region formed between the first and second channel regions.” *See* '806, Claim 8. As a result, the claimed invention avoids the issues arising from forming TACs through alternating dielectric/conductor stacks and “simplif[ies] the fabrication process and reduce[s] the fabrication cost.” '806, 18:41:46.

The Petition fails to establish that any of the Challenged Claims is disclosed or rendered obvious. Specifically, Petitioner sets forth three deficient obviousness grounds challenging '806 independent claim 8 and its dependent claims 9 and 11-12: Ground 1) Toyama's (Ex. 1005) “second modification of the fourth exemplary structure” (“Second Modification”); Ground 2) Toyama's “First Exemplary Structure;” and Ground 3) a modification of Toyama's Second Modification based

on Toyama's First Exemplary Structure. Petitioner does not assert that any of the cited references anticipates the Challenged Claims, and instead raises obviousness based on a mix of improper legal principles, faulty analysis, and pure hindsight.

Petitioner's arguments under Ground 1, which rely on Toyama's Second Modification, fail to meet multiple requirements of independent claim 8. First, Petitioner's argument directly contradicts binding Federal Circuit precedent. The claims require "a **plurality** of through array contacts (TACs) extending vertically through **the dielectric structure**" (limitation [8.g]), but Petitioner's arguments instead rely on multiple dielectric structures—each with its own TAC. Consistent with the Federal Circuit's decision in *Finjan LLC v. SonicWall, Inc.*, multiple TACs must extend through the same dielectric structure—extending through different dielectric structures does not satisfy the limitation. 84 F.4th 963, 974-975 (Fed. Cir. 2023). Second, Toyama's Second Modification does not disclose or render obvious "**a plurality of non-electrically functional channel structures surrounding the TAC region**" (limitation [8.h]) because Toyama's alleged non-electrically functional channel structures do not surround the alleged TAC region. The claimed TAC region must include a plurality of TACs, but the alleged non-electrically functional channel structures at most surround one single TAC in Toyama.

Petitioner's Ground 2 relies on Toyama's First Exemplary Structure, which lacks the claimed TAC region between two channel regions because the alleged TAC

region is placed on one side of the device. Realizing the deficiencies of Toyama's First Exemplary Structure, Petitioner proposes putting two devices next to each other in a repeating pattern, but Petitioner's modification adds a second memory device with a second channel region, rather than the claimed memory device with two channel regions. In addition, Petitioner ignores that such a modification would eliminate the peripheral circuitry that is already in that location according to Toyama.

Finally, Ground 3 relies on a modification of Toyama's Second Modification based on Toyama's First Exemplary Structure's unitary dielectric fill material. Petitioner's proposed modification replaces a path used for current flow with a large insulator (a block of dielectric fill material). A person of ordinary skill in the art would not have made this proposed modification, which is instead improperly driven by hindsight. In addition, Ground 3 relies on the same alleged non-electrically functional channel structures as Ground 1, and thus Ground 3 fails to disclose or render obvious ***“a plurality of non-electrically functional channel structures surrounding the TAC region”*** (limitation [8.h]) for the same reason as Ground 1.

Because Toyama’s teachings, individually or combined, fail to disclose or render obvious any of the Challenged Claims, the Board should find in favor of Patent Owner and uphold the validity of all Challenged Claims.¹

II. THE CLAIMED INVENTION OF THE ’806 PATENT

The claimed invention of the ’806 is directed to a “three-dimensional (3D) memory device” and related methods that address issues arising from the fabrication techniques known in the prior art and, as a result, “simplif[y] the fabrication process and reduce[] the fabrication cost.” ’806, Abstract, 18:41-46. Yang, ¶31.

Specifically, the ’806 is directed to an improved 3D memory device and methods for forming such a device in which “through array contacts (TACs)” “extend vertically through” the “dielectric structure,” which hosts a “TAC region.” Ex. ’806, Abstract, 6:17-20, 10:61-63, 21:20-28. 3D memory devices in the prior art at the earliest claimed priority date of the ’806 involved through array vias that form connections between various components of the device to reduce size and increase density. ’806, 1:24-36. These vias were placed within the alternating

¹ This Patent Owner Response is supported by the declaration of Dr. Yang. *See* Ex. 2004 (“Yang”), ¶¶1-30. All emphasis and color annotations have been added unless otherwise noted.

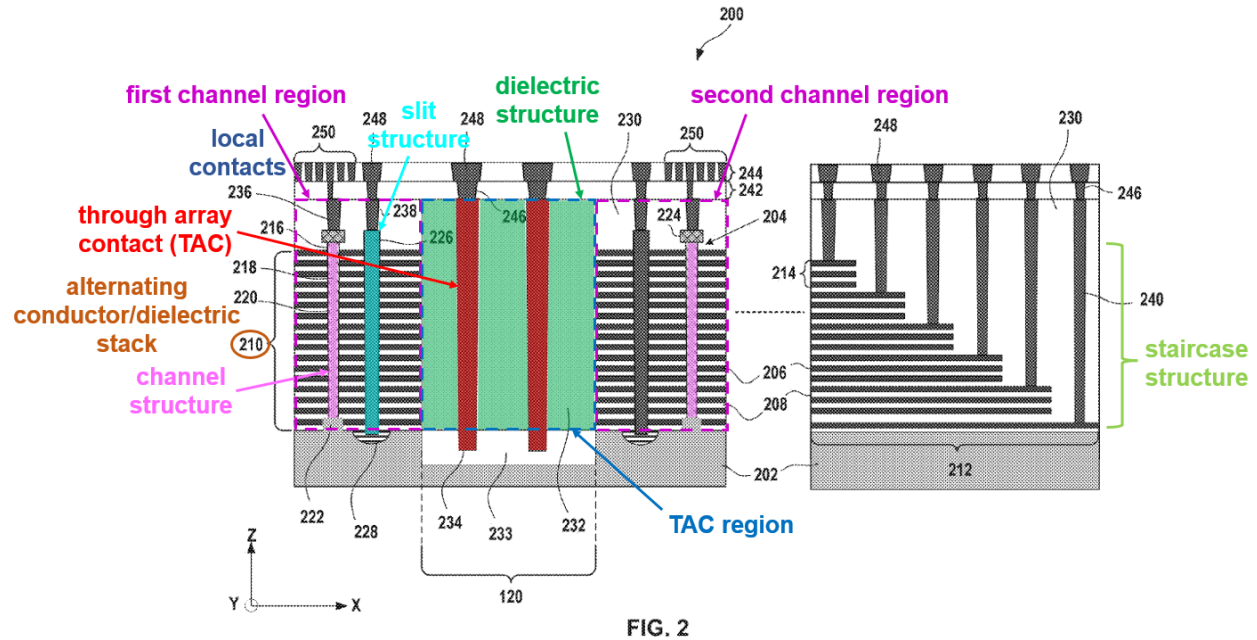
dielectric and conductive layers, which required a complex etching process and “increase[d] the fabrication cost.” ’806, 10:61-11:4. Yang, ¶32.

The novel device the ’806 teaches and recites in the Challenged Claims is characterized by **TACs** that “extend vertically through” the “**dielectric structure**” and are positioned within a “**TAC region.**” ’806, Abstract, 6:17-20, 10:61-63, 21:20-28, Claim 8. The **TAC region** can be between “**first and second channel regions**” comprising “**channel structures.**” *Id.* This novel configuration of elements allows for easier and less costly manufacture of 3D memory devices and achieves shorter interconnect routing. ’806, 5:61-65, 11:8-10, 18:32-38, 20:33-41. Yang, ¶33.

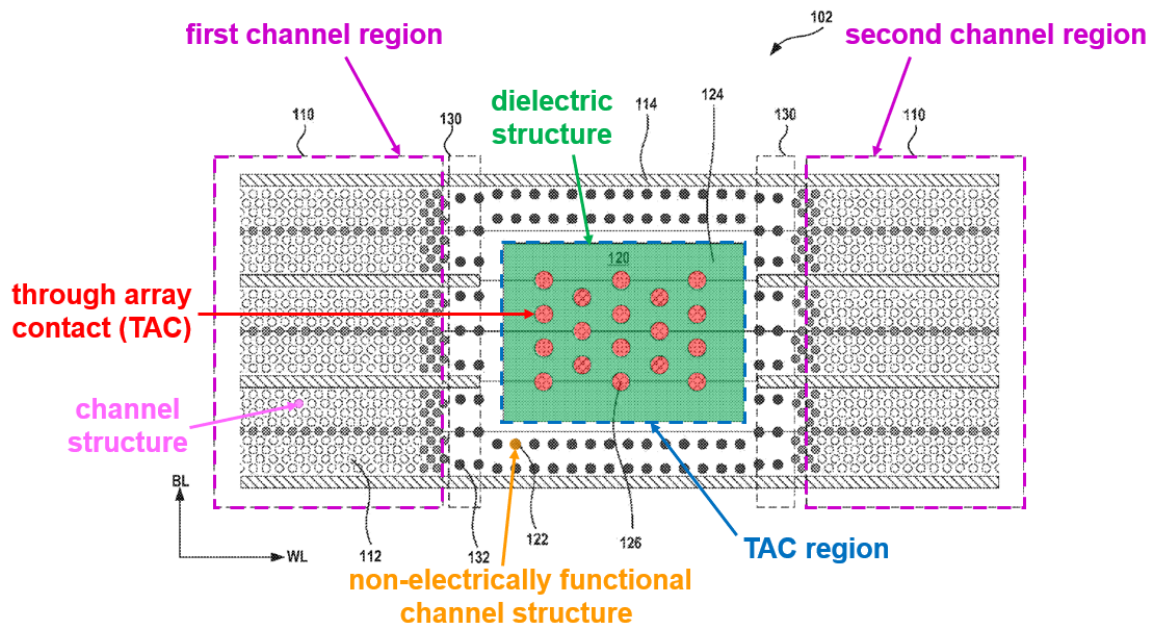
A representative embodiment of the ’806’s memory device includes: (1) “**alternating conductor/dielectric stack 210**” (’806, 8:23-31); (2) “**dielectric structure 232**” (’806, 10:23-34); (3) “**channel structures 216**” and “**slit structures 226**” extending vertically through “**alternating conductor/dielectric stack 210**” (’806, 9:7-12, 10:6-11); (4) “**staircase structure 212**” (’806, 8:54-61); (5) “**local contacts**” on “**channel structures 216**” and “**slit structures 226**” (’806, 9:7-12, 11:20-34); (6) “**TACs 234**” extending vertically through “**dielectric structure 232**” (’806, 10:62-64, 20:49-52); (7) “**first and second channel regions**” and a “**TAC region 120**” between them (’806, 6:4-11, Fig. 2, Claim 8); and (8) “**non-electrically functional channel structures 122**” surrounding the “**TAC region 120**” and

between “**first and second channel regions**” (’806, 6:22-29, Fig. 1A, Claim 8).

Vertical and horizontal cross-section views of the memory device are below.



’806, Fig. 2 (annotated).



’806, Fig. 1A (annotated). Yang, ¶¶34-35.

The only independent claim of the Challenged Claims, claim 8, is directed to aspects of the above-described invention:

[8.pre] A three-dimensional (3D) memory device, comprising:

[8.a] an alternating conductor/dielectric layer stack;

[8.b] a dielectric structure extending vertically through the alternating conductor/dielectric layer stack;

[8.c] first and second channel regions comprising first and second pluralities of channel structures, respectively;

[8.d] slit structures extending vertically through the alternating conductor/dielectric layer stack;

[8.e] a staircase structure disposed in the alternating conductor/dielectric layer stack, wherein the staircase structure comprises levels with each level having a conductor layer thereon;

[8.f] local contacts disposed on the first and second channel structures and the slit structures;

[8.g] a through array contact (TAC) region formed between the first and second channel regions, wherein the TAC region comprises a plurality of through array contacts (TACs) extending vertically through the dielectric structure; and

[8.h] a plurality of non-electrically functional channel structures surrounding the TAC region and between the first and second channel regions.

III. FILE HISTORY

The claims of the '806 remain patentable over the prior art for at least the same reason identified during prosecution. As discussed further below in §§VII-IX, the prior art does not disclose or render obvious, *inter alia*, the '806 claim element “a through array contact (TAC) region formed between the first and second channel regions, wherein the TAC region comprises a plurality of through array contacts (TACs) extending vertically through the dielectric structure.” Claims directed to these limitations were allowed after thorough prosecution and consideration of numerous prior art references.

The '806 was filed on May 5, 2020, as a continuation of application no. 16/047,182, filed on July 27, 2018, which was issued as U.S. Patent No. 10,658,378 (“’378”). The application included 3 independent claims (pending claims 1, 9, and 15) and 17 dependent claims (pending claims 2-8 that depended from pending claim 1, pending claims 10-14 that depended from pending claim 9, and pending claims 16-20 that depended from pending claim 15). Ex. 1002, 53-55 (05/05/2020 Claims). Yang, ¶¶36.

In a non-final office action, the Examiner rejected pending claims 1-16 and 18-20 under 35 U.S.C. § 103 as being allegedly obvious over U.S. Patent No.

9,659,956 (“Pachamuthu”) in view of U.S. Patent Publication No. 2017/0186758 (“Lee”), and rejected pending claim 17 under 35 U.S.C. § 103 as being allegedly obvious over these two references in further view of U.S. Patent Publication No. 2017/0365613 (“Gunji-Yoneoka”). Ex. 1002, 104-112 (06/23/2020 Office Action). Yang, ¶37.

In a response, Applicant amended pending independent claims 1, 9, and 15 “[w]ithout acquiescing to the propriety of the rejection” to “recite features that further distinguish itself from the applied references.” Ex. 1002, 128-137 (10/21/2020 Amendment and Reply). Applicant also canceled pending dependent claims 3, 11, and 17. *Id.* Having placed the independent claims in allowable form, Applicant requested that their respective dependent claims also be allowed. *Id.* Applicant further added three new claims that depend from the three pending independent claims. Ex. 1002, 128-137 (10/21/2020 Amendment and Reply). The Examiner subsequently allowed all pending claims. Ex. 1002, 147-154 (12/16/2020 Notice of Allowance). The ’806 issued on March 2, 2021 with twenty claims, including the renumbered independent claims 1, 8, and 13. Ex. 1002, 169 (02/10/2021 Issue Notification). Yang, ¶38.

With the original filing of the ’806, Applicant filed an information disclosure statement (IDS) that notified the Examiner of U.S. Patent Publication No. 2017/0179026 (“Toyama”). Ex. 1002, 81 (05/05/2020 Information Disclosure

Statement). The Examiner considered Toyama and explicitly cited it as a “reference[] considered.” Ex. 1002, 124 (06/23/2020 List of References Cited by Applicant and Considered by Examiner). In addition, the ’806 and its parent, the ’378, share the same Examiner (Calvin Y. Choi), who was presented with Toyama during the prosecution of the ’378 in an IDS with Toyama alone (Ex. 2005, 555 (12/03/2019 Information Disclosure Statement)) and considered it (Ex. 2005, 593 (01/13/2020 List of References Cited by Applicant and Considered by Examiner)). Petitioner’s assertion that “Patent Owner only gave Examiner a haystack” is belied by the fact that Applicant submitted an IDS solely to cite Toyama during the application of the parent, which was then explicitly considered by the Examiner, then submitted an IDS citing Toyama again during the application of the ’806. The Examiner, who was already familiar with Toyama even before the ’806 was filed, explicitly considered Toyama again during the prosecution of the ’806 application. Petitioner is aware of the prosecution history of the ’378 and yet omitted these relevant facts. Yang, ¶39.

Moreover, the ’806 was issued with nineteen references (twelve U.S. patent documents and seven foreign patent documents)—one of which is Toyama. ’806, (56). Thus, the Examiner duly considered Toyama twice—once for the ’378 and again when subsequently examining the ’806 at issue here—but found it lacking. Yang, ¶40.

IV. LEVEL OF ORDINARY SKILL IN THE ART

For purposes of this proceeding only, Patent Owner does not object to the definition of a person of ordinary skill in the art (“POSITA”) proffered by Petitioner and adopted by the Board at institution. Pet. 27. The Challenged Claims are valid regardless of the precise definition used for a POSITA. Yang, ¶¶41-45.

V. CLAIM CONSTRUCTION

Patent Owner submits that constructions of the claim terms are not necessary to assess whether the prior art reads on the Challenged Claims for the purposes of the *inter partes* review. Patent Owner, however, reserves the right to modify or elaborate on its proposed constructions and to raise further claim construction issues in the parallel district court proceedings. Yang, ¶46.

The parties exchanged proposed claim constructions in the parallel district court proceeding. Exs. 2002-2003. The claim construction disputes in district court do not impact the issues raised in this Response.

VI. BACKGROUND OF THE ASSERTED PRIOR ART²

A. U.S. Patent Publication No. 2017/0179026 (“Toyama”) (Ex. 1005)

Petitioner does not contend that Toyama anticipates the Challenged Claims, and instead argues only that it renders obvious the Challenged Claims in view of the knowledge of a POSITA. Pet. 7, 27-122. Yang, ¶47.

Toyama teaches a 3D NAND memory device with four exemplary structures and their modifications. Ex. 1005, [0004]. Only two of these exemplary structures are relied on by Petitioner: (1) Toyama’s “second modification of the fourth exemplary structure,” illustrated in Figures 44A-B to 49, and (2) Toyama’s “first exemplary structure,” illustrated in Figures 1A-B to 17A-F. Pet. 7. Yang, ¶48.

Toyama’s second modification of the fourth exemplary structure includes, among other elements: “**semiconductor substrate 9**” (Ex. 1005, [0163]); “**planar semiconductor material layer 10**” (Ex. 1005, [0170]); “**alternating stack (132, 146, 232, 246)**” (Ex. 1005, [0232]); “**channels**” (Ex. 1005, [0211]); “**laterally-elongated contact via structures 76**” (Ex. 1005, [0236]); “**drain contact via structures 88**” (Ex. 1005, [0241]); “**insulating liners 674**” (Ex. 1005, [0340]); and

² For the purposes of the present IPR proceeding only, Patent Owner does not contest that Toyama qualifies as prior art to the ’806.

view of Toyama's second modification of the fourth exemplary structure is below.

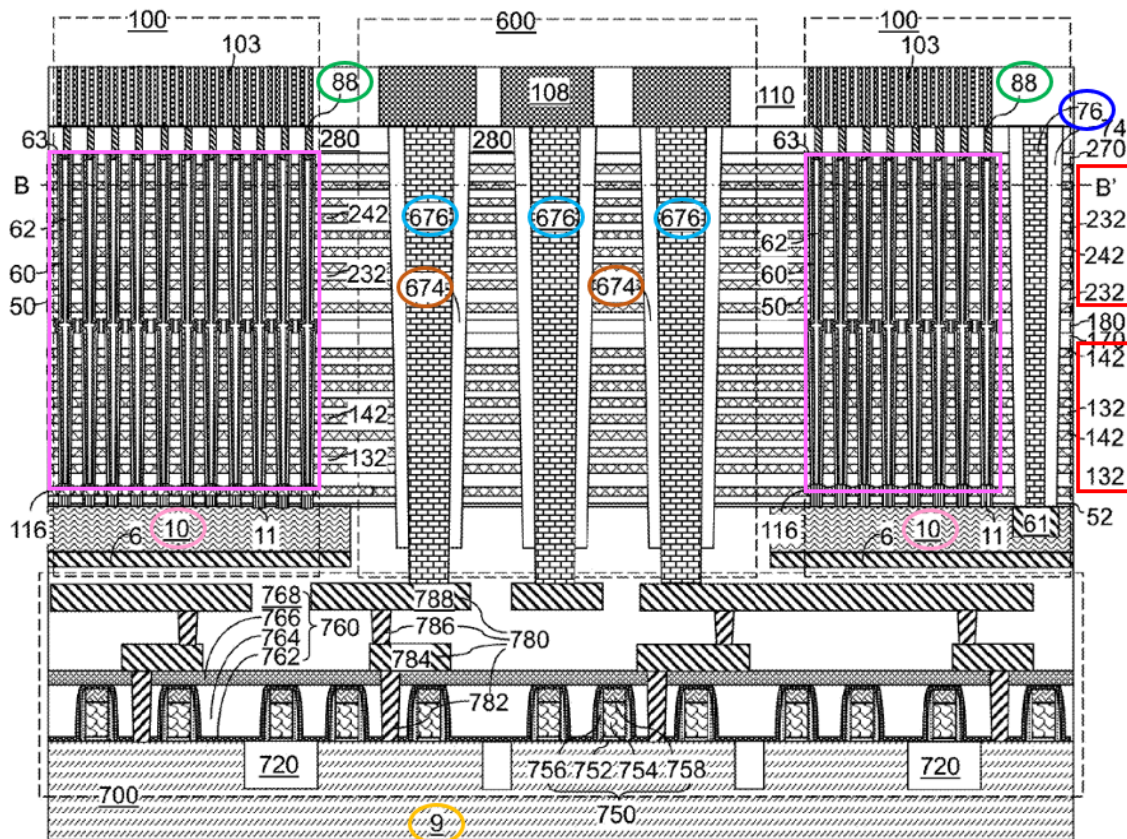


FIG. 49

Ex. 1005, Fig. 49 (annotated).³ Yang, ¶49.

³ Petitioner states: “In a clear typographical error, Fig. 49 (as well as Figs. 47A and 48A) labels its alternating conductor/dielectric layer stack as elements 132, 142, 232, 242. Elements 142 and 242 are ‘sacrificial material layers’ which, in a previous process step, were removed and replaced with ‘electrically conductive layers (146,

In Toyama's second modification of the fourth exemplary structure, **through-memory-level via structures 676** are not formed through a dielectric structure; instead, they are formed through **alternating stack (132, 146, 232, 246)**, where layers 146 and 246 are conductive, and as a result, they require separate **insulating liners 674** around each individual **through-memory-level via structure 676**. Yang, ¶50.

Toyama's first exemplary structure includes, among other elements: "**semiconductor substrate 9**" (Ex. 1005, [0163]); "**planar semiconductor material layer 10**" (Ex. 1005, [0170]); "**alternating stack (132, 146, 232, 246)**" (Ex. 1005, [0232]); "**channels**" (Ex. 1005, [0211]); "**laterally-elongated contact via structures 76**" (Ex. 1005, [0236]); "**drain contact via structures 88**" (Ex. 1005, [0241]); "**source connection via structures 91**" (Ex. 1005, [0250]); "**dielectric fill material portion 430**" (Ex. 1005, [0216]); and "**through-memory-level via structures 488**" (Ex. 1005, [0244]). A cross-section view of Toyama's first exemplary structure is below.

246).' Toyama, [0337], [0340]." Pet. 28. Patent Owner does not challenge this assertion for purposes of the Patent Owner Response.

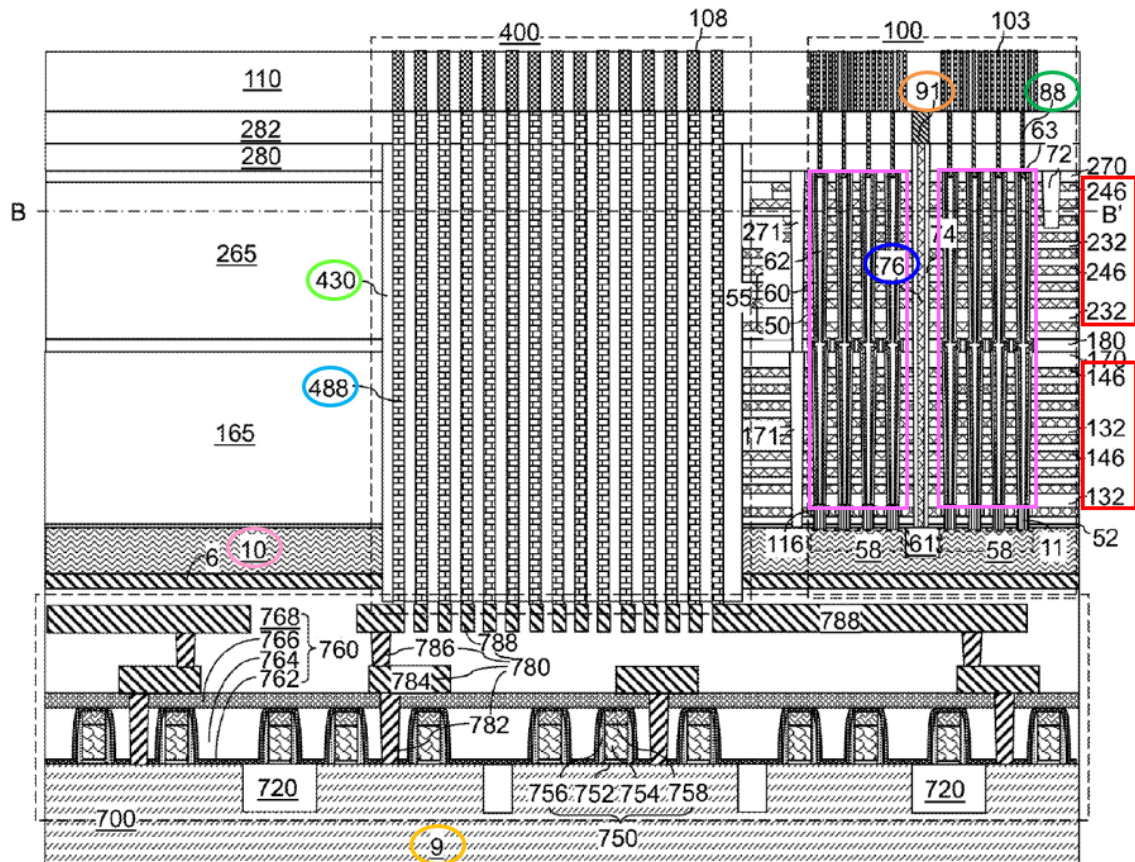


FIG. 17A

Ex. 1005, Fig. 17A (annotated). Yang, ¶51.

In Toyama's first exemplary structure, **dielectric fill material portion 430** hosts **through-memory-level via structures 488** to form vertical interconnects; however, Toyama's first exemplary structure lacks two regions with channel structures on opposite sides. Instead, **dielectric fill material portion 430** is formed in a staircase region and therefore has **channels** on one side only. As Toyama explains, the through-memory-level via region 400 (in which the through-memory-level via structures 488 are formed) "is located on a *lengthwise end* of the second

block B2 and between a staircase region of the first block B1 and a staircase region of the third block B3.” Ex. 1005, [0252], Fig. 17B. Yang, ¶52.

VII. GROUND 1: TOYAMA’S SECOND MODIFICATION DOES NOT DISCLOSE OR RENDER OBVIOUS CLAIMS 8-9 AND 11-12

In Ground 1, Petitioner relies on Toyama’s Second Modification as allegedly rendering obvious all Challenged Claims (Pet. 27-56), but Petitioner fails to show that Toyama’s Second Modification discloses or renders obvious “***a plurality of through array contacts (TACs) extending vertically through the dielectric structure***” as required by limitation [8.g] because Toyama’s alleged plurality of TACs does not extend vertically through any one purported dielectric structure. Petitioner’s mapping directly conflicts with Federal Circuit precedent holding that multiple alleged occurrences of a claim element (here, Toyama’s multiple separate dielectric liners) cannot be used to satisfy a limitation that must be satisfied by the same occurrence of the element (here, the claimed plurality of TACs must extend through “***the dielectric structure,***” meaning one specific dielectric structure). In addition, Toyama’s Second Modification does not disclose or render obvious “***a plurality of non-electrically functional channel structures surrounding the TAC region***” as required by limitation [8.h] because Toyama’s alleged non-electrically functional channel structures do not surround the alleged TAC region. Yang, ¶53.

A. Independent Claim 8: Toyama’s Second Modification Does Not Disclose or Render Obvious “a plurality of through array contacts (TACs) extending vertically through the dielectric structure” (Limitation [8.g])

Toyama’s Second Modification does not disclose or render obvious “*a plurality of through array contacts (TACs) extending vertically through the dielectric structure*” as required by limitation [8.g] because Toyama’s alleged TACs do not extend through the same structure (the claimed “dielectric structure”). Yang, ¶54.

The Challenged Claims require “a *plurality* of through array contacts (TACs) extending vertically through *the dielectric structure*”—i.e., the same dielectric structure—but this configuration is not disclosed or rendered obvious by Toyama’s Second Modification. As illustrated below in Toyama’s Fig. 49, Petitioner maps “*insulating liners 674*” of “*through-memory-level via structures 676*” to the claimed “dielectric structure” of the ’378 (Pet. 49-50), but this mapping relies on a separate insulating liner (i.e., a separate alleged dielectric structure) for each TAC.

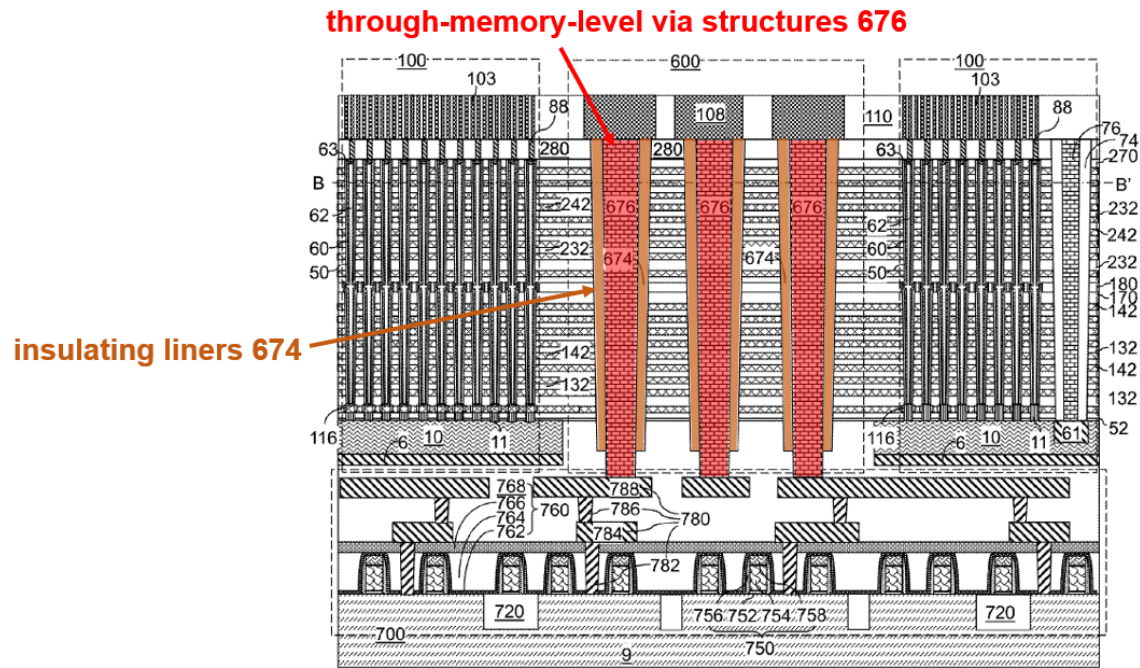


FIG. 49

Ex. 1005, Fig. 49 (annotated by Patent Owner to show Petitioner’s mapping); see Pet. 49-50 (using similar annotations but also adding a purple box over the image); Ex. 1005, [0340]-[0341] (explaining that one “through-memory-level cavity 679” is present within each insulating liner 674” for the through-memory-level via structure 676). In other words, only a single “**through-memory-level via structure 676**” (the alleged TAC)—not the claimed plurality of TACs—extends through a given “**insulating liner 674**.” Realizing this problem, Petitioner erroneously attempts to map multiple insulating liners 674 to a single “dielectric structure.” Pet. 31 (alleging that “these components together are ... a structure”), 49-50. Yang, ¶55.

Petitioner’s attempt to rely on separate dielectric structures as a single claimed “dielectric structure” is improper. The Federal Circuit has made clear that even if

the claims cover “one or more” of an element, there must still be at least one instance of the element, e.g., in the accused system or the prior art, that meets all the requirements of the claim for that element. *See Finjan LLC v. SonicWall, Inc.*, 84 F.4th 963, 974-975 (Fed. Cir. 2023) (“Even if an infringing system can use ‘one or more computers,’ the plain language of the claims requires at least one of those computers to perform all the functions listed in the claims of the ARB Patent.”). Specifically, the ’806 claims require that the same “dielectric structure” must have “a **plurality** of through array contacts (TACs) extend[] vertically through” it, which cannot be met by aggregating multiple separate instances of Toyama’s “insulating liner 674.” Thus, the Board correctly concluded in its Institution Decision that Toyama’s Second Modification does not show “a plurality of through array contacts (TACs) extending vertically through the dielectric structure” because “Petitioner has not sufficiently shown that Toyama’s three insulating liners are a single dielectric structure.” Pap. 11 (“DI”), 17. Yang, ¶56.

Petitioner misapplies the claim construction principle of *KCJ Corp. v. Kinetic Concepts* in which the Federal Circuit found that “an indefinite article ‘a’ or ‘an’ in patent parlance carries the meaning of ‘one or more’ in open-ended claims containing the transitional phrase ‘comprising.’” 223 F.3d 1351, 1356 (Fed. Cir. 2000). This principle merely means that a memory structure that reads on the claims could include more than one dielectric structure, and does **not** mean that more than

one dielectric structure can be combined or otherwise pieced together for any claimed requirements imposed on the claimed “dielectric structure” (singular). Indeed, as discussed, the Federal Circuit has made clear that even if the claims cover “one or more” of an element, there must still be at least one instance of the element, e.g., in the accused system or the prior art, that meets all the requirements of the claim for that element. *Finjan*, 84 F.4th at 974-975 (“‘[T]he indefinite article a means one or more in open-ended claims containing the transitional phrase comprising.’ But that is a separate issue from whether the claims require the same component to perform multiple functions or satisfy multiple limitations of a claim. ... Claim 1 of the ARB Patent requires that the same computer perform each of the claimed steps [...] Even if an infringing system can use ‘one or more computers,’ the plain language of the claims requires at least one of those computers to perform all the functions listed in the claims of the ARB Patent.”) (internal citations omitted). At institution, the Board properly recognized and applied this legal principle:

While the open-ended language may permit the claimed memory device to have more than one dielectric structure, this does not change ***the claim language that requires multiple TACs to extend vertically through a single dielectric structure***. In other words, even if the claim language’s use of indefinite article ‘a’ or ‘an’ or the open-ended transitional phrase ‘comprising’ permits more than one dielectric

structure in the memory device, ***the claim still requires that a plurality of TACs must extend through a single dielectric structure.***

DI, 17-18. Petitioner ignores this distinction, and its mapping of claim 8 to Toyama is doomed by this fundamental legal error.⁴ Yang, ¶57.

Therefore, Petitioner has failed to show that Toyama’s Second Modification discloses or renders obvious⁵ “a plurality of through array contacts (TACs) extending vertically through the dielectric structure” as required by limitation [8.g]. Yang, ¶58.

B. Independent Claim 8: Toyama’s Second Modification Does Not Disclose or Render Obvious “a plurality of non-electrically functional channel structures surrounding the TAC region” (Limitation [8.h])

Toyama’s Second Modification also does not disclose or render obvious “***a plurality of non-electrically functional channel structures surrounding the TAC***

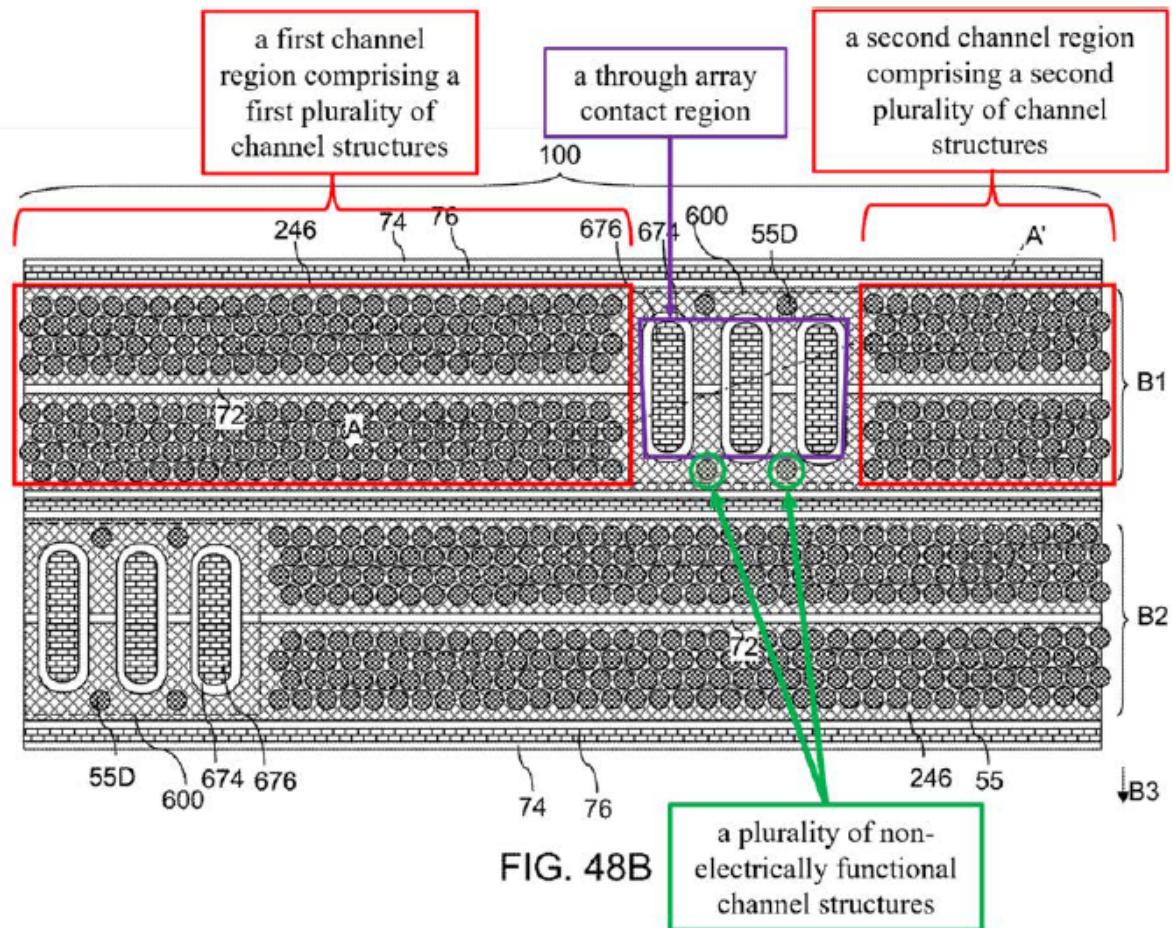
⁴ To be clear, the claims do not preclude multiple dielectric structures. But the limitation “a plurality of through array contacts (TACs) extending vertically through the dielectric structure” requires that the plurality of TACs extend through at least one particular dielectric structure, regardless of whether additional dielectric structures are also present in the device. Yang, ¶¶57.

⁵ In Ground 1, Petitioner does not argue that it would have been obvious to modify Toyama’s Second Modification to meet limitation [8.g]. See Pet. 49-50.

region” as required by limitation [8.h] because Toyama’s alleged non-electrically functional channel structures do not surround the alleged TAC region. Yang, ¶59.

As shown below in Figure 48B of Toyama, Petitioner maps Toyama’s “dummy memory stack structures 55D” to the claimed non-electrically functional channel structures, but Toyama’s dummy memory stack structures 55D do not “surround” the alleged TAC region. While there are two dummy memory stack structures 55D above the alleged TAC region and two below the alleged TAC region, they are positioned in such a way that they, at most, surround one TAC within the alleged TAC region⁶—they do not surround the alleged TAC region itself, which is a larger area that extends beyond a single TAC and includes “a plurality of through array contacts (TACs).”

⁶ For purposes of this Response, Patent Owner does not concede that the dummy memory stack structures 55D surround one TAC. The Board does not need to reach that issue because the claims instead require that a plurality of non-electrically functional channel structures surround the “TAC region” (which must include *a plurality of TACs*).



Ex. 1005, Fig. 48B (annotated by Petitioner, Pet. 52). Yang, ¶60.

The Board does not need to determine the precise scope of “surrounding” in the claims because under no possible interpretation do Toyama’s dummy memory stack structures 55D surround the alleged TAC region. As discussed, at most they surround one single TAC instead of the claimed “region” that comprises a plurality of TACs. Yang, ¶61.

Therefore, Petitioner has failed to show that Toyama's Second Modification discloses or renders obvious⁷ "a plurality of non-electrically functional channel structures surrounding the TAC region" as required by limitation [8.h]. Yang, ¶62.

VIII. GROUND 2: TOYAMA'S FIRST EXEMPLARY STRUCTURE DOES NOT DISCLOSE OR RENDER OBVIOUS CLAIMS 8-9 AND 11-12

In Ground 2, Petitioner relies on Toyama's First Exemplary Structure as allegedly rendering obvious all Challenged Claims (Pet. 56-95), but Petitioner fails to show that Toyama's First Exemplary Structure discloses or renders obvious at least "*a through array contact (TAC) region formed between the first and second channel regions*" as required by claim limitation [8.g]. Yang, ¶63.

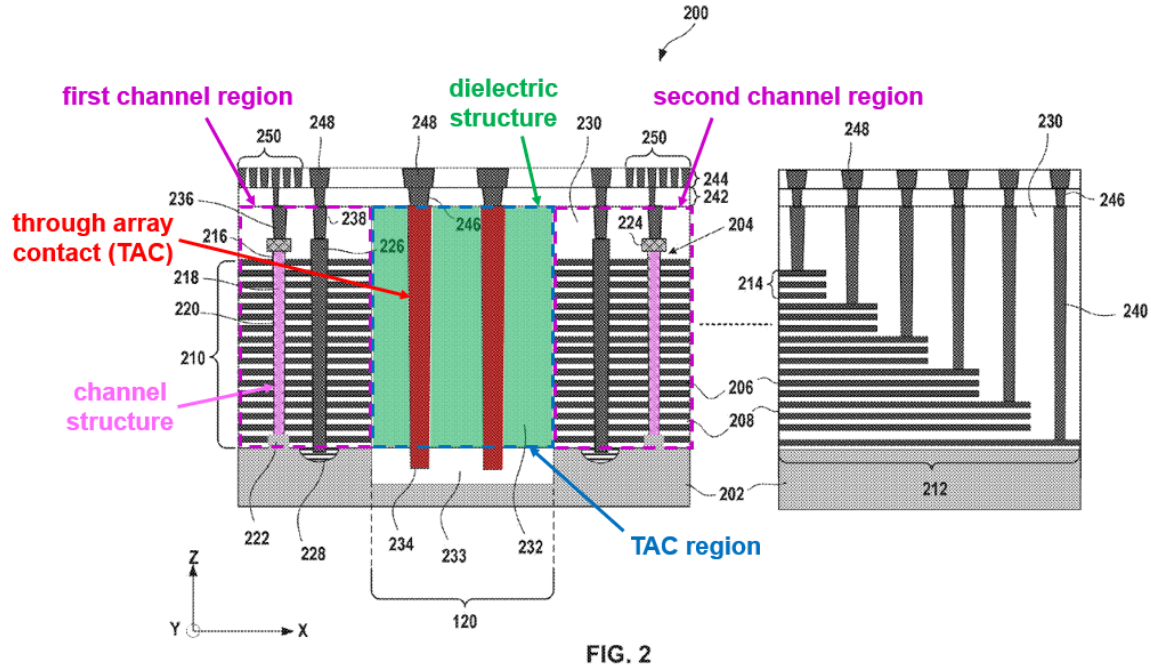
A. Independent Claim 8: Toyama's First Exemplary Structure Does Not Disclose or Render Obvious "*a through array contact (TAC) region formed between the first and second channel regions*" (Limitation [8.g])

Toyama's First Exemplary Structure does not disclose or render obvious "*a through array contact (TAC) region formed between the first and second channel regions*" as required by limitation [8.g] because the alleged TAC region is not formed between a first channel region and a second channel region. Instead, it has a channel region on only one side. While Petitioner proposes altering the First

⁷ Petitioner does not argue that it would have been obvious to modify Toyama's Second Modification to meet limitation [8.h]. See Pet. 51-54.

Exemplary Structure to repeat portions of the device and add a second channel region, its proposed modification adds a second memory device with a second channel region rather than the claimed memory device comprising a TAC region between two channel regions. In addition, its modification cannot and would not be made because it removes necessary neighboring structures (e.g., the driver circuit that connects to the memory structure on the second side) that would result in the Toyama memory structure failing to function as intended. Yang, ¶64.

The '806 claim 8 requires “a **through array contact (TAC) region** formed **between the first and second channel regions**,” which Toyama’s First Exemplary Structure fails to teach.



'806, Fig. 2 (annotated). As illustrated in Figure 2 of the '806, above, the claimed through array contacts (TACs) are formed in a **TAC region** that is formed in the

array region between the **first and second channel regions**. As a result of this placement, TACs are formed closer to memory device components, and interconnect routing may be shortened. '806, 11:8-14. Yang, ¶65.

In contrast to the '806, the channels in Toyama's First Exemplary Structure are positioned on only one side of each alleged TAC region (i.e., the alleged region containing dielectric fill material portion 430 and through-memory-level via structures 488):

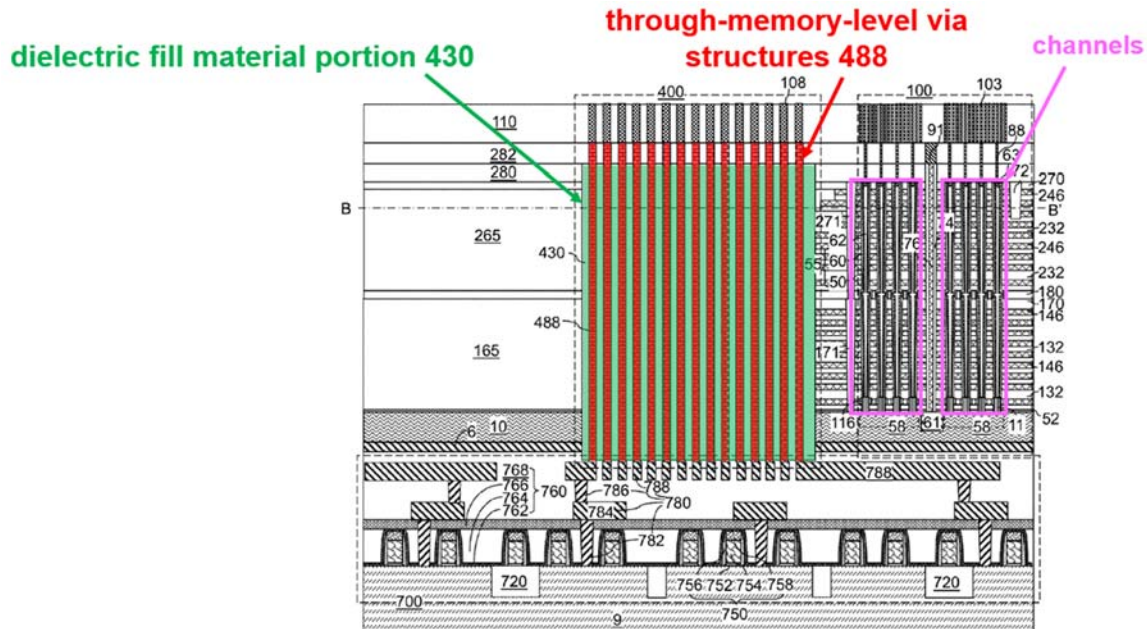


FIG. 17A

Ex. 1005, Fig. 17A (annotated by Patent Owner to show Petitioner's mapping); see Pet. 65, 85-87. Toyama never contemplates forming channels on both sides of the alleged TAC region of Toyama's First Exemplary Structure. Yang, ¶66.

In a hindsight-based attempt to overcome this deficiency, Petitioner alters Toyama's device to repeat a "layout" from one of Toyama's figures in both

horizontal directions (hd1 and hd2) so that the alleged TAC region would purportedly have channel structures on two sides. Pet. 69. Specifically, Figure 17E of Toyama shows a top-down view of the disclosed “layout” that Petitioner proposes repeating in the hd1 and hd2 directions:

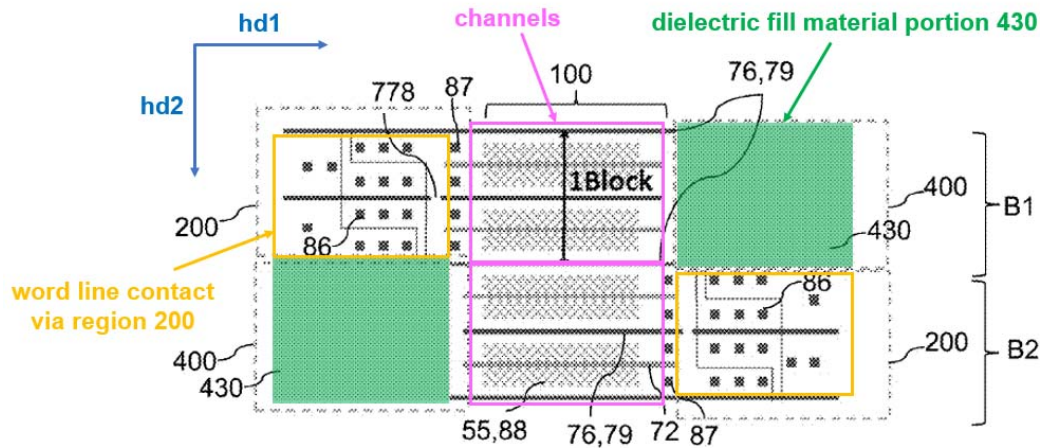


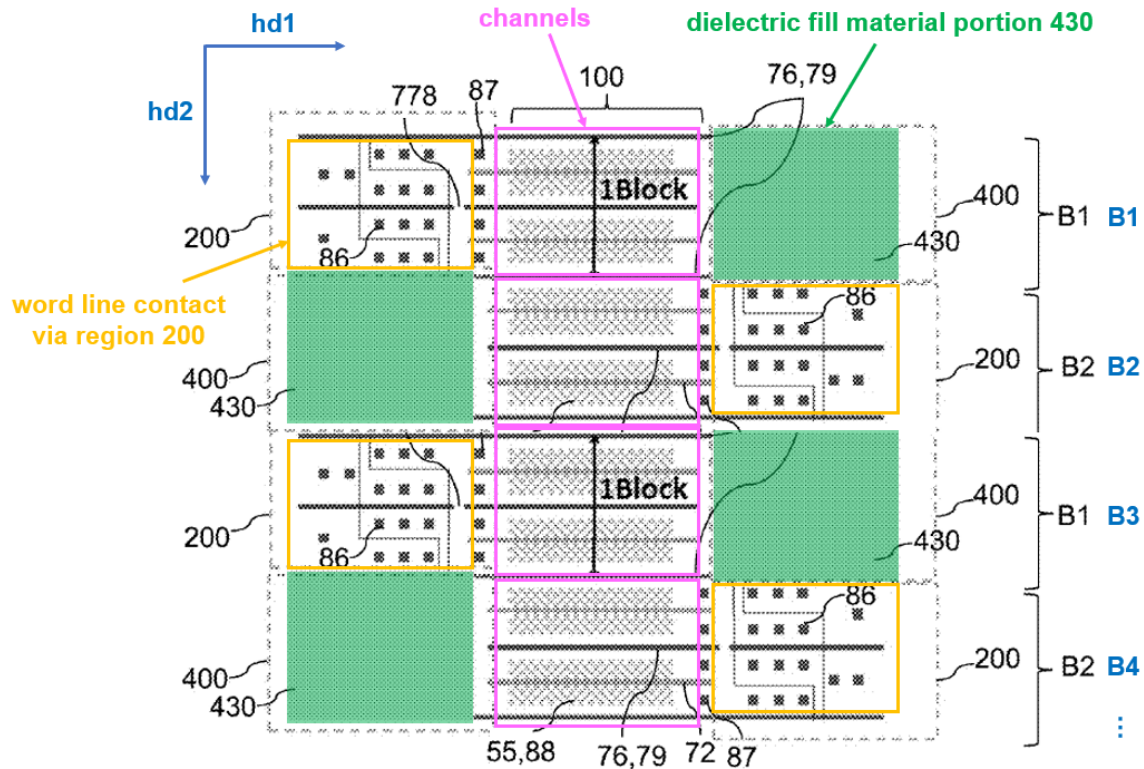
FIG. 17E

Ex. 1005, Fig. 17E (annotated). As discussed above, Petitioner maps the region containing dielectric fill material portion 430 to the claimed TAC region. Pet. 85-86. According to Petitioner, it would have been obvious to repeat this layout to create “multiple flash memory planes” “each including a distinct memory array region and staircase structure.” Pet. 69. Yang, ¶¶67.

Petitioner’s proposed modification does not result in the claimed “memory device” comprising “a through array contact (TAC) region formed between the first and second channel regions” because, by introducing a distinct “plane” for the second channel region, Petitioner is instead adding a second memory device with a

second channel region. As discussed above, the '806 is directed to a TAC region that is formed in an array between the first and second channel regions, which provides the benefit that TACs are closer to memory device components, and interconnect routing may be shortened. '806, 11:8-14. In other words, the claimed geometry having channel regions on both sides of the TAC region provides the disclosed benefit because ***both channel regions*** serve the same memory array as part of the same claimed “***memory device***.” Petitioner tries to circumvent this requirement with its proposed modification of Toyama by adding a “distinct” memory plane for the second channel region (Pet. 69), but that channel region is part of a second, “distinct” memory device, and thus does not meet the Challenged Claims. Yang, ¶¶68-69.

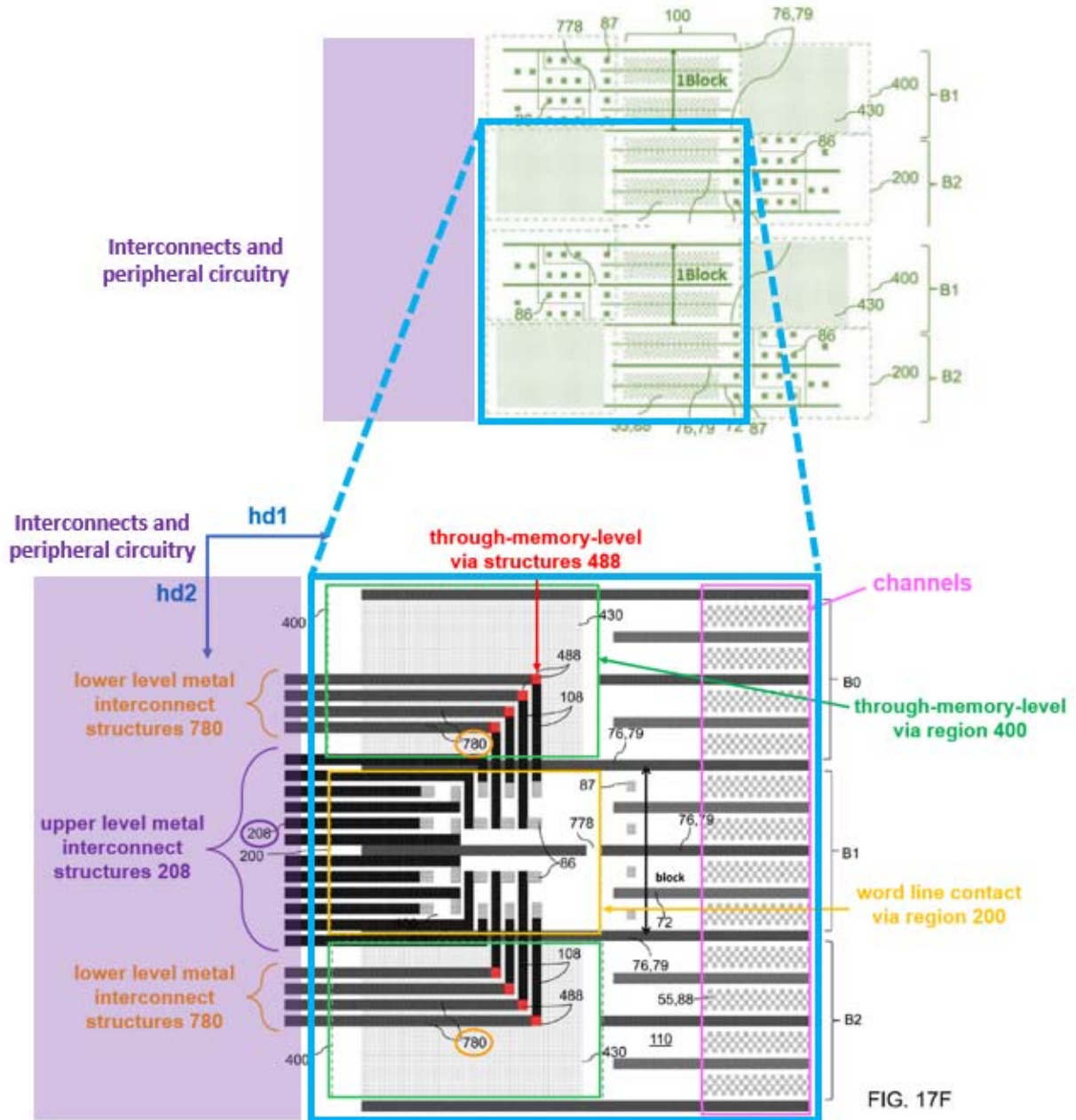
In addition, a POSITA could not and would not have made the proposed modification. As an initial matter, while Toyama does suggest repeating the Fig. 17E layout in the hd2 direction (bit line direction), repeating in the hd2 direction merely creates a row of adjacent channels and does not result in the claimed configuration of a TAC region with channel regions on both sides. Specifically, repeating Toyama’s layout along the bit line direction (hd2) does not alter the basic configuration of Toyama’s memory device: an alleged channel region on only one side of each alleged TAC region. As shown below, the alleged channel regions simply repeat in a row, as a contiguous set of channel regions:



Ex. 1005, Fig. 17E (modified by Petitioner and annotated by Patent Owner); Pet. 68. Thus, this proposed modification does not result in a TAC region formed between first and second channel regions as required by the Challenged Claims. Petitioner’s only proposal to arguably read on limitation [8.g] is to repeat in the hd1 direction. Yang, ¶¶70-71.

But Toyama never suggests that the Fig. 17E layout can be repeated in the hd1 direction (word line direction). In fact, this proposed modification ignores other circuitry, including driver circuits, that is in the hd1 direction—i.e., in the location where Petition proposes instead adding additional layouts. Specifically, Toyama includes “peripheral circuitry” to the left (and the right) of the alleged TAC regions.

Ex. 1005, [0163]. Such peripheral circuitry, such as “driver circuitry,” “supports[s] the operation of [the] memory structure.” *Id.* Critically, Toyama teaches that “upper level metal interconnect structures 208” connect to the driver circuits “at a location other than region 400” (the alleged TAC region) (Ex. 1005, [0251]) and Figure 17F—which is part of the First Exemplary Structure relied upon by Petitioner in this ground—shows these interconnect structures extending to the left of the alleged TAC region in the hd1 direction. The annotated figure below shows the location of these interconnects and peripheral circuitry relative to the “layouts” that are disclosed by Toyama:



Ex, 1005, Fig. 17F (annotated) and Fig. 17E (modified by Petitioner and annotated by Patent Owner); Pet. 69. As shown, the driver circuits and the interconnects that connect to them are located to the left of the “layout” that Petitioner proposes

repeating in the hd1 direction—i.e., precisely where Petitioner proposes adding the additional memory plane.⁸ Yang ¶72.

Petitioner’s proposed modification completely ignores the interconnects and peripheral circuitry, including the driver circuit, and therefore would not work. As shown below, Petitioner’s alteration of Toyama—to repeat in the hd1 direction—adds additional “layouts” in the location of necessary interconnects and driver circuitry:

⁸ Moreover, because Toyama’s blocks have “word line contact via regions 200” on the left and on the right of the channels, the interconnects and driver circuits are present on **both sides** of the layout in the hd1 direction. Yang ¶72.

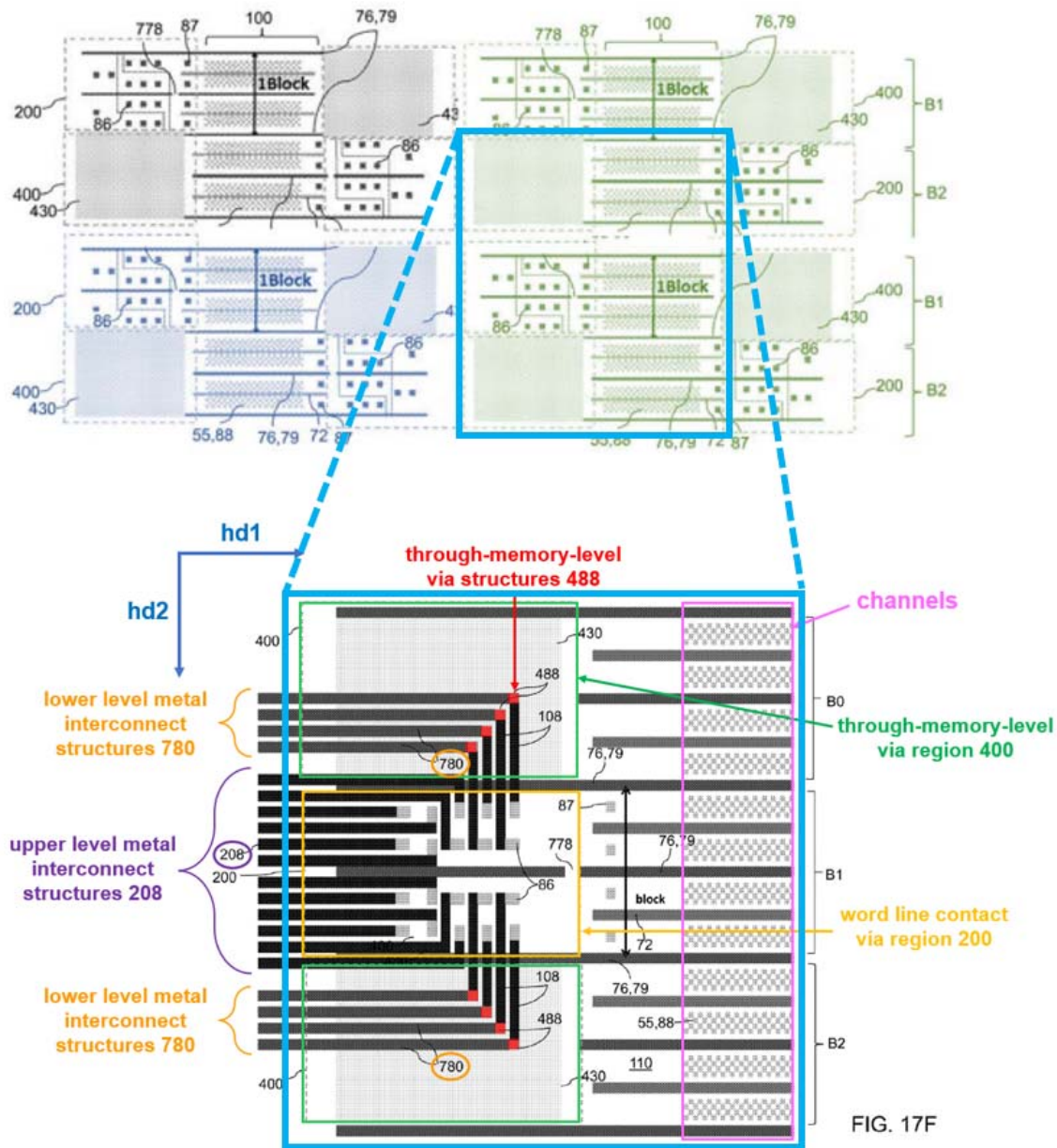


FIG. 17F

Ex. 1005, Fig. 17E (modified and annotated by Petitioner, Pet. 69) (top) and Fig. 17F (annotated by Patent Owner) (bottom). It is unsurprising that the layout of Figure 17E is not repeatable in the hd1 direction—Toyama is designed to instead repeat in the hd2 direction, with interconnects and peripheral circuitry on either side in the hd1 direction. But none of the circuitry needed to operate each memory array

and discussed in Toyama is included in Petitioner's modification. Petitioner relies on hindsight to blindly copy and paste elements of Toyama, in a way not taught by Toyama, and in a way that lacks the necessary interconnects and support circuitry for a functioning memory device. Yang, ¶¶73-74.

To the extent it is argued that the interconnects and driver circuits in Toyama are only on one side, and that additional planes could be created on the other side in the hd1 direction, this would not resolve the issue. As discussed, Toyama shows in Figure 17F that the memory array has interconnects and driver circuits on at least the left side, and thus in the modification adding additional planes, each plane would likewise include the required interconnects and driver circuitry on the left side. In other words, a new plane cannot be added on the right in the proposed location because that new plane would need to include interconnects and driver circuits to its left. Yang, ¶75.

Petitioner makes a series of arguments regarding why a POSITA allegedly would have been motivated and found it obvious to make the proposed modification (Pet. 69-77), but none of the analysis addresses the issue discussed above. Again, this is because Petitioner's analysis and proposed modification do not consider how Toyama's device would function as a workable memory device, and instead blindly copies and pastes elements of Toyama. Petitioner first argues that "[a] POSITA would have known how to implement a flash memory device with multiple planes

by placing the planes beside each other” (Pet. 70), but this provides no motivation to modify Toyama, and also does not establish that a POSITA would have known how to modify the specific device taught by Toyama to include multiple planes in the manner proposed. Indeed, the very fact that Petitioner’s expert, Dr. Lee, did not consider the necessary adjacent circuitry shows that Petitioner’s generalized citations to other references (Pet. 70-75) are not directly applicable to Toyama. Yang, ¶76.

Petitioner asserts that “a POSITA understood numerous benefits of a multi-plane flash memory device,” which Petitioner lumps together as “improve[d] ... performance of NAND based systems” (Pet. 74-76), but again, these purported benefits cannot be achieved with Petitioner’s proposed modification because Toyama’s device does not allow the proposed modification. Moreover, even assuming, *arguendo*, that there are workable ways to introduce multiple planes in Toyama’s device (i.e., layouts other than the one Petitioner has proposed), the Petition does not present any such alternatives and therefore has not shown that any such alternatives would result in “a through array contact (TAC) region formed between the first and second channel regions” as required by limitation [8.g]. Yang, ¶77.

Finally, for the same reasons, Petitioner has not established that “the obviousness combination is nothing more than applying a known technique

(implementing multiple planes of a NAND flash memory array) to a known device (Toyama’s first exemplary structure) to yield predictable results (a NAND flash device with improved performance).” Pet. 77. Yang, ¶78.

Therefore, Petitioner has failed to show that Toyama’s First Exemplary Structure discloses or renders obvious “a through array contact (TAC) region formed between the first and second channel regions” as required by limitation [8.g]. Yang, ¶79.

IX. GROUND 3: TOYAMA’S SECOND MODIFICATION IN COMBINATION WITH TOYAMA’S FIRST EXEMPLARY STRUCTURE DOES NOT DISCLOSE OR RENDER OBVIOUS CLAIMS 8-9 AND 11-12

In Ground 3, Petitioner relies on a modification of Toyama’s Second Modification based on Toyama’s First Exemplary Structure (which Petitioner refers to as “Obviousness Combination”) as allegedly rendering obvious all Challenged Claims (Pet. 96-122), but Petitioner fails to show that a POSITA would have made Petitioner’s hindsight-based modification. In addition, Petitioner’s Obviousness Combination does not disclose or render obvious “*a plurality of non-electrically functional channel structures surrounding the TAC region*” as required by limitation [8.h] because Toyama’s alleged non-electrically functional channel structures do not surround the alleged TAC region. Yang, ¶80.

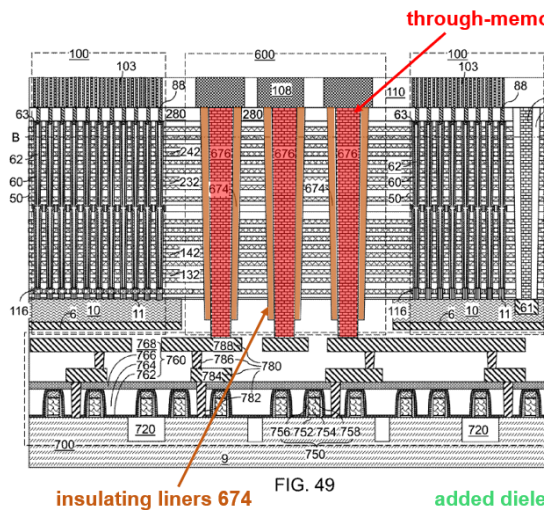
A. A POSITA Would Not Have Found It Obvious to Modify Toyama’s Second Modification in the Proposed Manner

Petitioner’s proposed modification of Toyama’s Second Modification based on Toyama’s First Exemplary Structure (Pet. 96-122) does not render obvious the Challenged Claims because Petitioner fails to show that a POSITA would have made the proposed hindsight-based modification—indeed, a POSITA would **not** have made the proposed modification because Toyama uses the alleged TAC openings for depositing etchant and conductive material during the gate replacement process, and the proposed unitary dielectric blocks that access. In addition, the proposed modification replaces conductive material used to conduct current to control memory with a large dielectric (an insulator), and Petitioner does not even attempt to address the impact that these changes would have had on Toyama’s memory structure. Yang, ¶81.

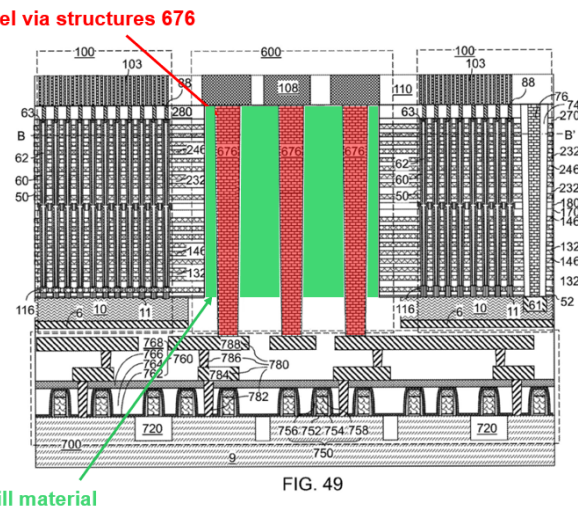
Petitioner fails to show that a POSITA would have been motivated to make its proposed modification of Toyama’s Second Modification based on Toyama’s First Exemplary Structure. As discussed in §VII.A, Toyama’s Second Modification does not disclose or render obvious “***a plurality of through array contacts (TACs) extending vertically through the dielectric structure***” as required by limitation [8.g] because Toyama’s alleged TACs do not extend through the same structure (the claimed “dielectric structure”). With the hope of overcoming this deficiency, in Ground 3, Petitioner puts forth a modification of Toyama’s Second Modification

based on Toyama's First Exemplary Structure, wherein the physically separated insulating liners around the alleged TACs are replaced with a unitary dielectric filling material around all the alleged TACs, as shown:

Toyama

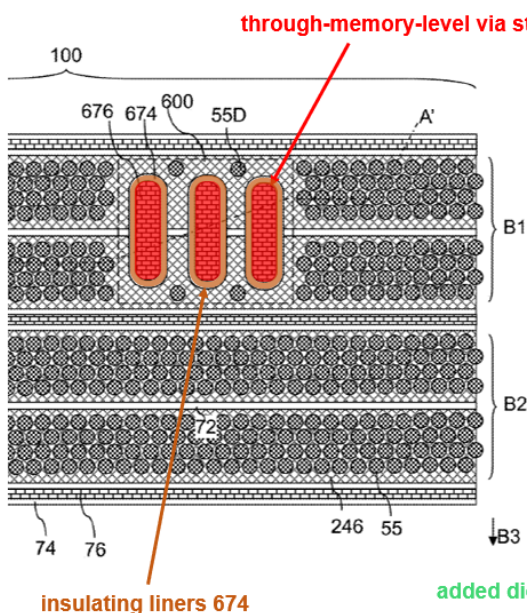


Petitioner's Proposed Modification

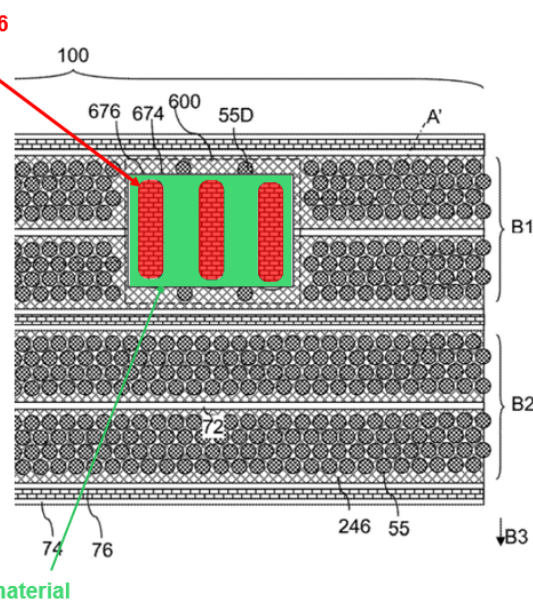


Ex. 1005, Fig. 49 (left: annotated by Patent Owner; right: modified by Petitioner at Pet. 99 and annotated by Patent Owner).

Toyama



Petitioner's Proposed Modification



Ex. 1005, Fig. 48B (left: annotated and excerpted by Patent Owner; right: modified by Petitioner at Pet. 100 and annotated and excerpted by Patent Owner). Yang, ¶82.

A POSITA would not have added a unitary dielectric fill material to Toyama's Second Modification for multiple reasons. First, adding the unitary dielectric fill material would have gone against Toyama's express teachings of using the alleged TAC openings for depositing etchant and conductive material during the gate replacement process—the proposed unitary dielectric completely blocks access to the alternating stack through the alleged TAC openings. For example, Toyama teaches forming “through-memory-level via structures 676” (the alleged TACs) by forming conductive material in “through-memory-level openings 679.” Ex. 1005, [0341]. Prior to the formation of the via structures 676, the openings 679 are “employed to introduce etchants that etch the sacrificial material layers (142, 242) selective to the insulating layers (132, 232)” as well as to introduce “conductive material” to form “electrically conductive layers (146, 246).” Ex. 1005, [0337]. This process is possible because, as shown in unmodified Figure 46A, below, the TAC openings (through-memory-level openings 679) directly abut sacrificial material layers (142, 242) of the alternating stack, allowing the alleged TAC openings to be used for introduction of etchants and conductive material.

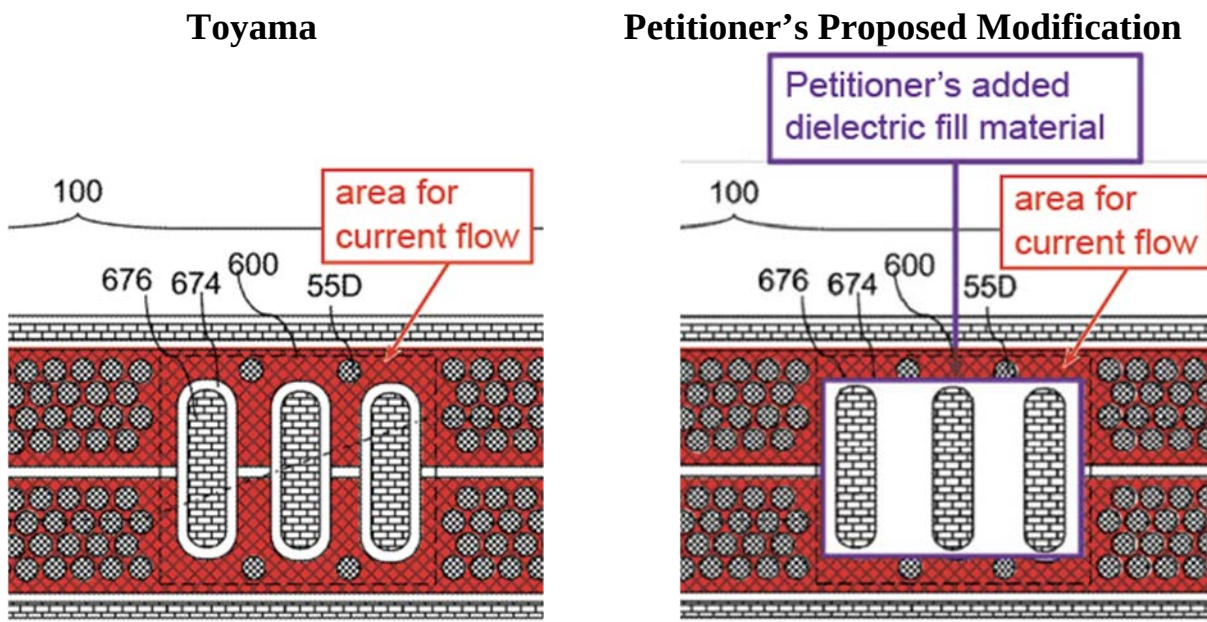


FIG. 46A

FIG. 49

added dielectric fill material

Second, Petitioner's proposed modification removes large portions of the conductive layers in the array region that form the word lines and replaces them with an insulator. Importantly, these word lines are conductive and used to conduct current to control the memory—replacing them with a large insulator would eliminate that capability in those areas. As illustrated below, Petitioner's proposed modification (enlarged and annotated below) would add an insulating dielectric fill material that has a much larger area than the original insulating liners, and extends all the way to dummy memory stack structures 55D:



Ex. 1005, Fig. 48B (left: annotated and excerpted by Patent Owner; right: modified by Petitioner at Pet. 100 and annotated and excerpted by Patent Owner). As such, this would eliminate current flow through these areas of the word lines that Petitioner proposed converting into dielectric fill material, thereby causing current to flow

through a much narrower region. A POSITA would have understood that, as a result of this restriction, Toyama's device would no longer work as intended. Yang, ¶84. Dr. Lee concedes that higher current density causes undesirable hot spots that "degrade" the device. See Ex. 2006, 36:16-37:1 ("assuming that everything remained the same" in comparison a wire "carrying less current density, [] a person of ordinary skill in the art would - - likely to conclude that the temperature of the high current density [wire] will be higher"), 32:9-10 ("local hot spot[s] ... can degrade your device reliability"). Petitioner does not even attempt to address this issue, including the adverse impact the restriction of current flow would have on the operability of the device. A POSITA would not have made this alteration to eliminate critical current flow in these areas. Yang, ¶85.

To overcome these difficulties, the '806 has a different arrangement of features in the relevant regions, which does not create the restrictions present in Petitioner's proposed Obviousness Combination and allows for wide areas around the dielectric structure for current flow through the word lines:

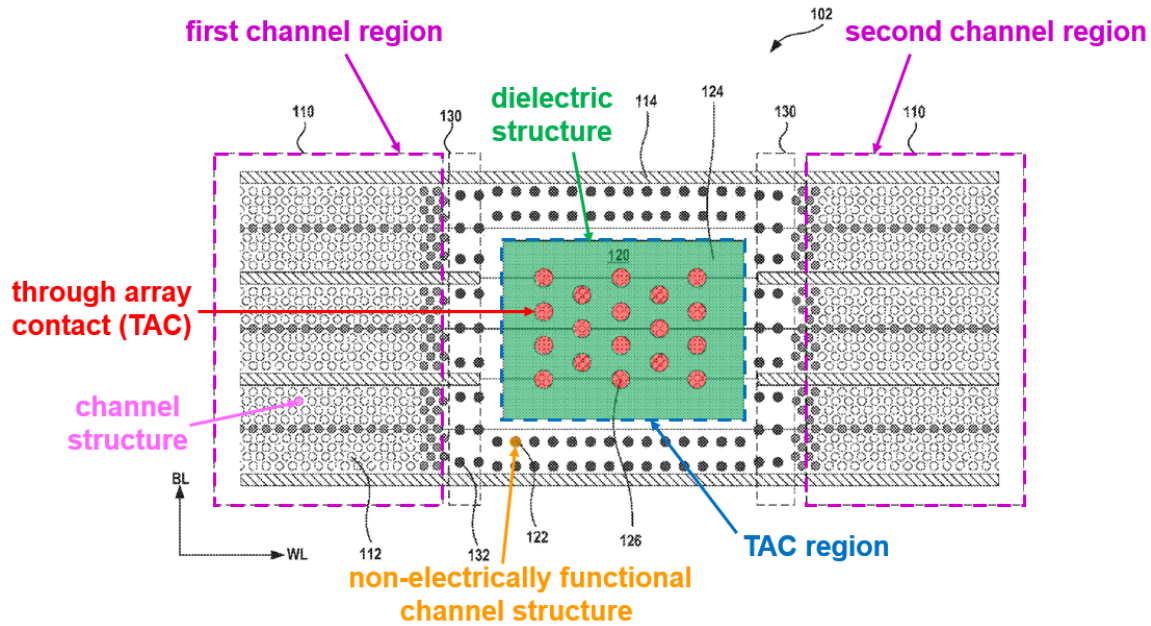


FIG. 1A

'806, Fig. 1A (annotated). In addition, the '806 uses an isolation structure onto which the dielectric structure is deposited with a high level of control using various patterning techniques, which Toyama does not teach. '806, 10:35-38, 14:63-15:30, 21:20-28. Forming a unitary dielectric fill material portion in a crowded memory array region with several other structures in its vicinity presents challenges that would have deterred a POSITA and are overcome by the novel teachings of the '806. Toyama does not teach placing multiple through-memory-level vias within a dielectric structure in the memory region, because this solution was not known. For example, if the dielectric structure is too small, the vias, which are significantly bigger than the channels, would not fit. If the dielectric structure is too large, the current flow through the word lines is blocked. Increasing the distance between the "laterally-elongated contact via structures 76" to solve the latter problem was not

feasible (and regardless, is not proposed by Petitioner), because the gate replacement process requires these structures not to be too distant from each other. Yang, ¶¶86-88. In contrast, Toyama's First Exemplary Structure was able to use a dielectric fill material portion large enough to fit multiple vias at the end of the stack opposite to the staircase region only because there is no need for the current to flow through the word lines in that location, which is at the end of the stack without word line contacts. Petitioner fails to address these considerations and simply asserts that the Obviousness Combination "is nothing more than the mere substitution of one element ... for another ... to yield a predictable result." Pet. 100. The only thing predictable about Petitioner's proposed alteration is that replacing the conductive material in the word lines used to control the memory with an insulator would cause the device to fail. Yang, ¶89.

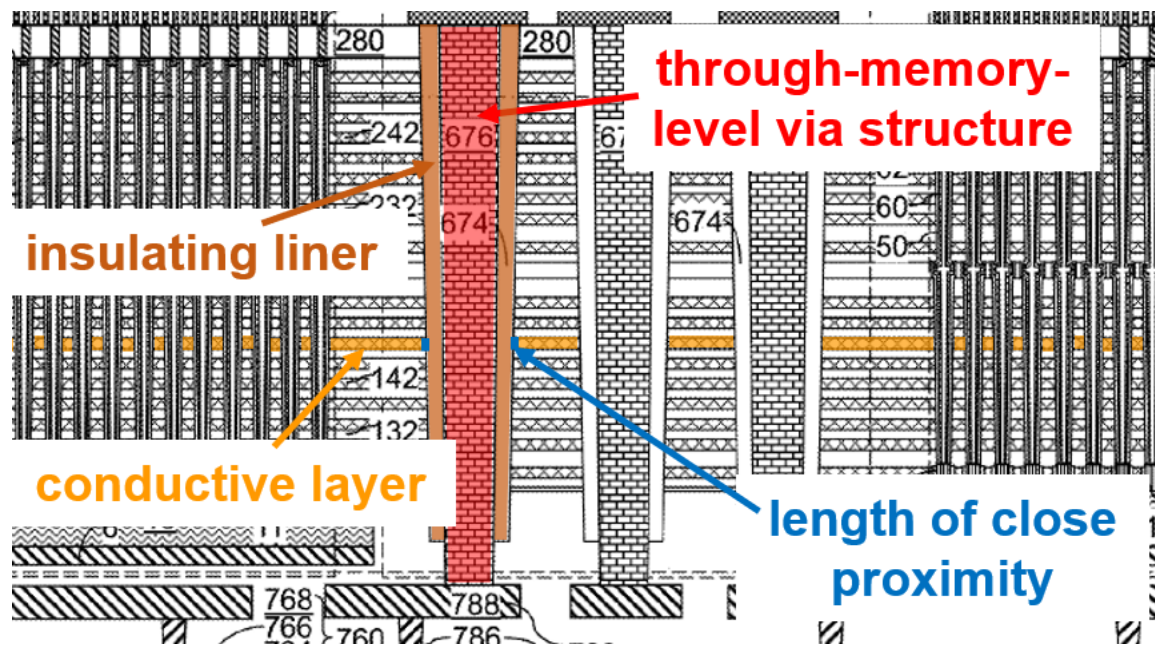
Notably, Toyama teaches more than a dozen embodiments with various configuration of elements, but none of these embodiments teaches forming a unitary dielectric block in the memory array region between two channel regions because it eliminates the conductive material in the word lines. Yang, ¶90.

Thus, as the Board correctly concluded at institution, "[a]s Patent Owner points out, based on the present record, Petitioner does not appear to address the impact of replacing the region containing conductive word lines with dielectric fill material. Based on the preliminary record, it appears that replacing the conductive

word lines with insulating material would eliminate the current that controls the memory, resulting in a non-functioning device.” DI, 34. Yang, ¶91.

Petitioner’s argument that a POSITA would have been motivated to make the combination because it “would reduce capacitive coupling as compared to Toyama’s Second Modification” (Pet. 101-103) is misplaced. As a preliminary matter, this purported motivation does not address the issue discussed above. In addition, while Petitioner argues that its modification addresses capacitive coupling between the through-memory-level vias (the alleged TACs) and the electrically conductive layers in that region, Toyama’s Second Modification already “minimizes” capacitive coupling by placing the through-memory-level via structures in the memory array region with dielectric liners. Ex. 1005, [0377]. As Toyama explains, these through-memory-level via structures “provide various control signals for a three-dimensional memory device in a manner that shortens the signal path, and thus, minimizes ... capacitive coupling.” *Id.* Petitioner’s expert, Dr. Lee, explains that there is a relation between capacitive coupling and distance between conductive elements (Ex. 1003 ¶ 186), but he fails to address that capacitive coupling is also a function of the length (or area) of overlap. See Ex. 1026 at 64 (“Crosstalk increases as the ... **length of their close proximity** (coupled length) increases”). In Toyama, the through-memory-level via structures and the “electrically conductive layers (146, 246)” run

perpendicular to one another—i.e., vertical vias passing through horizontal layers—and thus the length or area of their proximity is de minimis.



Ex. 1005, Fig. 49 (excerpted and annotated to show the length of close proximity between a through-memory-level via structure and a conductive layer). Thus, Petitioner has not shown that replacing Toyama’s insulating liners with a dielectric fill material portion would reduce capacitive coupling, particularly where Toyama expressly “minimizes” it already. Yang, ¶92.

Petitioner further argues that a POSITA would have recognized that placing the through-memory-level via structures (the alleged TACs) in the memory array region 100 has certain benefits (Pet. 103-104), but Toyama’s Second Modification—the embodiment that Petitioner proposes modifying—already has through-memory-level via structures (the alleged TACs) in the memory array region 100. Petitioner

is not proposing moving the alleged TACs. Thus, any benefits of having the alleged TACs in that particular location are irrelevant to whether a POSITA would make a different modification, i.e., adding a unitary dielectric fill material as proposed by Petitioner. Yang, ¶93.

Petitioner asserts that “elements of the [F]irst [E]xemplary [S]tructure and the Second Modification are compatible with each other” (Pet. 105; Ex. 1003, ¶¶184-197), but Toyama does not teach such compatibility or substitution between its embodiments. Rather, Petitioner’s argument is based on nothing more than the conclusory testimony of Petitioner’s expert. *See* Pet. 105-106 (citing Ex. 1003, ¶194). That a limited set of other, **different** structures may have the same name in both embodiments (*id.*) is irrelevant. Indeed, the issues discussed above demonstrate that the embodiments are not compatible. At the very least, they are not combinable in the way proposed by Petitioner. Yang, ¶94.

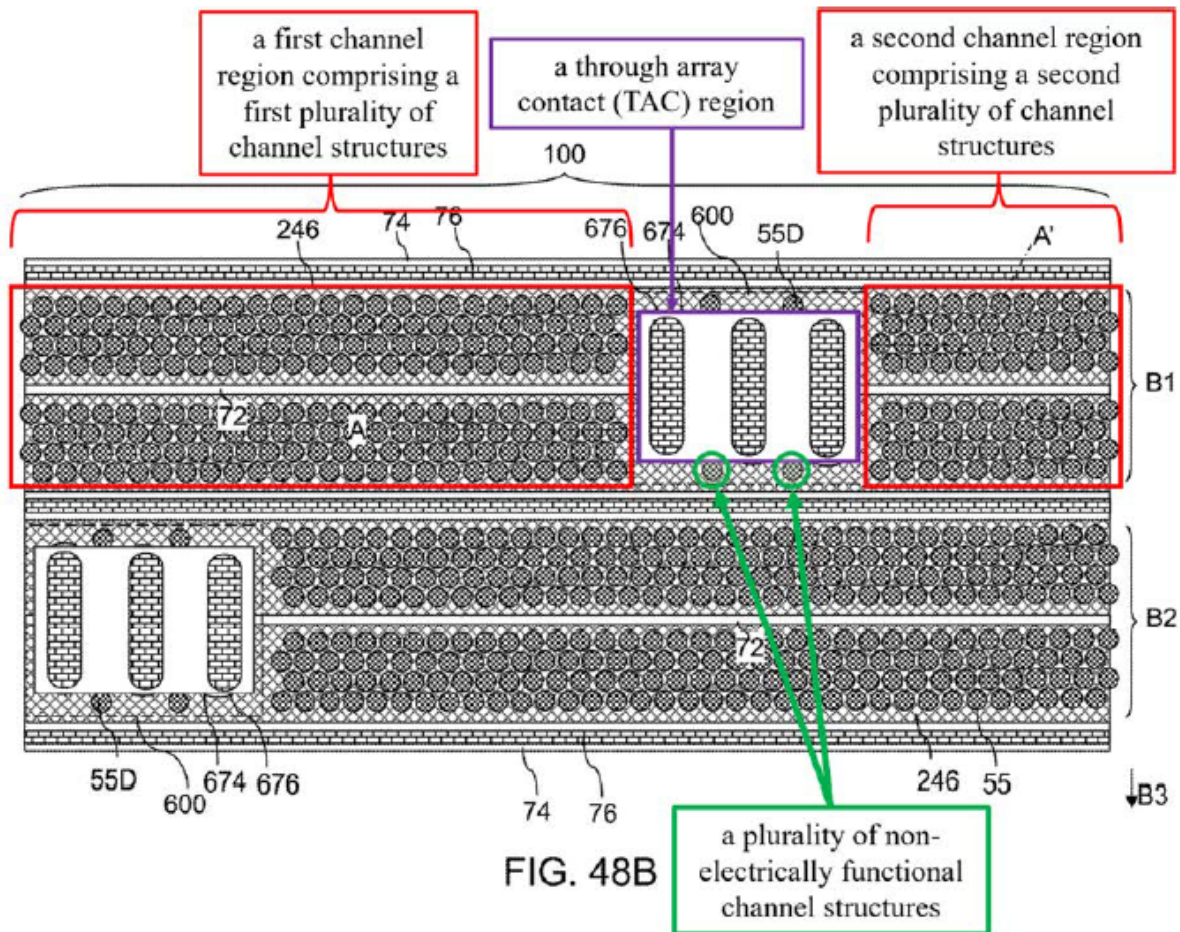
Petitioner’s assertion that a POSITA would have found the combination straightforward (Pet. 104-108, citing Ex. 1003, ¶¶184-197) relates to whether a POSITA could **manufacture** the device, and do not address the lack of motivation to make the proposed combination, let alone the adverse impact that replacing the conductive word lines with an insulator would have. *See* Pet. 105 (“A POSITA also would have understood how to manufacture a device implementing the obviousness combination.”). Yang, ¶95.

Therefore, Petitioner fails to show that a POSITA would have found it obvious to modify Toyama's Second Modification in the alleged manner. As a result, Ground 3 fails. Yang, ¶96.

B. Independent Claim 8: Petitioner's Obviousness Combination Does Not Disclose or Render Obvious "a plurality of non-electrically functional channel structures surrounding the TAC region" (Limitation [8.h])

Petitioner's Obviousness Combination also does not disclose or render obvious "*a plurality of non-electrically functional channel structures surrounding the TAC region*" as required by limitation [8.h] because Toyama's alleged non-electrically functional channel structures do not surround the alleged TAC region. Yang, ¶97.

For Ground 3, Petitioner relies on the teachings of only Toyama's Second Modification (Ground 1) for the alleged plurality of non-electrically functional channel structures, and cross-references its analysis from Ground 1 in the Petition. See Pet. 119-120 ("The obviousness combination does not alter the Second Modification's 'dummy memory stack structures 55D.' ... Thus, for the reasons explained in Ground 1, the obviousness combination renders obvious [Limitation [8.h]]."). Thus, for the same reasons discussed for Ground 1 (see §VII.B) and as shown below, Toyama's **dummy memory stack structures 55D** do not "surround" the alleged **TAC region**.



Ex. 1005, Fig. 48B (annotated by Petitioner, Pet. 120). Yang, ¶98.

Therefore, Petitioner has failed to show that the Obviousness Combination discloses or renders obvious “a plurality of non-electrically functional channel structures surrounding the TAC region” as required by limitation [8.h]. Yang, ¶99.

X. CONCLUSION

For the reasons above, Petitioner has failed to demonstrate by a preponderance of the evidence that any of the Challenged Claims of the '806 is anticipated or

obvious. Yang, ¶¶100-102. Accordingly, the Board should find in favor of Patent Owner and uphold the validity of all Challenged Claims.

Dated: February 19, 2025

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CERTIFICATE OF WORD COUNT

The undersigned certifies that the foregoing PATENT OWNER'S RESPONSE UNDER 37 C.F.R. § 42.120 complies with the type-volume limitation in 37 C.F.R. § 42.24(a)-(b). According to the word-processing system's word count, the brief contains 8,404 words, excluding the parts of the brief exempted by 37 C.F.R. § 42.24(c).

Dated: February 19, 2025

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ROPES & GRAY LLP

CERTIFICATE OF SERVICE

The undersigned certifies that the foregoing PATENT OWNER'S RESPONSE UNDER 37 C.F.R. § 42.120 was served in its entirety by filing through the Patent Trial and Appeal Case Tracking System (P-TACTS), as well as providing a courtesy copy via e-mail to the following attorneys of record for Petitioner listed below:

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Dated: February 19, 2025

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