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Transcript of Jack Lee, Ph.D.

Date: January 30, 2025
Case: Micron Technology, Inc. -v- Yangtze Memory Technologies Company, LTD., (PTAB)

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WORLDWIDE COURT REPORTING & LITIGATION TECHNOLOGY

1

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,)
)
Petitioner,)
)
vs.) Case No.
) IPR2024-00791
YANGTZE MEMORY TECHNOLOGIES)
COMPANY, LTD.,) Patent 10,937,806
)
Patent Owner.)
_____)

VIDEOTAPED DEPOSITION OF JACK LEE, PH.D.

VIA VIDEOCONFERENCE

THURSDAY, JANUARY 30, 2025

8:04 A.M.

Stenographically reported by:

Kayla Lotstein

California CSR No. 13916, CRR, RPR, CRC

2

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COMPANY, LTD.,) Patent 10,937,806
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Patent Owner.)
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VIDEOTAPED DEPOSITION OF JACK LEE, PH.D. taken on behalf of Patent Owner, at 8:04 a.m., Thursday, January 30, 2025, Via Videoconference, before Kayla Lotstein, Certified Shorthand Reporter No. 13916 of the State of California, pursuant to Notice.

3

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4

INDEX

WITNESS: JACK LEE, Ph.D.

EXAMINATIONS

Page
By Mr. Cross 8

5

EXHIBITS

No.	Description	Page
Exhibit A	United States Patent No. US 10,658,378 B2; Date of Patent: May 19, 2020	14

6

INDEX (CONTINUED)

PREVIOUSLY MARKED EXHIBITS

No.	Description
Exhibit 1001	United States Patent No. US 10,937,806 B2; Date of Patent: March 2, 2021
Exhibit 1003	Declaration of Jack C. Lee, Ph.D.
Exhibit 1005	United States Patent Application Publication No. US 2017/0179026 A1; Pub. Date: June 22, 2017

INFORMATION TO BE SUPPLIED

Page Line

(None)

QUESTIONS INSTRUCTED NOT TO ANSWER

Page Line

(None)

7

VIA VIDEOCONFERENCE; THURSDAY, JANUARY 30, 2025
8:04 A.M.
* * *

THE VIDEOGRAPHER: Here begins the videotaped deposition of Jack Lee, Ph.D., in the matter of Micron Technology, Incorporated, versus Yangtze Memory Technologies Company, Limited, in the United States Patent and Trademark Office, before patent and trial appeal board, Case Numbers IPR2024-00791 and PR2024-000911.

Today's date is 1/30/2025. The time on the video monitor is 8:05 Pacific time.

The remote videographer for today is Parker Simpson representing Planet Depos.

All parties of this video deposition are attending remotely.

Would counsel please voice-identify themselves and state whom they represent.

MR. CROSS: Allen Cross, Ropes & Gray, for patent owner, YMTC.

MR. SAGDEO: Parth Sagdeo with Orrick Herrington for Petitioner, Micron.

THE VIDEOGRAPHER: The court reporter today is Kayla Lotstein representing Planet Depos. The witness will now be sworn.

8

THE STENOGRAPHER: Hello. My name is Kayla Lotstein. My CSR number is 13916.

Jack Lee, Ph.D.,
called as a witness on behalf of the Patent Owner, and having been duly sworn, was examined and testified as follows:

EXAMINATION

BY MR. CROSS:

Q Good morning, Dr. Lee. Could you please state your name.

A Jack Lee.

Q And what address are you currently located at?

A 5803 Westslope Cove, Austin, Texas 78731.

Q And can you provide us with what materials you have in front of you, if any.

A Just a laptop.

Q Okay. And do you have any programs opened up on the laptop?

A No.

Q Do you have any other screens in -- in your room that you're in?

A Yeah. I have a monitor -- two monitors.

Q Okay. Connected to your laptop?

A Yes. Yes.

Q You understand that you are under oath today?

9

1 A **Yes.**
2 Q And you understand that I'll be asking
3 questions, and you'll be answering them?
4 A **Yes.**
5 Q Okay. And I ask that you please wait for me
6 to finish, and then I'll try and wait for you to do the
7 same.
8 A **Yes.**
9 Q Is there any reason why you cannot testify
10 truthfully and fully today?
11 A **No.**
12 Q And if I ask you a question that you don't
13 understand, do you agree to ask for clarification?
14 A **Yes.**
15 Q If you don't ask for clarification, I'll
16 assume that you understand the question.
17 Is that fair?
18 A **Yes.**
19 Q Before we proceed, I'd like to go through a
20 couple of terms that we'll be using today throughout.
21 Did you file a declaration in IPR2024-00791
22 labeled Exhibit 1003?
23 A **Can you -- is it possible that you upload**
24 **the -- my declaration? Because I don't remember the**
25 **page number or details at all.**

10

1 Q Sure.
2 Did you receive the document, Dr. Lee?
3 A **Yes.**
4 Q Great.
5 A **Yes. I received it.**
6 Q Great.
7 If I refer to this one as your first
8 declaration, you'll understand what I mean?
9 A **Yes.**
10 Q Great.
11 You also filed a -- what I refer to as a
12 second declaration in IPR2024-00911 also marked as
13 Exhibit 1003; is that correct?
14 A **Yeah.**
15 Q And I'll upload --
16 A **Yes.**
17 Q I'll upload that one as well.
18 A **Thank you, sir. Thank you.**
19 **I've received it.**
20 Q Great.
21 And are you familiar with US Patent
22 10,937,806?
23 A **Is this the one that we say is '806 patent?**
24 Q That's correct. So I'll refer to that as the
25 '806 patent going forward.

11

1 A **Yeah. Would you upload that, please.**
2 Q I can upload that.
3 And, finally, are you familiar with US Patent
4 Publication Number 2017/0179026, which was filed by a
5 Mr. Toyama?
6 A **Yes.**
7 **Would you mind uploading that too?**
8 Q It's a larger file. It's -- should be there
9 now.
10 A **Still uploading.**
11 **Okay. I have downloaded it.**
12 Q Great.
13 And I'll be referring to this as the Toyama
14 reference.
15 Do you agree?
16 A **Yes.**
17 Q Great.
18 Can you please state what your consulting rate
19 for this IPR is?
20 A **It's $680 an hour.**
21 Q Thank you.
22 And is that the same rate for all of your work
23 on these YMTC matters?
24 A **Yes.**
25 Q Dr. Lee, what did you do to prepare for

12

1 today's deposition?
2 A **I reviewed the four documents that you just**
3 **uploaded and I just downloaded, and I also review the**
4 **materials that I cited in each of the declarations in --**
5 **in the sections "Assignment and Materials Considered."**
6 **I have also discussed with counsel about some**
7 **of the details of the four documents and the materials**
8 **cited in each of the declarations.**
9 Q And about how long did you discuss these
10 materials with counsel?
11 A **I don't recall the exact time -- length of**
12 **time. In the last few weeks, we have number -- several**
13 **meetings via Zoom, and -- but this is for both the**
14 **depositions -- in preparation for the deposition of the**
15 **'378 patent that took place on Tuesday of this week and**
16 **in preparation of the deposition of the '806 patent that**
17 **take place -- that are taking place right now.**
18 Q When you reviewed your first declaration, did
19 you find any inaccuracies?
20 A **No.**
21 Q When you reviewed your second declaration, did
22 you find any inaccuracies?
23 A **No, not that I can recall.**
24 Q So these declarations reflect the opinions
25 you've formulated in these matters?

13

1 **A Yes.**
2 Q What materials did you consider in formulating
3 your opinions?
4 **A As I mentioned, that -- the materials that I**
5 **have considered are listed in both of the declarations**
6 **in these sections of "Assignment and Materials**
7 **Considered."**
8 Q You didn't consider anything outside of those
9 lists?
10 **A The list -- the -- the table listed all the**
11 **exhibit, and as I discuss in the sections, I also review**
12 **and considered the '806 patent, Exhibit 1001, and its**
13 **prosecution history, Exhibit 1002, and the materials**
14 **listed in the table in the sections of "Assignment and**
15 **Materials Considered."**
16 Q And that's true of both declarations; correct?
17 **A That is correct.**
18 Q And before you signed your declaration, did
19 you review either of the petitions?
20 **A No, I did not.**
21 Q Turning to the '806 patent, if you have that
22 up in front of you --
23 **A Yes.**
24 Q -- on the cover at Code 63, it reads,
25 "Continuation of Application No. 16/047,182, filed on

14

1 July 27, 2018, now Patent No. 10,658,378."
2 Did I read that correctly?
3 **A Yes.**
4 Q Do you understand what a "continuation" means?
5 **A I might have discussed this in my declaration.**
6 **Can you hold on one second.**
7 **Let's see. I don't know if I have discussed**
8 **that.**
9 Q Are you familiar with US Patent
10 Number 10,658,378?
11 **A Yes. Hold on one second. Let me make sure**
12 **that's the number.**
13 **Can you upload that patent, please.**
14 Q Sure.
15 **A I'm pretty sure that's the one that we discuss**
16 **on Tuesday, but I just want to make sure.**
17 MR. CROSS: I'm uploading what I've labeled as --
18 or titled Exhibit A - US 10,658,378.
19 If I could have that marked as Exhibit A.
20 (Whereupon Exhibit A was marked for
21 identification.)
22 THE WITNESS: Yes. That's the '378 patent that we
23 discussed on Tuesday.
24 BY MR. CROSS:
25 Q Does the '378 patent and the '806 patent share

15

1 the same specification?
2 **A I had not compare side by side, but I believe**
3 **that the written descriptions and the drawing are very**
4 **similar, if not the same.**
5 Q Thank you.
6 You filed declarations in IPRs challenging the
7 '378 patent; correct?
8 **A Those are the IPRs that we discussed on**
9 **Tuesday; is that correct? Yes.**
10 Q I believe so.
11 **A Thank you, sir.**
12 Q For terms that appear in both the challenged
13 '378 claims and the '806 claims, did you use the same
14 definitions?
15 **A Can you repeat that, please.**
16 Q For terms that appear in both the challenged
17 '378 claims and the '806 claims, did you use the same
18 definitions for those terms?
19 **A I'm sorry. I'm not sure what you mean by**
20 **"definition."**
21 **Do you mean the claim construction?**
22 Q Let me rephrase.
23 Are there any claim terms in which you applied
24 a different meaning in analyzing the '378 claims than
25 you applied in analyzing the '806 claims?

16

1 **A As I explain in the "Claim Construction"**
2 **section of my declarations, in paragraph 72 to 74, that,**
3 **first of all, I'm not an attorney, and so I offer no**
4 **opinions on the law, but I understand the claim**
5 **construction is a matter of law.**
6 **And I have been informed that the words of the**
7 **claim are generally given plain and ordinary meaning**
8 **that the term or the phrase would have to a person of**
9 **ordinary skill in the art at the time of the invention**
10 **in view of the surrounding claim language,**
11 **specification, and file history. Those collectively**
12 **called intrinsic evidence or intrinsic record.**
13 **I also understand that the courts may consider**
14 **what is called the extrinsic evidence, such as expert**
15 **and inventor's testimony, dictionary, and other learned**
16 **treatises, collectively called extrinsic evidence or**
17 **extrinsic record, but that in my -- that those extrinsic**
18 **evidence are given less weight than the intrinsic**
19 **evidence.**
20 **So, in my opinion, the challenged terms or the**
21 **challenged claims do not require further construction**
22 **and can be afforded the plain and ordinary meaning for**
23 **the purpose of analyzing the prior art that I'm**
24 **conducting in both of those declarations.**
25 Q So, to confirm, in both the '378 declarations

17

1 you filed and the '806 declarations you filed -- that
2 were filed, you applied the plain and ordinary meaning
3 of the terms that appear in the claims?
4 MR. SAGDEO: Objection. Form.
5 THE WITNESS: As I explained in this section, that
6 the challenged claim do not require further construction
7 and can be afford -- afforded the plain and ordinary
8 meaning for the purpose of the analysis of the prior
9 art.
10 And -- and, of course, as I discuss in this
11 section that the plain and ordinary meaning that the
12 terms would have to a person of ordinary skill in the
13 art at the time of the invention in viewed of the
14 intrinsic evidence and extrinsic evidence.
15 BY MR. CROSS:
16 Q Okay. I don't think the -- that answered my
17 question, which was whether or not you're applying a
18 different meaning to any of the terms that are in the
19 '378 declaration than in the '806 declaration when they
20 are using the same language.
21 MR. SAGDEO: Objection. Form.
22 BY MR. CROSS:
23 Q So can you please --
24 **A Is -- sorry. I was going to ask you the**
25 **question.**

18

1 Q Oh, go ahead.
2 **A Is there a particular term that you're**
3 **thinking that I'm applying a different meaning? If so,**
4 **can you -- can you refer where it was -- where it is in**
5 **my declarations.**
6 Q Right now, I'm asking if you're aware of any
7 terms where you applied a different meaning in one set
8 of declarations than the other set of declarations.
9 MR. SAGDEO: Objection. Form.
10 THE WITNESS: Do you mean Declaration 1 and
11 Declaration 2 for the '806 patent, or do you mean the
12 declarations of the '806 versus the declarations of the
13 '378 patent?
14 BY MR. CROSS:
15 Q Let's start with any differences between the
16 declarations of the '806 versus the declarations of the
17 '38 -- the '378 patent.
18 **A As I mention, that the claim -- the claims do**
19 **not require further construction, can be afforded their**
20 **plain and ordinary meaning for the purpose of this**
21 **analysis of the prior art and also given -- in view of**
22 **the intrinsic and extrinsic evidence to a person of**
23 **ordinary skill in the art at the time of invention.**
24 **Having said that, I don't recall that -- I**
25 **don't recall the -- any terms that is given different**

19

1 **meaning in the '378 declarations versus '806**
2 **declarations. I don't recall, but -- there might be,**
3 **but I don't recall. I have not consider that question.**
4 **But the claim construction, or what you say,**
5 **the definitions, how I -- how I define the terms in**
6 **the -- in the claims are described in my declarations,**
7 **for example, the Declaration 1 in paragraph 72 to 75.**
8 Q Thank you.
9 Dr. Lee, have you ever designed memory
10 devices?
11 **A Yes.**
12 Q Is density an important aspect of designing
13 memory devices?
14 **A I believe that I have discussed that in my**
15 **declarations in the -- in the "Technology Background and**
16 **State of the Art."**
17 **For example, in Declaration 1, at various**
18 **places, I discuss that NAND offer a higher integration**
19 **density than NOR flash, and the construction and the**
20 **fabrication of the 3D NAND memory chips involves various**
21 **technique in order to construct a high-density storage**
22 **architecture.**
23 **So a person of ordinary skill in the art would**
24 **understand that memory density, or what is called the**
25 **integration density, is an important consideration in**

20

1 **designing memory devices.**
2 Q Can you tell me what affects integration
3 density in memory devices?
4 **A Well, as I discuss in the sections of the**
5 **background -- "Technology Background and State of the**
6 **Art" in both of my declarations for the '806 patent,**
7 **that the memory density depends on various features of**
8 **the memory chip.**
9 **So, for example, it depends on the**
10 **architecture. There's mainly two types, the most common**
11 **types of so-called flash memory, NOR flash and NAND**
12 **flash.**
13 **NOR flash, commonly referred to as the**
14 **parallel architecture, whereas NAND flash are commonly**
15 **referred to as the series architecture.**
16 **As I mentioned just now, that -- and I discuss**
17 **here in the sections of "Technology Background and State**
18 **of the Art," that NAND flash offers a higher integration**
19 **density than NOR flash. So that's one thing that affect**
20 **the density of the -- of the memory chip.**
21 **And I also discuss other things that affect**
22 **your density. For example, in the old days, the NAND**
23 **flash is of two-dimensional, so-called planar**
24 **architecture. Planar means only an xy-plane. And**
25 **devices are fabricated -- devices, meaning the memory**

21

1 cells, are fabricated on the surface of the memory chip.
2 So one of the ways to improve and increase the
3 integration density is to move from two-dimensional to
4 three-dimensional NAND flashes and -- so that the memory
5 flash -- memory cells arranged in a vertical,
6 cylindrical columns.
7 So those are some of the examples of how
8 density of memory chips can be increased.
9 Of course, another important attribute is --
10 and I discuss that in the section, is the technology
11 itself, the fabrication technology that involve
12 patterning and etching.
13 And the etching technique, that's being
14 improved significantly over the years. For example, as
15 I discuss in my declarations, that the advent of dry
16 etching process, for example, so-called deep reactive
17 ion etching, have been used to allow etching with
18 high-aspect ratio and, therefore, increase the etching
19 capability as well, therefore, increase the integration
20 density.
21 So those are some of the effect -- that affect
22 the integration density of a memory chip. Of course,
23 there are a lot more than what I just discuss now, and
24 some of the details can be found in my -- in the
25 discussion sections of "Technology Background and State

22

1 of the Art."
2 Q Would feature size and the distances between
3 those structures affect integration density?
4 MR. SAGDEO: Objection. Form.
5 THE WITNESS: I believe -- when you say "feature
6 size," do you mean in -- in semiconductor field, feature
7 size means the equivalent of what is the smallest
8 dimension defined in a technology node?
9 Is that what you're referring to?
10 BY MR. CROSS:
11 Q I think I was referring to something more
12 general, as just the -- the sizes of the cells or the
13 sizes of particular structures within the memory device,
14 as those shrink, does that affect integration density?
15 A Yes. Obviously, that the size of the memory
16 cell depends on your capability -- the fabrication
17 capability that involve, as I mentioned, etching,
18 patterning, the use of hard mask, the use of what is
19 called a spacer etching, selective etching. And all
20 those are -- affect the size of the memory cells.
21 Now, obviously, the larger the size of each
22 memory cell, the lower the integration density of the
23 memory chip, because integration density, in the
24 simplest terms, is not exactly how it's defined, but you
25 can see that it's related to the number of memory cells

23

1 per unit area. The larger the memory cells means that
2 for a given area of the chip, the lower the number of
3 memory cells you can pack into the area and, therefore,
4 the lower the integration density.
5 Is that what you were thinking related to
6 feature size?
7 Q That is. Thank you very much, Dr. Lee.
8 A Thank you.
9 Q When designing memory devices, is operation
10 speed an important aspect to consider?
11 A Yes. As I discuss also in the "Technology
12 Background," the signal speed is -- is an important
13 factors.
14 So, for example, as I discuss in the section,
15 that by reducing the length of the interconnects, the
16 through array contacts enhance the signal speed and
17 reduce the power consumption. So that is one of the
18 important considerations.
19 Another consideration is -- that affect your
20 speed of the device is the parasitic capacitance. Not
21 only parasitic capacitance affect the noise but also
22 affect the speed as well.
23 Q Why does the length of an interconnect affect
24 the signal speed?
25 A Well, the speed of a single transmission, you

24

1 can think of it as how long does it take for an electron
2 to go from one place to another. The longer the
3 interconnects, meaning a wire, given everything else is
4 the same, one can imagine that it will take longer for
5 electron to go from input to output.
6 So by reducing the length of the interconnect,
7 for example, interconnects such as through array
8 contacts would enhance signal speed, is to -- is
9 described and discussed in my declarations in the
10 section that I mention, "Technology Background and State
11 of the Art."
12 Q And why would parasitic capacitance affect
13 signal speed?
14 A Have you heard of RC time constant?
15 Q I have, but if you could elucidate.
16 A Okay. So, in general, the speed of the chip
17 is also related to what is called the RC time constant.
18 R represent resistance, and C represent capacitance.
19 So within the chip, there's a lot of
20 capacitance between different electrodes, okay, that
21 basically give you a so-called capacitive -- capacitive
22 coupling. And as I discuss in the declarations, this
23 capacitive coupling not only can cause cross talk
24 between one conductive element to another conductive
25 element nearby, but because of the RC time constant,

25

1 **that the speed of the chip can also inadvertently be**
2 **affected by this parasitic capacitance, "parasitic"**
3 **meaning "unwanted," capacitance.**
4 Q So does this parasitic capacitance affect the
5 interconnects?
6 **A I'm not sure I understand what you mean by**
7 **that. You mean did the interconnect affect the**
8 **parasitic capacitance?**
9 **Interconnect, depending on how they are**
10 **arranged, would result in very different value of**
11 **parasitic capacitance, not the other way around.**
12 Q Sorry.
13 For clarification, you mentioned that there's
14 capacitive coupling between one conductive element and
15 another conductive element.
16 Is an example of these conductive elements
17 interconnects?
18 **A Yes. Any conductive element, such as**
19 **interconnects, can have a signal, electromagnetically**
20 **induced voltage or current, in a different nearby**
21 **conductive element, such as interconnects.**
22 **So if your question is whether what I refer to**
23 **as conductive element can be interconnects, yes.**
24 **Interconnects are conductive elements; so, therefore,**
25 **capacitive coupling can occur between two neighboring or**

26

1 **nearby conductive element -- elements; and, therefore,**
2 **the capacitive coupling can also occur between**
3 **neighboring or nearby interconnects because**
4 **interconnects are conductive elements.**
5 Q The longer the two interconnects are
6 neighboring each other lengthwise, would that increase
7 the parasitic capacitance?
8 **A Well, the amount of capacitive coupling**
9 **depends on the distance between the two conductors.**
10 **Obviously, the closer the two conductors are, the higher**
11 **the capacitive coupling. In other words, the amount of**
12 **capacitive coupling is inversely proportional to the**
13 **distance between the conductors.**
14 **Now, obviously, if the conductors are very**
15 **short, okay, the amount of capacitive coupling will be**
16 **reduced, but the capacitive coupling per unit length is**
17 **only inversely proportional to the distance between**
18 **conductors, and the permittivity of the ambient, or the**
19 **dielectrics, separate the two conductors.**
20 Q For clarification, capacitive coupling and
21 capacitive coupling per unit length are different terms;
22 correct?
23 MR. SAGDEO: Object to form.
24 THE WITNESS: I'm not sure what you mean by
25 "different terms."

27

1 It's describing the same phenomena. It's just
2 that the -- it's just that one is the -- when you talk
3 about capacitive coupling between two conductor, you can
4 think of it as the -- as proportional to the overlap
5 area and inversely proportional to the distance between
6 the two conductors. And so that's the net value of the
7 capacitive coupling, or sometimes they simply say the
8 total capacity and value.
9 But if you divide it by the area, then that's
10 the capacitive coupling per unit area, but they are both
11 describing the same phenomena.
12 BY MR. CROSS:
13 Q So we were talking about signal speed, and to
14 confirm, it's the total capacitive coupling that affects
15 signal speed; correct?
16 **A When you say the "signal speed," do you mean**
17 **the signal speed of the transmission --**
18 Q Yes.
19 **A -- or the signal speed of the memory device?**
20 **What do you -- what do you mean by "signal**
21 **speed"?**
22 **Do you mean the signal speed of the**
23 **transmission through the conductive layer or the signal**
24 **speed -- the net signal speed of the memory elements?**
25 Q So when we started this conversation, you

28

1 mentioned that reducing the length of the interconnects
2 would reduce -- or would affect the signal speed of the
3 transmission, and that's what I'm referring to in my
4 question.
5 So to rephrase or to restate, is it the total
6 capacitive coupling that affects the signal speed?
7 MR. SAGDEO: Object to form.
8 THE WITNESS: Again, I have to clarify what -- when
9 I talk about "signal speed" earlier, I was referring
10 to -- you were asking me about the length of the
11 interconnect; and I said, yeah, by reducing the length
12 of the interconnect, for example, the through array
13 contact enhanced signal speed, as I describe in my
14 declarations, what I referred there is the signal speed
15 transmission through the -- through the wire.
16 And so if that's what you're referring to,
17 yes, it does.
18 BY MR. CROSS:
19 Q Does operating temperature affect the
20 operation speed of a memory device?
21 **A I don't think I discussed that in my**
22 **declarations.**
23 **Is there something in my declaration that you**
24 **specifically want to ask?**
25 Q No. My question is directed towards your

29

1 expertise in designing memory devices more generally.
2 **A Well, in general, believe it or not, the --**
3 **you would think that the higher the temperature, the**
4 **faster the electron would go. No.**
5 **Actually, because we're dealing with solid**
6 **state, due to various phenomena, the mobility of the**
7 **charge carrier, such as electrons, which is negative**
8 **charge, or holes, which is positive charge, reduces when**
9 **the operating temperature increase. So, therefore, when**
10 **the chip become hot, that the operating speed of the**
11 **circuit will degrade.**
12 **And that is why that -- if you notice, that**
13 **your laptop, your desktop all have cooling system, a fan**
14 **or sometimes even put it -- put some kind of**
15 **refrigerations, to make sure that the chip does not heat**
16 **up. And that's one of the reasons why -- that such**
17 **techniques, using heat sink, fan, refrigerations, to**
18 **make sure that the chips do not get too high of the**
19 **temperature.**
20 **So in answer to your question, that**
21 **semiconductor chips, the operation, including speed,**
22 **would degrade as temperature goes up.**
23 Q What causes the operating temperature to go
24 up?
25 MR. SAGDEO: Objection. Form.

30

1 THE WITNESS: So this is what I teach in short
2 courses in -- in -- in industry as well as what I taught
3 at University of Texas for 35 years.
4 And so your question is, what causes the
5 temperature of the chip to go up?
6 Well, in general, silicon is what is called an
7 indirect bandgap material. So when electron are
8 conducting through the silicon, that the -- when
9 electron -- this is very detailed. But, in short, that
10 when electrons move around in the semiconductor, such as
11 silicon or germanium or silicon-germanium, temperature
12 would go up due to that indirect bandgap features of
13 silicon.
14 BY MR. CROSS:
15 Q Could increase in current density through the
16 conductive elements in the semiconductor cause
17 temperatures to go up?
18 **A Well, it depends. It depends on many things.**
19 **It depends on if you increase the temperature --**
20 **increasing the current. But if you increase the line**
21 **width or the thickness of the interconnects, then the**
22 **current density per unit area -- per unit area, the**
23 **cross section of the wire, remain the same, then the**
24 **temperature unlikely to go up.**
25 **However, if you maintain the same interconnect**

31

1 **geometry and you increase the current current, which**
2 **means the current density increases, under the same**
3 **operation remain, everything the same, you just crank up**
4 **the current through a very -- through the same cross**
5 **section, then the current -- then the temperature would**
6 **likely to go up.**
7 **Does that make sense?**
8 Q That makes sense.
9 But to rephrase, if you maintain the same
10 current but change the geometry so that the cross
11 section was smaller, temperature would also go up;
12 correct?
13 **A It -- essentially, it depends on the current**
14 **density, not the current itself.**
15 Q Okay.
16 **A Again, simplifies it significantly. The**
17 **temperature of the chip not only depends on the current**
18 **density but also depends on what kind of dielectric is**
19 **surrounding the -- the interconnects, what kind of heat**
20 **sink do you have, and so on and so forth.**
21 Q Understood.
22 When designing memory devices, is reliability
23 an important aspect?
24 **A So, obviously, it is important. In fact,**
25 **related to -- to your temperature questions, that have**

32

1 **high temperature, not only that affect your operations**
2 **of the memory chip; it also affects your reliability.**
3 **So, for example, on page 26, I discuss that --**
4 **at the bottom of page 26 of my first declaration, that**
5 **during the device operation, dummy strings assist in**
6 **heat distributions within the memory array, thereby**
7 **reducing the local hot spots that can affect device**
8 **reliability.**
9 **Local hot spot means that the temperature**
10 **become hot locally. Okay?**
11 **And -- and, therefore, when you have local hot**
12 **spot, that can degrade your device reliability; and,**
13 **therefore, that -- the reason why I talk about that is**
14 **because reliability is an important considerations. And**
15 **that's part of my research and -- and studies and**
16 **teaching at University of Texas at Austin and also in**
17 **short course environment in industry.**
18 Q Can you give me some examples of what causes
19 local hot spots.
20 **A Well, as I discuss, that when you have -- for**
21 **example, when you don't use a dummy string in your**
22 **memory chip, that can cause -- you know, that can cause**
23 **a local hot spot.**
24 **And another example, as we discuss earlier, if**
25 **you apply high -- high current density through a**

33

1 **interconnect, you could -- you could have -- create a**
2 **local hot spot situation.**
3 **Those are the obvious examples of causes for**
4 **local hot spot. And there are various example, and I**
5 **talk about that in my classes, that if you have**
6 **nonuniform depositions of -- of devices, you know, such**
7 **as dielectric or metal wire, you could cause a increase**
8 **in -- in temperature. And if you don't apply enough**
9 **heat sink, that can cause local hot spot. And in case**
10 **of memory devices, you can have inadvertent**
11 **overprogramming of a cell that can cause local hot spot.**
12 **So there's various -- there -- I mean, if --**
13 **if you like, you can come and take my course, and you**
14 **can learn all the -- all the things that I talk about**
15 **which can cause increase in local -- temperature**
16 **locally, also called a local hot spot.**
17 Q Thank you, Dr. Lee.
18 If you have a conductor that suddenly gets
19 thin, where it gets thin, that's where you would expect
20 a local hot spot to form?
21 MR. SAGDEO: Objection. Form.
22 THE WITNESS: Would it -- how does it low --
23 suddenly get thin? What do you mean by that?
24 BY MR. CROSS:
25 Q If the geometry is such that it's wide in some

34

1 spots and narrower in other spots, you would expect
2 local hot spots to form where it's narrower; correct?
3 MR. SAGDEO: Objection. Form.
4 THE WITNESS: Well, not necessarily. I mean,
5 that's such a general -- such a general statement that
6 that is not -- that's not always true, because when you
7 talk about a wire that is not uniform cross-sectional
8 area or a chip that is not uniform metal layer, it is
9 not a -- simple as you think it is, because when you
10 have a conductor buyer -- lines, whether it's a
11 conductive word lines or conductive bit line, if that
12 line has a smaller area, it's -- that's what you're
13 referring to -- the resistance is really -- depends on
14 various things.
15 For example, is the bottleneck remain the same
16 before you suddenly narrow the interconnect or -- and
17 after you -- you said suddenly narrow the wire?
18 It really -- it's not a -- a person of
19 ordinary skill in the art would understand that, you
20 know, if the bottleneck is -- remained about the same,
21 meaning that the part of conductor to which the current
22 is most concentrated or most restricted, then the
23 current density's about the same; and, therefore, you
24 might not have a local hot spot anyway.
25 So to answer your question, you really have to

35

1 give me the entire questions in details.
2 What is the cross-sectional area, what is it
3 made of, what is the surrounding regions, and so and so
4 forth.
5 BY MR. CROSS:
6 Q Okay. For a conductor, all things being
7 equal, would the local hot spot form where the current
8 density is greatest?
9 MR. SAGDEO: Objection. Form.
10 THE WITNESS: Again, it really depends on the
11 particular problems you're dealing -- you're working
12 with: What is the geometry of the -- of the device, the
13 cross section, the voltage that you apply, the
14 dielectric material that you use, and the conductive
15 material that you use, and the placement of these
16 materials?
17 And in order to answer your questions of would
18 the hot spot occurs at a spot where the local current
19 density is higher, it's not as simple as that.
20 That's -- that's why thermal management engineers --
21 it's not just one engineers, but a team of engineers
22 to -- to deal with that.
23 BY MR. CROSS:
24 Q So I prefaced my question as, all other
25 aspects being equal, would the current density -- strike

36

1 that.
2 So I prefaced the question as, where all
3 things being equal, would the hot spot form where the
4 current density is greatest?
5 MR. SAGDEO: Objection. Form.
6 THE WITNESS: And I think at -- at the beginning of
7 this discussion, I already discuss that and I talk about
8 that in the -- in the -- in the discussions in my
9 declarations, that if you have two wires and one -- and
10 both wire are the same, same length, same cross section,
11 if you have -- pump more current through one wire, wire
12 number one, and pump less current to wire number two,
13 and assuming everything else remain the same, then the
14 temperature of the wire that carry higher current
15 density would likely be higher.
16 But, again, you really have to consider all
17 the details that you discuss, that we discuss, and so it
18 is -- it is not as simple as you imagine. But assuming
19 that everything remained the same, then, yeah, sure.
20 Two wire, one carry high current density, one
21 carrying less current density, then a person of ordinary
22 skill in the art would -- likely to conclude that the
23 temperature of the high current density will be higher.
24 But how much higher, it really -- it really depends on
25 the -- many things, including the surrounding ambient,

37

1 surrounding materials.
2 MR. CROSS: Dr. Lee, we've been going for a little
3 bit over an hour.
4 Would you like a short break, or we can
5 continue?
6 THE WITNESS: Sure. Let's take a short break.
7 MR. CROSS: Okay.
8 THE VIDEOGRAPHER: We are going off the record.
9 The time is 9:22.
10 (Recess was taken at 9:22 a.m. until
11 9:34 a.m.)
12 THE VIDEOGRAPHER: We are back on the record. The
13 time is 9:34.
14 BY MR. CROSS:
15 Q Hi, Dr. Lee.
16 Could you please turn to page 17 of your first
17 declaration.
18 **A Page 17?**
19 Q That's right.
20 **A Paragraph 44?**
21 Q That's right.
22 **A Yes.**
23 Q Can you see the top leftmost image, it labels
24 the yellow structure there as "channel (CH)"?
25 Is that correct?

38

1 **A Yes.**
2 Q Are all of those yellow structures different
3 channels?
4 **A Yes.**
5 Q In the next figure that's diagonal, is that
6 label of "substrate" correct?
7 **A I have discussed what is a substrate, I**
8 **believe, in my declarations. Let's see. Apologize.**
9 **So in '806 patent, they explain what a**
10 **substrate is, in column 4, line 47 or so, that substrate**
11 **is a material that -- "onto which subsequent material**
12 **layers are added, or otherwise 'disposed.'" Right?**
13 **And then -- and then in column 5, '806,**
14 **row 10, '806 further say, "Substrate can be a layer, can**
15 **include one or more layers" -- "one or more layers**
16 **therein, and/or can" be -- "can have one or more layer**
17 **thereupon, thereabove, and/or therebelow."**
18 **And then further down, I believe in, yeah, row**
19 **49, in certain example, it says that, where array --**
20 **"where the array device and a peripheral device are**
21 **formed on different substrates."**
22 **So the question you have --**
23 **What page is that again? On page --**
24 Q 17?
25 **A -- 17 -- sorry -- whether the diagonal**

39

1 **components, where the yellow part is referred to as**
2 **"substrate," whether that's correct or not --**
3 **That was your question; right?**
4 Q That's right. Was that correctly labeled?
5 **A Well, this is extracted from a textbook, "3D**
6 **Flash Memories Textbook."**
7 **And depending on how substrate are defined in**
8 **the textbook, which I don't recall -- I don't have it in**
9 **front of me, unless you have it -- that I'm sure that**
10 **the author would label it accordingly.**
11 **And if -- based on '806 explanation what a**
12 **substrate is, that a substrate is a material on which --**
13 **onto which subsequent materials -- material layers are**
14 **added, or otherwise disposed. So -- and a substrate can**
15 **be a layer -- can include one or more layers therein**
16 **and/or can have one or more layer thereupon, thereabove,**
17 **and/or therebelow.**
18 **So I would think that here's the substrate,**
19 **that subsequent material layers are added and disposed,**
20 **and it can be a layer. So I don't have any reason why**
21 **it is not labeled correctly, but, again, it really**
22 **depends on what the textbook define a substrate is.**
23 **Does that make sense?**
24 Q Do you agree that the structure labeled
25 "substrate" is also a channel?

40

1 **A This is a non-NAND gate -- NAND memory devices**
2 **or planar memory devices. So when the -- when the word**
3 **lines, which is the control gates, are turned on, it**
4 **will induce a channel near the surface of the substrate.**
5 **So the substrate is not -- the question is not**
6 **really a -- is not really a precise question because the**
7 **substrate is not a channel, but the channel, which is**
8 **the electrons that carry the current, is located near**
9 **the surface of the substrate.**
10 **So I'm not sure what you mean by, is the**
11 **substrate the channel?**
12 **The channel -- the channel is -- occurs within**
13 **a substrate near the surface, between the oxide and the**
14 **silicons near the surface, close to the oxide interface.**
15 Q Previously, you agreed with me that the yellow
16 structures are different channels.
17 Are you saying that the yellow structures are
18 not channels?
19 MR. SAGDEO: Objection. Form.
20 THE WITNESS: You mean the upper corner, left-hand
21 corner?
22 BY MR. CROSS:
23 Q That's correct.
24 **A Well, I think that when I say that, yeah,**
25 **that's -- that's where the channel is, the channel is**

41

1 **occurring in the yellow regions near the silicon**
2 **dioxide/silicon interface. So, you know, roughly**
3 **speaking, you could say, well, that's -- that's the**
4 **channel.**
5 **To be more precise is where the channel**
6 **located. It's inside the yellow region near the**
7 **silicon/silicon dioxide interface.**
8 **Does that make sense to you?**
9 Q Yeah, that makes sense.
10 Let's turn to page 21 of your declaration.
11 **A 21. Okay.**
12 Q Are you there?
13 **A Yeah.**
14 Q Okay. Sorry.
15 **A No. I was waiting for your question.**
16 Q You refer to this 3D NAND architecture as Bit
17 Cost Scalable architecture, BiCS; correct?
18 **A Well, that's what it is known as. It's not my**
19 **reference. It is the -- what is known as the I -- Bit**
20 **Cost Scalable 3D NAND.**
21 Q So can you explain what the meaning of "Bit
22 Cost Scalable" is.
23 **A You mean why it is call "Bit Cost Scalable"?**
24 **Is that what you mean?**
25 Q That's right.

42

1 **A Well, if you -- I believe this is term by the**
2 **inventors of this architecture.**
3 **The primary goal of this architecture is to**
4 **deduce the Bit Cost while scaling the storage density.**
5 **So -- so, therefore, unlike planar devices, you have**
6 **stack memory that stacks vertically, and, therefore, it**
7 **increases the bit -- the bit density without stringing**
8 **the feature size, so that reduced the cost per bit.**
9 **And there are many other features of this**
10 **architecture, but I think that the reason why they call**
11 **it Bit Cost Scalable is kind of art they -- I know what**
12 **you mean, but -- but I think that it's related to reduce**
13 **the Bit Cost while scaling the density -- the storage**
14 **density.**
15 **Does that make sense?**
16 **I think that's what -- why they call that, but**
17 **I'm not quite sure. That's what it's known for, but I**
18 **believe that's what is -- the reason behind it is the**
19 **Bit Cost is reduced, meaning the cost per bit is**
20 **reduced, and the density is scale.**
21 Q Thank you.
22 So the top green element is labeled the "Bit
23 Line Selector (BLS)"; correct?
24 **A BLS -- the green part or the red part?**
25 Q Capital B, capital L, capital S. So the top

43

1 green.
2 **A Yeah. I don't recall exactly what it refers**
3 **to. It's been a while that I look at this.**
4 **And you said it's bit line select? Is that**
5 **what you're saying?**
6 Q That is what I said, but why don't you tell me
7 what you think the top green feature is.
8 MR. SAGDEO: Objection. Form.
9 THE WITNESS: I -- it makes sense that -- it makes
10 sense that that might be that -- what it stand for, but
11 I'm not sure because maybe -- let me see. I think I
12 might have -- let me see if I talk about that. I'm
13 trying to see if -- oh, I probably have discussed that
14 in my declaration. Let me -- give me a minute.
15 Yeah. If you look at -- sorry. If you look
16 at page 18, that -- in Figure A, in fact, in Figure B
17 also, BLS stand for "Bitline Selector." Not bit line
18 select. "Bitline Selector."
19 BY MR. CROSS:
20 Q Can you explain to me what the functionality
21 of a bit line selector is.
22 **A Well, bit line select -- selector is**
23 **responding -- is responsible for selecting and enable**
24 **the appropriate bit line within the NAND array.**
25 **So, therefore, it basically helps to control**

44

1 **which memory cell are access during -- during data**
2 **operations, such as read, program, and so on.**
3 Q So returning to the figure at page 21, do you
4 agree that the bit line selector is divided into four in
5 the Y direction, one for each row of channels in the Y
6 direction?
7 **A Yeah. So your individual line -- is that what**
8 **you mean?**
9 **Yeah. Sure.**
10 Q Then in red, there are eight bit lines in the
11 X direction that connect to each of the rows of channels
12 in the X direction, respectively; correct?
13 **A Eight bit lines.**
14 **So if you count the number of red lines on**
15 **the -- on the top in the Y directions, there are eight**
16 **bit lines. Eight separate bit lines. So, yeah, there's**
17 **eight of them.**
18 Q And just for clarification, those eight are
19 lined up in the X direction; correct?
20 **A Well, each bit line is in the Y direction, and**
21 **they are lined up in the X direction.**
22 Q You see that there are multiple channel gates,
23 CGs, for selecting the cells at a particular layer in
24 the Z direction; correct?
25 **A Yes.**

45

1 Q Each of these channels -- strike that.
2 Each of these channel gates is a word line;
3 correct?
4 **A I think you have the -- you use the wrong**
5 **terminology. CG does not stand for "channel gate."**
6 Q Control gate.
7 **A Yeah. If you look at page 18, CG stand for**
8 **"control gate."**
9 **So can you repeat your question, please.**
10 Q Yes. I'll start over.
11 So there are multiple control gates, CGs, for
12 selecting the cells at a particular layer in the
13 Z direction; correct?
14 **A That is correct. You can see that there's**
15 **number of layers -- of green layers in the Z direction.**
16 **Those are what is called the control gate or word lines.**
17 Q These control gates are not divided in the
18 xy-plane; correct?
19 **A What do you mean by "divided"?**
20 Q So the top layer, the bit line selector is
21 divided into four; correct?
22 MR. SAGDEO: Object to form.
23 THE WITNESS: You mean the top bit line select --
24 bit line selectors have discrete lines or, according to
25 you, there are four bit line selector, the green lines;

46

1 is that right?
2 BY MR. CROSS:
3 Q Right.
4 **A That's your question?**
5 **Yeah, that there's four discrete bit line**
6 **selector lines.**
7 Q And my question now is that the control gates
8 are not similarly divided; right?
9 **A So your question is that -- whether the**
10 **control gates, or the word lines, in each of the four**
11 **word lines that showed, right, are just one plane**
12 **instead of individual discrete line.**
13 **That's your question; right?**
14 Q That's correct.
15 **A Yeah. That -- that is correct, that word**
16 **lines are just one plane.**
17 Q So can you tell me the purpose of this
18 configuration, where the bit line selector is divided in
19 the Y direction, the bit lines themselves are divided in
20 the X direction, and the control gates are divided in
21 the Z direction?
22 **A I don't understand. What do you mean by --**
23 **you want me to explain how this works? Is that what**
24 **you -- you're asking?**
25 **So the bit line basic -- the word line**

47

1 **basically turn on the -- in the -- turn on the cells on**
2 **that plane. Right?**
3 **But you don't want to access all the -- all**
4 **the bit lines -- all the cells on that -- on the same**
5 **plane. You just want to access whether you want to do**
6 **the read or programming, that particular intersection**
7 **between the word lines and the bit line. Right?**
8 **If you want to access row 1, column 1 only,**
9 **right, then you turn on the word line of the first row,**
10 **but the turn ons all the -- basically apply voltage to**
11 **all the memory cells at the control gate of that -- on**
12 **that same plane. But you only want to access**
13 **column 1 -- row 1, column 1 in the -- the memory cell in**
14 **row 1, column 1; so, therefore, that the bit line has to**
15 **be discrete rather than on the same plane so that you**
16 **can individually access a particular column or, in other**
17 **words, a particular bit line.**
18 **Does that make sense?**
19 **If you don't -- if you do not have separate,**
20 **discrete word line -- bit lines for the bit line**
21 **selector, then you can individually select a particular**
22 **memory cells that you want to program or read or**
23 **whatnot, or erase.**
24 Q Thank you. That was helpful.
25 Can you tell me typically what is -- what are

48

1 the thicknesses of these layers?
2 MR. SAGDEO: Object to form.
3 THE WITNESS: What do you mean? It really depends
4 on the technology node you're talking about.
5 BY MR. CROSS:
6 Q Okay.
7 **A But what technology node are you talking**
8 **about? Are you talking about -- what year are you**
9 **referring to -- so --**
10 Q Generally -- oh.
11 **A I mean, it really depends on what are the --**
12 **you mean each individual gate -- control gate, the**
13 **green, and typical bit line selector control thickness?**
14 Q So --
15 **A Is that what you mean?**
16 Q -- looking at just the control gate layer,
17 what would be a typical thickness? Are we talking
18 millimeters? Microns? Nanometers?
19 MR. SAGDEO: Object to form.
20 THE WITNESS: What technology node are you talking
21 about?
22 BY MR. CROSS:
23 Q The technology node available at the time of
24 this publication.
25 **A What publications?**

49

1 Q Where you got this figure.
2 **A Where I got the figures. So this is Aritome,**
3 **which is -- 2000- -- 2016.**
4 **I would have to look at a particular road map**
5 **that -- what it is, but I can tell you that typical**
6 **thickness, for example, word lines, not in millimeters,**
7 **in nanometers.**
8 **Typically, individual control gate material,**
9 **let's say made of tungstens, are in that -- you know,**
10 **less than -- again, it depends on the technology node.**
11 **I would say around 5 to 20 nanometer. I don't know.**
12 **I -- I -- you know, all these numbers can**
13 **really pinpoint a certain year, and so -- sorry. Let me**
14 **quiet the -- let me close the door so that the cat**
15 **doesn't cause too much trouble.**
16 **I apologize. Sorry.**
17 **So 2016, I would say closer to a little bit**
18 **higher than -- higher end of the 5 to 20 nanometer.**
19 Q Thank you.
20 Moving on --
21 **A Again, I mean, I don't remember all those**
22 **number on top of my head. These are -- you can look up**
23 **quite easily, looking at the -- if I have -- if you --**
24 **do you have the Exhibit 1014? I can -- I can look at**
25 **it? Because I -- I don't have it. If you can**

50

1 **download -- upload it, I can look at it and tell you**
2 **what the thickness is.**
3 **Do you think that's necessary?**
4 Q I think we can maybe leave that for later.
5 But it's fair to say that you wouldn't expect
6 the control gate to be less than 1 nanometer or greater
7 than 100 nanometers?
8 MR. SAGDEO: Object to form.
9 THE WITNESS: Again, I -- without looking at the
10 exhibit, I would not be able to tell you, but I would
11 say that it's likely to be 20 nanometer or less, but I
12 don't know because I was told that this is not a memory
13 test and you -- you know, I don't think -- you know,
14 this is almost like memory test. Right?
15 Unless I write -- have written it, the
16 thickness of different layers, I would have to have a --
17 have the prior art in front of me to tell you what it
18 is.
19 So I would hesitate to tell you what it is at
20 a specific year at a specific time. It's specific
21 depending on the number of layers that is used in --
22 in -- in the 3D NAND and -- so, in general, I can tell
23 you that, in general, they're not in millimeter range,
24 like you said; they're in nanometer range. And the more
25 advanced chip, in general, the smaller the dimension.

51

1 BY MR. CROSS:
2 Q Okay. In your first and second declarations,
3 you included three grounds, all based on obviousness
4 over the Toyama reference; correct?
5 **A As you can see in my declaration, in -- in the**
6 **table of context -- contents, that all three ground in**
7 **each declaration are based on Toyama's prior art.**
8 Q Okay. Just to get some definitions aside, for
9 ground 1, you rely on the second modification to the
10 fourth exemplary structure.
11 Is it okay if I refer to this as the "second
12 modification"?
13 **A Are you referring to the first exhibit -- the**
14 **first declaration?**
15 Q I believe it's true in both declarations, but
16 we can focus on the first declaration.
17 **A As I explain in paragraph 85 in the first**
18 **declaration, that Toyama's second modification of the**
19 **fourth exemplary structure, which I refer to as Toyama**
20 **second modifications. And, similarly, in paragraph 104,**
21 **said the same thing. So yeah. Since I did that in --**
22 **in my declarations, so let's refer that as "second**
23 **modification" for shorthand.**
24 Q And for ground 2, this is reliant on the first
25 exemplary structure depicted in Figures 1 through 17.

52

1 Okay if I refer to this as "Toyama's first
2 exemplary structure"?
3 **A Sure. That's what I was -- that -- that's**
4 **what I refer to as -- in my declaration also.**
5 Q And for ground 3, it's an obviousness
6 combination of Toyama's second modification and first
7 exemplary structure; correct?
8 **A That is correct.**
9 Q You don't argue that Toyama anticipates any of
10 the claims; correct?
11 **A So as I explain in paragraph 85, for example,**
12 **that, in my opinion, when viewed and considered in light**
13 **of the knowledge of a POSITA, Toyama's second**
14 **modification renders claims 8 to 9 and 11 to 12 of the**
15 **'806 patent obvious. So I apply obviousness to**
16 **invalidate those claims, and I did not argue**
17 **anticipation in both of my declarations.**
18 Q Focusing on Toyama's first exemplary
19 structure, is this a Bit Cost Scalable architecture?
20 MR. SAGDEO: Object to form.
21 (Reporter clarification.)
22 THE WITNESS: Oh, I -- sorry. I just -- I didn't
23 say anything.
24 I'm not sure it is your -- whether one can say
25 the Toyama is Bit Cost Scalable because Bit Cost

53

1 Scalable is a trademark. It's a trademarked term and --
2 by Toshiba. So Toyama, looking at the '026 patent, is
3 SanDisk, but I believe that -- so your question is
4 that -- is Toyama's NAND structure a Bit Cost Scalable
5 structure?
6 Well, Bit Cost Scalable is a trademark term by
7 Toshiba and -- if I recall correctly, and Western
8 Digital, I believe.
9 So whether SanDisk -- even though Western
10 Digital acquired SanDisk at certain time, I don't know
11 whether SanDisk or Toyama will call this a Bit Cost
12 Scalable.
13 But in the background of Toyama, it does say
14 that ultra -- ultra high-density storage devices have
15 been proposed using three-dimensional (3D) stacked
16 memory stack structure, sometimes referred to as Bit
17 Cost Scalable (BiCS) architecture.
18 And this is a 3D NAND structure, but I don't
19 know what the trademark law is, whether at that time
20 Toyama would call this a Bit Cost Scalable device or
21 not, so -- but it is a 3D NAND stack memory cells --
22 memory devices that Toyama describe in his '026 patent.
23 Not sure if I answered your question.
24 BY MR. CROSS:
25 Q So like the Bit Cost Scalable architecture in

54

1 your background section of your declaration, does
2 Toyama's first exemplary structure have a bit line
3 selector that's divided in the Y direction, bit lines
4 that are divided in the X direction, and channel gates
5 divided in the Z direction?
6 MR. SAGDEO: Object to form.
7 THE WITNESS: Where are you reading?
8 BY MR. CROSS:
9 Q I'm not reading.
10 I'm simply asking, do we have the same kind of
11 division of structures as what we discussed regarding
12 the Bit Cost Scalable architecture that was in your
13 background section?
14 **A Yeah. They're very similar. But, once again,**
15 **they both are 3D NAND architecture. They both had**
16 **electrical contacts or an electrical connection formed**
17 **on top of the memory; and they both have source terminal**
18 **connected to low voltage, for example, ground; and**
19 **individual memory accessed by word line, typically**
20 **horizontal extensioned; and the word lines form**
21 **staircase structure and -- to be able to access to the**
22 **external peripheral circuit.**
23 **So in many ways, the device of Toyama are very**
24 **similar to Bit Cost Scalable architecture, but, as I**
25 **mention, that -- in my -- in my declarations, in**

55

1 **paragraph -- for example, paragraph 52, a variety of**
2 **modification to Bit Cost Scalable architecture were**
3 **known, for example, the use of slit structure and -- and**
4 **perhaps dummy string structure and so on and so forth.**
5 **So I believe that the device -- that Toyama**
6 **describe 3D NAND flash memory, but whether it can be**
7 **call Bit Cost Scalable, I think, is more a business**
8 **term, a trademark. So I cannot answer you directly**
9 **whether they can be called Bit Cost Scalable because I**
10 **don't know the legal boundary between SanDisk and**
11 **Western Digital, and so -- but no matter what you call**
12 **it, it is a 3D NAND memory cells -- memory chips.**
13 Q And is it fair to say that the Bit Cost
14 Scalable architecture in your background section and
15 Toyama's first exemplary structure would both have a bit
16 line selector that is divided in the Y direction?
17 **A Yeah. As Toyama -- in paragraph 163, it talk**
18 **about bit line sensing, bit line -- and bit line decoder**
19 **circuits, and that the bit lines are overlaying the**
20 **array of memory stack structure as connected to the**
21 **drain-side end of the vertical semiconductor channels.**
22 **So -- yeah. So the first exemplary structure**
23 **has a number of bit line layers overlaying the memory**
24 **chip.**
25 Q Turning to Toyama's second modification, like

56

1 the Bit Cost Scalable architecture in your background,
2 does Toyama's second modification have a similar bit
3 line selector that is divided in the Y direction?
4 MR. SAGDEO: Objection. Form.
5 THE WITNESS: So as I describe in the section of
6 "Overview of the Prior Art - Toyama," first, again, we
7 have to remember that Toyama is a very lengthy
8 reference. It has 70 figures, and many have subparts,
9 and over 60 columns of text, and -- but I focus on two
10 structure, which is, like I said, that first exemplary
11 structure and second modification to the fourth
12 exemplary structure, which I refer to as the second
13 modifications.
14 And as I describe in paragraph 81 at
15 Figure 17C, right, represent the -- the first -- is one
16 of the figure that describe the first exemplar.
17 BY MR. CROSS:
18 Q Sorry. I --
19 **A And then Figure 49 is one of the key figures**
20 **that describe the second modifications.**
21 Q So turning to Figure 49 of Toyama, can you
22 identify the bit line selector?
23 MR. SAGDEO: Objection. Form.
24 THE WITNESS: So the bit lines are labeled 103, the
25 bit lines that extend along the second horizontal

57

1 direction, which is perpendicular to the first
2 horizontal direction, hd1. Right?
3 So 103 is the -- the bit line -- the bit lines
4 and -- so yeah. So that's -- that's what a bit line is.
5 I don't think it shows the bit line selectors in these
6 figures.
7 BY MR. CROSS:
8 Q Is a bit line selector required?
9 MR. SAGDEO: Objection. Form.
10 THE WITNESS: I don't understand what you mean, is
11 it required.
12 Required in what sense?
13 BY MR. CROSS:
14 Q For a functional memory device of this
15 structure, do you need a bit line selector?
16 **A In Figure 49, for the Bit Cost Scalable device**
17 **by Toshiba, I believe they use the bit line selector as**
18 **we show in the figures before, and -- but not all the 3D**
19 **NAND architecture would require 3D NAND -- would require**
20 **bit line selector. So yeah. Some -- some require; some**
21 **don't.**
22 Q So my question is more specific to what's
23 illustrated in Figure 49.
24 Does Toshiba's second modification need a bit
25 line selector in order to operate?

58

1 MR. SAGDEO: Objection. Form.
2 THE WITNESS: Well, in general, 3D NAND memory
3 cells -- memory chips do not explicitly require a bit
4 line selector if, for example, it is a floating-gate --
5 floating-gate-based devices. So the -- I believe that
6 the 3 -- the Toyama make use of floating-gate materials.
7 So if -- if that's the case, then it does not
8 need -- does not need a dedicated bit line selectors,
9 but it is selected by, you know, bit line routing, and
10 so it does not need a separate BLS transistor alone.
11 BY MR. CROSS:
12 Q If you turn to paragraph 48 of your
13 declaration.
14 **A 48?**
15 **Okay.**
16 Q You explain that the drain-end select gate
17 transistor, SGD, is also known as the bit line select
18 transistor.
19 Is this all the same as the bit line selector?
20 **A Well, it's this -- different terminology.**
21 Q Different terminology for the same function
22 and structure?
23 **A So as I explained in the -- in that paragraph,**
24 **that -- that SGD, which is drain-end select transistors,**
25 **or S- -- SGC, is connected -- that at the string drain**

59

1 **end is to isolate it from the bit line. Okay?**
2 **And SG- -- SGD is also known as bit line**
3 **select transistors, or upper select gate. And so, yeah,**
4 **the SGD, in general, could also mean -- is also known as**
5 **the bit line selector.**
6 Q And this is the same thing as an upper select
7 gate; correct?
8 **A What is the same as upper select -- you said**
9 **upper select gate?**
10 Q Yeah. I'm looking at paragraph 48 of your
11 declaration. I think what you're saying is that the
12 drain-end select gate transistor is the same thing as a
13 bit line select transistor and an upper select gate.
14 **A Yeah. It's also known as the upper select**
15 **gate.**
16 Q So turning back to Toyama Figure 49, would the
17 upper select gate just be the topmost conductive layer,
18 270?
19 MR. SAGDEO: Object to form.
20 THE WITNESS: Say it again. I'm sorry.
21 BY MR. CROSS:
22 Q No, that's fine. Let me know when you're at
23 Figure 49.
24 **A Are you looking at page 49 -- 43?**
25 Q This is page 92, Figure 49 of Toyama.

60

1 **A Oh, okay. Yeah. Which is, by my declaration,**
2 **page 43.**
3 **Is that right?**
4 Q That's right. Yeah. Same figure.
5 So is the upper select gate the uppermost
6 conductive layer, 270, in Figure 49?
7 MR. SAGDEO: Object to form.
8 BY MR. CROSS:
9 Q Sorry. I think I got -- it's hard to see
10 these small numbers, but -- so let me rephrase the
11 question because the 270 is an insulating layer.
12 Would the topmost conductive layer in
13 Figure 49 be the upper select gate?
14 MR. SAGDEO: Object to form.
15 THE WITNESS: Wait. I don't understand. 270 is
16 insulated.
17 BY MR. CROSS:
18 Q Right.
19 So just beneath that is a conductive layer;
20 correct?
21 MR. SAGDEO: Object to form.
22 THE WITNESS: I -- what layer is that?
23 BY MR. CROSS:
24 Q I think it's a 242 layer -- or no. That's
25 a -- if we go to page 45 of your declaration --

61

1 **A 45.**
2 **Okay.**
3 Q -- you see that you've identified a number of
4 layers as an alternating conductor/dielectric layer
5 stack?
6 **A Right.**
7 Q Above that, what are those conductive layers?
8 **A You mean the conductive layer 246 and 146?**
9 Q I don't think that these layers are
10 specifically labeled, but you can see that you bracketed
11 a number of layers from 232 down to 132 as an
12 alternating conductor/dielectric layer stack; right?
13 **A Yes.**
14 MR. SAGDEO: Object to form.
15 BY MR. CROSS:
16 Q Do you see that above layer 232 are additional
17 conductor layers?
18 MR. SAGDEO: Object to form.
19 THE WITNESS: Yeah. I'm not sure if Toyama
20 described what they are. It might be -- it's just one
21 of space. It might be just word line. I don't know.
22 MR. CROSS: Okay. I think we can go off the
23 record.
24 THE WITNESS: Okay.
25 THE VIDEOGRAPHER: We are going off the record.

62

1 The time is 10:57.
2 (Recess was taken at 10:57 a.m. until
3 11:07 a.m.)
4 THE VIDEOGRAPHER: And we are back on the record.
5 The time is 11:07.
6 MR. CROSS: Hi, Dr. Lee. I -- thank you very much.
7 I have no further questions for you.
8 THE WITNESS: Thank you.
9 MR. SAGDEO: No redirect.
10 MR. CROSS: Great.
11 THE VIDEOGRAPHER: Okay. If there's nothing
12 further, this concludes the deposition of Jack Lee,
13 M.D. -- or Ph.D. The time is 11:07.
14 (A discussion was held off the record.)
15 THE STENOGRAPHER: Counsel, would you like to order
16 a certified copy?
17 MR. SAGDEO: For this transcript, just the sort of
18 standard final transcript.
19 (Proceedings concluded at 11:15 a.m.)
20
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63

1 CERTIFICATE OF SHORTHAND REPORTER - NOTARY PUBLIC
2
3 I, Kayla Lotstein, Certified Shorthand
4 Reporter Number 13916 within the State of California, do
5 hereby certify;
6 That JACK LEE, Ph.D., the witness whose
7 deposition is hereinbefore set forth, was duly sworn by
8 me before the commencement of such deposition and that
9 such deposition was taken before me and is a true record
10 of the testimony given by such witness.
11 I further certify that the adverse party was
12 represented by counsel at the deposition.
13 I further certify that the deposiition of JACK
14 LEE, Ph.D. occurred via videoconference on January 30,
15 2025, commencing at 8:04 a.m. PST and ending at 11:15
16 a.m. PST.
17
18 IN WITNESS WHEREOF, I have hereunto set my hand this 6th
19 day of February, 2025.
20
21 Kayla Lotstein
22
23 Kayla Lotstein, CA CSR, 13916
24
25

A
a1
6:10
able
50:10, 54:21
about
12:6, 12:9, 27:3, 27:13, 28:9, 28:10, 32:13, 33:5, 33:14, 34:7, 34:20, 34:23, 36:7, 43:12, 48:4, 48:8, 48:21, 55:18
above
61:7, 61:16
access
44:1, 47:3, 47:5, 47:8, 47:12, 47:16, 54:21
accessed
54:19
according
45:24
accordingly
39:10
acquired
53:10
actually
29:5
added
38:12, 39:14, 39:19
additional
61:16
address
8:12
advanced
50:25
advent
21:15
adverse
63:11
affect
20:19, 20:21, 21:21, 22:3, 22:14, 22:20, 23:19, 23:21, 23:22, 23:23, 24:12, 25:4, 25:7, 28:2, 28:19, 32:1, 32:7
affected
25:2
affects
20:2, 27:14, 28:6, 32:2
afford
17:7
afforded
16:22, 17:7, 18:19
after
34:17
again
28:8, 31:16, 35:10, 36:16, 38:23, 39:21, 49:10, 49:21, 50:9, 54:14, 56:6, 59:20
agree
9:13, 11:15, 39:24, 44:4
agreed
40:15
ahead
18:1
all
7:15, 9:25, 11:22, 13:10, 16:3, 22:19, 29:13, 33:14, 35:6, 35:24, 36:2, 36:16, 38:2, 47:3, 47:4, 47:10, 47:11, 49:12, 49:21, 51:3, 51:6, 57:18, 58:19
allen
3:12, 3:13, 7:19
allow
21:17
almost
50:14
alone
58:10
along
56:25
already
36:7
also
3:30, 10:11, 10:12, 12:3, 12:6, 13:11, 16:13, 18:21, 20:21, 23:11, 23:21, 24:17, 25:1, 26:2, 31:11, 31:18, 32:2, 32:16, 33:16, 39:25, 43:17, 52:4, 58:17, 59:2, 59:4, 59:14
alternating
61:4, 61:12
alto
3:16
always
34:6
ambient
26:18, 36:25
amount
26:8, 26:11, 26:15
analysis
17:8, 18:21
analyzing
15:24, 15:25, 16:23
another
21:9, 23:19, 24:2, 24:24, 25:15, 32:24
answer
6:18, 29:20, 34:25, 35:17, 55:8
answered
17:16, 53:23
answering
9:3
anticipates
52:9
anticipation
52:17
any
8:15, 8:17, 8:20, 9:9, 12:19, 12:22, 15:23, 17:18, 18:6, 18:15, 18:25, 25:18, 39:20, 52:9
anything
13:8, 52:23
anyway
34:24
apologize
38:8, 49:16
appeal
1:2, 2:2, 7:9
appear
15:12, 15:16, 17:3
appearances
3:1
application
6:9, 13:25
applied
15:23, 15:25, 17:2, 18:7
apply
32:25, 33:8, 35:13, 47:10, 52:15
applying
17:17, 18:3
appropriate
43:24
architecture
19:22, 20:10, 20:14, 20:15, 20:24, 41:16, 41:17, 42:2,

42:3, 42:10, 52:19, 53:17, 53:25, 54:12, 54:15, 54:24, 55:2, 55:14, 56:1, 57:19
area
23:1, 23:2, 23:3, 27:5, 27:9, 27:10, 30:22, 34:8, 34:12, 35:2
argue
52:9, 52:16
aritome
49:2
around
25:11, 30:10, 49:11
arranged
21:5, 25:10
array
23:16, 24:7, 28:12, 32:6, 38:19, 38:20, 43:24, 55:20
art
16:9, 16:23, 17:9, 17:13, 18:21, 18:23, 19:16, 19:23, 20:6, 20:18, 22:1, 24:11, 34:19, 36:22, 42:11, 50:17, 51:7, 56:6
aside
51:8
asking
9:2, 18:6, 28:10, 46:24, 54:10
aspect
19:12, 23:10, 31:23
aspects
35:25
assignment
12:5, 13:6, 13:14
assist
32:5
assume
9:16
assuming
36:13, 36:18
attending
7:16
attorney
16:3
attribute
21:9
austin
8:13, 32:16
author
39:10
available
48:23
avenue
3:14
aware
18:6

B

b2
5:4, 6:6
back
37:12, 59:16, 62:4
background
19:15, 20:5, 20:17, 21:25, 23:12, 24:10, 53:13, 54:1, 54:13, 55:14, 56:1
bandgap
30:7, 30:12
based
39:11, 51:3, 51:7
basic
46:25
basically
24:21, 43:25, 47:1, 47:10
because
9:24, 22:23, 24:25, 26:3, 29:5, 32:14, 34:6, 34:9, 40:6, 43:11, 49:25, 50:12, 52:25, 55:9, 60:11
become
29:10, 32:10
been
8:5, 16:6, 21:17, 37:2, 43:3, 53:15
before
1:2, 2:2, 2:21, 7:8, 9:19, 13:18, 34:16, 57:18, 63:8, 63:9
beginning
36:6
begins
7:4
behalf
2:19, 8:4
behind
42:18
being
21:13, 35:6, 35:25, 36:3
believe
15:2, 15:10, 19:14, 22:5, 29:2, 38:8, 38:18, 42:1, 42:18, 51:15, 53:3, 53:8, 55:5, 57:17, 58:5
beneath
60:19
between
18:15, 22:2, 24:20, 24:24, 25:14, 25:25, 26:2, 26:9, 26:13, 26:17, 27:3, 27:5, 40:13, 47:7, 55:10
bics
41:17, 53:17
bit
34:11, 37:3, 41:16, 41:19, 41:21, 41:23, 42:4, 42:7, 42:8, 42:11, 42:13, 42:19, 42:22, 43:4, 43:17, 43:21, 43:22, 43:24, 44:4, 44:10, 44:13, 44:16, 44:20, 45:20, 45:23, 45:24, 45:25, 46:5, 46:18, 46:19, 46:25, 47:4, 47:7, 47:14, 47:17, 47:20, 48:13, 49:17, 52:19, 52:25, 53:4, 53:6, 53:11, 53:16, 53:20, 53:25, 54:2, 54:3, 54:12, 54:24, 55:2, 55:7, 55:9, 55:13, 55:15, 55:18, 55:19, 55:23, 56:1, 56:2, 56:22, 56:24, 56:25, 57:3, 57:4, 57:5, 57:8, 57:15, 57:16, 57:17, 57:20, 57:24, 58:3, 58:8, 58:9, 58:17, 58:19, 59:1, 59:2, 59:5, 59:13
bitline
43:17, 43:18

bls
42:24, 43:17, 58:10
bls)"
42:23
board
1:2, 2:2, 7:9
both
12:13, 13:5, 13:16, 15:12, 15:16, 16:24, 16:25, 20:6, 27:10, 36:10, 51:15, 52:17, 54:15, 54:17, 55:15
bottleneck
34:15, 34:20
bottom
32:4
boundary
55:10
bracketed
61:10
break
37:4, 37:6
business
55:7
buyer
34:10

C

ca
63:23
california
1:25, 2:23, 3:16, 63:4
call
41:23, 42:10, 42:16, 53:11, 53:20, 55:7, 55:11
called
8:4, 16:12, 16:14, 16:16, 19:24, 22:19, 24:17, 30:6, 33:16, 45:16, 55:9
cannot
9:9, 55:8
capability
21:19, 22:16, 22:17
capacitance
23:20, 23:21, 24:12, 24:18, 24:20, 25:2, 25:3, 25:4, 25:8, 25:11, 26:7
capacitive
24:21, 24:23, 25:14, 25:25, 26:2, 26:8, 26:11, 26:12, 26:15, 26:16, 26:20, 26:21, 27:3, 27:7, 27:10, 27:14, 28:6
capacity
27:8
capital
42:25
carrier
29:7
carry
36:14, 36:20, 40:8
carrying
36:21
case
1:7, 2:8, 7:9, 33:9, 58:7
cat
49:14
cause
24:23, 30:16, 32:22, 33:7, 33:9, 33:11, 33:15, 49:15
causes
29:23, 30:4, 32:18, 33:3
cell
22:16, 22:22, 33:11, 44:1, 47:13
cells
21:1, 21:5, 22:12, 22:20, 22:25, 23:1, 23:3, 44:23, 45:12, 47:1, 47:4, 47:11, 47:22, 53:21, 55:12, 58:3
certain
38:19, 49:13, 53:10
certificate
63:1
certified
2:22, 62:16, 63:3
certify
63:5, 63:11, 63:13
cg
45:5, 45:7
cgs
44:23, 45:11
ch
37:24
challenged
15:12, 15:16, 16:20, 16:21, 17:6
challenging
15:6
change
31:10
channel
37:24, 39:25, 40:4, 40:7, 40:11, 40:12, 40:25, 41:4, 41:5, 44:22, 45:2, 45:5, 54:4
channels
38:3, 40:16, 40:18, 44:5, 44:11, 45:1, 55:21
charge
29:7, 29:8
chip
20:8, 20:20, 21:1, 21:22, 22:23, 23:2, 24:16, 24:19, 25:1, 29:10, 29:15, 30:5, 31:17, 32:2, 32:22, 34:8, 50:25, 55:24
chips
19:20, 21:8, 29:18, 29:21, 55:12, 58:3
circuit
29:11, 54:22
circuits
55:19
cited
12:4, 12:8
claim
15:21, 15:23, 16:1, 16:4, 16:7, 16:10, 17:6, 18:18, 19:4
claims
15:13, 15:17, 15:24, 15:25, 16:21, 17:3, 18:18, 19:6, 52:10, 52:14, 52:16
clarification
9:13, 9:15, 25:13, 26:20, 44:18, 52:21
clarify
28:8
classes
33:5
close
40:14, 49:14
closer
26:10, 49:17
code
13:24

collectively
16:11, 16:16
column
38:10, 38:13, 47:8, 47:13, 47:14, 47:16
columns
21:6, 56:9
com
3:5, 3:13
combination
52:6
come
33:13
commencement
63:8
commencing
63:15
common
20:10
commonly
20:13, 20:14
company
1:10, 2:11, 7:7
compare
15:2
components
39:1
concentrated
34:22
conclude
36:22
concluded
62:19
concludes
62:12
conducting
16:24, 30:8
conductive
24:24, 25:14, 25:15, 25:16, 25:18, 25:21, 25:23, 25:24, 26:1, 26:4, 27:23, 30:16, 34:11, 35:14, 59:17, 60:6, 60:12, 60:19, 61:7, 61:8
conductor
27:3, 33:18, 34:10, 34:21, 35:6, 61:4, 61:12, 61:17
conductors
26:9, 26:10, 26:13, 26:14, 26:18, 26:19, 27:6
configuration
46:18
confirm
16:25, 27:14
connect
44:11
connected
8:23, 54:18, 55:20, 58:25
connection
54:16
consider
13:2, 13:8, 16:13, 19:3, 23:10, 36:16
consideration
19:25, 23:19
considerations
23:18, 32:14
considered
12:5, 13:5, 13:7, 13:12, 13:15, 52:12
constant
24:14, 24:17, 24:25
construct
19:21
construction
15:21, 16:1, 16:5, 16:21, 17:6, 18:19, 19:4, 19:19
consulting
11:18
consumption
23:17
contact
28:13
contacts
23:16, 24:8, 54:16
contents
51:6
context
51:6
continuation
13:25, 14:4
continue
37:5
continued
6:1
control
40:3, 43:25, 45:6, 45:8, 45:11, 45:16, 45:17, 46:7, 46:10, 46:20, 47:11, 48:12, 48:13, 48:16, 49:8, 50:6
conversation
27:25
cooling
29:13
copy
62:16
corner
40:20, 40:21
correct
10:13, 10:24, 13:16, 13:17, 15:7, 15:9, 26:22, 27:15, 31:12, 34:2, 37:25, 38:6, 39:2, 40:23, 41:17, 42:23, 44:12, 44:19, 44:24, 45:3, 45:13, 45:14, 45:18, 45:21, 46:14, 46:15, 51:4, 52:7, 52:8, 52:10, 59:7, 60:20
correctly
14:2, 39:4, 39:21, 53:7
cost
41:17, 41:20, 41:22, 41:23, 42:4, 42:8, 42:11, 42:13, 42:19, 52:19, 52:25, 53:4, 53:6, 53:11, 53:17, 53:20, 53:25, 54:12, 54:24, 55:2, 55:7, 55:9, 55:13, 56:1, 57:16
could
8:9, 14:19, 24:15, 30:15, 33:1, 33:7, 37:16, 41:3, 59:4
counsel
3:1, 7:17, 12:6, 12:10, 62:15, 63:12
count
44:14
couple
9:20
coupling
24:22, 24:23, 25:14, 25:25, 26:2, 26:8, 26:11, 26:12, 26:15, 26:16, 26:20, 26:21, 27:3, 27:7, 27:10, 27:14, 28:6
course
17:10, 21:9, 21:22, 32:17, 33:13
courses
30:2

court
7:23
courts
16:13
cove
8:13
cover
13:24
crank
31:3
crc
1:25
create
33:1
cross
3:12, 4:5, 7:19, 8:8, 14:17, 14:24, 17:15, 17:22, 18:14, 22:10, 24:23, 27:12, 28:18, 30:14, 30:23, 31:4, 31:10, 33:24, 35:5, 35:13, 35:23, 36:10, 37:2, 37:7, 37:14, 40:22, 43:19, 46:2, 48:5, 48:22, 51:1, 53:24, 54:8, 56:17, 57:7, 57:13, 58:11, 59:21, 60:8, 60:17, 60:23, 61:15, 61:22, 62:6, 62:10
cross-sectional
34:7, 35:2
cross@ropesgray
3:13
crr
1:25
csr
1:25, 8:2, 63:23
current
25:20, 30:15, 30:20, 30:22, 31:1, 31:2, 31:4, 31:5, 31:10, 31:13, 31:14, 31:17, 32:25, 34:21, 34:23, 35:7, 35:18, 35:25, 36:4, 36:11, 36:12, 36:14, 36:20, 36:21, 36:23, 40:8
currently
8:12
cylindrical
21:6

D

data
44:1
date
5:4, 6:6, 6:11, 7:11
day
63:19
days
20:22
deal
35:22
dealing
29:5, 35:11
declaration
6:8, 9:21, 9:24, 10:8, 10:12, 12:18, 12:21, 13:18, 14:5, 17:19, 18:10, 18:11, 19:7, 19:17, 28:23, 32:4, 37:17, 41:10, 43:14, 51:5, 51:7, 51:14, 51:16, 51:18, 52:4, 54:1, 58:13, 59:11, 60:1, 60:25
declarations
12:4, 12:8, 12:24, 13:5, 13:16, 15:6, 16:2, 16:24, 16:25, 17:1, 18:5, 18:8, 18:12, 18:16, 19:1, 19:2, 19:6, 19:15, 20:6, 21:15, 24:9, 24:22, 28:14, 28:22, 36:9, 38:8, 51:2, 51:15, 51:22, 52:17, 54:25
decoder
55:18
dedicated
58:8
deduce
42:4
deep
21:16
define
19:5, 39:22
defined
22:8, 22:24, 39:7
definition
15:20
definitions
15:14, 15:18, 19:5, 51:8
degrade
29:11, 29:22, 32:12
density
19:12, 19:19, 19:24, 19:25, 20:3, 20:7, 20:19, 20:20, 20:22, 21:3, 21:8, 21:20, 21:22, 22:3, 22:14, 22:22, 22:23, 23:4, 30:15, 30:22, 31:2, 31:14, 31:18, 32:25, 35:8, 35:19, 35:25, 36:4, 36:15, 36:20, 36:21, 36:23, 42:4, 42:7, 42:13, 42:14, 42:20
density's
34:23
depending
25:9, 39:7, 50:21
depends
20:7, 20:9, 22:16, 26:9, 30:18, 30:19, 31:13, 31:17, 31:18, 34:13, 35:10, 36:24, 39:22, 48:3, 48:11, 49:10
depicted
51:25
depos
7:14, 7:24
deposiition
63:13
deposition
1:14, 2:18, 7:5, 7:15, 12:1, 12:14, 12:16, 62:12, 63:7, 63:8, 63:9, 63:12
depositions
12:14, 33:6
describe
28:13, 53:22, 55:6, 56:5, 56:14, 56:16, 56:20
described
19:6, 24:9, 61:20
describing
27:1, 27:11
description
5:2, 6:4

descriptions
15:3
designed
19:9
designing
19:12, 20:1, 23:9, 29:1, 31:22
desktop
29:13
detailed
30:9
details
9:25, 12:7, 21:24, 35:1, 36:17
device
22:13, 23:20, 27:19, 28:20, 32:5, 32:7, 32:12, 35:12, 38:20, 53:20, 54:23, 55:5, 57:14, 57:16
devices
19:10, 19:13, 20:1, 20:3, 20:25, 23:9, 29:1, 31:22, 33:6, 33:10, 40:1, 40:2, 42:5, 53:14, 53:22, 58:5
diagonal
38:5, 38:25
dictionary
16:15
dielectric
31:18, 33:7, 35:14, 61:4, 61:12
dielectrics
26:19
differences
18:15
different
15:24, 17:18, 18:3, 18:7, 18:25, 24:20, 25:10, 25:20, 26:21, 26:25, 38:2, 38:21, 40:16, 50:16, 58:20, 58:21
digital
53:8, 53:10, 55:11
dimension
22:8, 50:25
dioxide
41:2, 41:7
directed
28:25
direction
44:5, 44:6, 44:11, 44:12, 44:19, 44:20, 44:21, 44:24, 45:13, 45:15, 46:19, 46:20, 46:21, 54:3, 54:4, 54:5, 55:16, 56:3, 57:1, 57:2
directions
44:15
directly
55:8
discrete
45:24, 46:5, 46:12, 47:15, 47:20
discuss
12:9, 13:11, 14:15, 17:10, 19:18, 20:4, 20:16, 20:21, 21:10, 21:15, 21:23, 23:11, 23:14, 24:22, 32:3, 32:20, 32:24, 36:7, 36:17
discussed
12:6, 14:5, 14:7, 14:23, 15:8, 19:14, 24:9, 28:21, 38:7, 43:13, 54:11
discussion
21:25, 36:7, 62:14
discussions
36:8
disposed
38:12, 39:14, 39:19
distance
26:9, 26:13, 26:17, 27:5
distances
22:2
distributions
32:6
divide
27:9
divided
44:4, 45:17, 45:19, 45:21, 46:8, 46:18, 46:19, 46:20, 54:3, 54:4, 54:5, 55:16, 56:3
division
54:11
document
10:2
documents
12:2, 12:7
door
49:14
down
38:18, 61:11
download
50:1
downloaded
11:11, 12:3
dr
8:9, 10:2, 11:25, 19:9, 23:7, 33:17, 37:2, 37:15, 62:6
drain
58:25
drain-end
58:16, 58:24, 59:12
drain-side
55:21
drawing
15:3
dry
21:15
due
29:6, 30:12
duly
8:5, 63:7
dummy
32:5, 32:21, 55:4
during
32:5, 44:1

E

each
12:4, 12:8, 22:21, 26:6, 44:5, 44:11, 44:20, 45:1, 45:2, 46:10, 48:12, 51:7
earlier
28:9, 32:24
easily
49:23
east
3:16
effect
21:21
eight
44:10, 44:13, 44:15, 44:16, 44:17, 44:18
either
13:19
electrical
54:16
electrodes
24:20

electromagnetically
25:19
electron
24:1, 24:5, 29:4, 30:7, 30:9
electrons
29:7, 30:10, 40:8
element
24:24, 24:25, 25:14, 25:15, 25:18, 25:21, 25:23, 26:1, 42:22
elements
25:16, 25:24, 26:1, 26:4, 27:24, 30:16
else
24:3, 36:13
elucidate
24:15
enable
43:23
end
49:18, 55:21, 59:1
ending
63:15
engineers
35:20, 35:21
enhance
23:16, 24:8
enhanced
28:13
enough
33:8
entire
35:1
environment
32:17
equal
35:7, 35:25, 36:3
equivalent
22:7
erase
47:23
esq
3:4, 3:12
essentially
31:13
etching
21:12, 21:13, 21:16, 21:17, 21:18, 22:17, 22:19
even
29:14, 53:9
ever
19:9
everything
24:3, 31:3, 36:13, 36:19
evidence
16:12, 16:14, 16:16, 16:18, 16:19, 17:14, 18:22
exact
12:11
exactly
22:24, 43:2
examination
8:7
examinations
4:3
examined
8:5
example
19:7, 19:17, 20:9, 20:22, 21:14, 21:16, 23:14, 24:7, 25:16, 28:12, 32:3, 32:21, 32:24, 33:4, 34:15, 38:19, 49:6, 52:11, 54:18, 55:1, 55:3, 58:4
examples
21:7, 32:18, 33:3
exemplar
56:16
exemplary
51:10, 51:19, 51:25, 52:2, 52:7, 52:18, 54:2, 55:15, 55:22, 56:10, 56:12
exhibit
5:3, 6:5, 6:8, 6:9, 9:22, 10:13, 13:11, 13:12, 13:13, 14:18, 14:19, 14:20, 49:24, 50:10, 51:13
exhibits
5:1, 6:3
expect
33:19, 34:1, 50:5
expert
16:14
expertise
29:1
explain
16:1, 38:9, 41:21, 43:20, 46:23, 51:17, 52:11, 58:16
explained
17:5, 58:23
explanation
39:11
explicitly
58:3
extend
56:25
extensioned
54:20
external
54:22
extracted
39:5
extrinsic
16:14, 16:16, 16:17, 17:14, 18:22

F

fabricated
20:25, 21:1
fabrication
19:20, 21:11, 22:16
fact
31:24, 43:16
factors
23:13
fair
9:17, 50:5, 55:13
familiar
10:21, 11:3, 14:9
fan
29:13, 29:17
faster
29:4
feature
22:2, 22:5, 22:6, 23:6, 42:8, 43:7
features
20:7, 30:12, 42:9
february
63:19
few
12:12
field
22:6
figure
38:5, 43:16, 44:3, 49:1, 56:15, 56:16, 56:19, 56:21, 57:16, 57:23, 59:16, 59:23, 59:25, 60:4, 60:6, 60:13
figures
49:2, 51:25, 56:8, 56:19, 57:6, 57:18
file
9:21, 11:8, 16:11
filed
10:11, 11:4,

13:25, 15:6, 17:1, 17:2
final 62:18
finally 11:3
find 12:19, 12:22
fine 59:22
finish 9:6
first 10:7, 12:18, 16:3, 32:4, 37:16, 47:9, 51:2, 51:13, 51:14, 51:16, 51:17, 51:24, 52:1, 52:6, 52:18, 54:2, 55:15, 55:22, 56:6, 56:10, 56:15, 56:16, 57:1
flash 19:19, 20:11, 20:12, 20:13, 20:14, 20:18, 20:19, 20:23, 21:5, 39:6, 55:6
flashes 21:4
floating-gate 58:4, 58:6
floating-gate-based 58:5
floor 3:15
focus 51:16, 56:9
focusing 52:18
follows 8:6
form 17:4, 17:21, 18:9, 22:4, 26:23, 28:7, 29:25, 33:20, 33:21, 34:2, 34:3, 35:7, 35:9, 36:3, 36:5, 40:19, 43:8, 45:22, 48:2, 48:19, 50:8, 52:20, 54:6, 54:20, 56:4, 56:23, 57:9, 58:1, 59:19, 60:7, 60:14, 60:21, 61:14, 61:18
formed 38:21, 54:16
formulated 12:25
formulating 13:2
forth 31:20, 35:4, 55:4, 63:7
forward 10:25
found 21:24
four 12:2, 12:7, 44:4, 45:21, 45:25, 46:5, 46:10
fourth 51:10, 51:19, 56:11
front 8:15, 13:22, 39:9, 50:17
fully 9:10
function 58:21
functional 57:14
functionality 43:20
further 16:21, 17:6, 18:19, 38:14, 38:18, 62:7, 62:12, 63:11, 63:13

G

gate 40:1, 45:5, 45:6, 45:8, 45:16, 47:11, 48:12, 48:16, 49:8, 50:6, 58:16, 59:3, 59:7, 59:9, 59:12, 59:13, 59:15, 59:17, 60:5, 60:13
gates 40:3, 44:22, 45:2, 45:11, 45:17, 46:7, 46:10, 46:20, 54:4
general 22:12, 24:16, 29:2, 30:6, 34:5, 50:22, 50:23, 50:25, 58:2, 59:4
generally 16:7, 29:1, 48:10
geometry 31:1, 31:10, 33:25, 35:12
germanium 30:11
give 24:21, 32:18, 35:1, 43:14
given 16:7, 16:18, 18:21, 18:25, 23:2, 24:3, 63:10
go 9:19, 18:1, 24:2, 24:5, 29:4, 29:23, 30:5, 30:12, 30:17, 30:24, 31:6, 31:11, 60:25, 61:22
goal 42:3
goes 29:22
going 10:25, 17:24, 37:2, 37:8, 61:25
good 8:9
gray 3:11, 7:19
great 10:4, 10:6, 10:10, 10:20, 11:12, 11:17, 62:10
greater 50:6
greatest 35:8, 36:4
green 42:22, 42:24, 43:1, 43:7, 45:15, 45:25, 48:13
ground 51:6, 51:9, 51:24, 52:5, 54:18
grounds 51:3

H

hand 63:18
hard 22:18, 60:9
hd1 57:2
head 49:22

heard
24:14
heat
29:15, 29:17, 31:19, 32:6, 33:9
held
62:14
hello
8:1
helpful
47:24
helps
43:25
here
7:4, 20:17
here's
39:18
hereby
63:5
hereinbefore
63:7
hereunto
63:18
herrington
3:3, 7:21
hesitate
50:19
hi
37:15, 62:6
high
29:18, 32:1, 32:25, 36:20, 36:23
high-aspect
21:18
high-density
19:21, 53:14
higher
19:18, 20:18, 26:10, 29:3, 35:19, 36:14, 36:15, 36:23, 36:24, 49:18
history
13:13, 16:11
hold
14:6, 14:11
holes
29:8
horizontal
54:20, 56:25, 57:2
hot
29:10, 32:7, 32:9, 32:10, 32:11, 32:19, 32:23, 33:2, 33:4, 33:9, 33:11, 33:16, 33:20, 34:2, 34:24, 35:7, 35:18, 36:3
hour
11:20, 37:3
however
30:25

I

identification
14:21
identified
61:3
identify
56:22
illustrated
57:23
image
37:23
imagine
24:4, 36:18
important
19:12, 19:25, 21:9, 23:10, 23:12, 23:18, 31:23, 31:24, 32:14
improve
21:2
improved
21:14
inaccuracies
12:19, 12:22
inadvertent
33:10
inadvertently
25:1
inc
1:3, 2:4
include
38:15, 39:15
included
51:3
including
29:21, 36:25
incorporated
7:6
increase
21:2, 21:18, 21:19, 26:6, 29:9, 30:15, 30:19, 30:20, 31:1, 33:7, 33:15
increased
21:8
increases
31:2, 42:7
increasing
30:20
index
4:1, 6:1
indirect
30:7, 30:12
individual
44:7, 46:12, 48:12, 49:8, 54:19
individually
47:16, 47:21
induce
40:4
induced
25:20
industry
30:2, 32:17
information
6:13
informed
16:6
input
24:5
inside
41:6
instead
46:12
instructed
6:18
insulated
60:16
insulating
60:11
integration
19:18, 19:25, 20:2, 20:18, 21:3, 21:19, 21:22, 22:3, 22:14, 22:22, 22:23, 23:4
interconnect
23:23, 24:6, 25:7, 25:9, 28:11, 28:12, 30:25, 33:1, 34:16
interconnects
23:15, 24:3, 24:7, 25:5, 25:17, 25:19, 25:21, 25:23, 25:24, 26:3, 26:4, 26:5, 28:1, 30:21, 31:19
interface
40:14, 41:2, 41:7
intersection
47:6
intrinsic
16:12, 16:18, 17:14, 18:22
invalidate
52:16
invention
16:9, 17:13, 18:23
inventor's
16:15
inventors
42:2
inversely
26:12, 26:17, 27:5

involve
21:11, 22:17
involves
19:20
ion
21:17
ipr
1:8, 2:9, 7:9, 9:21, 10:12, 11:19
iprs
15:6, 15:8
isolate
59:1
itself
21:11, 31:14

J

jack
1:14, 2:18, 4:2, 6:8, 7:5, 8:3, 8:11, 62:12, 63:6, 63:13
january
1:16, 2:20, 7:1, 63:14
july
14:1
june
6:11

K

kayla
1:24, 2:21, 7:24, 8:1, 63:3, 63:23
key
56:19
kind
29:14, 31:18, 31:19, 42:11, 54:10
know
14:7, 32:22, 33:6, 34:20, 41:2, 42:11, 49:9, 49:11, 49:12, 50:12, 50:13, 53:10, 53:19, 55:10, 58:9, 59:22, 61:21
knowledge
52:13
known
41:18, 41:19, 42:17, 55:3, 58:17, 59:2, 59:4, 59:14

L

label
38:6, 39:10
labeled
9:22, 14:17, 39:4, 39:21, 39:24, 42:22, 56:24, 61:10
labels
37:23
language
16:10, 17:20
laptop
8:16, 8:18, 8:23, 29:13
larger
11:8, 22:21, 23:1
last
12:12
later
50:4
law
16:4, 16:5, 53:19
layer
27:23, 34:8, 38:14, 38:16, 39:15, 39:16, 39:20, 44:23, 45:12, 45:20, 48:16, 59:17, 60:6, 60:11, 60:12, 60:19, 60:22, 60:24, 61:4, 61:8, 61:12, 61:16
layers
38:12, 38:15, 39:13, 39:15, 39:19, 45:15, 48:1, 50:16, 50:21, 55:23, 61:4, 61:7, 61:9, 61:11, 61:17
learn
33:14
learned
16:15
leave
50:4
lee
1:14, 2:18, 4:2, 6:8, 7:5, 8:3, 8:9, 8:11, 10:2, 11:25, 19:9, 23:7, 33:17, 37:2, 37:15, 62:6, 62:12, 63:6, 63:14
left-hand
40:20
leftmost
37:23
legal
55:10
length
12:11, 23:15, 23:23, 24:6, 26:16, 26:21, 28:1, 28:10, 28:11, 36:10
lengthwise
26:6
lengthy
56:7
less
16:18, 36:12, 36:21, 49:10, 50:6, 50:11
let's
14:7, 18:15, 37:6, 38:8, 41:10, 49:9, 51:22
light
52:12
likely
31:6, 36:15, 36:22, 50:11
limited
7:7
line
6:14, 6:19, 30:20, 34:11, 34:12, 38:10, 42:23, 43:4, 43:17, 43:21, 43:22, 43:24, 44:4, 44:7, 44:20, 45:2, 45:20, 45:23, 45:24, 45:25, 46:5, 46:12, 46:18, 46:25, 47:7, 47:9, 47:14, 47:17, 47:20, 48:13, 54:2, 54:19, 55:16, 55:18, 55:23, 56:3, 56:22, 57:3, 57:4, 57:5, 57:8, 57:15, 57:17, 57:20, 57:25, 58:4, 58:8, 58:9, 58:17, 58:19, 59:1, 59:2, 59:5, 59:13, 61:21
lined
44:19, 44:21
lines
34:10, 34:11, 40:3, 44:10, 44:13, 44:14, 44:16, 45:16, 45:24, 45:25, 46:6, 46:10,

46:11, 46:16, 46:19, 47:4, 47:7, 47:20, 49:6, 54:3, 54:20, 55:19, 56:24, 56:25, 57:3
list 13:10
listed 13:5, 13:10, 13:14
lists 13:9
little 37:2, 49:17
llp 3:3, 3:11
local 32:7, 32:9, 32:11, 32:19, 32:23, 33:2, 33:4, 33:9, 33:11, 33:15, 33:16, 33:20, 34:2, 34:24, 35:7, 35:18
locally 32:10, 33:16
located 8:12, 40:8, 41:6
long 12:9, 24:1
longer 24:2, 24:4, 26:5
look 43:3, 43:15, 45:7, 49:4, 49:22, 49:24, 50:1
looking 48:16, 49:23, 50:9, 53:2, 59:10, 59:24
lot 21:23, 24:19
lotstein 1:24, 2:21, 7:24, 8:2, 63:3, 63:23
low 33:22, 54:18
lower 22:22, 23:2, 23:4

M

made 35:3, 49:9
mainly 20:10
maintain 30:25, 31:9
make 14:11, 14:16, 29:15, 29:18, 31:7, 39:23, 41:8, 42:15, 47:18, 58:6
makes 31:8, 41:9, 43:9
management 35:20
many 30:18, 36:25, 42:9, 54:23, 56:8
map 49:4
march 6:7
marked 6:3, 10:12, 14:19, 14:20
mask 22:18
material 30:7, 35:14, 35:15, 38:11, 39:12, 39:13, 39:19, 49:8
materials 8:14, 12:4, 12:5, 12:7, 12:10, 13:2, 13:4, 13:6, 13:13, 13:15, 35:16, 37:1, 39:13, 58:6
matter 7:5, 16:5, 55:11
matters 11:23, 12:25
maybe 43:11, 50:4
mean 10:8, 15:19, 15:21, 18:10, 18:11, 22:6, 25:6, 25:7, 26:24, 27:16, 27:20, 27:22, 33:12, 33:23, 34:4, 40:10, 40:20, 41:23, 41:24, 42:12, 44:8, 45:19, 45:23, 46:22, 48:3, 48:11, 48:12, 48:15, 49:21, 57:10, 59:4, 61:8
meaning 15:24, 16:7, 16:22, 17:2, 17:8, 17:11, 17:18, 18:3, 18:7, 18:20, 19:1, 20:25, 24:3, 25:3, 34:21, 41:21, 42:19
means 14:4, 20:24, 22:7, 23:1, 31:2, 32:9
meetings 12:13
memories 39:6
memory 1:9, 2:10, 7:6, 19:9, 19:13, 19:20, 19:24, 20:1, 20:3, 20:7, 20:8, 20:11, 20:20, 20:25, 21:1, 21:4, 21:5, 21:8, 21:22, 22:13, 22:15, 22:20, 22:22, 22:23, 22:25, 23:1, 23:3, 23:9, 27:19, 27:24, 28:20, 29:1, 31:22, 32:2, 32:6, 32:22, 33:10, 40:1, 40:2, 42:6, 44:1, 47:11, 47:13, 47:22, 50:12, 50:14, 53:16, 53:21, 53:22, 54:17, 54:19, 55:6, 55:12, 55:20, 55:23, 57:14, 58:2, 58:3
mention 18:18, 24:10, 54:25
mentioned 13:4, 20:16, 22:17, 25:13, 28:1
metal 33:7, 34:8
micron 1:3, 2:4, 7:5, 7:22
microns 48:18
might 14:5, 19:2, 34:24, 43:10, 43:12, 61:20,

61:21
millimeter
50:23
millimeters
48:18, 49:6
mind
11:7
minute
43:14
mobility
29:6
modification
51:9, 51:12, 51:18, 51:23, 52:6, 52:14, 55:2, 55:25, 56:2, 56:11, 57:24
modifications
51:20, 56:13, 56:20
monitor
7:12, 8:22
monitors
8:22
more
21:23, 22:11, 29:1, 36:11, 38:15, 38:16, 39:15, 39:16, 41:5, 50:24, 55:7, 57:22
morning
8:9
most
20:10, 34:22
move
21:3, 30:10
moving
49:20
much
23:7, 36:24, 49:15, 62:6
multiple
44:22, 45:11

N

name
8:1, 8:10
nand
19:18, 19:20, 20:11, 20:14, 20:18, 20:22, 21:4, 40:1, 41:16, 41:20, 43:24, 50:22, 53:4, 53:18, 53:21, 54:15, 55:6, 55:12, 57:19, 58:2
nanometer
49:11, 49:18, 50:6, 50:11, 50:24
nanometers
48:18, 49:7, 50:7
narrow
34:16, 34:17
narrower
34:1, 34:2
nd
3:6
near
40:4, 40:8, 40:13, 40:14, 41:1, 41:6
nearby
24:25, 25:20, 26:1, 26:3
necessarily
34:4
necessary
50:3
need
57:15, 57:24, 58:8, 58:10
negative
29:7
neighboring
25:25, 26:3, 26:6
net
27:6, 27:24
new
3:7
next
38:5
node
22:8, 48:4, 48:7, 48:20, 48:23, 49:10
noise
23:21
non-nand
40:1
none
6:15, 6:20
nonuniform
33:6
notary
63:1
nothing
62:11
notice
2:23, 29:12
number
8:2, 9:25, 11:4, 12:12, 14:10, 14:12, 22:25, 23:2, 36:12, 44:14, 45:15, 49:22, 50:21, 55:23, 61:3, 61:11, 63:4
numbers
7:9, 49:12, 60:10

O

oath
8:25
object
26:23, 28:7, 45:22, 48:2, 48:19, 50:8, 52:20, 54:6, 59:19, 60:7, 60:14, 60:21, 61:14, 61:18
objection
17:4, 17:21, 18:9, 22:4, 29:25, 33:21, 34:3, 35:9, 36:5, 40:19, 43:8, 56:4, 56:23, 57:9, 58:1
obvious
33:3, 52:15
obviously
22:15, 22:21, 26:10, 26:14, 31:24
obviousness
51:3, 52:5, 52:15
occur
25:25, 26:2
occurred
63:14
occurring
41:1
occurs
35:18, 40:12
offer
16:3, 19:18
offers
20:18
office
1:1, 2:1, 7:8
oh
18:1, 43:13, 48:10, 52:22, 60:1
okay
8:17, 8:23, 9:5, 11:11, 17:16, 24:16, 24:20, 26:15, 31:15, 32:10, 35:6, 37:7, 41:11, 41:14, 48:6, 51:2, 51:8, 51:11, 52:1, 58:15, 59:1, 60:1, 61:2, 61:22, 61:24, 62:11
old
20:22
once
54:14

one
10:7, 10:17, 10:23, 14:6, 14:11, 14:15, 18:7, 20:19, 21:2, 23:17, 24:2, 24:4, 24:24, 25:14, 27:2, 29:16, 35:21, 36:9, 36:11, 36:12, 36:20, 38:15, 38:16, 39:15, 39:16, 44:5, 46:11, 46:16, 52:24, 56:15, 56:19, 61:20
only
20:24, 23:21, 24:23, 26:17, 31:17, 32:1, 47:8, 47:12
ons
47:10
opened
8:17
operate
57:25
operating
28:19, 29:9, 29:10, 29:23
operation
23:9, 28:20, 29:21, 31:3, 32:5
operations
32:1, 44:2
opinion
16:20, 52:12
opinions
12:24, 13:3, 16:4
order
19:21, 35:17, 57:25, 62:15
ordinary
16:7, 16:9, 16:22, 17:2, 17:7, 17:11, 17:12, 18:20, 18:23, 19:23, 34:19, 36:21
orrick
3:3, 7:21
other
8:20, 16:15, 18:8, 20:21, 25:11, 26:6, 26:11, 34:1, 35:24, 42:9, 47:16
otherwise
38:12, 39:14
output
24:5
outside
13:8
over
21:14, 37:3, 45:10, 51:4, 56:9
overlap
27:4
overlaying
55:19, 55:23
overprogramming
33:11
overview
56:6
owner
1:12, 2:13, 2:19, 3:10, 7:20, 8:4
oxide
40:13, 40:14

P

pacific
7:12
pack
23:3
page
4:4, 5:2, 6:14, 6:19, 9:25, 32:3, 32:4, 37:16, 37:18, 38:23, 41:10, 43:16, 44:3, 45:7, 59:24, 59:25, 60:2, 60:25
palo
3:16
paragraph
16:2, 19:7, 37:20, 51:17, 51:20, 52:11, 55:1, 55:17, 56:14, 58:12, 58:23, 59:10
parallel
20:14
parasitic
23:20, 23:21, 24:12, 25:2, 25:4, 25:8, 25:11, 26:7
parker
3:31, 7:13
part
32:15, 34:21, 39:1, 42:24
parth
3:4, 7:21
particular
18:2, 22:13, 35:11, 44:23, 45:12, 47:6, 47:16, 47:17, 47:21, 49:4
parties
7:15
party
63:11
patent
1:1, 1:2, 1:10, 1:12, 2:1, 2:2, 2:11, 2:13, 2:19, 3:10, 5:3, 5:5, 6:5, 6:7, 6:9, 7:8, 7:19, 8:4, 10:21, 10:23, 10:25, 11:3, 12:15, 12:16, 13:12, 13:21, 14:1, 14:9, 14:13, 14:22, 14:25, 15:7, 18:11, 18:13, 18:17, 20:6, 38:9, 52:15, 53:2, 53:22
patterning
21:12, 22:18
perhaps
55:4
peripheral
38:20, 54:22
permittivity
26:18
perpendicular
57:1
person
16:8, 17:12, 18:22, 19:23, 34:18, 36:21
petitioner
1:5, 2:6, 3:2, 7:22
petitions
13:19
ph
1:14, 2:18, 4:2, 6:8, 7:5, 8:3, 62:13, 63:6, 63:14
phenomena
27:1, 27:11, 29:6
phrase
16:8
pinpoint
49:13
place
12:15, 12:17, 24:2
placement
35:15
places
19:18
plain
16:7, 16:22,

17:2, 17:7, 17:11, 18:20
planar 20:23, 20:24, 40:2, 42:5
plane 46:11, 46:16, 47:2, 47:5, 47:12, 47:15
planet 7:14, 7:24
please 7:17, 8:9, 9:5, 11:1, 11:18, 14:13, 15:15, 17:23, 37:16, 45:9
posita 52:13
positive 29:8
possible 9:23
power 23:17
pr 7:10
precise 40:6, 41:5
prefaced 35:24, 36:2
preparation 12:14, 12:16
prepare 11:25
present 3:30
pretty 14:15
previously 6:3, 40:15
primary 42:3
prior 16:23, 17:8, 18:21, 50:17, 51:7, 56:6
probably 43:13
problems 35:11
proceed 9:19
proceedings 62:19
process 21:16
program 44:2, 47:22
programming 47:6
programs 8:17
proportional 26:12, 26:17, 27:4, 27:5
proposed 53:15
prosecution 13:13
provide 8:14
psagdeo@orrick 3:5
pst 63:15, 63:16
pub 6:11
public 63:1
publication 6:10, 11:4, 48:24
publications 48:25
pump 36:11, 36:12
purpose 16:23, 17:8, 18:20, 46:17
pursuant 2:23
put 29:14

Q

question 9:12, 9:16, 17:17, 17:25, 19:3, 25:22, 28:4, 28:25, 29:20, 30:4, 34:25, 35:24, 36:2, 38:22, 39:3, 40:5, 40:6, 41:15, 45:9, 46:4, 46:7, 46:9, 46:13, 53:3, 53:23, 57:22, 60:11
questions 6:18, 9:3, 31:25, 35:1, 35:17, 62:7
quiet 49:14
quite 42:17, 49:23

R

range 50:23, 50:24
rate 11:18, 11:22
rather 47:15
ratio 21:18
rc 24:14, 24:17, 24:25
reactive 21:16
read 14:2, 44:2, 47:6, 47:22
reading 54:7, 54:9
reads 13:24
really 34:13, 34:18, 34:25, 35:10, 36:16, 36:24, 39:21, 40:6, 48:3, 48:11, 49:13
reason 9:9, 32:13, 39:20, 42:10, 42:18
reasons 29:16
recall 12:11, 12:23, 18:24, 18:25, 19:2, 19:3, 39:8, 43:2, 53:7
receive 10:2
received 10:5, 10:19
recess 37:10, 62:2
record 16:12, 16:17, 37:8, 37:12, 61:23, 61:25, 62:4, 62:14, 63:9
red 42:24, 44:10, 44:14
redirect 62:9
reduce 23:17, 28:2, 42:12
reduced 26:16, 42:8, 42:19, 42:20
reduces 29:8
reducing 23:15, 24:6, 28:1, 28:11, 32:7
refer 10:7, 10:11, 10:24, 18:4, 25:22, 41:16, 51:11, 51:19, 51:22, 52:1,

52:4, 56:12
reference
11:14, 41:19, 51:4, 56:8
referred
20:13, 20:15, 28:14, 39:1, 53:16
referring
11:13, 22:9, 22:11, 28:3, 28:9, 28:16, 34:13, 48:9, 51:13
refers
43:2
reflect
12:24
refrigerations
29:15, 29:17
regarding
54:11
region
41:6
regions
35:3, 41:1
related
22:25, 23:5, 24:17, 31:25, 42:12
reliability
31:22, 32:2, 32:8, 32:12, 32:14
reliant
51:24
rely
51:9
remain
30:23, 31:3, 34:15, 36:13
remained
34:20, 36:19
remember
9:24, 49:21, 56:7
remote
7:13
remotely
7:16
renders
52:14
repeat
15:15, 45:9
rephrase
15:22, 28:5, 31:9, 60:10
reported
1:23
reporter
2:22, 7:23, 52:21, 63:1, 63:4
represent
7:18, 24:18, 56:15
represented
63:12
representing
7:14, 7:24
require
16:21, 17:6, 18:19, 57:19, 57:20, 58:3
required
57:8, 57:11, 57:12
research
32:15
resistance
24:18, 34:13
respectively
44:12
responding
43:23
responsible
43:23
restate
28:5
restricted
34:22
result
25:10
returning
44:3
review
12:3, 13:11, 13:19
reviewed
12:2, 12:18, 12:21
right
12:17, 18:6, 37:19, 37:21, 38:12, 39:3, 39:4, 41:25, 46:1, 46:3, 46:8, 46:11, 46:13, 47:2, 47:7, 47:9, 50:14, 56:15, 57:2, 60:3, 60:4, 60:18, 61:6, 61:12
road
49:4
room
8:21
ropes
3:11, 7:19
roughly
41:2
routing
58:9
row
38:14, 38:18, 44:5, 47:8, 47:9, 47:13, 47:14
rows
44:11
rpr
1:25

S

s
58:25
sagdeo
3:4, 7:21, 17:4, 17:21, 18:9, 22:4, 26:23, 28:7, 29:25, 33:21, 34:3, 35:9, 36:5, 40:19, 43:8, 45:22, 48:2, 48:19, 50:8, 52:20, 54:6, 56:4, 56:23, 57:9, 58:1, 59:19, 60:7, 60:14, 60:21, 61:14, 61:18, 62:9, 62:17
said
18:24, 28:11, 34:17, 43:4, 43:6, 50:24, 51:21, 56:10, 59:8
same
9:7, 11:22, 15:1, 15:4, 15:13, 15:17, 17:20, 24:4, 27:1, 27:11, 30:23, 30:25, 31:2, 31:3, 31:4, 31:9, 34:15, 34:20, 34:23, 36:10, 36:13, 36:19, 47:4, 47:12, 47:15, 51:21, 54:10, 58:19, 58:21, 59:6, 59:8, 59:12, 60:4
sandisk
53:3, 53:9, 53:10, 53:11, 55:10
say
10:23, 19:4, 22:5, 27:7, 27:16, 38:14, 40:24, 41:3, 49:9, 49:11, 49:17, 50:5, 50:11, 52:23, 52:24, 53:13, 55:13, 59:20

saying
40:17, 43:5, 59:11
says
38:19
scalable
41:17, 41:20, 41:22, 41:23, 42:11, 52:19, 52:25, 53:1, 53:4, 53:6, 53:12, 53:17, 53:20, 53:25, 54:12, 54:24, 55:2, 55:7, 55:9, 55:14, 56:1, 57:16
scale
42:20
scaling
42:4, 42:13
screens
8:20
second
10:12, 12:21, 14:6, 14:11, 51:2, 51:9, 51:11, 51:18, 51:20, 51:22, 52:6, 52:13, 55:25, 56:2, 56:11, 56:12, 56:20, 56:25, 57:24
section
16:2, 17:5, 17:11, 21:10, 23:14, 24:10, 30:23, 31:5, 31:11, 35:13, 36:10, 54:1, 54:13, 55:14, 56:5
sections
12:5, 13:6, 13:11, 13:14, 20:4, 20:17, 21:25
see
14:7, 22:25, 37:23, 38:8, 43:11, 43:12, 43:13, 44:22, 45:14, 51:5, 60:9, 61:3, 61:10, 61:16
select
43:4, 43:18, 43:22, 45:23, 47:21, 58:16, 58:17, 58:24, 59:3, 59:6, 59:8, 59:9, 59:12, 59:13, 59:14, 59:17, 60:5, 60:13
selected
58:9
selecting
43:23, 44:23, 45:12
selective
22:19
selector
42:23, 43:17, 43:18, 43:21, 43:22, 44:4, 45:20, 45:25, 46:6, 46:18, 47:21, 48:13, 54:3, 55:16, 56:3, 56:22, 57:8, 57:15, 57:17, 57:20, 57:25, 58:4, 58:19, 59:5
selectors
45:24, 57:5, 58:8
semiconductor
22:6, 29:21, 30:10, 30:16, 55:21
sense
31:7, 31:8, 39:23, 41:8, 41:9, 42:15, 43:9, 43:10, 47:18, 57:12
sensing
55:18
separate
26:19, 44:16, 47:19, 58:10
series
20:15
set
18:7, 18:8, 63:7, 63:18
several
12:12
sg
59:2
sgc
58:25
sgd
58:17, 58:24, 59:2, 59:4
share
14:25
short
26:15, 30:1, 30:9, 32:17, 37:4, 37:6
shorthand
2:22, 51:23, 63:1, 63:3
should
11:8
show
57:18
showed
46:11
shows
57:5
shrink
22:14
side
15:2
signal
23:12, 23:16, 23:24, 24:8, 24:13, 25:19, 27:13, 27:15, 27:16, 27:17, 27:19, 27:20, 27:22, 27:23, 27:24, 28:2, 28:6, 28:9, 28:13, 28:14
signature-p1kal
63:21
signed
13:18
significantly
21:14, 31:16
silicon
30:6, 30:8, 30:11, 30:13, 41:1, 41:2, 41:7
silicon-germanium
30:11
silicons
40:14
similar
15:4, 54:14, 54:24, 56:2
similarly
46:8, 51:20
simple
34:9, 35:19, 36:18
simplest
22:24
simplifies
31:16
simply
27:7, 54:10
simpson
3:31, 7:14
since
51:21
single
23:25
sink
29:17, 31:20, 33:9
sir
10:18, 15:11
situation
33:2
size
22:2, 22:6,

22:7, 22:15, 22:20, 22:21, 23:6, 42:8
sizes
22:12, 22:13
skill
16:9, 17:12, 18:23, 19:23, 34:19, 36:22
slit
55:3
small
60:10
smaller
31:11, 34:12, 50:25
smallest
22:7
so-called
20:11, 20:23, 21:16, 24:21
solid
29:5
some
12:6, 21:7, 21:21, 21:24, 29:14, 32:18, 33:25, 51:8, 57:20
something
22:11, 28:23
sometimes
27:7, 29:14, 53:16
sorry
15:19, 17:24, 25:12, 38:25, 41:14, 43:15, 49:13, 49:16, 52:22, 56:18, 59:20, 60:9
sort
62:17
source
54:17
space
61:21
spacer
22:19
speaking
41:3
specific
50:20, 57:22
specifically
28:24, 61:10
specification
15:1, 16:11
speed
23:10, 23:12, 23:16, 23:20, 23:22, 23:24, 23:25, 24:8, 24:13, 24:16, 25:1, 27:13, 27:15, 27:16, 27:17, 27:19, 27:21, 27:22, 27:24, 28:2, 28:6, 28:9, 28:13, 28:14, 28:20, 29:10, 29:21
spot
32:9, 32:12, 32:23, 33:2, 33:4, 33:9, 33:11, 33:16, 33:20, 34:24, 35:7, 35:18, 36:3
spots
32:7, 32:19, 34:1, 34:2
stack
42:6, 53:16, 53:21, 55:20, 61:5, 61:12
stacked
53:15
stacks
42:6
staircase
54:21
stand
43:10, 43:17, 45:5, 45:7
standard
62:18
start
18:15, 45:10
started
27:25
state
2:23, 7:18, 8:9, 11:18, 19:16, 20:5, 20:17, 21:25, 24:10, 29:6, 63:4
statement
34:5
states
1:1, 2:1, 5:3, 6:5, 6:9, 7:7
stenographer
8:1, 62:15
stenographically
1:23
still
11:10
storage
19:21, 42:4, 42:13, 53:14
street
3:6
strike
35:25, 45:1
string
32:21, 55:4, 58:25
stringing
42:7
strings
32:5
structure
37:24, 39:24, 51:10, 51:19, 51:25, 52:2, 52:7, 52:19, 53:4, 53:5, 53:16, 53:18, 54:2, 54:21, 55:3, 55:4, 55:15, 55:20, 55:22, 56:10, 56:11, 56:12, 57:15, 58:22
structures
22:3, 22:13, 38:2, 40:16, 40:17, 54:11
studies
32:15
subparts
56:8
subsequent
38:11, 39:13, 39:19
substrate
38:6, 38:7, 38:10, 38:14, 39:2, 39:7, 39:12, 39:14, 39:18, 39:22, 39:25, 40:4, 40:5, 40:7, 40:9, 40:11, 40:13
substrates
38:21
suddenly
33:18, 33:23, 34:16, 34:17
supplied
6:13
sure
10:1, 14:11, 14:14, 14:15, 14:16, 15:19, 25:6, 26:24, 29:15, 29:18, 36:19, 37:6, 39:9, 40:10, 42:17, 43:11, 44:9, 52:3, 52:24, 53:23, 61:19
surface
21:1, 40:4, 40:9, 40:13, 40:14
surrounding
16:10, 31:19, 35:3, 36:25,

37:1
sutcliffe
3:3
sworn
7:25, 8:5, 63:7
system
29:13

T

table
13:10, 13:14, 51:6
take
12:17, 24:1, 24:4, 33:13, 37:6
taken
2:18, 37:10, 62:2, 63:9
taking
12:17
talk
24:23, 27:2, 28:9, 32:13, 33:5, 33:14, 34:7, 36:7, 43:12, 55:17
talking
27:13, 48:4, 48:7, 48:8, 48:17, 48:20
taught
30:2
teach
30:1
teaching
32:16
team
35:21
technique
19:21, 21:13
techniques
29:17
technologies
1:9, 2:10, 7:7
technology
1:3, 2:4, 7:6, 19:15, 20:5, 20:17, 21:10, 21:11, 21:25, 22:8, 23:11, 24:10, 48:4, 48:7, 48:20, 48:23, 49:10
tell
20:2, 43:6, 46:17, 47:25, 49:5, 50:1, 50:10, 50:17, 50:19, 50:22
temperature
28:19, 29:3, 29:9, 29:19, 29:22, 29:23, 30:5, 30:11, 30:19, 30:24, 31:5, 31:11, 31:17, 31:25, 32:1, 32:9, 33:8, 33:15, 36:14, 36:23
temperatures
30:17
term
16:8, 18:2, 42:1, 53:1, 53:6, 55:8
terminal
54:17
terminology
45:5, 58:20, 58:21
terms
9:20, 15:12, 15:16, 15:18, 15:23, 16:20, 17:3, 17:12, 17:18, 18:7, 18:25, 19:5, 22:24, 26:21, 26:25
test
50:13, 50:14
testified
8:5
testify
9:9
testimony
16:15, 63:10
texas
8:13, 30:3, 32:16
text
56:9
textbook
39:5, 39:6, 39:8, 39:22
thank
10:18, 11:21, 15:5, 15:11, 19:8, 23:7, 23:8, 33:17, 42:21, 47:24, 49:19, 62:6, 62:8
themselves
7:17, 46:19
thereabove
38:17, 39:16
therebelow
38:17, 39:17
thereby
32:6
therefore
21:18, 21:19, 23:3, 25:24, 26:1, 29:9, 32:11, 32:13, 34:23, 42:5, 42:6, 43:25, 47:14
therein
38:16, 39:15
thereupon
38:17, 39:16
thermal
35:20
thickness
30:21, 48:13, 48:17, 49:6, 50:2, 50:16
thicknesses
48:1
thin
33:19, 33:23
thing
20:19, 51:21, 59:6, 59:12
things
20:21, 30:18, 33:14, 34:14, 35:6, 36:3, 36:25
think
17:16, 22:11, 24:1, 27:4, 28:21, 29:3, 34:9, 36:6, 39:18, 40:24, 42:10, 42:12, 42:16, 43:7, 43:11, 45:4, 50:3, 50:4, 50:13, 55:7, 57:5, 59:11, 60:9, 60:24, 61:9, 61:22
thinking
18:3, 23:5
three
51:3, 51:6
three-dimensional
21:4, 53:15
through
9:19, 23:16, 24:7, 27:23, 28:12, 28:15, 30:8, 30:15, 31:4, 32:25, 36:11, 51:25
throughout
9:20
thursday
1:16, 2:20, 7:1
time
7:11, 7:12, 12:11, 12:12, 16:9, 17:13, 18:23, 24:14, 24:17, 24:25, 37:9, 37:13, 48:23, 50:20, 53:10, 53:19,

62:1, 62:5, 62:13
titled 14:18
today 7:13, 7:23, 8:25, 9:10, 9:20
today's 7:11, 12:1
told 50:12
took 12:15
top 37:23, 42:22, 42:25, 43:7, 44:15, 45:20, 45:23, 49:22, 54:17
topmost 59:17, 60:12
toshiba 53:2, 53:7, 57:17
toshiba's 57:24
total 27:8, 27:14, 28:5
towards 28:25
toyama 11:5, 11:13, 51:4, 51:19, 52:9, 52:25, 53:2, 53:11, 53:13, 53:20, 53:22, 54:23, 55:5, 55:17, 56:6, 56:7, 56:21, 58:6, 59:16, 59:25, 61:19
toyama's 51:7, 51:18, 52:1, 52:6, 52:13, 52:18, 53:4, 54:2, 55:15, 55:25, 56:2
trademark 1:1, 2:1, 7:8, 53:1, 53:6, 53:19, 55:8
trademarked 53:1
transcript 62:17, 62:18
transistor 58:10, 58:17, 58:18, 59:12, 59:13
transistors 58:24, 59:3
transmission 23:25, 27:17, 27:23, 28:3, 28:15
treatises 16:16
trial 1:2, 2:2, 7:8
trouble 49:15
true 13:16, 34:6, 51:15, 63:9
truthfully 9:10
try 9:6
trying 43:13
tuesday 12:15, 14:16, 14:23, 15:9
tungstens 49:9
turn 37:16, 41:10, 47:1, 47:9, 47:10, 58:12
turned 40:3
turning 13:21, 55:25, 56:21, 59:16
two 8:22, 20:10, 25:25, 26:5, 26:9, 26:10, 26:19, 27:3, 27:6, 36:9, 36:12, 36:20, 56:9
two-dimensional 20:23, 21:3
types 20:10, 20:11
typical 48:13, 48:17, 49:5
typically 47:25, 49:8, 54:19

U

ultra 53:14
under 8:25, 31:2
understand 8:25, 9:2, 9:13, 9:16, 10:8, 14:4, 16:4, 16:13, 19:24, 25:6, 34:19, 46:22, 57:10, 60:15
understood 31:21
uniform 34:7, 34:8
unit 23:1, 26:16, 26:21, 27:10, 30:22
united 1:1, 2:1, 5:3, 6:5, 6:9, 7:7
university 3:14, 30:3, 32:16
unless 39:9, 50:15
unlike 42:5
unlikely 30:24
until 37:10, 62:2
unwanted 25:3
upload 9:23, 10:15, 10:17, 11:1, 11:2, 14:13, 50:1
uploaded 12:3
uploading 11:7, 11:10, 14:17
upper 40:20, 59:3, 59:6, 59:8, 59:9, 59:13, 59:14, 59:17, 60:5, 60:13
uppermost 60:5
use 15:13, 15:17, 22:18, 32:21, 35:14, 35:15, 45:4, 55:3, 57:17, 58:6
using 9:20, 17:20, 29:17, 53:15

V

value 25:10, 27:6, 27:8
variety 55:1
various 19:17, 19:20, 20:7, 29:6, 33:4, 33:12, 34:14
versus 7:6, 18:12,

18:16, 19:1
vertical
21:5, 55:21
vertically
42:6
via
1:15, 2:20, 7:1, 12:13, 63:14
video
7:12, 7:15
videoconference
1:15, 2:21, 7:1, 63:14
videographer
3:31, 7:4, 7:13, 7:23, 37:8, 37:12, 61:25, 62:4, 62:11
videotaped
1:14, 2:18, 7:4
view
16:10, 18:21
viewed
17:13, 52:12
voice-identify
7:17
voltage
25:20, 35:13, 47:10, 54:18
vs
1:7, 2:8

W

wait
9:5, 9:6, 60:15
waiting
41:15
want
14:16, 28:24, 46:23, 47:3, 47:5, 47:8, 47:12, 47:22
way
25:11
ways
21:2, 54:23
we'll
9:20
we're
29:5
we've
37:2
week
12:15
weeks
12:12
weight
16:18
west
3:6
western
53:7, 53:9, 55:11
westslope
8:13
whatnot
47:23
whereas
20:14
whereof
63:18
whereupon
14:20
whether
17:17, 25:22, 34:10, 38:25, 39:2, 46:9, 47:5, 52:24, 53:9, 53:11, 53:19, 55:6, 55:9
wide
33:25
width
30:21
wire
24:3, 28:15, 30:23, 33:7, 34:7, 34:17, 36:10, 36:11, 36:12, 36:14, 36:20
wires
36:9
within
22:13, 24:19, 32:6, 40:12, 43:24, 63:4
without
42:7, 50:9
witness
4:2, 7:24, 8:4, 14:22, 17:5, 18:10, 22:5, 26:24, 28:8, 30:1, 33:22, 34:4, 35:10, 36:6, 37:6, 40:20, 43:9, 45:23, 48:3, 48:20, 50:9, 52:22, 54:7, 56:5, 56:24, 57:10, 58:2, 59:20, 60:15, 60:22, 61:19, 61:24, 62:8, 63:6, 63:10, 63:18
word
34:11, 40:2, 45:2, 45:16, 46:10, 46:11, 46:15, 46:25, 47:7, 47:9, 47:20, 49:6, 54:19, 54:20, 61:21
words
16:6, 26:11, 47:17
work
11:22
working
35:11
works
46:23
wouldn't
50:5
write
50:15
written
15:3, 50:15
wrong
45:4

X

xy-plane
20:24, 45:18

Y

yangtze
1:9, 2:10, 7:6
yeah
8:22, 10:14, 11:1, 28:11, 36:19, 38:18, 40:24, 41:9, 41:13, 43:2, 43:15, 44:7, 44:9, 44:16, 45:7, 46:5, 46:15, 51:21, 54:14, 55:17, 55:22, 57:4, 57:20, 59:3, 59:10, 59:14, 60:1, 60:4, 61:19
year
48:8, 49:13, 50:20
years
21:14, 30:3
yellow
37:24, 38:2, 39:1, 40:15, 40:17, 41:1, 41:6
ymtc
7:20, 11:23
york
3:7

Z

zoom
12:13

$

$680
11:20

0

000911
7:10
00791
1:8, 2:9, 7:9, 9:21
00911
10:12
0179026
6:10, 11:4
026
53:2, 53:22
04
1:17, 2:19, 7:2, 63:15
047,182
13:25
05
7:12
07
62:3, 62:5, 62:13

1

1
47:14
10
38:14, 62:1, 62:2
10,658,378
5:4, 14:1, 14:10, 14:18
10,937,806
1:10, 2:11, 6:6, 10:22
100
50:7
1001
6:5, 13:12
10019
3:7
1002
13:13
1003
6:8, 9:22, 10:13
1005
6:9
1014
49:24
103
56:24, 57:3
104
51:20
11
52:14, 62:3, 62:5, 62:13, 62:19, 63:15
12
52:14
132
61:11
13916
1:25, 2:22, 8:2, 63:4, 63:23
14
5:3
146
61:8
15
62:19, 63:15
16
13:25
163
55:17
17
37:16, 37:18, 38:24, 38:25, 51:25, 56:15
18
43:16, 45:7
19
5:5
1900
3:14

2

20
49:11, 49:18, 50:11
2000
49:3
2016
49:3, 49:17
2017
6:10, 6:11, 11:4
2018
14:1
2020
5:5
2021
6:7
2024
1:8, 2:9, 7:9, 7:10, 9:21, 10:12
2025
1:16, 2:20, 7:1, 7:11, 63:15, 63:19
21
41:10, 41:11, 44:3
212
3:8
22
6:11, 37:9, 37:10
232
61:11, 61:16
242
60:24
246
61:8
26
32:3, 32:4
27
14:1
270
59:18, 60:6, 60:11, 60:15

3

30
1:16, 2:20, 7:1, 7:11, 63:14
34
37:11, 37:13
35
30:3
378
12:15, 14:22, 14:25, 15:7, 15:13, 15:17, 15:24, 16:25, 17:19, 18:13, 18:17, 19:1
38
18:17
3d
19:20, 39:5, 41:16, 41:20, 50:22, 53:15, 53:18, 53:21, 54:15, 55:6, 55:12, 57:18, 57:19, 58:2

4

43
59:24, 60:2
44
37:20
45
60:25, 61:1
47
38:10
4794
3:17
48
58:12, 58:14, 59:10
49
38:19, 56:19, 56:21, 57:16, 57:23, 59:16, 59:23, 59:24, 59:25, 60:6, 60:13

5

5000
3:8
506
3:8
51
3:6
52
3:6, 55:1
57
62:1, 62:2

5803
8:13

6

60
56:9
617
3:17
63
13:24
650
3:17
6th
3:15, 63:18

7

70
56:8
72
16:2, 19:7
74
16:2
75
19:7
78731
8:13

8

8
1:17, 2:19,
7:2, 7:12, 63:15
806
10:23, 10:25,
12:16, 13:12,
13:21, 14:25,
15:13, 15:17,
15:25, 17:1,
17:19, 18:11,
18:12, 18:16,
19:1, 20:6,
38:9, 38:13,
38:14, 39:11,
52:15
81
56:14
85
51:17, 52:11

9

9
37:9, 37:10,
37:11, 37:13
92
59:25
94303
3:16