

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner
v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,
Patent Owner

Case No.: IPR2024-00791
U.S. Patent No. 10,937,806

PETITIONER'S REPLY

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1001	U.S. Patent No. 10,937,806 B2 to Tao et al.
1002	File History of U.S. Patent No. 10,937,806 B2 to Tao et al.
1003	Declaration of Jack C. Lee
1004	<i>Curriculum Vitae</i> of Dr. Jack C. Lee
1005	U.S. Patent Publ. No. 2017/0179026 A1 to Toyama et al. (“Toyama”).
1006	Minute Order, Dkt. No. 42, dated February 22, 2024 in <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC</i> , Case No. 3:23-cv-05792-RFL
1007	Combined Civil and Criminal Federal Court Management Statistics (December 31, 2023), available at https://www.uscourts.gov/sites/default/files/data_tables/fcms_na_distcomparison1231.2023.pdf
1008	Docket from <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC</i> , Case No. 3:23-cv-05792-RFL
1009	CN109075169A Office Action, dated November 14, 2019
1010	Certified Translation of CN109075169A Office Action, dated November 14, 2019
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1012	Certified Translation of CN109075169A Reexamination Decision, dated November 25, 2021
1013	Micheloni, “3D Flash Memories” (2016)

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1014	Aritome, “NAND Flash Memory Technologies” (2016)
1015	U.S. Patent Publ. No. 2018/0108671 A1 to Yu et al.
1016	U.S. Patent Publ. No. 2019/0229125 A1 to Zhou et al.
1017	U.S. Patent No. 10,354,980 B1 to Mushiga et al.
1018	U.S. Patent No. 9,293,348 B2 to Lai et al.
1019	U.S. Patent No. 8,598,643 B2 to Kawasaki et al.
1020	U.S. Patent No. 8,697,519 B2 to Jee et al.
1021	Excerpts from “Merriam-Webster’s Collegiate Dictionary,” Eleventh Edition (2014)
1022	Print out of https://www.studycountry.com/wiki/what-is-a-piece-of-land-surrounded-by-water-on-2-sides
1023	Michelson et al., “Inside Solid State Drives (SSDs)” (1 st Ed. 2013)
1024	U.S. Patent No. 10,043,558 to Shah et al.
1025	Michelson et al., “Inside NAND Flash Memories” (2010)
1026	Lau, “Ball Grid Array Technology” (1995)
1027	U.S. Patent No. 10,103,169 to Ge et al.
1028	U.S. Patent No. 9,935,050 to Dunga et al.
1029	<i>Intentionally Omitted</i>
1030	<i>Intentionally Omitted</i>
1031	<i>Intentionally Omitted</i>
1032	<i>Intentionally Omitted</i>

Exhibit	Description
1033	<i>Intentionally Omitted</i>
1034	<i>Intentionally Omitted</i>
1035	<i>Intentionally Omitted</i>
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1037	<i>Intentionally Omitted</i>
1038	Complaint for Patent Infringement, Dkt. No. 1, filed Nov. 9, 2023, in <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC</i> , Case No. 3:23-cv-05792-RFL
1039	First Amended Complaint for Patent Infringement, Dkt. No. 29, filed Feb. 2, 2024, in <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC</i> , Case No. 3:23-cv-05792-RFL
1040	Plaintiff and Counterclaim Defendant Yangtze Memory Technologies Company, Ltd.’s Disclosure of Asserted Claims and Infringement Contentions, dated May 6, 2024, in <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC</i> , Case No. 3:23-cv-05792-RFL
1041	Declaration of Jared Bobrow in Support of Petitioner’s Motion for Admission <i>Pro Hac Vice</i>
1042	<i>Intentionally Omitted</i>
1043	Reply Declaration of Dr. Jack C. Lee (“Lee-Reply”)
1044	Transcript of the Deposition of Woodward Yang, dated April 22, 2025, in <i>Micron Technology, Inc. v. Yangtze Memory Technologies Company, Ltd.</i> , Case Nos. IPR2024-00788, -00909

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1045	Woodward Yang, Deposition Exhibit 4, in <i>Micron Technology, Inc. v. Yangtze Memory Technologies Company, Ltd.</i> , Case Nos. IPR2024-00788, -00909
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1047	Transcript of the Deposition of Woodward Yang, dated April 24, 2025, in Case Nos. IPR2024-00791, -00911
1048	Woodward Yang, Deposition Exhibit 2, in Case Nos. IPR2024-00791, -00911
1049	Micheloni et al., “Inside Solid State Drives (SSDs)” (2 nd Ed. 2018)
1050	PCT Publication No. WO 2009/079014 A1 to Yang et al.
1051	Additional excerpt from “Merriam-Webster’s Collegiate Dictionary,” Eleventh Edition (2014)
1052	Print out of https://gf.com/about-us/gf-in-the-community/stem-at-gf/glossary-of-terms/

LISTING OF CHALLENGED CLAIMS

Ref. #	Listing of Challenged Claims
Claim 8:	
[8.PRE]	A three-dimensional (3D) memory device, comprising:
[8.A]	an alternating conductor/dielectric layer stack;
[8.B]	a dielectric structure extending vertically through the alternating conductor/dielectric layer stack;
[8.C]	first and second channel regions comprising first and second pluralities of channel structures, respectively;
[8.D]	slit structures extending vertically through the alternating conductor/dielectric layer stack;
[8.E]	a staircase structure disposed in the alternating conductor/dielectric layer stack, wherein the staircase structure comprises levels with each level having a conductor layer thereon;
[8.F]	local contacts disposed on the first and second channel structures and the slit structures;
[8.G]	a through array contact (TAC) region formed between the first and second channel regions, wherein the TAC region comprises a plurality of through array contacts (TACs) extending vertically through the dielectric structure; and
[8.H]	a plurality of non-electrically functional channel structures surrounding the TAC region and between the first and second channel regions.
Claim 9:	
[9]	The 3D memory device of claim 8, wherein the dielectric structure abuts a sidewall of each TAC of the TACs.

Ref. #	Listing of Challenged Claims
Claim 11:	
[11]	The 3D memory device of claim 8, wherein the dielectric material comprises silicon oxide.
Claim 12:	
[12]	The 3D memory device of claim 8, wherein the TACs comprise a conductive material.

I. INTRODUCTION

PO's Response fails to rebut the Petition's showing of unpatentability on any of the three raised grounds.

Ground 1. As to limitation [8.G], PO's single-dielectric-structure requirement relies on a construction contrary to the well-settled patent law principle that "a" ordinarily means "one or more," and that "the" refers back to the antecedent basis's numerosity (which, here, is "one or more"). PO also fails to recognize that multiple noncontiguous elements with a shared purpose (here, "insulating liners 674") can combine to form a single structure. As to limitation [8.H], PO's assertion that Toyama fails to teach non-electrically functional channel structures "surrounding" the TAC region ignores Toyama's express teachings that these structures are around the "periphery" of that region, and PO entirely fails to respond to Petitioner's obviousness theory for this limitation.

Ground 2. Although PO purports to contest limitation [8.G], PO does not dispute that the modification proposed in Ground 2 includes that limitation. PO's argument that an apparatus with two planes is not a "device" is contrary to the plain meaning of that term, and PO has not shown any basis for the preamble phrase "[a] three-dimensional (3D) memory device" to exclude multiplane memories. PO's argument that Toyama's peripheral circuitry would prevent a POSITA from making the proposed combination functional is not credible in view

of the commonplace use of planes in flash memory devices, which had peripheral circuitry, before the '806 patent.

Ground 3. PO's assertion that the proposed combination is unmanufacturable because it would require gate replacement through slit structures is not credible in view of the long-standing use of slit structures for gate replacement. PO's assertion that the proposed combination's dielectric block would render it inoperable is contradicted by the '806 patent (which shares the same basic structure) and Toyama (which expressly discloses embodiments that place a dielectric block in the same place as in the proposed combination). PO's motivation to combine arguments fall flat because PO does not and cannot dispute that the proposed combination's unitary dielectric fill has the desirable and predictable property of insulating the TACs within it, which is sufficient motivation. Although PO demands that Petitioner prove that the proposed combination is superior to the expressly disclosed embodiments on which it is based, the law requires no such showing.

II. CLAIM CONSTRUCTION

A. “a dielectric structure” and “a plurality of through array contacts (TACs) extending vertically through the dielectric structure”

The parties' dispute centers on whether the device's “through array contacts” may extend vertically through multiple dielectric structures (as Petitioner

contends, Lee-Reply ¶¶10-15) or whether the claim requires that multiple “through array contacts” extend through a “single dielectric structure” (as PO contends). POR 20-21.

PO’s position runs afoul of the “general rule of claim construction” that “a” means “one or more.” *KCJ Corp. v. Kinetic Concepts, Inc.*, 223 F.3d 1351, 1357 (Fed. Cir. 2000). Although a departure from the rule requires that “the patentee evinces a clear intent to so limit the article,” PO does not even attempt to surmount this high bar. *Id.* at 1356.

The specification expressly provides that “terms, such as ‘a,’ ‘an,’ or ‘the,’ ... may be understood to convey a singular usage or to convey a plural usage, depending at least in part upon context.” ’806, 4:17-25. The context of the ’806 supports a plural-allowing usage; the ’806 does not mandate a unitary block with multiple TACs, and on the contrary contemplates embodiments with multiple dielectric structures (each of which includes a single TAC). Lee-Reply ¶¶12-15; ’806, 21:11-28. Thus, the specification’s definition “reinforces ... the applicability here of the ‘one or more’ general rule concerning ‘a’ or ‘an.’” *ABS Glob., Inc. v. Cytonome/St, LLC*, 84 F.4th 1034, 1040-41 (Fed. Cir. 2023). “It also brings into play the lexicography principle—that, with narrow exceptions, ‘[w]here the specification instructs as to the meaning of a claim term, the inventor’s lexicography governs.’” *Id.*

PO's attempt to distinguish *KCJ* misses the mark. PO acknowledges that the claimed device may include multiple dielectric structures. POR 20-21. PO asserts, however, that the limitation "through array contacts ... extending vertically through **the** dielectric ... structure[]" means that multiple TACs must extend through a single dielectric structure. *Id.* (emphasis added). But "because the initial indefinite article ('a') carries either a single or plural meaning, any later reference to that same claim element merely reflects the same potential plurality." *Baldwin Graphic Sys., Inc. v. Siebert, Inc.*, 512 F.3d 1338, 1343 (Fed. Cir. 2008). In other words, "the reference-back 'the' takes its meaning from the meaning of the antecedent, so if ['a dielectric structure'] has a plural-allowing meaning, so does the reference-back ['the dielectric structure'] phrase." *ABS Glob.*, 84 F.4th at 1040.

The Federal Circuit's decision in *Baldwin* illustrates why PO's singular-mandating interpretation of "the dielectric ... structures" is flawed. In *Baldwin*, the claim at issue recited "a pre-soaked fabric roll ..., said fabric roll having a sealed sleeve." 512 F.3d at 1340. The district court held that "the use of 'said fabric roll' implies that the prior reference to 'a fabric roll' should be read as a single roll," and therefore held that an accused product with multiple fabric rolls having one, shared sealed sleeve did not infringe the asserted patent. *Id.* at 1343. The Federal Circuit reversed, explaining that "[i]n grammatical terms, the instances of 'said fabric roll' in the claim are anaphoric phrases, referring to the

initial antecedent phrase. Because the initial phrase”—that is, “a fabric roll”—“carries no definitive numerosity, the anaphoric phrases do not alter that meaning in the slightest.” *Id.* Thus, just as the district court in *Baldwin* erred by holding that “said fabric roll” required a single fabric roll, PO errs by arguing that “the dielectric and the isolation structures” requires a single dielectric structure.

PO’s reliance on *Finjan* misses the mark. *Finjan* involved a claim that recited method steps including, for example, “receiving, by a computer,” “determining, by the computer,” and “identifying, by the computer.” *Finjan LLC v. SonicWall, Inc.*, 84 F.4th 963, 966-67 (Fed. Cir. 2023). The Court held that the claim was not infringed when in the accused system some of the recited method steps were performed by one computer, and other method steps were performed by a “separate, remote computer[.]” *Id.* at 974. But *Finjan* did not involve a situation, as here, where the specification expressly states that the word “a” may be used “to convey a plural usage.” ’806, 4:17-25. Nor did *Finjan* involve a situation, analogous to here, where multiple computers each perform each “subsequent claim limitation[.]” *Finjan*, 84 F.4th at 975. Here, unlike in *Finjan*, the claim is met so long as “**at least one** ... [dielectric structure] perform[s] all [of] the [claimed] functions.” *Id.* (emphasis added).

There is nothing inconsistent between *Finjan*’s holding and Petitioner’s construction. Applied here, *Finjan* merely stands for the proposition that the

“**same** ‘one or more’” dielectric structures must satisfy all of the limitations reciting “the dielectric structure.” *Id.* at 974 (emphasis added). Petitioner’s Grounds meet that requirement. §III.A.

III. GROUND 1: TOYAMA’S SECOND MODIFICATION RENDERS THE CHALLENGED CLAIMS OBVIOUS

PO does not dispute that Toyama’s Second Modification’s discloses or renders obvious each limitation of every Challenged Claim except limitations [8.G] and [8.H]. PO’s attempts to distinguish the Second Modification from those limitations must fail.

A. [8.G]: “a through array contact (TAC) region formed between the first and second channel regions, wherein the TAC region comprises a plurality of through array contacts (TACs) extending vertically through the dielectric structure”

1. PO Does Not Dispute That under Petitioner’s Construction, Toyama Renders Limitation [8.G] Obvious

PO’s only dispute regarding this limitation is premised on its construction that would require multiple *through array contacts* to extend through a “singular” *dielectric structure*. POR 21. But, for the reasons explained in this Reply’s claim construction section, PO’s construction is improperly narrow. §II.A . PO does not dispute that if limitation [8.G] permits the *through array contacts* to extend through multiple *dielectric structures* (as the limitation should be interpreted), then Toyama’s Second Modification teaches limitation [8.G]. Pet. 45-51.

PO's analogy to *Finjan* falls flat because PO does not dispute that the same "insulating liners 674" satisfy every requirement of the claimed *dielectric structure*. In *Finjan*, the claim at issue recited a first "receiving" step performed "by a computer," and then a number of successive steps (e.g., "determining," and "instantiating,") performed "by the computer." *Finjan*, 84 F.4th at 966-67. The Court held that the claim required the "same 'one *or more* computers'" "perform each of several subsequent claim limitations." *Id.* at 974-75 (emphasis added). But, here, PO does not dispute that the same one *or more dielectric structures* ("insulating liners 674") satisfy all claim limitations. The same "insulating liners 674" that the *extend[] vertically through* also *extend[] vertically through the alternating conductor/dielectric layer stack* ([8.B], Pet. 30-33). Here, unlike in *Finjan*, the *same* "insulating liners 674" are "tied to all [of the (five) claimed] functions." *Finjan*, 84 F.4th at 974.

2. [8.G] Would Have Been Obvious Even under PO's Erroneous Construction

Toyama's Second Modification renders limitation [15.H] obvious even accepting PO's construction that erroneously requires multiple *through array contacts* to extend through a "single" *dielectric structure* because the combination

of Toyama’s “insulating liners 674” are collectively a single *dielectric structure*.¹
POR 19; Pet. 32-33; Lee-Reply ¶17-19.

As an initial matter, the term “structure” does not require all elements of the structure to be contiguous. Merriam-Webster’s defines a structure, for example, as “something arranged in a definite pattern of organization.” Ex. 1021, 4.² Thus, as PO’s expert agreed, the below wall is a structure even though its components are not all touching each other:

¹ Petitioner’s position here is consistent with its position that each of the “insulating liners 674” is individually a structure because “a structure ... can be composed of other structures.” Ex. 1044, 43:25-44:2; Lee-Reply ¶17 n.1.

² Although the Petition (at 31-32) focused on a different of Merriam-Webster’s definitions (“something (as a building) that is constructed”), Petitioner recognizes that this definition may not be sufficient to resolve the parties’ dispute.



Ex. 1045 (4/22/25 Yang Dep., Ex. 4); Ex. 1044, 45:3-4, 47:3-6 (identifying the “wooden posts” as a “wall structure”); Lee-Reply ¶18. Similarly, the staircase below is a structure even though the stairs do not contact each other:



Ex. 1046 (4/22/25 Yang Dep., Ex. 5); Lee-Reply ¶18.

As the Petition explained, the “insulating liners 674” of Toyama’s Second Modification are individually ***and collectively*** a dielectric structure:

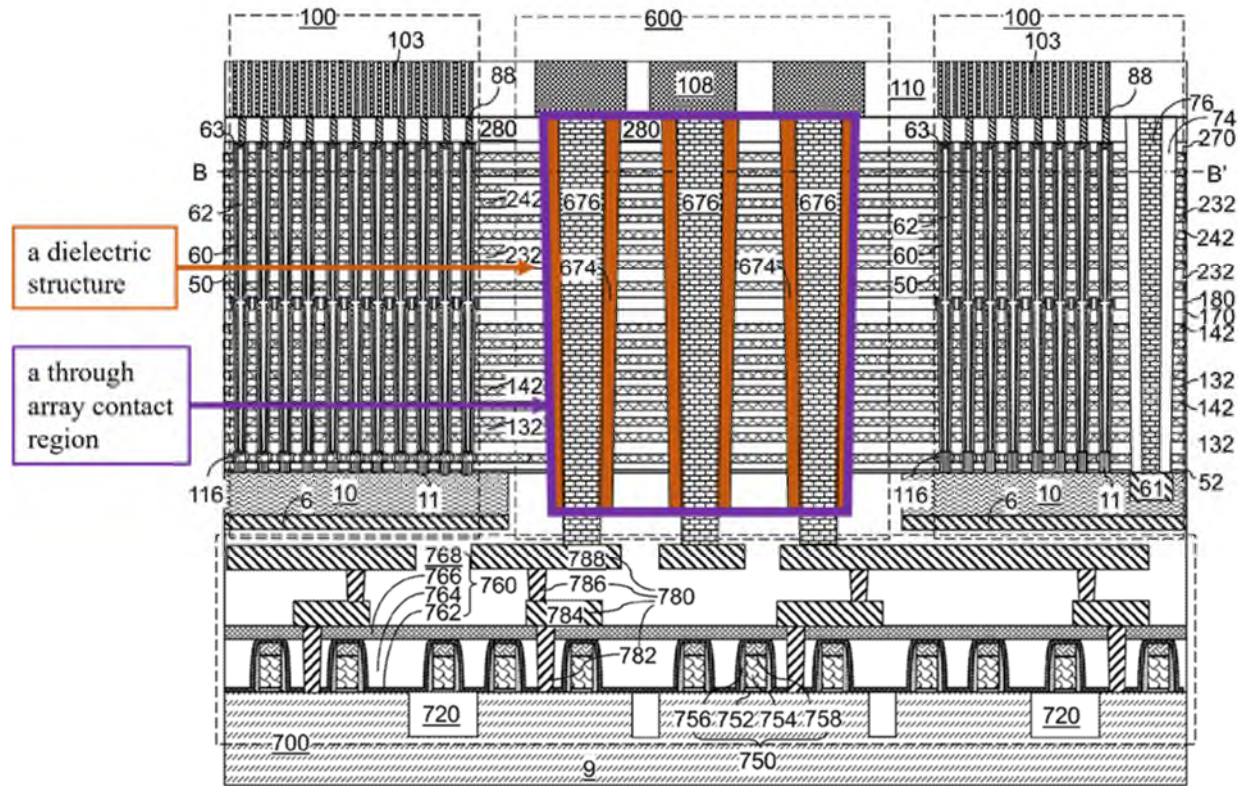


FIG. 49

Toyama, Figures 49 (annotated); Pet. 45-51; Lee-Reply ¶19. Like the wall posts and stairs above, each of “insulating liners 674” are arranged in a definite pattern of organization. Indeed, PO does not dispute that the liners all have the same function: insulating the *TACs* as they pass through the *alternating ... layer stack*.

Lee-Reply ¶19.

B. [8.H]: “a plurality of non-electrically functional channel structures surrounding the TAC region and between the first and second channel regions”

PO’s only argument with respect to this limitation is that Toyama’s “dummy memory stack structures 55D” are not *surrounding* the indicated part of “through-

memory-level region 600.” POR 22-25. PO’s argument must fail for three independently sufficient reasons.

1. PO’s Argument Relies on a Construction of “Surrounding” Contrary to Its Plain Meaning

PO’s assertion that Figure 48B fails to teach limitation [8.H] cannot be squared with the plain meaning of “surrounding.” PO asserts that because Figure 48B only shows *non-electrically functional channel structures* on two sides of the *TAC region*, the structures are not *surrounding* the TAC region. POR 24. But the PO ignores the Petition’s intrinsic and extrinsic evidence showing that a first feature may surround another on just two sides. Pet. 51-52 n.9; Lee ¶119; Lee-Reply ¶¶21-22.

2. PO Ignores Toyama’s Disclosure That Its Non-Electrically Functional Channel Structures Are “Provided at the Periphery” of Its TAC Region

As the Petition explained, yet PO ignores, a POSITA would have understood Toyama’s statement that “[d]ummy memory stack structures 55D can be provided at the periphery of the through-memory-level via region 600” to disclose placing these *non-electrically functional channel structures* on four sides of the *TAC region*. Pet. 54; Lee ¶120. Indeed, both parties’ experts agree that the periphery of a rectangle (like the *TAC region* here) is “the four sides of the rectangle.” Ex. 1047, 24:7-10; Lee-Reply ¶23.

3. PO Ignores the Petition’s Alternative Obviousness Argument

PO fails to respond to the Petition’s point that a POSITA would have found this limitation an obvious “predictable use of prior art elements ... according to their established functions.” Pet. 54-55; Lee ¶121; Lee-Reply ¶24.

IV. GROUND 2: TOYAMA’S FIRST EXEMPLARY STRUCTURE RENDERS THE CHALLENGED CLAIMS OBVIOUS

A. [8.G]

Although PO purports to challenge limitation [8.G], PO does not dispute that the proposed modification, if successfully implemented, renders limitation [8.G] obvious. Nor does PO dispute that a POSITA would have been motivated to implement multiple planes of Toyama’s first exemplary structure at least because of the well-recognized performance benefits from doing so.³ PO’s two arguments, neither of which relate to limitation [8.G], have no merit.

³ PO improperly conflates its argument regarding the purported inoperability of the proposed modification (which is, in essence, a reasonable expectation of success argument) with motivation to combine. POR 36.

1. PO's Argument That an Apparatus with Two Planes Is Not "a Device" Is Meritless.

a. A flash memory device with two planes is still a "device."

The preamble of claim 8 recites "[a] three-dimensional (3D) memory device, comprising" a number of recited elements. Petitioner's proposed modification is "to implement Toyama's first exemplary structure in *a 3D memory device* with multiple planes." Pet. 69-70 (emphasis added). PO's assertion that the implemented modification is not a single "device" is incorrect. POR 25-29; Lee-Reply ¶¶28-41.

The '806 patent's definition of "3D memory device," which PO ignores, is "a semiconductor device with vertically-oriented strings of memory cell transistors (referred to herein as 'memory strings,' such as NAND strings) on a laterally-oriented substrate so that the memory strings extend in the vertical direction with respect to the substrate." '806, 5:30-37.

The proposed modification meets this definition. Indeed, PO does not dispute (nor can it) that Toyama discloses channel structures (i.e., memory strings), or that they are vertically oriented with respect to a semiconductor substrate. Pet. 65-67; Lee-Reply ¶¶30-31. Nothing about the use of two planes takes the proposed modification outside of the '806 patent's definition; it continues to include vertically oriented memory strings on a laterally oriented substrate. Lee-

Reply ¶32. Indeed, the specification elsewhere reinforces that two planes can be a single device; it contemplates that one “device” can be part of another “device,” and that a device can include multiple substrates.⁴ ’806, 7:53-57 (“3D memory device” includes an “array device” and a “peripheral device,” and a device may comprise multiple substrates); Lee-Reply ¶33.

The specification is thus consistent with the ordinary meaning of “device” to a POSITA, which includes a NAND flash memory with two planes. Lee-Reply ¶¶34-38; Ex. 1023, 247 (device comprises multiple planes); Ex. 1049, 357 (same); Ex. 1014, 313 (“3D V-NAND flash memory device” comprises “two planes”); Ex. 1050, Figure 5 (PO’s expert’s patent showing two planes per device); Ex. 1047 (acknowledging that a solid-state drive is a device), 11:24-12:10; Lee-Reply ¶38 (a solid-state drive is a device that can include multiple planes).

PO’s assertion that forming a TAC region “between the first and second channel regions ... provides the benefit that [the] TACs are closer to [the] memory device components, and interconnect routing may be shortened” is beside the point. POR 28-29. But the passage of the specification on which PO relies does

⁴ Even if the proposed modification uses a different substrate (it would not), that would not cause the proposed modification to be multiple devices. Lee-Reply ¶34 n.3.

not limit that purported benefit to placing a TAC region between channel structures. Lee-Reply ¶¶39-41 (discussing '806, 11:8-14). Indeed, the patent includes embodiments in which the TACs are **not** between channel regions. *E.g.*, '806, Figure 1C. PO has not identified claim language, disclaimer, or lexicography that would justify requiring the word “device” to be narrowed to a single-plane device.

b. The Claim Is Not Limited to a Single “3D Memory Device”

Even if the Board were to find that the word “device” excludes multi-plane devices, the combination still renders claim 8 obvious because it is not limited to a single “device” for two independently sufficient reasons.

First, PO has not even attempted to show that the preamble here is limiting. “[A] preamble is not limiting ‘where a patentee defines a structurally complete invention in the claim body and uses the preamble only to state a purpose or intended use for the invention.’” *Catalina Mktg. Int’l, Inc. v. Coolsavings.com, Inc.*, 289 F.3d 801, 808 (Fed. Cir. 2002). Here, claim 8 recites a structurally complete invention and the preamble’s phrase “a three-dimensional (3D) memory device) merely “gives a descriptive name to the set of limitations in the body of the claim.” *IMS Tech., Inc. v. Haas Automation, Inc.*, 206 F.3d 1422, 1434 (Fed. Cir. 2000); Lee-Reply ¶43.

Second, PO has not shown that “a” here must be limited to the singular. As has been discussed at length in this Reply, the word “a” means “one or more” absent a clear intent to the contrary. *KCJ*, 223 F.3d at 1356. Yet there is no lexicography, disclaimer, or anything about the structure or purpose of the claim that would limit it to a single device. Lee-Reply ¶44.

2. PO’s Argument That a POSITA Would Not Have Been Able to Make the Proposed Combination Functional Is Not Credible.

PO’s argument that a POSITA would not have been motivated to make the proposed combination because Figure 17F’s peripheral circuitry would interfere with another plane is not credible. POR 28-29.

As an initial matter, Toyama’s first exemplary structure does not require the layout of Figure 17F. Indeed, whereas Toyama describes Figures 17A-D as related to its “first exemplary structure,” it describes Figure 17F as “of an **alternative** exemplary structure.” Toyama, [0045]-[0049] (emphasis added). Even assuming that Figure 17F layout were required to, Toyama merely provides that “upper level metal interconnect structures 208 **may be** electrically coupled to the driver circuits devices at a location other than region 400.” Toyama, [0251]. A POSITA would have understood that just because structures 208 were not in region 400, does not mean that such structures would necessarily conflict with structures of other planes. Lee-Reply ¶59.

Indeed, the longstanding use of planes in flash memory devices (which had peripheral circuitry) before the '806 patent confirms that the placement of peripheral circuitry was well within a POSITA's skill. Pet. 70-76; Lee-Reply ¶¶45-60. Indeed, the Petition cited some *four* prior art multi-plane memory devices. Pet. 70-76. Each of those prior art multi-plane disclosures includes the location of the device's peripheral circuitry. Lee-Reply ¶¶48-52 (citing Ex. 1023, 144; Ex. 1014, 308, 313-314; Ex. 1024, 13:45-46). For example, prior art discloses placing peripheral circuitry above and below, below, or underneath the memory array. *Id.*

Even aside from the disclosures that specifically discuss peripheral circuitry, the fact that numerous (functional) flash memory devices by 2018 included multiple planes further supports that placing peripheral circuitry in a multi-plane device was within the skill of a POSITA. Lee-Reply ¶¶53-57. That is because, as a POSITA would have understood, any flash memory device needs peripheral circuitry. Lee-Reply ¶54 (citing Ex. 1013, 82). These prior art disclosures demonstrate that it would have been within the skill of a POSITA to place peripheral circuitry in a multi-plane device. Lee-Reply ¶¶55-56.

PO's objection to the proposed modification is in essence the sort of "bodily incorporation" argument that courts have repeatedly rejected. PO argues that a POSITA would not have been able to make the proposed combination because

Toyama's Figure 17F shows peripheral circuitry on both sides of each plane and, therefore, that a POSITA would not have been able to implement multiple planes. POR 29-30. But, as discussed above, Toyama is not limited to that layout. Lee-Reply ¶59. Even if it were, whether Toyama's exact physical layout could be used for a multi-plane device is "basically irrelevant." *In re Etter*, 756 F.2d 852, 859 (Fed. Cir. 1985) (en banc) (rejecting bodily incorporation argument). It has long been settled that "[c]laims may be obvious in view of a combination of references, even if the features of one reference cannot be substituted physically into the structure of the other reference." *Orthopedic Equip. Co. v. United States*, 702 F.2d 1005, 1013 (Fed. Cir. 1983); *Elbrus Int'l Ltd. v. Samsung Elecs. Co.*, 738 F. App'x 694, 698 (Fed. Cir. 2018) (rejecting argument that a proposed combination "would lead to an inoperable circuit" as improperly requiring bodily incorporation to show obviousness); *Pulse Elecs., Inc. v. U.D. Elec. Corp.*, 860 F. App'x 735, 739 (Fed. Cir. 2021) (same); *In re Mouttet*, 686 F.3d 1322, 1332 (Fed. Cir. 2012) (same).

Here, the record evidence—including the numerous prior art 3D NAND flash memory devices that have implemented multiple planes, the specific prior art disclosures of the locations of peripheral circuitry in multi-plane flash memory devices, and PO's failure to rebut any of the Petition's evidence discussing peripheral circuitry—compels the conclusion that a POSITA would have been

motivated to implement multiple planes of Toyama's first exemplary structure in a functional device with a reasonable expectation of success. Lee-Reply ¶60.

In sum, the trial record only further bolsters the Institution Decision's holding that "a POSITA would have had a reasonable expectation of success in implementing multiple planes of Toyama's First Exemplary Structure in the hd1 direction because NAND devices having multiple planes existed for many years before the priority date of the '806 patent and that implementation of such a structure would have been straightforward as it merely applies a known technique (implementing multiple planes of [a] NAND flash memory array) to a known device (Toyama's first exemplary structure) to yield predictable results (a NAND flash device with improved performance)." ID 28-29.

V. GROUND 3: TOYAMA’S FIRST EXEMPLARY STRUCTURE AND SECOND MODIFICATION RENDER THE CHALLENGED CLAIMS OBVIOUS

A. A POSITA Would Have Been Motivated To Combine Toyama’s First Exemplary Structure and Its Second Modification

1. A POSITA Would Have Known How to Use Slit Structures (Toyama’s “Laterally Elongated Contact Via Structures 76”) to Perform Gate Replacement In the Proposed Combination

The intrinsic and extrinsic record contradicts PO’s assertion that the proposed combination would remove access for depositing conductive material during the gate replacement process. POR 38-41; Lee-Reply ¶¶61-67.

First, PO does not dispute that the proposed combination may continue to use the openings that ultimately become the combination’s slit structures—“backside contact trenches 79”—to allow access for gate replacement. Indeed, Toyama discloses in the context of its Second Modification that “[r]eactants can be introduced through the backside contact trenches 79 and the through-memory-level openings 679 to deposit the electrically conductive layers (146, 246).” Toyama, [0337]. Even if “openings 679” were no longer created, a POSITA would have recognized that gate replacement be performed through “trenches 79.” Lee-Reply ¶¶61-64.

Second, Toyama itself demonstrates that gate replacement may be performed solely using “trenches 79.” Indeed, Toyama’s first exemplary structure (which is the other embodiment on which the combination is based) uses “backside contact trenches 79” (and no other openings) to form its “electrically conductive layers (146, 246).” Lee-Reply ¶64; Toyama, Figures 12-13, [0217], [0221]-[0224], [0231]-[0232].

Third, the use of slit structure openings as the access points for gate replacement was a conventional, textbook approach. *See, e.g.*, Ex. 1013, 131-132; Ex. 1014, 308-313; Lee-Reply ¶¶65-66. Indeed, this prior art approach did not require the use of any other openings to perform gate replacement—just the openings that ultimately become the slit structures. *Id.*

Fourth, the ’806 patent’s disclosure further supports that a POSITA would have been able to make the proposed combination. Lee-Reply ¶67. Just like the proposed modification, the ’806 patent uses slit structure openings alone to perform gate replacement. ’806, 16:27-34. And far from disclosing any unconventional means for doing so, the ’806 patent simply notes in a single sentence that this conventional process is performed. Because the ’806 patent “is entirely silent on how to” perform gate replacement using only slit structure openings, it “suggest[s] that a person of ordinary skill in the art was more than

capable of” doing so. *Uber Techs., Inc. v. X One, Inc.*, 957 F.3d 1334, 1339 (Fed. Cir. 2020).

Thus, it would have been well within the skill of a POSITA to adjust Toyama’s design to account for the use of structures 79 (and not structures 679) for gate replacement. Lee-Reply ¶¶65. Despite in effect advancing a teaching-away argument, PO has not shown anything in Toyama or another reference that “criticizes, discredits, or otherwise discourages the solution claimed.” *In re Meza*, 780 F. App’x 895, 902 (Fed. Cir. 2019).

2. A POSITA Would Have Known How To Design The Proposed Combination’s Dielectric Structure So As To Allow The Device To Operate.

PO’s assertion that the proposed combination’s *dielectric structure* renders the device inoperable due to “current restriction” is meritless. POR 42-46.

First, Toyama’s conductive layers are made out of metal, which a POSITA would have understood has very little resistance. Toyama, [0229]; Lee-Reply ¶69. What’s more, the amount of conductive-layer resistance in the proposed modification (low as it is), is not materially higher than in the Second Modification because, as a POSITA knew, resistivity is in large part dependent on the “bottleneck”—that is, the part of the current path with the smallest cross-sectional area. Lee-Reply ¶¶70-72. That bottleneck is not materially changed in the proposed modification. *Id.*

Second, Toyama itself discloses embodiments that place unitary dielectric structures in a memory region:

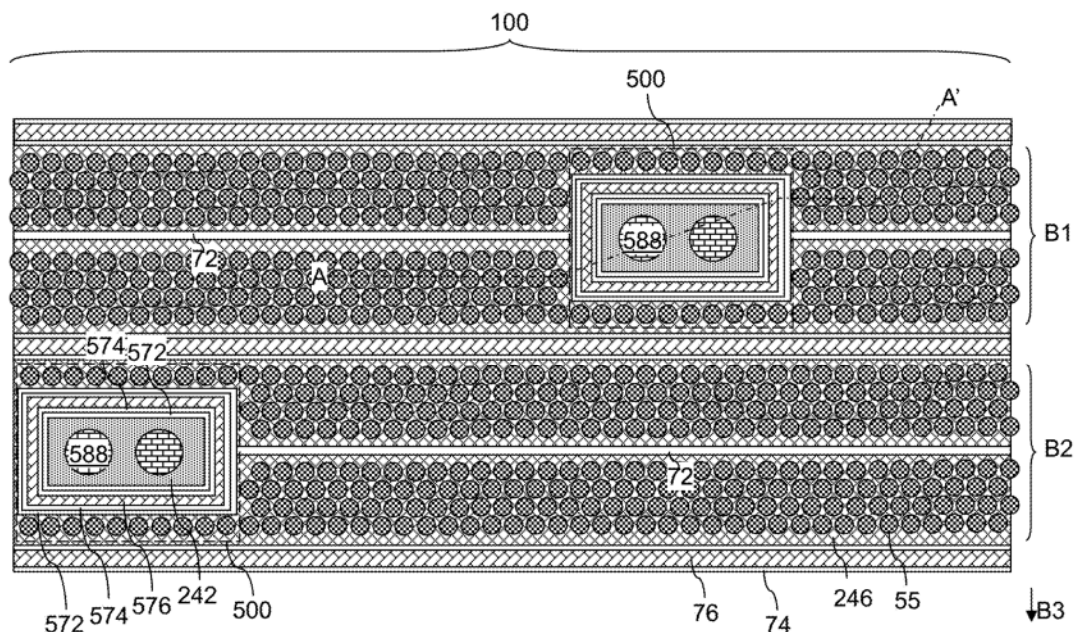


FIG. 39B

Toyama, Figures 39B (element 572), 69B (element 155). Far from the discouragement PO asserts (POR 42-43), Toyama's express disclosure thus confirms to a POSITA that dielectric blocks in the memory array (as in the proposed combination) are viable and desirable. Lee-Reply ¶77.

Third, a POSITA would have known of alternative techniques for propagating the conductive layers' signals to the channel structures that are intended to receive them. For example, a POSITA would have known to use vias (vertical interconnects) to convey an electrical signal to each side of the dielectric structure:

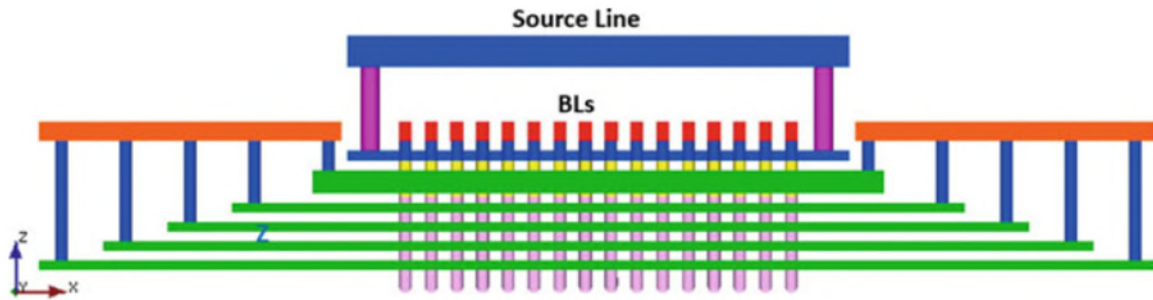


Fig. 4.33 X-Z cross section of Fig. 4.32

Ex. 1013, 120; Lee-Reply ¶78. Because these vias (in blue) are on both sides of the memory strings (in pink), they enable signals to reach both ends of the memory strings even if a dielectric structure blocks signals from traveling from one side to another. *Id.* An annotated, modified version of Figure 48B, below, illustrates how this conventional technique enables electrical signals (red arrows) to reach the NAND strings on both sides of the dielectric structure:

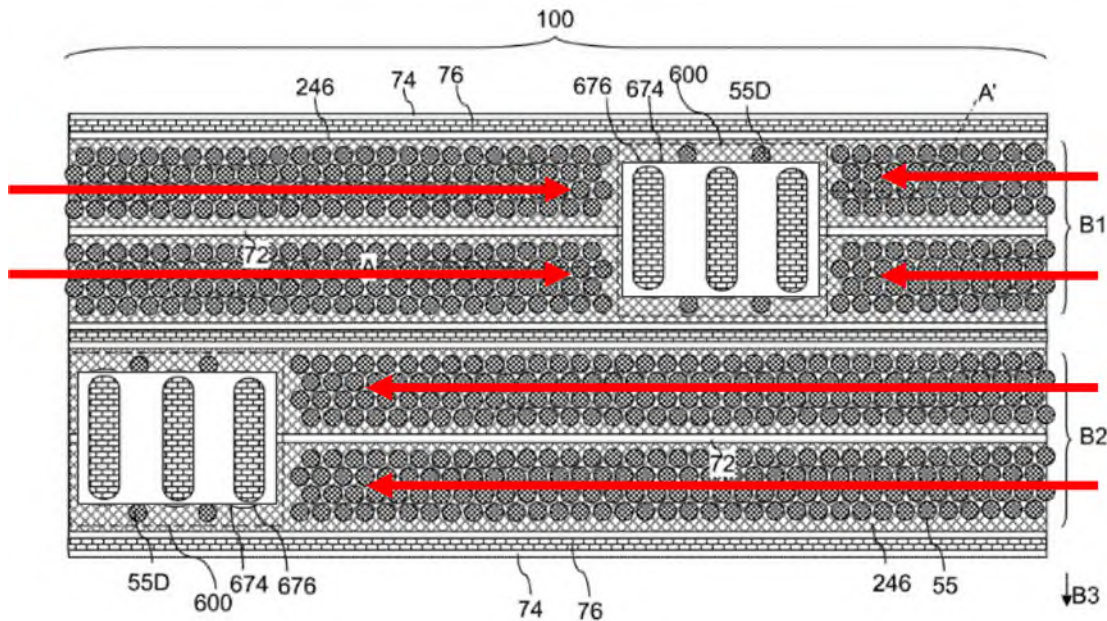


FIG. 48B

Toyama, Figure 48B (modified and annotated); Lee-Reply ¶79.

Fourth, the '806 patent confirms that a POSITA would have been able to size and scale the dielectric structure and the conductive layers so as to design a functional device. Not only are the '806 patent's figures expressly *not* to scale, but the '806 patent does not provide any guidance as to the relative sizes of its *dielectric structures* and its *conductive layers*. Because the '806 patent “is entirely silent on how to” size the dielectric structure and the conductor layer so as to preserve current flow through the conductor layer from one side of the dielectric structure to the other, it “suggest[s] that a person of ordinary skill in the art was more than capable of” doing so. *Uber*, 957 F.3d at 1339; Lee-Reply ¶¶74-76.

Fifth, PO's comparisons between Petitioner's modified version of Figure 48B and the '806 patent's figures are contrary to law. "[F]igures in a patent are not drawn to scale unless otherwise indicated." *Hockerson-Halberstadt, Inc. v. Avia Grp. Int'l, Inc.*, 222 F.3d 951, 956 (Fed. Cir. 2000). Here, that presumption is further buttressed by both references, which expressly state that their drawings are **not** to scale. Toyama, [0156]; '806, 3:57-59.

Flying in the face of this well-established law, many if not most of PO's arguments involve a comparison of the '806 patent's Figure 1A with the Petition's modified Figure 48B. For example, PO asserts that the '806 patent "allows for wide areas around the dielectric structure for current flow through the word lines," which is improperly premised on the relative sizes of the drawn *dielectric structure* (the unitary dielectric fill material) and the width of each drawn *conductive layer* ("electrically conductive layer 246"). POR 43. PO asserts that "[f]orming a unitary dielectric fill material portion in a crowded memory array region with several other structures in its vicinity presents challenges that would have deterred a POSITA and are overcome by the novel teachings of the '806 [patent]," but the degree of "crowded[ness]" is merely an inference from the not-to-scale Figure 48B. POR 44. And although PO generically asserts that "the '806 [patent] has a different arrangement of features in the relevant regions," the only "different arrangement" to which PO has pointed is the difference in the relative scale of

Figure 48B’s *dielectric structure* and its *conductive layer*. *Id.* In fact, there is no material difference in components between the ’806 patent and the proposed modification—only the relative sizes at which those components are shown. PO’s “arguments based on drawings not explicitly made to scale” are thus “unavailing.” *Hockerson*, 222 F.3d at 956.

At bottom, PO’s argument flies in the face of *KSR*, which instructs that “a person of ordinary skill is also a person of ordinary creativity, not an automaton.” *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 421-22 (2007). A POSITA would have been able to design the proposed combination—e.g., size the proposed combination’s unitary dielectric fill material, along with its TACs, and include any other necessary circuitry—so as to preserve the device’s functionality. Lee-Reply ¶¶68-79. Again, PO has not shown anything in Toyama or another reference that “criticizes, discredits, or otherwise discourages the solution claimed.” *Meza*, 780 F. App’x at 902.

3. PO’s Arguments Against Petitioner’s Motivation To Combine Are Factually And Legally Flawed

a. PO’s Capacitive-Coupling And TAC-Placement Objections Are Legally Irrelevant

Putting aside PO’s meritless teaching-way arguments (addressed in §§V.A.1, V.A.2), PO does not dispute that the proposed combination “is nothing more than the mere substitution of one element (the Second Modification’s ‘insulating liners

674’) for another known in the field (a unitary dielectric fill material, as in the first exemplary structure’s ‘dielectric fill material portion 430”) to yield a predictable result (e.g., electrically isolating the Second Modification’s ‘through-memory-level via structures’).” Pet. 100-102. That, alone, is sufficient to show motivation to combine. *KSR*, 550 U.S. at 417.

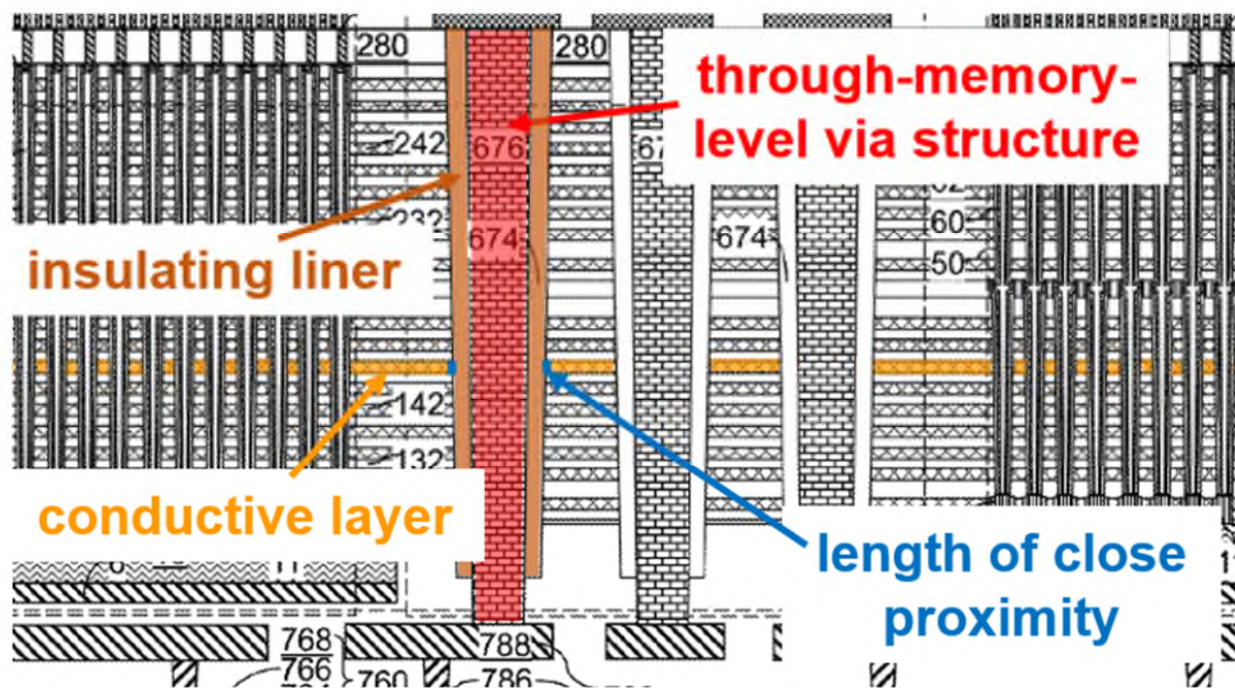
The arguments that PO does advance—pertaining to capacitive coupling and the placement of the TACs within the memory region—are in effect arguments that the proposed combination is not **superior** to Toyama’s expressly disclosed embodiments. But Petitioner does not need to show that the proposed combination is “an ‘improvement’ in a categorical sense.” *Intel Corp. v. PACT XPP Schweiz AG*, 61 F.4th 1373, 1380 (Fed. Cir. 2023) (emphasis in original).

b. PO’s Objection To Petitioner’s Capacitive-Coupling Benefit Is Meritless

PO’s assertion that capacitive coupling was already “minimiz[ed]” in Toyama’s Second Modification is both legally and factually flawed. POR 47. As an initial matter, PO does not dispute that the proposed modification would reduce capacitive coupling. Pet. 102-103; Lee ¶186. Instead, PO contends that the reduction allegedly would be immaterial because, to PO, the Second Modification already “minimizes” capacitive coupling. POR 46. But the passage in Toyama on which PO relies actually confirms the opposite: a POSITA would have been motivated to reduce capacitive coupling in Toyama’s designs. Lee-Reply ¶¶80-83

(discussing Toyama, [0337]). And even if PO's contention is taken as true, it does nothing to rebut the only thing that the Petitioner "ha[s] to show": that the proposed combination was a "suitable option." *Intel*, 61 F.4th at 1381.

What's more, PO's argument overlooks a key aspect of the modified device's structure. PO highlights a single conductive layer and asserts that capacitive coupling between that conductive layer and the through-memory-level via structure is minimal because the "length of close proximity" is small:



POR 47. But PO ignores that there are over a dozen conductive layers 146, 246 shown in Figure 49, which PO annotates (there may be many dozens in a real device), and each of them can capacitively couple to the through-memory-level via structure. Lee-Reply ¶¶83-84. Thus, the degree of capacitive coupling is far

greater than what PO suggests, and a POSITA would have seen a benefit in reducing it. Lee-Reply ¶¶83-84.

c. PO's Objection To Petitioner's TAC-Placement Benefit Is Meritless

PO does not dispute that placing the TACs within the memory array has certain benefits identified in the Petition (at 104-105), yet apparently contends that these benefits are irrelevant because one the two combined embodiments (Toyama's Second Modification) already has these benefits. POR 47-48. But, in an obviousness analysis, it is almost always the case that one of two references or embodiments being combined has a benefit that the combination achieves; that cannot negate a motivation to combine.

Contrary to PO's position, the law does not require Petitioner to demonstrate that the combination is "an 'improvement' in the categorical sense." *Intel*, 61 F.4th at 1381. The Petitioner has shown that the proposed combination is "nothing more than the mere substitution of one element ... for another known in the field ... to yield a predictable result." Pet. 101. That is sufficient to demonstrate a motivation to combine.

B. [8.H]

PO's argument that Ground 3 fails to render limitation [8.H] obvious fails for all the reasons explained above for Ground 1. §III.B.

VI. CONCLUSION

The Board should hold all Challenged Claims unpatentable.

Respectfully submitted,

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CERTIFICATE OF COMPLIANCE

The undersigned certifies that the foregoing Petitioner's Reply complies with the type volume limitation in 37 C.F.R. § 42.24. According to the utilized word-processing system's word count, the petition—excluding the caption, table of contents, table of exhibits, mandatory notices, certificate of word count, and certificate of service—contains 5,584 words.

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