

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,

Petitioner,

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,

Patent Owner.

Case IPR2024-00791

Patent 10,937,806

PATENT OWNER'S SUR-REPLY

TABLE OF CONTENTS

LIST OF EXHIBITS	v
LIST OF ABBREVIATIONS	vi
I. INTRODUCTION	1
II. CLAIM CONSTRUCTION	3
A. “a dielectric structure” and “a plurality of through array contacts (TACs) extending vertically through the dielectric structure” (Claim 8).....	3
III. Ground 1: Toyama’s Second Modification	7
A. Toyama’s Second Modification Does Not Disclose or Render Obvious “a Plurality of Through Array Contacts (TACs) Extending Vertically Through the Dielectric Structure”	7
B. Toyama’s Second Modification Does Not Disclose or Render Obvious “a Plurality of Non-Electrically Functional Channel Structures Surrounding the TAC Region”	10
IV. Ground 2: Toyama’s First Exemplary Structure	16
A. Petitioner’s Modification Results in Multiple Devices, None of Which Meet the Claimed Configuration	16
B. Petitioner’s Modification Results in an Inoperable Device	20
V. Ground 3: Toyama’s Second Modification in Combination with Toyama’s First Exemplary Structure.....	24
A. A POSITA Would Not Have Found It Obvious to Modify Toyama’s Second Modification in the Proposed Manner.....	24
1. Petitioner’s Obviousness Combination Would Fail with Respect to Gate Replacement	24
2. Petitioner’s Obviousness Combination Would Block Current and Render the Device Inoperable.....	26
3. Petitioner’s Proposed Motivations for the Obviousness Combination are Flawed	30
B. Petitioner’s Obviousness Combination Does Not Disclose or Render Obvious “a Plurality of Non-Electrically Functional Channel Structures Surrounding the TAC Region”	32
VI. CONCLUSION.....	33

TABLE OF AUTHORITIES

	Page(s)
Cases	
<i>ABS Glob., Inc. v. Cytonome/St, LLC</i> , 84 F.4th 1034 (Fed. Cir. 2023)	6
<i>Baldwin Graphic Sys., Inc. v. Siebert, Inc.</i> , 512 F.3d 1338 (Fed. Cir. 2008)	6, 7
<i>Carrum Techs., LLC v. Ford Motor Co.</i> , No. CV 18-1647-RGA, 2023 WL 7407778 (D. Del. Nov. 9, 2023)	6
<i>Catalina Mktg. Int’l, Inc. v. Coolsavings.com, Inc.</i> , 289 F.3d 801, 808 (Fed. Cir. 2002)	19
<i>Commscope, Inc. v. Tq Delta, LLC</i> , 2023 WL 7491181 (P.T.A.B. Nov. 13, 2023)	29
<i>Finjan LLC v. SonicWall, Inc.</i> , 84 F.4th 963 (Fed. Cir. 2023)	5, 6, 8, 19
<i>Henny Penny Corp. v. Frymaster LLC</i> , 938 F.3d 1324 (Fed. Cir. 2019)	1
<i>Intel Corp. v. PACT XPP Schweiz AG</i> , 61 F.4th 1373 (Fed. Cir. 2023)	29, 30
<i>KCJ Corp. v. Kinetic Concepts, Inc.</i> , 223 F.3d 1351 (Fed. Cir. 2000)	5, 6
<i>Salazar v. AT&T Mobility LLC</i> , 64 F.4th 1311 (Fed. Cir. 2023)	5, 19
<i>Uber Techs., Inc. v. X One, Inc.</i> , 957 F.3d 1334 (Fed. Cir. 2020)	25

Other Authorities

37 C.F.R. § 42.23(b)	1
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LIST OF EXHIBITS

Exhibit	Description
Ex. 2001	Joint Claim Construction Statement
Ex. 2002	Micron’s Preliminary Claim Constructions
Ex. 2003	YMTC’s Proposed Claim Constructions
Ex. 2004	February 19, 2025, Declaration of Dr. Yang (“Yang”)
Ex. 2005	File History of U.S. Patent No. 10,658,378 B2 to Tao et al.
Ex. 2006	Transcript of January 30, 2025, Deposition of Dr. Jack Lee
Ex. 2007	U.S. Patent No. 10,559,583 B2 to Park et al. (“Park”)
Ex. 2008	Transcript of June 13, 2025 Deposition of Dr. Jack Lee

LIST OF ABBREVIATIONS

Abbreviation	Term
'806 or '806 patent	U.S. Pat. No. 10,937,806
'806FH	File History of U.S. Pat. No. 10,937,806
Board or PTAB	Patent Trial and Appeal Board
Challenged Claims	'806 patent, claims 8-9, 11-12
DI	Decision Granting Institution for <i>Inter Partes</i> Review of U.S. Patent No. 10,937,806 (IPR2024-00791, Paper 11)
Lee(I)	May 2, 2025, Declaration of Dr. Jack C. Lee (Ex. 1003)
Lee(II)	May 14, 2025, Reply Declaration of Dr. Jack C. Lee (Ex. 1043)
Office or USPTO	U.S. Patent and Trademark Office
Parallel district court litigation	<i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc.</i> , NDCA-3-23-cv-05792 (N.D. Cal.)
Patent Owner or PO	Yangtze Memory Technologies Company, Ltd.
Petition or Pet.	Petition for <i>Inter Partes</i> Review of U.S. Patent No. 10,937,806 (IPR2024-00791, Paper 1)
Petitioner	Micron Technology, Inc.
POR	Patent Owner Response for <i>Inter Partes</i> Review of U.S. Patent No. 10,937,806 (IPR2024-00791, Paper 14)
POSITA	Person of ordinary skill in the art
Reply	Petitioner's Reply for <i>Inter Partes</i> Review of U.S. Patent No. 10,937,806 (IPR2024-00791, Paper 16)
Toyama	U.S. Patent Publication No. 2017/0179026

I. INTRODUCTION

Petitioner's Reply fails to address the issues raised in the POR, misunderstands the prior art, and misrepresents PO's positions. In addition, the Reply introduces new arguments, which the Board should disregard, as Petitioner needed to make its entire case in the Petition. 37 C.F.R. § 42.23(b); *Henny Penny Corp. v. Frymaster LLC*, 938 F.3d 1324, 1330-31 (Fed. Cir. 2019) (rejecting attempts to broaden the petition's ground in its reply). Because Petitioner has not been able to remedy the deficiencies in its Petition, the Board should uphold the validity of all Challenged Claims.

Ground 1 relies on an embodiment of Toyama called the "Second Modification." That disclosure, however, fails to teach "a plurality of through array contacts (TACs) extending vertically through the dielectric structure" as required by Claim 8 because the purported TACs each extend through separate insulating liners and not through the same dielectric structure. Petitioner's counterarguments contravene well-established Federal Circuit precedent that one instance of an element must meet all requirements of the claim for that element. Additionally, Toyama's Second Modification does not teach "a plurality of non-electrically functional channel structures surrounding the TAC region," as its structures are only on opposite sides of the alleged TAC region, and do not surround it.

Ground 2 relies on a different embodiment of Toyama called the “First Exemplary Structure.” The placement of the TAC region in this embodiment, however, is to one side of the channel region—not “formed between the first and second channel regions” as required. Petitioner’s proposed modification—adding a second memory plane—does not address this deficiency, as it merely places two separate memory devices side-by-side, rather than creating a memory device with two channel regions and a TAC region between them. Not only does this not meet the claims, but Petitioner also ignores that such a modification would eliminate the peripheral circuitry and interconnects that are already in that location according to Toyama. Petitioner’s Reply falls far short of curing these deficiencies.

Ground 3 is Petitioner’s redesign of Toyama’s Second Modification using Toyama’s First Exemplary Structure’s unitary dielectric fill material. Petitioner fails to show that this modification would have been obvious as it not only eliminates a critical aspect of Toyama’s gate replacement process but also drastically restricts current flow in each of the gate layers. Petitioner’s purported motivations for doing so are belied by its own expert.

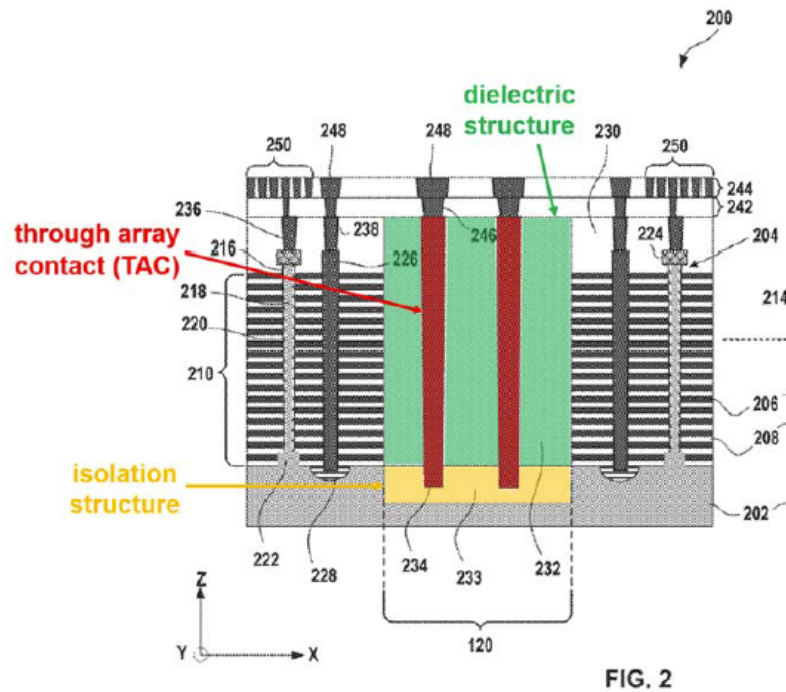
As explained in the POR and further detailed herein, Petitioner’s grounds do not satisfy the requirements for a showing of obviousness.

II. CLAIM CONSTRUCTION

A. “a dielectric structure” and “a plurality of through array contacts (TACs) extending vertically through the dielectric structure” (Claim 8)

Claim 8’s “a plurality of through array contacts (TACs) extending vertically through the dielectric structure” limitation requires multiple “through array contacts (TACs)” to extend through the same dielectric structure. Despite the plain language of this limitation, Petitioner incorrectly argues that it allows for multiple TACs extending vertically through multiple dielectric structures, such that no single dielectric structure includes more than one TAC. Reply, 2-3.

First, consistent with the claims, the disclosed embodiments with multiple TACs in the ’806 depict the TACs extending through the same dielectric, e.g., as shown in Figure 2:



Petitioner's mischaracterization of the '806 as "contemplat[ing] embodiments with multiple dielectric structures (each of which includes a single TAC)" is wrong. The passage in question ('806, 21:11-28) simply describes the formation of a single TAC within "the dielectric structure" rather than the claimed plurality of TACs just as it describes the formation of a single "channel structure" in the "alternating dielectric layer stack." There is no suggestion of using multiple dielectric structures, much less using a single TAC in each of the multiple dielectric structures. Using a separate dielectric structure for each TAC would contravene the '806 objective to reduce fabrication complexity and cost. See POR 5-6; Yang ¶¶ 32-33; '806, 10:64-11:7, 20:33-41. Petitioner offers no response other than the unsupported assertion that such an embodiment is claimed. Reply, 3.

Second, Petitioner’s understanding of Federal Circuit precedent is flawed. While an indefinite article “a” does not preclude more than one, there must still be at least one instance of the element, e.g., in the accused system or the prior art, that meets all the requirements of the claim for that element. *See Finjan LLC v. SonicWall, Inc.*, 84 F.4th 963, 974-75 (Fed. Cir. 2023) (“Even if an infringing system can use ‘one or more computers,’ the plain language of the claims requires at least one of those computers to perform all the functions listed in the claims of the ARB Patent.”); *Salazar v. AT&T Mobility LLC*, 64 F.4th 1311, 1317 (Fed. Cir. 2023) (“Here, it does not suffice to have multiple microprocessors, each able to perform just one of the recited functions; the claim language requires at least one microprocessor capable of performing each of the recited function.”). Thus, here one dielectric structure must meet all the requirements applicable to it, i.e., having TACs (plural) extending through it. The Board correctly concluded as much in its institution decision: “[w]hile the open-ended language may permit the claimed memory device to have more than one dielectric structure, this does not change the claim language that requires multiple TACs to extend vertically through a single dielectric structure.” DI, 17; *see also* POR, 20-22.

Petitioner’s cited cases (Reply 3-5) are inapposite, as they were not addressing the *Finjan* issue applicable here. *KCJ* merely addressed whether “a ... continuous ... chamber” encompasses one or more chambers, and not whether the same chamber

must satisfy each reference to the chamber throughout the claim. *KCJ Corp. v. Kinetic Concepts, Inc.*, 223 F.3d 1351, 1355-57 (Fed. Cir. 2000) (addressing only whether “an accused device having one or more continuous chambers would fall within the scope of clause (a)” which recites “a lower, continuous, inflatable chamber having an air-permeable, flexible upper wall portion”). Similarly, *ABS* addresses whether the claimed flow channel’s focusing region must be “configured for only a single sample stream” (i.e., whether the term excludes a second stream), which is a separate issue from whether the same sample stream must meet all the claimed requirements. *ABS Glob., Inc. v. Cytonome/St, LLC*, 84 F.4th 1034, 1040-43 (Fed. Cir. 2023); *Carrum Techs., LLC v. Ford Motor Co.*, No. CV 18-1647-RGA, 2023 WL 7407778, at *5 (D. Del. Nov. 9, 2023) (“Plaintiff’s reliance on *ABS Global* is misplaced because the Federal Circuit addressed a different issue there.”).

Petitioner’s reliance on *Baldwin* (Reply, 4-5) fares no better, and indeed the Federal Circuit in *Finjan* expressly distinguished *Baldwin* as directed to a separate issue. As the Court explained, while *Baldwin* addressed the principle that the indefinite article *a* means one or more, the decision was “***not addressing whether the use of a definite article to refer to the initial antecedent phrase requires the same component to perform the later limitation.***” *Finjan*, 84 F.4th at 974 (citing *Baldwin Graphic Sys., Inc. v. Siebert, Inc.*, 512 F.3d 1338, 1342 (Fed. Cir. 2008)). For example, while the court concluded that “said fabric roll having a sealed sleeve”

does not preclude multiple fabric rolls sharing a single sealed sleeve, *Baldwin*, 512 F.3d at 1340-43, there must still be a fabric roll that meets all the limitations including the claimed sleeve requirement, which is a separate issue that *Baldwin* did not address.

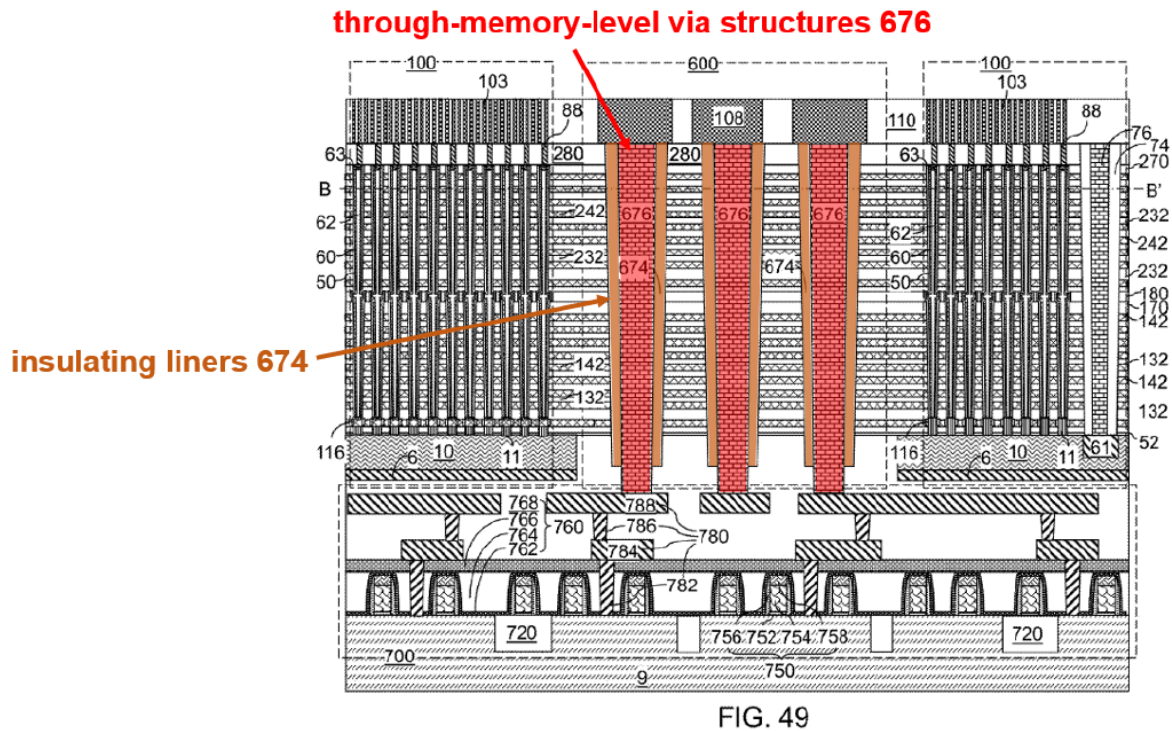
Thus, claim 8 requires that the “through array contacts (TACs)” must extend through the same dielectric structure.

III. GROUND 1: TOYAMA’S SECOND MODIFICATION

Toyama’s Second Modification fails to disclose or render obvious the Challenged Claims at least because Toyama’s Second Modification fails to disclose or render obvious multiple elements of claim 8—the sole independent claim.

A. Toyama’s Second Modification Does Not Disclose or Render Obvious “a Plurality of Through Array Contacts (TACs) Extending Vertically Through the Dielectric Structure”

As explained in the POR, Toyama’s Second Modification neither discloses nor renders obvious “a plurality of through array contacts (TACs) extending vertically through the dielectric structure.” POR, 18-22. Toyama shows only a single through-memory-level via structure 676 (purported TAC)—extending through any one insulating liner 674 (purported dielectric structures), so no “plurality” of TACs traverses a given dielectric structure:



Toyama, Fig. 49 (annotated by PO showing Petitioner’s mapping). Petitioner’s Reply does not cure this deficiency in Toyama’s Second Modification.

First, Petitioner’s claim construction arguments (Reply, 6-7) conflict with controlling precedent. See §II.A. *Finjan* requires that at least one recited element—here, a dielectric structure—to contain all claimed features. Petitioner’s construction ignores that requirement.

Petitioner’s fallback argument that Toyama’s discrete liners collectively form a dielectric structure (Reply, 7-11) also misses the mark. The Board already rejected this theory when Petitioner could not “sufficiently explain how multiple constructed items can be considered...a single structure” under the very definition of “structure” (as “something...that is constructed”) that Petitioner advanced. DI, 17-18; cf. Pet.

31-32. Switching definitions in the Reply (Reply 8)—now quoting “something arranged in a definite pattern of organization” (Ex. 1021, 4) does not fix the problem. Every component in a semiconductor is patterned with photolithography, yet that does not collapse distinct items into one “structure.” Therefore, Petitioner’s mapping remains deficient.

Unable to ground its position in intrinsic evidence, Petitioner cites the below photographs of a wooden fence and staircase:



Ex. 1045



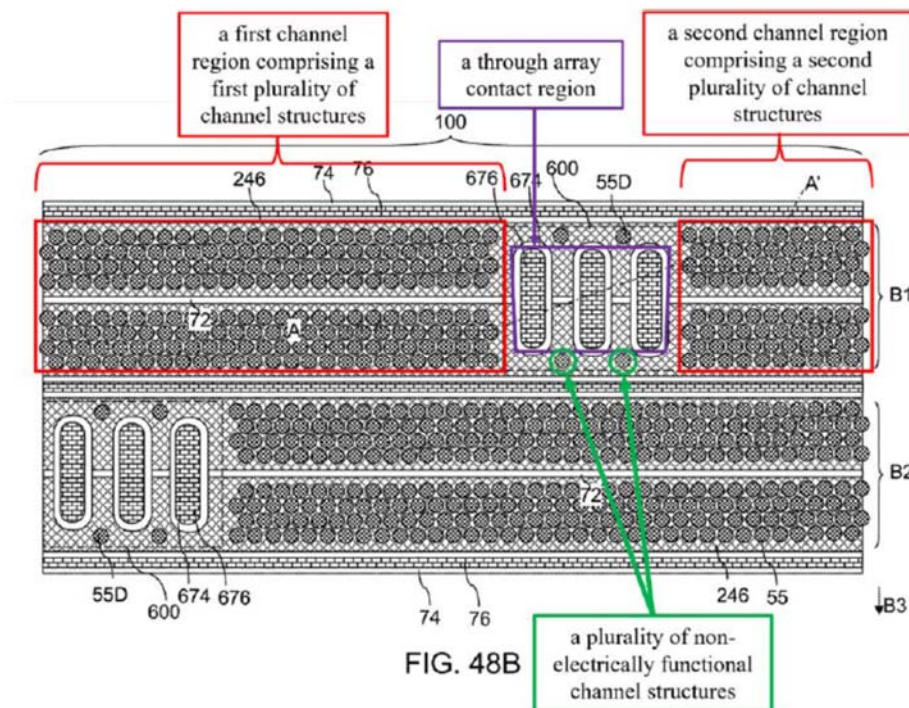
Ex. 1046

These examples are inapposite. Unlike Toyama’s liner, which independently serves as a dielectric isolating the TAC, a single post or step cannot function as a wall or staircase structure, respectively. Also, Petitioner claims the wall’s “components [] are not all touching each other,” but the posts visibly do touch; moreover as Dr. Yang testified, a wall would include additional material binding the posts together—otherwise they would “fall over.” Ex. 1044, 47:23-25, 52:7-53:8. Likewise, Dr.

Yang explained that “integral to the staircase structure” above is a “strong anchoring structure built into the wall” connecting the steps. *See* Ex. 1044, 48:2-50:16. Petitioner’s expert agrees. *See* Ex. 2008, 86:5-90:2 (admitting a staircase structure requires “provid[ing]...intended function”), 94:11-97:9 (admitting that without the additional anchoring mechanism of the wall the steps would “no longer exist as a functional unit”). The cited structures therefore consist of contiguous, integrated elements, and Petitioner’s reliance on them is misplaced.

B. Toyama’s Second Modification Does Not Disclose or Render Obvious “a Plurality of Non-Electrically Functional Channel Structures Surrounding the TAC Region”

Toyama’s Second Modification neither discloses nor renders obvious “a plurality of non-electrically functional channel structures surrounding the TAC region.” *See* POR, 22-25. Petition’s own annotation of Fig. 48B below shows the purported non-electrically functional channel structures (green) flank the alleged TAC region (purple) on two sides; they do not surround it.



Pet. 52 (Petitioner's annotations of Toyama, Fig. 48B).

The structures fail to surround the region under any reasonable reading; therefore, construing “surrounding” is unnecessary. POR, 24. Rejecting Petitioner's attempts to stretch “surrounding” to cover “features...on just two sides” is not “contrary” to the term's plain meaning. *Contra* Reply 12. Petitioner's “isthmus” analogy (Pet. 51; Ex. 1022), while misplaced, also does not support Petitioner's argument. An isthmus is a land mass bordered by water **along its full length** on two sides, which in no way resembles Toyama's two small dummy structures 55D above and below of the purported TAC region.

Nor does the '806 support Petitioner. *Contra* Reply 12. The specification's use of “surrounded” aligns with PO's interpretation and does not encompass

Toyama's dummy structures configuration. The '806 states that dielectric structures of Figs. 1A-C are "surrounded by conductor/dielectric stack 210"—which confirms that the conductor/dielectric stack is on more than just two sides of the dielectric structures. '806, 10:29-31. Contrary to Petitioner's arguments (Pet. 51-52, 60-61), the figures show the conductor/dielectric stack beyond two sides of each dielectric structure. Figure 1A illustrates the stack (lavender) on all four sides of the dielectric structure (pink) (indicated by regions of non-electrically functional channels 122 and contacts 132 (black circles) on all four sides):

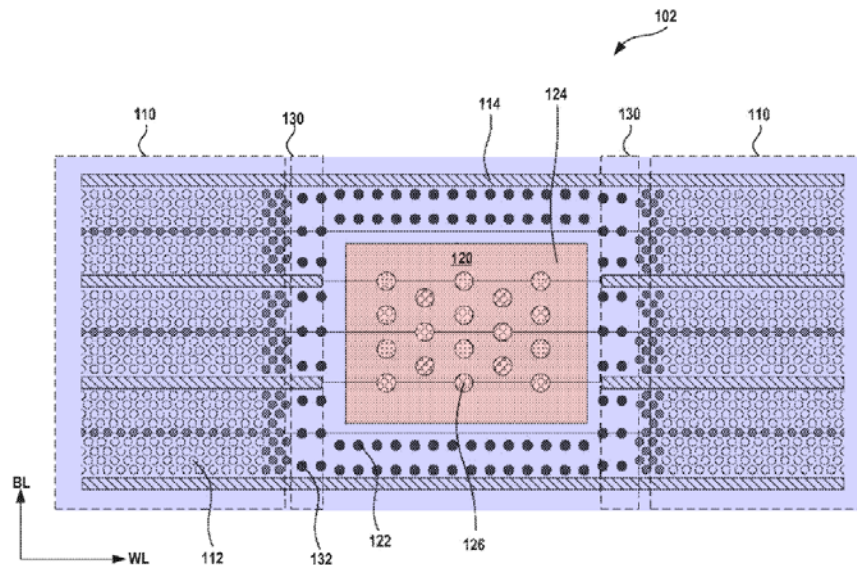
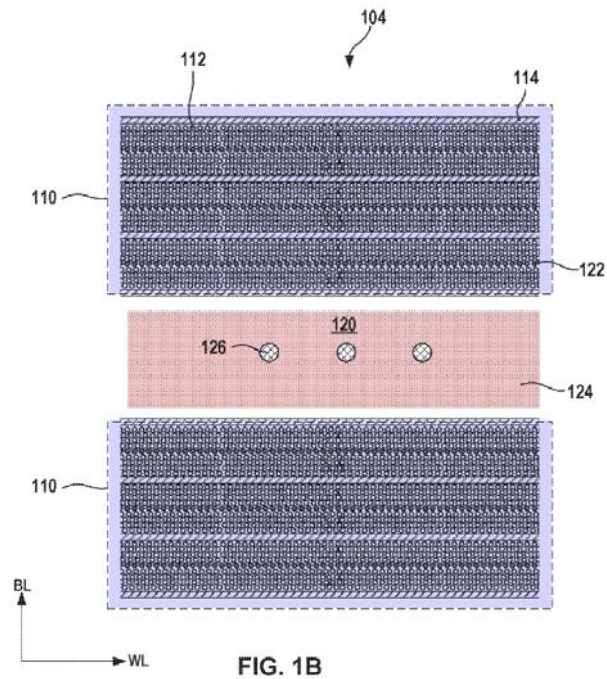


FIG. 1A

'806, Fig. 1A. Figure 1B shows conductor/dielectric stack (lavender) of the NAND string regions 110 extending beyond just the two sides of the dielectric structure 124 (pink):



'806 Fig. 1B (annotated). And Figure 1C (below) illustrates the conductor/dielectric stack (lavender) that forms the staircase region on more than just two sides of the dielectric structure 124 (pink):

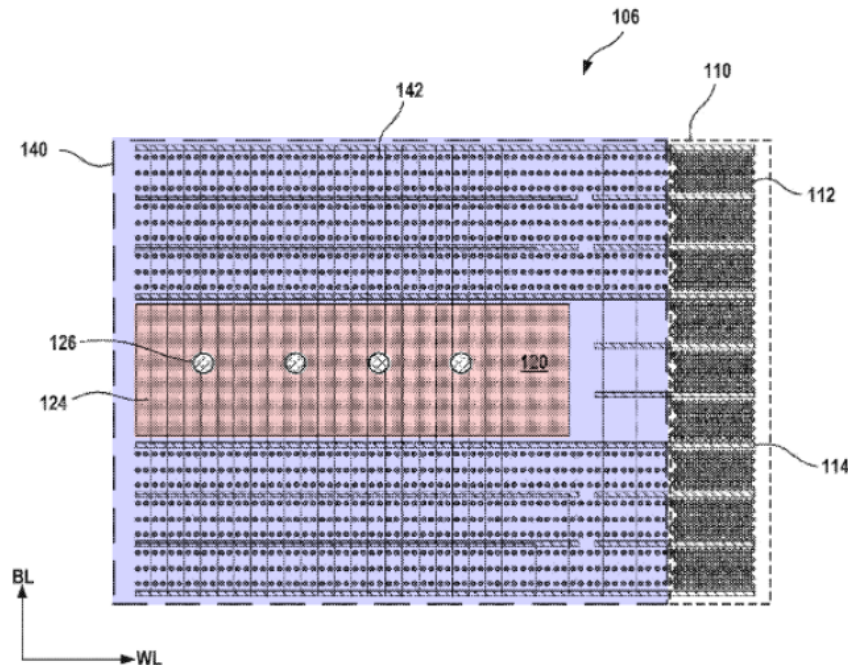


FIG. 1C

'806 Fig. 1C (annotated); *contra* Pet. 60-61 (incorrectly stating “dielectric structure 124 borders...staircase (i.e. word line) regions 140” “above and below” only), 52 (same).

On Reply, Petitioner’s attempt to stretch Toyama’s disclosure—that dummy structures 55D are “provided at the periphery” of TAC region 600—fails. Reply 12 (citing Toyama, [0333]). “[A]t a periphery” does not mean the dummy structures are present “along the entire periphery.” Toyama simply describes what Fig. 48B shows—a couple of dummy structures 55D at the top and bottom edges (i.e., at the

periphery, not the center) of the TAC region 600.¹ And Dr. Lee’s new assertion that a POSITA would add dummy channels to the other sides of region 600 (Ex. 1043, ¶23) due to “edge effects” is untimely and should have been raised in the Petition. Further, this assertion is conclusory and lacks evidence that such “edge effects” were “well known,” would occur at the sides of region 600, or that dummy structures would mitigate these effects.

Petitioner’s argument that a POSITA would have found it obvious to “[p]lac[e] dummy stack structures on all sides of the TAC region” (Pet. 53-54; Reply 13) lacks merit. And Petitioner’s assertion that this would provide “additional structural support” where “memory stack structures are not formed at a sufficiently high density” lacks evidentiary support. Pet. 53-54; Lee(I) ¶121 (quoting Toyama, [0182]); Lee(II) ¶24. Toyama contemplates “support pillar structures” near the staircase region, where memory stack structures are sparse (Toyama, Figs. 4A-4B; [0182]), but Petitioner has not shown that the periphery of the “through-memory-level via region” where channel structures are present, is similarly sparse. In fact, the left and right sides of the through-memory-level via region 600, where Petitioner

¹ Dr. Yang’s statement that a rectangle’s periphery is “the four sides of the rectangle” does not support Petitioner’s interpretation (Reply 12). Any location on one side of the rectangle is “at a periphery.”

proposes adding dummy stack structures, border memory stack structures (Toyama, Fig. 48B). Replacing them with dummy stack structures would only reduce memory capacity without adding mechanical support, since the memory stack structure already provides it.

IV. GROUND 2: TOYAMA’S FIRST EXEMPLARY STRUCTURE

Toyama’s First Exemplary Structure does not disclose or render obvious the Challenged Claims at least because it fails to teach “*a through array contact (TAC) region formed between the first and second channel regions,*” as required by independent claim 8. Specifically, the purported TAC region in Toyama’s structure is located to the side of a single, centralized channel region, not between two channel regions. Furthermore, Petitioner’s proposed modification adding a second memory device (plane) with its own channel region does not address this deficiency. See POR 25-37. Petitioner’s attempt to satisfy the claim using multiple 3D memory devices contradicts relevant case law and renders the Toyama’s memory structure inoperable. Petitioner’s Reply does not overcome these arguments.

A. Petitioner’s Modification Results in Multiple Devices, None of Which Meet the Claimed Configuration

Contrary to Petitioner’s incorrect assertion (Reply 13), the POR explains that, even if implemented, Petitioner’s modification would yield multiple memory devices—not a single device that satisfies the elements of claim 8. POR 25-26.

Petitioner’s modification duplicates elements of Toyama into several independent memory planes (i.e., multiple memory devices) in an attempt to satisfy claim 8, but this fragments the claim’s requirements of its “three-dimensional (3D) memory device.” Petitioner argues the claim allows for multiple 3D memory devices. Even if multiple devices are permitted, at least one device must meet all claim limitations, which Petitioner’s modification does not provide.

Petitioner does not dispute that its “modification adds a second memory device” to meet claim 8. POR 25-26, 28-29; *Cf.* Reply 14-17. Petitioner’s argument that “one ‘device’ can be part of another ‘device’” (Reply 14-16), is irrelevant to the meaning of “3D memory device,” as these limitations cannot be satisfied by features spread across different devices. Petitioner’s interpretation would unreasonably mean that any device containing one or more 3D memory devices—such as a hard drive, backup server, a server farm, or any plane, ship, or car with 3D flash memory used to store navigation data—would itself be a 3D memory device.² These claims are not directed to all memory devices everywhere or even ten, or five, or two 3D

² Dr. Lee’s examples from the extrinsic evidence about the usage of the term “device” (Ex. 1043, ¶¶33, 35-37) and Dr. Yang’s acknowledgement that a solid-state drive is a device (Ex. 1043, ¶38) are equally irrelevant.

memory devices within a larger device; they are directed a single “three-dimensional (3D) memory device” that must meet each of the claimed requirements.

Petitioner’s selective citation to the specification does not support its interpretation that a “3D memory device” can include such devices that separately satisfy different claim requirements. *Cf.* Reply, 14 (citing ’806, 5:30-37). The referenced passage does not define “3D memory device” as encompassing multiple 3D memory devices, and both the claims and specification are directed to a single device’s fabrication and configuration (not to the improvement of hard drives by adding more 3D memory devices).

Petitioner also misinterprets another ’806 passage, claiming a 3D memory device can include both an array device and a peripheral device on different substrates.³ Reply, 14-15 (citing ’806, 7:53-57); Ex. 1043, ¶34. This passage does not describe channel regions on different substrates or suggest that claim limitations can be met by features on different planes. Instead, the ’806 requires both channel regions to be part of the same memory device. *See* POR, 29 (citing ’806, 11:8-14);

³ Dr. Lee incorrectly equates the term “substrate” with “wafer” (Lee(II) at 24 n.3), when the specification defines “substrate” more generally as “material onto which subsequent material layers are added” (’806 4:47-49).

Yang, ¶69 (citing '806 Figs. 1A-B and 2). Toyama neither discloses nor suggests this arrangement.

Petitioner next argues that the “a” in “a three-dimensional (3D) memory device” may be plural. Reply, 17. However, the dispute is whether a single device must satisfy all limitations, regardless of additional devices present. Petitioner’s position—that different devices can collectively meet the claim—contradicts Federal Circuit precedent such as *Finjan* and *Salazar* (see §II.A) and leads to unreasonable results, e.g., a collection of devices where one has a dielectric structure, another has a staircase structure, and yet another has slit structures, could collectively meet the claim. Such a collection of devices is outside the claim’s scope. Petitioner’s reliance on *Catalina Mktg. Int’l, Inc. v. Coolsavings.com, Inc.* is misplaced. Reply 16 (citing 289 F.3d 801, 808 (Fed. Cir. 2002)). As Petitioner’s flawed interpretation demonstrates, the preamble’s “three-dimensional (3D) memory device” is necessary to “define[] a structurally complete invention.” 289 F.3d at 808.

Petitioner incorrectly claims that PO limits the benefit to placing a TAC region between channel structures. Reply, 15-16; Ex. 1043, ¶¶39-41. This is not the case. The claims only require that at least one TAC region be between a first and second channel region of the same device. The presence of a TAC region elsewhere (e.g.,

in the staircase region as Fig. 1C shows), does not change that the **same** “3D memory device” includes a TAC region between two channel regions (as Fig. 1A shows).

B. Petitioner’s Modification Results in an Inoperable Device

Petitioner’s proposed modification results in a configuration missing the essential interconnects and support circuitry for an operable device. POR, 30-35. Specifically, duplicating memory-cell structures of Figure 17E next to one another along the hd1 axis (*see* Pet. 69) causes the left memory structure to overlap with the right memory cell’s peripheral circuitry (shown in Fig. 17F, purple)—making one or both memory structures inoperable:

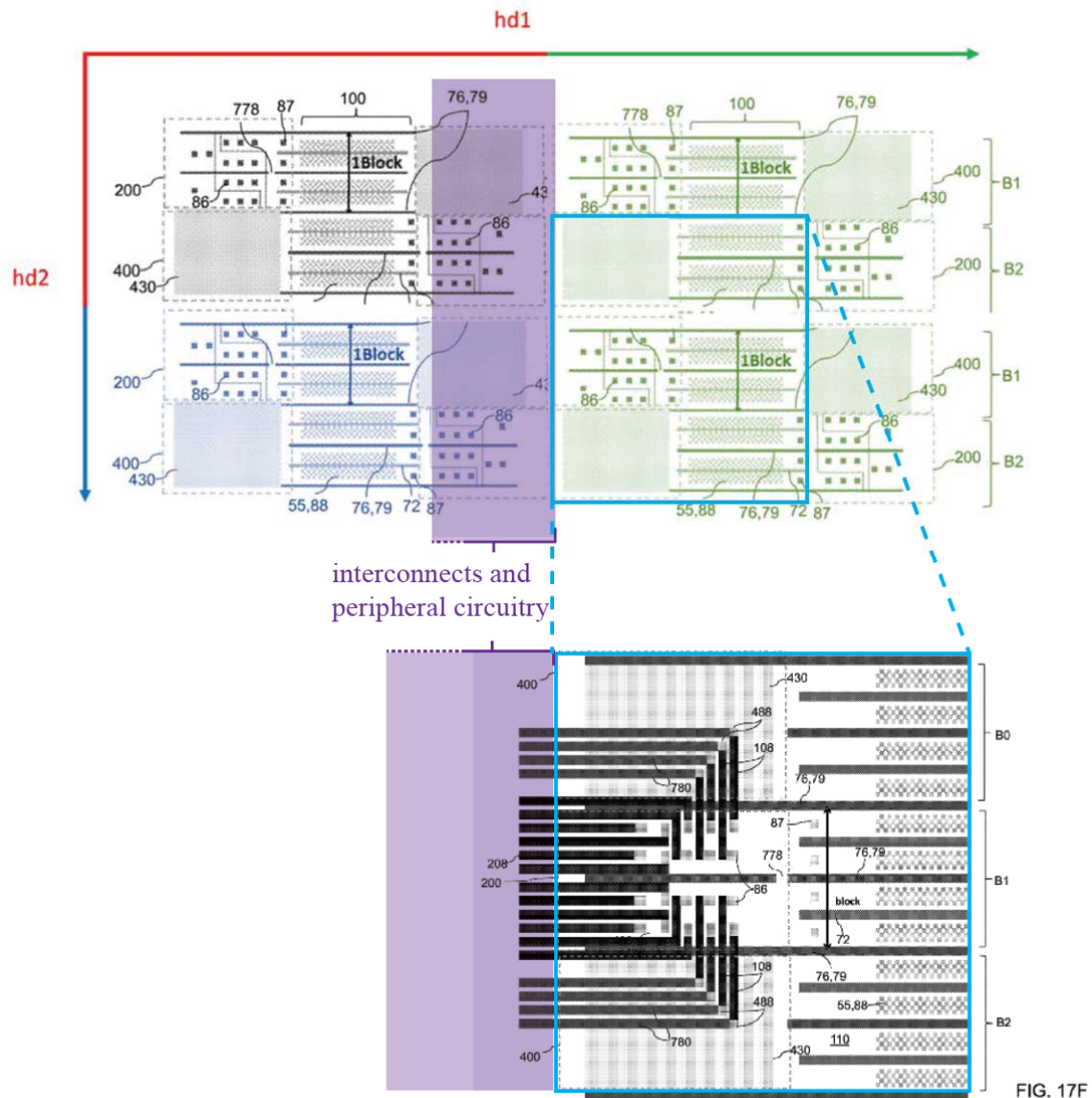


FIG. 17F

Pet. 69 (top, modifying Toyama, Fig. 17E with PO's purple and blue annotations) and Fig. 17F (annotated by PO) (bottom); see also POR, 30-35; Yang, ¶¶72-75. Petitioner's attempt to dismiss Toyama's Fig. 17F as merely an "alternative" or optional, "exemplary structure" (Reply, 17) is incorrect. Toyama states that "FIGS. 17E and 17F are top-down views of" the same structure (Toyama, [0049]), and the "repeat[ed] layout shown in Fig. 17E in the hd1 and hd2 directions, **as shown** in the

modified picture [above]” is the trial ground (Pet. 69 (emphasis added)). Petitioner cannot just ignore critical elements of the structure that forms the trial ground depicted in Fig. 17F.

Petitioner’s “bodily incorporation” arguments are unavailing. Reply, 18-19. The POR addresses the modification set forth in the Petition (Pet. 69). It is Petitioner that did not consider Toyama’s full structure when it “repeat[s] the layout shown in Fig. 17E.” *Id.* Attempts in the Reply to cure this deficiency are untimely. Petitioner’s argument that upper-level interconnects may be omitted because Toyama uses permissive language is unpersuasive; Toyama frequently uses “may,” but this does not suggest undisclosed configurations. It remains unrebutted that Toyama is designed to repeat only in the hd2 direction, with interconnects and peripheral circuitry on either side in the hd1 direction. POR 34; Yang ¶¶72-73. The existence of multiple-plane devices in the art does not change the fact that the proposed modification would render one or more planes inoperable. *Contra* Reply, 18. Petitioner’s late assertions that interconnects can be placed under, alongside, or above the array (Reply 18, Ex. 1043, ¶54) do not address Toyama’s disclosures of interconnects and circuits already under, alongside, and above the arrays, leaving no room for Petitioner’s new modifications. For example, Toyama at [0251] describes the “upper level metal interconnect structures 208...coupled to the driver circuit

devices” depicted in Figure 17F (above) to the left of the staircase region. And Figures 17A and 17C (below) illustrate the “underlying peripheral device region 700” (orange) to the left and beneath the TAC region (blue), staircase region (yellow), active region (green):

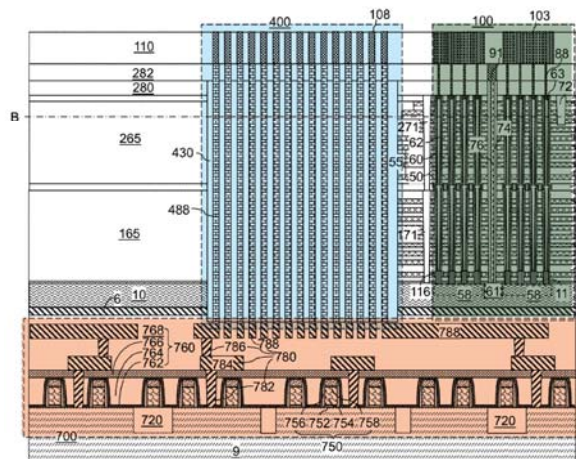


FIG. 17A

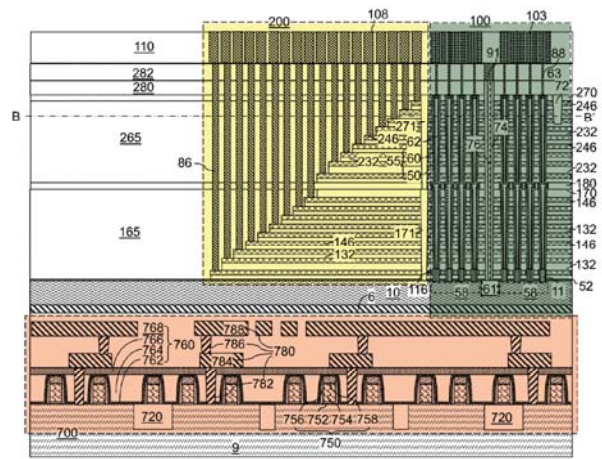


FIG. 17C

See also Toyama, [0164]-[0165] (describing underlying peripheral device region 700).

Dr. Lee’s assertion that “YMTC does not dispute that [using]...multiple planes improves performance” (Ex. 1043, ¶41) is misplaced. As the POR states, “even assuming, *arguendo*, that there are workable ways to introduce multiple planes in Toyama’s device (i.e., layouts other than the one Petitioner has proposed), the Petition does not present any such alternatives.” POR, 36-37. Without such alternatives, Dr. Lee’s claims of a “performance benefit” (Ex. 1043, ¶41) are speculative at best.

In conclusion, Petitioner has not shown that a POSITA would have disregarded Toyama's teachings by duplicating its device in the hd1 direction, as this would create significant interconnect issues. The Board's preliminary opinion was issued without the benefit of the full record, including Dr. Yang's testimony. The Board should revise its preliminary finding and reject Petitioner's modification as non-obvious.

V. GROUND 3: TOYAMA'S SECOND MODIFICATION IN COMBINATION WITH TOYAMA'S FIRST EXEMPLARY STRUCTURE

Petitioner's modification of Toyama's Second Modification based on Toyama's First Exemplary Structure ("Obviousness Combination") fails to disclose or render obvious the Challenged Claims because Petitioner fails to show that a POSITA would have made the hindsight-based modification. In addition, Petitioner's Obviousness Combination does not disclose or render obvious "*a plurality of non-electrically functional channel structures surrounding the TAC region*" as required by claim 8—the sole independent claim.

A. A POSITA Would Not Have Found It Obvious to Modify Toyama's Second Modification in the Proposed Manner

1. Petitioner's Obviousness Combination Would Fail with Respect to Gate Replacement

Toyama teaches using the openings of the alleged TACs of the Second Modification to deposit etchant and conductive material during gate replacement;

however, as explained in the POR, a POSITA would not have been motivated to add the First Exemplary Structure's unitary dielectric fill around these TAC openings, as this would curtail a critical step in forming the memory gates. POR, 40-41.

The Petition overlooked this function and now, in its Reply, Petitioner downplays the issue by claiming that the “backside contact trenches 79” (the alleged slits) would serve the same purpose. Reply, 21. Yet, even if these slit structures were used for gate replacement, large areas would remain inaccessible to etchant and replacement metal, as Dr. Yang explained (Ex. 2004, ¶88, citing Ex. 2007). Petitioner leaves these issues entirely unaddressed.

Petitioner's reliance on Toyama's First Exemplary Structure, which uses “trenches 79” for gate replacement (Reply, 22), is misplaced because this structure lacks the claimed dielectric block within the memory cell array of Toyama's Second Modification, which narrows the etchant and metal deposition flow paths and complicates gate replacement. In the First Exemplary Structure, the dielectric is present only in the staircase region, where the flow path is not restricted, and gate uniformity is less critical. Petitioner's textbook exhibits (Exs. 1013-1014) also do not address dielectric blocks in the array region and are, therefore, not determinative for the same reasons.

Contrary to Petitioner's arguments, *Uber Techs., Inc. v. X One, Inc.* is inapposite—the '806 is not “‘entirely silent on how to’ perform gate replacement

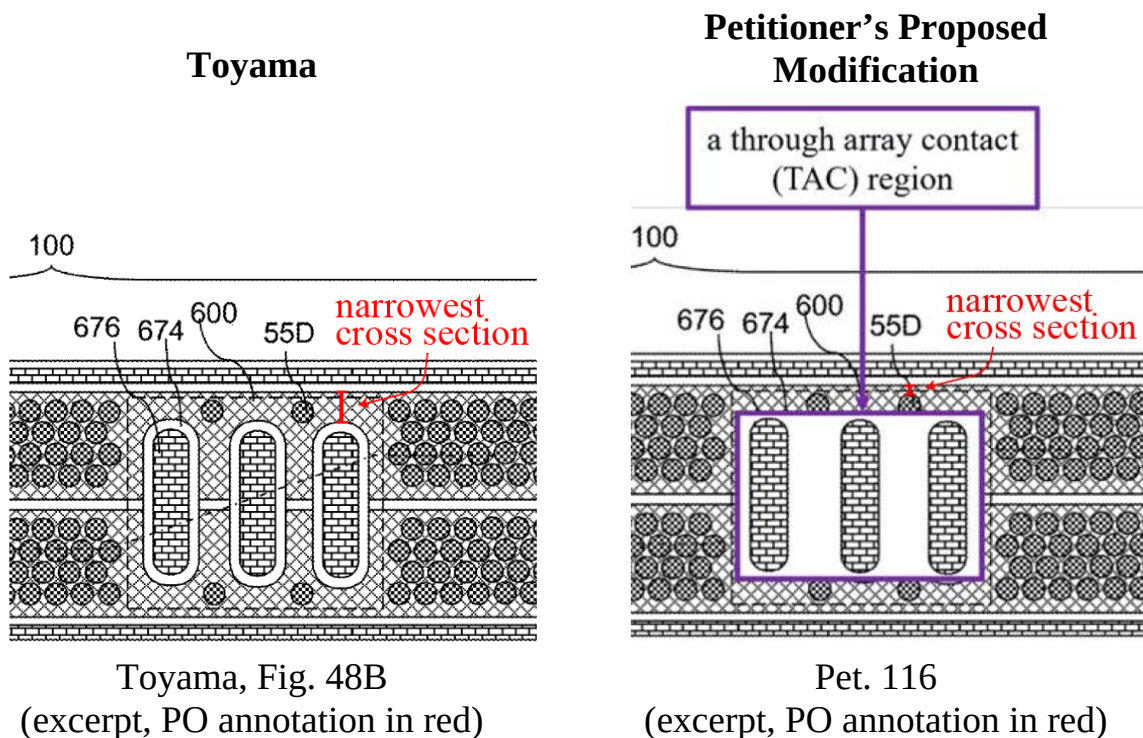
using only slit structure openings.” *Contra* Reply, 22-23 (quoting 957 F.3d 1334, 1339 (Fed. Cir. 2020)). The ’806 describes the process for gate replacement using slit structures (’806, 16:27-34) and specifies the etching process and etchant used (’806, 16:35-46). Furthermore, the ’806 geometry provides more open flow paths than Toyama’s as shown by comparing ’806 Fig. 1A (where the slits do not face dielectric trenches, which would obstruct etchant flow) *with* Toyama Fig. 47B (where trenches 72 run the length of the array and obstruct etchant flow). See Toyama [0198] (explaining trenches 72 are formed in the “sacrificial layer” before gate replacement), [0343] (same).

2. Petitioner’s Obviousness Combination Would Block Current and Render the Device Inoperable

As the Board recognized at institution, “replacing the conductive word lines with insulating material would eliminate the current that controls the memory, resulting in a non-functioning device.” DI, 34. PO has further explained this (POR, 42-46) and Petitioner fails to address these points in its Reply.

Petitioner’s assertion that word-line resistance is not a concern because the lines are “made out of metal” is belied by its own expert. Reply, 23. Dr. Lee testified that “*nonuniform depositions of...metal* wire [can] increase...temperature[, and] cause *[a] local hot spot.*” Ex. 2006, 32:18-33:16 (emphasis added). Here, using metals does not negate the concern regarding resistance, because the layers are very

thin. As Dr. Lee points out, resistance is inversely proportional to the cross-sectional area through which current flows. Ex. 1043, ¶71. Because the gate layers are very thin, the width of the passage (perpendicular to current flow) is critical to the resistance. As shown below, Petitioner's modification drastically decreases the narrowest cross section (width $\times$ thickness) in Toyama's gate layers:

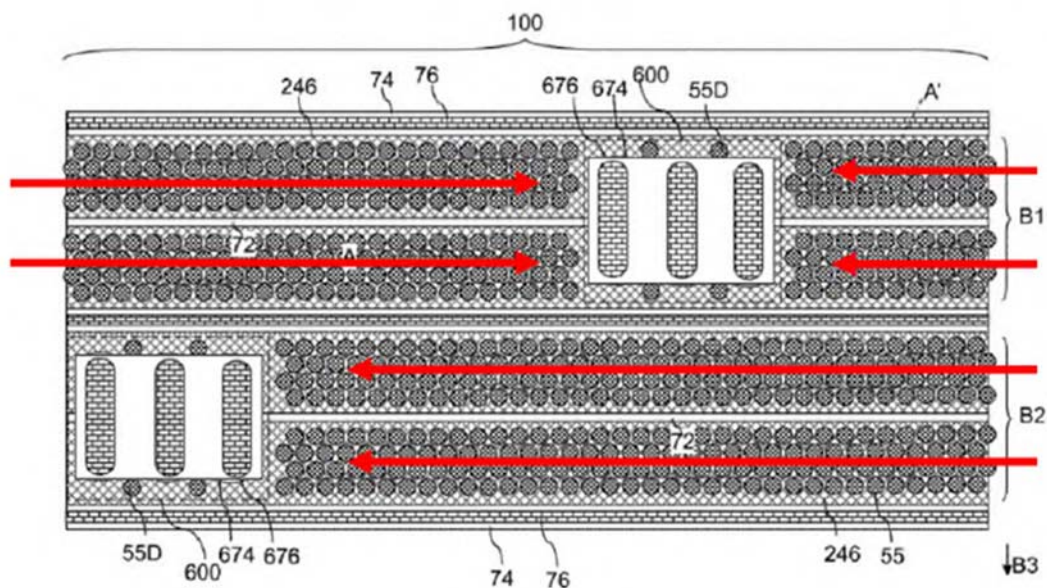


A smaller cross-sectional area at the bottleneck results in increased current density, which, as Dr. Lee admits, causes undesirable hot spots that “degrade” the device. See Ex. 2006, 36:16-37:1, 32:9-10; POR, 43.

Petitioner's new argument based on a different Toyama embodiment (Reply, 24, citing Fig. 39B) is improper, as it introduces new features requiring new analysis.

Regardless, this embodiment's unitary dielectric structure is irrelevant because its gates have a larger cross-section, and the memory array does not use dummy structures 55D.

The Reply's additional argument (illustrated below), that a POSITA would have used staircase contacts on both sides of the array to access the memory cells, is untimely and should be rejected. Even so, such changes would have been undesirable.



Reply, 26 (Petitioner's annotations of Toyama, Fig. 48B). **First**, adding staircases on both sides increases the device size, contrary to Toyama's goal of "decreas[ing]...device size/footprint." Toyama, [0389]. **Second**, the new modification would limit each memory block to one through-memory-level via

region, eliminating critical interconnect capabilities. **Third**, Petitioner does not address the impact adding a second staircase has on peripheral devices and interconnects. Petitioner fails to explain why a POSITA would have been motivated to make these disadvantageous changes.

Petitioner's reliance on *Uber Techs.* again fails. Reply 26 (quoting 957 F.3d at 1339). The '806 teaches how to size the dielectric structure with the help of the isolation structure. See e.g., '806, 10:35-48 (explaining how to size and align "dielectric structure 232"), 14:63-15:36, 21:20-28. And the '806 geometry (discussed above) provides larger current paths. See '806, Fig. 1A. Petitioner disregards these enabling teachings and incorrectly claims PO's arguments are based on the figures drawn to scale (Reply, 27-28). In fact, PO's arguments are based on the '806's teachings of a novel configuration using a dielectric structure, formed to the desired size with the help of an isolation structure. See, e.g., POR, 43-45. Petitioner does address these teachings or identify similar teachings in Toyama, making its assertion that "[a] POSITA would have been able to design the proposed combination" conclusory and unsupported. *Contra* Reply, 27-28.

Lastly, *Intel Corp. v. PACT XPP Schweiz AG* is inapposite. Reply 29 (quoting 61 F.4th 1373, 1380 (Fed. Cir. 2023)). While showing "an 'improvement' in the categorical sense" is not required, Petitioner must show that a unitary dielectric fill material is a "suitable option" for Toyama's Second Modification. See *Commscope*,

Inc. v. Tq Delta, LLC, 2023 WL 7491181, at *9 (P.T.A.B. Nov. 13, 2023) (distinguishing *Intel*, 61 F. 4th at 1381); Pet. 96-108. Petitioner has not done so, and as explained above and in the POR, a dielectric fill material is not a suitable replacement for Toyama's dielectric liner in the array region.

3. Petitioner's Proposed Motivations for the Obviousness Combination are Flawed

For the reasons discussed above and in the POR (POR, 38-49), a POSITA would not have been motivated to make the proposed modification or have had a reasonable expectation of success. Petitioner incorrectly claims that PO's arguments require the Obviousness Combination to be "superior to Toyama's expressly disclosed embodiments" (Reply, 28-29). In fact, Toyama does not disclose the proposed modification, and Petitioner has not identified a viable motivation for a POSITA to have made the proposed changes or addressed the several reasons a POSITA would have lacked a reasonable expectation of success. The purported advantages cited by Petitioner are **not** actual advantages (POR, 46-48). Without a motivation, a POSITA would not have made Petitioner's proposed changes, especially given the disadvantages, such as faulty gate replacement and blocked word line current.

Petitioner’s only alleged benefit to modify Toyama’s Second Modification—lower capacitive coupling—is contradicted by Dr. Lee repeatedly testified that a thin liner offers better electrical performance than a solid dielectric block:

Q. ...[H]ow does a liner have advantages in...electrical performance over dielectric structure?... A. I explained earlier that the—this liner base would provide electrical—better electrical characteristics, including lower parasitic capacitance, more uniform gate control, and better channel coupling.

Ex. 2008, 100:17-101:6, 97:15-100:13; Lee(II), ¶15. Dr. Lee also explained the physical advantages of a liner over a dielectric structure:

[T]his thin liner require[s]...less physical volume than a large, solid dielectric block, so this will leave more room for other important structure such as gate layers in a tightly packed memory array. So because this thin liner take less space and does not intrude significantly into the memory array, they would allow more of the wordlines, that is the gate layer, to remain intact. So this will in turn help to maintain the...gate length...crucial in controlling the current flow and threshold voltage in the memory array.”

Ex. 2008, 97:16-99:21.

Dr. Yang’s un rebutted testimony (Yang ¶92; see Reply 29-30; Lee(II) ¶83) further establishes that Toyama’s Second Modification already minimizes capacitive coupling by “shorten[ing] the signal path” (Toyama, [0377]). Petitioner also misrepresents PO’s position as “ignor[ing]” conductive layers in discussing the length of close proximity. Reply, 30-31. This is not the case, in fact, PO used an exemplary conductive layer to show that capacitive coupling between conductive

layers and the alleged TACs is minimal compared to the much larger capacitive coupling between neighboring conductive layers. POR, 46-48; Ex. 2006, 27:2-6 (Dr. Lee admitting that “when you talk about capacitive coupling between two conductor[s], you can think of it ... as proportional to the overlap area”). Petitioner does not address these arguments.

Finally, Petitioner’s argument that the benefits of Toyama’s Second Modification TAC placement are relevant to the proposed combination fall flat. The POR addresses the trial ground, which is to “*modify Toyama’s Second Modification* to electrically isolate ‘through-memory-level via structures 676’ *with a unitary dielectric fill material*, as taught by Toyama’s first exemplary structure.” Pet. 98, *see also* Pet. 96-108; *contra* Reply 29-31 (citing 61 F. 4th at 1381). The Reply, like the Petition, fails to explain how the benefits of TACs in the memory array region are relevant “modify[ing] Toyama’s Second Modification” when Toyama’s Second Modification already includes TACs in that region.

B. Petitioner’s Obviousness Combination Does Not Disclose or Render Obvious “a Plurality of Non-Electrically Functional Channel Structures Surrounding the TAC Region”

As explained in the POR, Petitioner’s Obviousness Combination neither discloses nor renders obvious “a plurality of non-electrically functional channel structures surrounding the TAC region” (POR, 49-50). Petitioner’s Reply fails in

its attempt to overcome the POR arguments (Reply, 31) for the same reasons in Ground 1 (§III.B).

VI. CONCLUSION

For the reasons above, Petitioner has failed to demonstrate by a preponderance of the evidence that any of the Challenged Claims of the '806 are anticipated or obvious. Accordingly, the Board should uphold the validity of all Challenged Claims.

Dated: June 25, 2025

Respectfully submitted,

By: /James L. Davis, Jr./

James L. Davis, Jr.

Reg. No. 57,325

ROPES & GRAY LLP

525 University Avenue, 8th Floor

Palo Alto, CA 94301

Telephone: +1-650-617-4794

James.L.Davis@ropesgray.com

Andrew T. Radsch

(*pro hac vice* forthcoming)

ROPES & GRAY LLP

525 University Avenue, 8th Floor

Palo Alto, CA 94301

Telephone: +1-650-617-4011

Andrew.Radsch@ropesgray.com

Christopher M. Bonny

Reg. No. 63,307

ROPES & GRAY LLP

525 University Avenue, 8th Floor

Palo Alto, CA 94301

Telephone: +1-650-617-4011
Christopher.Bonny@ropesgray.com

Allen S. Cross
Reg. No. 74,729
ROPES & GRAY LLP
2099 Pennsylvania Avenue, NW
Washington, D.C. 20006-6807
Phone: +1-202-508-4708
Allen.Cross@ropesgray.com

*Attorneys for Patent Owner, Yangtze
Memory Technologies Co. Ltd.*

CERTIFICATE OF WORD COUNT

The undersigned certifies that the foregoing PATENT OWNER'S SUR-REPLY under 37 C.F.R. § 42.23 complies with the type-volume limitation in 37 C.F.R. § 42.24(c). According to the word-processing system's word count, the brief contains 5,497 words, excluding the parts of the brief exempted by 37 C.F.R. § 42.24(c).

Dated: June 25, 2025

Respectfully submitted,

By: /James L. Davis, Jr./
James L. Davis, Jr.
Reg. No. 57,325
ROPES & GRAY LLP

CERTIFICATE OF SERVICE

The undersigned certifies that the foregoing PATENT OWNER'S SUR-REPLY UNDER was served in its entirety by filing through the Patent Trial and Appeal Case Tracking System (P-TACTS), as well as providing a courtesy copy via e-mail to the following attorneys of record for Petitioner listed below:

Lead Counsel	Back-up Counsel
Jeremy Jason Lang Registration No. 73,604 (jjlang@orrick.com) Postal & Hand-Delivery Address: Orrick, Herrington & Sutcliffe LLP 51 West 52nd Street New York, NY 10019 T: 212-506-5000; F: 212-506-5151 P52PTABDocket@orrick.com PTABDocketJL2@orrick.com PTABDocketJ3B3@orrick.com T61PTABDocket@orrick.com PTABDocketP2S7@orrick.com micron-ymtc_ohs@orrick.com	Travis Jensen Registration No. 60,087 (tjensen@orrick.com) K. Patrick Herman Registration No. 75,018 (pherman@orrick.com) Jared Bobrow <i>Pro Hac Vice</i> (jbobrow@orrick.com) Parth Sagdeo Registration No. 71,275 (psagdeo@orrick.com)
<i>Counsel for Petitioner Micron Technology, Inc.</i>	

Dated: June 25, 2025

By: /Jonathan Bradford/
Name: Jonathan Bradford

ROPES & GRAY LLP