

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner,

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,
Patent Owner.

IPR2024-00791 (Patent 10,937,806)
IPR2024-00911 (Patent 10,937,806)

Record of Oral Hearing
Held: September 4, 2025

Before JO-ANNE M. KOKOSKI, KIMBERLY MCGRAW, and
MICHAEL T. CYGAN, *Administrative Patent Judges*.

IPR2024-00791 (Patent 10,937,806)

IPR2024-00911 (Patent 10,937,806)

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IPR2024-00791 (Patent 10,937,806)

IPR2024-00911 (Patent 10,937,806)

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1 P R O C E E D I N G S

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3 JUDGE MCGRAW: Good afternoon, everyone. Welcome back.
4 This is a consolidated oral hearing being held in IPR2024-00791 and
5 IPR2024-00911 involving U.S. Patent Number 10,937,806. I am Judge Kim
6 McGraw. With me are Judges Kokoski and Cygan. For the hearing order,
7 similar to this morning, every party -- each party has 60 minutes total time to
8 argue their case. Petitioner will go first, followed by Patent Owner. Both
9 parties may reserve some rebuttal time. Let's begin with appearances on
10 behalf of Petitioner.

11 MR. SAGDEO: Your Honors, Parth Sagdeo with Orrick,
12 Herrington representing Petitioner Micron Technologies.

13 JUDGE MCGRAW: Thank you. And Patent Owner?

14 MR. RADSCH: Good afternoon, Your Honors. I'm Andrew
15 Radsch with Patent Owner YMTC. With me today arguing this afternoon
16 would be Allen Cross, Ropes & Gray; we have Chris Bonny; and from
17 YMTC, Mr. Weihua Cheng.

18 JUDGE MCGRAW: Thank you. Petitioner, how much rebuttal
19 time would you like to reserve?

20 MR. SAGDEO: Your Honor, we'd like to reserve 20 minutes for
21 rebuttal.

22 JUDGE MCGRAW: You may begin when you're ready.

23 MR. SAGDEO: May it please the Board. The '806 Patent IPRs
24 involve three grounds of unpatentability, each of these grounds renders
25 obvious all challenged claims across both IPRs. Given our limited time
26 today, I'll like to focus on Ground 2, which relates to Toyama's first

1 exemplary structure and, in particular, to a multi-plane implementation of
2 that exemplary structure; although I'll cover the other grounds, as time
3 permits, and I'm happy to answer any of the Board's questions on those
4 grounds. I plan to focus on Ground 2. The Board preliminarily concluded
5 in its Institution decision that the ground renders all challenged claims
6 obvious, and the trial record reinforces that conclusion.

7 Turning now to Slide 8, Ground 2 relates -- involves three issues.
8 The first issue relates to reasonable expectation of success. Patent Owner
9 says that a person of skill would be unable to implement multiple planes of
10 Toyama's first exemplary structure because the peripheral circuitry of those
11 planes would interfere with each other. But Patent Owner's position is a
12 classic and legally flawed bodily incorporation argument.

13 Patent Owner relies on Figure 17F. But the question is not
14 whether Toyama's Figure 17F or even Toyama can be bodily incorporated in
15 the proposed combination but instead what Toyama's disclosure teaches.
16 The recorded evidence here is completely one-sided. Prior art textbooks and
17 patents confirm that multi-plane implementations, just like the proposed
18 combination, were routine in the art.

19 The second issue relates to the preamble's phrase "a device."
20 Patent Owner says that if a memory has two planes, it is no longer "a
21 device," but two devices. But that again is contrary to all record evidence,
22 numerous textbooks, prior art publications, and even in Patent Owner's
23 expert's own patent describe multi-plane memories as a single device.
24 Patent Owner's expert cites zero evidence to the contrary. The final issue in
25 Ground 2 relates to Dependent Claim 10's etch stop plug limitation. Your
26 Honors have already heard argument on that this morning and I don't intend

1 to spend further time on it, unless Your Honors have any specific questions.

2 Turning to Slide 9 and to Ground 2's obviousness theory. The
3 petitions explained that a POSITA would have found it obvious to
4 implement Toyama's first exemplary structure in a three-dimensional
5 memory device with multiple planes. The petition provided a lengthy
6 discussion of reasonable expectation of success in which it explained that
7 multi-plane devices, just like the proposed combination, were well known in
8 the art.

9 The petition cited to textbooks, there's the Aritome textbook,
10 which is in the top figure, that's Exhibit 1014. There's the Micheloni
11 textbooks which also show multi-plane devices side by side and the Shah
12 patent, which further shows multi-plane devices side by side. Now,
13 importantly, these exhibits were in the petition and yet Patent Owner fails to
14 respond to them. These are unrebutted -- this is unrebutted evidence that use
15 of multiple planes for flash memories was routine in the art.

16 The petition also provided a detailed motivation to combine. Dr.
17 Lee explained, supported by textbook evidence, that a person of skill would
18 understand the use of multiple planes to be desirable because it has well-
19 known reliability and performance benefits. For example, if you use
20 multiple planes, you can do read operations in parallel, speeding them up.
21 Patent Owner doesn't dispute these recognized advantages of multi-plane
22 devices.

23 So Patent Owner made the exact same argument it makes here in
24 trial. It made that argument in its preliminary response. And the Board
25 rejected it. The Board preliminarily rejected it. It explained that at least at
26 that stage, the Petitioner had provided sufficient argumentative evidence

1 showing that a person of skill would be able to implement multiple planes
2 with a reasonable expectation of success, noting that NAND devices having
3 multiple planes had existed for many years.

4 And the Board articulated the combination, the proposed
5 combination, in a helpful way. They explained that the implementation of
6 such a structure would have been straightforward as it merely applies a
7 known technique implementing multiple planes of NAND flash memory to a
8 known device, Toyama's first exemplary structure to yield predictable
9 results, a NAND flash device with improved performance. And that was at
10 the '806-1 institution decision, page 29.

11 So Patent Owner's theory relies exclusively on Figure 17F. Now,
12 this was a figure not relied on at all in the petition, yet Patent Owner seizes
13 on it. And the argument, the inoperability argument, is entirely premised on
14 that figure. But Patent Owner's reliance on Figure 17F misses the mark
15 because Petitioner's theory is not limited to that figure. So for example, the
16 petition explained, and so did Dr. Lee, that -- so I'll back up.

17 Toyama's description notes that the layout that it depicts is not
18 mandatory. And so Patent Owner comes back and says, well, the petition
19 talks about Figure 17E. And I guess, Patent Owner's argument is you'd have
20 to use those two figures together. But for one, that's not supported by
21 Toyama. And second, the petition only uses Figure 17 as an example, as an
22 illustrative aid to talk about what the combination is. So for example, Dr.
23 Lee in paragraph 140, this is in the bottom right callout, talks about this use
24 of Figure 17 as an exemplary configuration. The obviousness combination
25 is much broader; it's not limited to Figure 17E.

26 Turning to Slide 14, Patent Owner further ignores -- and this is

1 new evidence in the trial record -- that Toyama expressly contemplates
2 modifications to its embodiments. Toyama describes Figure 17F as an
3 alternative exemplary structure. So it's alternative, meaning that it's
4 alternative to what's described in other of Toyama's figures. And it's
5 exemplary, it's just an example, it's not the entire universe of Toyama's
6 disclosure.

7 And that's confirmed by paragraph 390 in this callout from
8 Toyama. It will occur to those of ordinary skill in the art that various
9 modifications may be made to the disclosed embodiments and that such
10 modifications are intended to be within the scope of the disclosure.

11 So even assuming that Toyama itself were limited to Figure 17F,
12 then it's not, for the reasons I just mentioned, Patent Owner's argument still
13 fails because Patent Owner doesn't rebut that designing multiple planes or it
14 was routine in the art to do so. Patent Owner hasn't rebutted, for example,
15 on the bottom left here, this is Shah, it shows you have two blocks -- sorry,
16 two planes side by side and then on the right-hand side of that you have a
17 peripheral area 604. So this is one example, like the proposed combination
18 where you have two planes side by side and you have room for peripheral
19 circuitry.

20 So now, looking at the bottom right, this is an example from the
21 Micheloni textbook, and this too shows you have two planes side by side
22 and you have peripheral circuitry. So here, for example, it's on the top and
23 the bottom if you're kind of looking at it in a sort of top-down plan view.
24 Again, this is unrebutted evidence going to the routine nature of the
25 proposed combination.

26 JUDGE MCGRAW: How do we know what is shown in these two

1 exhibits is similar to what's in Toyama so that Toyama's teaching could be
2 applied as -- to be extended in hd1 direction as shown in these two exhibits?

3 MR. SAGDEO: So Toyama -- so Dr. Lee provides an explanation
4 of this. He explains that Toyama says you would implement multiple blocks
5 in the hd2 direction. And I'll just go back to figure -- sorry, Slide 13, which
6 sort of illustrates this. The hd2 direction is sort of the up-down direction
7 when you're looking bird's eye. And so Toyama says if you want to increase
8 the capacity of the memory, essentially, you implement multiple blocks in
9 the hd2 direction.

10 But Toyama is silent about repeating things in the hd1 direction.
11 And so Dr. Lee explains that a person of skill would have found it intuitive
12 to repeat multiple planes in the hd1 direction as in the proposed
13 combination. And these exhibits essentially buttress that and show that in
14 the art, people were doing exactly that, they were repeating multiple planes
15 in what Toyama calls the hd1 direction.

16 JUDGE MCGRAW: Well, I think Patent Owner's argument is that
17 because of the interconnects and the peripheral circuitry in Toyama, one of
18 skill in the art would not extend in the hd1 direction. And I know that
19 you've pointed, and Dr. Lee has pointed to other exhibits that show that it
20 was done. But how can I make the leap that what was shown in those prior
21 art references could apply to Toyama?

22 MR. SAGDEO: So there's two points, Your Honor, one is a point
23 about Toyama itself. And as I mentioned, Toyama is not limited to Figure
24 17F, it's just an exemplary -- an alternative exemplary structure. The second
25 thing is that these figures, they show peripheral circuitry. So they tell a
26 skilled artisan, or at least they demonstrate, that it would have been within

1 the skill of a skilled artisan to place peripheral circuitry in somewhere -- in a
2 position different from that expressly disclosed in Toyama.

3 So kind of backing up to the obviousness inquiry here, it's not can
4 we wholesale take Figure 17F and sort of just duplicate it, it's what would a
5 skilled artisan do with these teachings. These figures go to the point that a
6 skilled artisan could say, oh, well, I could put peripheral circuitry on the top
7 or bottom, I could put peripheral circuitry on the side. And that evidence of
8 a skilled artisan's knowledge is unrebutted.

9 And to Your Honor's point about the Figure 17F in Toyama, what
10 Patent Owner is trying to do here is a classic bodily incorporation argument.
11 And this is not the first time that a court has seen an argument exactly like
12 Patent Owner's. In the *Elbrus* case, for example, there was a combination.
13 And based on what the Patent Owner said is, well, you couldn't combine
14 those two things because it would lead to an inoperable circuit or an
15 unworkable circuit.

16 And the Federal Circuit rejected that. It explained that whether
17 you could combine those two circuits and have it work without any sort of
18 other modifications or adjustments, that's basically irrelevant, the question is
19 what a person of skill would do with these teachings. And I think it's telling
20 that although we cited *Elbrus* in our reply, we cited a number of other cases,
21 we cited *Ettder*, we also cited *Orthopedic*, we cited *Pulse*, we cited *Mouttet*.
22 These are all bodily incorporation cases. In fact, the other two, *Pulse* and
23 *Mouttet*, also involved circuitry.

24 And Patent Owner, in their sur-reply fails to discuss, cite, or
25 distinguish any of these cases. I think that's because Patent Owner realizes
26 that that these cases, the facts are materially the same and just as in those

1 cases, the idea that you have to take a prior art disclosure in a fixed sense
2 and totally just without any sort of creativity from a skilled artisan just
3 duplicate it, that's not what the law is, that's not the obviousness inquiry.

4 So Patent Owner says, well, also the evidence that we introduced
5 in reply is untimely, but that lacks merit for several reasons. First, as I
6 mentioned earlier, a lot of that evidence was in the petition. And it was
7 Patent Owner that decided not to respond to that in its POR. And the second
8 point is that what we're doing here -- so this is not a new claim happening.
9 This goes to reasonable expectation of success.

10 And courts have held that a Petitioner is allowed to respond to a
11 Patent Owner's challenge to the petition's reasonable expectation of success
12 argument and the Petitioner may essentially provide new evidence and
13 argument responding to that challenge. Here, the petition had a lengthy
14 reasonable expectation of success argument. It explained, with reference to
15 many of the figures that I've just covered, that the proposed modification
16 would be routine. And so the Petitioner is allowed to rebut the Patent
17 Owner's argument to the contrary.

18 JUDGE MCGRAW: And what is your evidence to support that it
19 would have been routine to repeat in the hd1 direction?

20 MR. SAGDEO: So Your Honor, I'll go back to Slide 15. And so
21 for example, in Exhibit 1024, that's the Shah Patent, we have two planes
22 which are essentially laid out, so it's 640 and 641. Those are repeated in
23 what Toyama would call the hd1 direction sort of a left right direction and
24 then you have a peripheral area on the side.

25 Now, Patent Owner has not argued that Shah is not enabled, Patent
26 Owner has not averred that it was unworkable in some way, this is evidence

1 going to the routineness of the proposed modification. I'll also point to the
2 bottom right, that's the Micheloni textbook. It describes, again, planes in the
3 hd1, the left-right direction. You have peripheral circuitry there, it's
4 accounted for. Again, Patent Owner doesn't contend that this is not enabled
5 -- I mean, this was -- and I'm looking at now the caption for that figure. This
6 is a typical NAND flash floor plan. And typical as of -- I forget if this is
7 2013 or 2016, but typical in the prior art. This is in a textbook.

8 And so these are the examples I have in my demonstratives. But if
9 Your Honors were to look at Dr. Lee's declarations, they have even more
10 examples just like these where you have multiple planes in the hd1 direction.

11 JUDGE MCGRAW: Now, if you could go back to that figure,
12 where are the peripheral circuits in this reference?

13 MR. SAGDEO: Your Honor, in the Shah reference, which is on
14 the left or -- so I know it's kind of a very small print here, but -- so 604
15 which -- let me see if I can actually annotate it here. So 604 is labeled here,
16 and that's the peripheral area. So here, there's the label peripheral area. And
17 if Your Honors were to look at the Shah's disclosure, it explains that that's
18 the area where you could put peripheral circuitry, which is things like sense
19 amplifiers, things that help the flash memory operate. And similarly, in the
20 Micheloni figure, you have peripheral circuitry here and here.

21 JUDGE MCGRAW: So in Toyama, there is peripheral circuitry in
22 between the repeated structures. I understand that you're saying there are
23 other pieces of prior art that have your structures repeated in a plane. But
24 what I'm lacking is an understanding of that they did have peripheral
25 circuitry in between what was repeated. It seems to me Patent Owner's
26 argument is you would not repeat structures when there is peripheral

1 circuitry that would have to be removed.

2 And I understand Petitioner to say yes, you would be able to do it.

3 But what I have not seen is where is it taught how to remove that peripheral
4 circuitry, that would have been obvious to one in skill in the art that you
5 could remove the peripheral circuitry in order to repeat.

6 MR. SAGDEO: Well, Your Honor, I would characterize that
7 slightly different, the modification does not involve removing peripheral
8 circuitry but moving it to a different place potentially. And so we've
9 provided evidence of here all the different places you could move it to. And
10 I think other than that, we have Dr. Lee's testimony that, well, another option
11 is you simply just have more space between these planes. And the
12 peripheral circuitry doesn't extend to infinity, it's got to extend the -- only a
13 certain amount of space and of course, you could just put another plane right
14 next to it.

15 So unless Your Honors have any further questions on the ground to
16 bodily -- or the ground to peripheral circuitry issue, I'd like to move to the
17 device limitation. So although the Patent Owner frames this as an issue with
18 respect to the Limitation 8G in its papers, really, what we're talking about is
19 the preamble. And the preamble recites a 3D -- "a three-dimensional
20 memory device comprising." What Patent Owner says is if you have two
21 planes, you no longer have a device, you have multiple devices. And Patent
22 Owner says now that it doesn't meet the claim.

23 But contrary to Patent Owner's assertion, the petition consistently
24 described the proposed combination as a multi-plane device in the singular.
25 And so for example -- and there's a callout here from the petition at 69, a
26 POSITA would have found it obvious to implement Toyama's first

1 exemplary structure in a three-dimensional memory device with multiple
2 planes.

3 And the Board similarly recognized that this is what the petition's
4 combination was. So the Board said -- and I'm paraphrasing the '806-1
5 institution decision at 27 to 28 -- that the modification was to extend the
6 device in the hd1 region such that a modified device having multiple planes
7 would meet patent limitation.

8 So what we're talking about here is you have one device, and you
9 have multiple planes. So Patent Owner says, well, by nature, I guess every
10 device -- or I should say every memory with multiple planes is no longer one
11 device, it's multiple devices. And the extrinsic evidence here is totally one-
12 sided. It rejects the Patent Owner's contention.

13 So the Micheloni textbook, which is the top callout, talks about a
14 NAND flash storage device, that NAND flash storage device may have
15 multiple chips, each chip has one or more sub-chips or dies, and each sub-
16 chip might have multiple planes. So here, you have device as a larger
17 logical construct and several layers beneath it, you know, in terms of
18 subcomponents, do you have claims? Also in the Aritome textbook, this is
19 the second callout, it talks about a 3D V-NAND flash memory device which
20 consists of two planes. So all of the extrinsic evidence describes or
21 contemplates that you could have a device with multiple planes.

22 Dr. Yang's own patent, which was prior art to this patent. You can
23 see there -- here the figure -- I should say the text talks about -- this is
24 paragraph 38 of Exhibit 1050 -- three devices of SLC NAND flash, and
25 parenthesis, (six planes). And the figure that reflects that text also shows
26 you have three devices, device 1, device 2, device 3; and each device has

1 two planes, P1 and P2. So what does Patent Owner have on the other side?
2 No extrinsic evidence whatsoever, just the say so of its expert that's
3 contradicted by that expert's own patent.

4 Let's turn to the intrinsic evidence. So Dr. Lee explained -- and
5 Patent Owner has not rebutted -- that the specifications definition of three-
6 dimensional memory device is met by a multiplane device. I won't dwell on
7 that definition. But basically, the proposed modification continues to have a
8 vertically-oriented strings of memory cell transistors on a laterally-oriented
9 substrate so that the memory strings extend in the vertical direction with
10 respect to the substrate.

11 Patent Owner fails to identify any disclaimer that would warrant
12 narrowing the word device, which as I've explained the plain meaning
13 clearly contemplates multiple claims. There's no disclaimer that would
14 warrant narrowing it beyond the plain meaning. And although the Patent
15 Owner talks about this benefit of shortening routing, then that's not
16 lexicography, that's not disclaimer.

17 The Patent Owner has provided no basis for that particular benefit
18 to limit the plain meaning of device to a single-plane device. Patent Owner
19 says that, well, if you have -- if you adopt Petitioner's understanding of
20 device, that leads to unreasonable results, such as a server farm or a plane or
21 a ship or a car being a device, but that's not at all what Petitioner is saying.

22 Dr. Lee explained that what we're talking about here is a single
23 device with a common function. So for example, you plug a solid-state
24 drive into a computer, that solid-state drive has multiple planes. And then
25 when the computer executes write operations, executes read operations,
26 they're working -- the planes are working together to fulfill that operation.

1 And so Dr. Lee says, because there is a single flash device that executes
2 unified access operations by coordinating parallel activity across its planes,
3 like that's what makes it a device. Now, we can -- we don't need necessarily
4 to define the broadest limits of a device to know that a multi-plane memory
5 is a device.

6 And I'll close my discussion of this limitation with a legal point,
7 which is, again, going back to my first point about this limitation were in the
8 preamble. And as the Board is well aware that the presumption is that a
9 preamble is not limiting. Patent Owner has identified no basis to make this
10 preamble limiting. And so whether or not a plane -- planes are multiple
11 devices or not, it's actually legally irrelevant, there's no basis to limit it.

12 So Your Honor, unless the Board -- Your Honors, unless the Board
13 has any further questions, I'll just briefly mention that this ground involves
14 the etch stop plug limitation. Your Honor has already heard argument on it
15 this morning, I don't intend to rehash all of those issues. And so I'll skip
16 over the section to Ground 3.

17 So Ground 3 involves a combination of Toyama's first exemplary
18 structure and its second modification. The petitions explained that a person
19 of skill in the art would have found it obvious to form Toyama's second
20 modifications through-memory-level via structures in a unitary material, as
21 in Toyama's first exemplary structure.

22 So instead of the liners, we use a dielectric block. The petitions
23 explained that the proposed combination is just a simple substitution. It's
24 nothing more than the mere substitution of one known element, that's
25 Toyama's "insulating liners 674" for another known in the field, that's the
26 unitary dielectric fill like in Toyama's first exemplary structure with

1 predictable results. You're going to be able to insulate the TACs just as you
2 did with the liners.

3 So to get to now to Patent Owner's gate-replacement inoperability
4 argument to provide a little bit of background. A control gate is a -- is
5 sometimes called a "word line". It's basically a conductive layer that's sort
6 of a plane and it's used to control flash memory devices. We have these
7 vertical strings, and each level of the string is controlled by one control gate.
8 Gate replacement refers to the process of actually creating these control
9 gates.

10 You usually start with what's known as a dielectric sacrificial layer
11 stack and you do basically an etch operation. So you take away those
12 sacrificial layers which are sort of alternating, and then you get -- essentially
13 get a void. And then you replace that void with metal, and now you have
14 your gate layers. So conventionally -- and this is sort of undisputed that in
15 the art -- etchant is applied to slit openings. So the slit structures are labeled
16 here, slit structure 76. Basically, before you fill that in, that's currently
17 metal, but in the manufacturing process, it's - at one point, it's just a sort of
18 trench, it's an opening. And you can basically put -- you can put etchant in
19 that opening, and it sort of dissolves away those sacrificial layers.

20 And so what Patent Owner says is -- so this is Toyama's second
21 modification. And what the proposed combination involves is instead of
22 you having 679, which will eventually become liners, you're going to have a
23 unitary fill. So they say, okay, well, if you get rid of these openings, 679,
24 you can't do gate replacement anymore, and so you can't make your device.

25 But the Petitioner has shown that a POSITA would still be able to
26 use these backside contact -- contact trenches, 79, which are still going to

1 be in the device in the proposed modification. And you just use those for
2 gate replacement. So Patent Owner's arguments are contradicted by Toyama
3 itself. So Toyama's -- both of Toyama's -- sorry, I should say, yeah, both of
4 Toyama's -- both of the embodiments on which the proposed combination is
5 based, the first embodiment and the second modification, those use backside
6 contact trenches 79. We pointed that out in our reply.

7 And then Patent Owner says, well, you couldn't just use 79 because
8 -- I guess they contend that that wouldn't work because you have a dielectric
9 block now in the memory array. But Toyama discloses embodiments that do
10 just that. So for example, Patent Owner -- so let's see this, so I'm flipping
11 out and looking at Figure 36B. So this is an embodiment in Toyama, which
12 has a dielectric block in the memory array, just like the proposed
13 combination. And they're labeled with that green arrow. And you still are
14 able to do gate replacement using trenches 79. So Patent Owner hasn't said
15 that Toyama is not enabled. In fact, the presumption is that Toyama is
16 enabled. And so Toyama has an enabled embodiment that does just what the
17 proposed combination does.

18 So Patent Owner, I guess, in response to this, says that the '806
19 Patent has "more open flow paths," whatever that means, than Toyama. But
20 what Patent Owner is doing is the classic and legally flawed approach of
21 comparing the scale of figures. If the '806 Patent shows a different sort of
22 aspect ratio than Toyama's figures, that's legally irrelevant. It's irrelevant
23 because both Toyama and the '806 Patent say that their figures are not to
24 scale. And of course, the legal presumption is that they're not to scale.

25 So at bottom what we have here is a teaching away argument or
26 reasonable expectation of success argument. But there's no teaching in

1 Toyama or anywhere else that Patent Owner has identified that would
2 criticize, discredit, or otherwise discourage the solution claimed. In fact, in
3 the prior art, Dr. Lee cites many examples of prior art that exclusively use
4 slit structures, as in the proposed combination for gate replacement. Toyama
5 itself has examples where you have a dielectric block within the memory
6 array and you're using slit structures for gate replacement.

7 And so it's just a matter of design optimization. It's the sort of
8 routine capability within a -- within the ability of a skilled artisan. So maybe
9 you might adjust, for example, the sizing and the spacing of the trenches in
10 order to make sure it works. But this is something that people had been
11 doing long before the '806 Patent, that's not disputed. And it's just a matter
12 of a POSITA applying routine sort of design decisions to make sure that the
13 embodiment works as intended.

14 JUDGE MCGRAW: To address that point, in order for there -- to
15 just be a routine optimization, doesn't there have to be kind of an even
16 substitution between what was in the prior art and what you're seeking to
17 change? So for example, if you go to Slide 45, here, you say you're just
18 substituting the opening 679 for the entire dielectric trench. But what about
19 all of the other material that is within that area, the word lines and the
20 conductive layers?

21 MR. SAGDEO: Right. So what this would look like is sort of like
22 the first exemplary structure where you -- instead of having those individual
23 openings, you would have a single opening and that would eventually be
24 filled with a dielectric material. And so that part of the device, which is
25 labeled in this figure as 600, there's some changes there.

26 But when we're talking about gate replacement, what we still have

1 -- and I'm now looking in the region 100, we still have those backside
2 contact trenches, 79. So Toyama's first exemplary structure exclusively uses
3 trenches 79 for gate replacement. I pointed to other embodiments within
4 Toyama, and this is -- I believe this is the fourth exemplary structure, not the
5 second modification to the fourth exemplary but it's just the original fourth
6 exemplary structure, which -- also, this has -- so this has a dielectric block
7 within the memory array.

8 And then you see 79, there's three of them sort of horizontally.

9 And there too, you have a gate replacement operation that happens just like
10 in the proposed combination where you use those trenches 79 as access
11 points. You put the etchant in there, it dissolves the sacrificial gates, and
12 then you can replace them with metal gates.

13 So I should also note that the '806 Patent is exactly this -- it doesn't
14 provide any new teachings in the art in this respect. So the '806 Patent, just
15 like the proposed combination, just like Toyama uses these slit structure
16 openings for gate replacement. So Patent Owner's credibility is sort of like,
17 well, you know, Toyama -- if to whatever extent Toyama has this alleged
18 problem, well, the '806 Patent would as well. So there's nothing in the '806
19 Patent that sort of teaches some unexpected way to do this gate replacement,
20 they just say do it.

21 And we've cited the *Uber* case, which stands for this proposition
22 where the '806 Patent's silence on how to do this gate replacement. They
23 just have a few sentences, suggests that a person of ordinary skill in the art
24 would be more than capable of doing so.

25 JUDGE MCGRAW: If you could go to Slide 43, please. Here,
26 Petitioner is arguing that it's a simple substitution of the insulating liners for

1 the dielectric fill portion. But isn't it true that you're actually substituting
2 more than just the dielectric fill material 430 for the insulating liners?

3 MR. SAGDEO: I don't think so, Your Honor. And I'll turn now to
4 Slide 45 to try to illustrate why. What we're talking about with this
5 proposed substitution is really confined to region 600. So, what we're saying
6 is in this region, instead of having three liners, you're going to have a
7 dielectric block, you first make a big opening and you fill it with dielectric.
8 We're not doing anything to change trenches 79, those stay. And so those
9 trenches which were already in the second modification and in the first
10 example structure, both of the sort of base embodiments for this
11 combination, that remains unchanged.

12 And the Petitioner's point with respect to this reasonable
13 expectation of success argument is you could use 79 to do a gate
14 replacement. And, you know, all the evidence we cite, the extrinsic
15 evidence, Toyama itself, different embodiments, all go to the point that this
16 unchanged trenches 79 may be used for gate replacement.

17 So unless the Board has any further questions on the gate
18 replacement issue in Ground 3, I'd like to move on to current-elimination.
19 So this is Patent Owner's argument that if we have a big dielectric block in
20 the memory array, now that's going to restrict the current, you wouldn't have
21 a working device anymore. And that argument is entirely without merit.

22 So Dr. Lee explained, basically, it's a matter of design optimization
23 again. And so for example, there are other embodiments in Toyama, that
24 sentence in reply that do exactly what the Patent Owner says is impossible,
25 which is to have a dielectric block in the memory array, I'm looking at
26 Figure 39 of Toyama. And so again, this is presumed to be enabled.

1 Patent Owner has not argued that it's not enabled. And so Toyama
2 itself, it's teaching say, well, yeah, sure, you can put a dielectric block in the
3 memory array. It's just a matter of, as Dr. Lee explains, it's sizing all the
4 relevant components so that it works. So the '806 Patent itself also
5 contradicts Patent Owner's current-elimination argument. The '806 Patent
6 has fundamentally the same structure as the proposed combination, so I'll
7 sort of try to illustrate that with scenarios.

8 So the '806 Patent has this dielectric block in the middle, that's
9 120. And all around it are -- is actually the gate layer. And so what happens
10 when current is traveling, it has to go around that dielectric block. It can't go
11 through it. And so you have current coming in like this, it would have to go
12 and essentially turn up and go past the dielectric structure. It can't go
13 through; it has to kind of go around it. And so the exact, like, flaw that
14 Patent Owner is allegedly pointing to in Toyama, it's the exact same
15 structure in the '806 Patent.

16 And so this gets us back up -- gets us back to the *Uber* case, which
17 says if the patent -- the challenged patent is not telling you some new way of
18 doing, you know, if the challenged patent had the same alleged problem as
19 the prior art and it doesn't tell you, like, some novel way of solving that
20 problem, well, then it suggests that a person of skill was more than capable
21 of sizing the relevant components to make the device work.

22 So I'll skip over sort of some of the other arguments with respect to
23 this issue and just to note briefly the surrounding limitation. So the petition
24 explained that Toyama discloses a plurality of non-electrically functional
25 channel structures. There's no dispute that these are, you know, dummy
26 structures 55D in Toyama. There's no dispute that they are non-electrically

1 functional channel structures, the dispute is about the word "surrounding."

2 And so Figure 48B here, it shows them on the top and the bottom.

3 But the petition also pointed to language in the specification saying that

4 -- there's language saying that these structures are on the periphery. And it's

5 right here on Slide 62, they're on the periphery of the through-memory-level

6 region. And Dr. Lee explained that a person of skill would understand that

7 periphery here means they encircle the memory-level via regions 600, they

8 go all around.

9 Now, I just want to make a point about timing here, which is that

10 we made all these arguments in the petition. We also, by the way, made an

11 obviousness argument in the petition saying that a person of skill would

12 have found it obvious in light of the well-known benefit of these dummy

13 structures 55D to put them all around. And the Patent Owner in the POR did

14 not respond to those arguments. They only responded to the figure, but not

15 to the obviousness argument, not to the periphery language.

16 And I think that's important because now, in sur-reply, Patent

17 Owner says, oh well, these disclosures are not sufficient. But even aside

18 from the merits, this is an untimely argument. The Patent Owner can't just

19 withhold its argument after it being in the petition and put it and argue it for

20 the first time in its sur-reply. We explained in our reply that Patent Owner

21 didn't respond to these arguments. And now, the Patent Owner is using the

22 sur-reply as sort of a way to, I guess, respond to it in a timely way.

23 So unless the Board has any questions, I'm happy to reserve my

24 remaining time for rebuttal.

25 JUDGE MCGRAW: I could just ask, on Slide 60 Figure 48B, are

26 the dummy structures located on the periphery?

1 MR. SAGDEO: They are not shown on the periphery because
2 they're only shown on two sides. And so, you know, this is not a figure
3 that's not scaled, these figures are just for illustrative purposes. It's really the
4 detailed description that talks about the periphery language and clarifies that
5 you could also -- Toyama contemplates also putting it on the periphery that
6 is on all sides.

7 JUDGE MCGRAW: Okay. Thank you. How much time would
8 you like to reserve for rebuttal?

9 MR. RADSCH: We'd like to reserve 15 minutes, Your Honor.
10 Before I begin, if I could just address one brief procedural matter. The
11 parties both jointly requested that the transcript from one of these
12 consolidated proceedings be entered into the other, like, we would -- went to
13 that request. We were just wondering if there's any other procedural steps
14 you need us to take post-hearing to effectuate that?

15 JUDGE MCGRAW: No, there isn't. When we enter the
16 transcripts for these two proceedings, they will be entered in both
17 proceedings.

18 MR. RADSCH: Thank you, Your Honor. Good afternoon, may it
19 please the Board. I will begin this afternoon with addressing the claims
20 instruction issues, just one of them. And then I will turn to Ground 2. My
21 colleague, Mr. Cross, will address Ground 1, which is Toyama's second
22 modification; and with time permitting, Ground 3.

23 Just very briefly on the claim construction issue with respect to the
24 '806 Patent, there is a similar limitation as found in '378 Patent that we
25 discussed this morning, namely a plurality of through array contacts
26 extending vertically through the dielectric structure that's shown on Slide 8.

1 We go back to the claim language. The antecedent basis for the structure is
2 shown -- or the dielectric structure is shown in Element 8B, it's a dielectric
3 structure.

4 So we're back to the same *Finjan* issue that we discussed this
5 morning, namely, when there's a recitation later in the claim of the structure
6 that refers back to a previously recited a dielectric structure which is
7 antecedent basis, this *Finjan* tells us you need at least one such structure that
8 meets all limitations of the claim. I think there are very three important
9 pieces from -- or aspects of *Finjan* to refer to. One, *Finjan* discusses the
10 early *Salazar* case and states -- this is the *Finjan* report writing.

11 For example, in *Salazar*, we agreed with the district court that
12 while the claimed term "a microprocessor" does not require there would be
13 only one microprocessor, the subsequent limitations referring back to said
14 microprocessor require that at least one microprocessor be capable of
15 performing each of the claimed functions. There must be at least one, there
16 can certainly be more than one that performs each of the claimed functions,
17 but at least one of them must perform each of the claim functions.

18 I think it's telling as well that the Patent -- the Petitioner has relied
19 exclusively on *Baldwin* and its arguments because the *Finjan* works -- it
20 discusses *Baldwin* and distinguishes it. *Baldwin* dealt only with the general
21 proposition of whether "a" means "one or more." And as the *Finjan* court
22 stated in referring to *Baldwin* says, that is a separate issue from whether the
23 claims require the same component to perform multiple functions or satisfy
24 multiple limitations of a claim, which is the issue we're discussing here.

25 JUDGE MCGRAW: But the language in this case, as opposed to
26 the case that we discussed this morning, is the claim language here recites a

1 plurality of through array contracts -- contacts extending through the
2 dielectric structure. So this claim requires a plurality of TACs to go through
3 a structure. How can you read that language as permitting a single TAC to
4 go through a single dielectric structure?

5 MR. RADSCH: I don't think there's any conceivable way one
6 could do that in this claim. Let me move on then, Your Honors, to the
7 substantive issues with respect to Ground 2, which is Toyama's first
8 exemplary structure. I'm now on Patent Owner Slide number 26. So what
9 we show here on Slide 26 is Figure 2 of the '806 Patent.

10 And again, the issue here, the claim limitation at issue is
11 requirement that there be a TAC region formed between the first and second
12 channel regions. And as exemplified in Figure 2, we see here in green, a
13 dielectric structure that also coincides with the TAC region surrounded on
14 the left by a first channel region, on the right by a second channel region that
15 have been dotted in pink.

16 What's important here is you'll see that this dielectric structure in
17 the TAC region within it is placed in the array because it bisects the array.
18 You have the first channel region on one side, the second channel region on
19 the other side, that's how you accomplish what's claimed. You have that
20 element there in the middle of the memory array. You have the first and
21 second channel regions of that memory device on either side.

22 '806 Patent explains what the benefit of that is and that's also
23 shown on Slide 26. This is at column 11, lines 8 to 10. It says, "TACS 234
24 can carry electrical signals from and/or to 3D memory device 200, such as
25 part of the power bus, with shortened -- or shorten interconnect routing." So
26 by placing those TACs there in the TAC region in the middle of the array,

1 such that there's a first and second channel region on each side, you shorten
2 the interconnect routing, which has performance benefits.

3 Let's turn now to the Toyama reference and what the Petitioner is
4 relying upon. On Slide 27, we have Figure 17E from Toyama. So unlike
5 the '806 Patent, what we see here in Toyama -- and this is the figure that
6 they're relying upon -- is that the purported TAC region, which is colored in
7 green, is outside of the array. It is where the staircase structures are formed
8 on the left or the right of the array. It's an entirely different configuration,
9 the result of which is that there is no first channel on one side and second
10 channel on the other side. The alleged TAC region is not formed between
11 first and second channel region because it's an entirely different approach.
12 We see that as well on Slide 28.

13 On Slide 28 of Patent Owner's demonstratives, you'll see what the
14 -- colored in green is the dielectric fill material portion 430 which is their
15 alleged TAC region. You'll see that in front of that staircase region or
16 somewhat bisecting the staircase region on the left of where the channel
17 structures are. Again, this is a different approach and doesn't provide the
18 benefits of those shortened interconnect routings with those performance
19 benefits. And as a result of the different approach you do not meet the claim
20 limitation of having a TAC region between first and second channel regions.

21 JUDGE CYGAN: So when you say that the benefit is a shortened
22 interconnect, the distance is shortened compared to what?

23 MR. RADSCH: To the elements of -- to the -- interconnects to the
24 different channel structures.

25 JUDGE CYGAN: So this --

26 MR. RADSCH: Within the memory array -- to -- each side of the

1 memory array, I would say.

2 JUDGE CYGAN: Right. It's creating vertical connects. It's the
3 verticality that's making the connection shorter, correct?

4 MR. RADSCH: Correct.

5 JUDGE CYGAN: As opposed to winding its way into the
6 (INDISCERNIBLE).

7 MR. RADSCH: Correct. So I would like to then turn to what the
8 petition ground is. And I wrote down a couple of comments from
9 Petitioner's Counsel because as I understand their argument today, it frankly
10 deviates significantly from what the petition ground is. As we know, the
11 petition governs the proceeding, and so it's important to understand what
12 their specific proposal is for the ground.

13 And I'm now here on the petition. This is Petitioner's petition at
14 page 74. They assert that a POSITA would have found it obvious to
15 implement Toyama's first exemplary structure in a 3D memory device with
16 multiple planes. Thus, a POSITA would have found it obvious to repeat the
17 layout shown in Figure 17E in the hd1 and hd2 directions as shown in the
18 modified figure below. So that's the petition ground. It's not generally
19 applying a multi-plane configuration to some teaching of Toyama.

20 The specific ground proposed is repeating the layout of 17E, the
21 hd1 and hd2 directions. There's no question about that is the specific
22 ground. And so when Counsel talked about 17E as being exemplary, it may
23 be exemplary in the context of Toyama, it's not exemplary in the context of
24 what the petition ground is. The ground is replicating exactly 17E in two
25 directions. This is perfectly clear from its expert as well.

26 I now turn to Petitioner's Exhibit 1043, which is the reply

1 declaration of Dr. Lee. He discusses the proposed modification. And as he
2 describes it, each individual plane is fabricated in exactly the same way as a
3 Toyama's first exemplary structure, resulting in vertically-oriented strings of
4 memory cell transistors, and it goes on.

5 This is not a case where we have improperly argued for bodily
6 incorporation. In fact, the bodily incorporation cases they talk about is
7 incorporating a second reference into a first reference. All we are doing is
8 responding to their specific petition ground, which is to exactly replicate the
9 Figure of 17E, that specific exemplary embodiment in the hd1 and hd2
10 declaration.

11 And to pile on, this is what I'm now at showing Exhibit 1003,
12 Petitioner's Exhibit 1003, which is the opening declaration of their expert,
13 Dr. Lee. He states, although Toyama does not expressly disclose repeating
14 the Figure 17E layout in the hd1, which is the horizontal left-right direction,
15 a POSITA would have found -- would have been motivated to do so. So
16 again, we are talking about modifying Toyama by repeating 17E in two
17 directions. That is the ground.

18 Now, Counsel also stated that -- and I wrote this down -- Figure
19 17F of Toyama is not relied on at all in the petition. I think that was a very
20 important concession. I think it dooms the ground. The reason for that is
21 17E and 17F are the same embodiment, they're just different perspectives of
22 the same layout. So let me turn now to exhibit 1005, which is Toyama. As
23 Toyama states, Figures 17E and 17F are top-down views of an alternative
24 exemplary structure according to the first embodiment of the present
25 disclosure. It's the same structure, the same embodiment, just different
26 perspectives.

1 They've conceded that they do not address 17F in the order of the
2 petition. They do not rely upon it. They ignore it. That's a shortcoming
3 because they cannot show -- it failed to show how one would replicate 17E
4 in a manner that is workable and allows it to continue to function. So that's
5 a significant shortcoming in their proofs. And again, 17F is not simply
6 exemplary, it is the same structure as shown in 17E. So when they rely upon
7 17E replicating 17E for their ground, they necessarily have to take account
8 of 17F, it's the same structure. And they have failed to do so.

9 JUDGE CYGAN: Counselor, is part of your argument with the
10 17E replication that Petitioner would cut off the circuitry area on the sides,
11 that they're only repeating the structure up to the staircase, they're not
12 accounting for the interconnects and peripheral circuitry?

13 MR. RADSCH: Well, it is that. You know they are -- the
14 configuration does not allow even for the placement of the interconnect
15 circuitry and peripheral circuitry that extends to the left and the right of each
16 of these blocks. So let me go back to petition here. This is the proposed
17 modification, these four blocks side to side, right, and on end.

18 I'm going to turn now to Patent Owner's demonstrative. What
19 we've done here on Slide 31 is shown on the top, that's their proposed
20 modification. On the bottom is Figure 17F, that shows the interconnects and
21 peripheral circuitry that extends to the left but also to the right of each of the
22 middle channel structures, recall the channel structure is at 100 region in the
23 middle. And there's the peripheral circuitry that extends beyond the left
24 hand and right-hand side of the 17E aspect ratio. In their mapping, there is
25 simply, A, no place for those interconnects or peripheral circuitry, nor did
26 they address as they concede, since they did not address 17F at all, what one

1 would do with those interconnects in their peripheral circuitry.

2 And so the question isn't, generally, was it known in the art how to
3 create a multi-plane device or a multi-plane 3D device? Because that's not
4 their ground. The question is, would a person of ordinary skill in the art
5 been motivated to replicate in a specific way, as their expert says, to exactly
6 duplicate these structures in this manner. And the answer is clearly not
7 because you have this jumble of intersecting interconnects nowhere to put
8 peripheral circuitry. And that's now -- we're addressing the petition or Dr.
9 Lee's declaration of where you put those elements. So --

10 JUDGE CYGAN: So your argument is it's not enough even if one
11 of ordinary skill in the art would have understand -- would have understood
12 how to account for the interconnects and peripheral circuitry. It's just that
13 the way Petitioner has arranged it, Petitioner is essentially saying, our
14 combination eliminates those because we're not showing those in our
15 duplications.

16 MR. RADSCH: I think it's both that, it eliminates them and they
17 want to argue, well, you put them somewhere else. They did not describe
18 that in their petition, where you put those. In fact, it conceded that. He said,
19 nowhere in the petition is 17F had been discussed or referred to or relied
20 upon. So that's just not even addressed. But we can see from their mapping
21 that there's simply -- leaves no room for them.

22 JUDGE CYGAN: Would it also be a problem for their
23 obviousness case if they had the interconnects in there and they repeated
24 -- essentially, 17E interconnects sort of and they had included, let's say, 17F,
25 is that a further problem or is it -- or is that just sort of beyond the scope of
26 your argument?

1 MR. RADSCH: Well, so they've not made that argument. So I
2 guess I'm sort of -- I guess shooting at a hypothetical in a way. I think it'd
3 still be a problem. And I think frankly, it reinforces the other argument that
4 you wind up with multiple distinct memory devices, like each with all of its
5 own circuitry, driver circuitry, its own interconnects. They're not
6 communicating, you know, with each other to work as one unit, they're these
7 separate units.

8 And so just like the issue with respect to what we're just discussing
9 it's not about was it generally known how to add multi-planes to a device—
10 the question specifically here is, as a proposed combination, would it have
11 been obvious to a person of ordinary skill in the art being motivated to
12 exactly replicate those blocks as shown?

13 The question of whether you can have a multi-plane device is not
14 the question presented. The question presented is when you have the
15 specific configuration, is there a ground? Are those separate planes
16 collectively a device? But they're not, they're each operating independently,
17 they function independently with their own circuitry.

18 And so that specific case of this specific ground, those are not just
19 individual planes, they're individual memory devices that function and
20 operate and are driven independently. And so whether a person of ordinary
21 skill in the art would have known how to do so as a general proposition
22 simply doesn't answer the ground, which is this precise replication of
23 elements.

24 Dr. Yang is -- Petitioner -- Patent Owner's Slide 32 explains of this
25 -- explains these issues with respect to how this would result in multiple
26 distinct devices, that is if you take these -- you exactly replicate as which is

1 their proposal and you in fact leave room for that circuitry to in fact be
2 included somewhere which they don't explain, you end up with these
3 multiple individual devices.

4 I want to turn then -- before we turn -- the next issue to their
5 argument that the claim language that -- a device is non-limiting.

6 JUDGE CYGAN: Counselor, can I ask you one further question
7 before you go there?

8 MR. RADSCH: Yes.

9 JUDGE CYGAN: Why in Toyama would it be acceptable to
10 duplicate in the hd2 direction and still have a single device but not in the hd1
11 direction, or are you also contending that as soon as you duplicate in the hd2
12 direction it would be separate devices?

13 MR. RADSCH: So just -- I think there are two parts to that
14 answer, to answer the question. Let me just start with Figure 17E, which is
15 like the building block that they rely upon. This shows blocks -- these
16 blocks one and two. And then if you go to the next figure, which is Figure
17 17F, it shows how there -- these can -- these blocks can be repeated, these
18 blocks can be repeated in the hd1, or these blocks can be repeated, sorry, in
19 the hd2 direction. And that makes sense because of where the circuitry is
20 placed. And they're -- you can see they're cooperating and interconnected
21 together, right? They're going to be attached to the same peripheral
22 circuitry, driven together, cooperate together.

23 Under the mapping that they have proposed that configuration is
24 either -- neither shown or addressed but would not occur. You have
25 attempted a completely separate independently structured and controlled and
26 operating, functioning unit of these memory cells that are a separate device.

1 So to answer your question specifically, you can have this replication in the
2 hd2 direction and have one device. But of course, if they're not cooperating
3 as a device, if they're separately operating, separately driven, separately
4 functioning, then they could still be also separate devices, the hd2 direction.
5 So it does matter on the implementation.

6 JUDGE CYGAN: So you're characterizing "device" as
7 components which act for a single purpose then, I suppose.

8 MR. RADSCH: They can -- they have to function together as
9 memory device. And I don't think it's fair to call an automobile which has
10 many different, you know, memory devices and many other components in
11 memory device. It certainly has that. It has a lot more. What we're talking
12 about here is a 3D memory device with these specific structures.

13 And I go back, really, you know, to the purpose of the '806 Patent's
14 invention, okay, which is this dielectric structure in the array portion that
15 bisects the first and second channel regions to provide these shortened
16 interconnect routings. And so it's describing when it says it's between first
17 and second channel regions, not just taking, you know, three chips and
18 putting one chip on the left, one chip on the right, another chip in the middle.

19 And therefore, you have some, you know, TAC region from one
20 chip in between a channel region, another chip in between some other
21 channel region, another chip -- which is how I think they would essentially
22 read the claim is that there's -- doesn't matter where you find limitations as
23 long as you find them somewhere. These need to be in a memory device.
24 And this notion that the limitation -- sorry, the preamble is not limiting.

25 I think their arguments, really, highlight why it is, right? Their
26 arguments would be you can find these elements anywhere, therefore, you

1 have the device, even if they're on different structures, different planes,
2 different devices, as long as it can find the structure A and structure B
3 somewhere, I have what's claimed. But that's clearly not what is claimed.
4 What's claimed is a memory device comprising these specific features and
5 functions without the context of it being a memory device.

6 I suppose one would argue, as they have, that you just find an
7 interconnect somewhere, you know, a dielectric stacked in another place and
8 you put that all together in a big wafer, for example. And I don't think that's
9 a fair reading of the claim, particularly in view of the specification and the
10 purpose of the invention.

11 JUDGE MCGRAW: What is the difference between a memory
12 device and a memory array?

13 MR. RADSCH: Well, the array is the -- well, I would -- in this
14 context, array is referring to the portion where, you know, the memory
15 -- where the storage of information, right, which is in the middle, not on the
16 staircase; so basically, I would say the middle of the stack, as it were, in the
17 lateral direction. The device is going to include the array. It's going to
18 include "more" as well.

19 So just to really, I think, summarize on those points, right, the
20 Figure 2 is important because it shows how you have a TAC region with
21 channels -- with channel regions on either side. This accomplishes the
22 purpose of the invention. What we have in Toyama is the complete opposite
23 arrangement, and so they have to stretch to repeat 17E.

24 What we hear from Counsel today is that 17E is exemplary, while
25 true of Toyama generally, it's not exemplary of the petitioned grounds. It is
26 the petition ground. It's replicating 17E exactly. You would not do that.

1 Once you do that, you run into a host of problems that are not addressed.

2 They do not reach the claims and do not render them obvious.

3 Unless there are any other further questions on that issue, I'll cede
4 the rest of my time to Mr. Cross. Because I think the only remaining issue
5 for Ground 2 is amply covered this morning, so I don't believe there's a need
6 to address it again this afternoon.

7 MR. CROSS: All right. Good afternoon, Your Honors. I'll be
8 addressing primarily Ground 3, as Petitioner did. And time permitting, I will
9 touch upon some of the issues regarding Ground 1. So turning to Slide 14 of
10 Patent Owner's demonstratives -- oh, sorry, turning to Slide, I think, 35, to
11 go to Ground 3 of Patent Owner's demonstratives, it's important to revisit the
12 trial ground as it was set forth in the petition. And in fact, that's best done
13 by going to Slide 43 of Petitioner's demonstratives. And here, we can see
14 that this explains the proposed combination. And specifically, it says the
15 obviousness combination here is nothing more than the mere substitution of
16 one element.

17 The second modifications insulating liner 674 or another known in
18 the field, that is the dielectric fill material portion 430 of the first exemplary
19 structures. So that's the ground. This is the same language where this is the
20 language that's taken from the petition at -- and this is the '911 petition page
21 105. What's important here is if we go to the preceding page, at the top, it
22 says that the below figure, which is modified version of Figure 49 illustrates
23 the obviousness combination of Toyama's second modification and its first
24 exemplary structure.

25 Similarly, at the bottom, it says a modified version Figure 48B
26 below illustrates the top view of the obviousness combination. So any

1 argument that bodily -- that we're making bodily incorporation arguments
2 fails as we are addressing precisely the trial grounds that are set forth in the
3 petition.

4 The problem here is that -- and going back to Patent Owner's
5 demonstratives -- is that in Patent Owner's response, we presented and set
6 forth at least two critical problems with the proposed modification that
7 Petitioner failed to consider in its petition when substituting the insulating
8 liner 674 for the dielectric fill material portion 430 as it was illustrated in the
9 petition.

10 And in reply, Petitioner repeatedly attempts to cure these problems
11 by proposing new and significant modifications, thus departing from the
12 petition's ground of doing nothing more than a mere substitution of one
13 element for another. So for example, the first such problem that Patent
14 Owner identified and Petitioner failed to address in the petition is the fact
15 that the proposed modification eliminates the sources for gate -- eliminates
16 critical sources for the gate replacement etchant and conductive materials.

17 So we can see in Figure 46A on the left, this is the unmodified
18 Toyama figure. There are through-memory-level openings 679 that are
19 formed during the process and it's through these openings that Toyama
20 discloses forming the gate replacement process. Because it provides the
21 paths for introduction of etchants and conductive material on -- and whereas
22 in Petitioner's modified figure on the right, we see that the dielectric fill
23 material is first added and thus, when you're forming the through-memory-
24 level via structures, you no longer have these additional paths.

25 So that's the issue that Patent Owner identified Petitioner had
26 failed to address in its petition. But on -- in its reply -- and this is going to

1 Slide 40, in its reply, Petitioner argues that the trenches 79 would be
2 sufficient for gate replacement in Toyama's second modification. However,
3 their evidence for this are entirely different embodiments of Toyama's that
4 have different structures and lack key claimed elements.

5 Specifically, neither of Figures 39B or 69B, which Petitioner
6 points to support its arguments that the trenches 79 are sufficient for gate
7 replacement process, neither of these embodiments have the same structure
8 as Toyama's second modification. And specifically, none of them include,
9 for example, the plurality of dummy structures, 55, which Petitioner relies
10 upon to satisfy their limitation.

11 JUDGE CYGAN: Counselor, can I ask you about your phrasing it
12 as of this as an inoperability argument? Your argument here is about the
13 fact that this would make it impossible to do gate replacement, correct?

14 MR. CROSS: I don't think we said that it was impossible to do, it's
15 -- we said that in the petition -- or in the Patent Owner response that they
16 -- removes critical paths for it. And this is not an issue that was addressed in
17 the petition as to, like, other sources for the replacing the gate, the -- for
18 performing gate replacement. However, Dr. Yang has testified that these are
19 critical elements for the replacement process and that person of ordinary
20 skill in the art would not have just simply removed them by adding the
21 dielectric fill material around it.

22 JUDGE CYGAN: So is this an argument about motivation or an
23 argument about inoperability?

24 MR. CROSS: It's about -- it's the fact that Petitioner has not fully
25 addressed the obviousness combination and whether or not a person of
26 ordinary skill in the art would have been motivated to do it.

1 JUDGE CYGAN: And why -- can you draw the connection
2 between gates and the claims?

3 MR. CROSS: Between gates and the claims?

4 JUDGE CYGAN: Yes.

5 MR. CROSS: Well, the stack structure would be the gates, and the
6 channels go through -- the channel structures are structures that go through
7 the gate material in order to form memory devices -- or to form memory
8 cells for memory device.

9 JUDGE CYGAN: If you were looking at Claim 1 with its -- are
10 you contending that Claim 1 is only --

11 MR. CROSS: Are we talking about Claim 8?

12 JUDGE CYGAN: I'm sorry, Claim 8. That when we read Claim
13 8, we can't understand it as having the sacrificial material, we have to
14 understand it as having the replacing gate material. Is that the language
15 we're drawing from it?

16 MR. CROSS: And so the first limitation here is 8A, an alternating
17 conductor dielectric layer stack. So that's the alternating layers in a memory
18 structure that is the gate layers separated by dielectric. Now, Toyama uses a
19 gate replacement process.

20 JUDGE CYGAN: But isn't it also true that the sacrificial material
21 is also a conductor before it's replaced?

22 MR. CROSS: I don't believe so. I believe that's a combination of
23 -- it's typically two different dielectrics, one that is susceptible to a particular
24 etching, and that's the selective etching method used.

25 JUDGE CYGAN: So the line you're drawing to get to Claim 1 is
26 that the gate is the conductors in the alternating conductor dielectric layer

1 stack? I'm trying to connect your argument of gates so that we understand it,
2 so we understand why it's inoperable to the language of Claim 8. And I was
3 hoping you could help me with that.

4 MR. CROSS: Okay. So I think this issue of gate replacement is
5 different than the one where we talk about the current that goes through the
6 gate layers, and that's the conductive layers. And yes, it's the alternating
7 conductor dielectric layer, which is what forms the gate material. And if you
8 -- and we can get to this, this will be Slide 37. Here, we can see that by
9 placing the dielectric structure, instead of using the insulating liners, you're
10 now narrowing the cross section through which the current flows through the
11 gate layers. And that would be the conductive layers. This is similarly
12 shown here where we can see the -- sorry, and this is Slide 38, where we can
13 see the conductive layers, these are the gate layers. Does that answer your
14 question?

15 So in Slide 37, where the narrowest cross section is reduced
16 significantly, Dr. Yang testified that this would introduce reliability and
17 manufacturing issues. And that's because, as Dr. Lee had testified, local hot
18 spots form where the current density increases, and that's where there's a
19 narrowest cross section. And this can degrade your device reliability.

20 So it's because the current flows through a very narrow region, the
21 current density increases, creating local hot spots. And basically, it can
22 cause an open circuit. If it gets hot enough, it can frustrate the process of
23 channeling current to the selective memory cells in the channel structures
24 because you've got an open circuit. I hope I've answered your question. But
25 if not, I'm happy to try again.

26 JUDGE CYGAN: Oh, thank you. That's good enough.

1 MR. CROSS: So looking at Slide 37 again, we talked about how it
2 went from Toyama's unmodified structure, where the narrowest cross section
3 is from the liner of the TAC structure all the way to the trench above it. But
4 because they place this dielectric structure such that it makes -- that it abuts
5 or makes contact with Element 55D, which is the dummy structures, the path
6 of the current is now vastly reduced to just between the area between the
7 dummy structure and the trench structure.

8 Once again, Petitioner's solution to this, however -- and this is on
9 Slide 41 -- is that a POSITA would have known to use vias to convey an
10 electrical signal to each side of the dielectric structure. But this is
11 effectively adding -- or requires the addition of a second staircase for vias in
12 this new modification. And that's a far cry from the petition's ground, which
13 is nothing more than the simple substitution of the two elements of the liners
14 for the dielectric structure now.

15 And moreover, they didn't even address the additional issues that
16 would come from adding a second staircase region for -- and adding
17 additional vias for the same gate layer or conductive layer. As this would
18 increase the size of the device, it would limit each memory block to having
19 only one TAC region because you now have to be able to -- you have to be
20 able to address each side of the channel regions.

21 And therefore, having multiple TACs would create regions in
22 which the current couldn't flow from either direction, right? So there's only
23 one TAC region, which would eliminate interconnect capabilities. And
24 there's other issues that they failed to consider, such as the impact second
25 staircases would have on peripheral devices interconnects and the overall
26 power consumption.

1 Turning now to the purported motivation to combine. Petitioner's
2 sole motivation to combine in this case for this substitution of liners for
3 dielectric structure is that it would reduce the capacitive coupling between
4 the gate and the TAC. However, capacitive coupling between the gate and
5 the TAC is minimal. As Dr. Lee had explained in his deposition, capacitive
6 coupling between two conductors is proportional to the overlap of the area.

7 And here, we have TAC structures that run perpendicular to the
8 conductive layer. And so the overlap is minimal in comparison to the
9 overlap, say, between two of the gate layer -- the conductive layers, which
10 run parallel to each other and therefore have a large overlap area. That's
11 when you have to worry about capacitive coupling, not when two structures
12 run perpendicular to each other.

13 Moreover, turning to Slide 39, Dr. Lee's testimony entirely belies
14 their motivation to use dielectric structures instead of thin dielectric liners.
15 As he admits that it's dielectric liners, not a dielectric block, that would
16 provide better electrical characteristics, lower parasitic capacitance, more
17 uniform gate control, and better channel coupling.

18 If there's no questions on the issue of the replacement of liners or
19 on this issue, I'll turn to the surrounding issue of Limitation 8H. And that is
20 starting on slide -- sorry, excuse me. Well, I did want to address one other
21 thing regarding Petitioner's suggestion that Patent Owner is comparing the
22 figures of '806 to the figures of Toyama. That's just not true that we're
23 comparing scales but rather very different configuration.

24 So taking a look at Slide 47 of Petitioner, we see that the etchant
25 flow is obstructed by this line 72, which is a dielectric trench. That's
26 completely different than the '806 structure which is shown on Slide 52 of

1 Petitioner's demonstratives. Here, there are no such dielectric trenches and
2 that's why there's an increased of etchant flow.

3 Moreover, the '806 Patent fully explains how one would
4 implement the slit structures for the gate replacement process, and this is in
5 columns 16 of the '806 Patent, starting at lines 27 down through the rest of
6 that column. Moving on to the surrounding issue, this one is similar to
7 Ground 1. And so I'll turn over to those slides momentarily.

8 But one particular issue with Ground 2 and the replacement
9 process is that there'd be no need for Element 55D in Petitioner's
10 modification. As Toyama explains in paragraph 333 that the purpose of 55D
11 is to provide the structural support in areas where the sacrificial material has
12 been removed and there are no other structures to provide support. But here,
13 we have this large dielectric structure providing support, so there's no reason
14 to have these non-electrically functional structures in the proposed
15 modification.

16 Turning to Slide 18, I'll just briefly show. Here is the argument
17 that Petitioner is arguing that dummy structures 55D surround the drawn
18 TAC region that they have here because it's above and below. But these are
19 just sparsely distributed two on top and two on bottom that's hardly
20 considered surrounding.

21 However, Petitioner's argument that the intrinsic evidence shows
22 that a first feature may surround another on just two sides is also incorrect.
23 As we can see in Slide 19 Figure 1C shows the stack on all four sides and
24 Figure 1B shows that the stack extends beyond both sides, the left and the
25 right, of the TAC region. This is not analogous to Toyama where we just
26 have two structures at the top and bottom.

1 Regarding the periphery issue, that does no more than simply
2 describe what's being shown in Figure 48B. It's two dummy structures at the
3 periphery of figure -- of Element 600 but on the top side and two at the
4 periphery on the bottom side. There's no suggestion that just because
5 Toyama says that it can be located at the periphery, that it's all along
6 periphery on all four sides.

7 Finally, Petitioner's obviousness arguments fair no better here.
8 Patent Owner is pointing to the rationale is that Toyama describes having
9 pillar structures that can be formed in other regions. They point to language
10 that is referencing Figures 4A and 4B. These pillar structures are in the
11 staircase region where there are no other structures to provide support.

12 Instead, that's why you need dummy structures because otherwise
13 during the sacrificial -- during the removal of the sacrificial layer, it would
14 collapse because there are no other structures, whereas in the memory array,
15 you have tons of structures, you have lots of channel structures, you have
16 TACs. And Toyama only describes providing 55D in these specific
17 locations when the TACs are surrounded by liners.

18 And with that, if there are no other questions, I'll reserve the
19 remainder of my time for --

20 JUDGE MCGRAW: To confirm, did you reserve 15 minutes?

21 MR. SAGDEO: Twenty, Your Honor.

22 JUDGE MCGRAW: You may begin when you're ready.

23 MR. SAGDEO: Your Honors, Patent Owner made great hay about
24 Figure 17E and Figure 17F with respect to Ground 2. But I want to
25 emphasize that Toyama is not limited to ground -- to Figure 17E and F, that
26 Patent Owner does not dispute and nor was the Petitioner's theory. The

1 Petitioner explained that a POSITA would have known how to implement
2 Toyama's first exemplary structure by implement -- or implement multiple
3 planes of Toyama's first exemplary structure.

4 And the use of Figure 17E was an example, you know, the
5 highlighted sentence is a general statement of the obviousness combination.
6 Thus, for example, you could use Figure 17E to illustrate that example.
7 Moreover, Figure 17E itself is extremely broad. It's just got sort of a kind of
8 a conceptual diagram of various regions of the device.

9 Toyama does not state that the first exemplary structure is limited
10 to 17E. And Toyama doesn't say anywhere that if you use Figure 17E, you
11 have to use Figure 17F. Moreover, the entire -- so the exercise of
12 obviousness here is we're taking the teachings from Toyama. It's Patent
13 Owner that is really just sort of putting form over substance when it fixates
14 on a figure that was never in the petition that we're not drawing teachings
15 from. This is not part of the ground.

16 And so I would point the Courts, for example -- sorry, the Board
17 had various questions about Dr. Lee's testimony here. And I thought it
18 might be helpful to go through some of his testimony on this issue of routing
19 peripheral circuitry. So let's see if I can -- this is Dr. Lee's '806-1
20 declaration, paragraph 47, implementing peripheral circuitry was highly
21 routine and had been standard memory design for many decades prior to the
22 '806 Patent.

23 Dr. Lee describes many examples of the use and the placement of
24 peripheral circuitry, examples that I should add, Patent Owner does not
25 rebut. And Dr. Lee further states that what we're doing here is the
26 obviousness combination involves a placement of peripheral circuitry. And

1 that's something that would need to be done in the combination.

2 But I should add, this is not a claim limitation. This is a reasonable
3 expectation of success argument. This was not something that Petitioner had
4 to show in its petition. I mean, Patent Owner's argument is sort of like if it
5 faulted the Petitioner for not saying where the power supply is or what the
6 housing is made out of, this is not a claim element.

7 This is sort of routine and conventional design work that would go
8 into any sort of memory design, something that was within the skill of a
9 skilled artisan. And so Dr. Lee continues, he notes -- and I'm sort of
10 paraphrasing, paragraph 54 -- now that there are many places to put
11 peripheral circuitry, even under the memory array, for example, in the
12 context of 3D devices, designers have great flexibility in the placement of
13 peripheral circuitry. So it's not like you had to follow a specific constrained
14 layout. This was never Petitioner's theory that you had to follow any
15 specific constrained layout.

16 And so in summary -- and this is, essentially, unrebutted expert
17 testimony -- a POSITA would not have encountered any problems or
18 difficulties in placing peripheral circuitry when modifying Toyama's first
19 exemplary structure, to include multiple memory planes, this is paragraph
20 56. There are all these -- there are textbooks on which Dr. Lee relies.

21 I would encourage the Board to review them if they would like
22 more detail that talk about this routine exercise. And so at bottom, there's
23 nothing -- and I should add, there's nothing within Toyama that would
24 suggest that you have to place the peripheral circuitry in one place or
25 another. Dr. Lee explains that Toyama's structure did not preclude or
26 complicate peripheral circuit integration, as paragraph 57.

1 So where does this sort of leave us? We're not relying on Figure
2 17F for the location of vertical circuitry. Toyama does nowhere require the
3 use of Figure 17F. And so, really, Patent Owner's argument is the classic
4 bodily incorporation argument. Not only is it improper because they're
5 relying on a theory that Petitioner ever advanced, but they're also -- even if
6 Petitioner did rely on it, it was -- it wouldn't -- which we didn't. It would
7 just be sort of a mindless reliance on that without asking the more
8 fundamental question of how a person of skill would put these teachings
9 together.

10 Moving to Ground 2 or -- and sorry, the device limitation of
11 ground so --

12 JUDGE MCGRAW: Before you move on, what you're showing us
13 on the -- on this slide right now-- is from which proceeding?

14 MR. SAGDEO: This is the '806-1 proceeding that is, I believe, the
15 IPR ending in 791.

16 JUDGE MCGRAW: And this is Dr. Lee's --

17 MR. SAGDEO: Reply declaration.

18 JUDGE MCGRAW: Reply declaration. Thank you.

19 JUDGE CYGAN: And your answer to Patent Owner's argument is
20 what? Patent Owner's argument, to the extent that we need to follow exactly
21 what you have put in the petition, in the petition you seem to only account
22 for certain portions of Toyama and not other portions. What's your response
23 to that argument?

24 MR. SAGDEO: So the petition relies on certain teachings from
25 Toyama. To kind of back up a bit, the exercise that we're going through is
26 what would a person of skill in the art, you know, having references in hand,

1 what would be obvious to them. And we're not relying on, you know,
2 Toyama's very lengthy references, as this Board well knows, we're not
3 relying on every little bit and piece of it. We're relying on certain teachings
4 from it. We're relying, for example, on Figure 17A and Figure 17B which
5 talk about the arrangement of the first exemplary structure. And we're not
6 relying on Figure 17F. We're not relying on the second exemplary structure.

7 And so we don't have to sort of explain every aspect of Toyama
8 that we're not relying on. We've identified the parts of Toyama, the relevant
9 teachings in the prior art that we're using in our petition. And so that's
10 Patent Owner's attempt to bring in a different figure is legally improper.

11 JUDGE CYGAN: Well, apart from Figure 17F, in your Petition,
12 when you're replicating in the hd1 direction, you're only showing certain
13 portions of Toyama being replicated. I think their argument is that your
14 obviousness case does not involve replicating other portions that aren't
15 shown in that picture, regardless of what a POSITA might do in a different
16 way, that we should be bound by exactly the way you have arranged the
17 parts in your obviousness case.

18 MR. SAGDEO: Well, we didn't or -- so figures -- the diagram of
19 the modified version of Figure 17E is just an example. It's not the limit of
20 Petitioner's theory. And I don't think the Petitioner's theory should be read
21 as limited to that figure. What we're talking about here is something that is
22 not in the claims but is in a literal sense peripheral. It's something that might
23 be part of -- it would be part of the device, but it's not claimed.

24 And so when we're doing our -- we're sort of making our prima
25 facie showing, we don't have to talk about what the power supply, the
26 peripheral circuitry, the housing. We've explained that what we're doing is

1 using a known technique. Let's see if I can find the exact language. But
2 we're essentially taking a known technique, which is the implementation of
3 multiple planes.

4 So this is the petition at 77, it's applying a known technique,
5 implementing multiple planes of a NAND flash memory to a known device,
6 Toyama's first exemplary structure to yield predictable results, a NAND
7 flash device with improved performance. So none of these predicate facts to
8 the obviousness combination are disputed.

9 There's no dispute that multiple planes or a known technique, no
10 dispute that Toyama's first exemplary structure was known, and there's no
11 dispute that the proposed combination would have the predictable and
12 beneficial result of improved performance. I think that Patent Owner's
13 attempt to cherry-pick certain statements in the petition and misread them
14 should be rejected because that was never what the obviousness combination
15 was about.

16 JUDGE CYGAN: So are you arguing there was something
17 broader in your petition than simply duplicating planes, including a distinct
18 memory array and a staircase structure?

19 MR. SAGDEO: Well, I would point, Your Honor, to this
20 language. The obviousness combination is using a known technique to
21 -- which is to say implementing multiple memory planes of Toyama's first
22 exemplary structure. That exemplary structure, it's not disputed, it's not
23 limited to Figure 17F. And we articulate this theory in multiple different
24 places in a broad way.

25 So for example, now, on page 69 -- and I'm just looking at the
26 heading -- a POSITA would have found it obvious to implement multiple

1 planes of Toyama's first exemplary structure in the hd1 direction. A
2 POSITA would have found it obvious to implement Toyama's first
3 exemplary structure in a 3D memory device with multiple planes. So
4 repeatedly, we've identified and explained our theory in a way that is not
5 limited to Figure 17E or Figure 17F.

6 JUDGE CYGAN: But in the example on 69, your language only
7 highlights the memory array region in the staircase structure. How does the
8 person reading this understand that you have a broader replication and not
9 just those features which you're mentioning?

10 MR. SAGDEO: Well, I think -- Your Honor, I don't see any -- I
11 think I would point the Court to the petition as a whole, which talks about
12 the claim mapping parts, where we talk about where you can find channel
13 structures, where you can find an alternating stack. So we focus on the
14 claim limitations because that's sort of the purpose of the petition.

15 But we never had to sort of provide a detailed schematic saying
16 exactly how -- you know, a manufacturing ready schematic showing exactly
17 how this device would look. That's not Petitioner's burden. And so when
18 Patent Owner comes back in reply and talks about peripheral circuitry -- or
19 sorry, in its response, it talks about peripheral circuitry, not in the context of
20 a claim mapping but in a sort of reasonable expectation of success argument,
21 then the Petitioner is entitled to respond and say, well, here's how you would
22 design these other parts of the device which are not teed up by the claims;
23 but nevertheless, a person of skill would be able to implement them.

24 JUDGE CYGAN: So am I understanding your argument now to
25 say that your petition is addressing the requirements of the claims and not
26 other requirements which may be necessary to show the details of how they

1 get put together? Is that what you're saying?

2 MR. SAGDEO: I don't think I would agree with that phrasing,
3 Your Honor. I would say the petition focused on the language of the claims
4 and it made a strong prima facie case that there would be motivation to
5 combine and reasonable expectation of success. What Patent Owner has
6 done is contest reasonable expectation of success.

7 And so in reply, we've identified additional evidence showing that
8 their arguments lack merit. And I would -- going to the device limitation
9 briefly, I'll note that Patent Owner hasn't attempted to show that -- to rebut
10 any of the extrinsic evidence showing that the plain meaning of device
11 includes multi-plane devices. Patent Owner hasn't attempted to show that
12 we have -- that there's a basis to depart from the usual rule that a device -- or
13 that preamble term is not limiting.

14 On Ground 3, I wanted to point out a confession by Patent Owner
15 that no, it's not impossible to do gate replacement. So Patent Owner is
16 admitting that the proposed combination would not have this issue. What
17 Patent Owner is really saying -- and this is improper -- is, well, we didn't
18 explain in the petition how to do gate replacement or address -- or any
19 potential current restriction in the petition.

20 But again, these are not plain terms, these are issues that go to
21 reasonable expectation of success. And in reply, we explained, using
22 Toyama, using other extrinsic evidence, that these purported problems are
23 not really problems, people have overcome them. Toyama itself overcomes
24 them. And the '806 Patent doesn't teach anything that would sort of
25 distinguish itself from Toyama in these respects.

26 With respect to Ground 3, Patent Owner also didn't dispute that the

1 -- that it's arguments with respect to the surrounding limitation, many of
2 those are waived. Patent Owner didn't dispute that it didn't say in its POR
3 that -- it didn't attempt to distinguish the periphery language in its POR.
4 Patent Owner doesn't dispute that it didn't respond to the petition's
5 obviousness theory in its POR for the surrounding limitation of Ground 3.

6 And so on Ground 2 -- returning to Ground 2, I'll note that figure
7 -- so Figure 17E is -- I was just pointing the Board to the bodily
8 incorporation cases that we cited in our papers because they rejected
9 arguments very similar to the argument that Patent Owner is now making.
10 Basically, Patent Owner tried to make this sort of burden of proof argument
11 where they said, oh, well, your petition only explained the combination in
12 this way and so you're limited to it.

13 And the Federal Circuit, in each of those cases, rejected -- at least
14 many of those cases rejected that argument and said, you know, you -- I
15 think in one of the cases, the language was something like the Board was
16 parsing the combination with too fine a filter. The obviousness combination
17 that we articulated in the petition is not limited to specific figures, let alone
18 Figures 17E or 17F.

19 And so I think it's -- those cases stand for the proposition that what
20 the inquiry is, is not whether Toyama's first exemplary structure, or certain
21 figures of it, can be copy-pasted, but instead whether a person of skill would
22 be able to use those teachings and construct a multi-plane version of that
23 structure with the features that we've identified. And the petition did that.
24 The reply brief confirmed that.

25 And I think when Patent Owner argues to the contrary, it's
26 mischaracterizing what the theory is. Oh, one thing I'd like to just mention

1 with respect to Ground 3, Patent Owner says, when we rely on -- so we rely
2 on certain embodiments in Toyama that essentially disprove their arguments.
3 So for example, they say, if you have a dielectric block in the memory array,
4 you're going to have trouble with gate replacement, you're going to have
5 trouble with current restriction or elimination.

6 So we point to embodiments in Toyama that essentially refute that
7 because they're dielectric blocks in the memory array and they're presumed
8 to be functional. And Patent Owner doesn't contend otherwise. So these are
9 not new mappings. We're not, you know, putting forth a new ground in our
10 reply. This is persuasive extrinsic evidence that goes to motivation to
11 combine and reasonable expectation of success. This is saying Patent
12 Owner's argument about current restriction has no merit because Toyama
13 itself rejects it.

14 Toyama has embodiments that have precisely the features of -- that
15 relate to its objections, its inoperability arguments. The fact that those
16 different embodiments don't have other claim limitations is totally irrelevant.
17 Like, the relevant aspect of those embodiments is that they reject Patent
18 Owner's inoperability arguments.

19 Their features are -- they both involve dielectric blocks just like the
20 proposed combination and they make it work. So I think that Patent Owner's
21 characterization of those embodiments is incorrect and they're not untimely
22 because they respond to Patent Owner's arguments raised in its POR. I think
23 with that, I'm just about out of time.

24 JUDGE MCGRAW: I do have one question for you about Ground
25 1 and Claim 8 regarding the plurality of TACs. Let me look at the exact
26 language. The claim requires a plurality of TACs extending vertically

1 through the dielectric structure. Can you explain why it's your position that
2 you can have a single TAC through a single dielectric and the claim does not
3 require a plurality of TACs through a dielectric structure?

4 MR. SAGDEO: Yes, Your Honor. So I'll start the answer by
5 noting that it's our position that Claim 8 and that language is materially the
6 same as the other -- the claims of the '378 -- or I should say the Claim 15 of
7 the '378 Patent in the sense that they both recite through array contacts
8 through a dielectric structure, you know, there's certain differences.

9 But what I would note for *Finjan* is that case involved when you
10 had multiple limitations in the same claim, like -- of what -- 3 and where you
11 had -- you have to have the same set of components meet each and every one
12 of these limitations. Here, we have a different situation. There's only one
13 limitation in dispute.

14 And there's no dispute that the same set of dielectric liners meet
15 each of the dielectric structure limitations, the limitation which recites it
16 abutting the alternating stack, the limitation that recites it being made of a
17 dielectric material. So the same set of components meet every single
18 limitation that distinguishes us from *Finjan*. And so I think what *Baldwin's*
19 lesson is, is you sort of -- and *Baldwin* involved the word "said," which is
20 sort of like the word "of," in that it refers back to previous -- you know, it
21 has an antecedent basis.

22 What *Baldwin* stands for is the idea that when a limitation uses the
23 word "the," it takes on its numerosity from its antecedent basis. So because
24 it would -- the first use was a dielectric structure, the subsequent uses are
25 -- and that means one or more, the subsequent uses are one or more. What
26 *Finjan* stands for is the more, which is a -- as the distinct proposition is that

1 you have to point to the same set of structures for every single limitation.

2 And there's no dispute that in this case the dielectric liners are the
3 same set of one or more -- in this case more -- structures that meet every
4 limitation. So it is in this claim plurality of through array contacts extending
5 vertically through one or more dielectric structures. And so basically, that's
6 sort of the lesson of *Baldwin*. And so we do have this through a plurality of
7 through array contacts extending through one or more dielectric structures
8 here, and that's why it's met.

9 JUDGE MCGRAW: Are you asserting that the three dielectric
10 liners constitute one dielectric structure?

11 MR. SAGDEO: We are asserting that. But the argument that I
12 just made is not premised on that in the sense that when in Claim 8 of the
13 '806 Patent in that limitation that recites the dielectric structure, it's really
14 that "the" should be understood to permit multiple dielectric structures so
15 long as we have pointed to the same dielectric structures for every other
16 limitation reciting the dielectric structure.

17 JUDGE MCGRAW: Thank you. You may begin when you're
18 ready.

19 MR. RADSCH: Thank you, Your Honor. So I just like to start
20 with the Ground 2 issue, again, back to this discussion of what the ground is.
21 The only description in this petition of what the modification here is the
22 repetition of Figure 17E. That's not ever described as simply one exemplary
23 modification. And they don't rely upon any other figures or disclosures for
24 the elements that are required, that is the particular structures, your TAC
25 region in between the channel regions.

26 So it's 17E that they rely upon for that configuration in this

1 particular repeated embodiment. So it is 17E, it's specific repetition that
2 they're relying upon. They say so expressly in the petition. This is at
3 paragraph number -- or page 74. Again, coming back to what their own
4 experts said in the reply declaration, each -- in the proposed modification,
5 each individual plane is fabricated in exactly the same way. So it is an
6 exactly repeating pattern, according to their proposed ground.

7 There's further discussion of the bodily incorporation case law. I
8 would submit that that is not pertinent here, not proposing modifying or
9 combining two references. They are proposing replicating a particular
10 disclosure, which is 17E. Now, in 17E we see, for example, these features
11 86, that is the word line contact via structures.

12 So we know that there are these structures to which interconnects a
13 TAC. And now, they have argued that, well, the claims don't address or
14 recite peripheral circuitries or interconnects. And therefore, we did not need
15 to address that in the petition. I would submit that that is the exact opposite
16 of what they needed to do.

17 Now, they didn't need to show that they are present since they're
18 not claimed. But where they are present here -- and they do impact what
19 their proposed modification is -- they had an obligation to explain how that
20 modification would work in view of those features. And Counsel also stated
21 that you don't have to use Figure 17F with 17E.

22 To start with, 17E is the only thing the petition relies upon. And I
23 don't really understand that statement about using 17F with 17E because as
24 Toyama expressly says at paragraph 49, 17E and 17F are simply top-down
25 views of the same structure. They're just different views of the same thing.
26 So it's not about using one with the other. It's just accounting for that

1 structure. Of course, as the law tells us, we have to use a prior art for all that
2 it discloses. We can't put our blinders on, pretend 17F doesn't exist. It is
3 part of the structure of 17E, it's just at a different plane.

4 Going back just very briefly to the issue of the reply declaration,
5 Counsel stated that there was testimony about reasonable expectation of
6 success and that it was un rebutted. That reasonable expectation of success
7 in moving the peripheral circuitry, Your Honor asked what declaration it
8 was. He explained it was the reply declaration.

9 Well, of course it's un rebutted. It's a reply declaration. You do not
10 have the opportunity but to put in a declaration in sur-reply. So the first time
11 they address moving the circuitry to some other location and whether there's
12 reasonable expectation of doing that, which I would submit that not shown
13 would be in the reply declaration, and an obligation to do that in their
14 petition when it's their proposed combination that they're addressing.

15 In addition, the issue is not one of reasonable expectation of
16 success, that is the location of the circuitry in Figure 17E that they're relying
17 upon. It doesn't have to do with reasonable expectation of success. It has to
18 do with whether you have a functioning memory device at all. Here, there is
19 absolutely no room left for adding those interconnects or circuitry. You do
20 not have a functioning device. You would have to further modify this in
21 ways that are unexplained and unaddressed.

22 And so it is simply a matter of a failure of proof, a failure to
23 address the claim limitations, failure to address what Toyama discloses
24 expressly in the embodiment that they are relying upon, the only
25 embodiment they are relying upon. And in addition, it is perhaps in addition
26 to a reasonable expectation of successes is issue. It's certainly not -- that's

1 not the only issue with the peripheral circuitry.

2 Now, the -- Counsel also stated that they didn't have to address
3 these issues in their petition because they only have to make a prima facie
4 showing and that's all they've done. And that's the wrong standard. They
5 have to show that there's, like, preponderance of evidence that the claims are
6 rendered obvious. They have not done that.

7 They've utterly failed to address the full disclosure of Toyama with
8 respect to what they are relying upon, how that impacts the ability to
9 replicate exactly as they have -- the expert has explained the hd1 and hd2
10 direction, these individual memory devices. Turning just then -- briefly just
11 to the *Finjan* issue again, I just want to reiterate because Counsel again
12 referenced *Baldwin*.

13 *Finjan* is explicit, *Baldwin* does not address the issue of whether
14 subsequent limitations, referring back to an antecedent claimed element,
15 what the requirements of that are, that's what *Finjan* addresses *Baldwin*
16 simply -- that the proposition that "a" means one or more and that -- so that
17 does -- that -- going to the issue of multiple TACs through a structure as
18 *Finjan* would tell us, there needs to be at least one structure that has multiple
19 TACs, one dielectric structure. It can also be two that have multiple TACs,
20 there can be three that have multiple TACs. And as *Finjan* expressly says,
21 there must be at least one. So they're simply wrong, we would submit on the
22 case law.

23 I think my -- unless there are any questions on the *Finjan* issue or
24 on Ground 2, the first exemplary embodiment, I will cede the podium to Mr.
25 Cross who has just a few points to make.

26 MR. CROSS: Your Honors, I'd just like to address one issue that

1 came up in Counsel's -- for the first time in Counsel's rebuttal, and that's that
2 the plurality of dielectric liners forms a single dielectric structure. Turning
3 to Slide 16, just to note that this argument was preliminarily rejected at
4 institution and nothing since has changed that these liners are not a single
5 dielectric structure.

6 Patent Owner's interpretation is -- whereas Patent Owner's
7 interpretation is consistent with all embodiments having multiple TACs
8 through a dielectric structure. Petitioner has not identified any intrinsic
9 support that the claims cover multiple liners with only one TAC through
10 each respective liner. Furthermore, turning to Slide 8, the disclosed
11 embodiments with multiple TACs depicts TACs extending through the same
12 dielectric structure.

13 And this is intentional because this is the intended purpose of
14 invention of the '806 Patent where it's avoiding having to form multiple
15 TACs and TAC liners through the alternating layer stack, which would
16 increase the fabrication and cost. And it's -- thus, the intention of the claims
17 -- it clearly goes against the intention of the patent that suggests that the
18 claims of having a plurality TACs extending through the same dielectric
19 structure would encompass individual liners with individual TACs going
20 through them. If there are no questions, we'll cede the rest of our time.

21 JUDGE MCGRAW: Thank you.

22 Thank you again for having such wonderful presentations and
23 being prepared for today's hearing. We very much appreciate it. If either
24 party has color copies of the demonstratives that they would like to pass up
25 to the panel, we could take those now. With that, the hearing has concluded.
26 And the final written decision, we'll issue in due course. Thank you.

IPR2024-00791 (Patent 10,937,806)

IPR2024-00911 (Patent 10,937,806)

1 (Whereupon, the above-entitled matter went off the record at 4:05
2 p.m.)

IPR2024-00791 (Patent 10,937,806)

IPR2024-00911 (Patent 10,937,806)

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