

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner
v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,
Patent Owner

Case No.: IPR2024-00791
U.S. Patent No. 10,937,806

**PETITIONER'S REQUEST FOR DIRECTOR REVIEW OF THE BOARD'S
FINAL WRITTEN DECISION**

TABLE OF CONTENTS

	Page
I. INTRODUCTION	1
II. THE BOARD ERRED IN ALLOWING PATENT OWNER’S CONCERNS ABOUT OPERABILITY TO DEFEAT MICRON’S SHOWING OF A MOTIVATION TO MODIFY IN GROUND 2.....	3
A. The Board Erroneously Required Bodily Incorporation.....	6
B. The Board Erroneously Disregarded Reply Arguments That Directly Refuted Patent Owner’s Operability Concerns.....	7
C. The Board Required Evidence Of Anticipation Rather Than Obviousness.....	10
III. THE BOARD ERRED IN ALLOWING PATENT OWNER’S CONCERNS ABOUT OPERABILITY TO DEFEAT MICRON’S SHOWING OF A MOTIVATION TO COMBINE IN GROUND 3.	12
IV. CONCLUSION.....	15

TABLE OF AUTHORITIES

	Page(s)
Cases	
<i>Apple Inc. v. Andrea Elecs. Corp.</i> , 949 F.3d 697 (Fed. Cir. 2020)	8, 14
<i>Arctic Cat, Inc. v. Bombadier Recreational Prods., Inc.</i> , 876 F.3d 1350 (Fed. Cir. 2017)	15
<i>Banner Eng’g Corp. v. Tri-Tronics Co., Inc.</i> , 11 F.3d 1071, 1993 WL 43283 (Fed. Cir. Oct. 27, 1993)	11
<i>Elbrus Int’l Ltd. v. Samsung Elec. Co., Ltd.</i> , 738 F. App’x 694 (Fed. Cir. 2018)	6, 7, 8, 9
<i>Ethicon LLC v. Intuitive Surgical, Inc.</i> , No. 21-1995, 21-1997, 2022 WL 1613188 (Fed. Cir. May 23, 2022)	7
<i>Google LLC v. Ji-Soo Lee</i> , 759 F. App’x 992 (Fed. Cir. 2019)	12
<i>Idemitsu Kosan Co., Ltd. v. SFC Co., Ltd.</i> , 870 F.3d 1376 (Fed. Cir. 2017)	9
<i>Intel Corp. v. PACT XPP Schweiz AG</i> , 61 F.4th 1373 (Fed. Cir. 2023)	11
<i>Intel Corp. v. PACT XPP Schweiz AG</i> , No. 22-1038, 2023 WL 2198649 (Fed. Cir. Feb. 24, 2023)	7
<i>KSR Int’l Co. v. Teleflex Inc.</i> , 550 U.S. 393 (Fed. Cir. 2007)	passim
<i>Laitram, LLC v. Ashworth Bros., Inc.</i> , Nos. 22-1044, 22-1045, 22-1084, 2023 WL 3449148 (Fed. Cir. May 15, 2023)	6, 7
<i>Rembrandt Diagnostics, LP v. Alere, Inc.</i> , 76 F.4th 1376 (Fed. Cir. 2023)	8

<i>Sanofi Aventis Deutschland GmbH v. Mylan Pharms. Inc.</i> , 791 F. App'x 916 (Fed. Cir. 2019)	10, 14
<i>In re Sovish</i> , 769 F.2d 738 (Fed. Cir. 1985)	11

LISTING OF EXHIBITS

Exhibit	Description
1001	U.S. Patent No. 10,937,806 B2 to Tao et al.
1002	File History of U.S. Patent No. 10,937,806 B2 to Tao et al.
1003	Declaration of Jack C. Lee
1004	<i>Curriculum Vitae</i> of Dr. Jack C. Lee
1005	U.S. Patent Publ. No. 2017/0179026 A1 to Toyama et al. (“Toyama”).
1006	Minute Order, Dkt. No. 42, dated February 22, 2024 in <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC</i> , Case No. 3:23-cv-05792-RFL
1007	Combined Civil and Criminal Federal Court Management Statistics (December 31, 2023), available at https://www.uscourts.gov/sites/default/files/data_tables/fcms_na_distcomparison1231.2023.pdf
1008	Docket from <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC</i> , Case No. 3:23-cv-05792-RFL
1009	CN109075169A Office Action, dated November 14, 2019
1010	Certified Translation of CN109075169A Office Action, dated November 14, 2019
1011	CN109075169A Reexamination Decision, dated November 25, 2021
1012	Certified Translation of CN109075169A Reexamination Decision, dated November 25, 2021
1013	Micheloni, “3D Flash Memories” (2016)

Exhibit	Description
1014	Aritome, “NAND Flash Memory Technologies” (2016)
1015	U.S. Patent Publ. No. 2018/0108671 A1 to Yu et al.
1016	U.S. Patent Publ. No. 2019/0229125 A1 to Zhou et al.
1017	U.S. Patent No. 10,354,980 B1 to Mushiga et al.
1018	U.S. Patent No. 9,293,348 B2 to Lai et al.
1019	U.S. Patent No. 8,598,643 B2 to Kawasaki et al.
1020	U.S. Patent No. 8,697,519 B2 to Jee et al.
1021	Excerpts from “Merriam-Webster’s Collegiate Dictionary,” Eleventh Edition (2014)
1022	Print out of https://www.studycountry.com/wiki/what-is-a-piece-of-land-surrounded-by-water-on-2-sides
1023	Michelson et al., “Inside Solid State Drives (SSDs)” (1 st Ed. 2013)
1024	U.S. Patent No. 10,043,558 to Shah et al.
1025	Michelson et al., “Inside NAND Flash Memories” (2010)
1026	Lau, “Ball Grid Array Technology” (1995)
1027	U.S. Patent No. 10,103,169 to Ge et al.
1028	U.S. Patent No. 9,935,050 to Dunga et al.
1029	<i>Intentionally Omitted</i>
1030	<i>Intentionally Omitted</i>
1031	<i>Intentionally Omitted</i>
1032	<i>Intentionally Omitted</i>

Exhibit	Description
1033	<i>Intentionally Omitted</i>
1034	<i>Intentionally Omitted</i>
1035	<i>Intentionally Omitted</i>
1036	<i>Intentionally Omitted</i>
1037	<i>Intentionally Omitted</i>
1038	Complaint for Patent Infringement, Dkt. No. 1, filed Nov. 9, 2023, in <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC</i> , Case No. 3:23-cv-05792-RFL
1039	First Amended Complaint for Patent Infringement, Dkt. No. 29, filed Feb. 2, 2024, in <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC</i> , Case No. 3:23-cv-05792-RFL
1040	Plaintiff and Counterclaim Defendant Yangtze Memory Technologies Company, Ltd.’s Disclosure of Asserted Claims and Infringement Contentions, dated May 6, 2024, in <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC</i> , Case No. 3:23-cv-05792-RFL
1041	Declaration of Jared Bobrow in Support of Petitioner’s Motion for Admission <i>Pro Hac Vice</i>
1042	<i>Intentionally Omitted</i>
1043	Reply Declaration of Dr. Jack C. Lee (“Lee-Reply”)
1044	Transcript of the Deposition of Woodward Yang, dated April 22, 2025, in <i>Micron Technology, Inc. v. Yangtze Memory Technologies Company, Ltd.</i> , Case Nos. IPR2024-00788, -00909

Exhibit	Description
1045	Woodward Yang, Deposition Exhibit 4, in <i>Micron Technology, Inc. v. Yangtze Memory Technologies Company, Ltd.</i> , Case Nos. IPR2024-00788, -00909
1046	Woodward Yang, Deposition Exhibit 5, in <i>Micron Technology, Inc. v. Yangtze Memory Technologies Company, Ltd.</i> , Case Nos. IPR2024-00788, -00909
1047	Transcript of the Deposition of Woodward Yang, dated April 24, 2025, in Case Nos. IPR2024-00791, -00911
1048	Woodward Yang, Deposition Exhibit 2, in Case Nos. IPR2024-00791, -00911
1049	Michelson et al., “Inside Solid State Drives (SSDs)” (2 nd Ed. 2018)
1050	PCT Publication No. WO 2009/079014 A1 to Yang et al.
1051	Additional excerpt from “Merriam-Webster’s Collegiate Dictionary,” Eleventh Edition (2014)
1052	Print out of https://gf.com/about-us/gf-in-the-community/stem-at-gf/glossary-of-terms/
1053	Petitioner’s Hearing Demonstratives

TABLE OF ABBREVIATIONS

ABBREVIATION	TERM
PO or Patent Owner	Yangtze Memory Technologies Co. Ltd.
Petitioner	Micron Technology, Inc.
IPR2024-00791	
Petition or Pet.	Petition for <i>Inter Partes</i> Review of U.S. Patent No. 10,937,806 (IPR2024-00791, Paper 1)
PO Response	Patent Owner’s Response (IPR2024-00791, Paper 14)
Reply	Petitioner’s Reply (IPR2024-00791, Paper 16)
PO Sur-Reply	Patent Owner’s Sur-Reply (IPR2024-00791, Paper 18)
FWD	Final Written Decision Determining No Challenged Claim Unpatentable (IPR2024-00791, Paper 35)
’806 patent	U.S. Patent No. 10,937,806 B2 (IPR2024-00791, Ex. 1001)

I. INTRODUCTION

Petitioner Micron Technology, Inc. requests Director Review of the Board's Final Written Decision ("FWD," Paper 35) holding claims 8-9 and 11-12 of the '806 patent not unpatentable for obviousness. Micron demonstrated that various embodiments of Toyama, alone or in combination with one another, render claims 8-9 and 11-12 of the '806 patent obvious. The Board's rejection of those grounds rests on clear factual and legal errors that warrant Director Review and reversal or vacatur. *See* Director Review Process, § 2.B.

The Board erred in declining to find a motivation to modify Toyama's First Exemplary Structure to implement multiple planes of memory, as Micron proposed in Ground 2. The Board mistakenly credited Patent Owner's argument that implementing multiple planes of memory would interfere with peripheral circuitry located to the left of Toyama's memory array in the First Exemplary Structure. But the Federal Circuit does not require bodily incorporation of prior art references to establish obviousness. And regardless, Micron demonstrated that a skilled artisan would have easily accounted for the placement of peripheral circuitry in modifying Toyama. The Board abused its discretion in refusing to consider that evidence solely because it appeared in Micron's reply brief. A petitioner is not—and cannot possibly be—expected to preempt every possible criticism of an unpatentability ground at the petition stage. Rather, so long as the petition lays out a *prima facie* obviousness

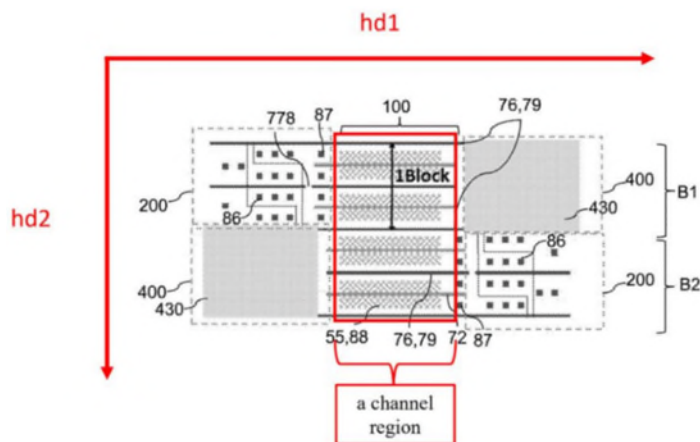
case, the petitioner may provide new arguments and evidence to refute criticisms on reply. Finally, the Board incorrectly required Micron to provide evidence that a structure *just like* Toyama's had been modified *just like* Micron proposed. Micron established a motivation to arrive at the claimed invention by showing that the advantages of multi-plane memory would have led a skilled artisan to make the proposed modification. The Board was wrong to require more.

The Board's rejection of Ground 3 repeats many of the same errors that the Board made with respect to Ground 2. In Ground 3, Micron demonstrated that substituting one of the dielectric structures Toyama discloses for another would have had predictable results and led to a suitable memory device. Yet again, the Board declined to find a motivation to combine, relying on Patent Owner's argument that Micron's proposed combination would pose operability hurdles. And again, the Board refused to consider any of the evidence or arguments Micron made in reply—even though those arguments were limited to refuting Patent Owner's operability concerns. In effect, the Board created a rule whereby patent owners with obvious claims may avoid unpatentability determinations simply by raising concerns about operability—and no matter how unfounded or easily refuted those concerns may be, petitioners are powerless to respond. The Director should intervene to restore the proper procedural and substantive rules for establishing obviousness.

II. THE BOARD ERRED IN ALLOWING PATENT OWNER'S CONCERNS ABOUT OPERABILITY TO DEFEAT MICRON'S SHOWING OF A MOTIVATION TO MODIFY IN GROUND 2.

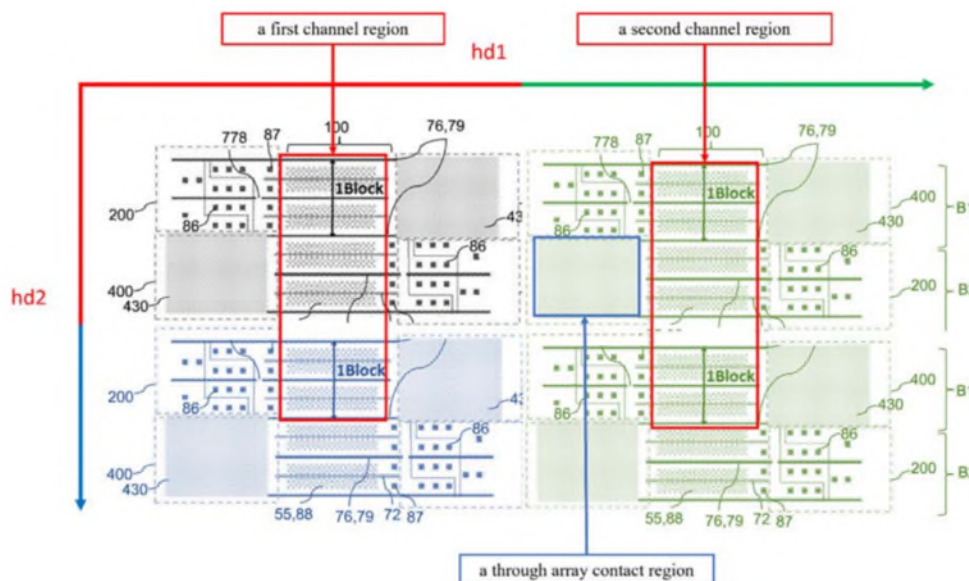
Independent claim 8 of the '806 patent requires “first and second channel regions comprising first and second pluralities of channel structures, respectively” and “a through array contact (TAC) region formed between the first and second channel regions.” '806 patent, 23:58-59, 24:1-2. In Ground 2, Micron demonstrated that these claim limitations would have been obvious, because a skilled artisan would have been motivated to implement Toyama's First Exemplary Structure in a 3D memory device with multiple planes. Pet., 59-86.

Toyama discloses memory stack structures 55 forming a channel region, as illustrated by Figure 17E below:



Pet., 67 (quoting Toyama, Fig. 17E (annotated)). Toyama expressly contemplates that this block layout could be repeated along the “hd2” direction (see up-down direction labeled “hd2” in the figures above and below). See Pet., 67-68; Toyama, [0220]. And as Micron demonstrated (at Pet., 68-78), a skilled artisan would have

found it obvious to further repeat that same block layout in the “hd1” direction (see right-left direction labeled “hd1” in the figures above and below) as well—resulting in a structure with a TAC region between a first and second channel regions:



Pet., 86 (quoting Toyama, Fig. 17E (modified)).

Micron’s expert established that such a modification would have been obvious in light of the many, well-known benefits of multi-plane memory architecture: such as increased read throughput, increased write throughput, and optimized overall performance. Ex. 1003, ¶¶ 145-148; *see* Pet., 76-77. Moreover, since numerous prior art examples taught implementing multiple planes of memory in a 3D memory device, a skilled artisan would have had a reasonable expectation of success implementing that architecture in Toyama. Indeed, Micron’s expert testified that the proposed modification would have been a “straightforward exercise with predictable results.” Ex. 1003, ¶¶ 150-151; Pet., 76-77.

Based on the undisputed evidence and the Board's own factual findings, the Board should have determined that Ground 2 renders claim 8 obvious. YMTC never disputed that the memory device resulting from Micron's proposed modification satisfies every element of the challenged claims. And the Board's factual findings establish a motivation to modify Toyama as Micron proposed. The Board acknowledged both (1) that "there are certain advantages" to having multiple planes in a 3D memory device; and (2) that numerous prior art references teach implementation of a multi-plane memory array. FWD, 36. Indeed, Patent Owner had never disputed the benefits of multi-plane memory architecture or the fact that techniques for implementing that architecture were well known in the prior art. Ex. 1043, ¶ 23; *see* PO Sur-Reply, 23. Those undisputed factual findings require a finding of obviousness: "[I]f a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious." *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 393, 417 (Fed. Cir. 2007).

Yet the Board rejected this obviousness ground, holding that Micron had not provided sufficient evidence of a motivation to modify Toyama. FWD, 34, 37. In reaching this conclusion, the Board credited Patent Owner's argument that a skilled artisan would not repeat Toyama's First Exemplary Structure in the lateral hd1 direction because it would interfere with "peripheral circuitry" located to the left of

the memory array in Toyama’s First Exemplary Structure. FWD, 33-34 (citing PO Response, 30-36). The Board declined to consider or address Micron’s arguments in reply, which showed that a skilled artisan would have known to place this peripheral circuitry elsewhere, because “they were not set forth in the Petition.” FWD, 35. And in the alternative, the Board determined that, even if a skilled artisan “*could have*” modified Toyama as proposed, Micron had not shown that a skilled artisan “*would have been motivated* to do so.” FWD, 36-37. Every one of the Board’s justifications for its decision rests on legal error.

A. The Board Erroneously Required Bodily Incorporation.

To start, the Board erred in requiring Micron to demonstrate how a skilled artisan would have repeated Toyama’s First Exemplary Structure in the hd1 direction despite “the presence of [Toyama’s] interconnects and peripheral circuitry” to the left of the memory array. FWD, 34. The Federal Circuit has roundly rejected the notion that a petitioner must demonstrate how to “bodily incorporate” prior art teachings in a proposed combination. *See generally Elbrus Int’l Ltd. v. Samsung Elec. Co., Ltd.*, 738 F. App’x 694, 698-99 (Fed. Cir. 2018); *Laitram, LLC v. Ashworth Bros., Inc.*, Nos. 22-1044, 22-1045, 22-1084, 2023 WL 3449148, at *7 (Fed. Cir. May 15, 2023) (Board “applied the wrong legal standard” by requiring petitioner to “reconcile” physically incompatible elements of prior art references in proposed combination). As such, Micron had no obligation to demonstrate how a

skilled artisan would “bodily incorporate[e]” every aspect of Toyama’s First Exemplary Structure in the proposed modification—including its placement of peripheral circuitry to the left of the memory array. *Id.*; *see also Intel Corp. v. PACT XPP Schweiz AG*, No. 22-1038, 2023 WL 2198649, at *3 (Fed. Cir. Feb. 24, 2023) (Board erred in requiring petitioner to explain “*how* a [POSA] would have modified [the prior art] ... to *incorporate* [a second prior art teaching]” to establish obviousness). The question is instead whether “a skilled artisan would have been motivated to combine the teachings of the prior art references to achieve the claimed invention.” *Elbrus*, 738 F. App’x at 698 (quoting *Allied Erecting & Dismantling Co., Inc. v. Genesis Attachments, LLC*, 825 F.3d 1373, 1381 (Fed. Cir. 2016)). And as already discussed, the “advantages” of a multi-plane memory device (e.g., improved performance) would have supplied that motivation. *Supra* 5.

B. The Board Erroneously Disregarded Reply Arguments That Directly Refuted Patent Owner’s Operability Concerns.

Regardless, as Micron explained, a skilled artisan would not have blindly repeated Toyama’s memory array in the hd1 direction without accounting for peripheral circuitry that “any flash memory device needs.” Reply, 18. The “interaction of multiple components means that changing one component often requires that others be modified as well.” *KSR*, 550 U.S. at 421. And as a person of ordinary creativity—not an “automaton,” *id.*—a skilled artisan would have known to alter Toyama to “fit [the] pieces” of the proposed modification together, *Ethicon*

LLC v. Intuitive Surgical, Inc., No. 21-1995, 21-1997, 2022 WL 1613188, at *4 (Fed. Cir. May 23, 2022). Indeed, as Micron’s expert testified, placing peripheral circuitry in a multi-plane device was well within the capability of a skilled artisan. *See* Ex. 1043, ¶¶ 47, 54 (“[i]mplementing peripheral circuitry was highly routine”). And the prior art examples of multi-plane memory devices disclose multiple techniques for placing peripheral circuitry in devices with that architecture (such as above, below, and to the side of the multi-plane memory array). Ex. 1043, ¶¶ 48-55. In sum, the record plainly establishes that “any operability hurdles” in modifying Toyama to implement multiple planes “would be overcome by a person of ordinary skill.” *Elbrus*, 738 F. App’x at 699.

The Board abused its discretion in disregarding this evidence because it had not been “set forth in the Petition.” FWD, 35. A petitioner is permitted to “introduce new evidence after the petition stage if the evidence is a legitimate reply to evidence introduced by the patent owner.” *Rembrandt Diagnostics, LP v. Alere, Inc.*, 76 F.4th 1376, 1384 (Fed. Cir. 2023) (“[T]he very nature of the reply and sur-reply briefs are to respond (whether to refute, rebut, explain, discredit, and so on.)”; *see also Apple Inc. v. Andrea Elecs. Corp.*, 949 F.3d 697, 706-707 (Fed. Cir. 2020) (abuse of discretion to exclude reply arguments that “squarely respond[]” to patent owner’s brief). And that makes sense: Otherwise, a patent owner could defeat any claims of unpatentability simply by **raising** concerns about the operability of a proposed

modification or combination—even if, in reality, those “operability hurdles” are easily surmountable and do not undermine the skilled artisan’s reasonable expectation of success. *See Elbrus*, 738 F. App’x at 699; *infra* 13-15. Micron’s arguments and supporting evidence were properly set out in the reply because they directly refuted Patent Owner’s contention that the proposed modification “would not work” due to Toyama’s placement of peripheral circuitry. PO Resp., 33.

Moreover, the Board erred in suggesting that Micron should have somehow “preemptively addressed” Patent Owner’s concerns about the placement of peripheral circuitry in the petition. *Idemitsu Kosan Co., Ltd. v. SFC Co., Ltd.*, 870 F.3d 1376, 1380-81 (Fed. Cir. 2017); *see* FWD, 35. The Federal Circuit’s reasoning in *Idemitsu* squarely applies to this case: There, a patent owner “first raised” concerns about the operability of a proposed combination in its response brief, arguing that the combination lacked the “preferred energy gap relationship” that one of the prior art references disclosed. 870 F.3d at 1381. Although the petitioner refuted this argument on reply, the patent owner claimed that the counterargument arrived “too late” for the Board to consider it. *Id.* The Federal Circuit rejected the patent owner’s position as “plainly mistaken,” recognizing that a petitioner has no obligation to “anticipate and set forth every legal or factual issue that might arise in the course of the trial” in the petition. *Id.* at 1381 (quoting *Genzyme Therapeutic Prods. Ltd. P’ship v. Biomarin Pharm., Inc.*, 825 F.3d 1360, 1366 (Fed. Cir. 2016)).

Rather, a petitioner who makes out a *prima facie* case of obviousness is entitled to offer new evidence in reply “to show why a patent owner’s response is wrong in its criticisms of the petition’s case for unpatentability”—including where a patent owner raises concerns about whether a proposed combination would have a “reasonable expectation of success” or predictable result. *Sanofi Aventis Deutschland GmbH v. Mylan Pharms. Inc.*, 791 F. App’x 916, 925 (Fed. Cir. 2019). Because that is precisely what happened here, the Board abused its discretion.

C. The Board Required Evidence Of Anticipation Rather Than Obviousness.

In the alternative, the Board held that even if a skilled artisan “*could* have modified Toyama’s Figure 17E to repeat in the hd1 direction,” Micron had not established that a skilled artisan “would have done so.” FWD, 36-37. The Board thus completely ignored the fact that implementing multi-plane memory architecture in a 3D memory device provides numerous “advantages,” as the Board itself acknowledged. FWD, 36; *see* Ex. 1003, ¶¶ 145-148 (discussing advantages of increased read throughput, increased write throughput, and enhanced overall performance); *see* Pet., 76-77. Those advantages provide the requisite motivation to modify Toyama as Micron proposed. *See, e.g., KSR*, 550 U.S. at 424 (“motivation” to combine or modify satisfied where skilled artisan “would have seen a benefit”).

The Board erred in asserting that, to establish a motivation to modify, Micron needed evidence demonstrating that a “known NAND flash device similar to that of

Figure 17E” had already been modified “to implement multiple planes of that *particular device*.” FWD, 36 (emphasis added); *see id.* (faulting Micron for failing to provide evidence of “modifying the *particular structure shown [in] Toyama’s Figure 17E* to repeat in the hd1 direction”). As an initial matter, Micron made that showing. Micron demonstrated that one of the prior art examples of multi-plane memory architecture places peripheral circuitry “on one side of [its] memory planes”—just like Toyama does in the First Exemplary Structure. Ex. 1043, ¶ 52 (quoting Ex. 1024, 13:45-46). As discussed above, the Board erred in disregarding this evidence because it appeared in reply. *See supra* 8-10.

In any event, Micron had no obligation to identify a “prior art reference” that already “taught the claimed combination.” *Banner Eng’g Corp. v. Tri-Tronics Co., Inc.*, 11 F.3d 1071, 1993 WL 43283, at *3 (Fed. Cir. Oct. 27, 1993). Such a rule would inappropriately conflate anticipation and obviousness. *Id.* By contrast, obviousness does not require “precise teachings directed to the specific subject matter of the challenged claim.” *Intel Corp. v. PACT XPP Schweiz AG*, 61 F.4th 1373, 1380 (Fed. Cir. 2023). Rather, the question is whether a skilled artisan “*familiar*” with prior art examples of multi-plane memory devices and “*familiar*” with Toyama “would have found it obvious to make a structure corresponding to [the claimed invention].” *In re Sovish*, 769 F.2d 738, 742 (Fed. Cir. 1985). Given

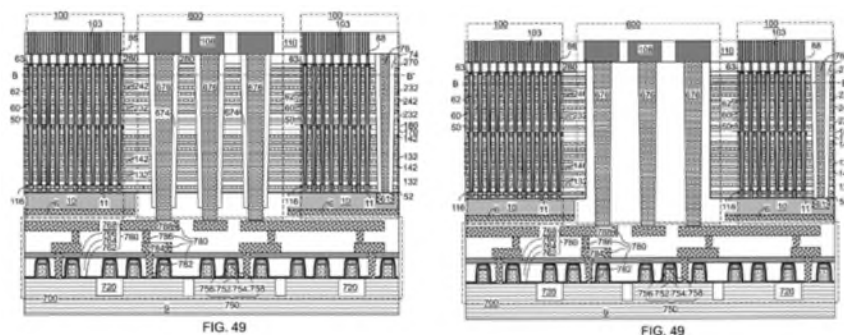
the undisputed “advantages” to implementing Toyama in a memory device with multiple planes, that standard is satisfied here. *KSR*, 550 U.S. at 424.

* * *

In sum, the Director should vacate or reverse in light of undisputed evidence establishing a motivation to modify Toyama as proposed. *See Google LLC v. Ji-Soo Lee*, 759 F. App’x 992, 996 (Fed. Cir. 2019).

III. THE BOARD ERRED IN ALLOWING PATENT OWNER’S CONCERNS ABOUT OPERABILITY TO DEFEAT MICRON’S SHOWING OF A MOTIVATION TO COMBINE IN GROUND 3.

Many of the same errors that the Board committed with respect to Ground 2 also led it to erroneously reject Ground 3. Micron established that every element of claim 8 is rendered obvious by a combination of Toyama’s Second Modification and First Exemplary Structure. *Pet.*, 96-120. Specifically, Micron demonstrated that a skilled artisan would have found it obvious to substitute the insulating liners 674 from the Second Modification (Toyama, Fig. 49) with the unitary dielectric fill material portion 430 of the First Exemplary Structure (Toyama, Fig. 15A), as shown:



Unmodified

Modified

Ex. 1003, ¶ 182 (modifying Toyama, Fig. 49); *see* Pet., 96-108. Micron demonstrated that a skilled artisan would have pursued this combination because it involves a simple substitution of one form of a dielectric structure for another—as each of these dielectric structures perform the function of electrically isolating through-array contacts (TACs) from conductive material in Toyama’s First Exemplary Structure and Second Modification, respectively. *See* Pet., 100; Ex. 1003, ¶ 182; *see KSR*, 550 U.S. at 417 (“simple substitution of one element for another” is obvious). Micron also established that a skilled artisan would have had a reasonable expectation of success in making the proposed combination, and that it would have yielded predictable results. Pet., 104-108; Ex. 1003, ¶¶ 190-197.

The Board rejected Ground 3 solely because Patent Owner raised concerns about operability hurdles in Patent Owner’s response brief. The Board relied on Patent Owner’s arguments that the proposed combination would inhibit Toyama’s gate replacement process by removing sacrificial layers and inhibit current flow by removing conductive layers that form word lines. FWD, 43; *see* PO Response, 37-46. The Board then once again declined to consider *any* of the arguments or evidence Micron provided in reply because it had not been “set forth in the petition,” FWD, 45—even though Micron’s reply arguments and evidence established that none of these so-called operability hurdles would actually inhibit performance or discourage a skilled artisan from making the proposed combination, *see* Reply, 21-

28; Ex. 1043, ¶¶ 61-79. And finally, without making any finding that Patent Owner’s concerns would actually undermine the operability of the proposed combination, the Board held that the “potential hazards” that Patent Owner had raised precluded Micron from demonstrating that its proposed combination would have been obvious. FWD, 44-45 (quoting *Arctic Cat, Inc. v. Bombadier Recreational Prods., Inc.*, 876 F.3d 1350, 1363-64 (Fed. Cir. 2017)).

Again, the Board erred in allowing Patent Owner to avoid a finding of obviousness by doing nothing more than *suggest* that the proposed combination would pose operability hurdles. The Board had an obligation to address and consider the responsive arguments Micron made in reply that soundly refuted Patent Owner’s concerns about operability. *See supra* 8-9; *Apple*, 949 F.3d at 706-07 (Fed. Cir. 2020) (abuse of discretion to exclude “reply arguments ... responsive to arguments raised in the patent owner’s brief”). And again, the Board erred in faulting Micron for failing to preempt Patent Owner’s arguments in the petition. *See supra* 9-10; *Sanofi Aventis*, 791 F. App’x at 925. Micron’s petition made a *prima facie* case for obviousness, and as such, Micron was entitled to address Patent Owner’s “criticisms of the sufficiency of the petition’s case for unpatentability in reply”—including with new evidence refuting Patent Owner’s contention that operability hurdles would discourage the proposed combination. *Id.*; *see supra* 9-10.

The Board also never assessed or made factual findings regarding whether or not a skilled artisan would have understood that replacing one of Toyama’s dielectric structures with another would have predictable results. Given the Board’s failure to make any such inquiry, the Board’s determination that Micron’s proposed combination does not constitute a “simple substitution of known elements to achieve a known result” is utterly unsupported. FWD, 45. And *Arctic Cat* does not support the Board’s conclusion either. There, the Court upheld a jury’s finding of no motivation to combine based on (1) a prior art reference that explicitly cautioned against the proposed combination because it would be “difficult to predict” the frequency of “potential hazards”; and (2) testimony that expressed “surprise” about how the combination functioned. 876 F.3d at 1362-63. The Court thus upheld the jury’s finding that the proposed combination “would not have been a predictable solution yielding expected results.” *Id.* at 1363. The Court never held that any “potential hazards”—let alone those merely raised by a patent owner in a response brief—could preclude a finding of obviousness. In sum, the Director should vacate the Board’s decision and remand.

IV. CONCLUSION

For the reasons stated above, the Board’s final written decision finding claims 8-9 and 11-12 of the ’806 patent not unpatentable must be reversed or vacated.

Respectfully submitted,

ORRICK, HERRINGTON & SUTCLIFFE LLP

Dated: February 4, 2026

/Jeremy Jason Lang/

Jeremy Jason Lang
Lead Counsel for Petitioner
Reg. No. 73,604
1000 Marsh Road
Menlo Park, CA 94025-1015
T: (650) 614-7400
F: (650) 614-7401
Email: PTABDocketJL2@orrick.com

*Attorneys for Petitioner Micron
Technology, Inc.*

CERTIFICATE OF SERVICE

The undersigned hereby confirms that the foregoing paper was caused to be served on February 4, 2026 via electronic mail, upon the following attorneys of record for the Patent Owner:

Heather E. Takahashi (heather.takahashi@mto.com)

Andrew T. Radsch (andrew.radsch@mto.com)

Kevin Yang (kevin.yang@mto.com)

YMTC-Micron-IPRs-MTOService@mto.com

/Karen Johnson/

Karen Johnson