UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,
Patent Owner

Case No.: IPR2024-00792
U.S. Patent No. 11,468,957
Issue Date: October 11, 2022

Title: ARCHITECTURE AND METHOD FOR NAND MEMORY OPERATION

PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 11,468,957 PURSUANT TO 35 U.S.C. §§311-319 and 37 C.F.R. §42

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4. [1.A.ii] "apply, in the pre-verify stage, a first bias voltage on a gate terminal of at least one memory cell of the first memory cell string that is not programmed;" 33
5. [1.A.iii] "apply, in a verify stage, a second verify voltage on the gate terminal of the selected memory cell of the first memory cell string; and" 36
6. [1.A.iv] "apply, in the verify stage, a second bias voltage on the gate terminal of the at least one memory cell of the first memory cell string that is not programmed, wherein the second bias voltage is smaller than the first bias voltage." 39
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LISTING OF EXHIBITS

Exhibit	Description
1001	U.S. Patent No. 11,468,957 B2 to Lee et al.
1002	File History of U.S. Patent No. 11,468,957 to Lee et al.
1003	Declaration of David Kuan-Yu Liu, Ph.D.
1004	*Curriculum Vitae* of David Kuan-Yu Liu, Ph.D.
1005	Chinese Patent Publ. No. 109065091 A to Hongtao Liu et al. (certified translation and original) ("Hongtao")
1006	U.S. Patent Publ. No. 2019/0198117 A1 to Yu et al. ("Yu")
1007	U.S. Patent Publ. No. 2021/0082505 A1 to Suzuki ("Suzuki")
1008	U.S. Patent Publ. No. 2018/0012667 A1 to Costa ("Costa")
1009	U.S. Patent Publ. No. 2021/0027848 A1 to Seo ("Seo")
1010	Minute Order, Dkt. No. 42, dated February 22, 2024 in *Yangtze Memory Technologies Company, Ltd. V. Micron Technology, Inc. and Micron Consumer Products Group, LLC*, Case No. 3:23-cv-05792-RFL
1011	Combined Civil and Criminal Federal Court Management Statistics (December 31, 2023), available at https://www.uscourts.gov/sites/default/files/data_tables/fcms_na_distcomparison1231.2023.pdf
1012	Docket from *Yangtze Memory Technologies Company, Ltd. V. Micron Technology, Inc. and Micron Consumer Products Group, LLC*, Case No. 3:23-cv-05792-RFL
1013	U.S. Patent No. 9,589,978 B1 to Yip
1014	Aritome, "NAND Flash Memory Technologies" (2016)
1015	Silvagni, "3D NAND Flash Based on Planar Cells," Computers 2017

Exhibit	Description
1016	U.S. Patent Publ. No. 2020/0168276 A1 to Yang
1017	U.S. Patent No. 9,620,233 B1 to Dong et al.
1018	Micheloni, "3D Flash Memories" (2016)
1019	U.S Patent No. 9,361,993 B1 to Chen et al.
1020	U.S Patent No. 10,276,251 B1 to Lobana et al.
1021	U.S. Patent Publ. No. 2019/0348122 A1 to Ko et al.
1022	U.S. Patent Publ. No. 2013/0077404 A1 to Nawata et al.
1023	U.S Patent No. 10,121,529 B2 to Lee
1024	U.S. Patent Publ. No. 2016/0293271 A1 to Won et al.
1025	U.S. Patent No. 11,600,342 to Chen et al.

LISTING OF CHALLENGED CLAIMS

Ref. #	Listing of Challenged Claims
Claim 1:	
[1.PRE]	An apparatus for reading a memory device including a first memory cell string and a second memory cell string, the first memory cell string including a bottom-select-gate (BSG) transistor, memory cells, and a top-select-gate (TSG) transistor that are connected in series, the second memory cells string including a BSG transistor, memory cells, and a TSG transistor that are connected in series, the apparatus comprising:
[1.A]	processing circuitry configured to:
[1.A.i]	apply, in a pre-verify stage, a first verify voltage on a gate terminal of a selected memory cell of the first memory cell string, the selected memory cell being programmed and arranged between a first adjacent memory cell and a second adjacent memory cell;
[1.A.ii]	apply, in the pre-verify stage, a first bias voltage on a gate terminal of at least one memory cell of the first memory cell string that is not programmed;
[1.A.iii]	apply, in a verify stage, a second verify voltage on the gate terminal of the selected memory cell of the first memory cell string; and
[1.A.iv]	apply, in the verify stage, a second bias voltage on the gate terminal of the at least one memory cell of the first memory cell string that is not programmed, wherein the second bias voltage is smaller than the first bias voltage.
Claim 2:	
[2]	The apparatus of claim 1, wherein the at least one memory cell of the first memory cell string that receives the first bias voltage and the second bias voltage is positioned between the first adjacent memory cell of the selected memory cell and the TSG transistor of the first memory cell string.

Ref. #	Listing of Challenged Claims
Claim 3:	
[3]	The apparatus of claim 1, wherein the at least one memory cell of the first memory cell string that receives the first bias voltage and the second bias voltage is positioned between the second adjacent memory cell of the selected memory cell and the BSG transistor of the first memory cell string.
Claim 4:	
[4.PRE]	The apparatus of claim 1, wherein the processing circuitry is further configured to:
[4.A]	in the pre-verify stage,
[4.A.i]	apply a first gate voltage on a gate terminal of the TSG transistor of the second memory cell string,
[4.A.ii]	apply a first pass voltage on a gate terminal of the first adjacent memory cell of the selected memory cell in the first memory cell string, and
[4.A.iii]	apply a first read voltage on a gate terminal of the second adjacent memory cell of the selected memory cell in the first memory cell string; and
[4.B]	in the verify stage,
[4.B.i]	apply a second gate voltage on the gate terminal of the TSG transistor of the second memory cell string,
[4.B.ii]	apply a second pass voltage on the gate terminal of the first adjacent memory cell of the selected memory cell in the first memory cell string, and
[4.B.iii]	apply a second read voltage on the gate terminal of the second adjacent memory cell of the selected memory cell of the first memory cell string, wherein

Ref. #	Listing of Challenged Claims
[4.C]	at least one of the second pass voltage and the second read voltage is larger than the second gate voltage.
Claim 5:	
[5.PRE]	The apparatus of claim 2, wherein the processing circuitry is further configured to:
[5.A]	apply a bottom bias voltage on a gate terminal of the BSG transistor of the first memory cell string in the pre-verify stage and the verify stage;
[5.B]	apply a top bias voltage on a gate terminal of the TSG transistor of the first memory cell string in the pre-verify stage and the verify stage; and
[5.C]	apply a positive voltage on gate terminals of any memory cells that are positioned between the second adjacent memory cell of the selected memory cell and the BSG transistor of the first memory cell string in the pre-verify stage and the verify stage.
Claim 6:	
[6.PRE]	The apparatus of claim 3, wherein the processing circuitry is further configured to:
[6.A]	apply a bottom bias voltage on a gate terminal of the BSG transistor of the first memory cell string in the pre-verify stage and the verify stage;
[6.B]	apply a top bias voltage on a gate terminal of the TSG transistor of the first memory cell string in the pre-verify stage and the verify stage; and
[6.C]	apply a positive voltage on gate terminals of any memory cells that are positioned between the first adjacent memory cell of the selected memory cell and the TSG transistor of the first memory cell string in the pre-verify stage and the verify stage.

I. INTRODUCTION

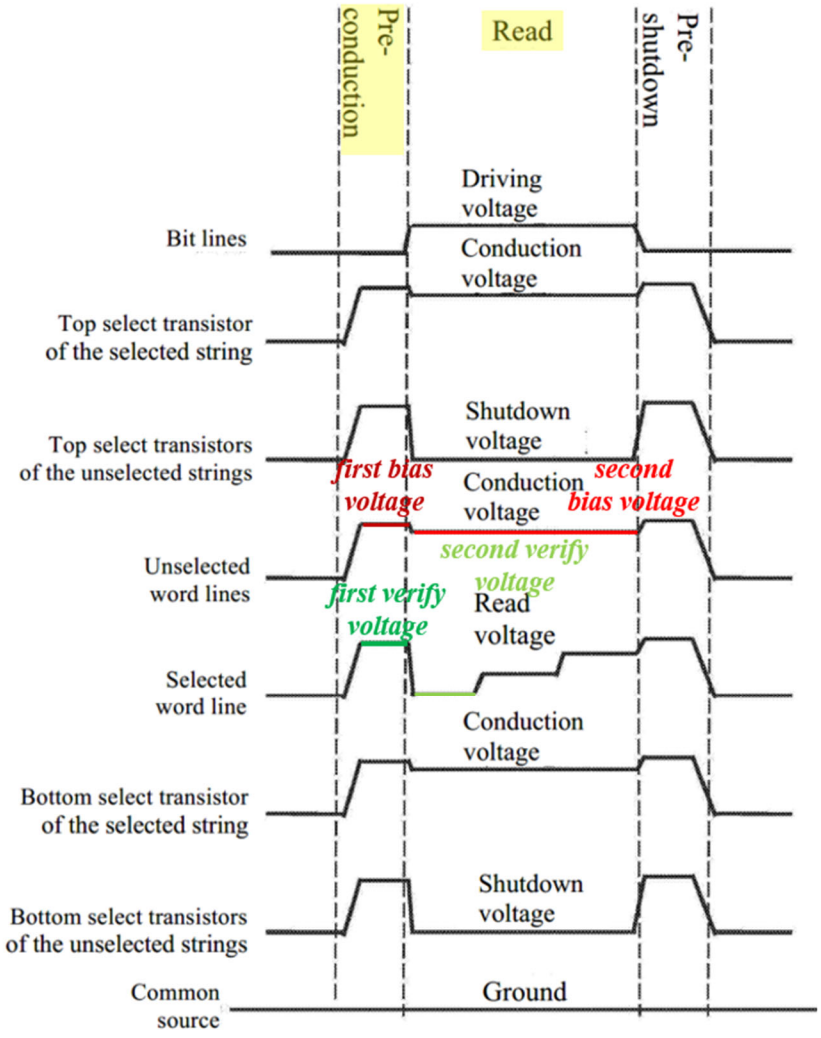
Petitioner respectfully requests *inter partes* review of claims 1-6 ("Challenged Claims") of U.S. Patent No. 11,468,957 ("the '957 patent") assigned to Yangtze Memory Technologies Co., Ltd. ("Patent Owner" or "PO"). There is more than a reasonable likelihood that Petitioner will prevail with respect to at least one Challenged Claim.

In the context of 3D NAND, the '957 patent relates to a read operation that verifies the success of a program operation. Claim 1 recites applying voltages on a selected memory cell (via a gate terminal) and an unprogrammed memory cell (via a gate terminal) in a pre-verify stage and a verify stage. The selected memory cell need only receive a first verify voltage and a second verify voltage in the two stages, respectively. But the claim specifies that the unprogrammed memory cell must receive a first and a second bias voltage in the two stages, respectively, wherein the second bias voltage is less than the first bias voltage.

This voltage scheme, however, was nothing new. Prior art references that the Examiner did not consider make clear that the scheme is obvious.

Ground 1 focuses on Hongtao—assigned to Patent Owner but never disclosed during the prosecution of the '957 patent—describes this exact voltage sequence. Ground 1 combines Hongtao with Yu to demonstrate that it would have been obvious for Hongtao's read operation to be used for verification and that Hongtao's

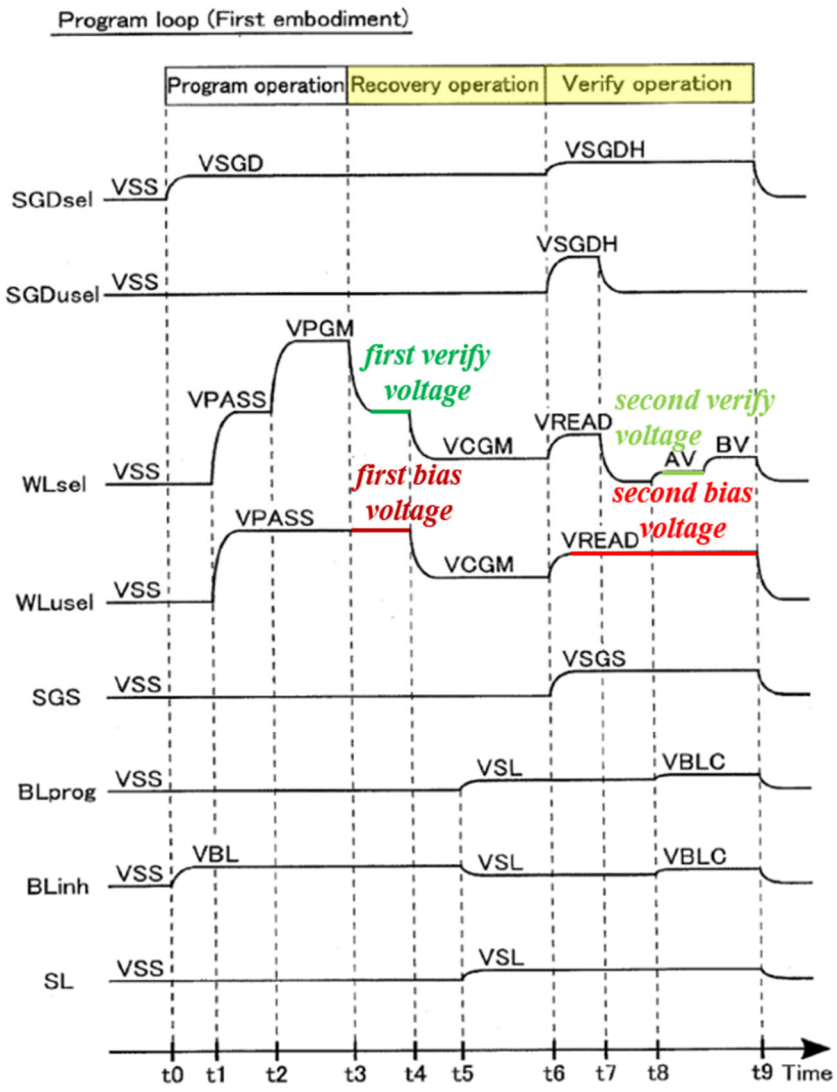
programming would occur in sequential order such that there would be unprogrammed memory cells. Hongtao's relevant waveforms are below:



Hongtao, Fig. 2.[1]

Ground 2 relies on Suzuki as an anticipatory reference. It, too, discloses this exact voltage sequence:

[1] All colored annotations in figures herein are added.



Suzuki, Fig. 11.

Ground 3 combines Costa, which discloses the voltages for the verify stage, and Seo, which discloses the pre-verify voltages. Seo teaches the benefits of a high voltage on the unprogrammed cells during pre-verify. Costa teaches the benefits of using a low voltage on unprogrammed cells during verify.

Dependent claims add trivial limitations that each Ground discloses or renders obvious.

Because the Challenged Claims are directed to nothing new, and to nothing more than a routine, predictable combination of known elements, Petitioner requests that the Board institute trial and find the Challenged Claims unpatentable.

II. MANDATORY NOTICES

A. Real Party-in-Interest

Petitioner Micron Technology, Inc. and its subsidiaries, including Micron Consumer Products Group LLC, are the real parties-in-interest.

B. Related Matters

PO has asserted the '957 patent and U.S. Patent Nos. 10,658,378, 10,861,872, 10,868,031, 10,937,806, 10,950,623, 11,468,957, 11,501,822, and 11,600,342 in a co-pending litigation, *Yangtze Memory Technologies Co., Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC*, Case No. 3:23-cv-05792-RFL (N.D. Cal., filed Nov. 9, 2023) ("Co-Pending Litigation").

In addition to this Petition, Petitioner is filing (or has filed) petitions for *inter partes* review of each of the asserted patents in the Co-Pending Litigation: Petition for *Inter Partes* Review of U.S. Patent No. 10,658,378, IPR2024-00788, Petition for *Inter Partes* Review of U.S. Patent No. 10,861,872, IPR2024-00789, Petition for *Inter Partes* Review of U.S. Patent No. 10,868,031, IPR2024-00790, Petition for *Inter Partes* Review of U.S. Patent No. 10,937,806, IPR2024-00791, Petition for *Inter Partes* Review of U.S. Patent No. 10,950,623, IPR2024-00794, Petition for

Inter Partes Review of U.S. Patent No. 11,501,822, IPR2024-00795, and Petition for *Inter Partes* Review of U.S. Patent No. 11,600,342, IPR2024-00793.

C. Counsel, Service, and Fee Information

Pursuant to 37 C.F.R. §§42.8(b)(3)-(4) and 42.10(a), Petitioner provides the following designation of lead and back-up counsel.

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The Director is authorized to charge the fee specified by 37 C.F.R. §42.15(a), and any other required fees, to Deposit Account No. 15-0665.

III. REQUIREMENTS FOR IPR

A. Grounds for Standing

Petitioner certifies that the '957 patent is available for IPR; Petitioner is not barred or estopped from requesting this IPR. Micron was served with a Complaint alleging infringement of the '957 patent on November 14, 2023.

B. Identification of Challenged Claims and Statement of Precise Relief Requested

This Petition assumes that the '957 patent has the earliest listed priority date: December 15, 2020. Ex. 1001, Cover.

Petitioner relies on the following references: (1) Chinese Patent Publ. No. 109065091 A ("Hongtao"), (2) U.S. Patent Publ. No. 2019/0198117 A1 ("Yu"), (3) U.S. Patent Publ. No. 2021/0082505 A1 ("Suzuki"), (4) U.S. Patent Publ. No. 2018/0012667 A1 ("Costa"), and (5) U.S. Patent Publ. No. 2021/0027848 A1

("Seo"). These references are all prior art. *Infra* §VIII. The Examiner did not consider or discuss any of these references.

Petitioner advances the following grounds:

Ground 1: Claims 1–6 are obvious over Hongtao in view of Yu;

Ground 2: Claims 1–6 are anticipated by Suzuki; and

Ground 3: Claims 1–6 are obvious over Costa in view of Seo.

IV. INSTITUTION SHOULD BE GRANTED

Petitioner has established a reasonable likelihood of success on the merits. All other requirements for IPR have been met. The Board should institute IPR.

A. There Are No Grounds for a §314 Discretionary Denial in this Case

There is a pending district court action involving the '957 Patent. Petitioner submits that it presents a compelling case, and thus the Board should not discretionarily deny. 6/21/22 Interim Procedure, 2, 4-5.

Further, the *Fintiv* factors weigh in favor of institution. *See Apple Inc. v. Fintiv, Inc.*, Case No. IPR2020-00019, Paper No. 11 (Mar. 20, 2020) (precedential) ("*Fintiv*").

1. Possibility of a Stay

Petitioner intends to seek a stay if the Board institutes IPR. This factor is neutral. *See Sand Revolution II, LLC v. Continental Intermodal Group – Trucking LLC*, IPR2019-01393, Paper 24 at 7 (PTAB June 16, 2020) (informative) ("*Sand*

Revolution").

2. Proximity of the Court's Trial Date

Trial is set for December 1, 2025. *See* Ex. 1010. If instituted, the IPR should conclude before the scheduled trial date. *See also* Ex. 1011 (statistics indicating an average 48.9 months for time-to-trial in the district). This weighs strongly in favor of institution.

3. Investment in the Parallel Proceeding

To date, the parties and Court have invested very little. Beyond motion practice over the pleadings, no substantive progress has been made. The parties are months away from completing the exchange of infringement and invalidity contentions and have not taken any depositions. Fact discovery is in its infancy. Claim construction and expert discovery has yet to begin. This weighs in favor of institution. *See Sand Revolution*, 1.

The Board also has explained that institution is appropriate where "the petitioner filed the petition expeditiously…." *Fintiv*, 11. Against 8 patents, Petitioner proceeded with diligence, filing approximately 5 ½ months after being served with the original complaint and approximately 3 months after the filing of an amended complaint. *See* Ex. 1012. This also weighs strongly in favor of institution.

4. Issue Overlap

Given the early stage of the parallel proceeding, it is not yet possible to determine the amount of overlap. Regardless, should the Board institute, Petitioner

stipulates that it will not advance in District Court any invalidity defense that formed the basis of any of the grounds in this Petition. Micron submits that this eliminates any potential overlap in issues between the proceedings here and in District Court. The Board has found that such stipulations weigh in favor of institution. *Sand Revolution* at 11-12.

5. Party Overlap

Both Petitioner and Patent Owner are parties in the parallel proceeding.

6. Other Circumstances

Here, Petitioner submits that its petition has significant substantive merit, which is based on prior art that the Patent Office did not previously consider. Thus, this factor also weighs in favor of institution.

B. Denial Under §325(d) Would Be Inappropriate

Neither Patent Owner nor the Examiner cited or discussed Hongtao, Yu, Suzuki, Costa, or Seo during prosecution of the '957 patent. Ex. 1002. Indeed, the Examiner issued no prior-art rejections. *Id.* Thus, these references present noncumulative invalidity arguments.

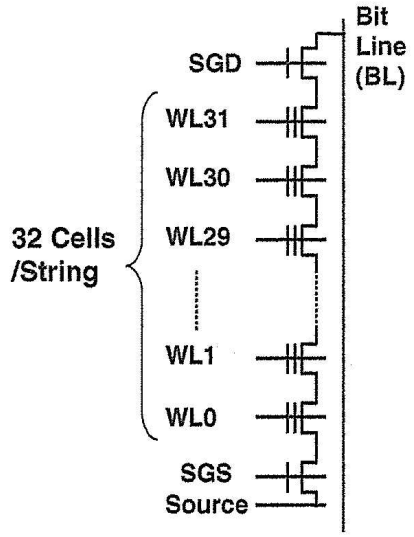
V. THE '957 PATENT

A. Technology Background

1. 3D NAND Flash Structure

Flash memory cells, e.g., NAND cells, are arranged in "strings" with multiple cells "connected in series." Ex. 1014, 38. The cells are surrounded by "select

transistors (SGD, SGS)," one on the top (usually, drain side) and one on the bottom (usually, source side). *Id.*, 38-39. One such string is shown below:

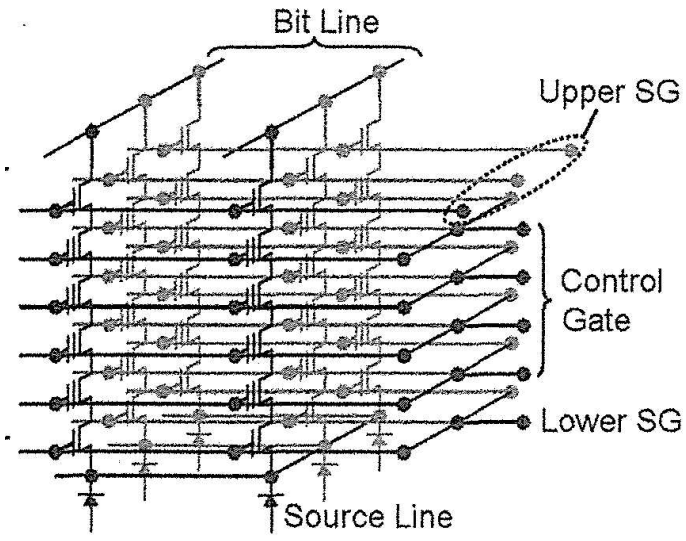


Id., 39; *see also* Liu [2], ¶ 41.

Early NAND devices were formed as two-dimensional arrays of cells on a substrate surface. Ex. 1014, 38. But "three-dimensional (3D) NAND flash cells" were developed. *Id.*, 292. Conceptually, "turning the 2D NAND string upside," results in a "3D structure" with a "vertical channel." Ex. 1015, 3. Memory cells (comprising transistors) are formed vertically by stacking alternating layers of metal and dielectric (e.g., oxide such as SiO_2) around a cylindrical pillar. Ex. 1014, 294-95. Each metal layer acts as the control gate (gate terminal) of a transistor. *Id.*, 295.

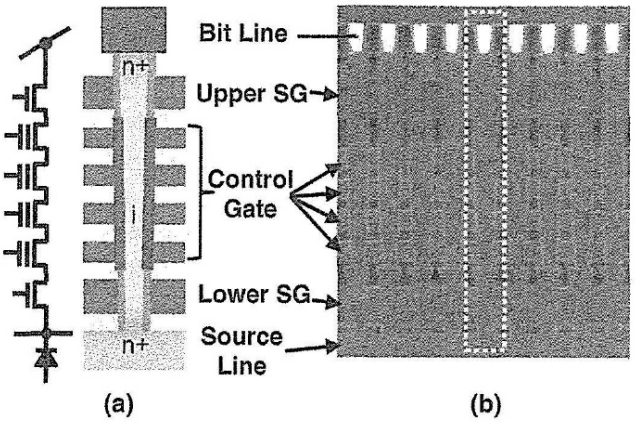
[2] David Kuan-Yu Liu, Ph.D. is a leading expert in the physics of read and interference issues in memories. Liu, ¶¶ 5-14.

Multiple such vertical pillars/channels are then repeated in a three-dimensional array:



Id., 296. A particular vertical memory cell is selected using a word line and bit line, along with the select gates. *Id.*, 295-97; Liu, ¶ 42.

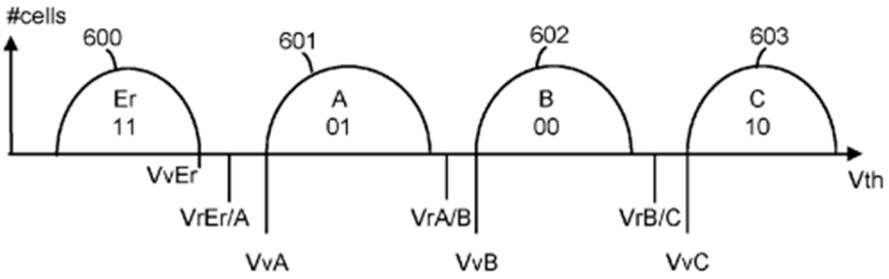
An example 3D NAND vertical memory cell string with a charge-trapping layer is shown below:



Ex. 1014, 296. The two most common types of 3D Flash memory cells are conductive floating gate memory cells and charge-trap memory cells. Ex. 1018, 145; Liu, ¶¶ 43-44.

2. 3D NAND Flash Operation

A memory cell is programmed to store a data state by storing some amount of charge in its charge-storage material. The threshold voltage (Vth) at which the cell transistor turns on increases "in proportion to the amount of stored charge." Ex. 1017, 13:43-49. A two-bit-per-cell NAND memory may have a Vth-versus-data-state distribution illustrated below:



Id., Fig. 6; *see also* Ex. 1014, 342-44 (Fig. 7.77 showing same). Unprogrammed cells have the erased Er state and a low (typically negative) Vth. Ex. 1017, 14:11-12; Liu, ¶ 45.

During read operations, all cell transistors on a selected memory string—except the selected cell to be read—can be given a pass voltage that is higher than the highest Vth of all possible data states to render the transistors conductive. Ex. 1017, 3:21-27, 3:33-37. A read voltage between two data states is applied to the control gate of the selected cell to determine (read) its data state. *Id.*, 3:10-29, 9:66-10:15, 14:31-37; Liu, ¶ 46.

NAND device programming involves a cycle of two steps: a programming operation and a read (also known as verify) operation. The programming operation is typically done via incremental step pulse programming ("ISPP"). ISPP involves applying a voltage pulse to a control gate of the selected word line. *See e.g.*, Ex. 1019, 11:47-49. Then, a read (verify) operation may be performed after the programming operation to verify whether the pulse was successful. Ex. 1020, 10:43-47; Ex. 1019, 11:50-52; Ex. 1017, 10:47-49. This verify operation can be identical

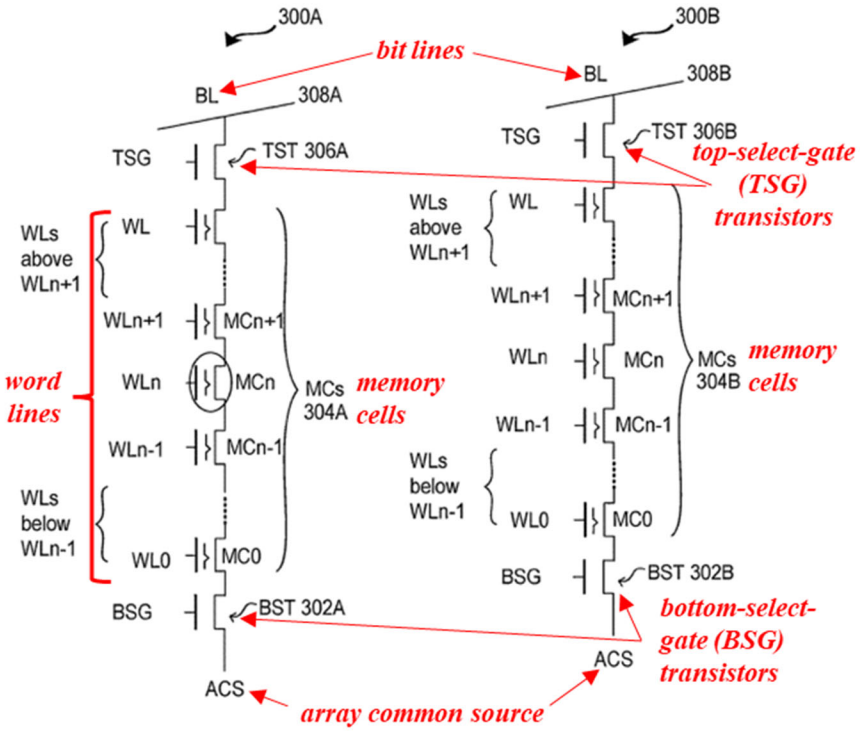
to the read operation described above (using a verify voltage). Ex. 1021, [0103]; Ex. 1020, 16:16-21; Ex. 1019, 17:10-14; Ex. 1017, 3:21-29. ISPP will stop if the verify operation confirms success or may continue if additional pulses are necessary. Ex. 1019, 11:27-32; Liu, ¶ 47.

Cells on a memory string are typically programmed from one end to the other, i.e., from source side to drain side, or vice versa. Ex. 1014, 45 (Fig. 2.12); Ex. 1021, [0110]-[0112].

Data storage using NAND flash is subject to various influences, such as data-retention degradation and read disturb, that reduce its reliability. Ex. 1014, 28. Read disturb can occur when read operations repeatedly apply high pass voltages on unselected word lines, which induces a boosting effect called hot-carrier injection ("HCI"). *Id.*, 254; Costa, [0096]; Liu, ¶ 48.

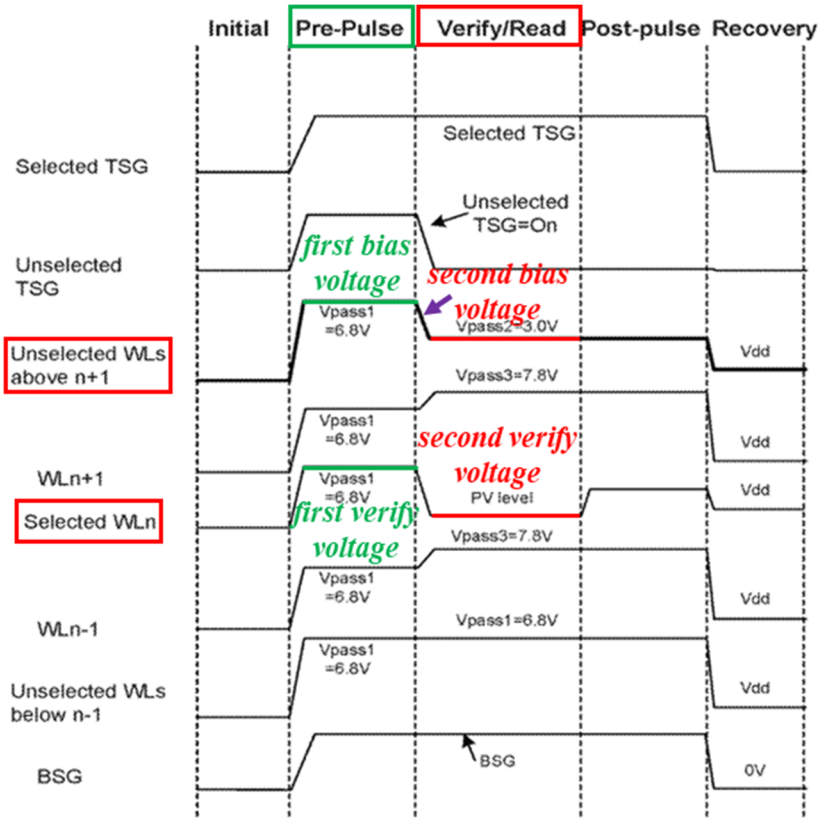
B. Overview of the Patent

The '957 patent's alleged objective is to reduce HCI (read disturb) on 3D NAND flash devices by including a pre-verify stage (a stage before the verify operation). Ex. 1001, 1:44-49, 17:7-17; Liu, ¶ 51. None of the patent's claims, however, are limited to this purported objective. The '957 patent comprises conventional NAND memory cell strings:



Ex. 1001, Fig. 3, 9:3-30; Liu, ¶ 52.

Verify and bias voltages are applied to a selected cell and to an unprogrammed cell, respectively, during a pre-verify (or pre-pulse) stage and a verify (or read) stage, wherein the bias voltage on the unprogrammed cell in the verify stage is lower than the voltage in the pre-verify stage, as indicated by a purple arrow below. Ex. 1001, Abstract, 6:50-7:12, 12:63-13:4, 14:19-30, 15:18-30.



Id., Fig. 6. In embodiments, the first and second bias voltages and the first verify voltage are set sufficiently high to turn on the corresponding cells. *Id.*, 11:12-15. The second verify voltage is set to "program verify (PV) level" to measure the cell's threshold value. *Id.*, 11:35-39; Liu, ¶¶ 53-55.

Claims 1 and 4-6 repeatedly recite "apply[ing]" a voltage "on a gate terminal" of a memory cell or a top-select-gate ("TSG") or bottom-select-gate ("BSG") transistor. Ex. 1001, 17:41-56, 18:13-30, 18:35-45, 18:48-58. The respective voltage is applied through a word line coupled to a corresponding memory cell. The voltage applied to the gate terminal controls the cell (transistor), e.g., to turn it on or off. Liu, ¶ 56.

C. Prosecution History

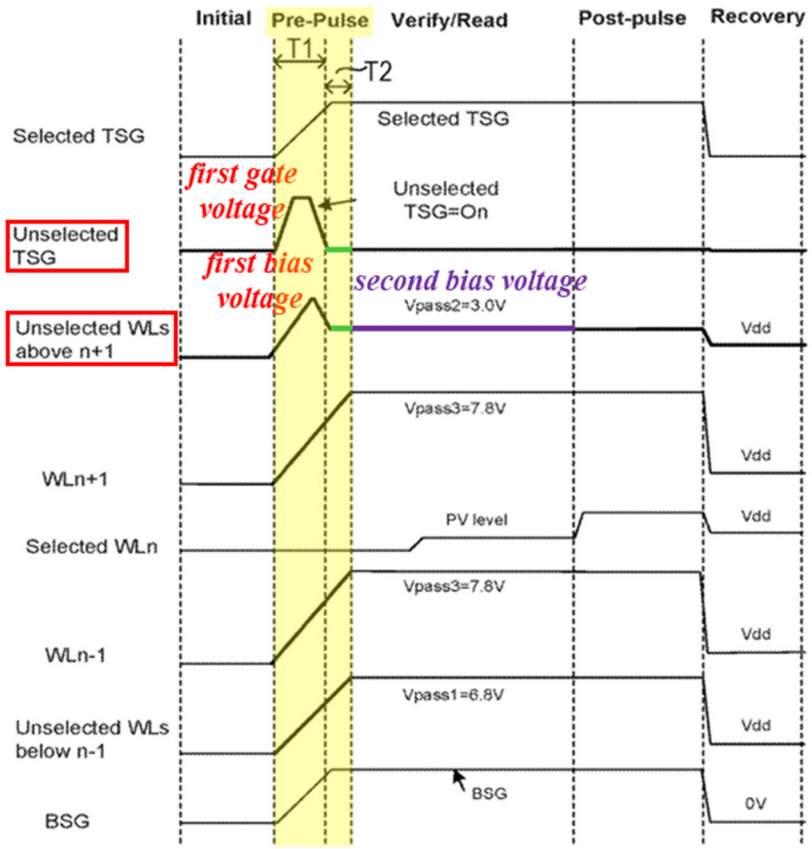
The '957 patent was filed on March 4, 2021, and claims priority to December 15, 2020 (via a PCT application). Ex. 1001, Cover.

After only a restriction/election requirement rejection and election of claims 15-20 (now claims 1-6), the claims were allowed. Ex. 1002, 212-217, 220-221.

VI. CLAIM CONSTRUCTION

The Board applies the same Phillips claim construction standard used by district courts. *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (*en banc*). For purposes of this Petition, Petitioner submits that no express constructions are necessary, and the claim terms can be afforded their plain and ordinary meaning. The below, however, addresses the scope of one term.

The claims recite "apply[ing]" voltages "in" a "pre-verify" and/or "verify stage." Consistent with the plain and ordinary meaning, the '957 patent makes clear that the claims do not require applying these voltages throughout the given stage. For example, as recited in claims 1 and 4 and as can be seen below, the first bias voltage and the first gate voltage are not applied throughout the pre-pulse (pre-verify) stage:



Ex. 1001, Fig. 7, 13:11-25, 17:32-42. As also can be observed from the figure, claim 1's limitation that "the second bias voltage is smaller than the first bias voltage" does not require the second bias voltage during the verify stage to be smaller than the first bias voltage for the entire duration of the pre-verify stage. Liu, ¶¶ 63-65.

VII. LEVEL OF ORDINARY SKILL IN THE ART

A POSITA in the field of the '957 patent would have had a master's degree in electrical engineering or a similar discipline, along with 4-5 years of professional experience working with (e.g., researching, designing, or developing) NAND flash memory devices (including issues relating to the operation, e.g., reading of said

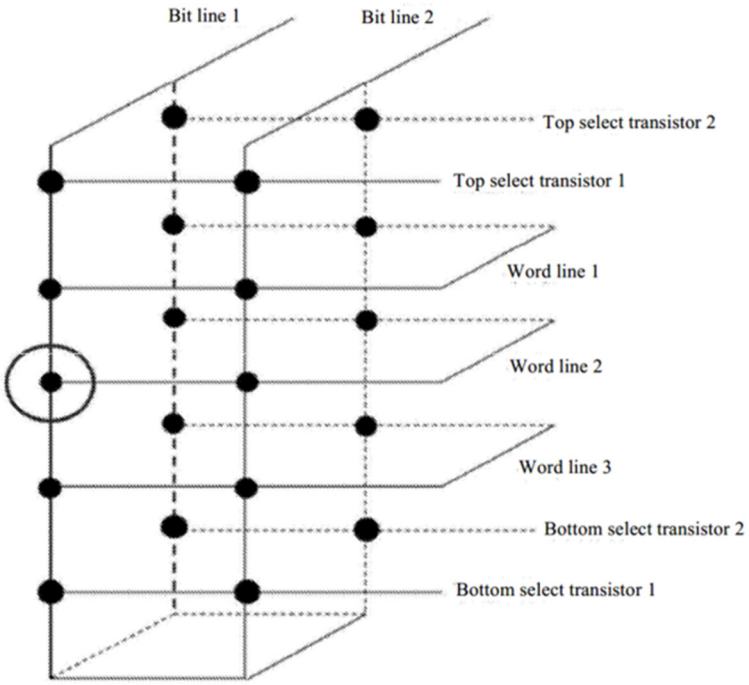
devices), or an equivalent level of skill, knowledge, and experience (e.g., an advanced degree may replace some of the professional experience). Liu, ¶¶ 35-39.

VIII. PRIOR ART OVERVIEW

A. Hongtao

Chinese Patent Publ. No. 109065091A ("Hongtao") was filed on August 1, 2018, and was published on December 21, 2018. Hongtao, Cover. Assigned to Patent Owner but never disclosed during prosecution of the '957 patent, Hongtao is prior art to the '957 patent under 35 U.S.C. §102(a)(1) (AIA).

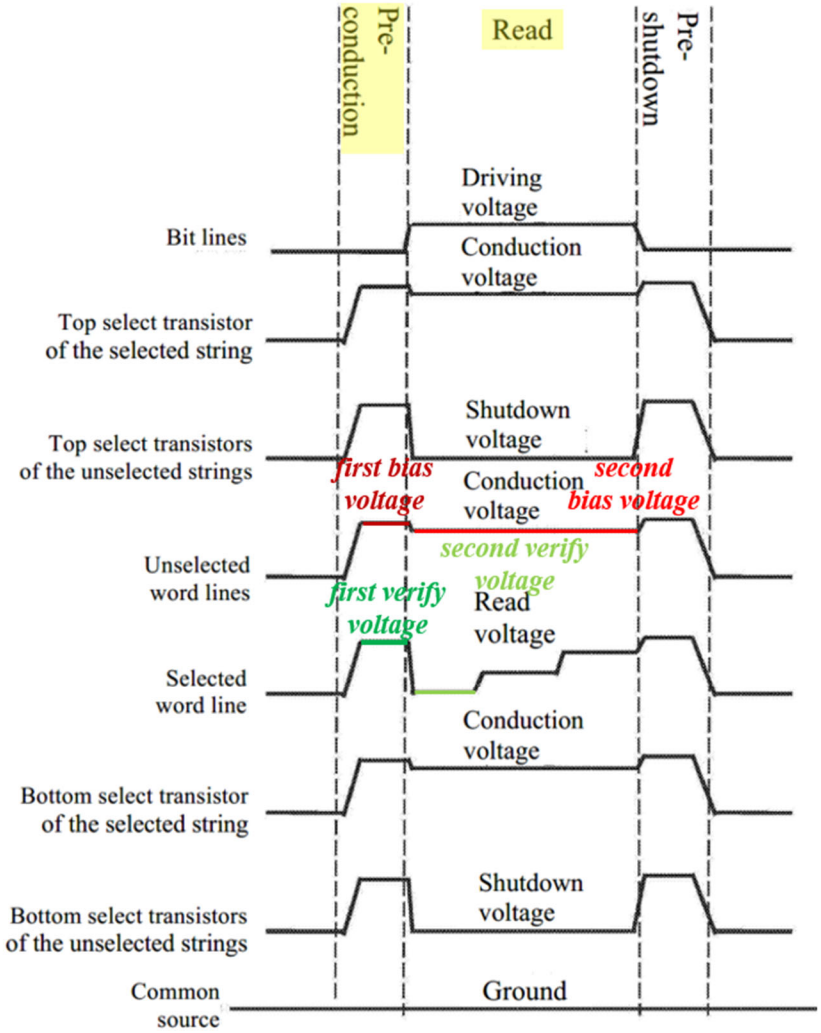
Hongtao is directed to read operations of 3D NAND flash memory. Hongtao, Abstract, [0001].



Id., Fig. 1. Like the '957 patent, Hongtao's memory devices comprise memory strings with conventional elements. *See id.*

Hongtao relates to reducing HCI. Hongtao, [0003]-[0004], [0020], [0023]; §V.A.2. Hongtao's solution comprises two parts.

Specifically, just like the '957 patent, Hongtao discloses two stages: a "pre-conduction phase" and a "read phase." The channels of unselected strings and the selected string are pre-conditioned to 0V during the pre-conduction phase. Hongtao, [0022]-[0024]. This is accomplished using waveforms that match the '957 patent claims:



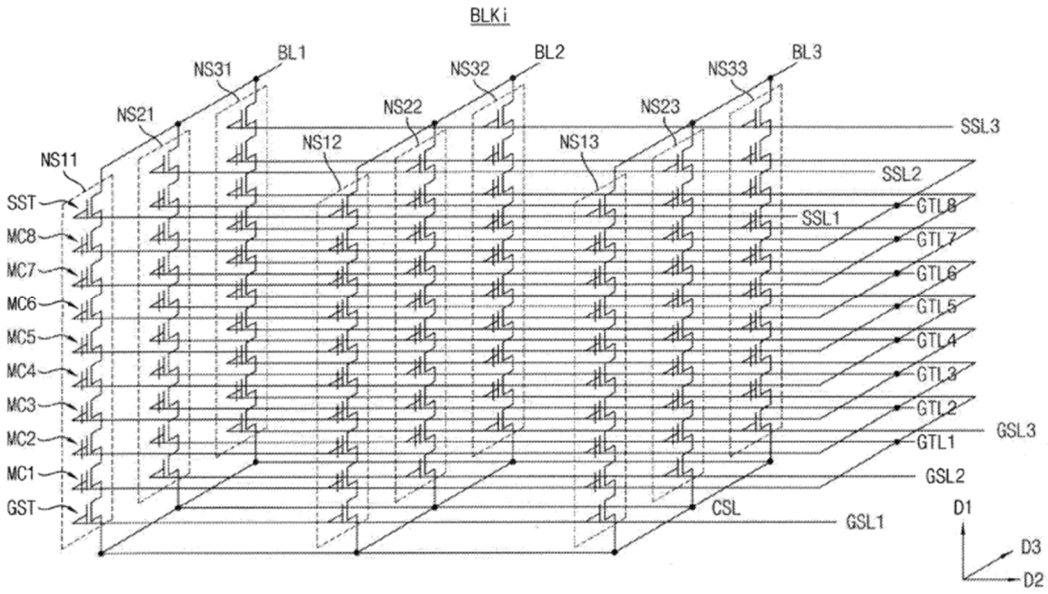
Hongtao, Fig. 2.

Notably, during the read phase, Hongtao applies a conduction voltage on unselected word lines lower than the pre-conduction voltage. Hongtao acknowledges that "the greater the conduction voltage, the greater the read disturbance to the memory cell." Hongtao, [0026]. Thus, by lowering the conduction voltage, read disturbance is reduced. Liu, ¶¶ 68-75.

B. Yu

U.S. Patent Publ. No. 2019/0198117 ("Yu") was filed on September 25, 2018, and published on June 27, 2019. Yu, Cover. Yu is prior art to the '957 patent under 35 U.S.C. §§102(a)(1)-(2) (AIA).

Yu is directed to methods of programming 3D NAND memory devices. Yu, Abstract, [0004]. Yu's devices have a conventional structure:

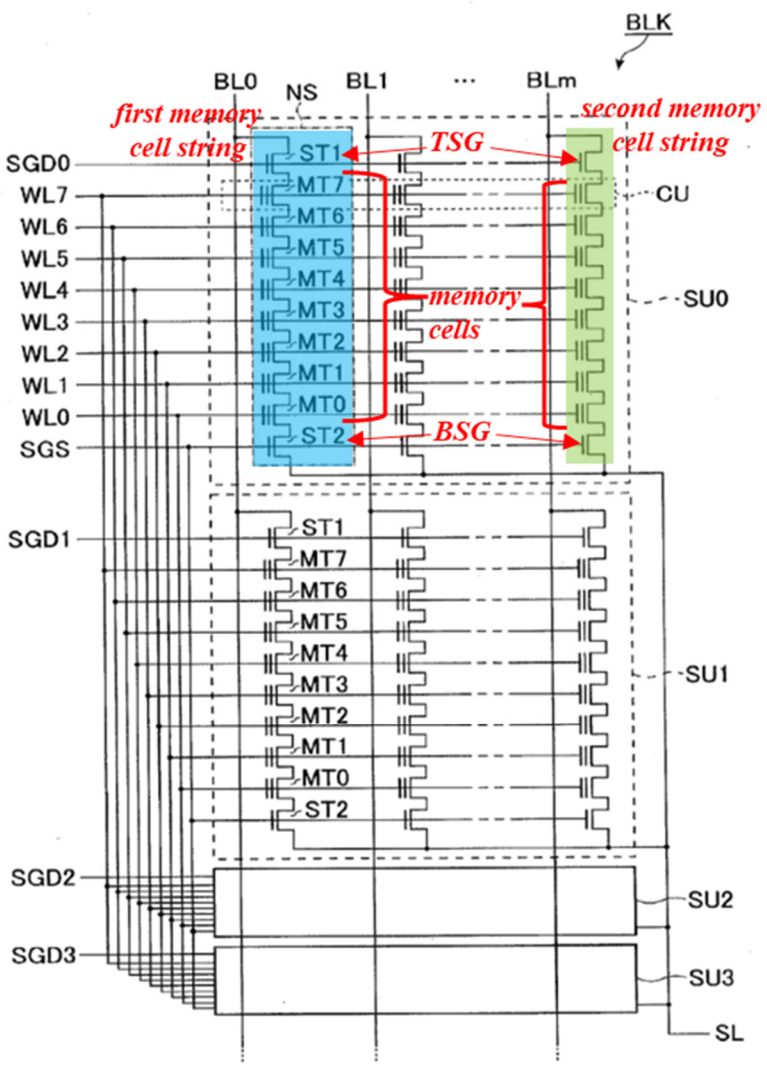


Id., Fig. 6. Yu discloses that programming may proceed from the source end to the drain end of a string, or vice versa. *Id.*, [0115], [0130]; Liu, ¶¶ 76-78.

C. Suzuki

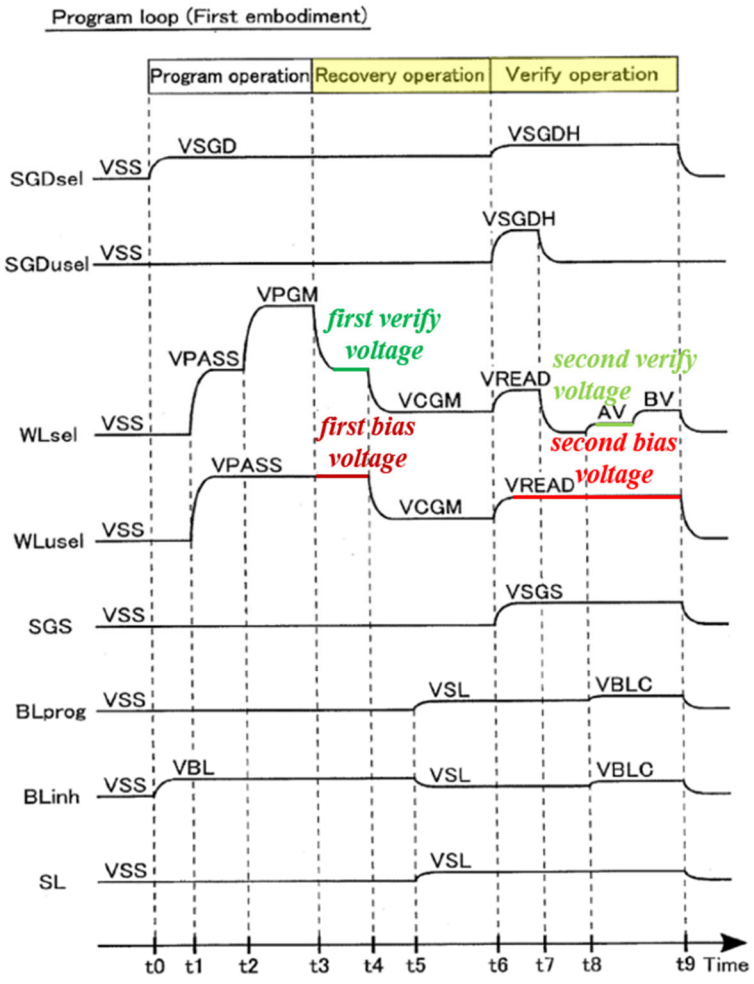
U.S. Patent Publ. No. 2021/0082505 ("Suzuki") was filed on July 13, 2020, and was published on March 18, 2021. Suzuki, Cover. Suzuki is prior art to the '957 patent at least under 35 U.S.C. §102(a)(2) (AIA).

Suzuki discloses a conventional 3D NAND flash memory structure. Suzuki, [0003].



Id., Fig. 2, [0047]-[0050].

Suzuki further discloses a program loop comprising, sequentially, a program operation, a recovery operation, and a verify operation. Suzuki, Abstract. Suzuki recognizes that read-back errors result from post-verify threshold-voltage drift due to de-trapping. *Id.*, [0148]-[0152]. Suzuki reduces such errors by applying control voltages to facilitate de-trapping in the recovery operation. *Id.*, [0153]. Suzuki discloses the claimed '957 waveforms:

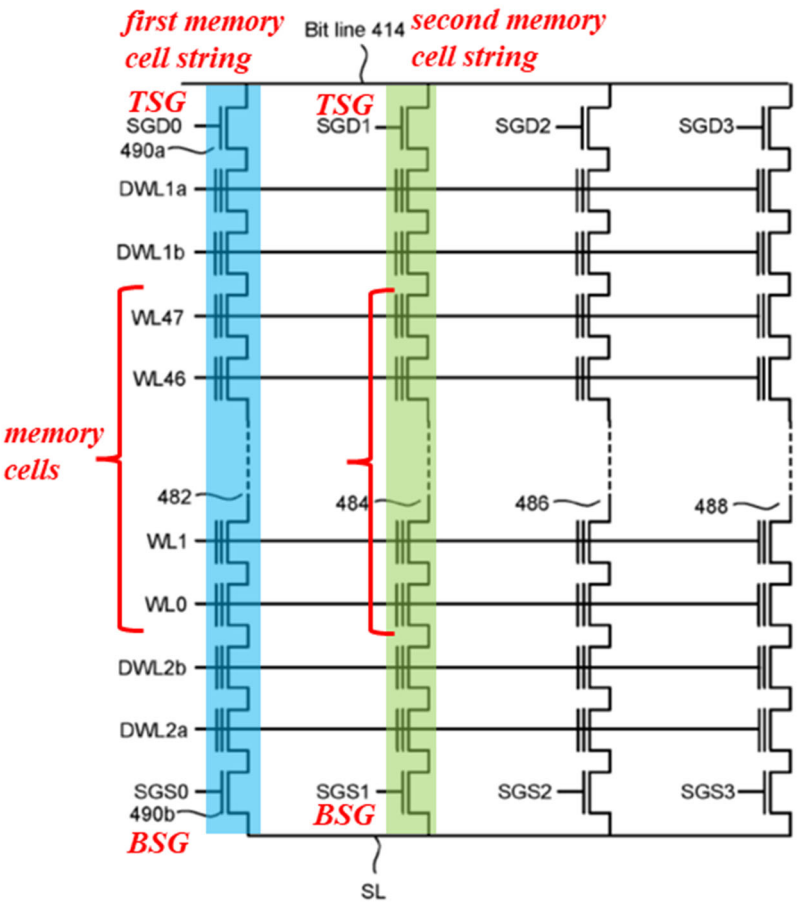


Id., Fig. 11; Liu, ¶¶ 79-82.

D. Costa

U.S. Patent Publ. No. 2018/0012667 ("Costa") was published on January 11, 2018. Costa, Cover. Costa is prior art to the '957 patent under 35 U.S.C. §§102(a)(1)-(2) (AIA).

Costa discloses a conventional 3D NAND flash memory structure:



Costa, Fig. 4F, [0077].

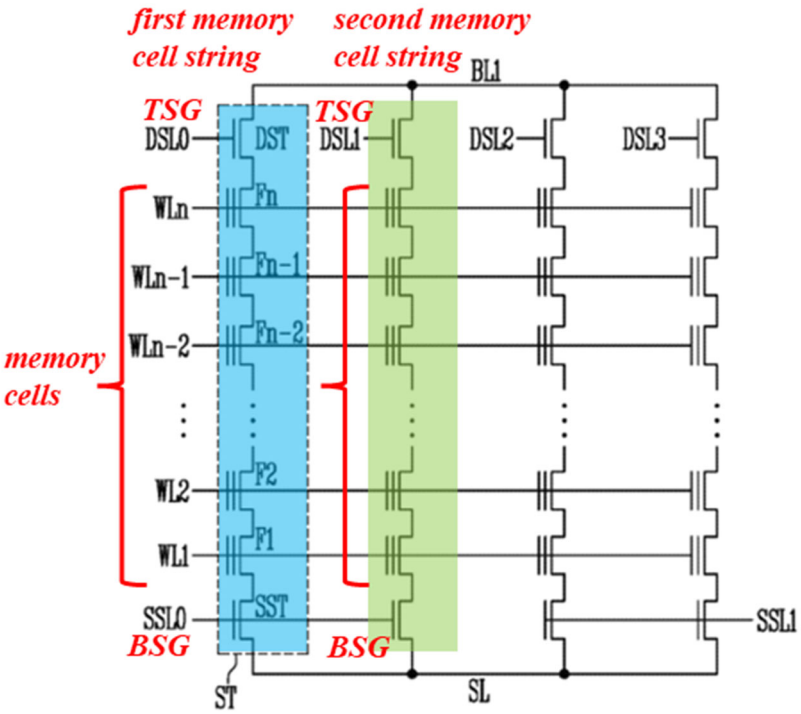
Costa discloses that channel resistance increases as more memory cells are programmed. Costa, Abstract. To mitigate this issue, Costa teaches a technique that

uses a low read pass voltage on unprogrammed cells. *Id.*, Abstract, cl. 5; Liu, ¶¶ 83-85.

E. Seo

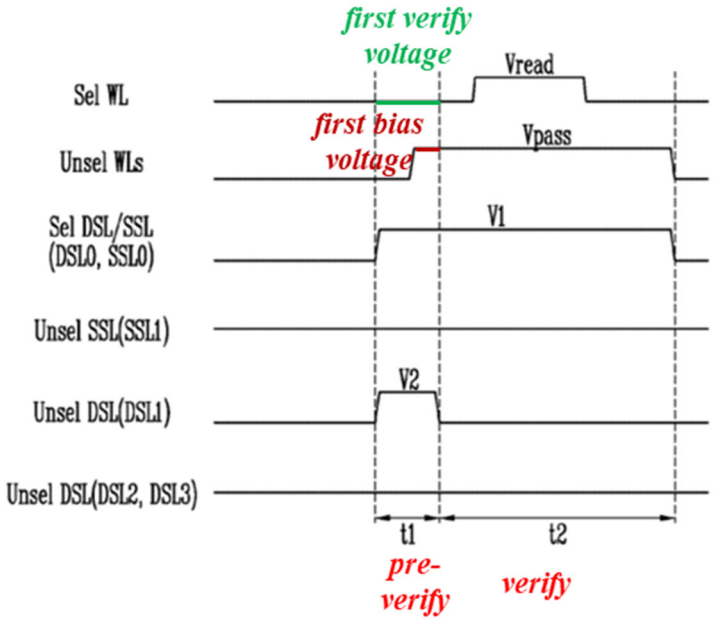
U.S. Patent Publ. No. 2021/0027848 ("Seo") was filed on October 18, 2019, and was published on January 28, 2021. Seo, Cover. Seo is prior art to the '957 patent under 35 U.S.C. §§102(a)(1)-(2) (AIA).

Seo relates to read operations of conventional 3D NAND flash memory. Seo, Abstract, [0004]-[0007].



Id., Fig. 4, [0053]-[0059].

Seo relates to reducing HCI on unselected memory strings during read operations. Seo, [0008]. Seo applies voltages in a time period t1 before the read operation that match the claimed '957 voltages. *Id.*, [0088]-[0089].



Id., Fig. 8; Liu, ¶¶ 86-89.

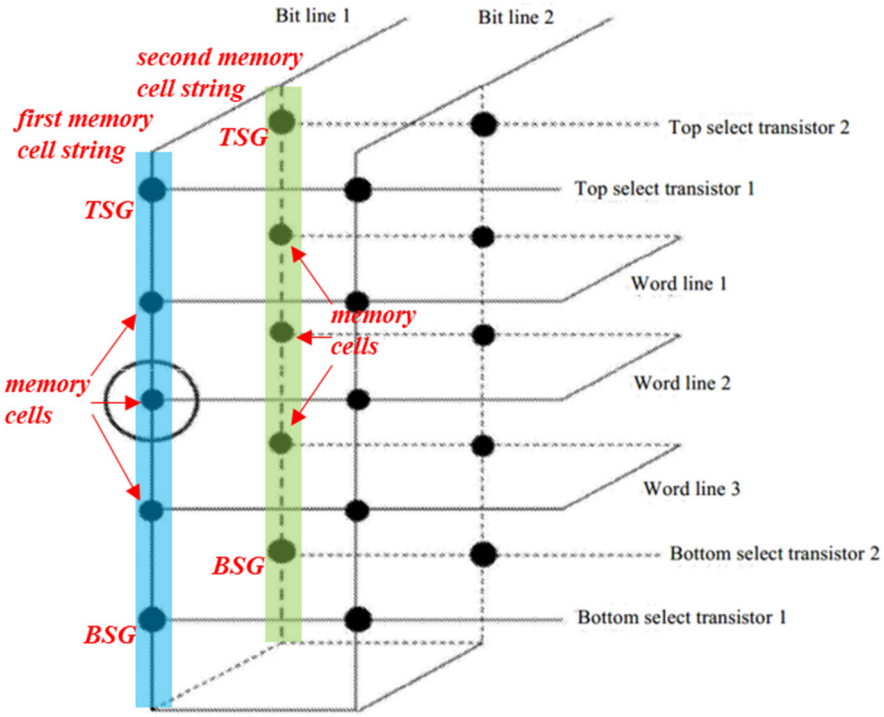
IX. GROUND 1: CLAIMS 1-6 ARE OBVIOUS OVER HONGTAO IN VIEW OF YU

A. Claim 1:

1. [1.PRE] "An apparatus for reading a memory device including a first memory cell string and a second memory cell string, the first memory cell string including a bottom-select-gate (BSG) transistor, memory cells, and a top-select-gate (TSG) transistor that are connected in series, the second memory cells string including a BSG transistor, memory cells, and a TSG transistor that are connected in series, the apparatus comprising:"

To the extent the preamble is limiting, Hongtao discloses it.

Hongtao discloses "a reading method of 3D NAND flash memory." Hongtao, Abstract. This NAND flash, *an apparatus for reading a memory device*, includes multiple memory strings such as *a first memory cell string* (highlighted blue) *and a second memory cell string* (green):[3]



Id., Fig. 1, [0006], [0017], [0018]. As shown above, Hongtao discloses that each "memory string" includes a "top select transistor" (*a top-select-gate (TSG) transistor*) and "bottom select transistor" (*a bottom-select-gate (BSG) transistor*), with *memory cells* that are *connected in series*. *Id.*, [0018]; Liu, ¶¶ 92-95.

[3] For clarity, red italics in claim-mapping sections herein denotes claim language.

2. [1.A] "processing circuitry configured to:"

Hongtao discloses, or at least renders obvious, in view of a POSITA's knowledge or Yu, *processing circuitry*.

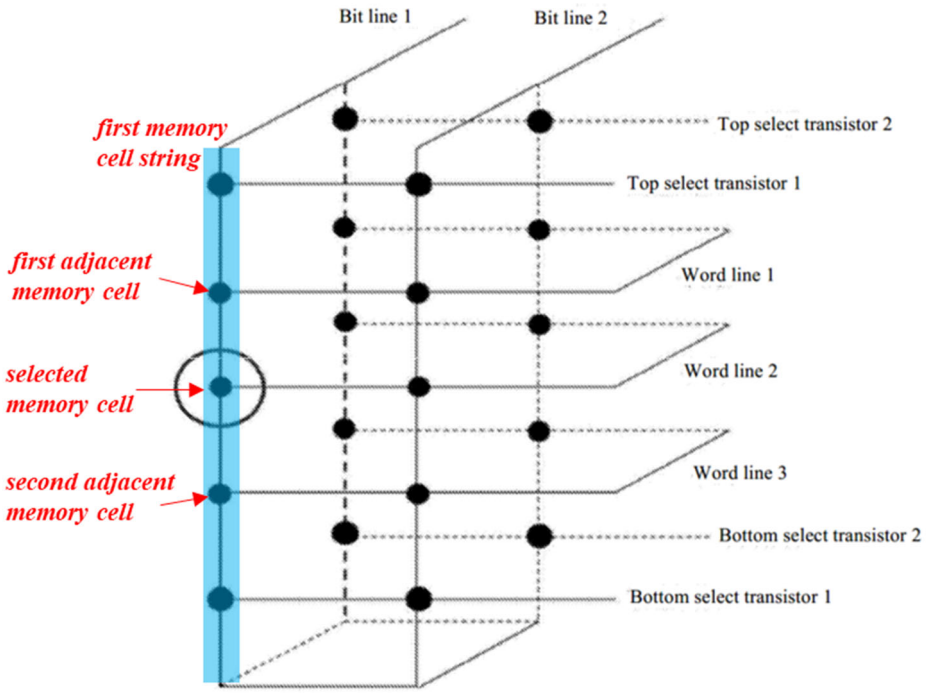
Processing circuitry is simply the circuitry that applies the claimed voltages. Ex. 1001, 4:25-36, 16:55-60.

Hongtao discloses applying various voltages as required. *Infra* §§IX.A.3-IX.A.6. A POSITA would have thus understood that Hongtao discloses *processing circuitry* to apply these voltages and certainly would have found it obvious, given that such circuitry was the conventional (perhaps the exclusive) way to apply such signals, and was well understood and routine to implement. Liu, ¶¶ 96-99; *see also* §§X.A.2, XI.A.2 (a POSITA's knowledge as shown in Grounds 2 and 3 references). Additionally, a POSITA would have found *processing circuitry* obvious in view of Yu's conventional circuitry for generating and applying voltages to operate memory cell arrays. Yu, Fig. 3, [0045]-[0059]; Liu ¶¶ 98-99.

3. [1.A.i] "apply, in a pre-verify stage, a first verify voltage[4] on a gate terminal of a selected memory cell of the first memory cell string, the selected memory cell being programmed and arranged between a first adjacent memory cell and a second adjacent memory cell;"

Hongtao in view of Yu renders this limitation obvious.

As to the *memory cell*, Hongtao illustrates its method through "read[ing] … the *selected memory cell* circled in Figure 1." Hongtao, [0019]. The *selected memory cell*, e.g., coupled to word line 2, is positioned between adjacent memory cells:

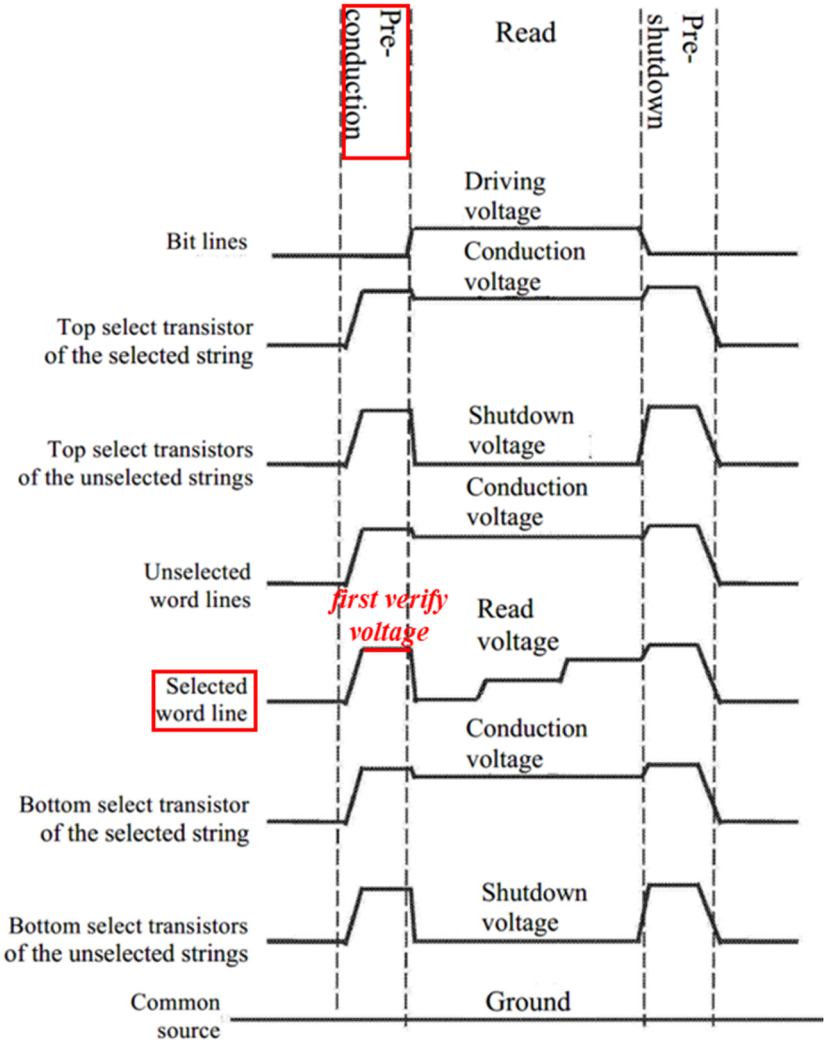


Id., Fig. 1.

[4] That the '957 patent uses a "verify voltage" in the pre-verify stage is a misnomer, because verification (reading) does not occur in that stage. Liu, ¶ 106.

When using Hongtao's read operation to verify program operations, the same selected cell is programmed and then verified. Hongtao, Fig. 1, [0019]. Accordingly, when the *selected memory cell* is being verified, it is *programmed*. In view of Yu and a POSITA's knowledge, it would have been obvious to employ Hongtao's read for program verification. *See* §IX.G; Liu, ¶ 103.

Hongtao discloses that the selected cell to be read is connected to the selected word line. Hongtao, [0022]; *see also* §V.A.2 (word line-memory cell coupling). Hongtao further discloses applying "a pre-conduction voltage" to the "selected word line" in a "pre-conduction phase." Hongtao, [0008], [0023].

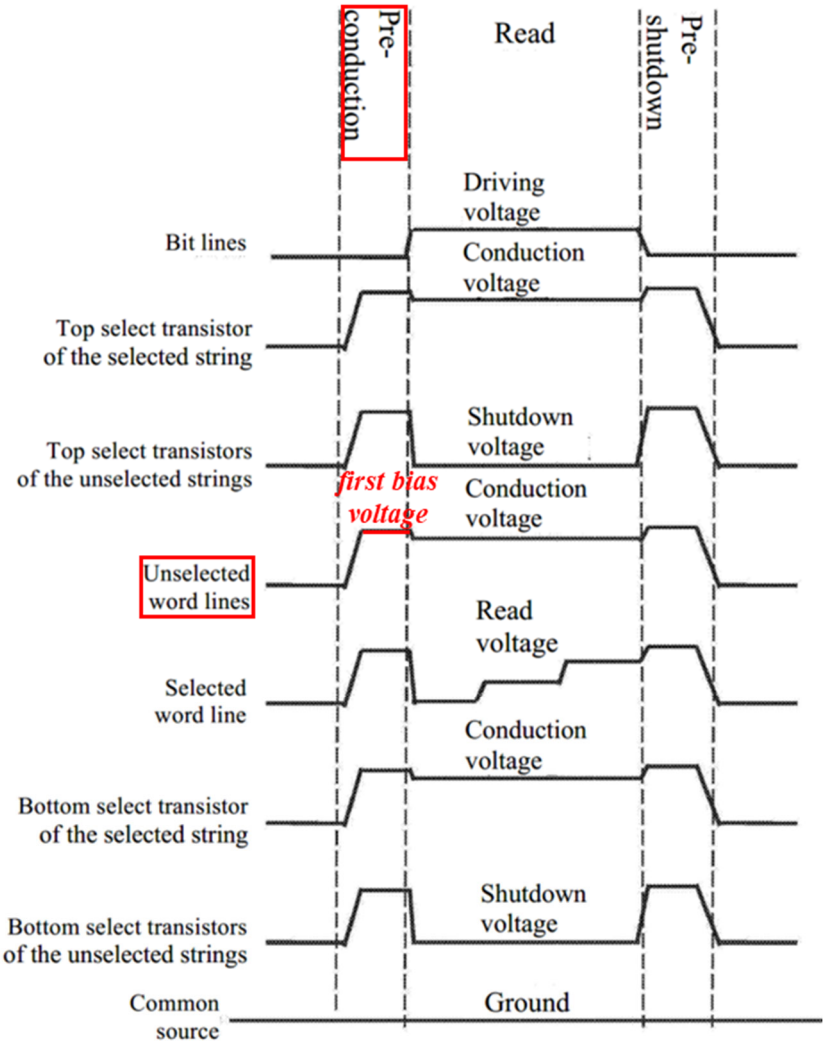


Id., Fig. 2. The pre-conduction phase precedes the read/verify phase. *Id.*, claim 1, [0022]. While not limiting, like the first verify voltage of embodiments of the '957 patent, the pre-conduction voltage turns on the channel. Ex. 1001, 11:12-15; Hongtao, [0023]. Thus, this "pre-conduction voltage" constitutes *a first verify voltage on … a selected memory cell, appl[ied] in a pre-verify* (pre-conduction) *stage*. Liu, ¶¶ 100-105.

4. [1.A.ii] "apply, in the pre-verify stage, a first bias voltage on a gate terminal of at least one memory cell of the first memory cell string that is not programmed;"

Hongtao in view of Yu renders this limitation obvious.

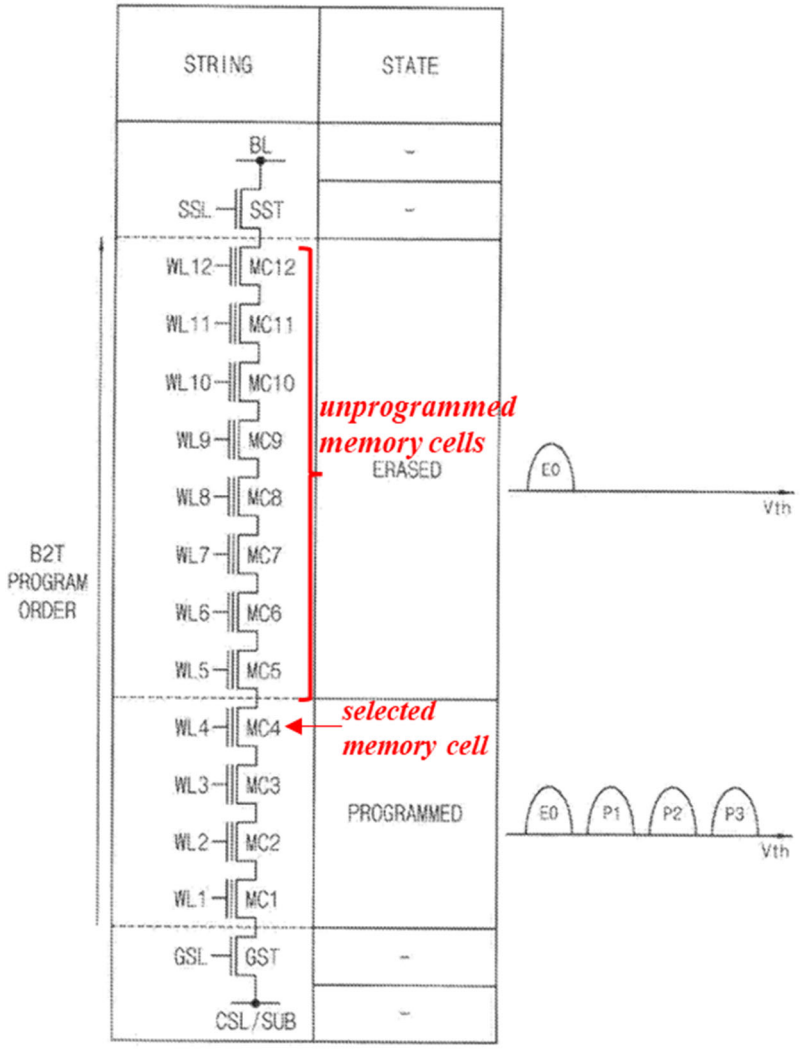
Hongtao discloses applying "a pre-conduction voltage … to … unselected word line[s]" "in the pre-conduction stage." Hongtao, [0023], *see also id.*, [0008].



Id., Fig. 2. The unselected word lines, e.g., word lines 1 and 3, are coupled to unselected cells in the selected memory string. *Id.*, [0019]. Thus, Hongtao discloses *apply[ing], in the pre-verify stage* (the pre-conduction stage), *a first bias voltage* (a

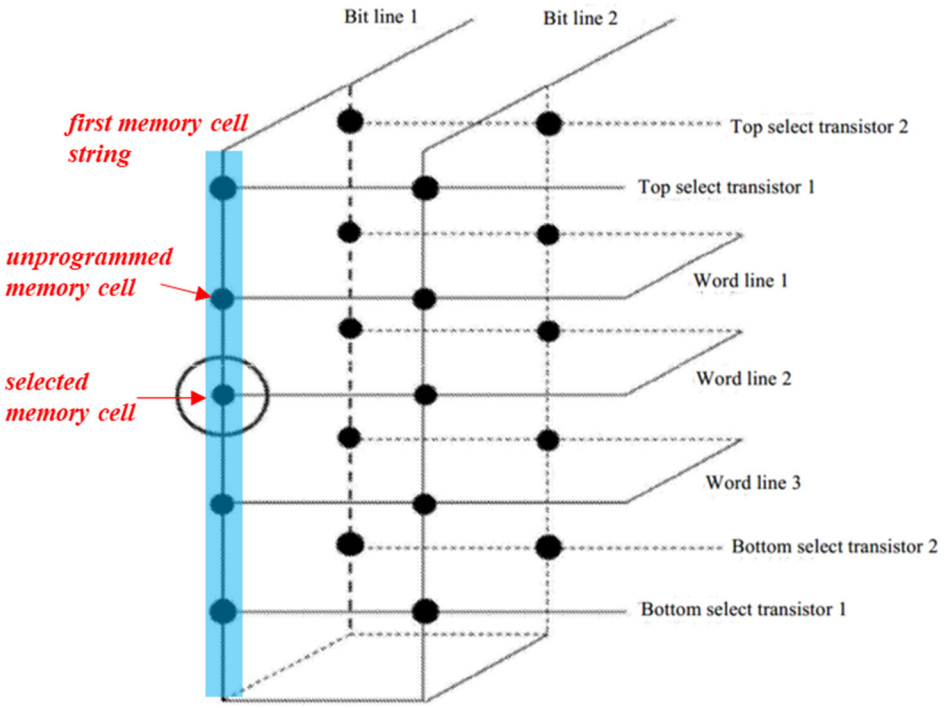
pre-conduction voltage) *on … at least one memory cell* (e.g., at word line 1) *of the first memory cell string* (the selected string). Liu, ¶¶ 107-110.

In view of Yu and the knowledge of a POSITA, this *at least one memory cell … is not programmed*. Liu, ¶¶ 111-113; §IX.G (motivations). Yu discloses "the program operation may be performed in an upward direction from a lowest word line … from bottom to top (B2T program order)." Yu, [0115]. When memory cell MC4 below undergoes programming verification, cells MC1 through MC4 have been programmed, and cells MC5 through MC12 are unprogrammed and "in an erased state." *Id.*



Id., Fig. 11.

The B2T program order can be illustrated in Hongtao's embodiment as follows:

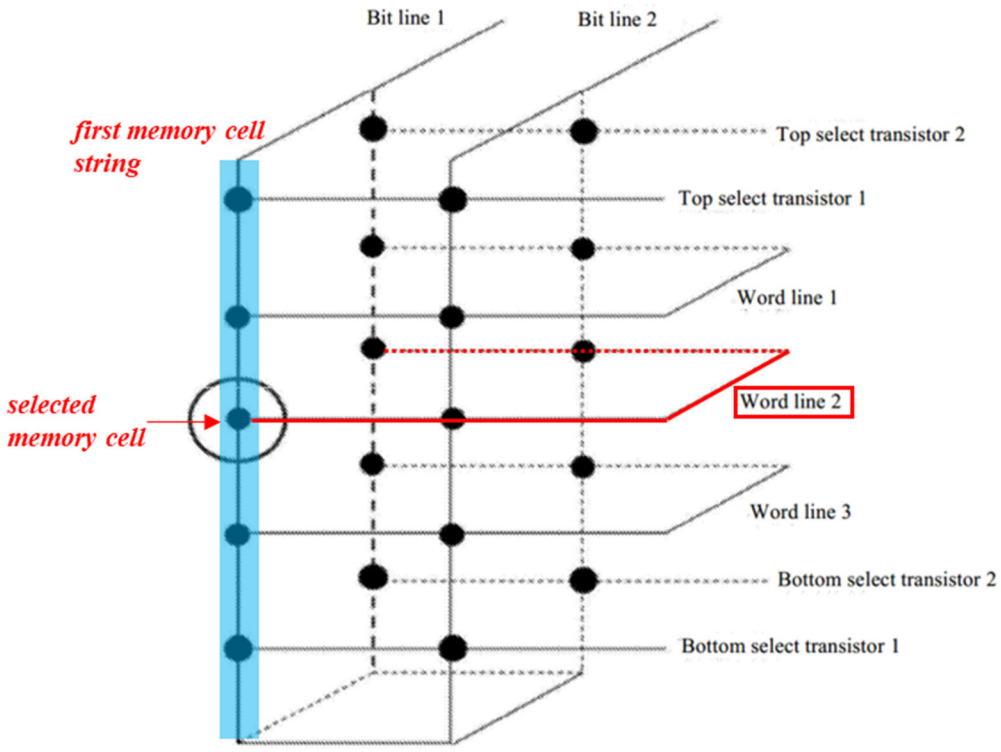


Hongtao, Fig. 1. The pre-conduction voltage is applied to unselected memory cells, including the unprogrammed memory cell illustrated above. As §IX.B demonstrates, Hongtao would have been understood to disclose longer memory strings (or it would have been obvious), such that additional unprogrammed cells above the adjacent memory cell would also receive the voltages of [1.A.ii] and [1.A.iv]. Liu, ¶ 113.

5. [1.A.iii] "apply, in a verify stage, a second verify voltage on the gate terminal of the selected memory cell of the first memory cell string; and"

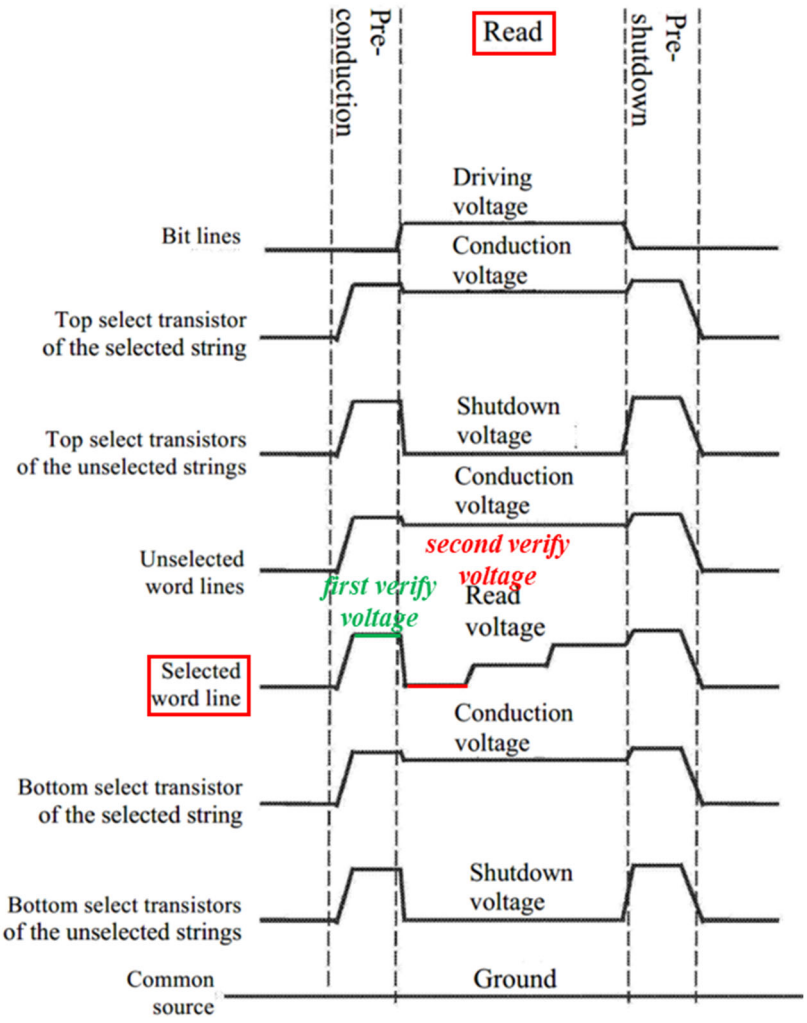
Hongtao discloses this limitation.

The limitation refers to the memory cell coupled to, e.g., word line 2. *See* §IX.A.3.



Hongtao, Fig. 1.

Hongtao discloses "apply[ing] a read voltage to the word line 2 … to read the information in the selected memory cell" in a read phase. Hongtao, [0019]. Note that Hongtao discloses multiple read voltages as shown during that phase.



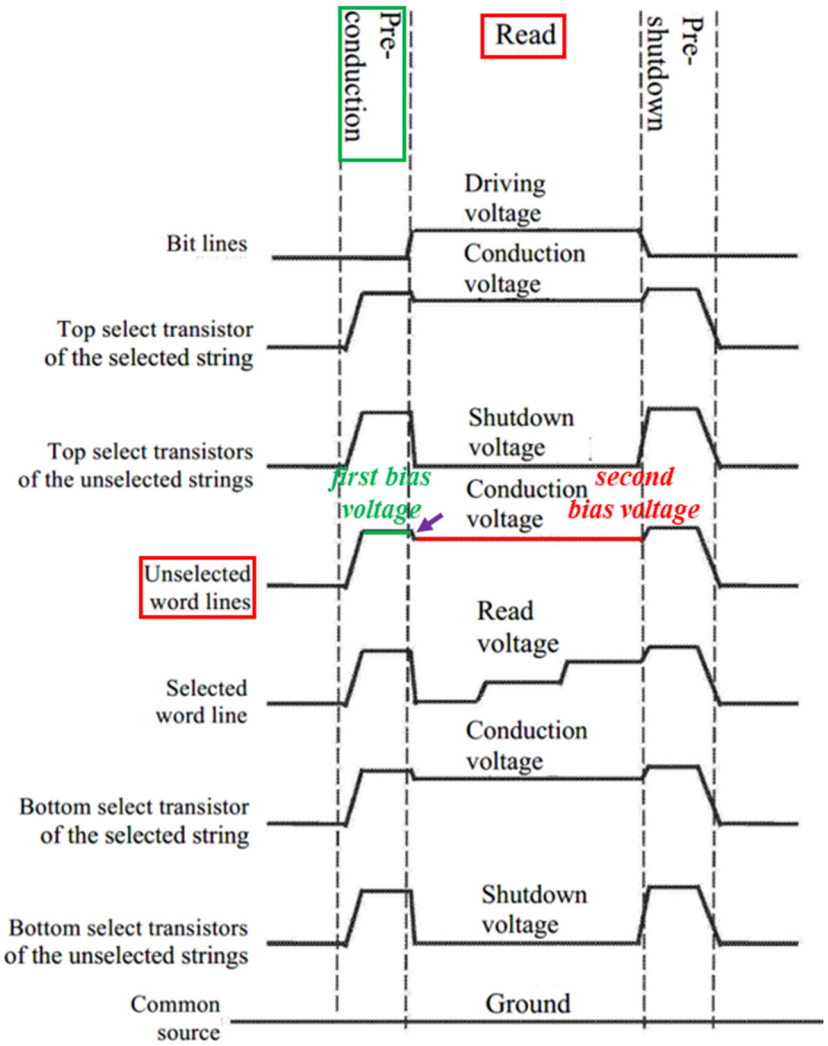
Id., Fig. 2. Like *the second verify voltage* of '957 patent embodiments, the read voltage determines the selected memory cell's data state. Ex. 1001, 11:35-39; *supra* §V.A.2. Thus, the read phase constitutes a verify stage.

Accordingly, Hongtao discloses *apply[ing], in a verify stage* (read phase)*, a second verify voltage* (read voltage) *on … the selected memory cell* (e.g., at word line 2) *of the first memory cell string* (the selected string). Liu, ¶¶ 114-117.

6. [1.A.iv] "apply, in the verify stage, a second bias voltage on the gate terminal of the at least one memory cell of the first memory cell string that is not programmed, wherein the second bias voltage is smaller than the first bias voltage."

Hongtao discloses this limitation.

This limitation refers to the same memory cell in claim [1.A.ii]. *See* §IX.A.4. Hongtao further discloses applying *a second bias voltage* (a conduction voltage) on the same cell through the same unselected word lines *in the verify stage* (the read phase):



Hongtao, Fig. 2; *see also id.*, [0019], [0025]. As indicated by the purple arrow, the voltage signal applied to the unselected word lines ramps down from the pre-conduction voltage to reach the conduction voltage. Thus, *the second bias voltage is smaller than the first bias voltage*. Liu, ¶ 120. "It is well settled that description for purposes of [invalidity] may be by drawings alone, as well as by words." *In re Boyd*, 55 F.2d 493, 494 (C.C.P.A. 1932); *see also ArthroCare Corp. v. Smith & Nephew, Inc.*, 406 F.3d 1365, 1374 (Fed. Cir. 2005) (finding clear and convincing evidence of invalidity based on figures in an article).

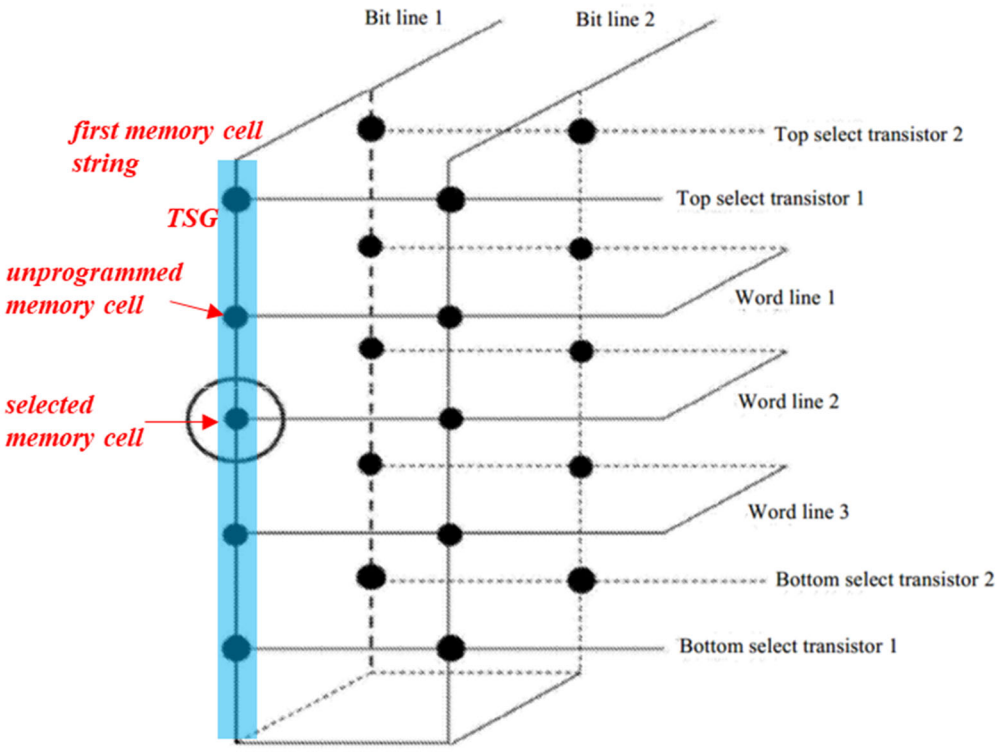
Hongtao explains that "the greater the conduction voltage, the greater the read disturbance to the memory cell." Hongtao, [0026]; *see also id.*, [0024]-[0025]. Accordingly, the conduction voltage is reduced during the read phase to reduce read disturbance. Liu, ¶¶ 118-120.

B. Claim 2:

1. [2] "The apparatus of claim 1, wherein the at least one memory cell of the first memory cell string that receives the first bias voltage and the second bias voltage is positioned between the first adjacent memory cell of the selected memory cell and the TSG transistor of the first memory cell string."

Hongtao in view of Yu renders this limitation obvious.

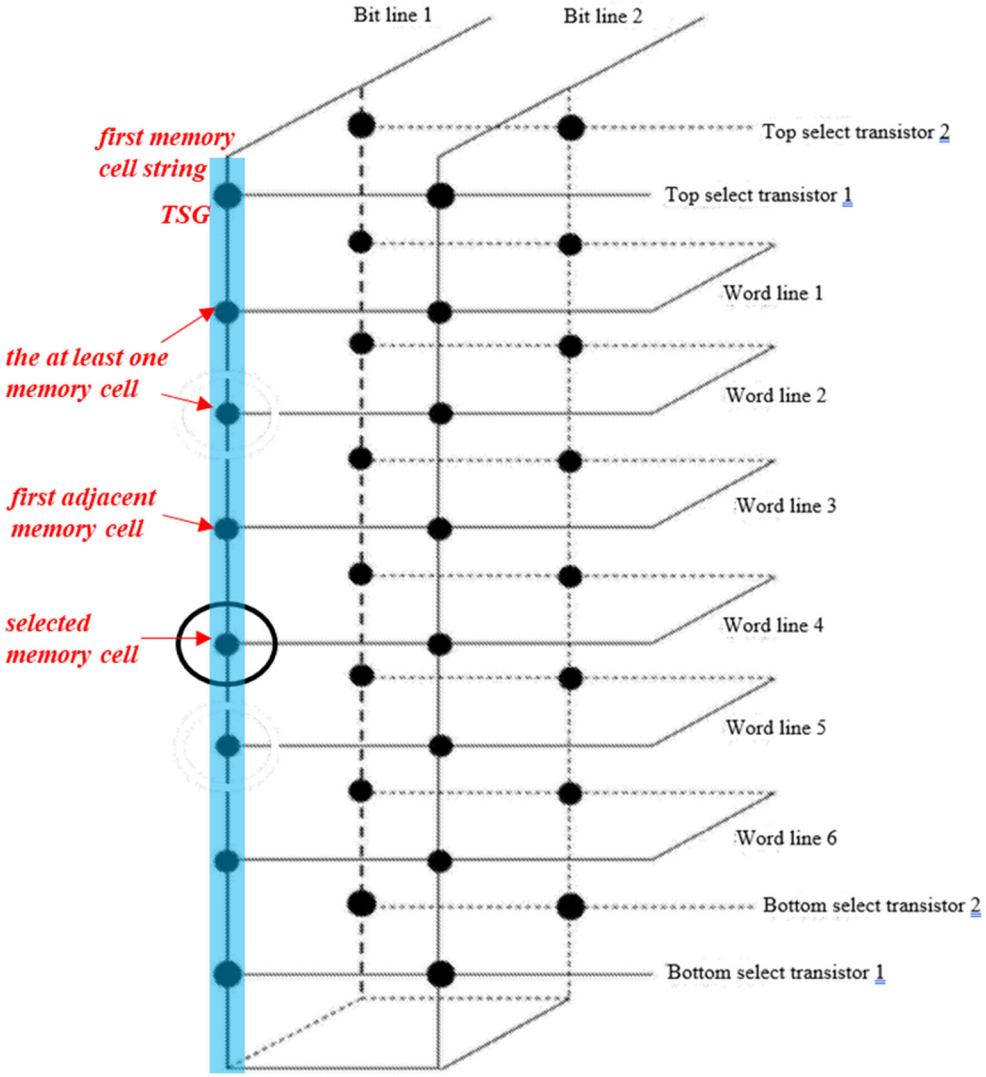
Claim 2 refers to the *not programmed* memory cell of claim [1.A.ii], [1.A.iv].



Hongtao, Fig. 1. This figure shows the unprogrammed cell as the same cell as the first adjacent memory cell. But the figure is merely an illustration.

Hongtao at least renders this limitation obvious. Hongtao does not limit the size of its memory device to the illustrated size, and states generally such strings include "a plurality of memory cells." Hongtao, Abstract. A POSITA would have understood, or certainly found obvious, that Hongtao is applicable to memory strings with many more than three cells, as was conventional, textbook material and routine to implement at the time. Liu, ¶ 123. Thus, with more than three memory cells per string, and with the selected cell as the one coupled to word line 4 as an example, there is *at least one memory cell* (e.g., at word line 1 or 2) *... that receives the first*

bias voltage and the second bias voltage [that] is positioned between the first adjacent memory cell (at word line 3) *... and the TSG transistor ...*:



Hongtao, Fig. 1 (expanded); Liu, ¶¶ 121-123.

C. Claim 3:

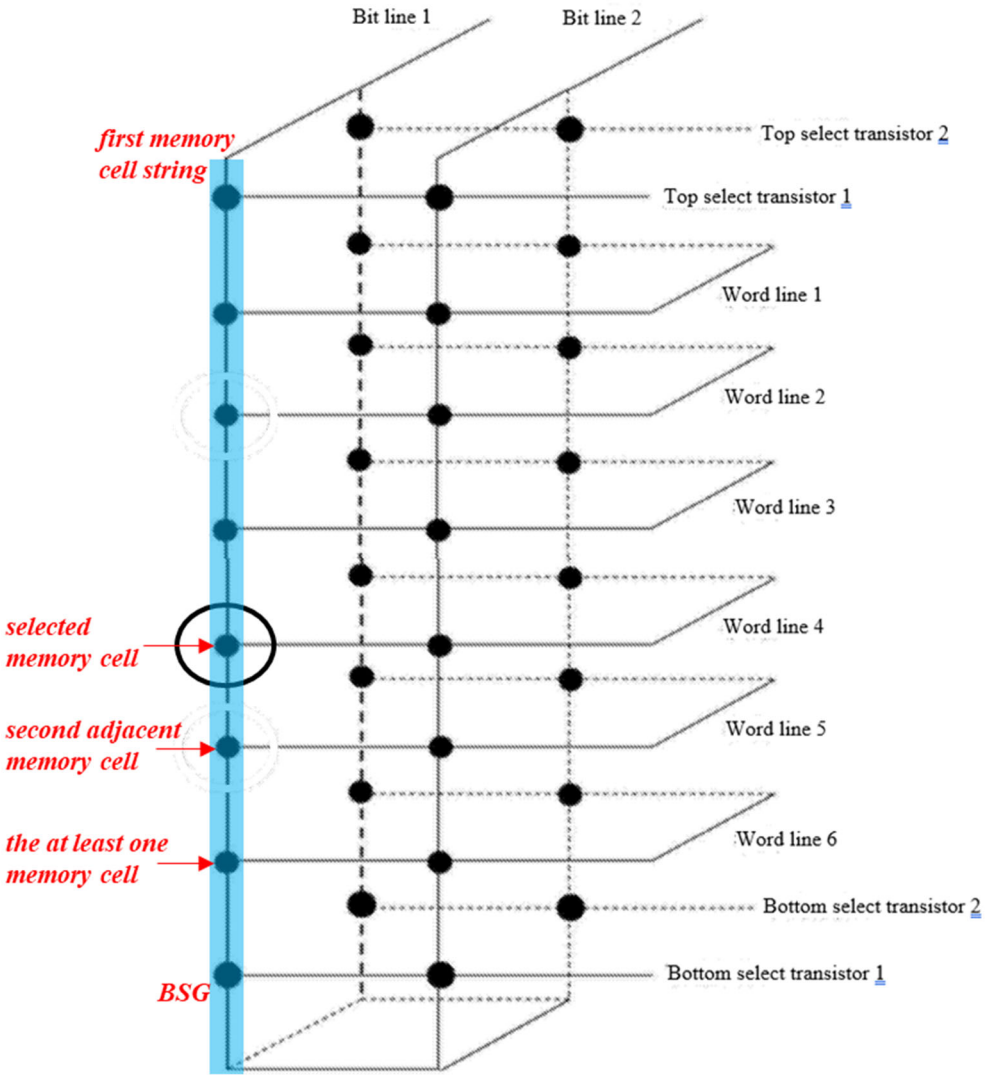
1. [3][5]

Hongtao in view of Yu renders this limitation obvious.

This limitation is the mirror image of claim 2. Here, claim 3 requires that the unprogrammed memory cell receiving the bias voltages be *positioned below* the selected cell, *between the second adjacent memory cell … and the BSG transistor*.

Hongtao discloses that all unselected cells receive the bias voltages. *See* §§IX.A.4, IX.A.6. Again, Figure 1 is not limiting. *Supra* §IX.B.1. Accordingly, if the memory cell coupled to word line 4 is the selected cell and the cell coupled to word line 5 is the second adjacent memory cell, then another cell below, e.g., one coupled to word line 6, can constitute *the at least one memory cell … that receives the … bias voltage[s]*:

[5] For Grounds 2 and 3, and the remainder of Ground 1, the Petition cites to the Listing of Challenged Claims.

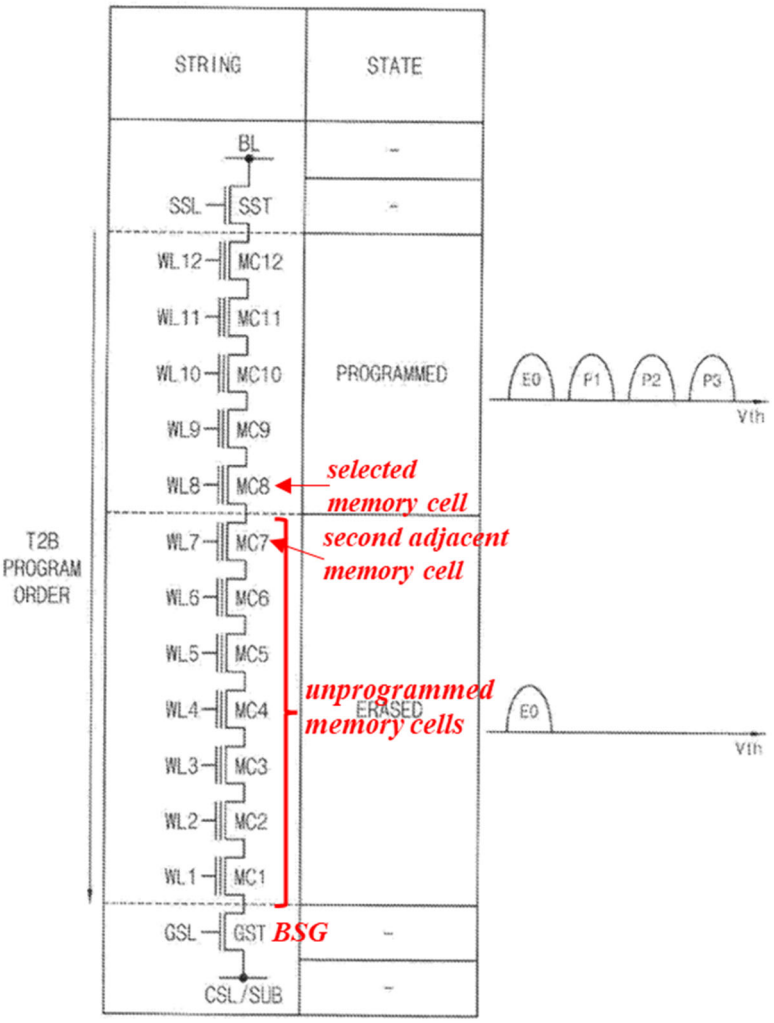


Hongtao, Fig. 1 (expanded); Liu, ¶¶ 124-126.

Yu renders obvious that this memory cell would be *not programmed* as required by claim 1.

Yu teaches that "the program operation may be performed in a downward direction from an uppermost word line … from top to bottom (T2B program order)." Yu, [0130]. When memory cell MC8 below is being verified, cells MC12 through

MC8 have been programmed, and cells MC7 through MC1 are unprogrammed and "in an erased state." *Id.*



Id., Fig. 14. Unprogrammed cells MC6 through MC1 are positioned between the second adjacent memory cell MC7 and the ground selection transistor GST, Yu's

BSG. Yu teaches that, using a T2B program order, Hongtao's memory cell at word line 6 is unprogrammed.[6] Liu, ¶¶ 127-129.

D. Claim 4:

1. [4.PRE]

Hongtao discloses or at least renders obvious a *processing circuitry further configured to* perform the limitations of claim 4. *Supra* §IX.A.2 Liu, ¶ 130.

2. [4.A]

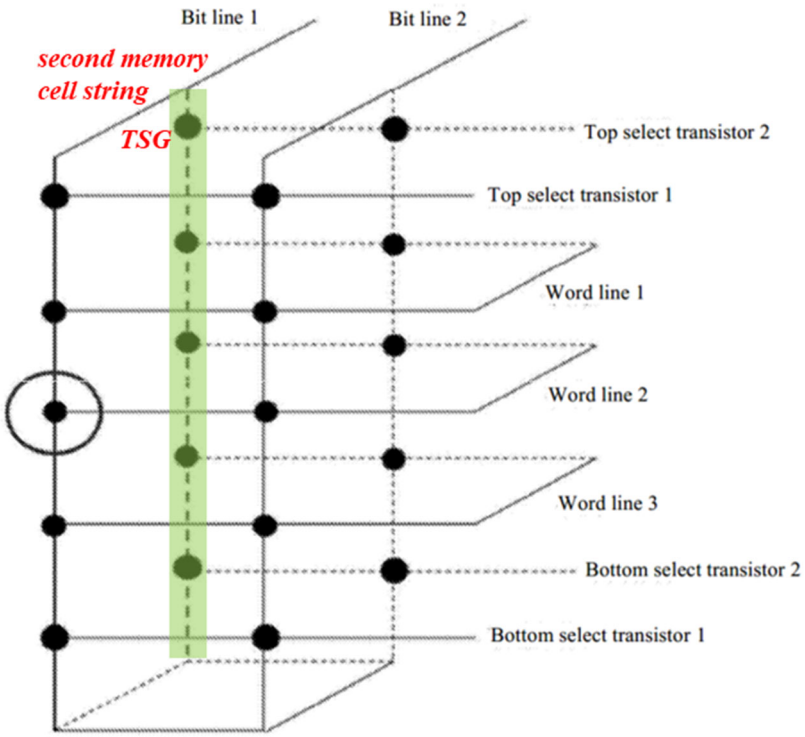
The pre-verify stage corresponds to Hongtao's "pre-conduction phase." *Supra* §§IX.A.3-IX.A.4; Liu, ¶ 131.

3. [4.A.i]

Hongtao discloses this limitation.

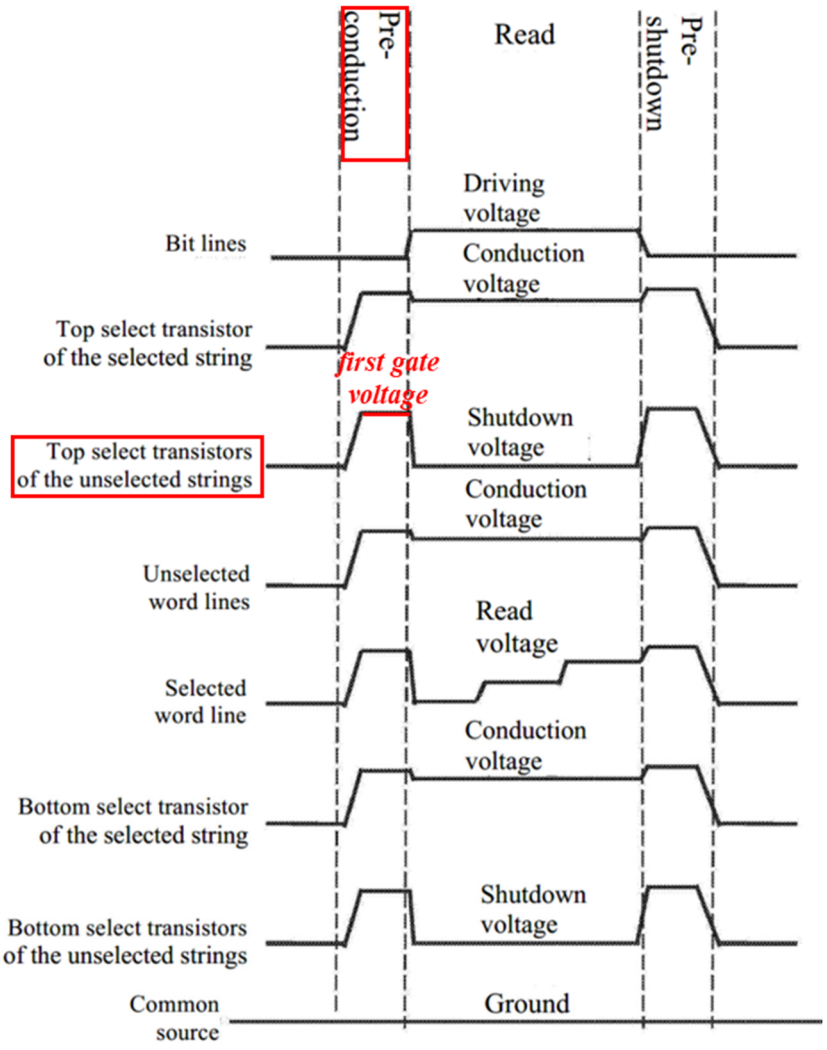
The second memory cell string is an unselected memory string since the selected memory cell belongs the first memory cell string. Ex. 1001, 17:41-43 (claim [1.A.i]). Hongtao discloses a top select transistor (*TSG transistor*) of an unselected memory string (*the second memory string*):

[6] Claim [1.A.ii] merely requires an unprogrammed memory cell to receive the bias voltages—without imposing any location requirement on this cell. Either the B2T or the T2B program order satisfies that limitation, and the B2T program order is used there merely to explain that limitation. *Supra* §IX.A.4.



Hongtao, Fig. 1; *see also supra* §IX.A.1 (claim [1.PRE] showing the same figure).

Hongtao further discloses *apply[ing] a gate voltage* on this transistor *in the pre-verify stage* (pre-conduction phase):

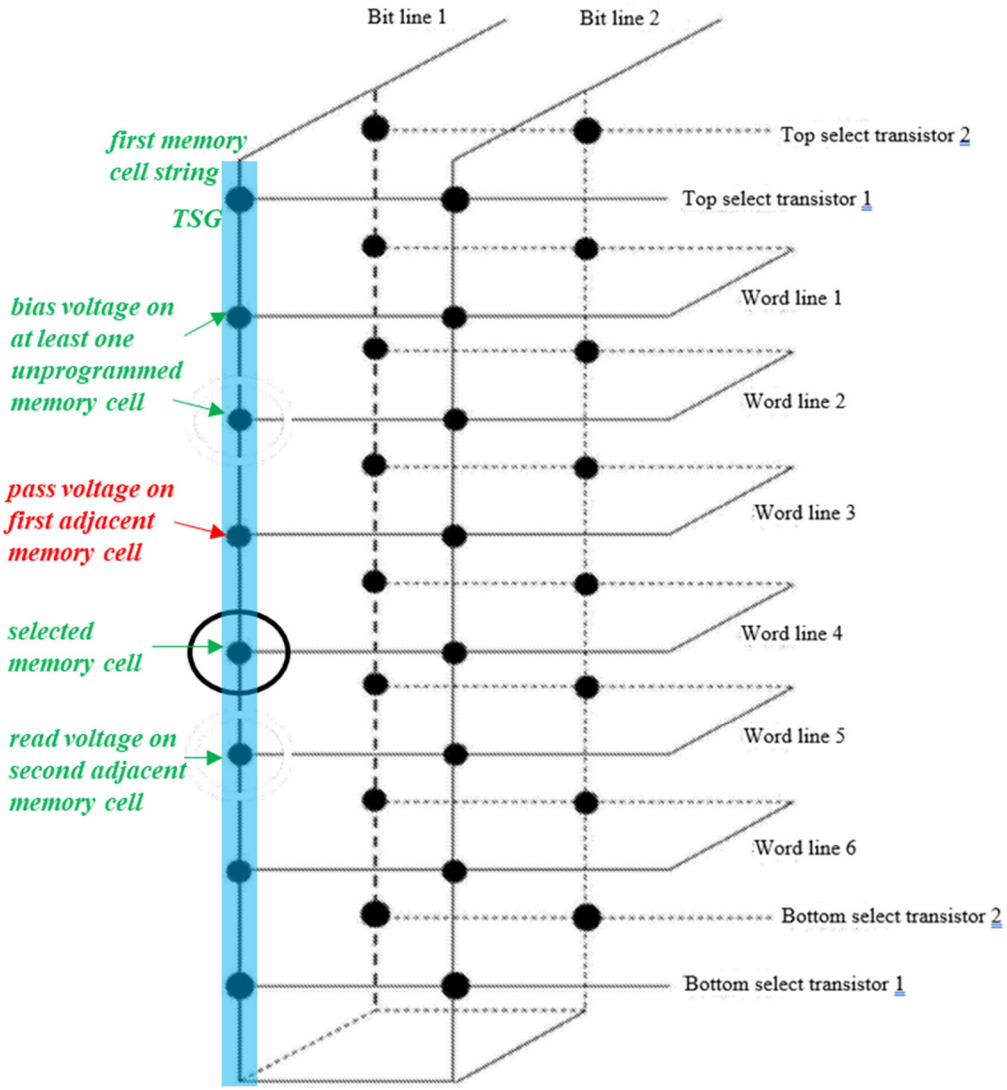


Hongtao, Fig. 2, Abstract, [0006] (turning on the transistor), [0031]; Liu, ¶¶ 132-134.

4. [4.A.ii]

Hongtao in view of Yu renders this limitation obvious.

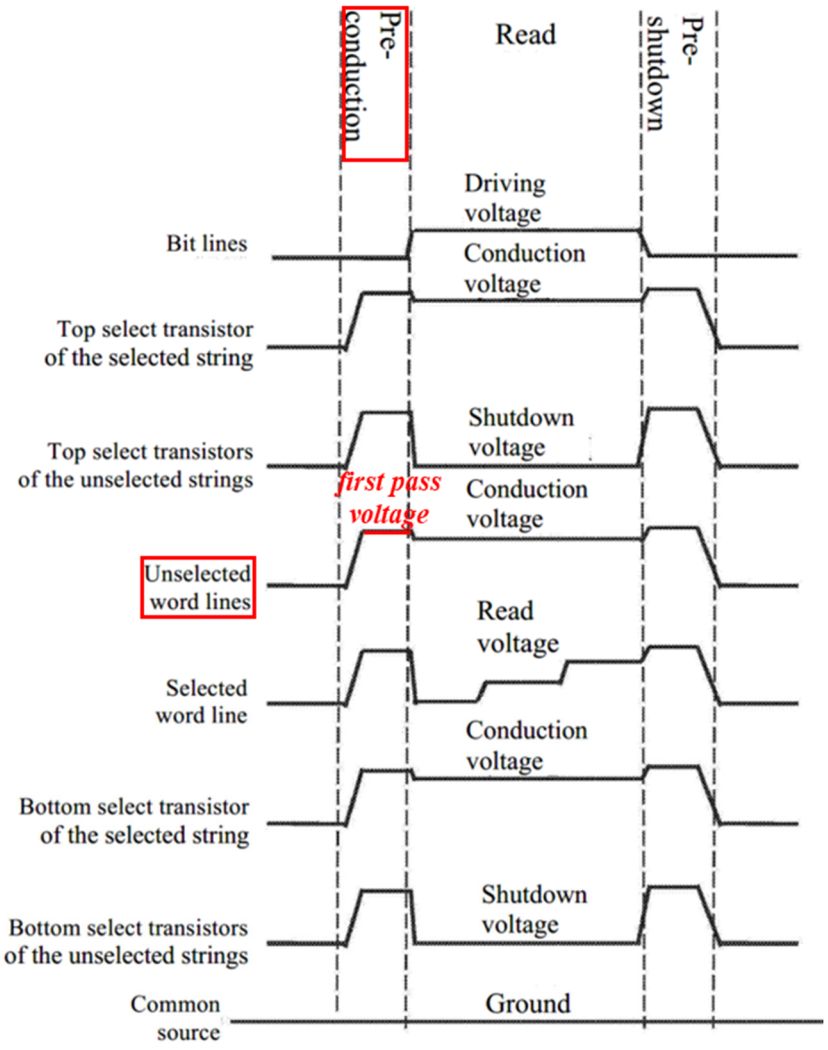
For example, *the first adjacent memory cell* may be located as illustrated below:



Hongtao, Fig. 1 (expanded).[7] *See* §IX.B.1 (for obvious extension of Hongtao's memory string).

And the *first pass voltage* is the voltage on unselected word lines:

[7] This expanded Figure 1 satisfies claim 1 even though it is not used in the discussion above.



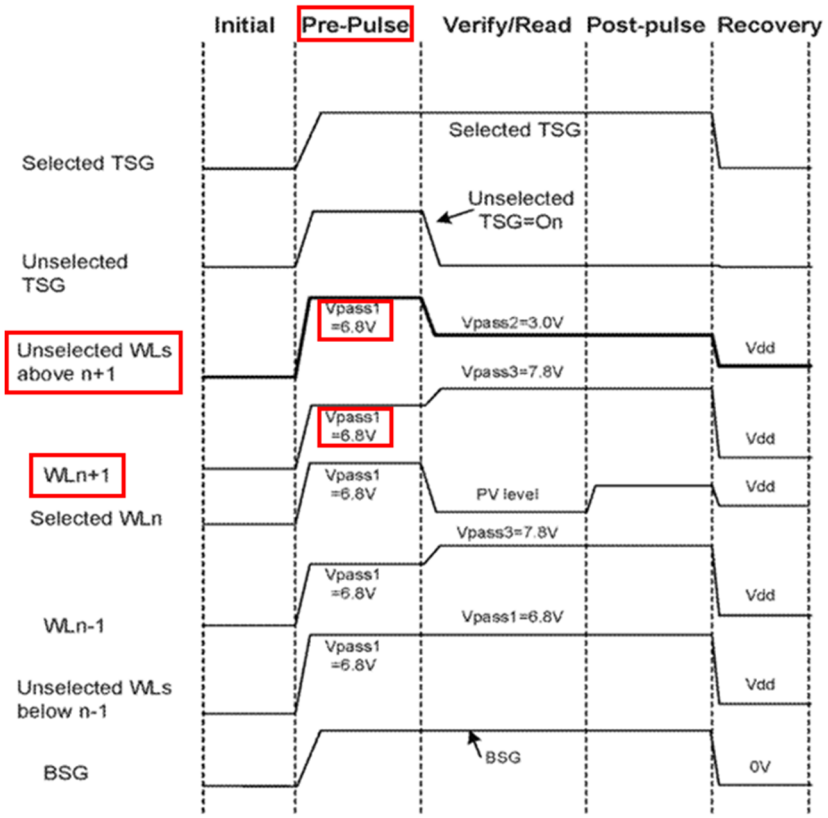
Hongtao, Fig. 2, [0023]; Liu, ¶¶ 135-137.

To the extent that Patent Owner argues the first pass voltage and the first bias voltage must have different values or be distinct voltages, Patent Owner is wrong.

When the '957 patent requires two voltage terms to have different values, its claim states so, e.g., claim 1 requires "the second bias voltage [to be] smaller than the first bias voltage." Ex. 1001, 17:55-56 (claim [1.A.iv]). As another example, claim 4 requires that "at least one of the second pass voltage and the second read

voltage is larger than the second gate voltage." *Id.*, 18:31-32 (claim [4.C]). But the claims impose no such requirements on the first bias voltage vis-à-vis the first pass voltage.

Further, embodiments of the '957 patent uses the same voltage—6.8V—for both the first bias voltage (applied on "Unselected WLs above n+1") and the first pass voltage (applied on "WLn+1"):



Ex. 1001, Fig. 6; *id.*, Fig. 8 (same), 11:3-5 (describing the same in Figure 4).

Moreover, as the figure also shows, both the first bias voltage and the first pass voltage are "Vpass1." *See also* Ex. 1001, Fig. 8 (same). Notably, the '957 patent equates bias voltages with pass voltages three different times. *Id.*, 9:35, 11:4,

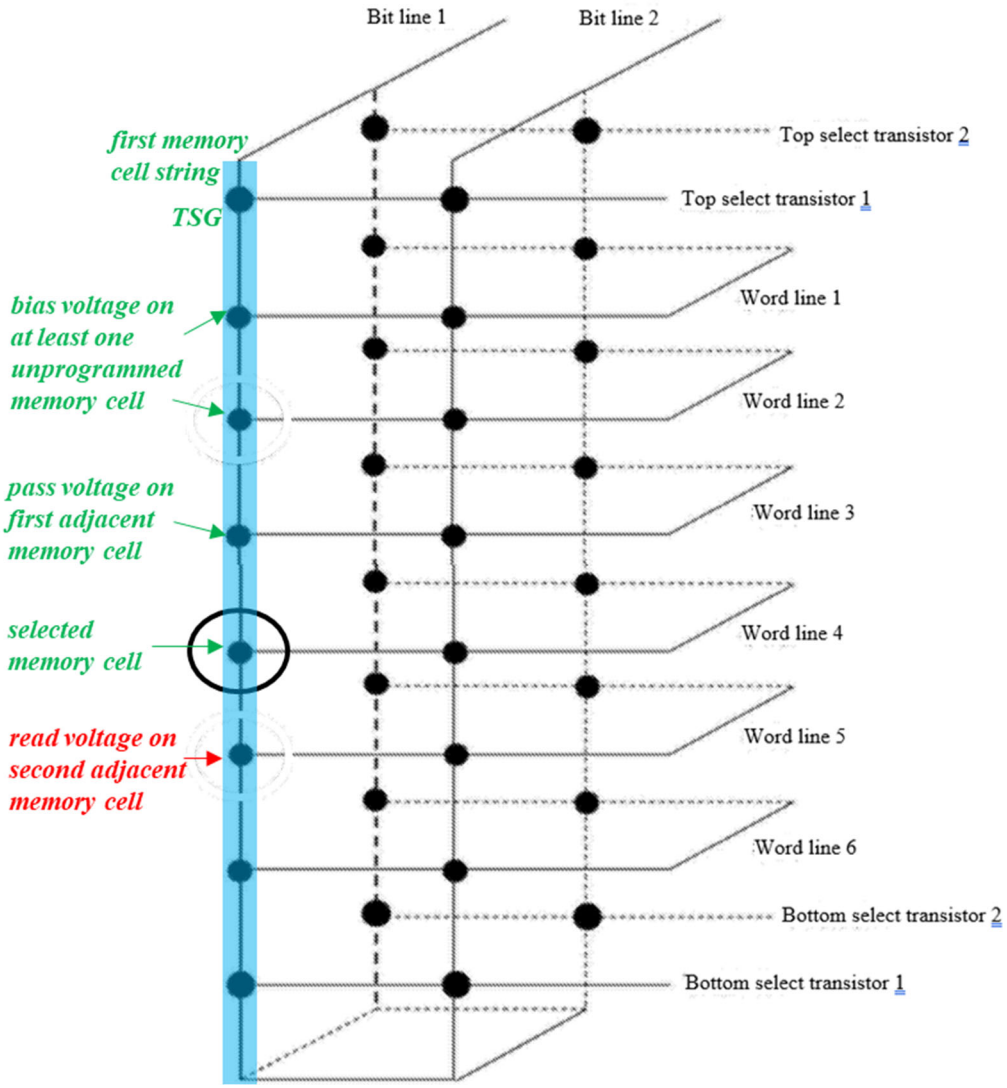
11:26-27.[8] Either bias voltages or pass voltages can be applied to unselected memory cells. *Id.*, 9:34-38. Moreover, "[a] bias voltage (*or* pass voltage) … can be applied on the WLn+1," the first adjacent memory cell. *Id.*, 11:4-5, 11:26-28 (emphasis added). Accordingly, bias voltages and pass voltages need not be distinct voltages. Liu, ¶¶ 138-142.

5. [4.A.iii]

Hongtao discloses this limitation.

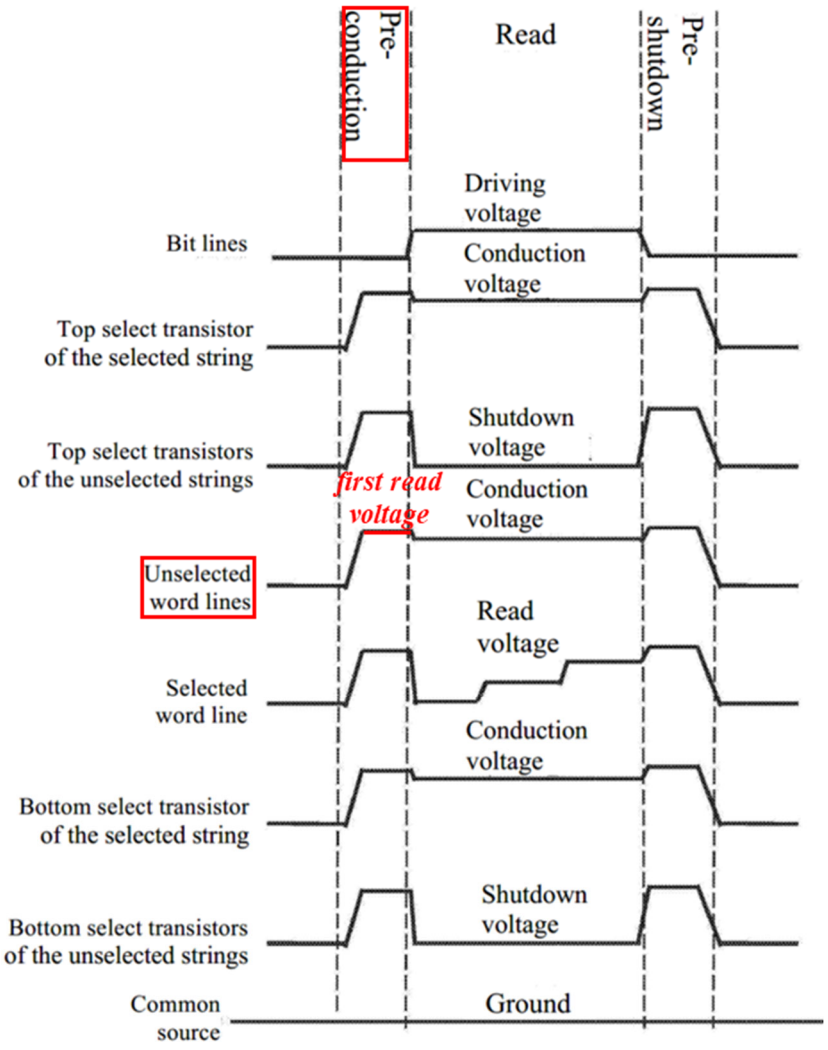
For example, *the second adjacent memory cell* may be located as illustrated below:

[8] Although the latter two references are to Figure 4, the waveforms during the pre-pulse stage in Figures 4, 6, and 8 are identical.



Hongtao, Fig. 1 (expanded). *See* §IX.B.1 (for obvious extension of Hongtao's memory string).

And the *first read voltage* is the voltage on unselected word lines:

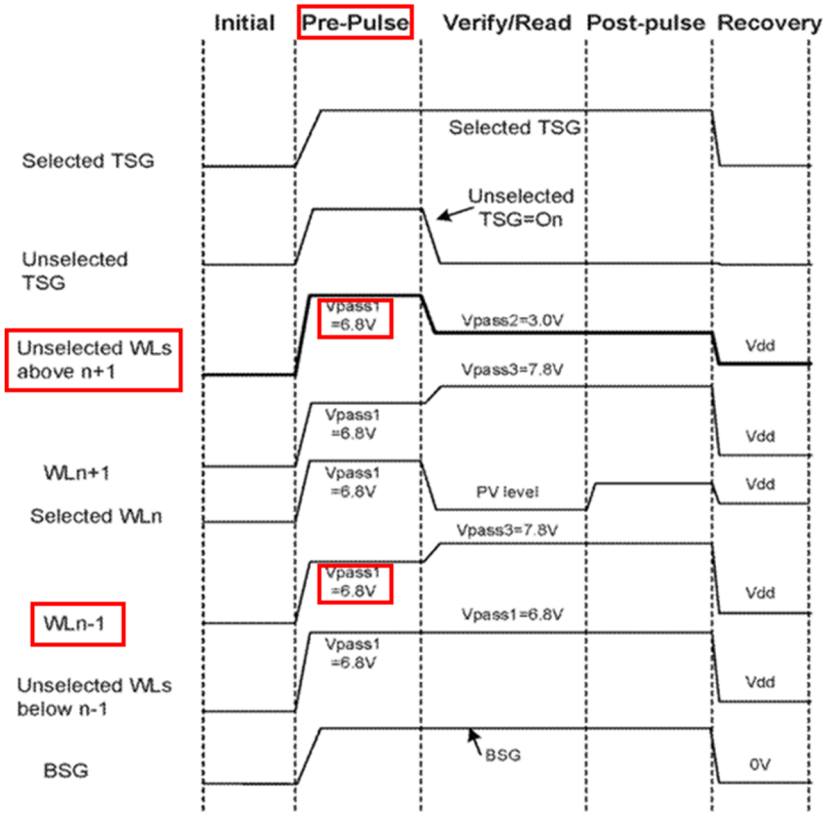


Hongtao, Fig. 2, [0023]; Liu, ¶¶ 143-145.

To the extent that Patent Owner argues the first read voltage and the first bias voltage must have different values or be distinct voltages, Patent Owner is wrong.

As explained above, when the '957 patent requires two voltage terms to have different values, its claim states so. *Supra* §IX.D.4. But the claims impose no such requirements here.

Further, embodiments of the '957 patent use the same voltage—6.8V—for both the first bias voltage (applied on "Unselected WLs above n+1") and the first read voltage (applied on "WLn-1"):



Ex. 1001, Fig. 6; *id.*, Fig. 8 (same).

Moreover, as the figure also shows, both the first bias voltage and the first read voltage are "Vpass1." *See also* Ex. 1001, Fig. 8 (same). Notably, the '957 patent twice equates bias voltages with read voltages in the context of WLn-1, *the*

second adjacent memory cell. *Id.*, 11:7-8, 11:29-30.[9] The voltage applied on WLn-1 can be either "[a] bias voltage (or read voltage)." *Id.*; Liu, ¶¶ 146-149.

6. [4.B]

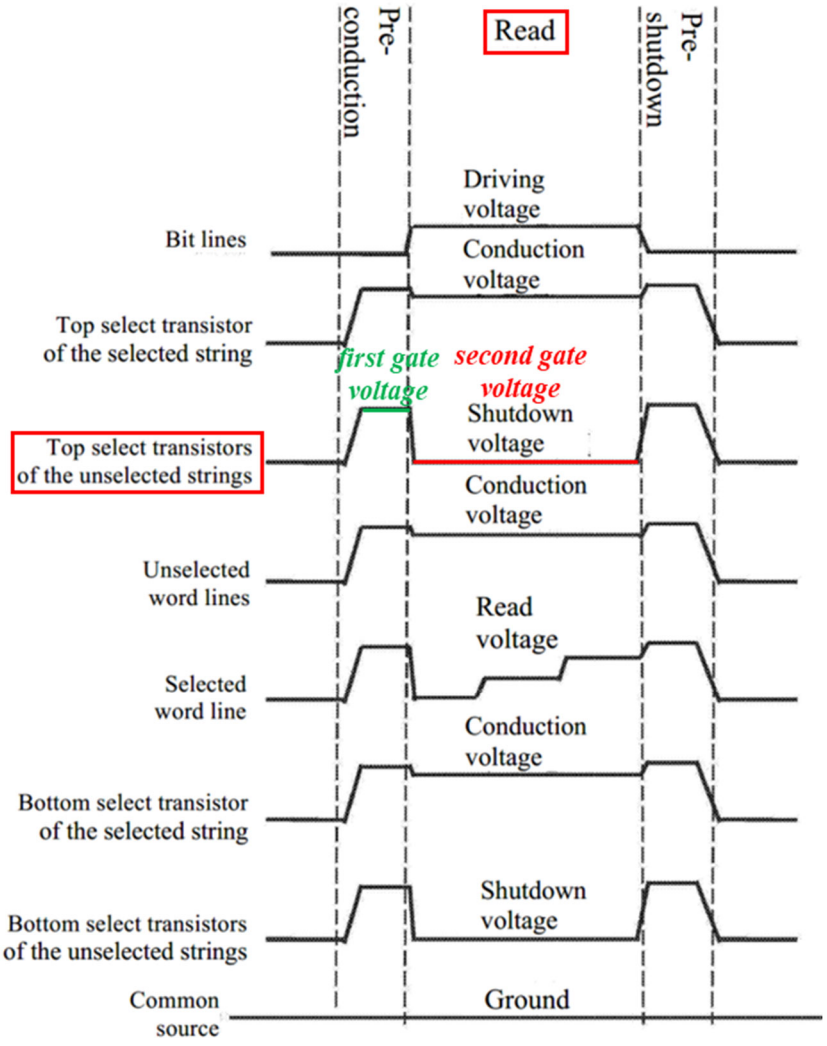
The verify stage corresponds to Hongtao's "read phase." *Supra* §§IX.A.5-IX.A.6; Liu, ¶ 150.

7. [4.B.i]

Hongtao discloses this limitation.

This limitation refers to the same transistor in claim [4.A.i]. *Supra* §IX.D.3. The *second gate voltage* is shown below:

[9] Although these references are to Figure 4, the waveforms during the pre-pulse stage in Figures 4, 6, and 8 are identical.

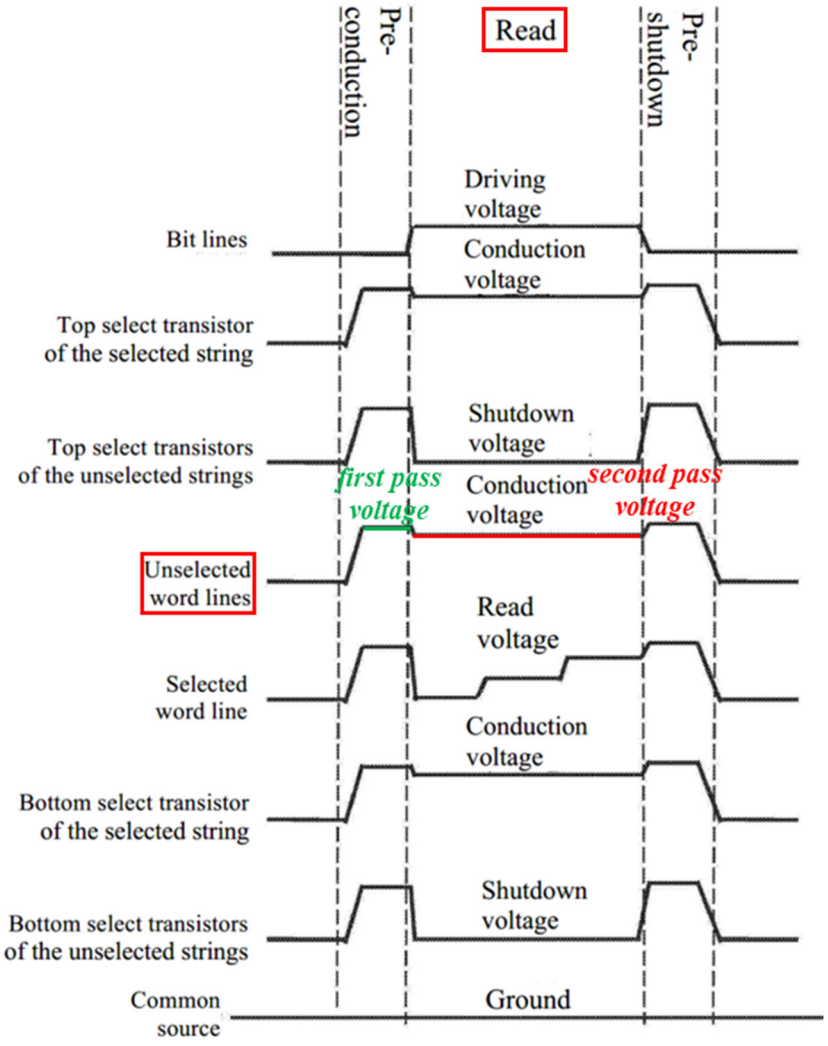


Hongtao, Fig. 2. This "[s]hutdown voltage" or "disconnection voltage" turns off the *TSG* of the unselected memory string (*second*), in a similar fashion as many '957 embodiments. *Compare* Hongtao, [0008], [0012], [0019], [0024], [0034] *with* Ex 1001, Fig. 6; Liu, ¶¶ 151-152.

8. [4.B.ii]

Hongtao in view of Yu renders this limitation obvious.

This limitation refers to the same transistor in claim [4.A.ii]. *Supra* §IX.D.4. The *second pass voltage* is shown below:



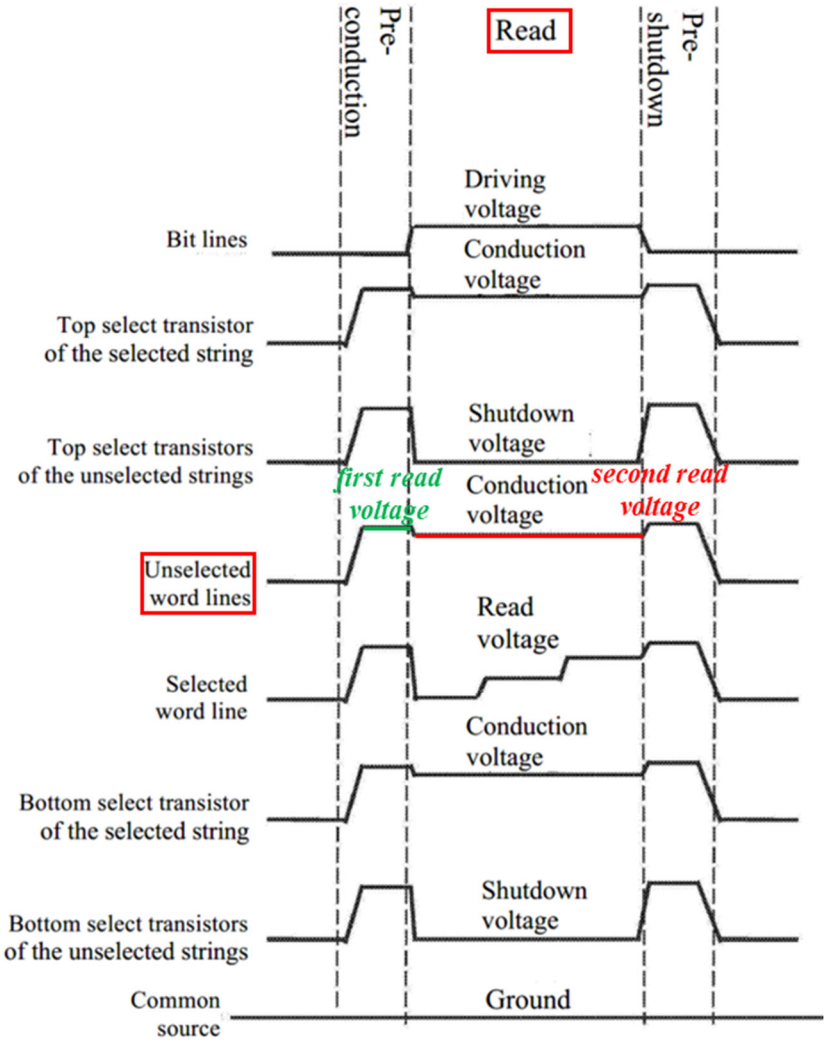
Hongtao, Fig. 2, [0019], [0025]; Liu, ¶¶ 153-154.

9. [4.B.iii]

Hongtao in view of Yu renders this limitation obvious.

This limitation refers to the same transistor in claim [4.A.iii]. *Supra* §IX.D.5.

The *second read voltage* is shown below:



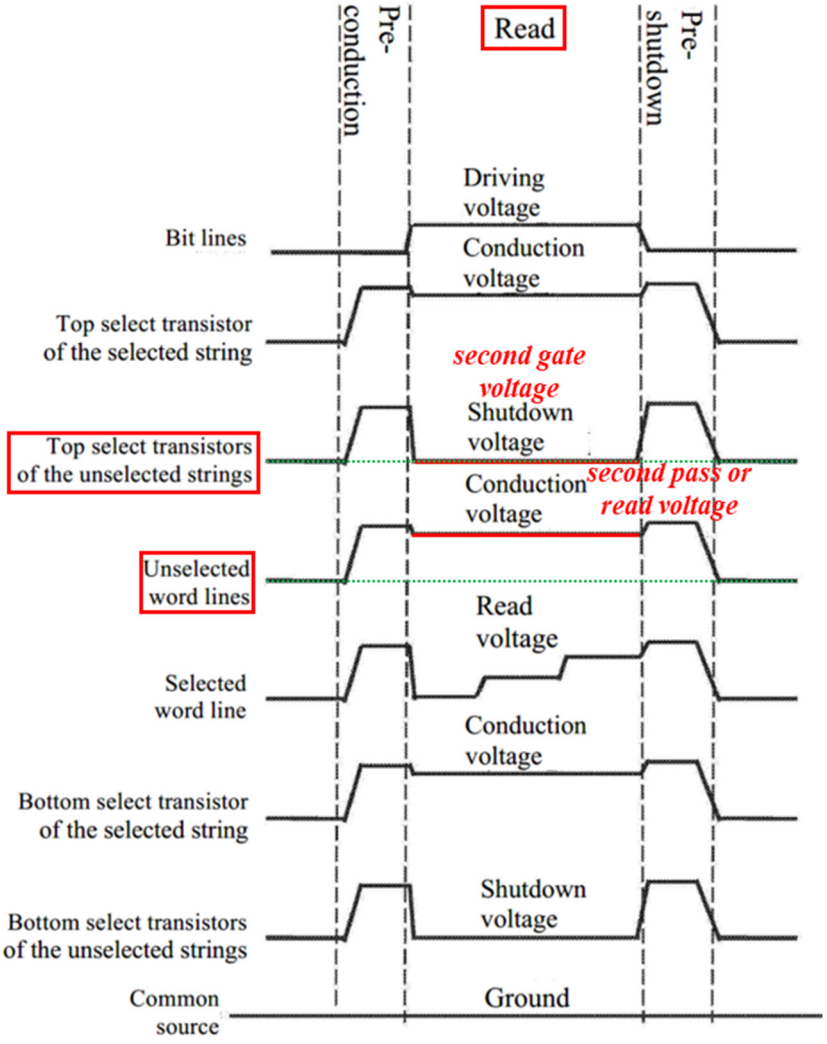
Hongtao, Fig. 2, [0019], [0025]; Liu, ¶¶ 155-156.

10. [4.C]

Hongtao in view of Yu renders this limitation obvious.

Both the *second pass voltage* and the *second read voltage* are Hongtao's conduction voltage. *Supra* §§IX.D.8-9. The *second gate voltage* is Hongtao's shutdown voltage or disconnection voltage. *Supra* §IX.D.7. The conduction voltage turns on a memory cell while the shutdown voltage turns off the TSG. *See, e.g.*,

Hongtao, [0008], [0019], [0025], [0034]. Thus, *the second pass voltage and the second read voltage [are] larger than the second gate voltage*:



Id., Fig. 2; Liu, ¶¶ 157-158.

E. Claim 5:

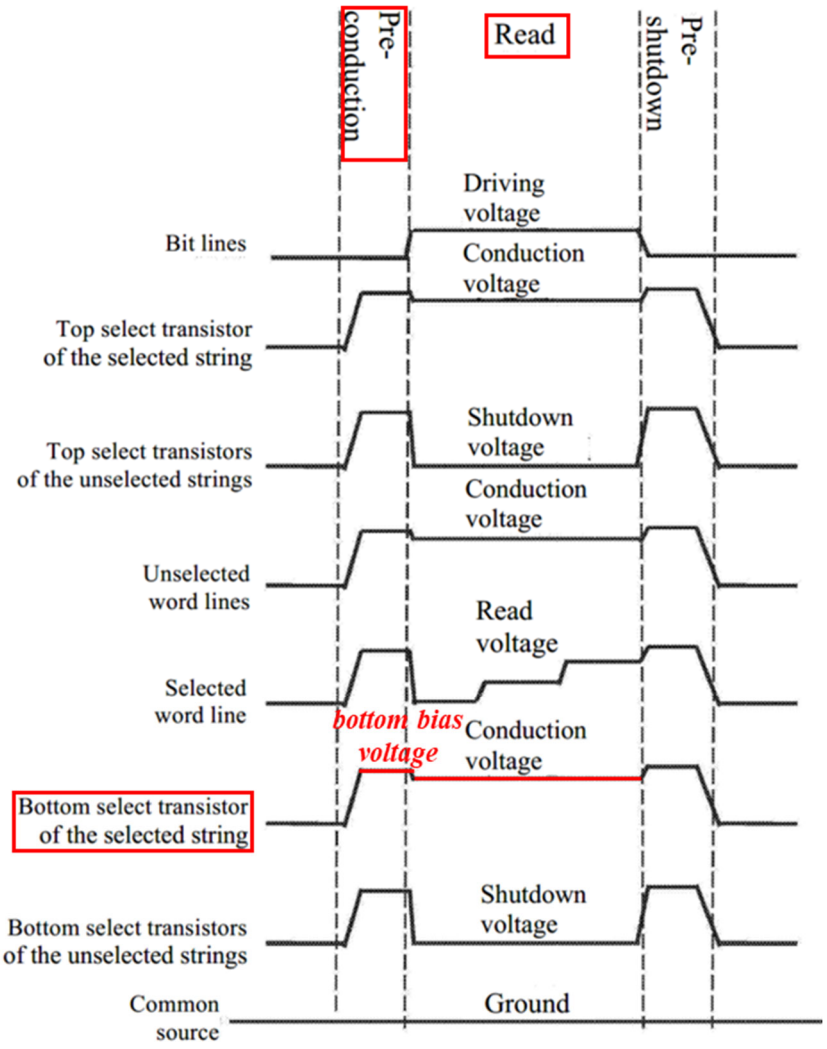
1. [5.PRE]

Hongtao discloses or at least renders obvious *processing circuitry further configure to* perform the limitations of claim 5. *Supra* §IX.A.2; Liu, ¶ 159.

2. [5.A]

Hongtao in view of Yu renders this limitation obvious.

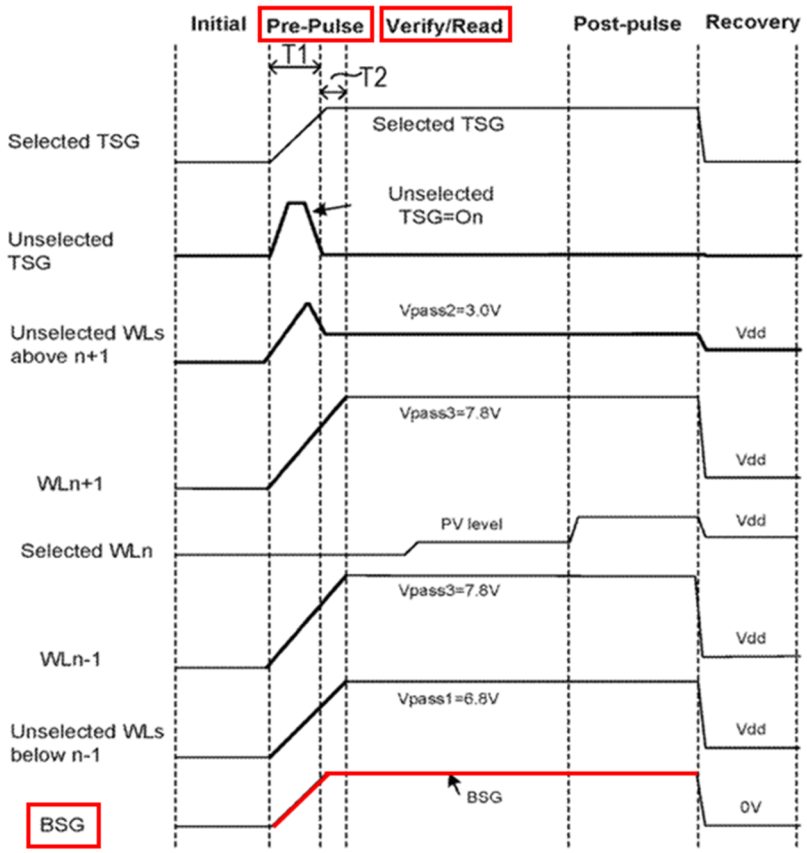
Hongtao discloses *apply[ing] a bottom bias voltage* (a pre-conduction voltage and conduction voltage) *on … the BSG transistor of the first memory cell string* (the selected string) *in the pre-verify stage* (the pre-conduction phase) *and the verify stage* (the read phase):



Hongtao, Fig. 2, [0023], [0025]. The conduction voltage is high enough to "turn on" the bottom select (BSG) transistor. *Id.*, [0019]; Liu, ¶¶ 160-162.

To the extent that Patent Owner argues "a bottom bias voltage" must have only one voltage level, Patent Owner is wrong.

The '957 patent discloses that a bottom bias voltage may "be increased from the initial voltage to a voltage that is maintained through the second portion of the pre-verify stage and the verify stage." Ex. 1001, 2:56-59, 4:4-7:

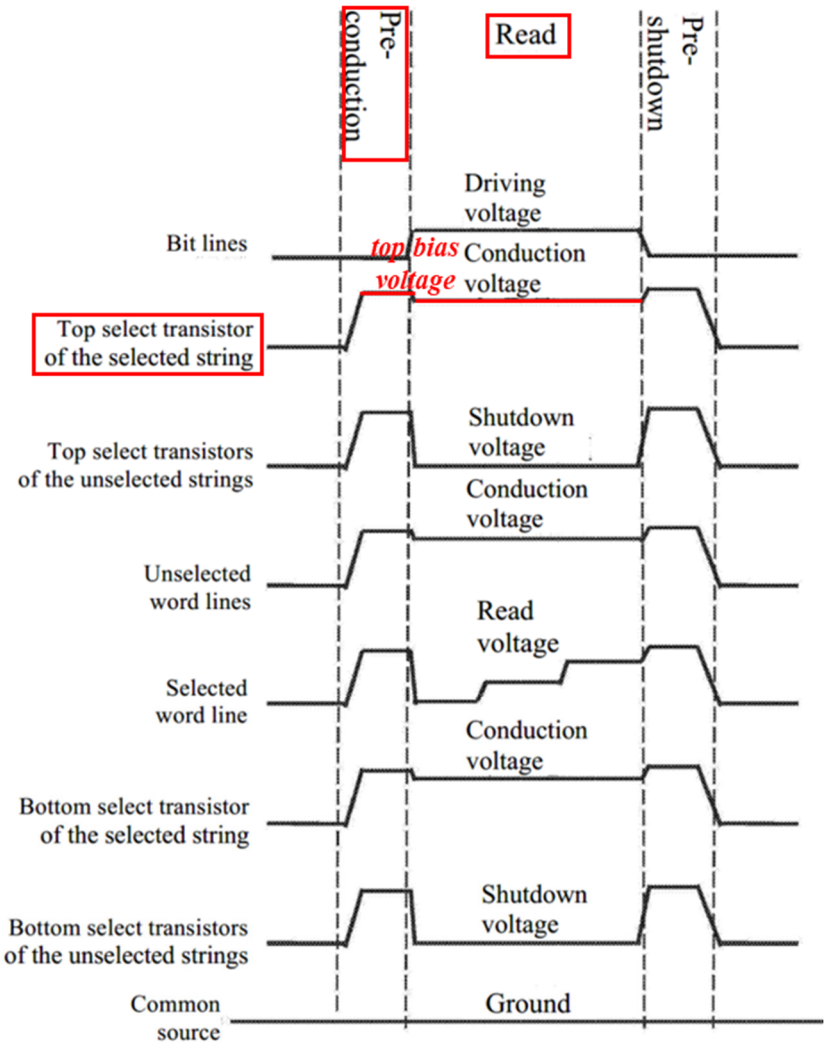


Id., Fig. 7, 13:43-47. Based on the disclosure, the bottom bias voltage may have more than one voltage level. Liu, ¶¶ 163-164; *Elkay Mfg. Co. v. Ebco Mfg. Co.*, 192 F.3d 973, 977 (Fed. Cir. 1999) ("a" can mean more than one).

3. [5.B]

Hongtao in view of Yu renders this limitation obvious.

Hongtao discloses *apply[ing] a top bias voltage* (a pre-conduction voltage and conduction voltage) *on … the TSG transistor of the first memory cell string* (the selected string) *in the pre-verify stage* (the pre-conduction phase) *and the verify stage* (the read phase):



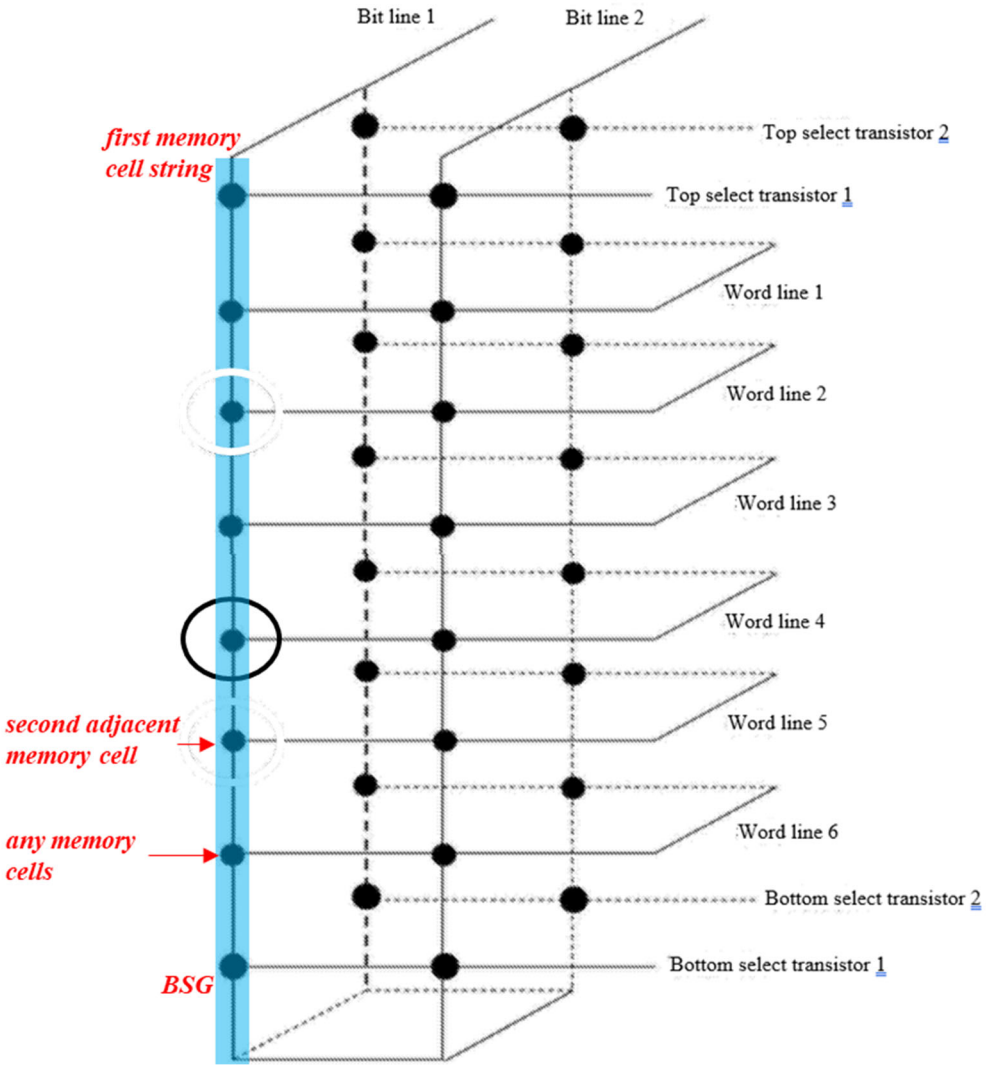
Hongtao, Fig. 2; *id.*, Abstract, [0023], [0025]. The pre-conduction and conduction voltages are high enough to turn on the top select (TSG) transistor. *Id.*, [0006], [0019].

Like the bottom bias voltage, a top bias voltage also need not have only one voltage level for the same reasons. *Supra* §IX.E.2; Ex. 1001, 2:59-61, 4:7-9; 13:49-53, Fig. 7; Liu, ¶¶ 165-167.

4. [5.C]

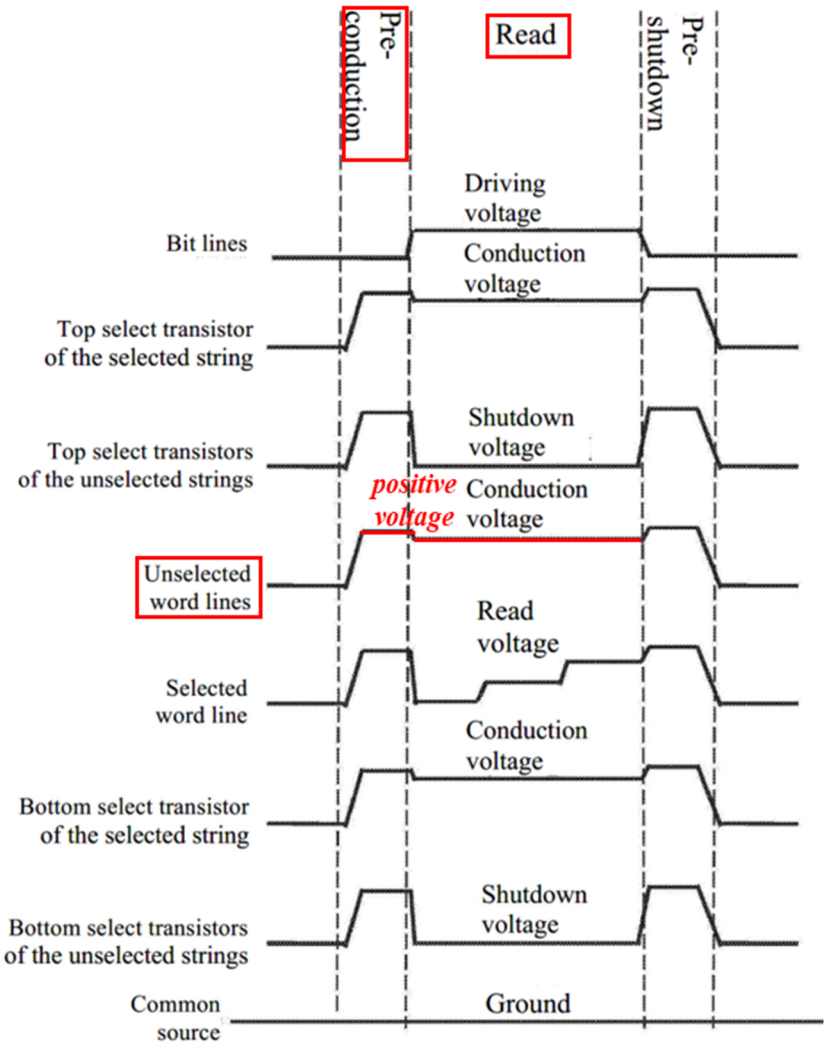
Hongtao in view of Yu renders this limitation obvious.

The *any memory cells* may be *positioned* as shown:



Hongtao, Fig. 1 (expanded). *See* §IX.B.1 (for obvious extension of Hongtao's memory string).

Hongtao discloses *apply[ing] a positive voltage* (a pre-conduction voltage and conduction voltage) *on … any memory cells that are positioned* (at word line 6) *between the second adjacent memory cell of the selected memory cell and the BSG transistor of the first memory cell string* (the selected string) *in the pre-verify stage* (the pre-conduction phase) *and the verify stage* (the read phase):

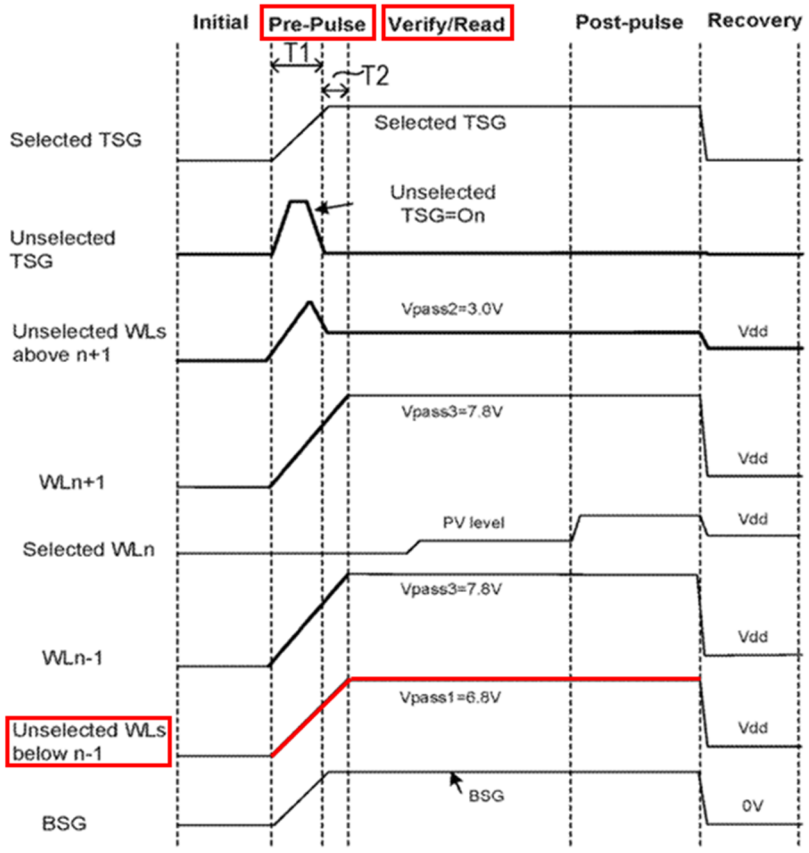


Hongtao, Fig. 2; Liu, ¶¶ 168-170.

To the extent that Patent Owner argues "a positive voltage" must have only one voltage level or that it must be a voltage distinct from the bias voltages, Patent Owner is wrong.

The '957 patent discloses that a positive voltage may "be increased from the initial voltage in the pre-verify stage." Ex. 1001, 2:62-63, 4:10-11. Indeed, the '957

patent refers to different levels of voltages as "*the* positive voltage." *Id.*, 13:54-58 (describing Figure 7).



Id., Fig. 7. Thus, a positive voltage may have more than one voltage level. *Elkay Mfg.*, 192 F.3d at 977.

Moreover, a *positive voltage* and a *bias voltage* need not be distinct voltages. Notably, the '957 patent twice equates bias voltages with positive voltages. Ex. 1001, 11:7-9, 11:39. In fact, the patent refers to the (positive) voltage applied to word lines between the second adjacent memory cell and the BSG transistor ("WLs (<n-1)") as a "bias voltage." *Id.* 11:7-10, 11:39-41; Liu, ¶¶ 171-173.

F. Claim 6:

1. [6.PRE]

Hongtao discloses or at least renders obvious *processing circuitry further configured to* perform the limitations of claim 6. *Supra* §IX.A.2; Liu, ¶ 174.

2. [6.A]

This limitation is identical to claim [5.A]. Hongtao in view of Yu renders this limitation obvious for the same reasons. *Supra* §IX.E.2; Liu, ¶ 175.

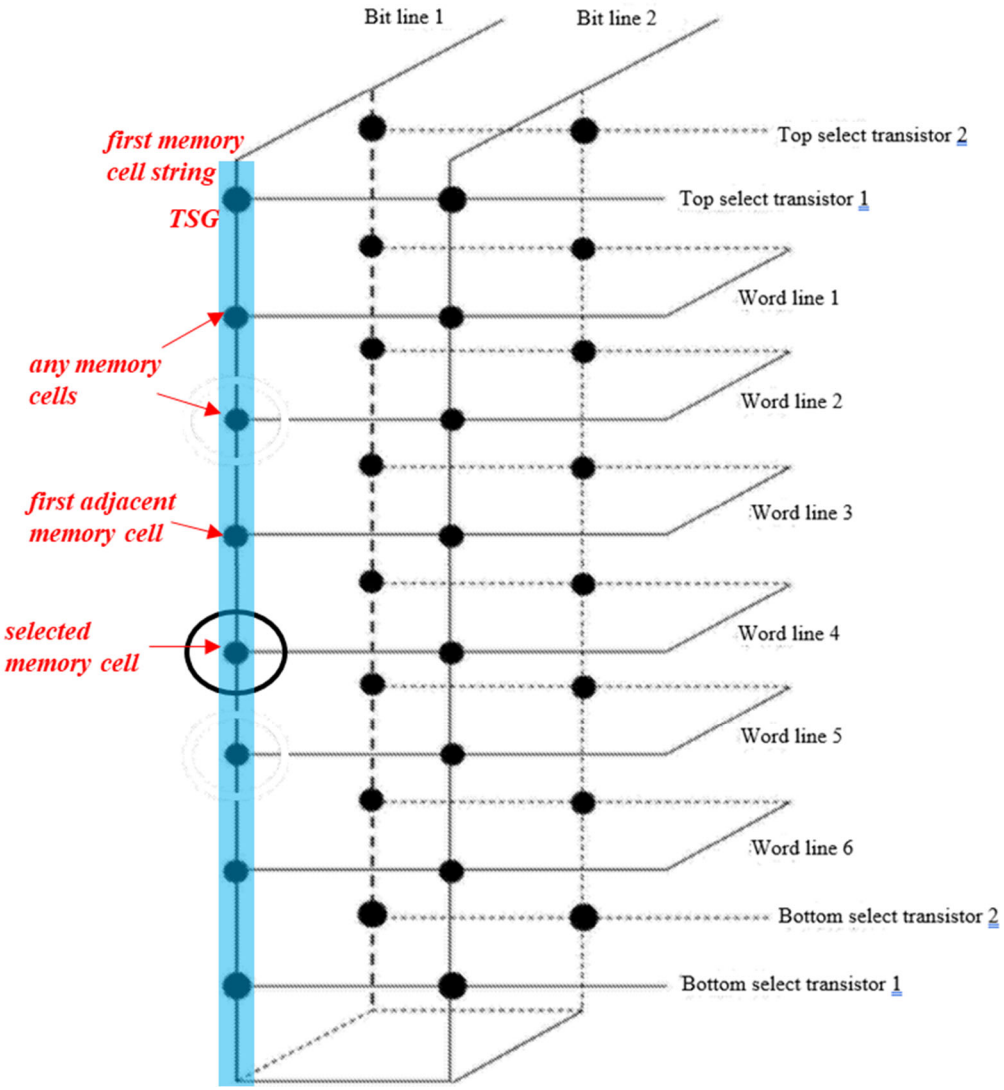
3. [6.B]

This limitation is identical to claim [5.B]. Hongtao in view of Yu renders this limitation obvious for the same reasons. *Supra* §IX.E.3; Liu, ¶ 176.

4. [6.C]

Hongtao discloses or at least renders obvious this limitation.

This limitation is the mirror image of claim [5.C], reciting any memory cells that are positioned above the first adjacent cell. The *any memory cells* may be *positioned* as shown:



Hongtao, Fig. 1 (expanded). *See* §IX.B.1 (for obvious extension of Hongtao's memory string).

Because Hongtao's positive voltage is applied on all unselected word lines, including those above and below the selected memory cell, Hongtao discloses or at least renders obvious this limitation for the same reasons explained with respect to claim [5.C]. *Supra* §IX.E.4; Liu, ¶¶ 177-179.

G. Motivation to Combine

Yu also demonstrates a POSITA's knowledge with respect to the basic concept of programming order and verification. As this Section demonstrates, use of these two concepts in Hongtao would have been obvious simply in view of this knowledge as well. This Section, however, also addresses the motivation to combine Hongtao and Yu.[10]

Programming Order

A POSITA would have been motivated, with a reasonable expectation of success, to apply Yu's teaching on programming order to Hongtao's memory device for several reasons. Liu, ¶ 180.

First, while Hongtao discloses read operations, it is silent on program operations. A memory that is read was programmed. Thus, a POSITA would have been motivated to consider Yu's programming teachings. Indeed, both Hongtao and Yu disclose 3D NAND devices with similar structures, making Yu's programming teachings particularly applicable to Hongtao. Hongtao, Abstract, Fig. 1; Yu, [0004], Fig. 6. Liu, ¶ 181.

[10] To the extent Yu is used to render processing circuitry obvious, a POSITA would have found it obvious to combine Yu with Hongtao's with a reasonable expectation of success. Liu, ¶ 196 n.3.

Second, both Hongtao and Yu are directed to reducing disturbance during memory operations. Hongtao, [0026], [0034]-[0035]; Yu, [0005]-[0006], [0010]. Thus, a POSITA would have been motivated to apply Yu's disturbance-reducing programming techniques to complement Hongtao's disturbance-reducing reading techniques. Combining them would contribute to Hongtao's goal to "improve the accuracy of … data." Hongtao, [0004]; Liu, ¶ 182.

Third, a sequential program order simplifies controller decoding operation. Liu, ¶ 183. Such advantages would have motivated a POSITA to adopt Yu's programming sequence. *Id.*

Fourth, sequential programming provides the benefit of easily knowing that either the rows above or below are programmed (and the other rows are erased). *Id.*, ¶ 184. Thus, that known state is taken into account when attempting to mitigate issues relating to access operations, e.g., for programming. Ex. 1023, 8:18-52.

Fifth, at bottom, it would be necessary to implement a programming scheme for Hongtao's device. Yu's sequential program order represents an advantageous, conventional approach. Liu, ¶ 185.

A POSITA would have had a reasonable expectation of success in applying Yu's well-known technique to Hongtao. First, per above, both Hongtao and Yu are in the context of 3D NAND devices. Second, the sequential program order was conventional, textbook material, and such implementation merely involves using a

pointer to identify the next-to-program row. Ex. 1014, 45 (Fig. 2.12); Ex. 1021, [0110]-[0112]. Again, per above, such an approach actually simplifies decoder operation. Liu, ¶ 186.

Using Read to Verify

A POSITA would have been motivated, with a reasonable expectation of success, to employ Hongtao's read operations in a program-verification loop in view of Yu and the knowledge of a POSITA for several reasons. Liu, ¶ 187.

As an initial matter, Yu discloses: "Each program loop may include a program operation and a program verification operation." Yu, [0049]. This refers to the basic programming process of non-volatile memory. *See* §V.A.2; Liu, ¶ 188.

First, it was well known that read operations and verify operations are virtually identical. *Supra* §V.A.2 (citing Exs. 1017, 1019-1021). Indeed, "the read operation may include the verification read operation for verifying the success of the program operation or the normal read operation for determining the data stored in the memory cells." Ex. 1021, [0103]. Further, it was well known that the program loop requires cycles of a program operation and a verification. Yu, [0049]; §V.A.2. And of course, programming is a fundamental use of a non-volatile memory. Thus, a POSITA would have been motivated to use Hongtao's read operation as a verification operation to enable programming. Liu, ¶ 189.

Second, as is evident from Hongtao, the specifics of a read operation are important to reduce disturb issues. §VIII.A. There are a host of similar issues relating to read operations. §VIII.C-E. For example, the read can inadvertently alter the data state of the target and other memory cells. The same problem exists when verifying, because verification is merely a read operation. Thus, a POSITA would have been motivated to employ Hongtao's read operation, which reduces these problems, for verification. Liu, ¶ 190.

Third, as is evident from Hongtao (as well as Suzuki, Costa, and Seo), the specifics of a read operation are tuned to address the issues that can inadvertently alter data states. A POSITA would have been motivated to use the same, fine-tuned read operation for verification and not "reinvent the wheel." Liu, ¶ 191.

A POSITA would have had a reasonable expectation of success in employing Hongtao's read operation for verification. First, it was well known that a read operation can be used for "the normal read operation" or for "verifying the success of the program operation." Ex. 1021, [0103]. Second, it was known how to use a read operation for verification (namely, slightly adjusting the read voltage on the selected word line during the verification stage to the verify voltage), which was conventional. *See* Ex. 1024, [0181], Ex. 1019, 25:2-8; Ex. 1021, [0054]-[0055]. There is just a slight difference in these voltages, because, for example, the verify voltage may be set to the low end of the threshold distribution and the read voltage

is between data states (for a multi-level cell). Ex. 1019, 25:2-8. The voltages on other memory elements are the same as the read operation, because those voltages are meant to mitigate issues relating to inadvertently altering data states. Third, Hongtao already discloses circuitry to generate different read voltage levels. Thus, generating additional levels for verify operations simply uses this same type of circuitry. Liu, ¶¶ 192-195.

Finally, while fast-charge loss is an issue for verification in charge-trap memories, the claims of the '957 patent are not limited to charge-trap memories. Regardless, even if one were to consider charge-trap memories, accounting for this issue during verification was known. *E.g.*, Suzuki, [0150]; Liu, ¶ 196.

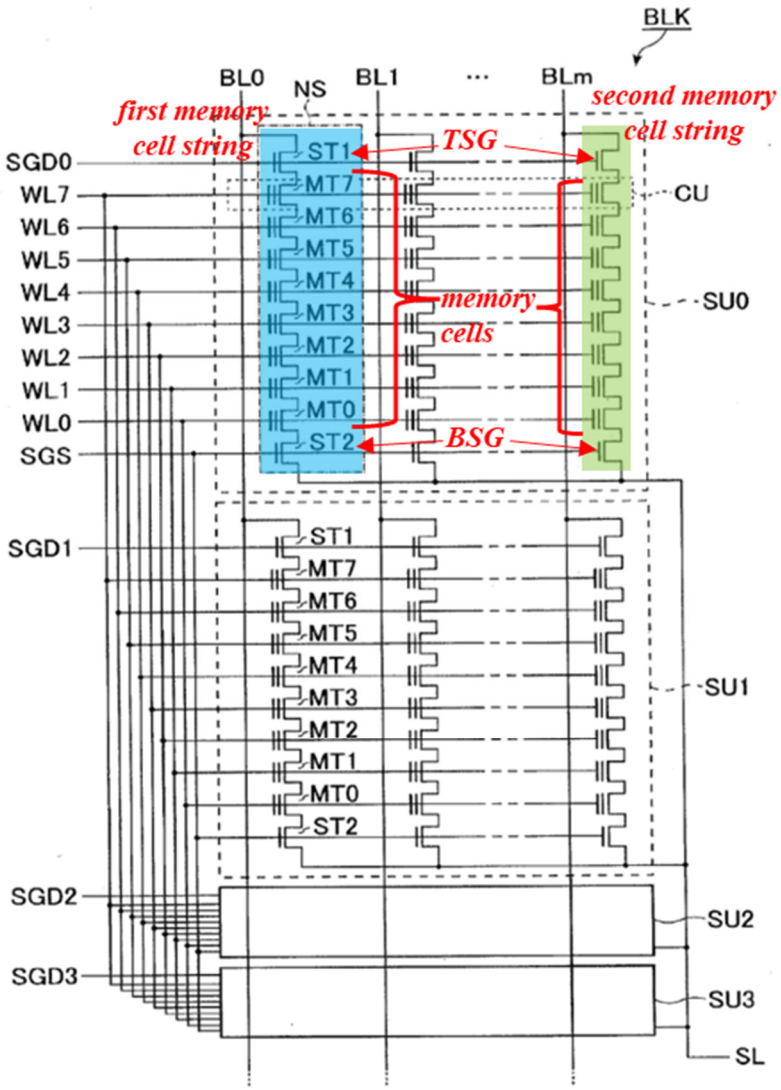
X. GROUND 2: CLAIMS 1-6 ARE ANTICIPATED BY SUZUKI

A. Claim 1:

1. [1.PRE]

To the extent the preamble is limiting, Suzuki discloses it.

Suzuki discloses a semiconductor device comprising drain select transistors (*TSG transistor*), source select transistors (*BSG transistors*), and *memory cells*. Suzuki, Abstract. This device is configured to execute a program operation and a verify operation and is *an apparatus for reading a memory device*. *Id.* It includes multiple memory strings such as *a first memory cell string* (highlighted blue) *and a second memory cell string* (green):

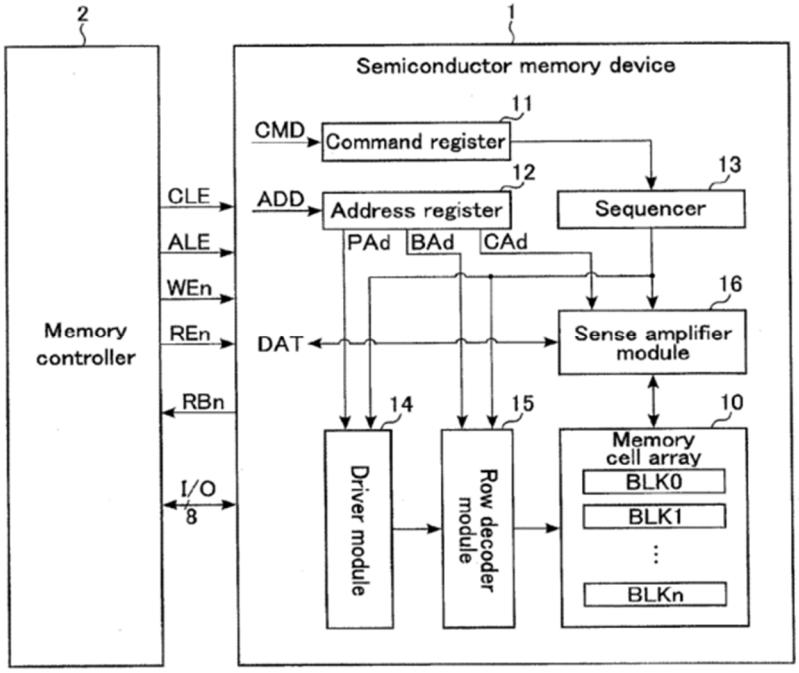


Id., Fig. 2; *see also id.*, [0049] (*connected in series*); [0047]-[0050]; [0048], [0232] (each memory string comprising a drain select transistor ST1 and a source select transistor ST2); Liu, ¶¶ 199-200.

2. [1.A]

Suzuki describes that its controller is configured to execute verify operations. Suzuki, Abstract, [0028]. The controller in conjunction with components including

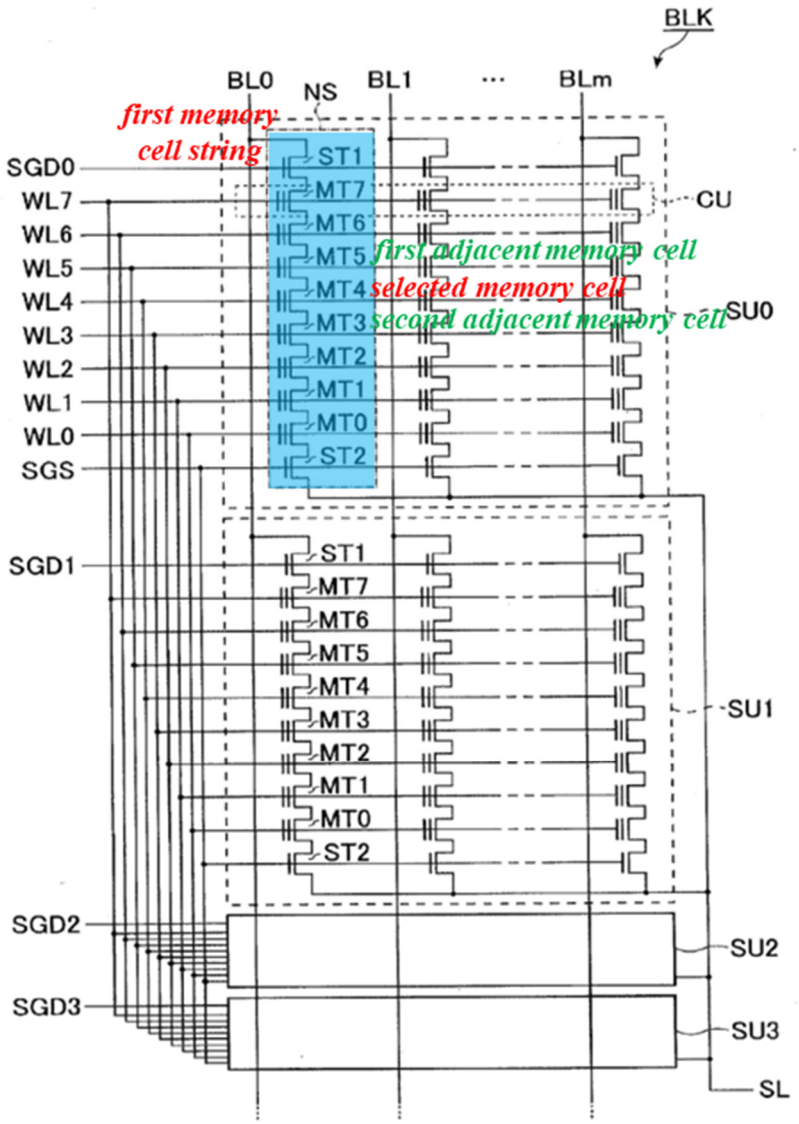
a driver module and a row decoder ("*processing circuitry*") apply various voltages in the verify and pre-verify operations. *Id.*, [0038]-[0040], [0117].



Id., Fig. 1; *see also id.*, [0034], Fig. 3; Liu, ¶ 201.

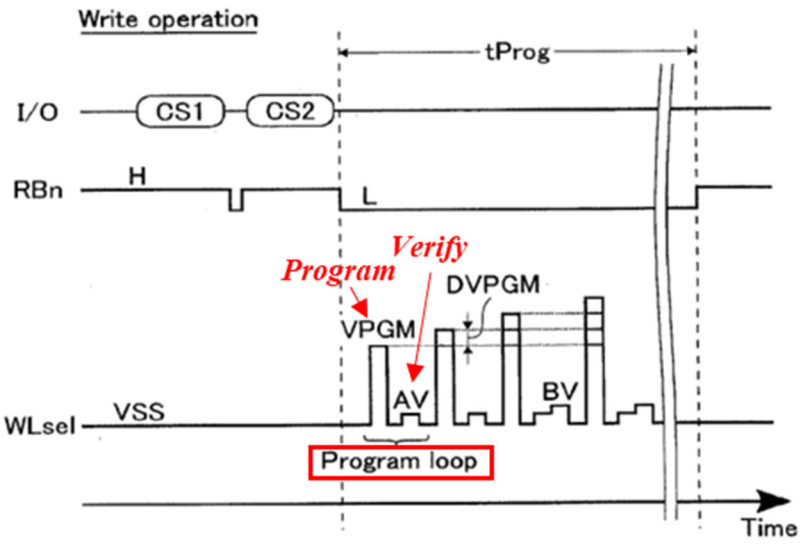
3. [1.A.i]

As to the *memory cell*, Suzuki discloses operations to verify a "memory cell transistor MT." Suzuki, [0125]. For purposes of illustration, the discussion herein chooses MT4 as *a selected memory cell of the first memory cell string*:



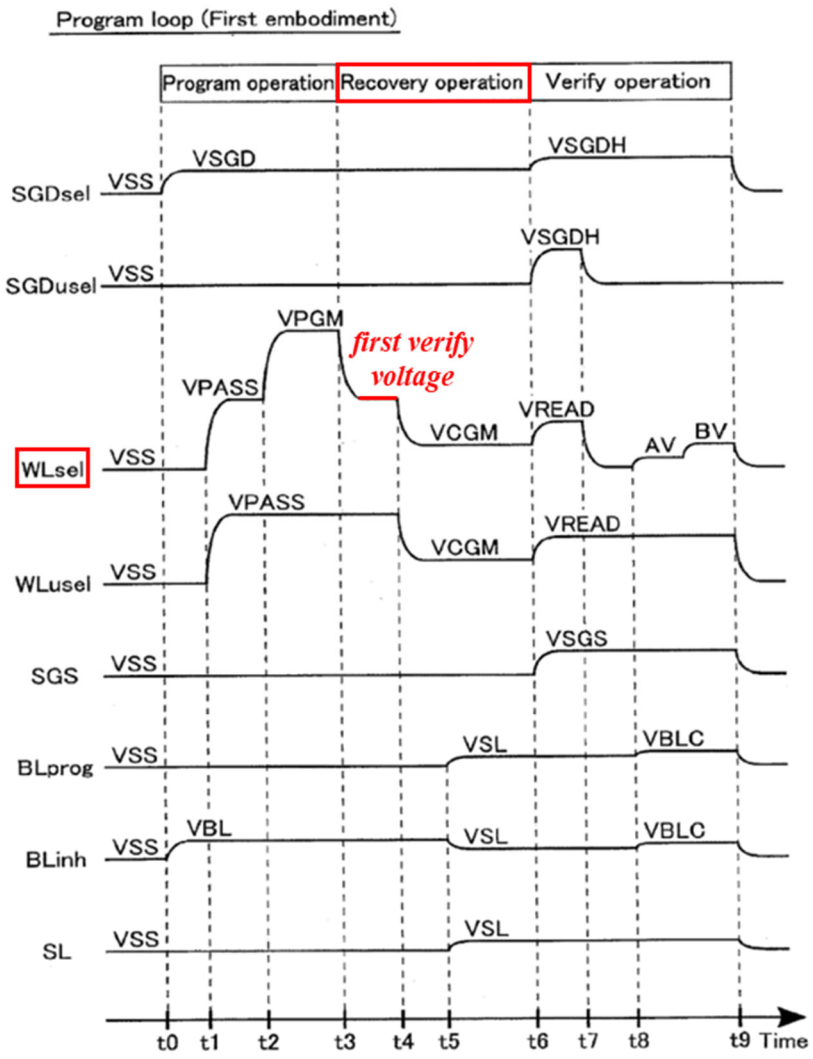
Id., Fig. 2. As shown, MT4 *[is] arranged between a first adjacent memory cell* (MT5) *and a second adjacent memory cell* (MT3).

Suzuki discloses a program loop comprising a program operation followed by a verify operation. *Id.*, Abstract, [0124]-[0125]. The sequence is illustrated below:



Id., Fig. 10, [0122]. Accordingly, at the time the *selected memory cell* undergoes verification, it is *programmed*. Liu, ¶¶ 202-203.

As explained above, the gate terminal of a memory cell is coupled to a word line. *Supra* §V.A.1. Suzuki refers to "a selected word line … as WLsel." Suzuki, [0117]. Suzuki further discloses applying voltage VPASS to Wlsel at time t3 in a recovery operation before the verify operation, i.e., *in a pre-verify stage*. *Id.*, [0137].



Id., Fig. 11. This VPASS constitutes *a first verify voltage on ... [the] selected memory cell*. Liu, ¶ 204 (describing that Vpass is a term of art that turns on a transistor).

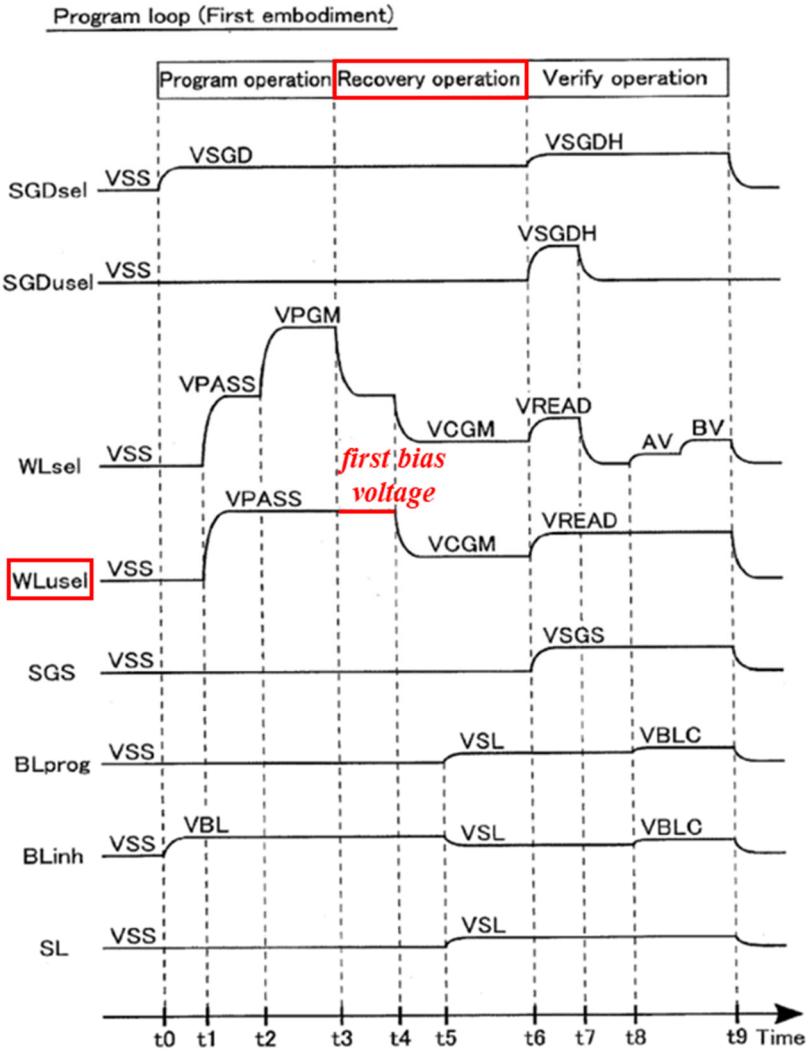
Note that Suzuki's recovery operation is a *pre-verify stage*. The claims of the '957 patent provide no indication of what the *pre-verify stage* is other than that the pre-verify stage occurs before ("pre-") the verify stage. From the figures of the '957 patent, we also know that the *pre-verify stage* comes before, but is a separate phase

from, the *verify stage*. Ex. 1001, Figs. 4-9. The specification largely just repeats what occurs in the pre-verify stage without any discussion of when it occurs (other than before the verify stage). *E.g., id.*, Abstract. Elsewhere, the specification states the purpose of the "pre-verify scheme" is to assist in the "verify/read [of] programmed memory cells." *Id.*, 7:13-18. There is no lexicography or disclaimers that would limit the ordinary meaning of "pre-verify stage." Liu, ¶ 205.

Like the '957 patent, Suzuki's "recovery period" is separate from, and comes before, the verify step. Suzuki, Fig. 11. Specifically, Suzuki discloses that "a period from time t0 to time t3 corresponds to a program operation, a period from time t3 to time t6 corresponds to a recovery operation, and a period from time t6 to time t9 corresponds to a verify operation." *Id.*, [0131]. At t3, the programming operation is complete, because VPGM terminates. *Id.*, [0137]. The recovery operation functions to recover from the program operation and prepare for what follows, namely, a verify operation. *Id.*, [0131]. Indeed, Suzuki discloses the program loop of Figure 11 (*see* above), in which what occurs after the program loop is necessarily preparing for the pending verification. Thus, a POSITA would have understood the recovery period to correspond to the "pre-verify stage" of the '957 patent. Liu, ¶ 206.

4. [1.A.ii]

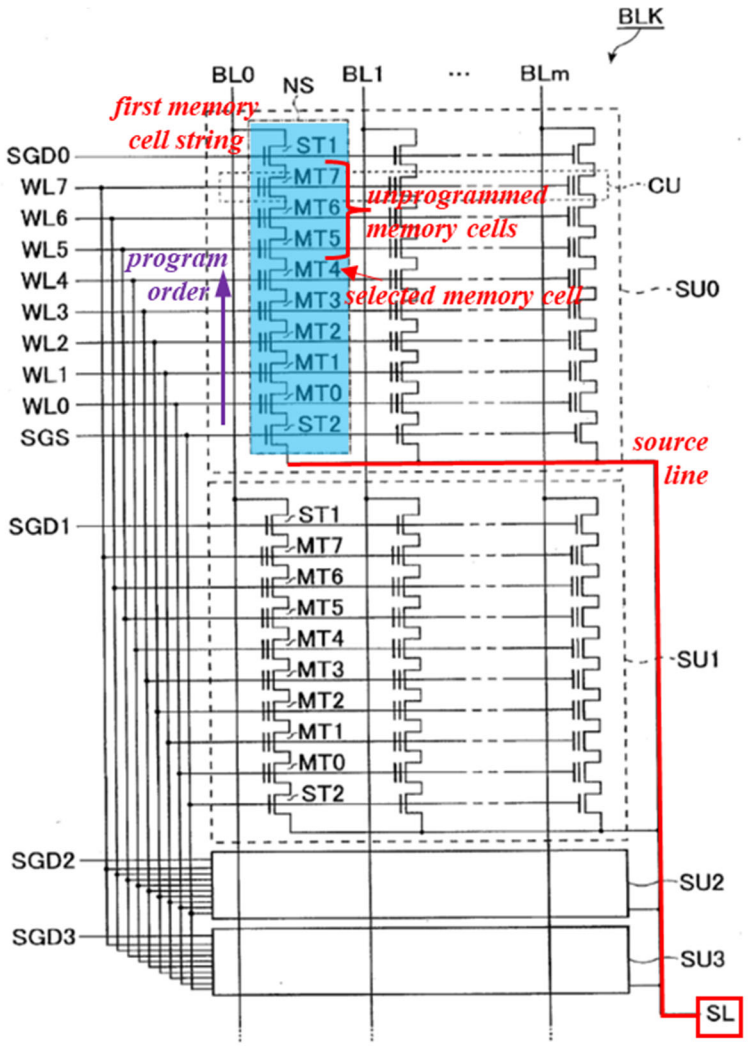
Suzuki refers to "non-selected word line[s]" as Wlusel. Suzuki, [0117]. *[I]n the pre-verify stage*, voltage VPASS is applied to Wlusel:



Id., Fig. 11; *see also id.*, [0134]. The unselected word lines are coupled to, e.g., unselected memory cells MT5 through MT7 in the illustrated scenario. *Supra* §X.A.3. Thus, Suzuki discloses applying *a first bias voltage* (VPASS) *on … at least*

one memory cell (e.g., MT6 or MT7) *of the first memory cell string* (the selected string).

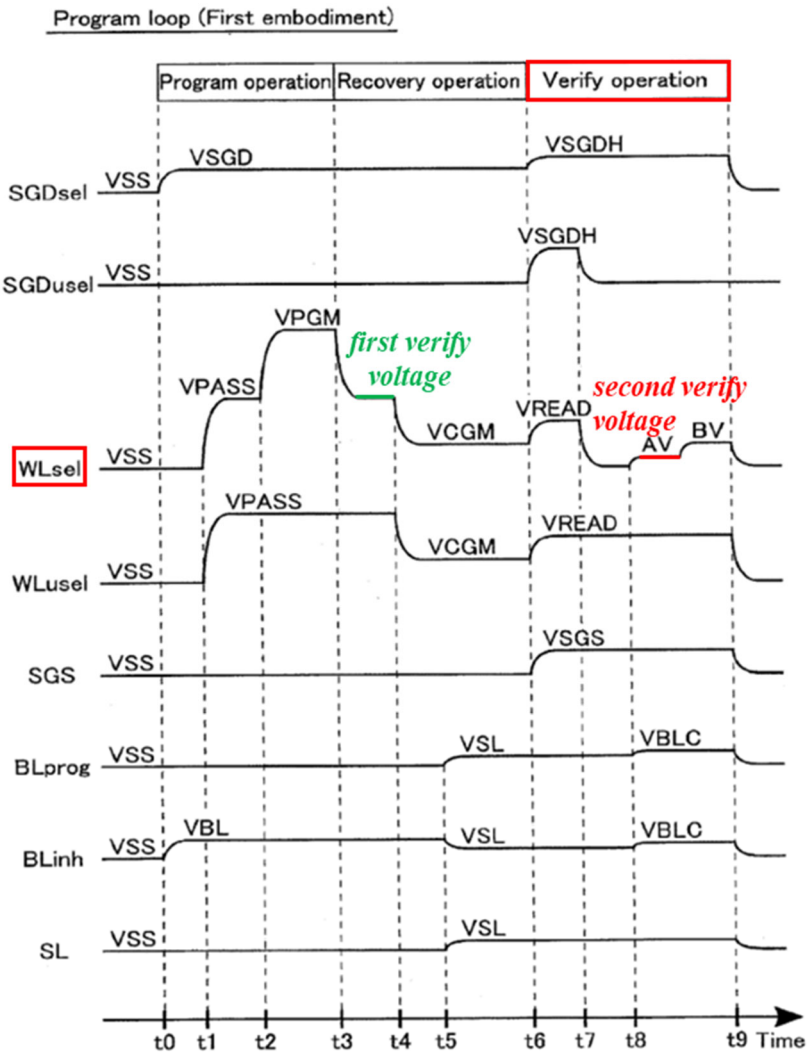
Suzuki discloses that this *at least one memory cell* (e.g., MT6 or MT7) *... is not programmed*. In Suzuki's embodiment, memory cell MT0 is at the end of the source line side. And the program operation may proceed "from cell units CU on the source line SL side in sequence." Suzuki, [0116].



Id., Fig. 2. Thus, when MT4 is selected for programming verification, MT6 and MT7 are not programmed. *Id.*, [0140]; Liu, ¶¶ 207-208.

5. [1.A.iii]

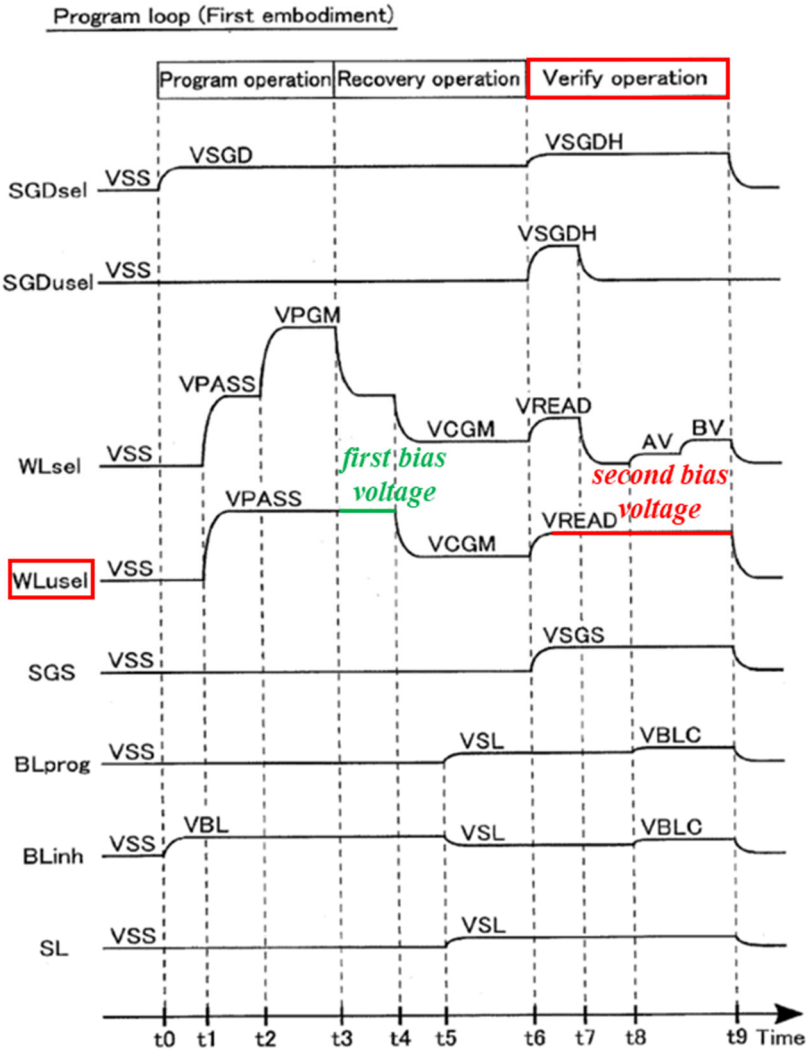
Suzuki discloses *apply[ing], in a verify stage* (verify operation)*, a second verify voltage* (verify voltage AV) *on … the selected memory cell* (e.g., MT4) *of the first memory cell string*.



Suzuki, Fig. 11, [0144]; Liu, ¶ 209.

6. [1.A.iv]

Suzuki discloses applying *a second bias voltage* (VREAD) through the same unselected word lines to *the at least one memory cell in the verify stage*:

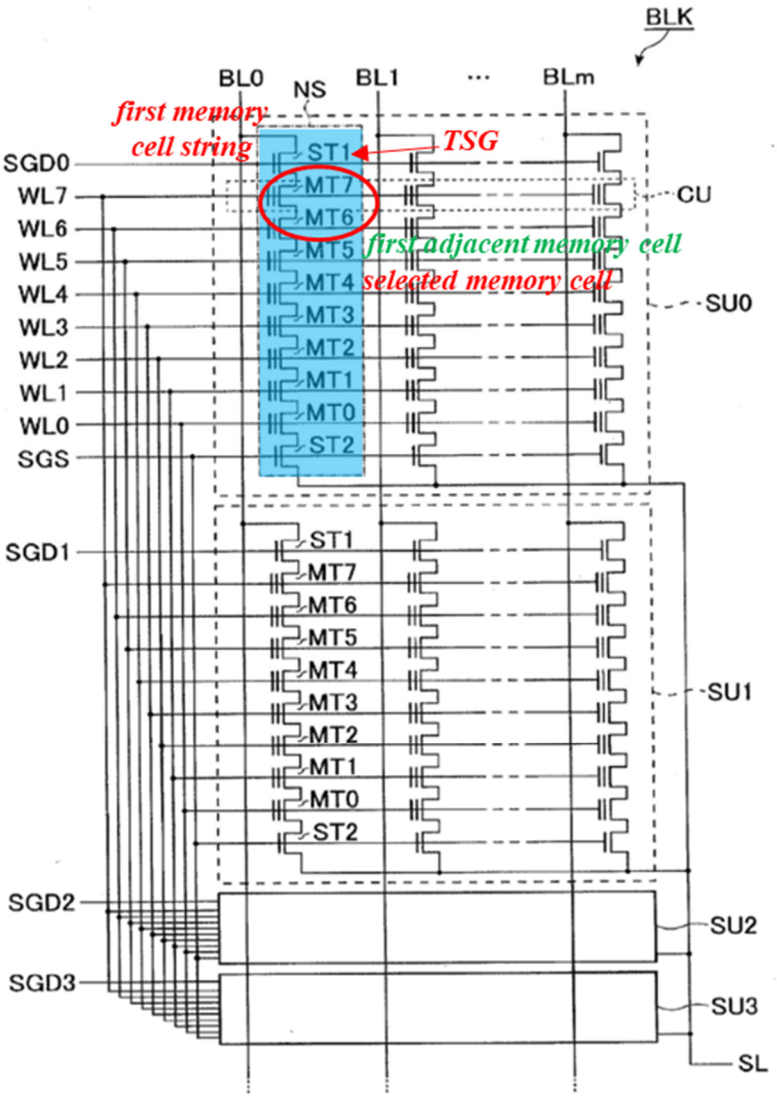


Suzuki, Fig. 11; *see also id.*, [0142]. VREAD may be 8V. *Id.* VPASS may be 10V. *Id.*, [0134]. Thus, *the second bias voltage* (VREAD) *is smaller than the first bias voltage* (VPASS). Liu, ¶ 210.

B. Claim 2:

1. [2]

Claim 2 refers to the *not programmed memory cell* of claim [1.A.ii] and [1.A.iv]. That memory cell can be MT6 or MT7. *See* §§X.A.4, X.A.6. Either MT6 or MT7 satisfies this limitation:



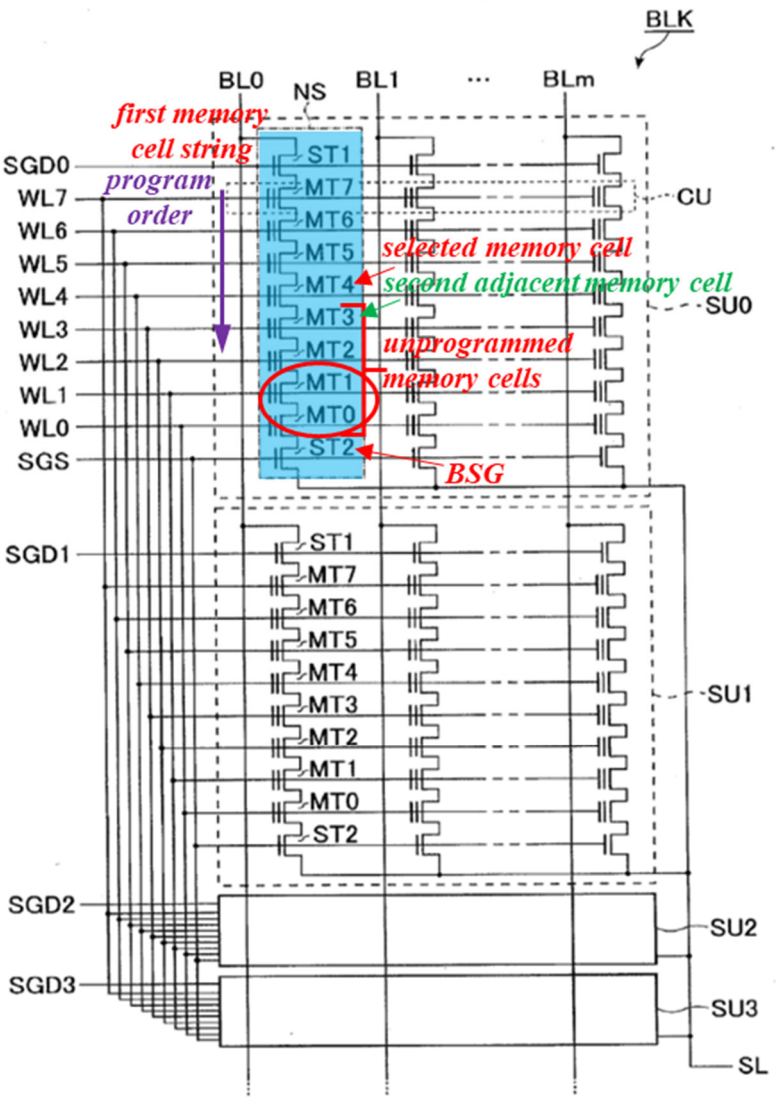
Suzuki, Fig. 2; *see also id.*, [0232] (drain select transistor ST1 is the *TSG*); Liu, ¶ 211.

C. Claim 3:

1. [3]

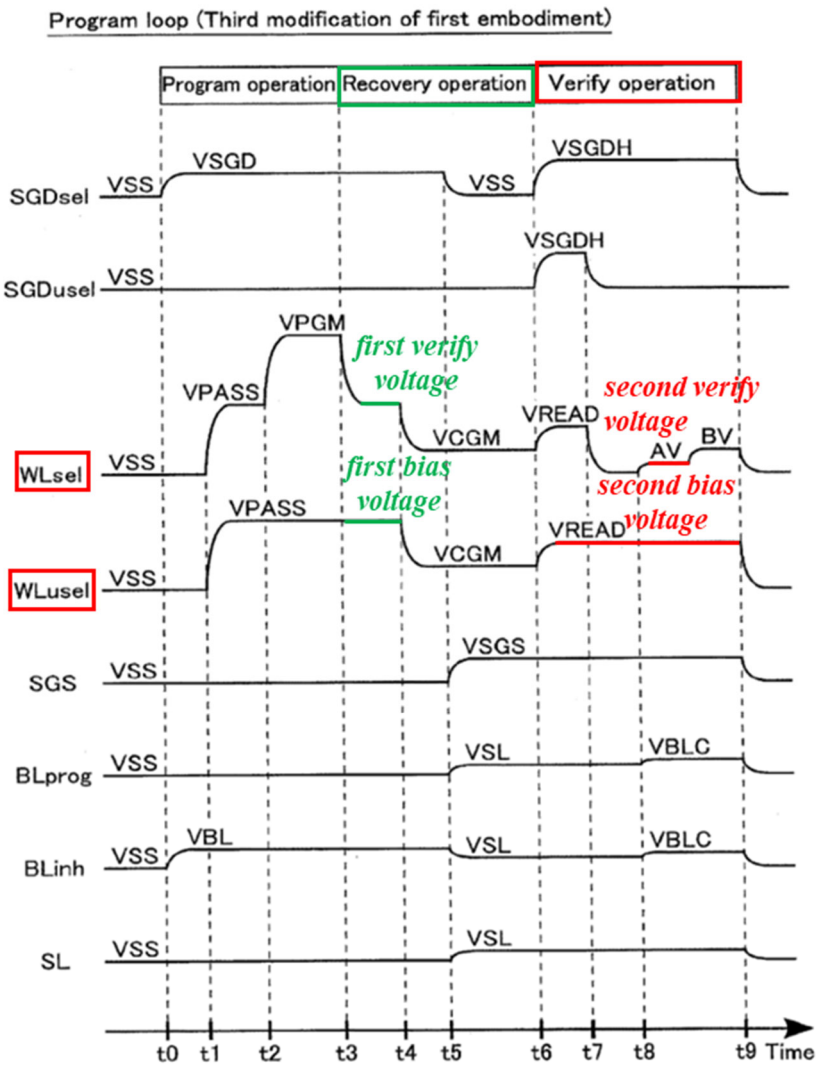
As explained in Ground 1, claim 3 requires an unprogrammed memory cell positioned *below* the second adjacent memory cell. *Supra* §IX.C.

Claims 1 and 2 above have been described using an embodiment wherein the drain side contains the last cell (e.g., MT6 and MT7) to be programmed. Suzuki further discloses, however, that programming can proceed from the drain side to the source side. Suzuki, [0170]. This can be illustrated as follows:



Id., Fig. 2. In this embodiment, the *selected memory cell* may still be MT4, and the *at least one memory cell* may be, e.g., MT0 or MT1 and is unprogrammed, because of the drain-to-source directional programming.

This embodiment satisfies claim 3 as shown:



Id., Fig. 16; *see also id.*, [0171]-[0174] (describing modifications from Figure 11 to Figure 16 that are irrelevant to claim 3); Liu, ¶¶ 212-214.

D. Claim 4:

1. [4.PRE]

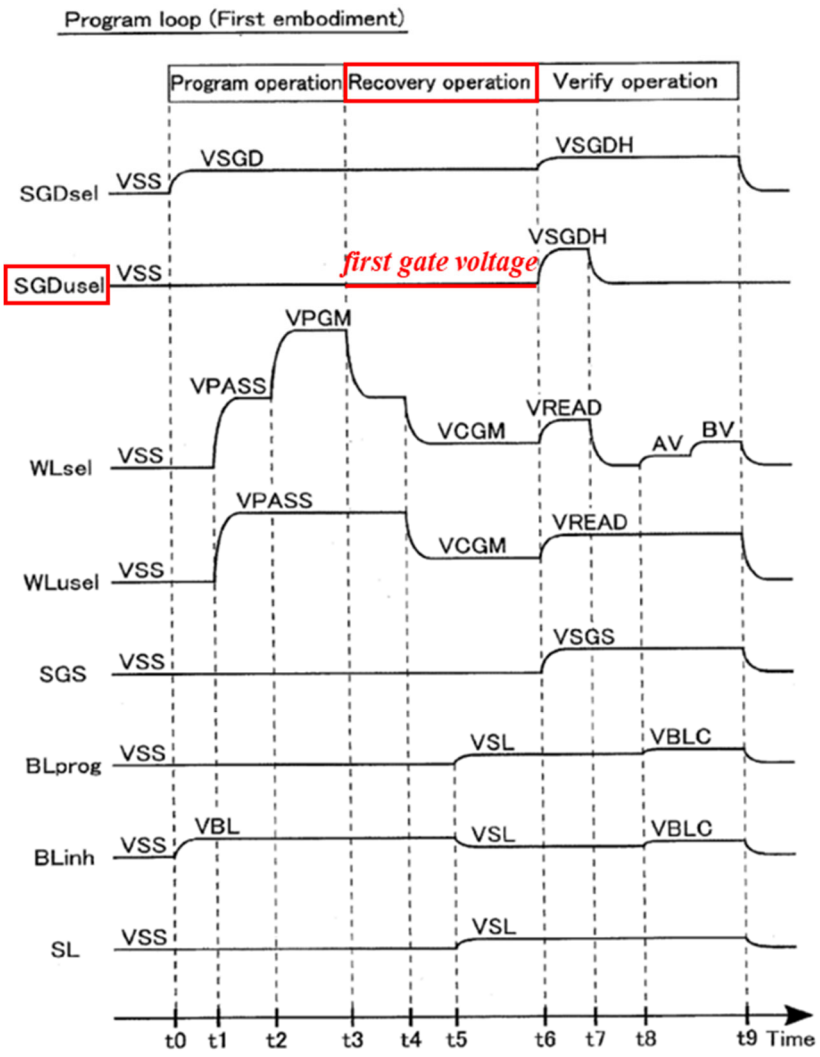
Suzuki discloses *processing circuitry further configured to* perform the limitations of claim 4. *See* §X.A.2; Liu, ¶ 215.

2. [4.A]

The pre-verify stage corresponds to Suzuki's "recovery operation." *Supra* §§X.A.3-XI.A.4; Liu, ¶ 216.

3. [4.A.i]

The second memory cell string is an unselected memory string since the selected memory cell is the first memory cell string. Ex. 1001, 17:41-43 (limitation [1.A.i]). Further, based on the specific context of the '957 patent, a ground or zero voltage can be "applied." *Id.*, 10:57-61, 11:19-23, 11:35-39. Suzuki refers to the line coupled to *TSG transistor of the [unselected,] second memory cell string* as SGDusel. Suzuki, [0117]. Suzuki discloses *apply[ing] a first gate voltage* to this *TSG transistor*:

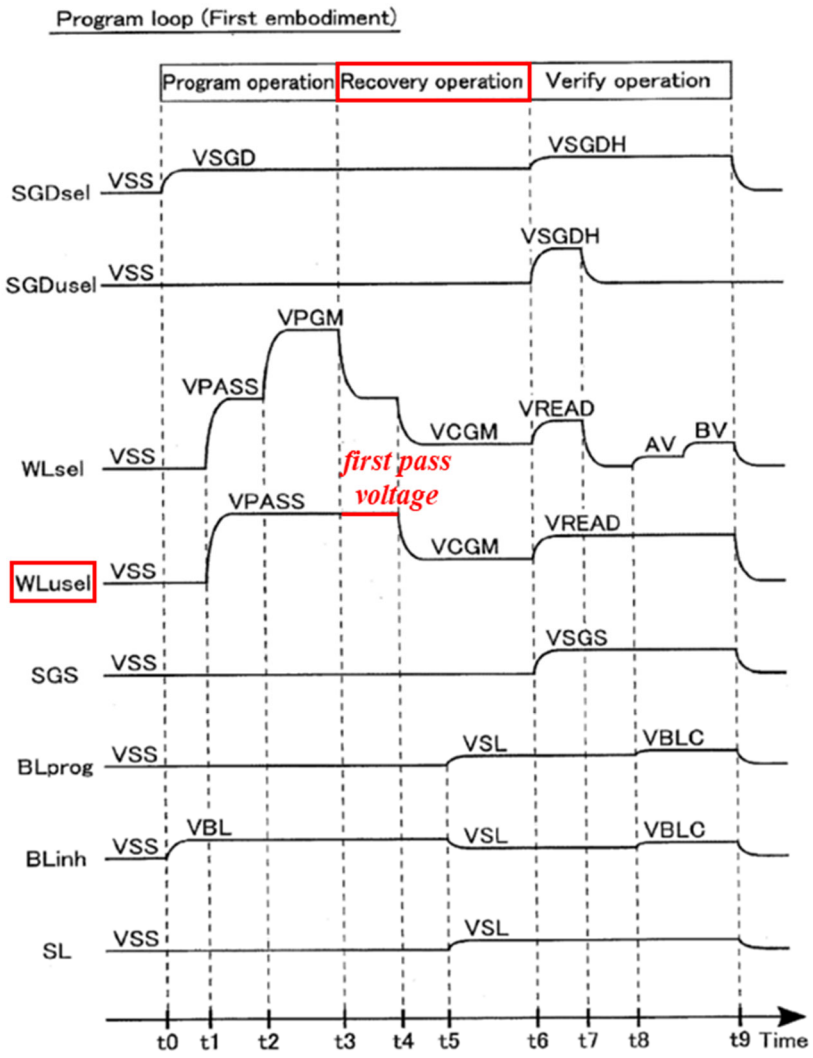


Suzuki, Fig. 11; *see also id.*, [0130]; Liu, ¶ 217.

4. [4.A.ii]

Suzuki discloses applying voltage VPASS to Wlusel. *Supra* §X.A.4. Wlusel includes WL5, coupled to *the first adjacent memory cell of the selected memory cell*. *Id.* As explained in Ground 1, the '957 patent does not require the first bias voltage of claim 1 and the first pass voltage of claim 4 to have different values, or even that

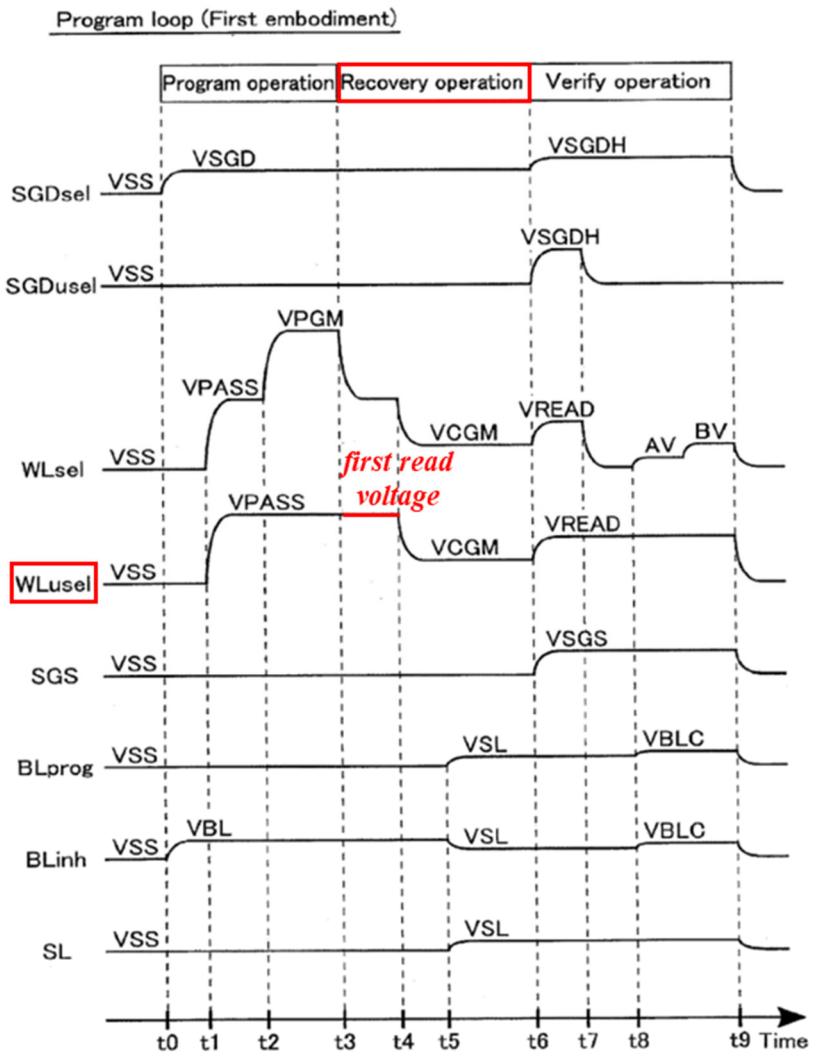
they be distinct voltages. *See* §IX.D.4. Thus, VPASS may constitute *a first pass voltage*.



Suzuki, Fig. 11; Liu, ¶ 218.

5. [4.A.iii]

Suzuki discloses applying the VPASS voltage to unselected word lines in the *pre-verify stage* (recovery operation).



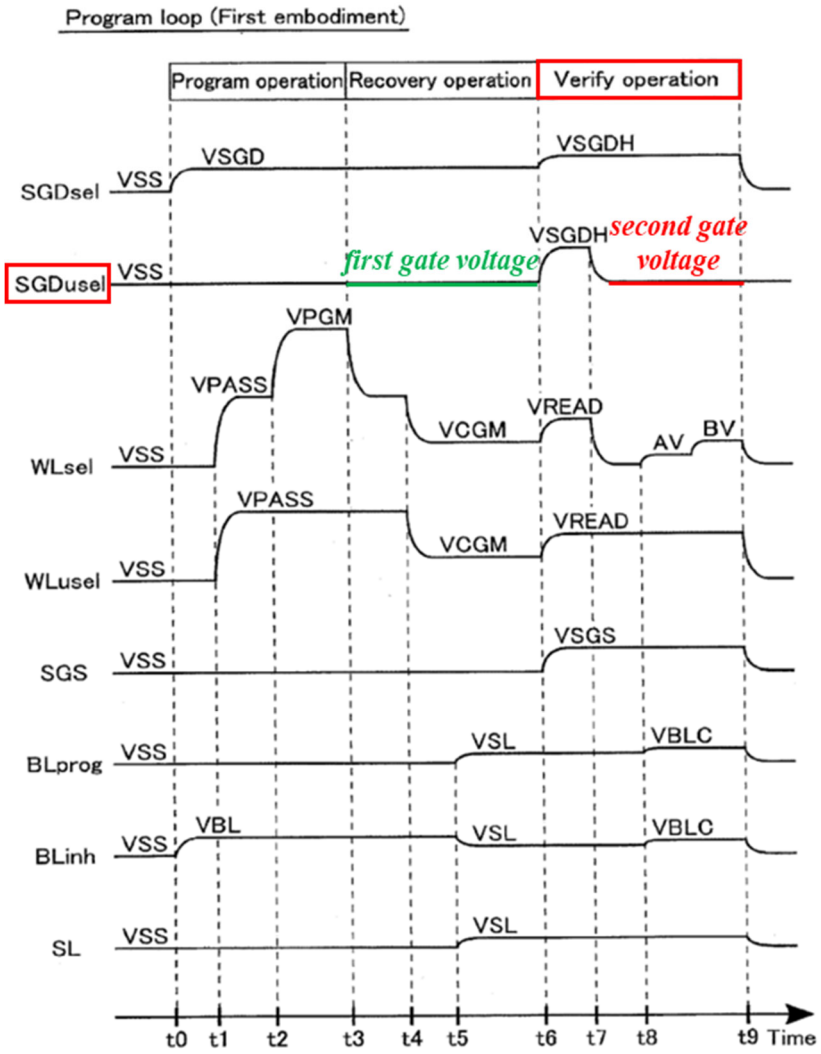
Suzuki, Fig. 11. As explained in Ground 1, the '957 patent does not require the first bias voltage of claim 1 and the first read voltage of claim 4 to have different values, or even that they be distinct voltages. *Supra* §IX.D.5. Thus, this voltage constitutes the *first read voltage on … the second adjacent memory cell* (e.g., MT3) *… in the first memory cell string*. Liu, ¶ 219.

6. [4.B]

The verify stage corresponds to Suzuki's "verify operation." *Supra* §§X.A.5-XI.A.6; Liu, ¶ 220.

7. [4.B.i]

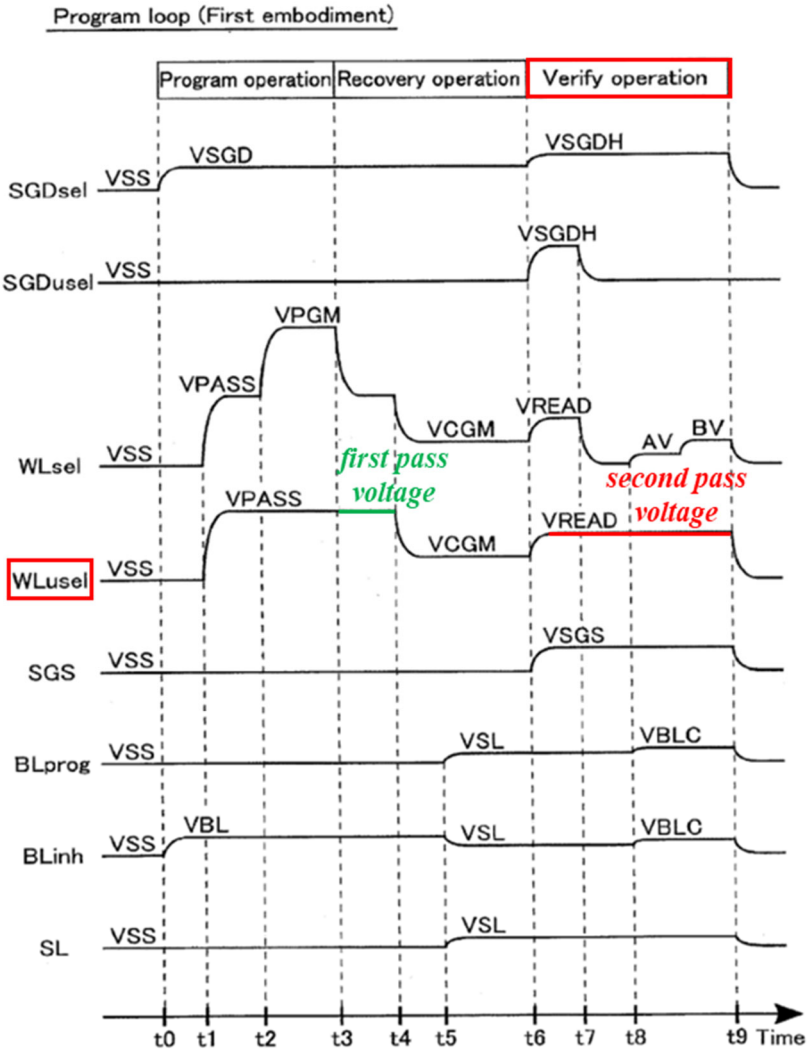
This limitation refers to the same transistor in claim [4.A.i] during the subsequent verify stage. *Supra* §X.D.3. The *second gate voltage* is shown below:



Suzuki, Fig. 11. This VSS voltage turns off the source select transistor. *Id.*, [0143]; Liu, ¶ 221.

8. [4.B.ii]

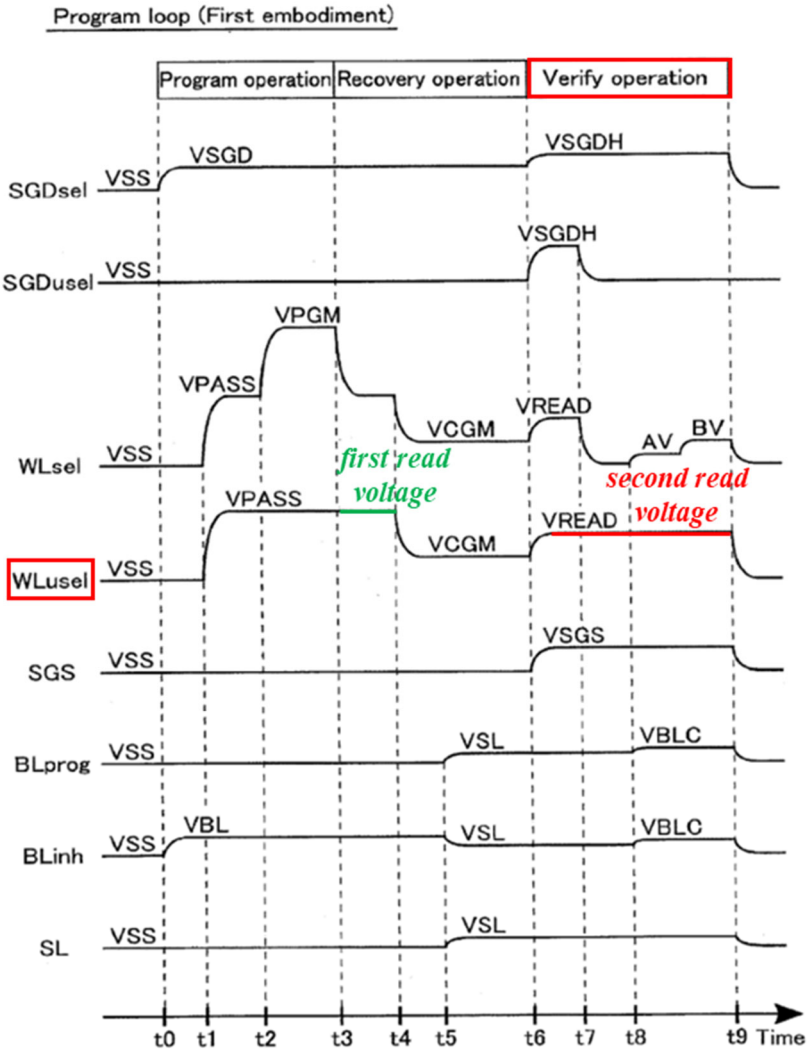
This limitation refers to the same transistor in claim [4.A.ii] during the subsequent verify stage. *Supra* §X.D.4. The *second pass voltage* is shown below:



Suzuki, Fig. 11; *id.*, [0142]. Vread is, for example, 8 volts and turns on those transistors and is a pass voltage. *Id.*; Liu, ¶ 222.

9. [4.B.iii]

This limitation refers to the same transistor in claim [4.A.iii] during the subsequent verify stage. *Supra* §X.D.5. The *second read voltage* is shown below:



Suzuki, Fig. 11; *id.*, [0142]; Liu, ¶ 223.

10. [4.C]

Both the *second pass voltage* and the *second read voltage* are Suzuki's VREAD. *Supra* §§X.D.8-9. The second gate voltage is VSS. *Supra* §X.D.7.

VREAD may be 8V. Suzuki, [0142]. VSS may be 0V. *Id.*, [0130]. Thus, *the second pass voltage and the second read voltage [are] larger than the second gate voltage*.[11] Liu, ¶¶ 224-225.

E. Claim 5:

1. [5.PRE]

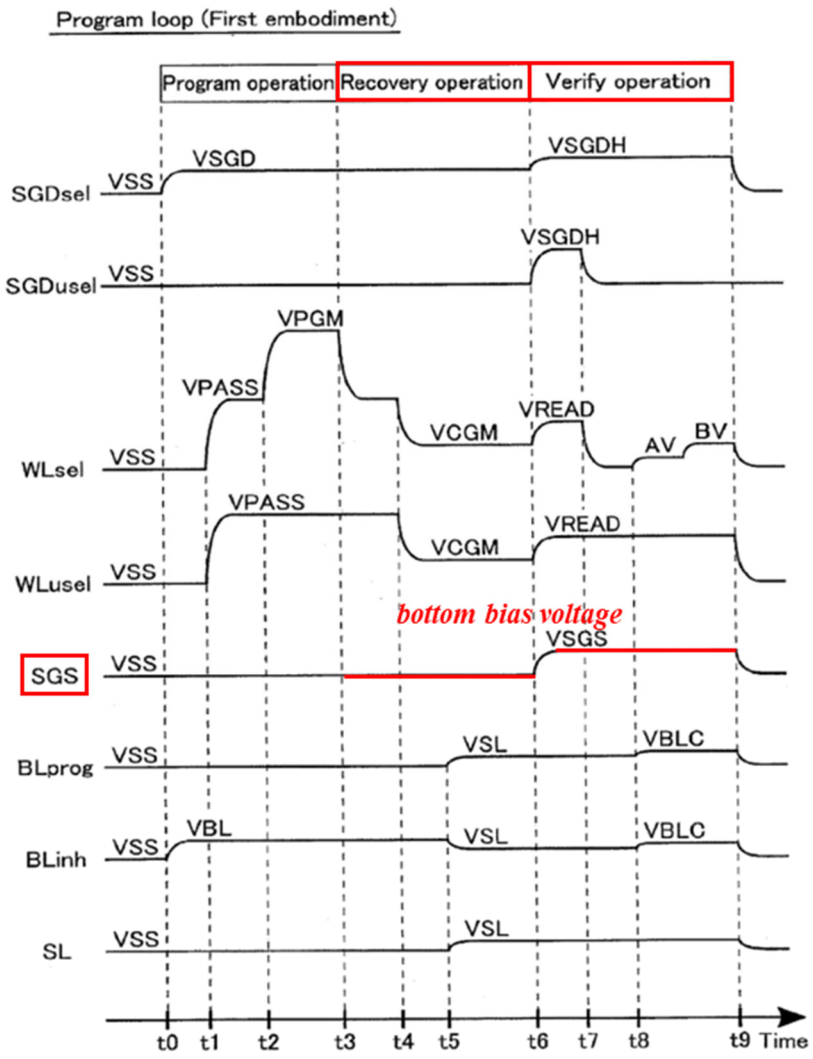
Suzuki discloses *processing circuitry further configured to* perform the limitations of claim 5. *Supra* §X.A.2; Liu, ¶ 226.

2. [5.A]

As explained in Ground 1, "a bottom bias voltage" need not have only one voltage level. *Supra* §IX.E.2.

Suzuki discloses *apply[ing] a bottom bias voltage* (VSS and VSGS) *on ... the BSG transistor of the first memory cell string in the pre-verify stage* (the recovery operation) *and the verify stage* (the verify operation):

[11] An alternative second gate voltage for claim [4.B.i] and [4.C] is VSGDH, which is applied on SGDusel in the verify operation and may be 6V, which also is lower than VREAD's 8V. Suzuki, Fig. 11, [0142].

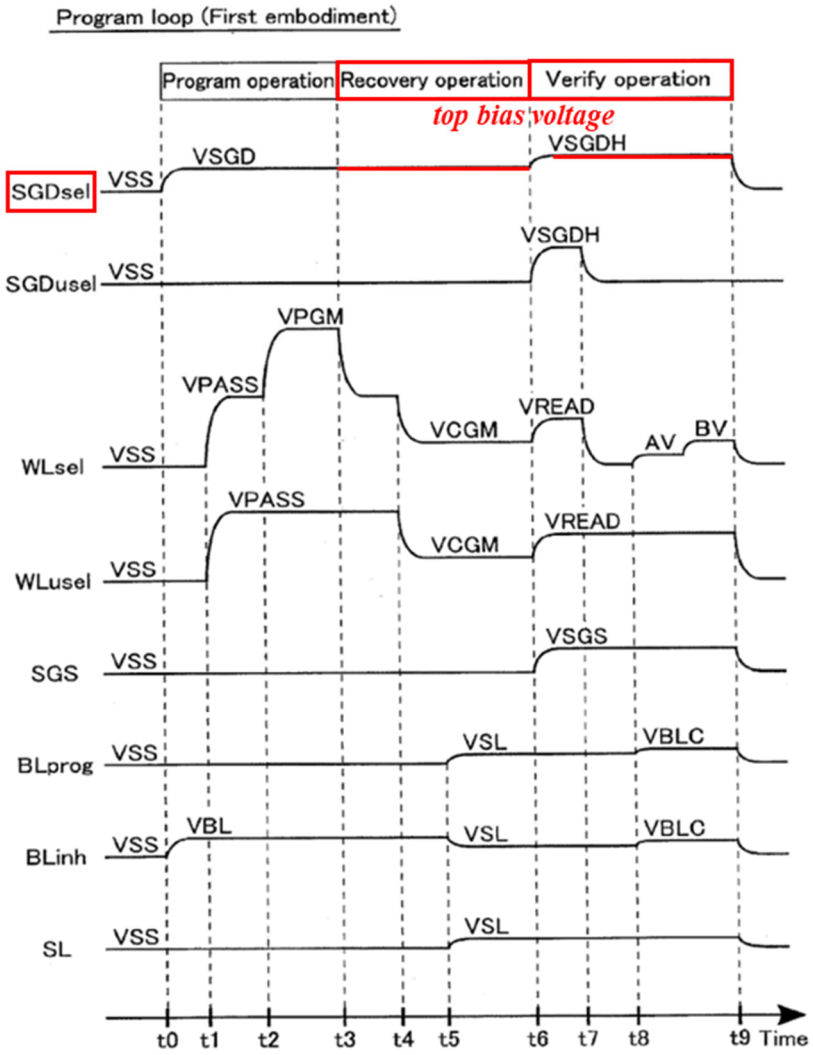


Suzuki, Fig. 11, [0142]. VSGS is high enough to turn on the BSG transistor ST2. *Id.*; Liu; ¶¶ 227-228.

3. [5.B]

As explained in Ground 1, "a top bias voltage" also need not have only one voltage level. *Supra* §IX.E.3.

Suzuki discloses *apply[ing] a top bias voltage* (VSGD and VSGDH) *on … the TSG transistor of the first memory cell string* (the selected string) *in the pre-verify stage* (the recovery operation) *and the verify stage* (the verify operation):

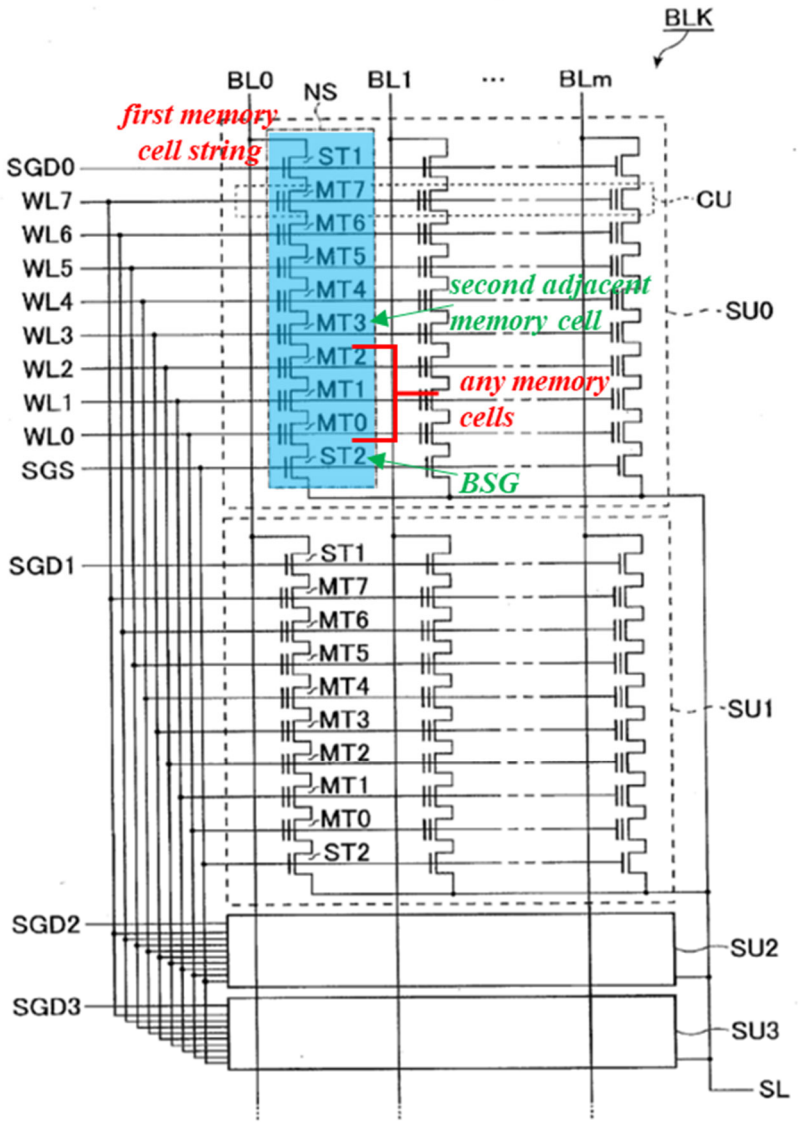


Suzuki, Fig. 11, [0133], [0142]. VSGD and VSGDH are high enough to turn on the top select (TSG) transistor. *Id.*, [0133], [0142]; Liu; ¶¶ 229-230.

4. [5.C]

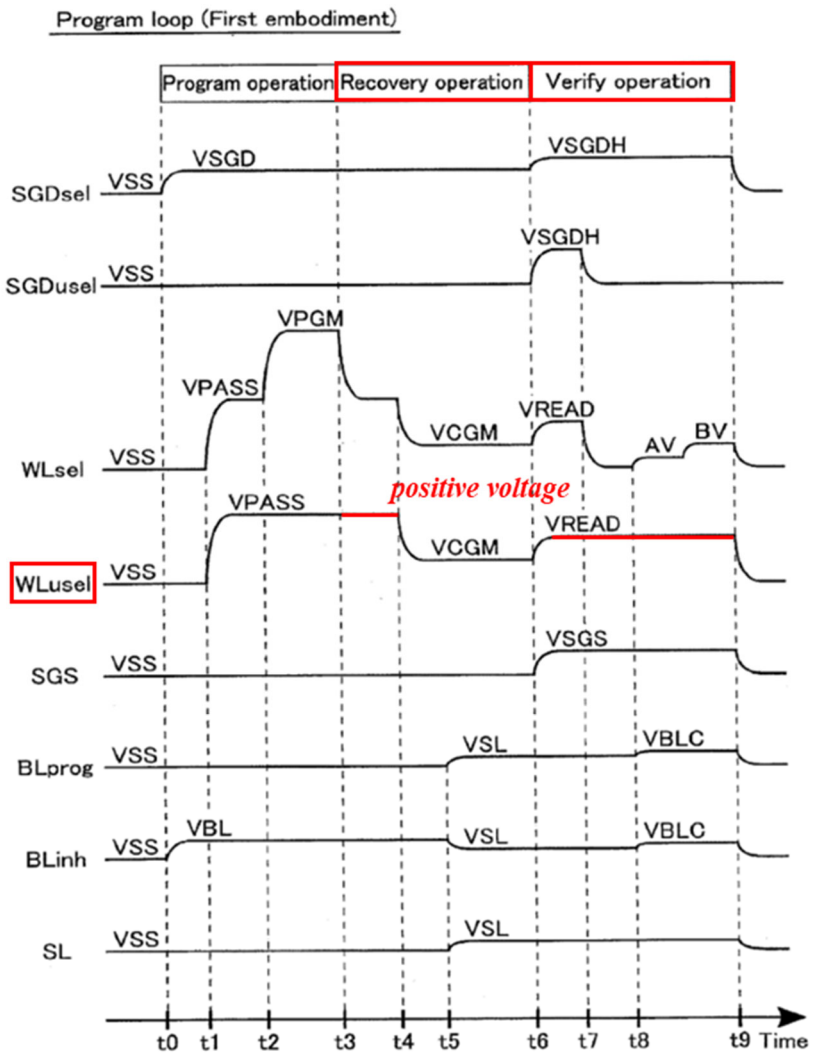
As explained in Ground 1, "a positive voltage" also need not have only one voltage level. *See* §IX.E.4. Relatedly, a *positive voltage* and a *bias voltage* need not be distinct voltages. *Id.*

The second adjacent memory cell, e.g., MT3, is the cell immediately below the selected cell, e.g., MT4. *Supra* §X.A.3. Thus, any unselected memory cell below MT3 and above the bottom select transistor ST2, e.g., MT2 through MT0, can be used to satisfy this limitation:



Suzuki, Fig. 2.

Accordingly, Suzuki discloses *apply[ing] a positive voltage* (VPASS and VREAD) *on … any memory cells that are positioned* (as depicted) *between the second adjacent memory cell of the selected memory cell and the BSG transistor of the first memory cell string* (the selected string) *in the pre-verify stage* (the recovery operation) *and the verify stage* (the verify operation):



Suzuki, Fig. 11; Liu; ¶¶ 231-233.

F. Claim 6:

1. [6.PRE]

Suzuki discloses *processing circuitry further configured to* perform the limitations of claim 6. *Supra* §X.A.2; Liu, ¶ 234.

2. [6.A]

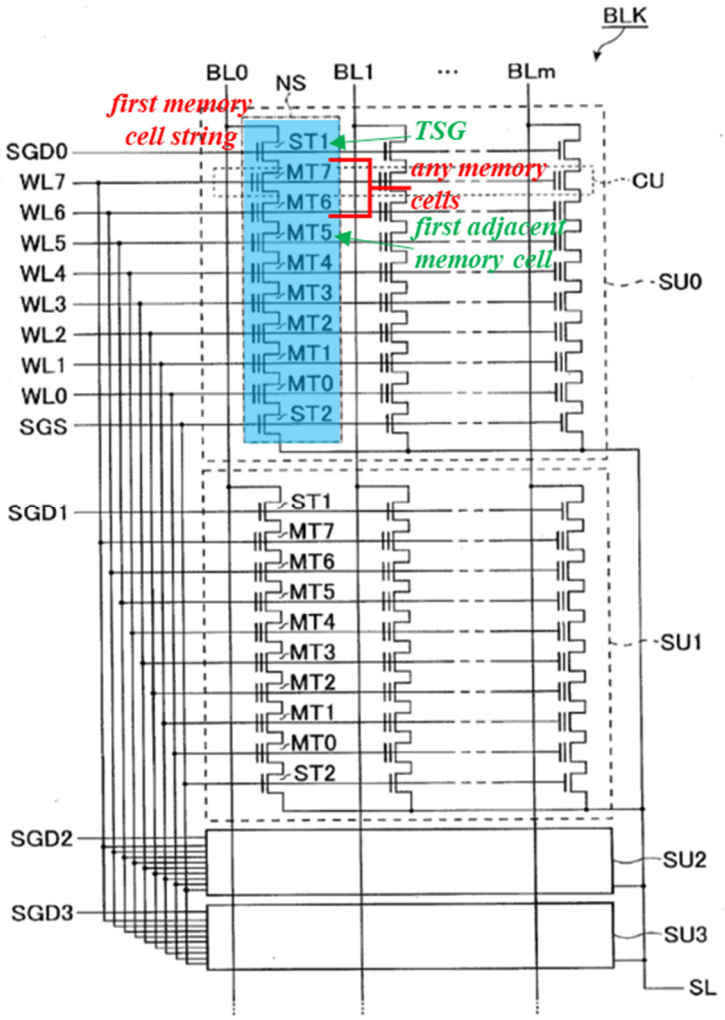
This limitation is identical to claim [5.A]. Suzuki discloses it for the same reasons. *Supra* §X.E.2; Liu, ¶ 235.

3. [6.B]

This limitation is identical to claim [5.B]. Suzuki discloses it for the same reasons. *Supra* §X.E.3; Liu, ¶ 236.

4. [6.C]

As explained in Ground 1, just as claim 3 is the mirror image of claim 2, this limitation is the mirror image of claim [5.C]. *Supra* §IX.F.4. The *any memory cells* may be *positioned* as shown.



Suzuki, Fig. 2.

Because Suzuki's positive voltage is applied on all unselected word lines, including those above and below the selected cell, Suzuki discloses *apply[ing] a positive voltage … in the pre-verify stage and the verify stage* for the same reasons explained with respect to claim [5.C]. *Supra* §X.E.4: Liu, ¶¶ 237-238.

XI. GROUND 3: CLAIMS 1-6 ARE OBVIOUS OVER COSTA IN VIEW OF SEO

For claim 1, Costa discloses the claimed voltages during the verify stage. As §XI.G explains, Costa teaches a verify stage technique to address channel resistance issues. For claim 1, Seo discloses the claimed voltages during the pre-verify stage. As §XI.G further explains, a POSITA would have been motivated to apply Seo's pre-verify stage teachings before Costa's verify stage to reduce HCI effects (as Seo teaches). Together, this renders claim 1 obvious. For certain dependent claims, while Costa is silent as to the unselected strings, Seo fills that gap. Together, all claims are unpatentable as obvious over Costa in view of Seo. Liu, ¶¶ 239-240.

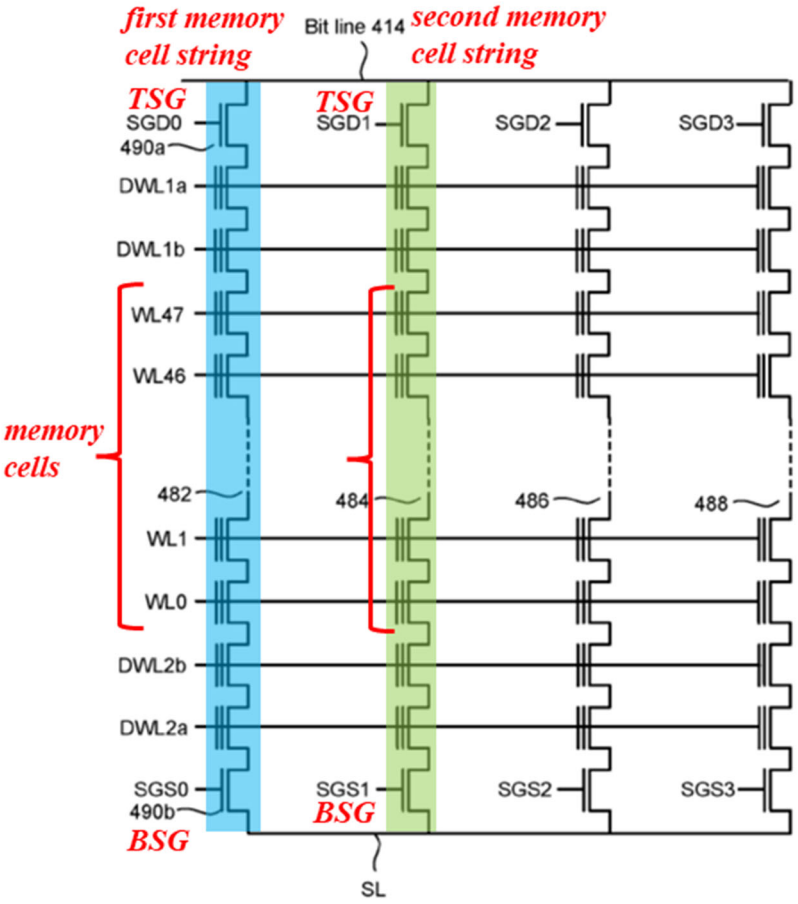
A. Claim 1:

1. [1.PRE]

To the extent the preamble is limiting, Costa discloses it.

Costa discloses "[s]ensing in non-volatile memory." Costa, Abstract. "Sensing may be performed during reading [or] program verification…." *Id.*, [0093]; *see also id.*, Fig. 14, [0160]-[0168].

Costa's non-volatile memory, *an apparatus for reading a memory device*, includes a plurality of memory strings including *a first memory cell string and a second memory cell string* (both highlighted):

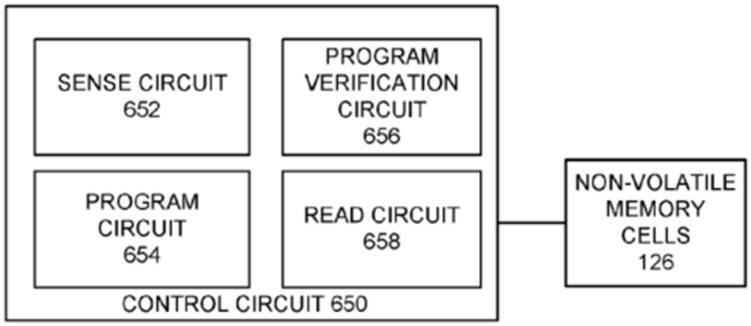


Id., Fig. 4F. As shown above, each of the memory strings includes *a bottom-select-gate (BSG) transistor* (source select gate), *memory cells* (at word lines WLs), *and a top-select-gate (TSG) transistor* (drain select gate) *that are connected in series*; *see also id.*, [0029] (memory cell strings), [0069] (bottom), [0073] (top), [0075] (memory cells connected in series), [0077] (select gates), [0161] (verification); Liu, ¶¶ 241-243.

2. [1.A]

Costa discloses *processing circuitry*, which can be configured to perform the claims of the '957 patent.

Costa's sense circuit or program verification circuit constitutes such processing circuitry.

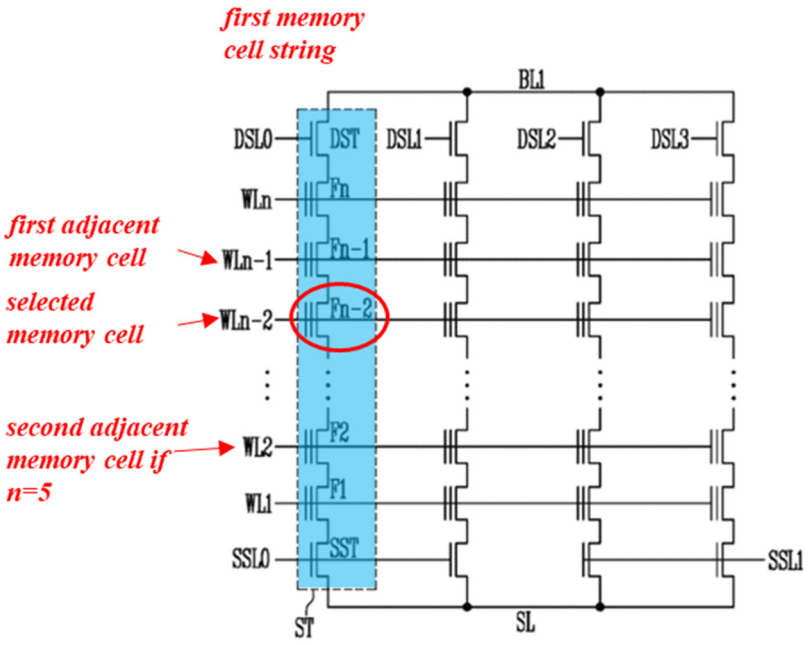


Costa, Fig. 15, [0169]-[0172] (generating voltages for access operations), [0175] (same); Liu, ¶ 244.

3. [1.A.i]

Costa in view of Seo renders this limitation obvious.

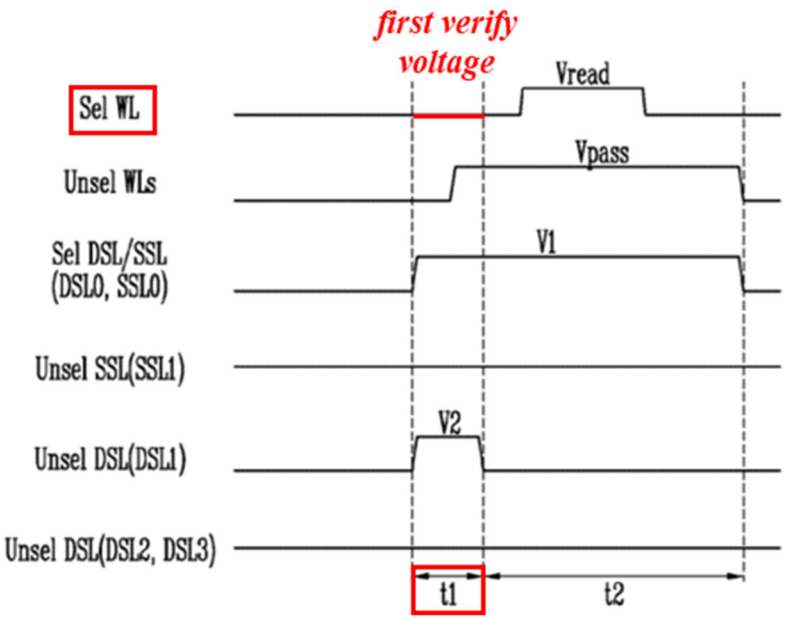
Seo's method involves selecting a memory cell for reading. Seo, Fig. 7, [0073]. For example, a memory cell coupled to DSL0 and WLn-2 may be selected. *Id.*, [0074]:



Id., Fig. 4. As shown, the *selected memory cell* (at WLn-2) belongs to *the first memory cell string* and *[is] arranged between a first adjacent memory cell* (at WLn-1) *and a second adjacent memory cell* (at WLn-3, or WL2 if n=5).

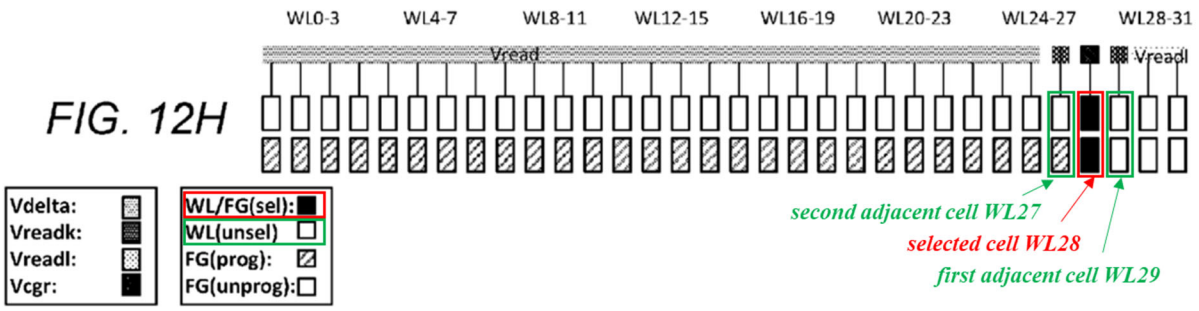
Costa discloses using its read operations to verify programming. *See* §V.A.2; Costa, [0093]-[0094]. Moreover, the same selected cell is programmed and then verified. *Supra* §V.A.2; Costa, Fig. 6; *see also id.*, [0086]-[0087]. Accordingly, when the *selected memory cell* is being verified, it is *programmed*. Liu, ¶¶ 245-248.

Seo discloses *apply[ing], in a pre-verify stage* (a first time period t1 preceding a read/verify period t2)*, a first verify voltage* (a low voltage) *on … a selected memory cell*:



Id., Fig. 8; *see also id.*, [0090]. In the context of the '957 patent, even applying zero volts is applying a voltage, which is *bias voltage* or *verify voltage*. Ex. 1001, 10:57-61, 11:19-23, 11:35-39. And Figure 7 is an embodiment in which 0 volts is the first verify voltage. Also, that the '957 patent uses a "verify voltage" in the pre-verify stage is a misnomer, because verification (reading) does not occur in that stage. Liu, ¶ 106.

On an illustrated embodiment of Costa's memory device, this *first verify voltage* would be applied to the *selected memory cell* coupled to WL28, with *a first and a second adjacent memory cell* at WL29 and WL27, respectively:



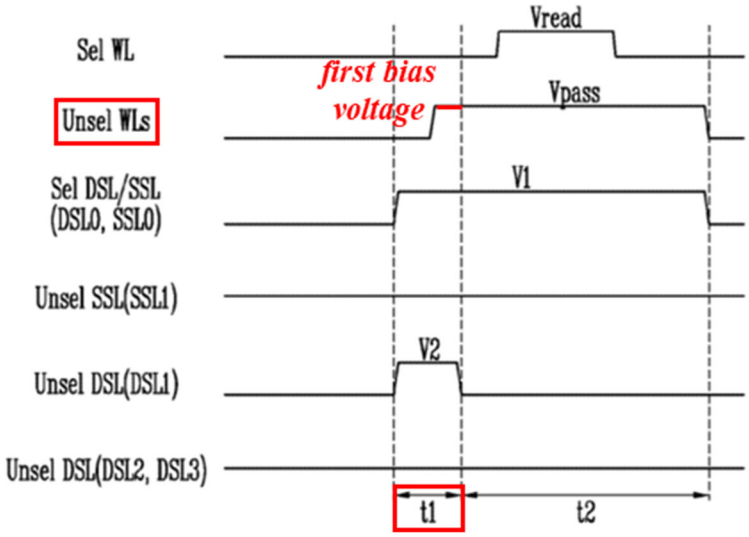
Costa, Fig. 12H, [0138]-[0139]; *id.*, [0140]-[0143] (identifying drain side toward WL31 and source side toward WL0); Liu, ¶¶ 249-250.[12]

4. [1.A.ii]

Costa in view of Seo renders this limitation obvious.

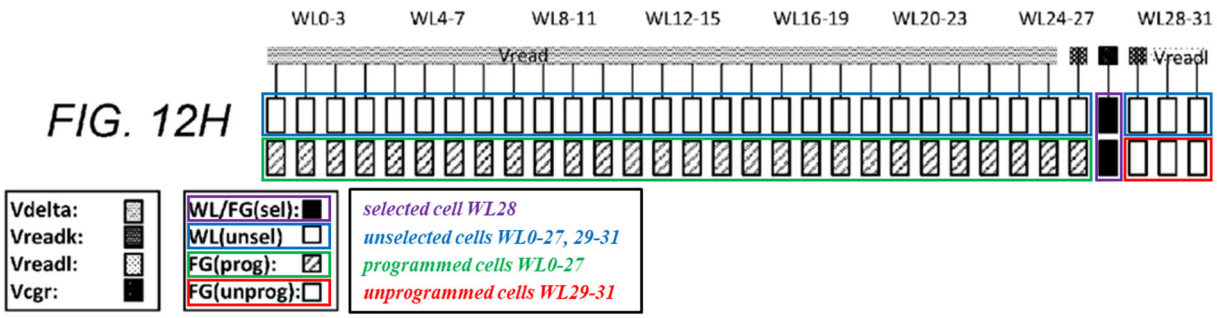
Seo discloses applying a "pass voltage Vpass … to unselected word lines" during a first time period t1. Seo, [0088]-[0089].

[12] Costa Figure 10 and associated descriptions disclose the same concept in a tabular form. Figure 12H corresponds to the Zone 7 column of Figure 10 because WL28 is located in Zone 7. Costa, [0147]; Liu, ¶ 251.



Id., Fig. 8. Thus, Seo discloses *apply[ing], in the pre-verify stage* (the first time period t1)*, a first bias voltage* (Vpass) *on … at least one memory cell* (via the Unsel WLs) *of the first memory cell string*.

Costa discloses that this *at least one memory cell … is not programmed*. Costa teaches that programming of memory cell strings "generally occurs in a programming order that begins at one end of each NAND string and proceeds to the other end." Costa, [0100]. Accordingly, unprogrammed cells are typically positioned between the selected word line and a select line, e.g., SGD0. *Id.*, [0033]; Liu, ¶ 255. For example, in the following illustration, the unprogrammed cells are at WL29-31, above (toward SGD on the drain side of) the selected cell at WL28:



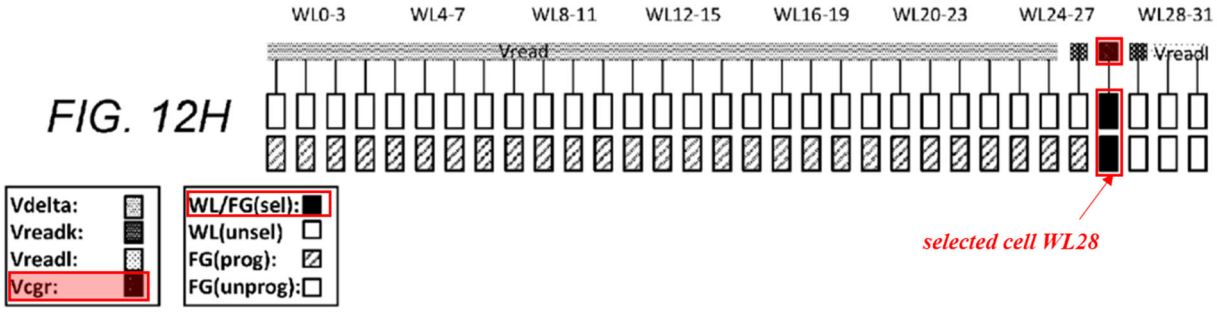
Costa, Fig. 12H; *see also id.*, [0139], [0147], [0109].

Applying Seo's first bias voltage Vpass on unselected word lines of Costa's memory device, Vpass is applied on unprogrammed memory cells such as those at WL29-31 in this illustrated scenario. Liu, ¶¶ 252-256.

5. [1.A.iii]

Costa discloses this limitation.

This limitation refers to the same memory cell in claim [1.A.i], e.g., at WL28, during the subsequent verify stage. *See* §XI.A.3.



Costa, Fig. 12H. "WL28 … is selected for verification and receives Vcgr." *Id.*, [0147]. "The waveform of Vcgr … may be considered a read pulse or a read reference voltage which is used during a sense operation." *Id.*, [0098]; *see also id.*, [0094] (describing Vcgr). "For example, Vcgr may be set to … Vv1, Vv2, Vv3, etc.

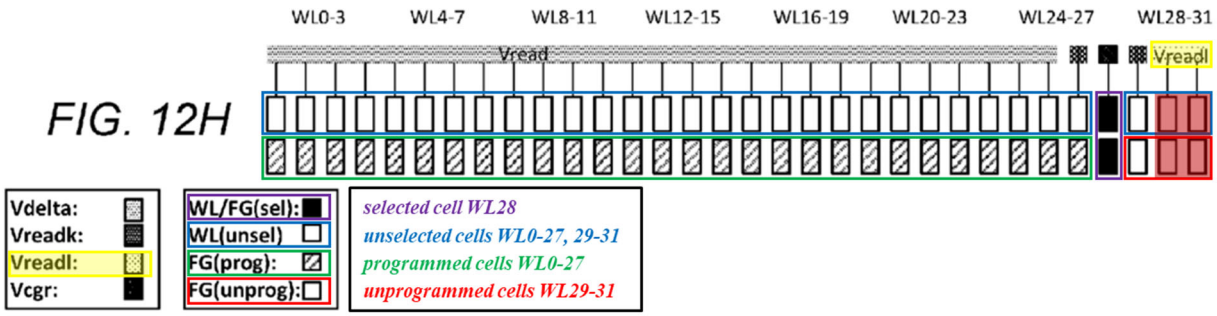
to sense at various verify levels for target states during programming." *Id.*, [0098]. This occurs during the sensing phase of operation. *Id.*, [0166].

Accordingly, Costa discloses *apply[ing], in a verify stage* (sensing phase)*, a second verify voltage* (Vcgr) *on … the selected memory cell* (at WL28) *of the first memory cell string*. Liu, ¶¶ 257-259.

6. [1.A.iv]

Costa in view of Seo renders this limitation obvious.

This limitation refers to the same memory cell in claim [1.A.ii] during the subsequent verify stage. *Supra* §XI.A.4. Specifically, that memory cell can be WL30 or WL31. Costa further discloses applying *a second bias voltage* (VreadL) on the same unselected word lines *in the verify stage* (sensing phase):



Costa, Fig. 12H, [0147]. "VreadL is a lowest read pass voltage used in one example. For example, VreadL may be several millivolts less (e.g., 5.2V) than the standard read pass voltage Vread." *Id.*, [0122]. "VreadL may be used [on WL30 and WL31] because the word lines on the drain side have not undergone programming, and thus

the corresponding memory cells should be in the erased state" and have a low threshold voltage. *Id.*, Liu, ¶¶ 260-261.

A POSITA would have found it obvious that Seo's *first bias voltage* is no lower than the standard read pass voltage because the same voltage level is applied to all unselected memory cells, including those already programmed, to ensure that they all conduct regardless of the program state. Seo, Fig. 8; Liu, ¶ 262. And as §XI.G explains, in the ***pre-verify stage***, Seo does this to reduce HCI effects, in which case a sufficiently high Vpass voltage on all unselected gates minimizes the voltage gradient through the channels of memory strings and overcomes the bit line voltage due to Seo's selected word line being grounded during pre-verify. And as §XI.G further explains, ***during verify***, Costa seeks to reduce channel resistance issues without introducing read disturb due to an unnecessarily high read pass voltage on the unprogrammed cells, in which case low Vpass voltages are optimal for unselected gates (e.g., gates of unprogrammed cells). Thus, a POSITA would not have lowered Seo's standard read pass voltage during pre-verify. Therefore, *the second bias voltage* (VreadL) *is smaller than the first bias voltage* (pass voltage Vpass). Liu, ¶ 262.

B. Claim 2:

1. [2]

Costa in view of Seo renders this limitation obvious.

Claim 2 refers to the at least one unprogrammed memory cell of claim ([1.A.ii] and [1.A.iv]) that receives the bias voltages. That memory cell can be a cell (at WL30 or WL31) *positioned between the first adjacent memory cell* (at WL29) *... and the TSG transistor of the first memory cell string*. *Supra* §§XI.A.3, X.A.4, X.A.6; Liu, ¶¶ 263-264.

C. Claim 3:

1. [3]

Costa in view of Seo renders this limitation obvious.

As explained in Ground 1, claim 3 requires an unprogrammed memory cell positioned *below* the second adjacent memory cell. *Supra* §IX.C. Costa discloses that programming may proceed from the source end to the drain end, or vice versa. Costa, [0100], [0165]. Claims 1 and 2 above have been described using an illustration wherein the drain side (e.g., WL29 through WL31) are the last cells to be programmed. When the programming order proceeds from the drain end to the source end, an unprogrammed memory cell *positioned between the second adjacent memory cell and the BSG transistor* exists. In this scenario, the first bias voltage (Seo's Vpass) is applied to this cell because it is applied to all unselected cells. *Supra* §XI.A.4. The second bias voltage (Costa's VreadL) is also applied on this cell

because it is an unprogrammed, nonadjacent cell. Costa, [0122] (applying VreadL on unprogrammed cells); Liu, ¶¶ 265-266.

D. Claim 4:

1. [4.PRE]

Costa discloses *processing circuitry further configured to* perform the limitations of claim 4 as explained with respect to claim [1.A]. *Supra* §XI.A.2; Liu, ¶ 267.

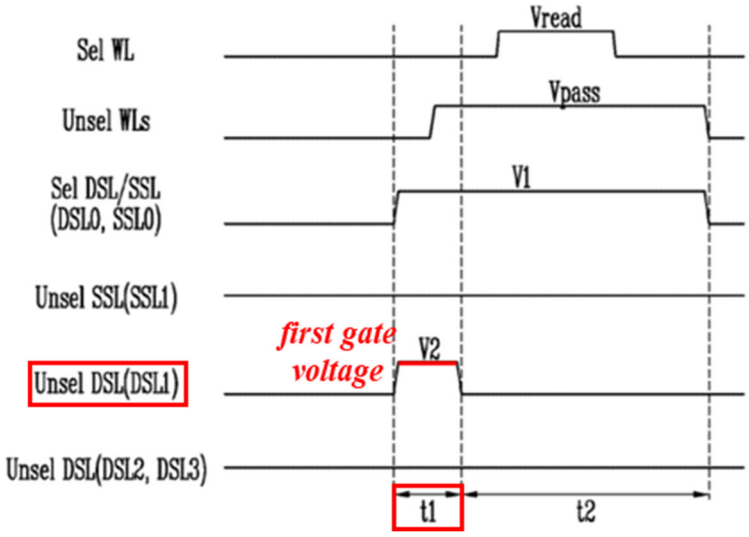
2. [4.A]

The pre-verify stage corresponds to Seo's first time period t1. *Supra* §§XI.A.3-XI.A.4; Liu, ¶ 268.

3. [4.A.i]

Costa in view of Seo renders this limitation obvious.

The second memory cell string is an unselected memory string since the selected memory cell belongs to the first memory cell string. Ex. 1001, 17:41-43 (claim [1.A.i]). Seo discloses *apply[ing] a first gate voltage* (V2) *on … the TSG transistor of the second memory cell string* (Unsel DSL):



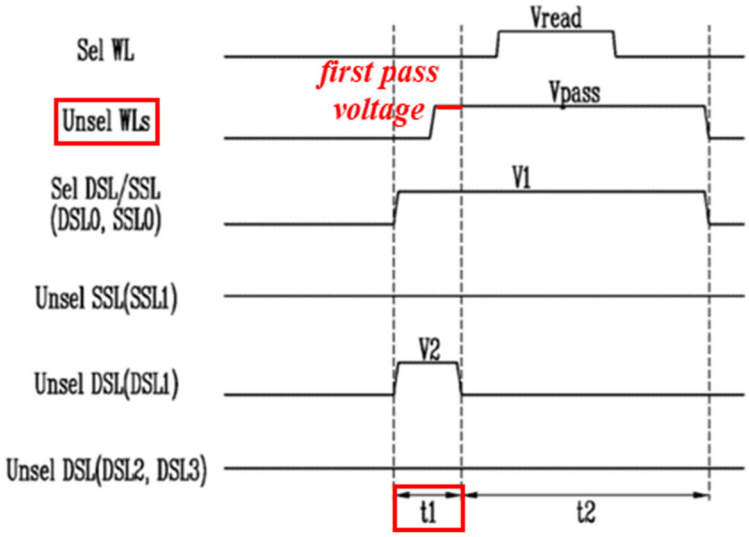
Seo, Fig. 8; *id.*, [0088]. Voltage V2 turns on the drain select transistor. *Id.* This voltage can be applied to Costa's unselected drain select line SGD1. Liu, ¶¶ 269-270.

4. [4.A.ii]

Costa in view of Seo renders this limitation obvious.

As explained in Ground 1, the '957 patent does not require the first bias voltage of claim 1 and the first pass voltage of claim 4 to have different values, or even that they be distinct voltages. *Supra* §IX.D.4.

The first bias voltage may be applied to at least one unprogrammed memory cell, e.g., at WL30 or WL31. *Supra* §XI.A.4. The *first pass voltage* (Vpass) may be applied to *the first adjacent memory cell* (e.g., WL29) *in the pre-verify stage* (the first time period t1):



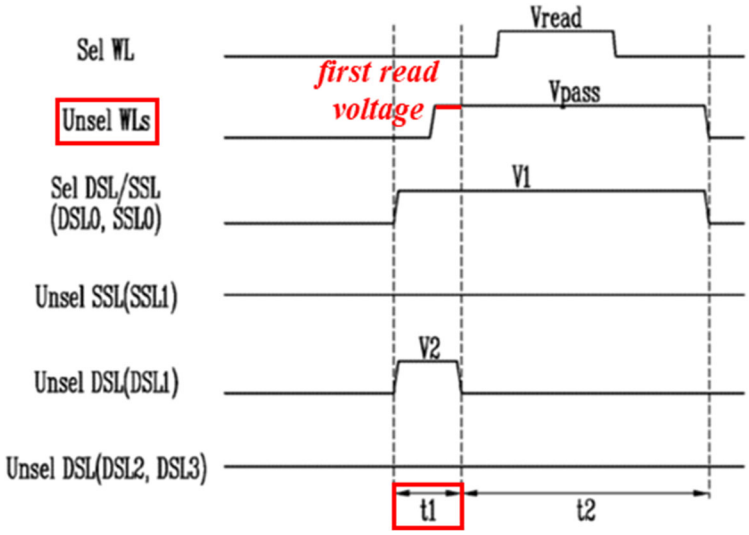
Seo, Fig. 8; Liu, ¶¶ 271-273.

5. [4.A.iii]

Costa in view of Seo renders this limitation obvious.

As explained in Ground 1, the '957 patent does not require the first bias voltage of claim 1 and the first read voltage of claim 4 to have different values, or even that they be distinct voltages. *Supra* §IX.D.5.

Seo discloses applying the same Vpass voltage to unselected word lines in its *pre-verify stage* (the first time period t1). *Supra* §XI.D.4. Applied to Costa's Figure 12H embodiment, this Vpass voltage also constitutes the *first read voltage on … the second adjacent memory cell* (at WL27) *… in the first memory cell string*.



Seo, Fig. 8; Liu, ¶¶ 274-276.

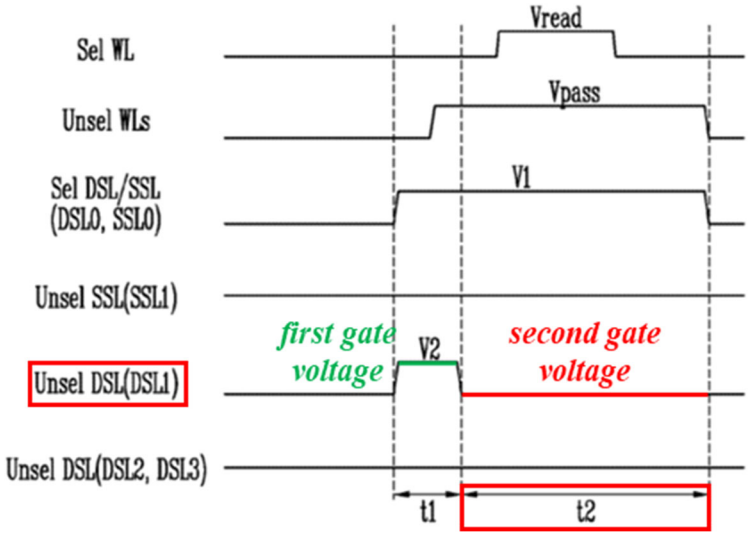
6. [4.B]

The verify stage corresponds to Seo's second time period t2 and Costa's verify operation. *Supra* §§XI.A.5-X.A.6; Liu, ¶ 277.

7. [4.B.i]

Costa in view of Seo renders this limitation obvious.

This limitation refers to the same transistor in claim [4.A.i]. *Supra* §XI.D.3. The *second gate voltage appl[ied] on … the TSG transistor of the second memory cell string* is shown below:



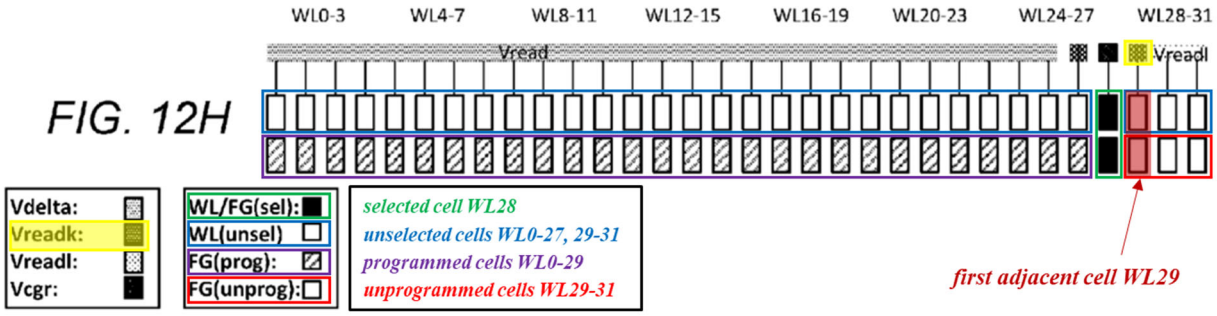
Seo, Fig. 8. Contrary to the first gate voltage V2, which turns on the drain select transistor DST, this voltage turns off the DST. *See id.*, [0088]-[0090]; Liu, ¶ 279.

Seo represents the knowledge of a POSITA, namely, disconnecting the unselected string from the bit line (by turning off the drain select transistor) is, in practice, a necessary condition because unselected memory strings must be isolated from the bit line so that the current level from the selected memory string (and the data state of the selected cell) may be determined accurately via the verify operation. A POSITA knew that to accurately verify, this condition was necessary and certainly obvious, and it was routine to implement, because this was the conventional approach in 3D NAND. Liu, ¶¶ 278-79, 305; §§IX.D.7, X.D.7 (demonstrating knowledge of a POSITA to ground unselected drain select gate during sensing).

8. [4.B.ii]

Costa discloses this limitation.

This limitation refers to the same transistor in claim [4.A.ii]. In the combination, that transistor can be, for example, at WL29 in Costa's illustration. *Supra* §XI.D.4. Costa discloses *apply[ing] a second pass voltage* (Vreadk) *on … the first adjacent memory cell* (WL29) *… in the first memory cell string*:

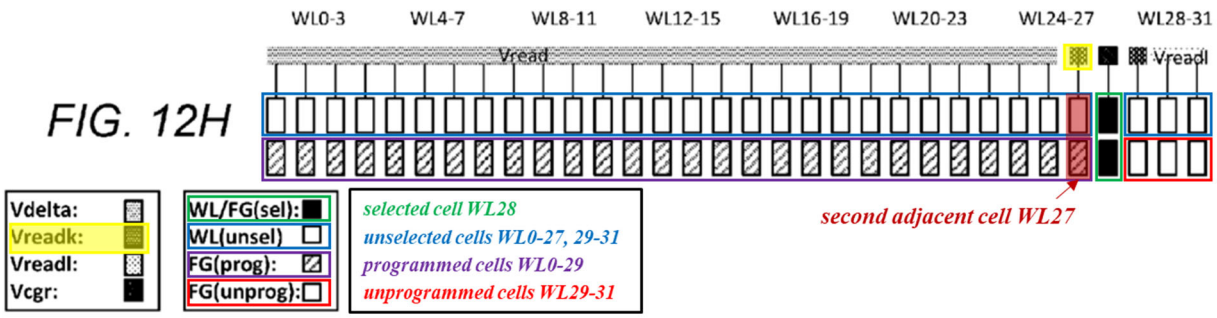


Costa, Fig. 12H, [0147], [0165]. "Vreadk is a highest read pass voltage." *Id.*, [0121]; Liu, ¶¶ 280-281.

9. [4.B.iii]

Costa discloses this limitation.

This limitation refers to the same transistor as in claim [4.A.iii]. In the combination, that transistor can be, for example, at WL27 in Costa's illustration. *Supra* §XI.D.5. Costa discloses *apply[ing] a second read voltage* (Vreadk) *on … the second adjacent memory cell* (WL27) *… of the first memory cell string*:



Costa, Fig. 12H, [0147], [0165], [0121]; Liu, ¶¶ 282-283.

10. [4.C]

Costa discloses this limitation.

Both the *second pass voltage* and the *second read voltage* are Costa's Vreadk. *Supra* §XI.D.8-9. "Vreadk is a highest read pass voltage … [and] may be [hundreds of] millivolts higher … than a standard read pass voltage Vread." Costa, [0121]. Read pass voltages are sufficiently high such that the memory cells to which they apply are turned on and conduct current. *Id.*, [0096]. The *second gate voltage* is Seo's voltage to turn off the DST. *Supra* §XI.D.7. This voltage may be the ground voltage Vss. Seo, [0075]. A read pass voltage that turns on memory cells regardless of their data state is higher than a voltage, e.g., Vss, that is low enough to turn off the DST. Thus, *the second pass voltage and the second read voltage* (Vreadk) *[are] larger than the second gate voltage* (e.g., Vss). Liu, ¶¶ 284-285.

E. Claim 5:

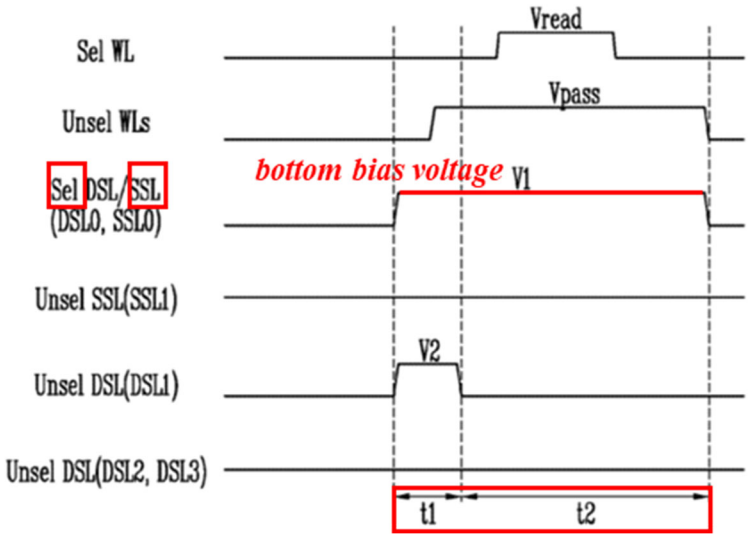
1. [5.PRE]

Costa discloses *processing circuitry further configured to* perform the limitations of claim 5 for the same reason discussed with respect to claim 4. *See* §XI.D.1; Liu, ¶ 286.

2. [5.A]

Costa in view of Seo renders this limitation obvious.

Seo discloses *apply[ing] a bottom bias voltage* (V1) *on … the BSG transistor of the first memory cell string* (Sel SSL, e.g., SSL0) *in the pre-verify stage* (the first time period t1) *and the verify stage* (the second time period t2):



Seo, Fig. 8, [0088]. "[V]oltage V1 may be a voltage to turn on … the source select transistor SST." *Id.*, [0088].

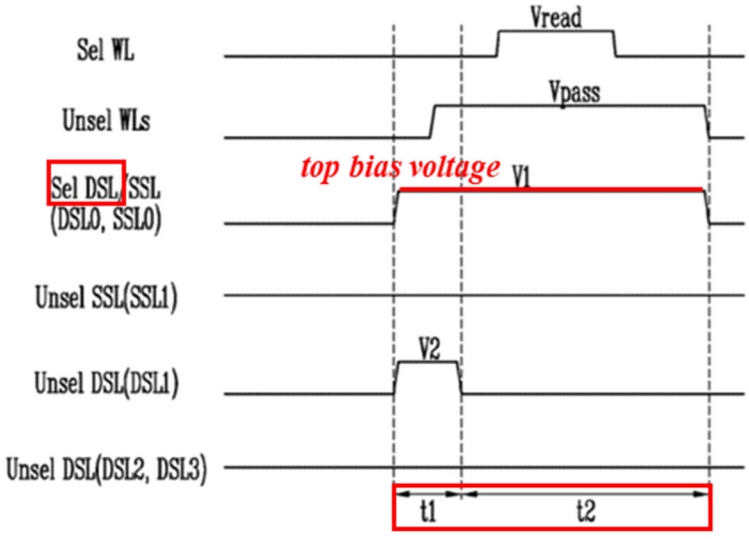
Costa discloses that, during *the verify stage* (the sensing phase), "[t]he source select line … [is] set to VSG [*the bottom bias voltage*] to turn on source select gate [*the BSG transistor*] …." Costa, [0097].

Because both Seo's voltage V1 and Costa's VSG are used to turn on the source select transistor, Costa's VSG may be used in both stages in the combination. Liu, ¶¶ 287-290.

3. [5.B]

Costa in view of Seo renders this limitation obvious.

Seo discloses *apply[ing] a top bias voltage* (V1) *on … the TSG transistor of the first memory cell string* (Sel DSL, e.g., DSL0) *in the pre-verify stage* (the first time period t1) *and the verify stage* (the second time period t2):



Seo, Fig. 8, [0088]. "[V]oltage V1 may be a voltage to turn on the drain select transistor DST…." *Id.*, [0088].

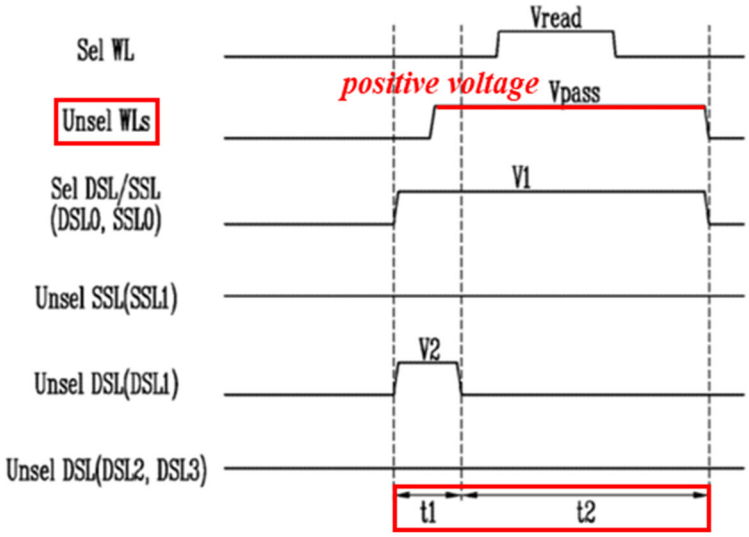
Costa discloses that, during *the verify stage* (the sensing phase), the "drain select line … [is] set to VSG [*the top bias voltage*] to turn on … drain select gate [*the TSG transistor*] …." Costa, [0097].

Because both Seo's voltage V1 and Costa's VSG are used to turn on the drain select transistor, Costa's VSG may be used in both stages in the combination. Liu, ¶¶ 291-294.

4. [5.C]

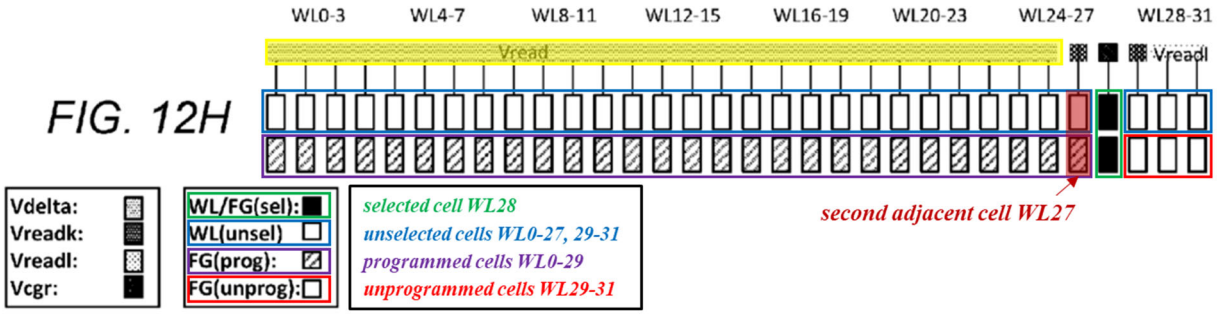
Costa in view of Seo renders this limitation obvious.

Seo discloses *apply[ing] a positive voltage* (Vpass) *on … any* unselected *memory cells*—including those *that are positioned between the second adjacent memory cell of the selected memory cell and the BSG transistor—of the first memory cell string in the pre-verify stage* (the first time period t1) *and the verify stage* (the second time period t2):



Seo, Fig. 8, [0088]. Vpass is a voltage that turns on the unselected memory cells regardless of the data states or threshold voltages of the cells. *Supra* §V.A.2; Liu, ¶¶ 295-296.

Costa also discloses *apply[ing] a positive voltage* (standard read pass voltage Vread, (Costa, [0121]-[0128])) *on … any memory cells* (WL0-WL26) *that are positioned between the second adjacent memory cell* (WL27) *… and the BSG transistor of the first memory cell string in … the verify stage* (the sensing phase):



Costa, Fig. 12H, [0147]; Liu, ¶ 297.

Because both Seo and Costa apply a nominal read pass voltage on the memory cells recited by this limitation, Costa's nominal read pass voltage may be used in both stages in the combination. Liu, ¶ 298.

F. Claim 6:

1. [6.PRE]

Costa discloses *processing circuitry further configured to* perform the limitations of claim 6 for the same reason discussed with respect to claim 4. *See* §XI.D.1; Liu, ¶ 299.

2. [6.A]

This limitation is identical to claim [5.A]. Costa in view of Seo renders it obvious for the same reasons. *Supra* §XI.E.2; Liu, ¶ 300.

3. [6.B]

This limitation is identical to claim [5.B]. Costa in view of Seo renders it obvious for the same reasons. *Supra* §XI.E.3; Liu, ¶ 301.

4. [6.C]

Costa discloses or at least renders obvious this limitation. Specifically, as explained below, when programming proceeds from the drain end to the source end, a standard read pass voltage Vread (*a positive voltage*) is applied to memory cells *between the first adjacent memory cell of the selected memory cell and the TSG transistor*.

As explained in Ground 1, just as claim 3 is the mirror image of claim 2, this limitation is the mirror image of the claim [5.C] limitation. *Supra* §IX.F.4. Specifically, claim 2 recites memory cells *above* (on the *drain* side of) the selected cell, while claim [5.C], which depends from claim 2, recites the remaining unselected memory cells, *i.e.*, those *below* (on the *source* side of) the selected cell. Claims 2 and [5.C] are satisfied through a source-to-drain programming order. *Supra* §§XI.B.1, X.E.4. Similarly, but in a mirror image, claim 3 recites memory cells *below* (on the *source* side of) the selected cell, while claim [6.C] recites the remaining unselected memory cells, *i.e.*, those *above* (on the *drain* side of) the selected cell. Thus, Costa discloses or at least renders obvious this limitation through a drain-to-source programming order but otherwise for the same reason as it discloses claim [5.C]. *See* Costa, [0101] (explaining that the increase in channel resistance changes direction with the programming order); *id.*, [0115], [0119] (illustrating embodiments using a source-to-drain programming order); Liu, ¶¶ 302-303.

G. Motivation to Combine

A POSITA would have been motivated to apply Seo's HCI-reduction technique to Costa's verify operation to precondition unselected-string channels during the pre-verify phase, and would have had a reasonable expectation of success, for several reasons. Liu, ¶¶ 304-305.

Costa and Seo focus on two different phenomena that impact the reliability of memory devices. Costa's techniques reduce the adverse impact on threshold voltages of cells in the selected string from increasing channel resistance as programming progresses through the string, without compromising the susceptibility to read disturb. Costa, Abstract, [0029], [0101]-[0104], [0122]. To do this while minimizing read disturb, Costa seeks to reduce the voltage on unselected gate lines as much as possible based on the extent to which a memory string has been programmed. *See, e.g.*, *id.*, Figs. 10-11. More specifically, because a potentially low Vcgr voltage is applied to the selected word line (e.g., at WL28), a low read pass voltage VreadL is applied to unprogrammed cells (e.g., at WL30 and WL31) beyond the adjacent cell (e.g., at WL29) to prevent a high voltage gradient across the adjacent cell and to minimize read disturb. *Id.*, [0147], [0120], Fig. 7E. On the other hand, Seo's pre-verify stage reduces HCI-induced read disturb on unselected memory strings. Seo, [0008], [0089], [0127]; Ex. 1014, 254. To do this, Seo applies the same pass voltage on all unselected word lines. *See* §XI.A.4. The same pass voltage is applied to all unselected word lines to minimize voltage gradient across the channel, which minimizes HCI. Importantly, Seo recognizes that this pre-verify stage is shorter than the verify stage. Seo, [0075]. This further enables a reduction in HCI while guarding against other issues caused by long periods of high voltages on the unselected gate lines. A POSITA would have recognized that both Costa's

and Seo's issues should be addressed to improve the reliability of flash devices. Thus, a POSITA would have considered Costa's techniques with other techniques, such as Seo's technique, for a more comprehensive improvement of memory reliability. Liu, ¶ 307.

A POSITA would have also understood that in Seo's bias scheme, Seo is passing the bit line voltage to the drain side of the selected transistor (hence, Seo turns off the selected word line during pre-verify). To do this, Seo uses, and must use, high Vpass voltages. For example, the voltage on the source of the transistor above the selected transistor will start to build to the bit line voltage, and thus its threshold voltage will increase (as the threshold voltage is relative to the source voltage). Thus, Seo applies the same Vpass voltage to the drain and the source side unselected memory cells to compensate for this effect. Liu, ¶ 308. A high Vpass voltage is also needed for a drain-to-source programming sequence to reduce HCI disturb because, like Costa, Seo's device memory strings on separate source select gates. *Id.* ¶ 309.

To the extent Seo is used to render a second gate voltage obvious, a POSITA would have been motivated to apply Seo's second gate voltage to Costa's device. *Id.* ¶ 310.

A POSITA would have had a reasonable expectation of success in combining Costa's and Seo's voltage regimes (including in the verify stage if necessary)

because they are mutually compatible extensions. For example, Seo's pre-verify voltages—used for HCI reduction—may be prepended to Costa's verify voltages. *Id.*, ¶ 311. Costa's position-dependent pass voltages on unselected cells simply extend a single Vpass voltage—that Seo already deploys—into multiple levels. *Id.* In fact, Seo's application of a single Vpass voltage on all unselected lines is discussed in Costa:

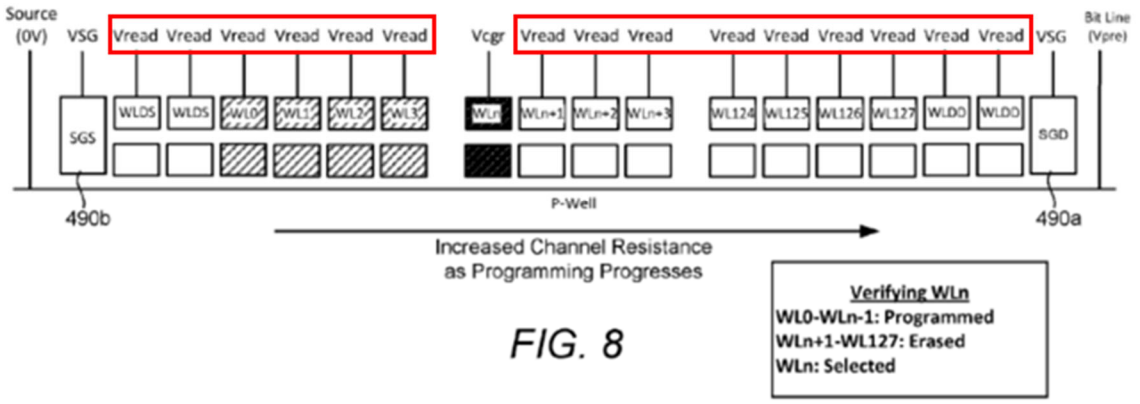
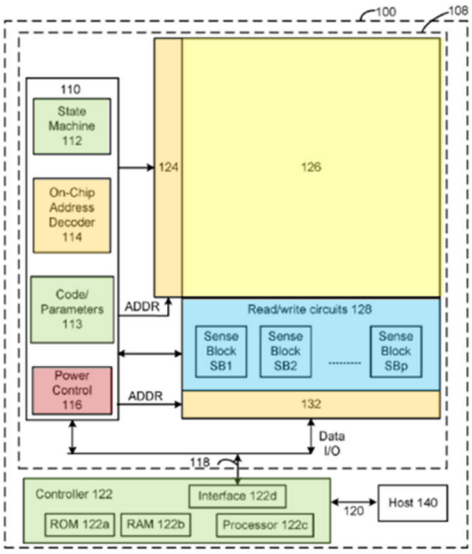
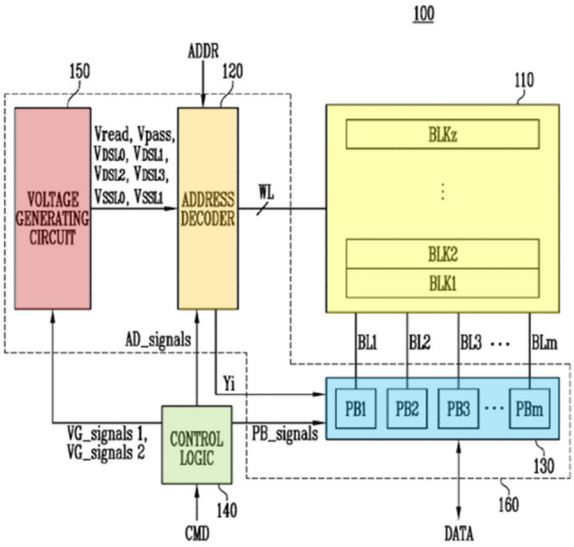


FIG. 8

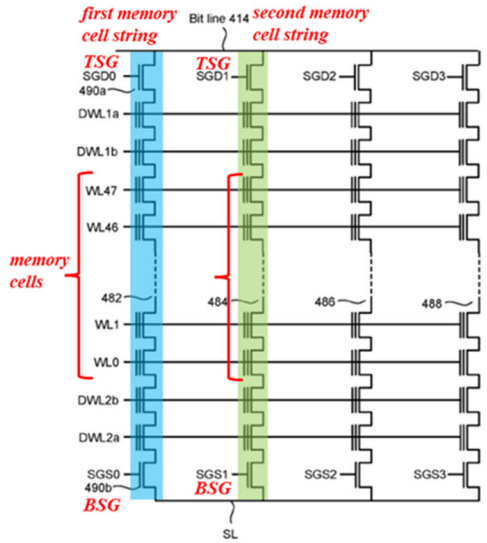
Costa, Fig. 8 (showing pass voltage Vread on all unselected cells). Thus, Costa's techniques improve upon Seo's basic configuration. *Id.*, [0096]-[0104]. Further, there are no conflicting applications of voltages between the two. *Supra* §§XI.A-XI.F; Liu, ¶ 312.

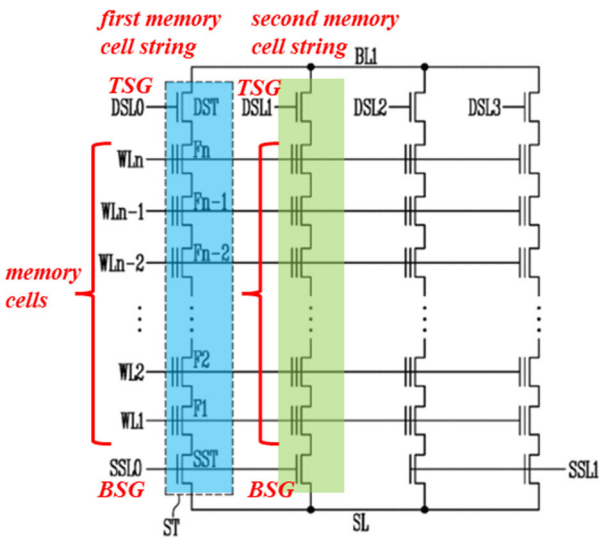
Moreover, a POSITA also would have had a reasonable expectation of success combining the teachings of Costa and Seo because they disclose similar control circuitry, memory arrays, and read-operation processes:



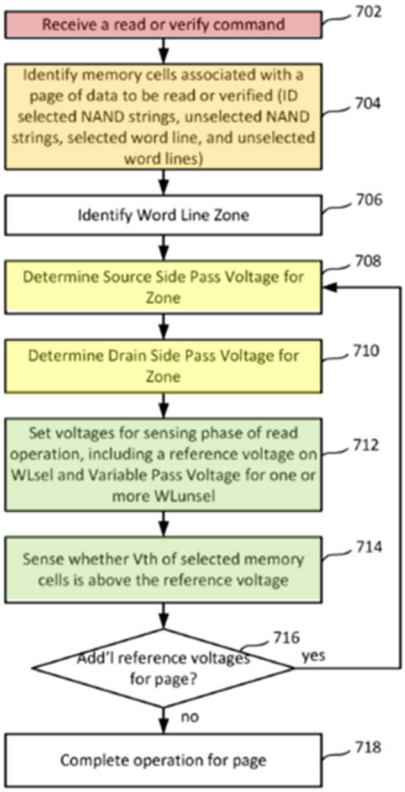


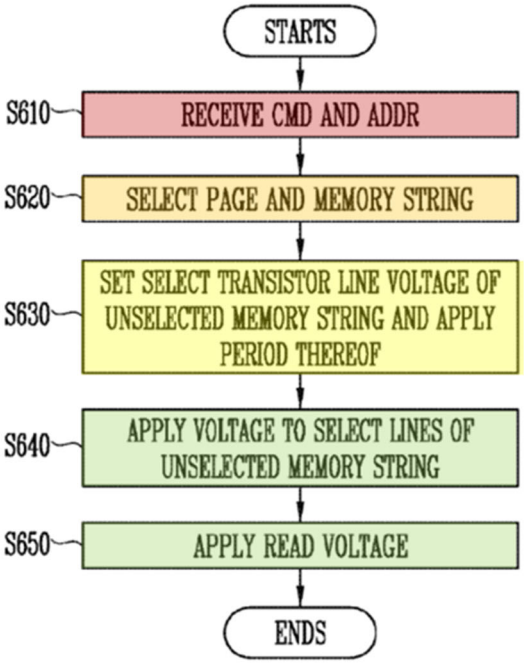
Costa, Fig. 2; *see also id.*, [0038]; Seo, Fig. 1. For example, both Costa and Seo disclose a voltage-generating circuit and associated circuitry that generate and output control voltages to the memory cell array. Costa, [0038]-[0043]; Seo, [0040], [0049], [0065]-[0067], [0077]-[0085].





Costa, Fig. 4F, [0029], [0075], [0077], [0161]; Seo, Fig. 4, [0053]-[0059], Abstract.





Costa, Fig. 14; Seo, Fig. 7. Thus, a POSITA would have had a reasonable expectation of success in applying Seo's voltage scheme to Costa's embodiment. Liu, ¶¶ 313-316.

The claims are not limited to charge-trap memories, but even if they were, Seo's pre-verify operation creates an electrical field that mitigates the fast-charge loss verification issue in such memories. *Id.*, ¶ 317.

XII. SECONDARY CONSIDERATIONS

Petitioner is unaware of any applicable secondary considerations of nonobviousness. None were identified during prosecution. *See generally* Ex. 1002. Regardless, none would overcome the strong *prima facie* showing of obviousness. Liu, ¶¶ 318-319.

XIII. CONCLUSION

For the foregoing reasons, Petitioner respectfully requests institution of IPR and cancellation of claims 1-6.

Respectfully submitted,

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Dated: April 29, 2024

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CERTIFICATE OF COMPLIANCE

The undersigned certifies that the foregoing PETITION FOR *INTER PARTES* REVIEW complies with the type volume limitation in 37 C.F.R. § 42.24(a). According to the utilized word-processing system's word count, the petition—excluding the caption, table of contents, table of exhibits, mandatory notices, certificate of word count, and certificate of service—contains 13,532 words.

Dated: April 29, 2024

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CERTIFICATE OF SERVICE

The undersigned hereby confirms that the foregoing Petition for *Inter Partes* Review and associated exhibits were caused to be served on April 29, 2024 via overnight courier upon the following counsel of record for Patent Owner:

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