

SCORE Placeholder Sheet for IFW Content

Application Number: 17191768

Document Date: 03/04/2021

The presence of this form in the IFW record indicates that the following document type was received in electronic format on the date identified above. This content is stored in the SCORE database.

Since this was an electronic submission, there is no physical artifact folder, no artifact folder is recorded in PALM, and no paper documents or physical media exist. The TIFF images in the IFW record were created from the original documents that are stored in SCORE.

- Drawing

At the time of document entry (noted above):

- USPTO employees may access SCORE content via DAV or via the SCORE web page.
- External customers may access SCORE content via PAIR using the Supplemental Content tab.

Form Revision Date: March 1, 2019

Docket No. 533055US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

INVENTOR(S) Changhyun LEE, et al.

SERIAL NO: New Application

ART UNIT:

FILING DATE: Herewith

EXAMINER:

FOR: ARCHITECTURE AND METHOD FOR NAND MEMORY OPERATION

FEE TRANSMITTAL

- ☐ No additional fee is required
- ☐ Small entity status of this application under 37 C.F.R. §1.9 and §1.27 is claimed.
- ☐ Track 1 Prioritized Examination

The Fee has been calculated as shown below:

FOR	NUMBER FILED	NUMBER EXTRA	RATE	CALCULATIONS
TOTAL CLAIMS	20 - 20 =	0	x \$100 =	\$0.00
INDEPENDENT CLAIMS	3 - 3 =	0	x \$480 =	\$0.00
UTILITY APPLICATION SIZE FEE	42* - 100 = (* 56 x .75)	0 (each addtl. 50 sheets over 100)	x \$420 =	\$0.00
☐ MULTIPLE DEPENDENT CLAIMS (If applicable)			+ \$860 =	\$0.00
☐ LATE FILING OF DECLARATION			+ \$160 =	\$0.00
☐ NON-ELECTRONIC FILING FEE			+ \$400 =	\$0.00
☒ FILING FEE (\$320.00)	☒ SEARCH FEE (\$700.00)	☒ EXAMINATION FEE (\$800.00)	BASIC FEES	\$1,820.00
TOTAL OF ABOVE CALCULATIONS				\$1,820.00
☐ REDUCTION BY 50% FOR FILING BY SMALL ENTITY				\$0.00
☐ FILING FEE REDUCED IF E-FILED – SMALL ENTITY			+ \$-80 =	\$0.00
☐ FILING IN NON-ENGLISH LANGUAGE			+ \$140 =	\$0.00
TOTAL				\$1,820.00

- ☐ Please charge Deposit Account No. **15-0030** in the amount of **\$0.00**
- ☒ Credit card payment is being made online (if electronically filed), or is attached hereto (if paper filed), in the amount of **\$1,820.00**.
- ☒ The Director is hereby authorized to charge any additional fees which may be required for the papers being filed herewith and for which no payment is enclosed herewith, or credit any overpayment to Deposit Account No. **15-0030**, with the **EXCEPTION** of deficiencies in fees for multiple dependent claims in new applications.

Submitted by: 

Johnny Ma

Registration No. 59,976

Customer Number

22850

Tel. (703) 413-3000
Fax. (703) 413-2220
(OMMN 02/12)

Leonidas Boutsikaris, Ph.D.

Registration No.: 61,377

ARCHITECTURE AND METHOD FOR NAND MEMORY OPERATION

RELATED APPLICATION

[0001] This application is a bypass continuation of International Application No. PCT/CN2020/136482, filed on December 15, 2020. The entire disclosure of the prior application is hereby incorporated by reference in its entirety.

BACKGROUND

[0002] Flash memory devices have recently been through a rapid development. The flash memory devices are able to retain the stored data for a long period of time without applying a voltage. Further, the reading rate of the flash memory devices is relatively high, and it is easy to erase stored data and rewrite data into the flash memory devices. Thus, the flash memory devices have been widely used in micro-computers, automatic control systems, and the like. To increase the bit density and reduce the bit cost of the flash memory devices, three-dimensional (3D) NAND (Not AND) flash memory devices have been developed.

[0003] The 3D-NAND memory device can include a plurality of memory cell strings. Each of the memory cell strings can include a bottom-select-gate (BSG) transistor, memory cells, and a top-select-gate (TSG) transistor that are connected in series. In a method of verifying/reading memory cells of the 3D-NAND flash memory devices that are programmed, a pre-pulse scheme (or stage) and a verify/read scheme (or stage) can be included. In the pre-pulse scheme, a pass voltage, such as 6.8 volts, can be applied on word lines (WLs) of the memory cells in a selected memory cell string, while a gate

terminal of the TSG transistor can be turned on at an unselected memory cell string. In the verify/read scheme, the pass voltage can be sustained further through the verify/read scheme at unselected WLs of the selected memory cell string, and a verify voltage can be applied on a WL of a selected memory cell in the selected memory cell string.

SUMMARY

[0004] The present disclosure describes embodiments generally related to apparatuses and methods for verifying/reading memory cells of a 3D-NAND memory device to reduce hot carrier injection (HCI)-induced edge summation (ESUM) loss, and reduce power consumption during verifying/reading the memory cells of the 3D-NAND memory device.

[0005] According to an aspect of the disclosure, a method for reading a memory device is provided. The memory device can include a first memory cell string and a second memory cell string, where the first memory cell string can include a bottom-select-gate (BSG) transistor, memory cells, and a top-select-gate (TSG) transistor that are connected in series, and the second memory cells string can include a BSG transistor, memory cells, and a TSG transistor that are connected in series. In the method, in a pre-verify stage, a first verify voltage can be applied on a gate terminal of a selected memory cell of the first memory cell string, where the selected memory cell can be programmed and arranged between a first adjacent memory cell and a second adjacent memory cell. In the pre-verify stage, a first bias voltage can be applied on a gate terminal of at least one memory cell of the first memory cell string that is positioned between the first adjacent memory cell of the selected memory cell and the

TSG transistor of the first memory cell string. In a verify stage, a second verify voltage can be applied on the gate terminal of the selected memory cell of the first memory cell string. Further, in the verify stage, a second bias voltage can be applied on the gate terminal of the at least one memory cell of the first memory cell string that is positioned between the first adjacent memory cell of the selected memory cell and the TSG transistor of the first memory cell string. The second bias voltage is smaller than the first bias voltage.

[0006] In some embodiments, the second bias voltage can be from 20% to 30% smaller than the first bias voltage.

[0007] In the method, in the pre-verify stage, a first gate voltage can be applied on a gate terminal of the TSG transistor of the second memory cell string. A first pass voltage can be applied on a gate terminal of the first adjacent memory cell of the selected memory cell of the first memory cell string. A first read voltage can be applied on a gate terminal of the second adjacent memory cell of the selected memory cell of the first memory cell string. Further, in the verify stage, a second gate voltage can be applied on the gate terminal of the TSG transistor of the second memory cell string. A second pass voltage can be applied on the gate terminal of the first adjacent memory cell of the selected memory cell in the first memory cell string. A second read voltage can be applied on the gate terminal of the second adjacent memory cell of the selected memory cell in the first memory cell string. In addition, at least one of the second pass voltage and the second read voltage can be larger than the second gate voltage.

[0008] In the method, a bottom bias voltage can be applied on a gate terminal of the BSG transistor of the first memory cell string in the pre-verify stage and the verify

stage. A top bias voltage can be applied on a gate terminal of the TSG transistor of the first memory cell string in the pre-verify stage and the verify stage. A positive voltage can be applied on gate terminals of any memory cells that are positioned between the second adjacent memory cell of the selected memory cell and the BSG transistor of the first memory cell string in the pre-verify stage and the verify stage.

[0009] In some embodiments, the first verify voltage can be smaller than the second verify voltage.

[0010] In some embodiments, the first bias voltage can be increased from an initial voltage, and then reduced to the second bias voltage in a first portion of the pre-verify stage, where the first bias voltage can be equal to the second bias voltage in a second portion of the pre-verify stage. The first pass voltage can be increased from the initial voltage to the second pass voltage in the pre-verify stage. The first read voltage can be increased from the initial voltage to the second read voltage in the pre-verify stage. The first gate voltage can be increased from the initial voltage to a voltage that is maintained for a duration of time, and then the first gate voltage is reduced to the second gate voltage in the first portion of the pre-verify stage, where the first gate voltage can be equal to the second gate voltage in the second portion of the pre-verify stage.

[0011] In some embodiments, the bottom bias voltage can be increased from the initial voltage to a voltage that is maintained through the second portion of the pre-verify stage and the verify stage. The top bias voltage can be increased from the initial voltage to a voltage that is maintained through the second portion of the pre-verify stage and

the verify stage. The positive voltage can be increased from the initial voltage in the pre-verify stage.

[0012] According to another aspect of the disclosure, a method for reading a memory device is provided. The memory device can include a first memory cell string and a second memory cell string. The first memory cell string can include a bottom-select-gate (BSG) transistor, memory cells, and a top-select-gate (TSG) transistor that are connected in series. The second memory cells string can include a BSG transistor, memory cells, and a TSG transistor that are connected in series. In the method, in a pre-verify stage, a first verify voltage can be applied on a gate terminal of a selected memory cell of the first memory cell string, where the selected memory cell can be programmed and arranged between a first adjacent memory cell and a second adjacent memory cell. In the pre-verify stage, a first bias voltage can be applied on a gate terminal of at least one memory cell of the first memory cell string that is positioned between the second adjacent memory cell of the selected memory cell and the BSG transistor of the first memory cell string. In a verify stage, a second verify voltage can be applied on the gate terminal of the selected memory cell of the first memory cell string. In addition, in the verify stage, a second bias voltage can be applied on the gate terminal of the at least one memory cell of the first memory cell string that is positioned between the second adjacent memory cell of the selected memory cell and the BSG transistor of the first memory cell string. The second bias voltage can be smaller than the first bias voltage.

[0013] In some embodiments, the second bias voltage can be from 20% to 30% smaller than the first bias voltage.

[0014] In the method, in the pre-verify stage, a first gate voltage can be applied on a gate terminal of the TSG transistor of the second memory cell string. A first pass voltage can be applied on a gate terminal of the first adjacent memory cell of the selected memory cell in the first memory cell string. A first read voltage can be applied on a gate terminal of the second adjacent memory cell of the selected memory cell in the first memory cell string. Further, in the verify stage, a second gate voltage can be applied on the gate terminal of the TSG transistor of the second memory cell string. A second pass voltage can be applied on the gate terminal of the first adjacent memory cell of the selected memory cell in the first memory cell string. A second read voltage can be applied on the gate terminal of the second adjacent memory cell of the selected memory cell in the first memory cell string. In addition, at least one of the second pass voltage and the second read voltage can be larger than the second gate voltage.

[0015] In the method, a bottom bias voltage can be applied on a gate terminal of the BSG transistor of the first memory cell string in the pre-verify stage and the verify stage. A top bias voltage can be applied on a gate terminal of the TSG transistor of the first memory cell string in the pre-verify stage and the verify stage. A positive voltage can be applied on gate terminals of any memory cells that are positioned between the first adjacent memory cell of the selected memory cell and the TSG transistor of the first memory cell string in the pre-verify stage and the verify stage.

[0016] In some embodiments, the first verify voltage can be smaller than the second verify voltage.

[0017] In some embodiments, the first bias voltage can be increased from an initial voltage, and then reduced to the second bias voltage in a first portion of the pre-verify

stage. The first bias voltage can be equal to the second bias voltage in a second portion of the pre-verify stage. The first pass voltage can be increased from the initial voltage to the second pass voltage in the pre-verify stage. The first read voltage can be increased from the initial voltage to the second read voltage in the pre-verify stage. The first gate voltage can be increased from the initial voltage to a voltage that is maintained for a duration of time, and then the first gate voltage is reduced to the second gate voltage in the first portion of the pre-verify stage. The first gate voltage can be equal to the second gate voltage in the second portion of the pre-verify stage.

[0018] In some embodiments, the bottom bias voltage can be increased from the initial voltage to a voltage that is maintained through the second portion of the pre-verify stage and the verify stage. The top bias voltage can be increased from the initial voltage to a voltage that is maintained through the second portion of the pre-verify stage and the verify stage. The positive voltage can be increased from the initial voltage in the pre-verify stage.

[0019] According to yet another aspect of the disclosure, an apparatus for reading a memory device is provided. The memory cell can include a first memory cell string and a second memory cell string. The first memory cell string can include a bottom-select-gate (BSG) transistor, memory cells, and a top-select-gate (TSG) transistor that are connected in series. The second memory cells string can include a BSG transistor, memory cells, and a TSG transistor that are connected in series. The apparatus can include processing circuitry configured to apply, in a pre-verify stage, a first verify voltage on a gate terminal of a selected memory cell of the first memory cell string, where the selected memory cell can be programmed and arranged between a first

adjacent memory cell and a second adjacent memory cell. The processing circuitry can also be configured to apply, in the pre-verify stage, a first bias voltage on a gate terminal of at least one memory cell of the first memory cell string that is not programmed. In a verify stage, the processing circuitry can be configured to apply a second verify voltage on the gate terminal of the selected memory cell of the first memory cell string. Further, the processing circuitry can be configured to apply, in the verify stage, a second bias voltage on the gate terminal of the at least one memory cell of the first memory cell string that is not programmed. The second bias voltage can be smaller than the first bias voltage.

[0020] In some embodiments, the at least one memory cell of the first memory cell string that receives the first bias voltage and the second bias voltage can be positioned between the first adjacent memory cell of the selected memory cell and the TSG transistor of the first memory cell string.

[0021] In some embodiments, the at least one memory cell of the first memory cell string that receives the first bias voltage and the second bias voltage is positioned between the second adjacent memory cell of the selected memory cell and the BSG transistor of the first memory cell string.

[0022] In the pre-verify stage, the processing circuitry can further be configured to apply a first gate voltage on a gate terminal of the TSG transistor of the second memory cell string. The processing circuitry can be configured to apply a first pass voltage on a gate terminal of the first adjacent memory cell of the selected memory cell in the first memory cell string. The processing circuitry can be configured to apply a first read voltage on a gate terminal of the second adjacent memory cell of the selected memory

cell in the first memory cell string. In the verify stage, the processing circuitry can be configured to apply a second gate voltage on the gate terminal of the TSG transistor of the second memory cell string. The processing circuitry can also be configured to apply a second pass voltage on the gate terminal of the first adjacent memory cell of the selected memory cell in the first memory cell string. The processing circuitry can be configured to apply a second read voltage on the gate terminal of the second adjacent memory cell of the selected memory cell in the first memory cell string, where at least one of the second pass voltage and the second read voltage can be larger than the second gate voltage.

[0023] In an embodiment, the processing circuitry can be configured to apply a bottom bias voltage on a gate terminal of the BSG transistor of the first memory cell string in the pre-verify stage and the verify stage. The processing circuitry can be configured to apply a top bias voltage on a gate terminal of the TSG transistor of the first memory cell string in the pre-verify stage and the verify stage. The processing circuitry can be configured to apply a positive voltage on gate terminals of any memory cells that are positioned between the second adjacent memory cell of the selected memory cell and the BSG transistor of the first memory cell string in the pre-verify stage and the verify stage.

[0024] In another embodiment, the processing circuitry can be configured to apply a bottom bias voltage on a gate terminal of the BSG transistor of the first memory cell string in the pre-verify stage and the verify stage. The processing circuitry can be configured to apply a top bias voltage on a gate terminal of the TSG transistor of the first memory cell string in the pre-verify stage and the verify stage. The processing

circuitry can be configured to apply a positive voltage on gate terminals of any memory cells that are positioned between the first adjacent memory cell of the selected memory cell and the TSG transistor of the first memory cell string in the pre-verify stage and the verify stag

[0025] Aspects of the disclosure also provide a non-transitory computer-readable medium storing instructions which when executed by a computer for verifying/reading a memory device cause the computer to perform one or more of the methods described above.

BRIEF DESCRIPTION OF THE DRAWINGS

[0026] Aspects of the present disclosure can be understood from the following detailed description when read with the accompanying figures. It is noted that, in accordance with the standard practice in the industry, various features are not drawn to scale. In fact, the dimensions of the various features may be increased or reduced for clarity of discussion.

[0027] Figure 1 is a schematic diagram of a 3D-NAND memory device, in accordance with exemplary embodiments of the disclosure.

[0028] Figure 2 is a cross-sectional view of a 3D-NAND memory device, in accordance with exemplary embodiments of the disclosure.

[0029] Figure 3 is a schematic diagram of NAND memory cell strings, in accordance with exemplary embodiments of the disclosure.

[0030] Figure 4 is a first schematic diagram of verifying/reading memory cells in a related example, in accordance with exemplary embodiments of the disclosure.

[0031] Figure 5 is a second schematic diagram of verifying/reading memory cells in a related example, in accordance with exemplary embodiments of the disclosure.

[0032] Figure 6 is a first schematic diagram of verifying/reading memory cells that are programmed in a forward order, in accordance with exemplary embodiments of the disclosure.

[0033] Figure 7 is a second schematic diagram of verifying/reading memory cells that are programmed in a forward order, in accordance with exemplary embodiments of the disclosure.

[0034] Figure 8 is a first schematic diagram of verifying/reading memory cells that are programmed in a reverse order, in accordance with exemplary embodiments of the disclosure.

[0035] Figure 9 is a second schematic diagram of verifying/reading memory cells that are programmed in a reverse order, in accordance with exemplary embodiments of the disclosure.

[0036] Figures 10 is a flow chart diagram of a method for verifying/reading memory cells, in accordance with exemplary embodiments of the disclosure.

[0037] Figure 11 is a block schematic of an electronic system, in accordance with exemplary embodiments of the disclosure.

DETAILED DESCRIPTION

[0038] The following disclosure provides many different embodiments, or examples, for implementing different features of the provided subject matter. Specific examples of components and arrangements are described below to simplify the present disclosure.

These are, of course, merely examples and are not intended to be limiting. For example, the formation of a first feature over or on a second feature in the description that follows may include embodiments in which the first and second features may be in direct contact, and may also include embodiments in which additional features may be formed between the first and second features, such that the first and second features may not be in direct contact. In addition, the present disclosure may repeat reference numerals and/or letters in the various examples. This repetition is for the purpose of simplicity and clarity and does not in itself dictate a relationship between the various embodiments and/or configurations discussed.

[0039] Further, spatially relative terms, such as “beneath,” “below,” “lower,” “above,” “upper” and the like, may be used herein for ease of description to describe one element or feature’s relationship to another element(s) or feature(s) as illustrated in the figures. The spatially relative terms are intended to encompass different orientations of the device in use or operation in addition to the orientation depicted in the figures. The apparatus may be otherwise oriented (rotated 90 degrees or at other orientations) and the spatially relative descriptors used herein may likewise be interpreted accordingly.

[0040] In a related example, in order to verify/read memory cells of a 3D-NAND memory device that are programmed, a pre-pulse scheme (or stage) and a verify/read scheme (or stage) can be included in a verify/read operation. In the pre-pulse scheme, a pass voltage, such as 6.8 volts, can be applied on word lines (WLs) of the memory cells in a selected memory cell string, while a gate terminal of a TSG transistor can be turned on at an unselected memory cell string. In the verify/read scheme, the pass voltage can be sustained further through the verify/read scheme at unselected WLs of the selected

memory cell string, and a verify voltage can be applied on a WL of a selected memory cell in the selected memory cell string.

[0041] When a sufficient pre-pulse time is applied in the pre-pulse scheme, the pass voltage can be developed fully before the TSG transistor is switched off at the unselected memory cell string. As a result, when the TSG transistor of the unselected memory cell string is turned off in the verify/read scheme, although a drain-side channel (or terminal) of the unselected memory cell string is isolated from a bit line that is coupled to the unselected memory cell string, a considerable gradient of a channel potential may not be induced by subsequent verify/read voltages in the verify/read scheme. Accordingly, hot carrier injections (HCI) may not be generated from a selected memory cell to an upper memory cell of the selected memory cell in the selected memory cell string. Thus, an edge summation (ESUM) loss can be prevented. The ESUM loss can be associated with a read margin of the 3D-NAND memory device.

[0042] However, when an insufficient pre-pulse time is applied in the pre-pulse scheme, the pass voltage may not be developed fully before the TSG transistor is switched off at the unselected memory cell string. In the verify/read scheme, when the TSG transistor is switched off at the unselected memory cell string, the pass voltage applied on WLs of memory cells that are positioned above the selected memory cell in the selected memory cell string can still be developed to a target value, such as 6.8 volts. Thus, the drain-side channel of the unselected memory cell string can be boosted additively by the increment of the pass voltage in the verify/read scheme, which in turn can bring in the HCI between the selected memory cell and the upper adjacent memory cell of the selected memory cell, and result in the ESUM loss.

[0043] In the present disclosure, in order to verify/read programmed memory cells of a 3D-NAND memory device, a pre-pulse voltage can be applied on at least one memory cell of the selected memory cell string that is positioned above an upper adjacent memory cell of the selected memory cell string in the pre-verify scheme. A pass voltage that is smaller than the pre-pulse voltage can be applied on the at least one memory cell of the selected memory cell string that is positioned above the upper adjacent memory cell of the selected memory cell in the verify/read scheme. In addition, a pass voltage that is applied on one of the upper adjacent memory cell and a lower adjacent memory cell of the selected memory cell can be larger than a bias voltage applied on the TSG transistor of the unselected memory cell string in the verify/read scheme, where the bias voltage is applied to turn off the TSG transistor of the unselected memory cell string. Accordingly, hot-carrier injection (HCI)-induced ESUM loss can be prevented, and power consumption during verifying/reading the memory cells of the 3D-NAND memory device can be reduced.

[0044] A 3D-NAND device can include a plurality of planes. Each of the planes can include a plurality of blocks. FIG. 1 is an exemplary embodiment of a 3D-NAND device 100 (or device 100). As shown in FIG. 1, the device 100 can include planes 102 and 104. Each of the planes 102 and 104 can include two respective blocks. For example, the plane 102 can include two blocks 106 and 108, and the plane 104 can include two blocks 110 and 112. Further, each of the blocks can include a plurality of memory cell strings, where memory cells are disposed sequentially and in series over a substrate along a height direction of the device 100. Of course, it should be noted that FIG. 1 is

merely an example, and the device 100 can include any number of planes, and each of the planes can include any number of blocks according to the device designs.

[0045] In the device 100, each of the planes can be coupled to a respective cache structure, such as a dynamic data cache (DDC), or a static page buffer (SPB). For example, the block 106 can be coupled to a cache structure 114 and the block 108 can be coupled to a cache structure 116. The cache structure can include sense amplifiers that are coupled to bit lines and configured to sense signals during the operation of the 3D-NAND device 100, such as verifying/reading, programming, or erasing memory cells of the 3D-NAND device 100. The device 100 can also include periphery circuits 122 that can include decoder structures, driver structures, charge structures, and other structures to operate the memory cells.

[0046] In the device 100, each of the blocks can include staircase regions and array regions that are formed in a stack of word line layers and insulating layers. FIG. 2 is an exemplary embodiment of the block 106 of the device 100. As shown in FIG. 2, the block 106 can include an array region 200A and staircase regions 200B-200C that are arranged in a dielectric layer 24. The array region 200A can be arranged between the staircase regions 200B-200C, and formed in a stack of alternating word line layers 12a-12p and insulating layers 14a-14q over a substrate 10. The word line layers 12a-12p can include one or more bottom select gate (BSG) layers, gate layers (or word line layers), and one or more top select gate (TSG) layers that are arranged sequentially over the substrate 10. For example, the word line layer 12a can be a BSG layer, and the word line layer 12p can be a TSG layer in the device 100.

[0047] In some embodiments, the device 100 can include one or more bottom dielectric trenches (e.g., 26 and 28) that are formed in the one or more BSGs (e.g., in the word line layer 12a). The bottom dielectric trenches 26 and 28 can extend in an X-direction of the substrate 10 to separate the BSGs into a plurality of sub-BSGs (e.g., 12a-1, 12a-2, and 12a-3). In addition, one or more top dielectric trenches (e.g., 30 and 32) can be formed in the one or more TSGs (e.g., in the word line layer 12p). The top dielectric trenches 30 and 32 can also extend in the X-direction of the substrate 10 to separate the TSGs into a plurality of sub-TSGs (e.g., 12p-1, 12p-2, and 12p-3). The sub-BSGs and sub-TSGs can divide the device 100 into a plurality of sub-blocks. Each of the sub-blocks can have a respective sub-BSG and a respective sub-TSG. Thus, memory cells strings in a corresponding sub-block can be operated individually through controlling the respective sub-BSG and respective sub-TSG.

[0048] The array region 200A can include a plurality of channel structures 18. Each of the channel structures 18 can include a respective top channel contact 19 and a respective bottom channel contact 21. Each of the channel structure 18 can extend through the stack and be coupled to the word line layers 12a-12p to form a respective vertical NAND memory cell string. The vertical NAND memory cell string can include one or more bottom select transistors (BSTs), a plurality of memory cells (MCs), and one or more top select transistors (TSTs) that are disposed sequentially and in series over the substrate along a height direction (e.g., Z direction) of the substrate 10. The one or more BSTs can be formed of the channel structure and the one or more BSG layers, the MCs can be formed of the channel structure and the word line layers, and the

one or more TSTs can be formed of the channel structure and the one or more TSG layers.

[0049] In the device 100, each of the memory cells can store one or more logic bits, according to the device designs. For example, the memory cells can be single level cells (SLCs), multiple level cells (MLCs), or triple level cells (TLCs). Accordingly, each of the memory cells can store one logic bit, two logic bits, or three logic bits.

[0050] Still referring to FIG. 2, the word line layers 12a-12p can be formed in a stair-cased configuration in the staircase regions 200A-200B, and a plurality of word line contacts 22 can be formed along the height direction and coupled to the word line layers 12a-12p. Thus, gate voltages can be applied on gates of the memory cells through the word line contacts 22 that are coupled to the word line layers 12a-12p.

[0051] In addition, each of the channel structures can further be coupled to a respective bit line (or bit line structure). In some embodiments, the bit line can be connected to the top channel contact 19 of the channel structure 18, and configured to apply a bias voltage when operating the channel structure, such as programming, erasing, or reading the channel structure. The device 100 can have a plurality of slit structures (or gate line slit structures). For example, two slit structures 20a-20b are included in FIG. 2. The slit structures 20a-20b can be made of conductive materials and positioned on array common source (ACS) regions 16 to serve as contacts. The ACS regions are formed in the substrate 10 to serve as common sources of the device 100.

[0052] FIG. 3 is a schematic view of NAND memory cell strings (or strings) 300A and 300B that can be formed in the device 100. As shown in FIG. 3, the string 300A can include a bottom select transistor (BST) or bottom-select-gate (BSG) transistor 302A, a

plurality of memory cells (MCs) 304A, and a top select transistor (TST) or top-select-gate (TSG) transistor 306A that are disposed sequentially and in series over the substrate along the height direction (e.g., Z direction) of the substrate 10. Similarly, the string 300B can include a bottom select transistor (BST) or bottom-select-gate (BSG) transistor 302B, a plurality of memory cells (MCs) 304B, and a top select transistor (TST) or top-select-gate (TSG) transistor 306B that are disposed sequentially and in series over the substrate along the height direction (e.g., Z direction) of the substrate 10. The string 300A can be coupled to a bit line 308A through a drain terminal of the TST 306A, and coupled to an ACS (e.g., 16) through a source terminal of the BST 302A. The string 300B can be coupled to a bit line 308B through a drain terminal of the TST 306B, and coupled to the ACS (e.g., 16) through a source terminal of the BST 302B. During the operation of the device 100, appropriate voltages can be applied to the bit lines 308A and 308B, the gates of the TST 306A and 306B through the sub-TSG layers (e.g., 12p-1, 12p-2, and 12p-3), the gates of the MCs 304A and 304B through the WL layers (e.g., 12b-12o), the gates of the BST 302A and 302B through the sub-BSG layers (e.g., 12a-1, 12a-2, and 12a-3), and the ACS through the slit structures (e.g., 20a or 20b).

[0053] When a selected memory cell of the 3D-NAND memory device is programmed, a verify/read operation can be applied to verify if a selected memory cell (e.g., MCn) has been programmed successfully. In the verify/read operation, bias voltages (or pass voltages) can be applied on gate terminals (or gates) of the TSG transistor through the TSG layer, the BSG transistor through the BSG layer, and the unselected MCs through the WL layers respectively. The bias voltages can be sufficient, such as 6.8 volts, to

turn on the TSG transistor, the BSG transistor, and the unselected MCs. In addition, a read (or verify) voltage can be applied on the gate terminal (or gate) of the selected memory cell MC_n through a WL layer (e.g., WL_n) that is coupled to the selected memory cell MC_n. The read voltage can be equal to a threshold voltage of the selected memory cell when the selected memory cell is not programmed. When the selected memory cell is programmed, the threshold voltage can be increased. Thus, when the selected memory cell is programmed successfully, the read voltage cannot turn on the selected memory cell. Accordingly, the sense amplifier cannot detect current to flow through the memory cell string from ACS region (e.g., 16) to the bit line. When the selected memory cell is not programmed successfully, the read voltage can turn on the selected memory cell, and the sense amplifier can detect current to flow through the memory cell string from ACS region (e.g., 16) to the bit line.

[0054] FIG. 4 is a first schematic diagram of a verify/read operation to verify/read memory cells of a 3D-NAND memory device (e.g., device 100) in a related example. As shown in FIG. 4, the verify/read operation can include an initial stage, a pre-pulse stage, a verify/read stage, a post-pulse stage, and a recovery stage. The verify/read operation can be configured to verify whether memory cells are programmed successfully by applying appropriate bias voltages on the word line layers of the memory cells, the TSG layer of the TSG transistor, and the BSG layer of the BSG transistor. In an exemplary embodiment of FIG.4, the memory cells of the device 100 can be programmed in a forward order. Thus, memory cells in a memory cell string are programmed from a bottom MC adjacent to the BSG transistor to a top MC adjacent to the TSG transistor. For example, in the memory cell string 300A, the memory cells are

programmed sequentially from MC0 to the top MC that is adjacent to the TSG transistor 306A.

[0055] FIG. 4 illustrates the bias voltages applied on two exemplary memory cell strings that include a selected memory cell string (e.g., 300A) and an unselected memory cell string (e.g., 300B). The selected memory cell string can have a selected TSG layer coupled to the TSG transistor (e.g., 306A), a selected word line layer WLn coupled to a selected memory cell (e.g., MCn), a word line layer $WLn+1$ coupled to a memory cell $MCn+1$ that is an upper adjacent memory cell of selected memory cell MCn , a word line layer $WLn-1$ coupled to a memory cell $MCn-1$ that is a lower adjacent memory cell of the selected memory cell MCn , word line layers $WLs (>n+1)$ coupled to the memory cells that are unselected and positioned above the memory cell $MCn+1$, word line layers $WLs (<n-1)$ coupled to the memory cells that are unselected and positioned below the memory cell $MCn-1$, and a BSG layer coupled to the BSG transistor (e.g., 302A). The TSG transistor (or TST) 306A, the memory cells, and the BSG transistor (BST) 302A are connected in series, which can be shown in FIG. 3.

[0056] Still referring to FIG. 4, the unselected memory cell string (e.g., 300B) can have a unselected TSG layer coupled to the TSG transistor (e.g., 306B), a selected word line layers WLn coupled to a selected memory cell (e.g., MCn), a word line layer $WLn+1$ coupled to a memory cell $MCn+1$ that is an upper adjacent memory cell of the selected memory cell MCn , a word line layer $WLn-1$ coupled to a memory cell $MCn-1$ that is a lower adjacent memory cell of the selected memory cell MCn , word line layers $WLs (>n+1)$ coupled to the memory cells that are unselected and positioned above the memory cell $MCn+1$, word line layers $WLs (<n-1)$ coupled to the memory cells that are

unselected and positioned below the memory cell MCn-1, and a BSG layer coupled to the BSG transistor (e.g., 302B). As shown in FIG. 3, the TSG transistor (or TST) 306B, the memory cells, and the BSG transistor (or BST) 302B are connected in series.

[0057] In some embodiments the selected TSG layer and the unselected TSG layer can be one of the sub-TSG layers 12p-1, 12p-2, and 12p-3 that are separated from one another by the top dielectric trenches 30 and 32, for example. In some embodiments, the word line layers in the selected memory cell string and the word line layers in the unselected memory cell string can be the word line layers 12b-12o that are illustrated in FIG. 2. Thus, a memory cell of the selected memory cell string is coupled to a memory cell in a corresponding position of the unselected memory cell. For example, the selected memory cell MCn of the selected memory cell string 300A is coupled to the selected memory cell MCn of the unselected memory cell string 300B through a same word line layer.

[0058] When the verify/read operation is started, in the initial stage of the verify/read operation shown in FIG. 4, an initial voltage, such as zero volt, can be applied on the selected TSG layer, the unselected TSG layer, the WLs ($>n+1$), the WLn+1, the WLn, the WLs ($<n-1$), and the BSG layer. Further, appropriate bias voltages can be applied on the selected TSG layer, the unselected TSG layer, the WLs ($>n+1$), the WLn+1, the WLn, the WLs ($<n-1$), and the BSG layer in the pre-pulse stage respectively. For example, a bias voltage (or top bias voltage), such as 5 volts, can be applied on the selected TSG layer of the selected memory cell string. A bias voltage (or gate voltage), such as 5 volts, can be applied on the unselected TSG layer of the unselected memory cell string. A bias voltage, such as 6.8 volts, can be applied on the WLs ($>n+1$). A bias

voltage (or pass voltage), such as 6.8 volts, can be applied on the $WLn+1$. A bias voltage (or verify voltage), such as 6.8 volts, can be applied on the selected word line layer WLn . A bias voltage (or read voltage), such as 6.8 volts, can be applied on $WLn-1$. A bias voltage (or positive voltage), such as 6.8 volts, can be applied on the WLs ($<n-1$). In addition, a bias voltage (or bottom bias voltage), such as 5 volts, can be applied on the BSG layer. The pre-pulse stage can be configured to apply sufficient bias voltages to form conducting channels in the selected memory cell string and the unselected memory cell string respectively.

[0059] When the verify/read operation proceed to the verify/read stage, the bias voltage (or top bias voltage) applied on the selected TSG layer of the selected memory cell string remains. The bias voltage (or gate voltage) applied on the unselected TSG layer of the unselected memory cell string can be reduced to a lower voltage, such as zero volt to turn off the TSG transistor (e.g., 306B) of the unselected memory cell string. Accordingly, the unselected memory cell string is isolated from the bit line (e.g., 308B). The bias voltage applied on the WLs ($>n+1$) can be maintained to keep the channel of the selected memory cell string conductive. The bias voltage (or pass voltage) applied on the $WLn+1$ can be increased, such as by one volt, from the bias voltage applied on the pre-pulse stage. In addition, the bias voltage (or read voltage) applied on $WLn-1$ can be increased, such as by one volt, from the bias voltage applied on the pre-pulse stage. A higher bias voltage applied on the $WLn+1$ and the $WLn-1$ can help form source/drain regions for the selected memory cell MCn .

[0060] Still referring to FIG. 4, the bias voltage (or verify voltage) applied on the selected word line layer WLn can be reduced to a programming verify (PV) level. In

some embodiments, the PV level can be in a range from zero volt to one volt. The bias voltage (or positive voltage) applied on the WLs ($<n-1$) can be maintained to keep the channel of the selected memory cell string conductive. In addition, the bias voltage (or bottom bias voltage) applied on the BSG layer can be maintained to keep the channel of the selected memory cell string conductive. As mentioned above, the bias voltage (or verify voltage) applied on the selected word line layer WLn can be equal to the threshold voltage of the selected memory cell when the selected memory cell is not programmed. When the selected memory cell is programmed, the threshold voltage can be increased. Thus, when the selected memory cell is programmed successfully, the read voltage cannot turn on the selected memory cell. Accordingly, the sense amplifier cannot detect current to flow through the memory cell string from ACS to the bit line. When the selected memory cell is not programmed successfully, the read voltage can turn on the selected memory cell, and the sense amplifier can detect current to flow through the memory cell string from ACS to the bit line.

[0061] It should be noted that in FIG. 4, a long pre-pulse time, such as in a range from 1ns to 10 us, is applied in the pre-pulse stage. When the long pre-pulse time is sufficient for the bias voltages to be developed fully before the TSG transistor is switched off at the unselected memory cell string, a considerable gradient of a channel potential may not be induced by subsequent verify/read pulses in the verify/read stage. Thus, hot carrier injection (HCI) may not be generated from the selected memory cell to the upper adjacent memory cell of the selected memory cell in the selected memory cell. However, when the long pre-pulse time is insufficient for the bias voltages in the pre-pulse stage to be developed fully before the TSG transistor is switched off at the

unselected memory cell string, a considerable gradient of the channel potential can be induced by subsequent verify/read pulses in the verify/read stage, and HCI can be generated from the selected memory cell to the upper adjacent memory cell of the selected memory cell in the selected memory cell.

[0062] FIG. 5 is a second schematic diagram of a verify/read operation to verify/read memory cells of a 3D-NAND memory device (e.g., device 100) that are also programmed in the forward order in a related example. The verify/reading operation can have a pre-pulse stage with a short pre-pulse time. The short pre-pulse time may be insufficient for the bias voltages applied on the WLs ($>n+1$), $WLn+1$, WLn , $WLn-1$, and WLs ($<n-1$) to be developed fully in the pre-pulse stage. For example, as shown in FIG. 5, the bias voltages are less than a target value, such as 6.8 volts. The bias voltages can still be developed to the target value, such as 6.8 volts, in the verify/read stage. Thus, the drain-side channel of the unselected memory cell string can be boosted additively by incrementing the bias voltages in the verify/read stage, which can bring in the HCI between the selected memory cell (WLn) and the upper adjacent memory cell ($WLn+1$) of the selected memory cell, and result in the ESUM loss.

[0063] FIG. 6 is a first schematic diagram of a verify/read operation to verify/read memory cells of a 3D-NAND memory device (e.g., device 100) in accordance with exemplary embodiments of the disclosure. As shown in FIG. 6, the memory cells can be programmed in the forward order, and the verify/read operation can include a long pre-pulse time in the pre-pulse stage. In an exemplary embodiment of FIG. 6, the memory cells $MC0$ - MCn are programmed, and the memory cells above MCn are not

programmed. In addition, the memory cell MC_n that is coupled to the WL_n is selected to receive the verify/read operation.

[0064] Compared to the verify/read operation in FIG. 4, the bias voltage applied on the WLs (>n+1) in the verify/read stage is lower than the bias voltage applied on the WLs (>n+1) in the pre-pulse stage. In an exemplary embodiment of FIG. 6, the bias voltage applied on the WLs (>n+1) in the verify/read stage can be 3 volts, and the bias voltage applied on the WLs (>n+1) in the pre-pulse stage can be 6.8 volts. In some embodiments, the bias voltage applied on the WLs (>n+1) in the verify/read stage is a percentage (e.g., from 20% to 30%) lower than the bias voltage applied on the WLs (>n+1) in the pre-pulse stage. In some embodiments, each of the memory cells that are positioned above the upper adjacent memory cell of the selected memory cell MC_n can receive a bias voltage through the WLs (>n+1) in the verify/read stage that is lower than a bias voltage in the pre-pulse stage. In some embodiments, at least one memory cell of the memory cells that are positioned between the upper adjacent memory cell of the selected memory cell MC_n and the TSG transistor can receive a bias voltage through the WLs (>n+1) in the verify/read stage that is lower than a bias voltage in the pre-pulse stage. For example, a memory cell that is adjacent to the TSG transistor can receive a bias voltage in the verify/read stage that is lower than a bias voltage in the pre-pulse stage.

[0065] By introducing a lower bias voltage in the verify/read stage in the memory cells that are positioned above the upper adjacent memory cell MC_{n+1} of the selected memory cell MC_n, the gradient of the channel potential of the selected memory cell string can be reduced. Accordingly, HCI cannot be generated from the selected memory

cell to the upper adjacent memory cell of the selected memory cell in the selected memory cell string. Thus, the ESUM loss can be prevented.

[0066] FIG. 7 is a second schematic diagram of a verify/read operation to verify/read memory cells of a 3D-NAND memory device (e.g., device 100) in accordance with exemplary embodiments of the disclosure. As shown in FIG. 7, the memory cells can be programmed in the forward order, and the verify/read operation can include a short pre-pulse time in the pre-pulse stage. As shown in FIG. 7, the pre-pulse stage can include a first portion T1 and a second portion T2. Compared to the verify/read operation in FIG. 5, the bias voltages applied in the pre-pulse stage can be full developed to (or completely reach) target values in FIG. 7. For example, the bias voltage applied on the WLs ($>n+1$) can be fully developed in the pre-pulse stage. As shown in FIG. 7, the bias voltage applied on the WLs ($>n+1$) can be increased to a target value from the initial voltage in the first portion of the pre-pulse stage. The target value can be 6.8 volts, for example. The bias voltage can then be reduced in the first portion of the pre-verify stage to a lower value (e.g., 3 volts) that is equal to the bias voltage of the verify/read stage. The bias voltage is further maintained in the second portion of the pre-verify stage.

[0067] Still referring to FIG. 7, the pass voltage applied on the $WLn+1$ can be increased from the initial voltage to a target value (e.g., 7.8 volts) in the pre-verify stage, where the target value is equal to the pass voltage of the verify/read stage. The read voltage applied on the $WLn-1$ can be increased from the initial voltage to a target value (e.g., 7.8 volts) in the pre-verify stage, where the target value is equal to the read voltage of the verify/read stage. The gate voltage applied on the unselected TSG can be

increased from the initial voltage to a target value (e.g., 5 volts) in the first portion of the pre-pulse stage. The gate voltage can then be maintained for a duration of time, and then be reduced to a value that is equal to the gate voltage of the verify/read stage in the first portion of the pre-verify stage. The gate voltage can be maintained to be equal to the gate voltage of the verify/read stage in the second portion of the pre-verify stage.

[0068] The bottom bias voltage applied on BSG transistor can be increased from the initial voltage to a target value (e.g., 5 volts) in the first portion of the pre-pulse stage, where the target value is equal to the bottom bias voltage of the verify/read stage. The bottom bias voltage can be maintained through the second portion of the pre-verify stage and the verify stage. Similarly, the top bias voltage applied on the selected TSG transistor can be increased from the initial voltage to a target value (e.g., 5 volts) in the first portion of the pre-pulse stage. The top bias voltage can further be maintained through the second portion of the pre-verify stage and the verify stage. The positive voltage applied on the WLs ($<n-1$) can be increased from the initial voltage in the pre-verify stage to a target value (e.g., 6.8 volts) in the pre-pulse stage, where the target value is equal to the positive voltage applied in the verify/read stage.

[0069] In the verify/read operation in FIG. 7, the bias voltage applied on the WLs ($>n+1$) in the verify/read stage can be lower than the bias voltage applied on the WLs ($>n+1$) in the pre-pulse stage. In an exemplary embodiment of FIG. 7, the bias voltage applied on the WLs ($>n+1$) in the verify/read stage can be 3 volts, and the bias voltage applied on the WLs ($>n+1$) in pre-pulse stage can be 6.8 volts. In some embodiments, each of the memory cells that are positioned above the upper adjacent memory cell MC_{n+1} of the selected memory cell MC_n can receive a bias voltage through the WLs

($>n+1$) in the verify/read stage that is lower than a bias voltage in the pre-pulse stage.

In some embodiments, at least one memory cell of the memory cells that are positioned between the upper adjacent memory cell MC_{n+1} of the selected memory cell MC_n and the TSG transistor can receive a bias voltage through the WLs ($>n+1$) in the verify/read stage that is lower than a bias voltage in the pre-pulse stage. For example, a memory cell that is adjacent to the TSG transistor can receive a bias voltage in the verify/read stage that is lower than a bias voltage in the pre-pulse stage.

[0070] Further, in the verify/read operation in FIG. 7, at least one of the upper adjacent memory cells MC_{n+1} and the lower adjacent memory cell MC_{n-1} of the selected memory cell MC_n can receive a bias voltage that is higher than the bias voltage applied on the unselected TSG transistor in the verify/read stage.

[0071] Compared to the verify/read operation in FIG. 5, the bias voltages applied in the pre-pulse stage of the verify/read operation in FIG. 7 are fully developed to target values. In addition, a lower bias voltage is introduced in the verify/read stage for the memory cells positioned above the upper adjacent memory cell of the selected memory cell MC_n . Accordingly, the gradient of the channel potential of the selected memory cell string can be reduced, and formation of the HCI can be prevented from the selected memory cell to the upper adjacent memory cell of the selected memory cell in the selected memory cell string. Thus, the ESUM loss can be prevented.

[0072] FIG. 8 is a first schematic diagram of a verify/read operation to verify/read memory cells that are programmed in a reverse order in accordance with exemplary embodiments of the disclosure. As shown in FIG. 8, the memory cells can be programmed in the reverse order in that the memory cells are programmed from a top

memory cell adjacent to the TSG transistor to a bottom memory cell (e.g., MC0) adjacent to the BSG transistor. In an exemplary embodiment of FIG. 8, the selected memory cell MC_n and the memory cells above the selected memory cell MC_n are programmed. In addition, the pre-pulse stage of the verify/read operation in FIG. 8 can have a long pre-pulse time.

[0073] As shown in FIG. 8, compared to the verify/read operation shown in FIG. 6 to verify/read the memory cells that are programmed in the forward order, the bias voltage applied on the WLs (<n-1) in the verify/read stage is lower than the bias voltage applied on the WLs (<n-1) in the pre-pulse stage. In some embodiments, each of the memory cells that are positioned between the lower adjacent memory cell MC_{n-1} of the selected memory cell MC_n and the BSG transistor can receive a bias voltage through the WLs (<n-1) in the verify/read stage that is lower than a bias voltage in the pre-pulse stage. In some embodiments, at least one memory cell of the memory cells that are positioned between the lower adjacent memory cell MC_{n-1} of the selected memory cell MC_n and the BSG transistor can receive a bias voltage through the WLs (<n-1) in the verify/read stage that is lower than a bias voltage in the pre-pulse stage. For example, a memory cell that is adjacent to the BSG transistor can receive a bias voltage in the verify/read stage that is lower than a bias voltage in the pre-pulse stage.

[0074] FIG. 9 is a second schematic diagram of a verify/read operation to verify/read memory cells that are programmed in a reverse order in accordance with exemplary embodiments of the disclosure. Compared to the verify/read operation shown in FIG. 7 to verify/read the memory cells that are programmed in the forward order, the bias voltage applied on the WLs (<n-1) in the verify/read stage is lower than the bias voltage

applied on the WLs ($<n-1$) in the pre-pulse stage. In some embodiments, each of the memory cells that are positioned below the lower adjacent memory cell MC $n-1$ of the selected memory cell MC n can receive a bias voltage through the WLs ($<n-1$) in the verify/read stage that is lower than a bias voltage in the pre-pulse stage. In some embodiments, at least one memory cell of the memory cells that are positioned between the lower adjacent memory cell MC $n-1$ of the selected memory cell MC n and the BSG transistor can receive a bias voltage through the WLs ($<n-1$) in the verify/read stage that is lower than a bias voltage in the pre-pulse stage. For example, a memory cell that is adjacent to the BSG transistor can receive a bias voltage in the verify/read stage that is lower than a bias voltage in the pre-pulse stage.

[0075] Similar to the verify/read operations shown in FIGS. 6 and 7, the verify/read operations shown in FIGS. 8 and 9 include a bias voltage that can fully be developed in the pre-pulse stage. In addition, the bias voltage applied on at least one of the memory cells that are not programmed in the pre-pulse stage can be lower than the bias voltage applied in the verify/read stage. Accordingly, the gradient of the channel potential of the selected memory cell string can be reduced, and formation of the HCI can be prevented from the selected memory cell MC n to the lower adjacent memory cell MC $n-1$ of the selected memory cell in the selected memory cell string. Thus, the ESUM loss can be prevented.

[0076] FIG. 10 is a flow chart diagram of a method 1000 for reading a memory device including a first memory cell string and a second memory cell string. The first memory cell string can include a bottom-select-gate (BSG) transistor, memory cells, and a top-select-gate (TSG) transistor that are connected in series. The second memory cell string

can include a BSG transistor, memory cells, and a TSG transistor that are connected in series. As shown in FIG. 10, the method 1000 can start at S1002 and proceed to S1004, where a first verify voltage can be applied on a gate terminal of a selected memory cell of the first memory cell string in a pre-verify stage. The selected memory cell can be programmed and arranged between a first adjacent memory cell and a second adjacent memory cell.

[0077] At S1004, a first bias voltage can be applied on a gate terminal of at least one memory cell of the first memory cell string that is not programmed in the pre-verify stage.

[0078] At S1006, a second verify voltage can be applied on the gate terminal of the selected memory cell of the first memory cell string in a verify stage.

[0079] At S1008 of the method 1000, in the verify stage, a second bias voltage can be applied on the gate terminal of the at least one memory cell of the first memory cell string that is not programmed, where the second bias voltage is smaller than the first bias voltage.

[0080] In some embodiments, the at least one memory cell of the first memory cell string that receives the first bias voltage and the second bias voltage can be positioned between the first adjacent memory cell of the selected memory cell and the TSG transistor of the first memory cell string.

[0081] In some embodiments, the at least one memory cell of the first memory cell string that receives the first bias voltage and the second bias voltage can be positioned between the second adjacent memory cell of the selected memory cell and the BSG transistor of the first memory cell string.

[0082] In the method 1000, in the pre-verify stage, a first gate voltage can be applied on a gate terminal of the TSG transistor of the second memory cell string. A first pass voltage can be applied on a gate terminal of the first adjacent memory cell in the selected memory cell of the first memory cell string. A first read voltage can be applied on a gate terminal of the second adjacent memory cell of the selected memory cell in the first memory cell string. Further, in the verify stage, a second gate voltage can be applied on the gate terminal of the TSG transistor of the second memory cell string. A second pass voltage can be applied on the gate terminal of the first adjacent memory cell of the selected memory cell in the first memory cell string. A second read voltage can be applied on the gate terminal of the second adjacent memory cell in the selected memory cell of the first memory cell string. Further, at least one of the second pass voltage and the second read voltage can be larger than the second gate voltage.

[0083] FIG. 11 is a simplified block diagram of a memory device 1001 according to an embodiment of the disclosure, and on which various embodiments of the disclosure can be implemented. The memory device 1001 can include a memory array 1004 arranged in rows and columns. The memory array 1004 can include memory cells (e.g., MCs 304 in FIG. 3) that are formed based on a plurality of channel structures (e.g., channel structures 18 in FIG. 2). The channel structures can be formed in a stack of alternating word line layers (e.g., 12 in FIG. 2) and insulating layers (e.g., 14 in FIG. 2). A row decode circuit 1008 and a column decode circuit 1010 are provided to decode address signals provided to the memory device 1001. Address signals are received and decoded to access the memory array 1004. Memory device 1001 can also include an input/output (I/O) control circuit 1012 to manage input of commands, addresses and data to the

memory device 1001 as well as output of data and status information from the memory device 1001. An address register 1014 is coupled between the I/O control circuit 1012 and the row decode circuit 1008 and column decode circuit 1010 to latch the address signals prior to decoding. A command register 1024 is coupled between the I/O control circuit 1012 and a control logic 1016 to latch incoming commands.

[0084] The control logic 1016 can control access to the memory array 1004 in response to the commands and generate status information for the external processor 1030. The control logic 1016 is coupled to the row decode circuit 1008 and the column decode circuit 1010 to control the row decode circuit 1008 and column decode circuit 1010 in response to the addresses. For example, bias voltages can be applied to selected memory cells by the control logic 1016 through the row decode circuit 1008 and column decode circuit 1010 to operate the selected memory cells, such as reading, writing or erasing the memory cells. The control logic 1016 can be also coupled to sense amplifier and latch circuitry 1018 to control the sense amplifier and latch circuitry 1018 in response to the commands and generate status information for the external processor 1030. The sense amplifier and latch circuitry 1018 can be coupled to the memory array 1004 and can latch data, either incoming or outgoing, in the form of analog voltage levels. The sense amplifier and latch circuitry 1018 can be configured to read signals of the memory cells when the memory cells are operated.

[0085] Still referring to FIG. 11, a status register 1022 can be coupled between the I/O control circuit 1012 and the control logic 1016 to latch the status information for output to the external processor 1030. The memory device 1001 receives control signals at control logic 1016 over a control link 1032. The control signals may include a chip

enable CE#, a command latch enable CLE, an address latch enable ALE, and a write enable WE #. The memory device 1001 may receive commands in the form of command signals, addresses in the form of address signals, and data in the form of data signals from an external processor over a multiplexed input/output (I/O) bus 1034 and output data to the external processor over the I/O bus 1034.

[0086] The various embodiments described herein offer several advantages over methods in related examples to verify/read memory cells of a 3D-NAND memory device that are programmed. In related examples, HCI can be generated between the selected memory cell and one of the adjacent memory cells of the selected memory cell, and result in the ESUM loss. In the present disclosure, hot-carrier injection (HCI)-induced edge summation (ESUM) loss can be prevented, and power consumption during verifying/reading the memory cells of the 3D-NAND memory device can be reduced.

[0087] The foregoing outlines features of several embodiments so that those skilled in the art may better understand the aspects of the present disclosure. Those skilled in the art should appreciate that they may readily use the present disclosure as a basis for designing or modifying other processes and structures for carrying out the same purposes and/or achieving the same advantages of the embodiments introduced herein. Those skilled in the art should also realize that such equivalent constructions do not depart from the spirit and scope of the present disclosure, and that they may make various changes, substitutions, and alterations herein without departing from the spirit and scope of the present disclosure.

WHAT IS CLAIMED IS:

1. A method for reading a memory device including a first memory cell string and a second memory cell string, the first memory cell string including a bottom-select-gate (BSG) transistor, memory cells, and a top-select-gate (TSG) transistor that are connected in series, the second memory cells string including a BSG transistor, memory cells, and a TSG transistor that are connected in series, the method comprising:

applying, in a pre-verify stage, a first verify voltage on a gate terminal of a selected memory cell of the first memory cell string, the selected memory cell being programmed and arranged between a first adjacent memory cell and a second adjacent memory cell;

applying, in the pre-verify stage, a first bias voltage on a gate terminal of at least one memory cell of the first memory cell string that is positioned between the first adjacent memory cell of the selected memory cell and the TSG transistor of the first memory cell string;

applying, in a verify stage, a second verify voltage on the gate terminal of the selected memory cell of the first memory cell string; and

applying, in the verify stage, a second bias voltage on the gate terminal of the at least one memory cell of the first memory cell string that is positioned between the first adjacent memory cell of the selected memory cell and the TSG transistor of the first memory cell string, wherein the second bias voltage is smaller than the first bias voltage.

2. The method of claim 1, wherein the second bias voltage is from 20% to 30% smaller than the first bias voltage.

3. The method of claim 1, further comprising:

in the pre-verify stage,

applying a first gate voltage on a gate terminal of the TSG transistor of the second memory cell string,

applying a first pass voltage on a gate terminal of the first adjacent memory cell of the selected memory cell in the first memory cell string, and

applying a first read voltage on a gate terminal of the second adjacent memory cell of the selected memory cell in the first memory cell string; and

in the verify stage,

applying a second gate voltage on the gate terminal of the TSG transistor of the second memory cell string,

applying a second pass voltage on the gate terminal of the first adjacent memory cell of the selected memory cell in the first memory cell string, and

applying a second read voltage on the gate terminal of the second adjacent memory cell of the selected memory cell in the first memory cell string, wherein

at least one of the second pass voltage and the second read voltage is larger than the second gate voltage.

4. The method of claim 3, further comprising:

applying a bottom bias voltage on a gate terminal of the BSG transistor of the first memory cell string in the pre-verify stage and the verify stage;

applying a top bias voltage on a gate terminal of the TSG transistor of the first memory cell string in the pre-verify stage and the verify stage; and

applying a positive voltage on gate terminals of any memory cells that are positioned between the second adjacent memory cell of the selected memory cell and the BSG transistor of the first memory cell string in the pre-verify stage and the verify stage.

5. The method of claim 1, wherein the first verify voltage is smaller than the second verify voltage.

6. The method of claim 4, wherein:

the first bias voltage is increased from an initial voltage, and then reduced to the second bias voltage in a first portion of the pre-verify stage, the first bias voltage being equal to the second bias voltage in a second portion of the pre-verify stage,

the first pass voltage is increased from the initial voltage to the second pass voltage in the pre-verify stage,

the first read voltage is increased from the initial voltage to the second read voltage in the pre-verify stage, and

the first gate voltage is increased from the initial voltage to a voltage that is maintained for a duration of time, and then the first gate voltage is reduced to the

second gate voltage in the first portion of the pre-verify stage, the first gate voltage being equal to the second gate voltage in the second portion of the pre-verify stage.

7. The method of claim 6, wherein:

the bottom bias voltage is increased from the initial voltage to a voltage that is maintained through the second portion of the pre-verify stage and the verify stage,

the top bias voltage is increased from the initial voltage to a voltage that is maintained through the second portion of the pre-verify stage and the verify stage, and

the positive voltage is increased from the initial voltage in the pre-verify stage.

8. A method for reading a memory device including a first memory cell string and a second memory cell string, the first memory cell string including a bottom-select-gate (BSG) transistor, memory cells, and a top-select-gate (TSG) transistor that are connected in series, the second memory cells string including a BSG transistor, memory cells, and a TSG transistor that are connected in series, the method comprising:

applying, in a pre-verify stage, a first verify voltage on a gate terminal of a selected memory cell of the first memory cell string, the selected memory cell being programmed and arranged between a first adjacent memory cell and a second adjacent memory cell;

applying, in the pre-verify stage, a first bias voltage on a gate terminal of at least one memory cell of the first memory cell string that is positioned between the second adjacent memory cell of the selected memory cell and the BSG transistor of the first memory cell string;

applying, in a verify stage, a second verify voltage on the gate terminal of the selected memory cell of the first memory cell string; and

applying, in the verify stage, a second bias voltage on the gate terminal of the at least one memory cell of the first memory cell string that is positioned between the second adjacent memory cell of the selected memory cell and the BSG transistor of the first memory cell string, wherein the second bias voltage is smaller than the first bias voltage.

9. The method of claim 8, wherein the second bias voltage is from 20% to 30% smaller than the first bias voltage.

10. The method of claim 8, further comprising:

in the pre-verify stage,

applying a first gate voltage on a gate terminal of the TSG transistor of the second memory cell string,

applying a first pass voltage on a gate terminal of the first adjacent memory cell of the selected memory cell in the first memory cell string, and

applying a first read voltage on a gate terminal of the second adjacent memory cell of the selected memory cell in the first memory cell string; and

in the verify stage,

applying a second gate voltage on the gate terminal of the TSG transistor of the second memory cell string,

applying a second pass voltage on the gate terminal of the first adjacent memory cell of the selected memory cell in the first memory cell string, and

applying a second read voltage on the gate terminal of the second adjacent memory cell of the selected memory cell in the first memory cell string, wherein

at least one of the second pass voltage and the second read voltage is larger than the second gate voltage.

11. The method of claim 10, further comprising:

applying a bottom bias voltage on a gate terminal of the BSG transistor of the first memory cell string in the pre-verify stage and the verify stage;

applying a top bias voltage on a gate terminal of the TSG transistor of the first memory cell string in the pre-verify stage and the verify stage; and

applying a positive voltage on gate terminals of any memory cells that are positioned between the first adjacent memory cell of the selected memory cell and the TSG transistor of the first memory cell string in the pre-verify stage and the verify stage.

12. The method of claim 8, wherein the first verify voltage is smaller than the second verify voltage.

13. The method of claim 11, wherein:

the first bias voltage is increased from an initial voltage, and then reduced to the second bias voltage in a first portion of the pre-verify stage, the first bias voltage being equal to the second bias voltage in a second portion of the pre-verify stage,

the first pass voltage is increased from the initial voltage to the second pass voltage in the pre-verify stage,

the first read voltage is increased from the initial voltage to the second read voltage in the pre-verify stage, and

the first gate voltage is increased from the initial voltage to a voltage that is maintained for a duration of time, and then the first gate voltage is reduced to the second gate voltage in the first portion of the pre-verify stage, the first gate voltage being equal to the second gate voltage in the second portion of the pre-verify stage.

14. The method of claim 13, wherein:

the bottom bias voltage is increased from the initial voltage to a voltage that is maintained through the second portion of the pre-verify stage and the verify stage,

the top bias voltage is increased from the initial voltage to a voltage that is maintained through the second portion of the pre-verify stage and the verify stage, and

the positive voltage is increased from the initial voltage in the pre-verify stage.

15. An apparatus for reading a memory device including a first memory cell string and a second memory cell string, the first memory cell string including a bottom-select-gate (BSG) transistor, memory cells, and a top-select-gate (TSG) transistor that are connected in series, the second memory cells string including a BSG transistor,

memory cells, and a TSG transistor that are connected in series, the apparatus comprising:

processing circuitry configured to:

apply, in a pre-verify stage, a first verify voltage on a gate terminal of a selected memory cell of the first memory cell string, the selected memory cell being programmed and arranged between a first adjacent memory cell and a second adjacent memory cell;

apply, in the pre-verify stage, a first bias voltage on a gate terminal of at least one memory cell of the first memory cell string that is not programmed;

apply, in a verify stage, a second verify voltage on the gate terminal of the selected memory cell of the first memory cell string; and

apply, in the verify stage, a second bias voltage on the gate terminal of the at least one memory cell of the first memory cell string that is not programmed, wherein the second bias voltage is smaller than the first bias voltage.

16. The apparatus of claim 15, wherein the at least one memory cell of the first memory cell string that receives the first bias voltage and the second bias voltage is positioned between the first adjacent memory cell of the selected memory cell and the TSG transistor of the first memory cell string.

17. The apparatus of claim 15, wherein the at least one memory cell of the first memory cell string that receives the first bias voltage and the second bias voltage is

positioned between the second adjacent memory cell of the selected memory cell and the BSG transistor of the first memory cell string.

18. The apparatus of claim 15, wherein the processing circuitry is further configured to:

in the pre-verify stage,

apply a first gate voltage on a gate terminal of the TSG transistor of the second memory cell string,

apply a first pass voltage on a gate terminal of the first adjacent memory cell of the selected memory cell in the first memory cell string, and

apply a first read voltage on a gate terminal of the second adjacent memory cell of the selected memory cell in the first memory cell string; and

in the verify stage,

apply a second gate voltage on the gate terminal of the TSG transistor of the second memory cell string,

apply a second pass voltage on the gate terminal of the first adjacent memory cell of the selected memory cell in the first memory cell string, and

apply a second read voltage on the gate terminal of the second adjacent memory cell of the selected memory cell of the first memory cell string, wherein

at least one of the second pass voltage and the second read voltage is larger than the second gate voltage.

19. The apparatus of claim 16, wherein the processing circuitry is further configured to:

apply a bottom bias voltage on a gate terminal of the BSG transistor of the first memory cell string in the pre-verify stage and the verify stage;

apply a top bias voltage on a gate terminal of the TSG transistor of the first memory cell string in the pre-verify stage and the verify stage; and

apply a positive voltage on gate terminals of any memory cells that are positioned between the second adjacent memory cell of the selected memory cell and the BSG transistor of the first memory cell string in the pre-verify stage and the verify stage.

20. The apparatus of claim 17, wherein the processing circuitry is further configured to:

apply a bottom bias voltage on a gate terminal of the BSG transistor of the first memory cell string in the pre-verify stage and the verify stage;

apply a top bias voltage on a gate terminal of the TSG transistor of the first memory cell string in the pre-verify stage and the verify stage; and

apply a positive voltage on gate terminals of any memory cells that are positioned between the first adjacent memory cell of the selected memory cell and the TSG transistor of the first memory cell string in the pre-verify stage and the verify stage.

ABSTRACT

In a method for reading a memory device including a first memory cell string, in a pre-verify stage, a first verify voltage is applied on a gate terminal of a selected memory cell of the first memory cell string, where the selected memory cell is programmed and arranged between a first adjacent memory cell and a second adjacent memory cell. A first bias voltage is applied on a gate terminal of at least one memory cell of the first memory cell string that is not programmed. In a verify stage, a second verify voltage is applied on the gate terminal of the selected memory cell of the first memory cell string. A second bias voltage is applied on the gate terminal of the at least one memory cell of the first memory cell string that is not programmed, where the second bias voltage is smaller than the first bias voltage.

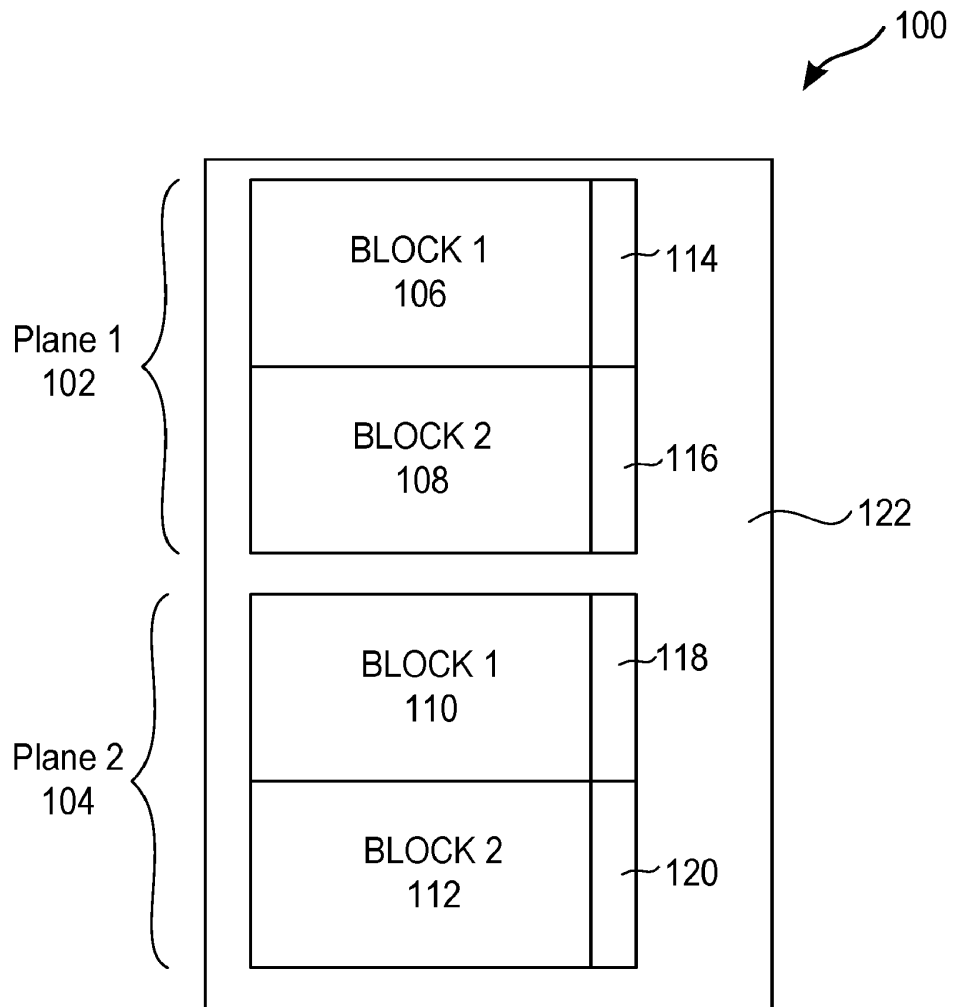


FIG. 1

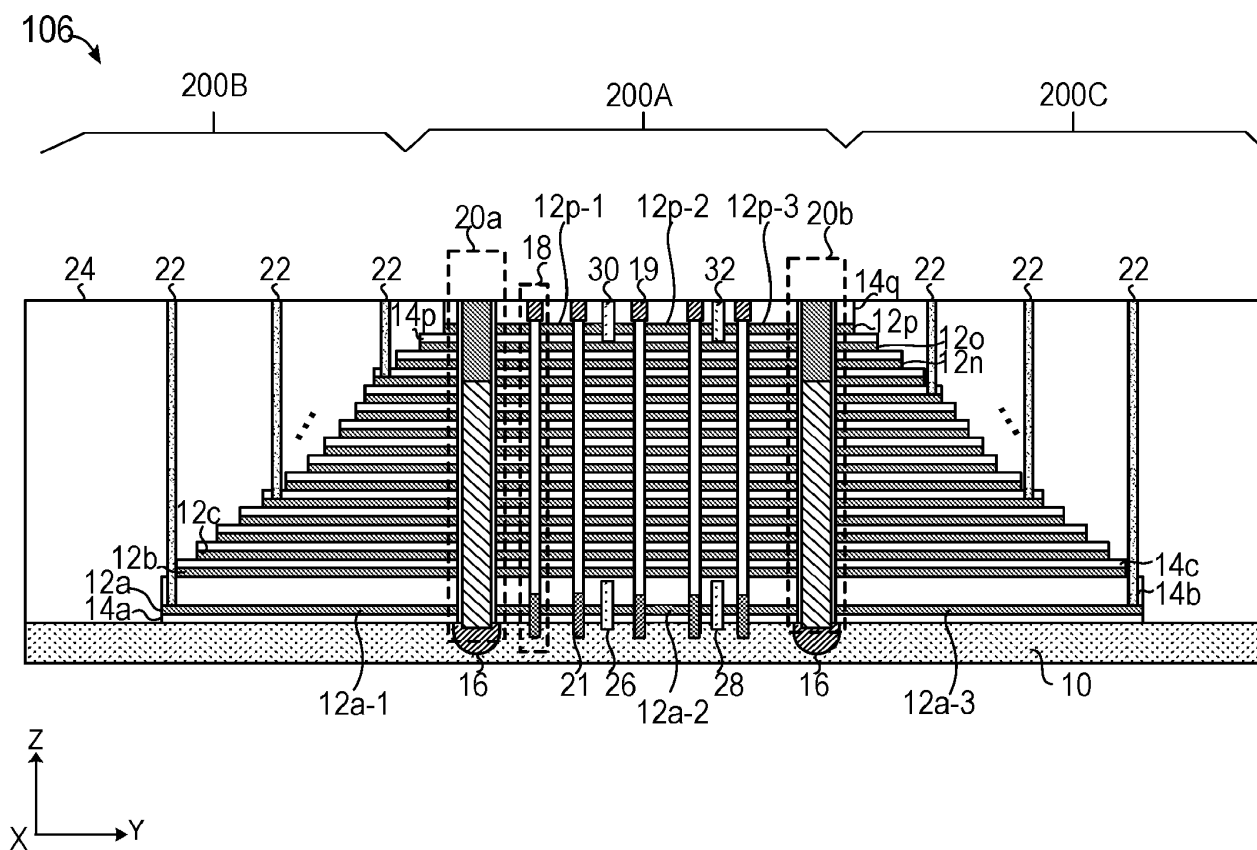


FIG. 2

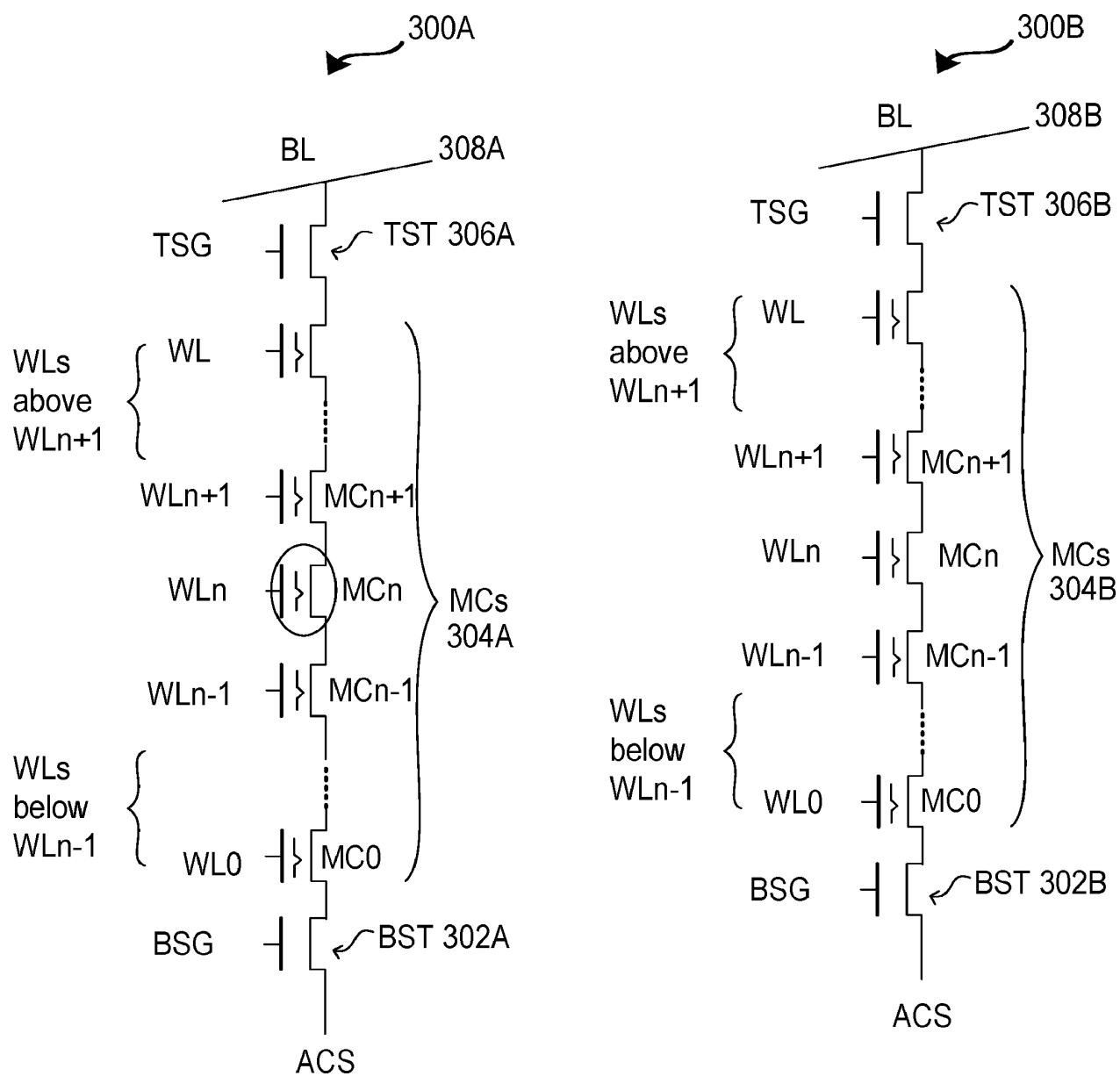


FIG. 3

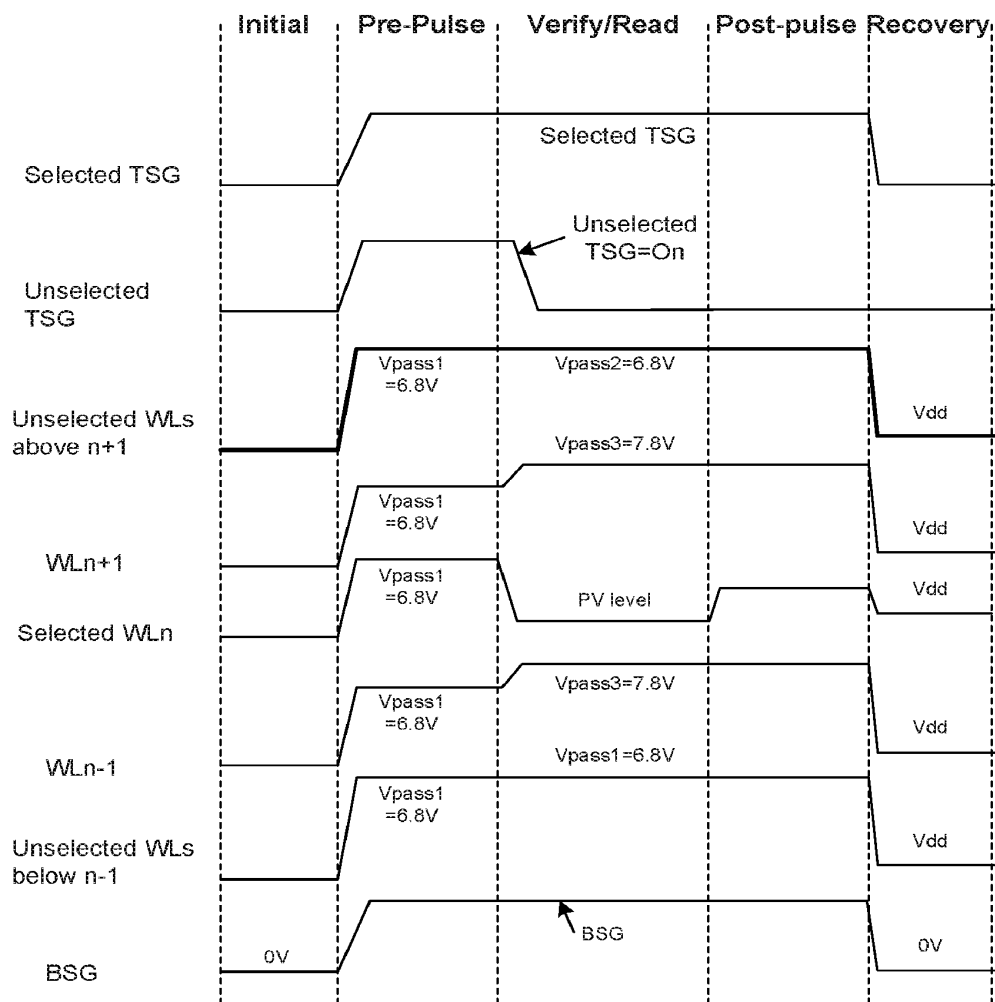


FIG. 4

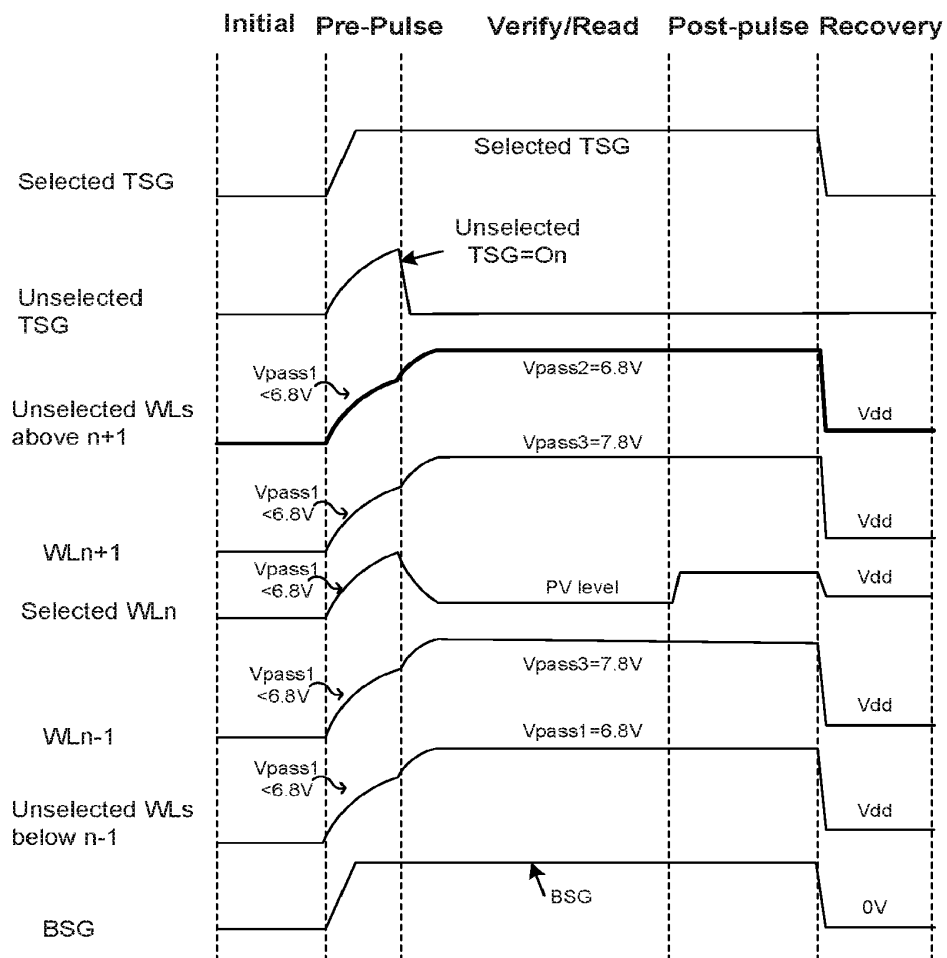


FIG. 5

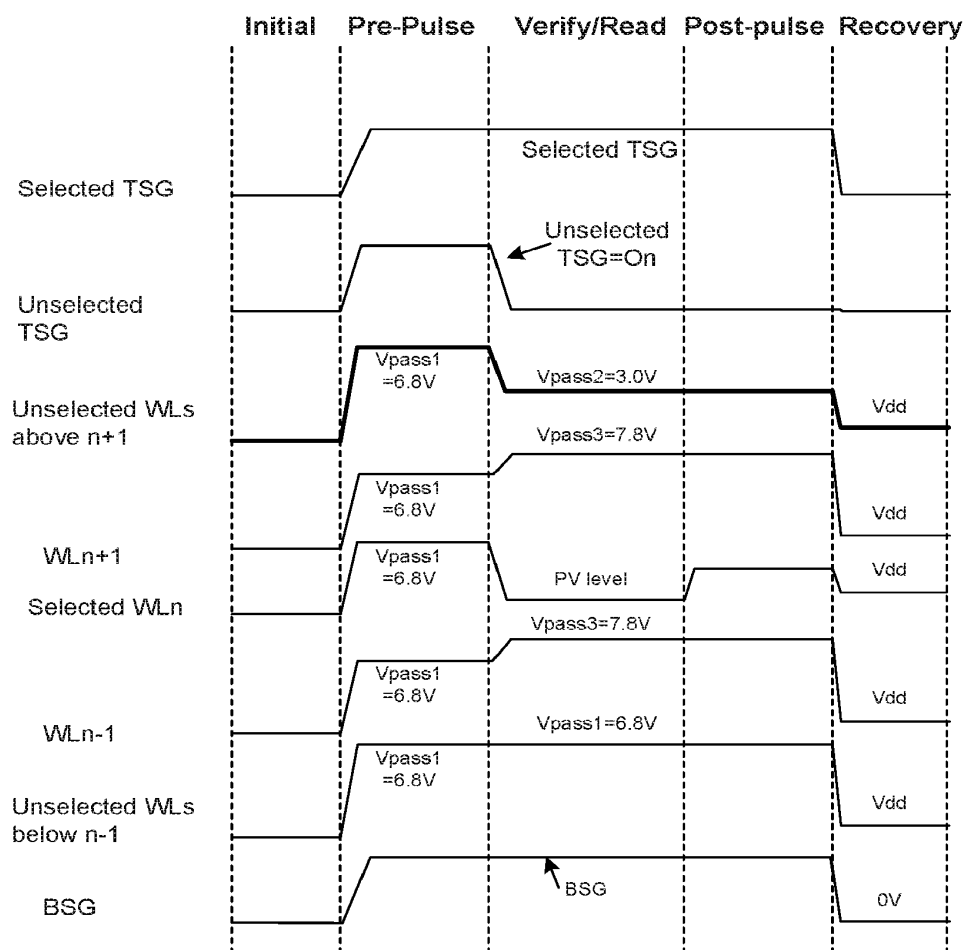


FIG. 6

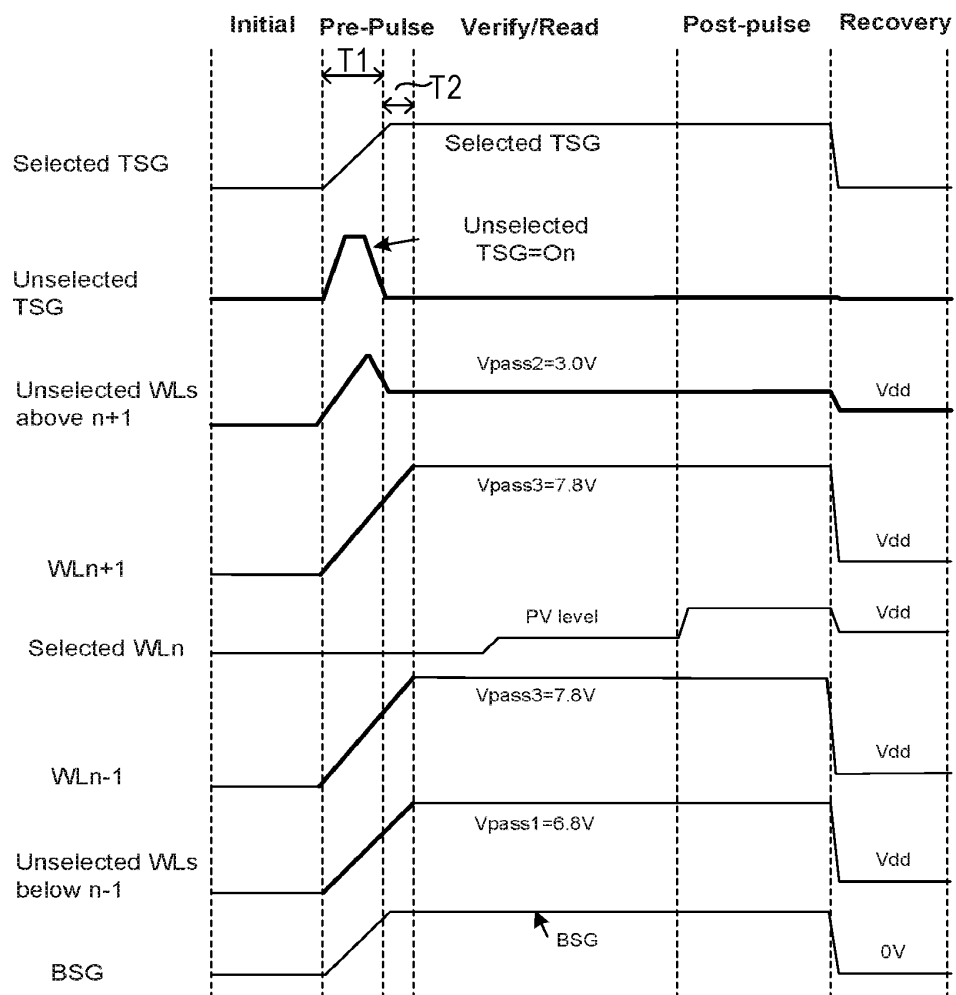


FIG. 7

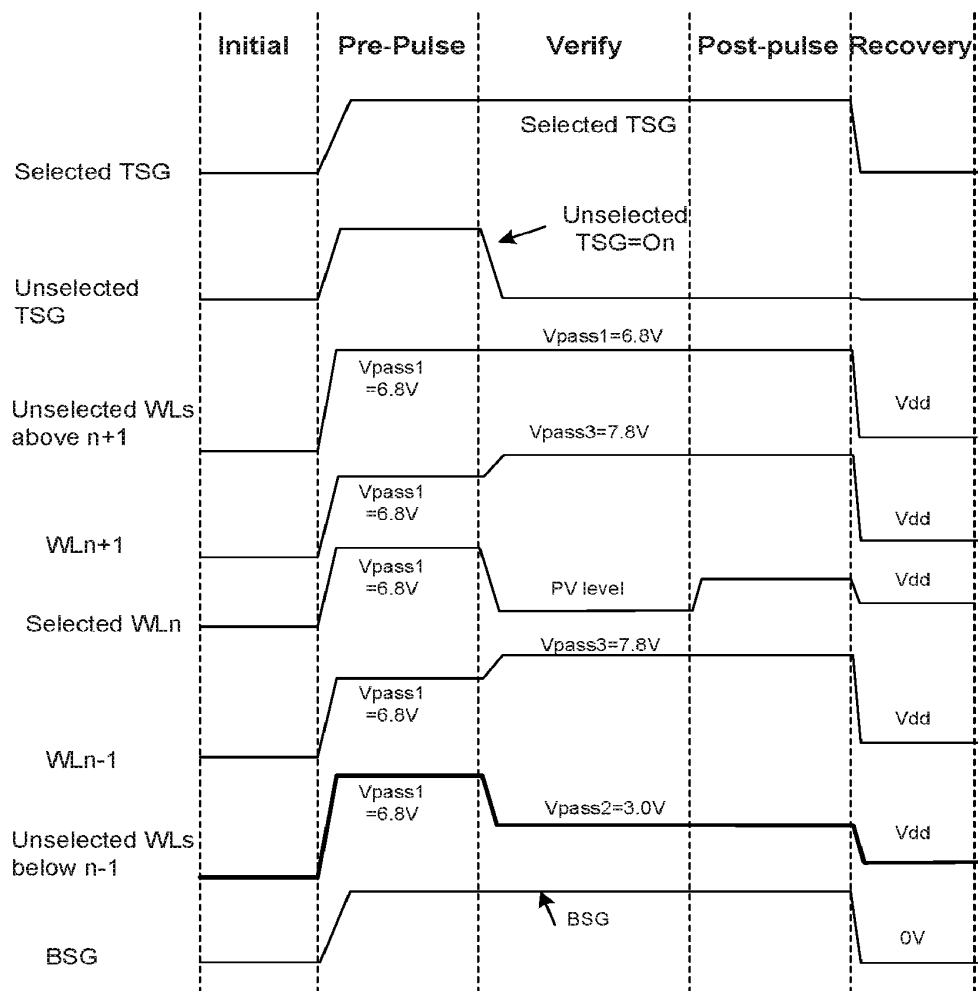


FIG. 8

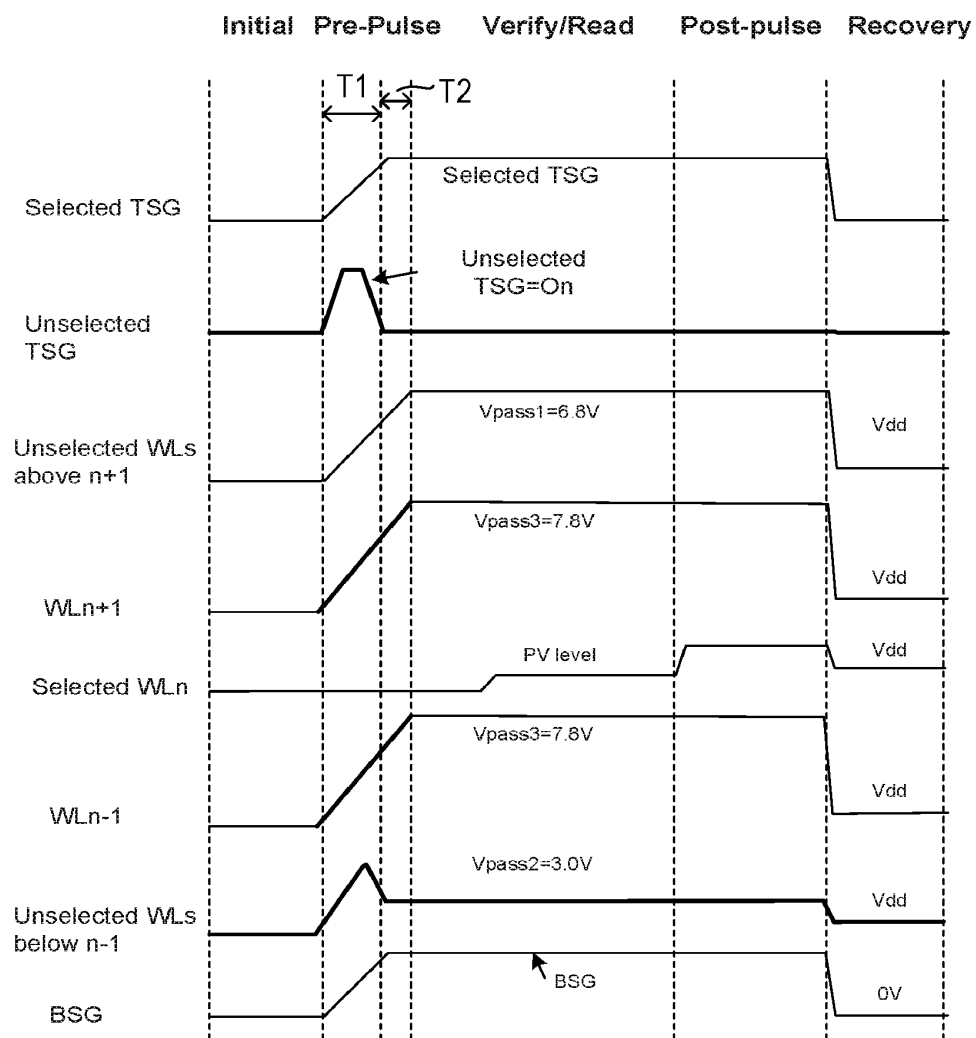


FIG. 9

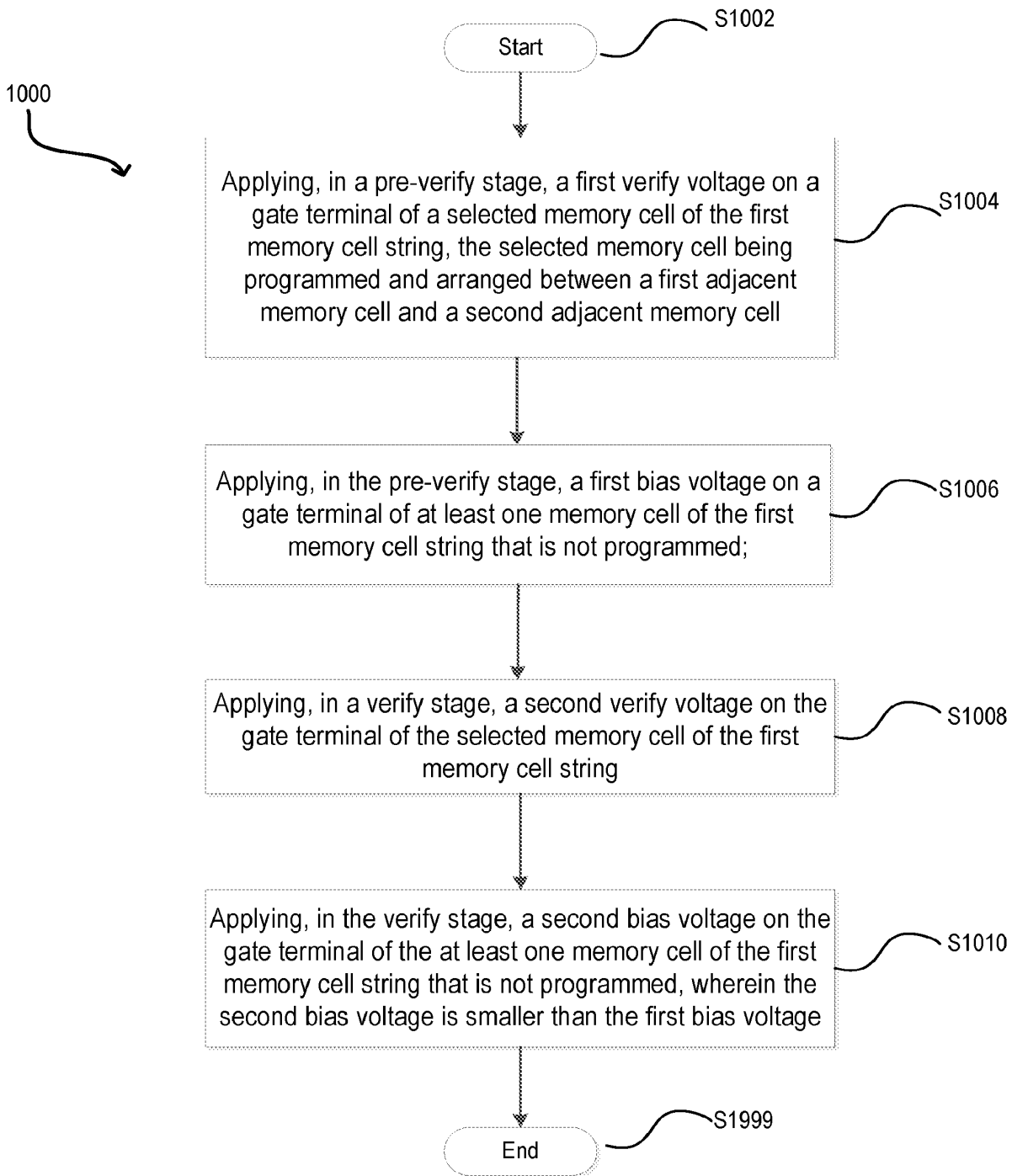


FIG. 10

1001

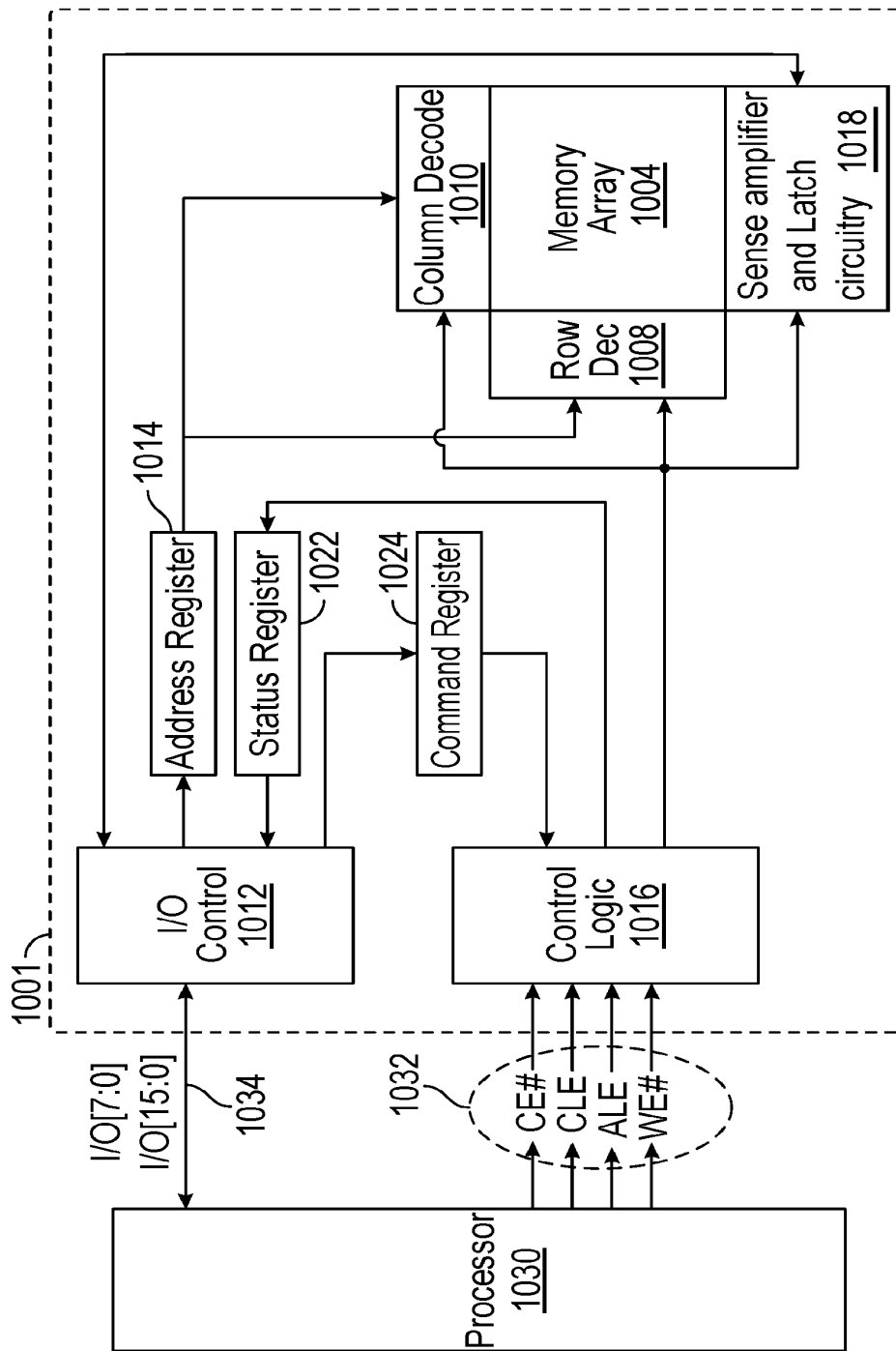


FIG. 11

COMBINED DECLARATION AND ASSIGNMENT

DECLARATION

As the below named inventors, I hereby declare that:

This declaration is directed to:

- ☒ The attached application, or
- ☐ United States application or PCT international application number _____
filed on _____

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. § 1001 by fine or imprisonment of not more than five (5) years, or both.

ASSIGNMENT

In consideration of the sum of One Dollar (\$1.00) or equivalent and other good and valuable consideration paid to each of the below named inventors, each of the below named inventors, hereby sell and assign to **Yangtze Memory Technologies Co., Ltd.**, a corporation formed under the laws of China, whose mailing address is No.88 Weilai 3rd Road, East Lake High-tech Development Zone, Wuhan, Hubei, China (hereafter referred to as the Assignee), his/her entire right, title and interest, including the right to sue for past infringement and to collect for all past, present and future damages, for the United States of America (as defined in 35 U.S.C. § 100) and throughout the world,

(a) in the invention(s) known as **ARCHITECTURE AND METHOD FOR NAND MEMORY OPERATION** for which application(s) for patent in the United States of America is identified above, in any and all applications thereon, in any and all Letters Patent(s) therefor, and

(b) in any and all applications that claim the benefit of the patent application identified above in part (a), including non-provisional applications, continuing (continuation, divisional, or continuation-in-part) applications, reissues, extensions, renewals and reexaminations of the patent application or Letters Patent therefor listed above in part (a), to the full extent of the term or terms for which Letters Patents issue, and

(c) in any and all inventions described in the patent application identified above in part (a), and in any and all forms of intellectual and industrial property protection derivable from such patent application, and that are derivable from any and all continuing applications, reissues, extensions, renewals and reexaminations of such patent application, including, without limitation, patents, applications, utility models, inventor's certificates, and designs together with the right to file applications therefor; and including the right to claim the same priority rights from any previously filed applications under the International Agreement for the Protection of Industrial Property, or any other international agreement, or the domestic laws of the country in which any such application is filed, as may be applicable;

all such rights, title and interest to be held and enjoyed by the above-named Assignee, its successors, legal representatives and assigns to the same extent as all such rights, title and interest would have been held and enjoyed by the Assignor had this assignment and sale not been made.

The below named inventors agree to execute all papers necessary in connection with the application(s) and any non-provisional, continuing (continuation, divisional, or continuation-in-part), reissue, reexamination or corresponding application(s) thereof and also to execute separate assignments in connection with such application(s) as the Assignee may deem necessary or expedient.

The below named inventors agree to execute all papers necessary in connection with any patent enforcement action (judicial or otherwise) related to the application(s) or any non-provisional, continuing (continuation, divisional, or continuation-in-part), reissue or reexamination application(s) thereof and to cooperate with the Assignee in every way possible in obtaining evidence and going forward with such patent enforcement action.

The below named inventors hereby represent that he/she has full right to convey the entire interest herein assigned, and that he/she has not executed, and will not execute, any agreement in conflict therewith.

The below named inventors hereby represent that he/she understands that the patent practitioners associated with **CUSTOMER NUMBER 22850** are the legal representatives of, and attorneys for, the assignee, and are NOT the legal representatives of, and attorneys for, the inventors.

IN WITNESS WHEREOF, executed by the below named inventors on the date opposite his/her name.

LEGAL NAME OF INVENTOR

Inventor: Changhyun LEE Date: Feb. 16th, 2021

Signature of Inventor: 

Inventor: Xiangnan ZHAO Date: _____

Signature of Inventor: _____

Inventor: Haibo LI Date: _____

Signature of Inventor: _____

Inventor: _____ Date: _____

Signature of Inventor: _____

Inventor: _____ Date: _____

Signature of Inventor: _____

IN WITNESS WHEREOF, executed by the below named inventors on the date opposite his/her name.

LEGAL NAME OF INVENTOR

Inventor: Changhyun LEE Date: _____

Signature of Inventor: _____

Inventor: Xiangnan ZHAO Date: 2021/2/19

Signature of Inventor: Xiangnan Zhao

Inventor: Haibo LI Date: _____

Signature of Inventor: _____

Inventor: _____ Date: _____

Signature of Inventor: _____

Inventor: _____ Date: _____

Signature of Inventor: _____

IN WITNESS WHEREOF, executed by the below named inventors on the date opposite his/her name.

LEGAL NAME OF INVENTOR

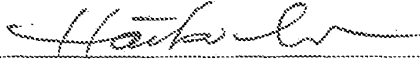
Inventor: Changhyun LEE Date: _____

Signature of Inventor: _____

Inventor: Xiangnan ZHAO Date: _____

Signature of Inventor: _____

Inventor: Haibo LI Date: 02/16/2021

Signature of Inventor: 

Inventor: _____ Date: _____

Signature of Inventor: _____

Inventor: _____ Date: _____

Signature of Inventor: _____

**TRANSMITTAL FOR POWER OF ATTORNEY TO ONE OR MORE
REGISTERED PRACTITIONERS**

NOTE: This form is to be submitted with the Power of Attorney by Applicant form to identify the application to which the Power of Attorney is directed, in accordance with 37 CFR 1.5. If the Power of Attorney by Applicant form is not accompanied by this transmittal form or an equivalent, the Power of Attorney will not be recognized in the application.

Application Number	NEW APPLICATION		
Patent Number			
Filing Date	HEREWITH		
Issue Date			
First Named Inventor	Changhyun LEE		
Title	ARCHITECTURE AND METHOD FOR NAND MEMORY OPERATION		
Art Unit			
Examiner Name			
Attorney Docket Number	533055US		
SIGNATURE of Applicant or Patent Practitioner			
Signature	/ Leonidas Boutsikaris/	Date	03/04/2021
Name	Leonidas Boutsikaris, Ph.D.	Telephone	703-413-3000
Registration Number	Registration No.: 61,377		
NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4(d) for signature requirements and certifications.			
■ *Total of <u>1</u> forms are submitted.			

POWER OF ATTORNEY BY APPLICANT

I hereby revoke all previous powers of attorney given in the application identified in either the attached transmittal letter or the boxes below.

Application Number	Filing Date

(Note: The boxes above may be left blank if information is provided on form PTO/AIA/82A.)

☒ I hereby appoint the Patent Practitioner(s) associated with the following Customer Number as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above:

OR

☐ I hereby appoint Practitioner(s) named in the attached list (form PTO/AIA/82C) as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the patent application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above. (Note: Complete form PTO/AIA/82C.)

22850

Please recognize or change the correspondence address for the application identified in the attached transmittal letter or the boxes above to:

☒ The address associated with the above-mentioned Customer Number

OR

☐ The address associated with Customer Number

OR

☐ Firm or Individual Name

Address

City

State

Zip

Country

Telephone

Email

I am the Applicant (if the Applicant is a juristic entity, list the Applicant name in the box):

Yangtze Memory Technologies Co., Ltd.

- ☐ Inventor or Joint Inventor (title not required below)
- ☐ Legal Representative of a Deceased or Legally Incapacitated Inventor (title not required below)
- ☒ Assignee or Person to Whom the Inventor is Under an Obligation to Assign (provide signer's title if applicant is a juristic entity)
- ☐ Person Who Otherwise Shows Sufficient Proprietary Interest (e.g., a petition under 37 CFR 1.40(b)(2) was granted in the application or is concurrently being filed with this document) (provide signer's title if applicant is a juristic entity)

SIGNATURE of Applicant for Patent

The undersigned (whose title is supplied below) is authorized to act on behalf of the applicant (e.g., where the applicant is a juristic entity).

Signature

Date (Optional)

Name

SIMON SHI-NING YANG

Title

CEO

NOTE: Signature - This form must be signed by the applicant in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. If more than one applicant, use multiple forms.

☐ Total of forms are submitted.

This collection of information is required by 37 CFR 1.131, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 38 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 5 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1480, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1480, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	533055US
		Application Number	
Title of Invention	ARCHITECTURE AND METHOD FOR NAND MEMORY OPERATION		
The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76. This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.			

Secrecy Order 37 CFR 5.2:

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Inventor Information:

Inventor 1		Remove	
Legal Name			
Prefix	Given Name	Middle Name	Family Name
	Changhyun		LEE
Residence Information (Select One) US Residency • Non US Residency Active US Military Service			
City	Wuhan	Country of Residence ⁱ	CN
Mailing Address of Inventor:			
Address 1	No.88, Weilai Third Road		
Address 2	East Lake High-tech Development Zone		
City	Wuhan, Hubei	State/Province	
Postal Code	430223	Country ⁱ	CN
Inventor 2		Remove	
Legal Name			
Prefix	Given Name	Middle Name	Family Name
	Xiangnan		ZHAO
Residence Information (Select One) US Residency • Non US Residency Active US Military Service			
City	Wuhan	Country of Residence ⁱ	CN
Mailing Address of Inventor:			
Address 1	No.88, Weilai Third Road		
Address 2	East Lake High-tech Development Zone		
City	Wuhan, Hubei	State/Province	
Postal Code	430223	Country ⁱ	CN
Inventor 3		Remove	
Legal Name			

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	533055US
		Application Number	
Title of Invention	ARCHITECTURE AND METHOD FOR NAND MEMORY OPERATION		

Prefix	Given Name	Middle Name	Family Name	Suffix
	Haibo		LI	
Residence Information (Select One) US Residency ☒ Non US Residency Active US Military Service				
City	Wuhan	Country of Residence ⁱ	CN	
Mailing Address of Inventor:				
Address 1	No.88, Weilai Third Road			
Address 2	East Lake High-tech Development Zone			
City	Wuhan, Hubei	State/Province		
Postal Code	430223	Country ⁱ	CN	
All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the Add button. Add				

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below. For further information see 37 CFR 1.33(a).			
☐ An Address is being provided for the correspondence information of this application.			
Customer Number	22850		
Email Address	Oblonpat@oblon.com	Add Email	Remove Email

Application Information:

Title of the Invention	ARCHITECTURE AND METHOD FOR NAND MEMORY OPERATION		
Attorney Docket Number	533055US	Small Entity Status Claimed	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	11	Suggested Figure for Publication (if any)	

Filing By Reference:

Only complete this section when filing an application by reference under 35 U.S.C. 111(c) and 37 CFR 1.57(a). Do not complete this section if application papers including a specification and any drawings are being filed. Any domestic benefit or foreign priority information must be provided in the appropriate section(s) below (i.e., "Domestic Benefit/National Stage Information" and "Foreign Priority Information").

For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	533055US
		Application Number	
Title of Invention	ARCHITECTURE AND METHOD FOR NAND MEMORY OPERATION		

Publication Information:
☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

Request Not to Publish. I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32). Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.

Please Select One:	☒ Customer Number	☐ US Patent Practitioner	☐ Limited Recognition (37 CFR 11.9)
Customer Number	22850		

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, 365(c), or 386(c) or indicate National Stage entry from a PCT application. Providing benefit claim information in the Application Data Sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.

When referring to the current application, please leave the "Application Number" field blank.

Prior Application Status	Pending	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
	Continuation of	PCT/CN2020/136482	2020-12-15
Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the Add button.			Add

Foreign Priority Information:

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55. When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX)¹ the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(i)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	533055US
		Application Number	
Title of Invention	ARCHITECTURE AND METHOD FOR NAND MEMORY OPERATION		

Application Number	Country ⁱ	Filing Date (YYYY-MM-DD)	Remove Access Code ^j (if applicable)
Additional Foreign Priority Data may be generated within this form by selecting the Add button.			Add

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

☐ This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.

NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	533055US
		Application Number	
Title of Invention	ARCHITECTURE AND METHOD FOR NAND MEMORY OPERATION		

Authorization or Opt-Out of Authorization to Permit Access:

When this Application Data Sheet is properly signed and filed with the application, applicant has provided written authority to permit a participating foreign intellectual property (IP) office access to the instant application-as-filed (see paragraph A in subsection 1 below) and the European Patent Office (EPO) access to any search results from the instant application (see paragraph B in subsection 1 below).

Should applicant choose not to provide an authorization identified in subsection 1 below, applicant **must opt-out** of the authorization by checking the corresponding box A or B or both in subsection 2 below.

NOTE: This section of the Application Data Sheet is **ONLY** reviewed and processed with the **INITIAL** filing of an application. After the initial filing of an application, an Application Data Sheet cannot be used to provide or rescind authorization for access by a foreign IP office(s). Instead, Form PTO/SB/39 or PTO/SB/69 must be used as appropriate.

1. Authorization to Permit Access by a Foreign Intellectual Property Office(s)

A. Priority Document Exchange (PDX) - Unless box A in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the State Intellectual Property Office of the People's Republic of China (SIPO), the World Intellectual Property Organization (WIPO), and any other foreign intellectual property office participating with the USPTO in a bilateral or multilateral priority document exchange agreement in which a foreign application claiming priority to the instant patent application is filed, access to: (1) the instant patent application-as-filed and its related bibliographic data, (2) any foreign or domestic application to which priority or benefit is claimed by the instant application and its related bibliographic data, and (3) the date of filing of this Authorization. See 37 CFR 1.14(h)(1).

B. Search Results from U.S. Application to EPO - Unless box B in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the EPO access to the bibliographic data and search results from the instant patent application when a European patent application claiming priority to the instant patent application is filed. See 37 CFR 1.14(h)(2).

The applicant is reminded that the EPO's Rule 141(1) EPC (European Patent Convention) requires applicants to submit a copy of search results from the instant application without delay in a European patent application that claims priority to the instant application.

2. Opt-Out of Authorizations to Permit Access by a Foreign Intellectual Property Office(s)

☐ A. Applicant **DOES NOT** authorize the USPTO to permit a participating foreign IP office access to the instant application-as-filed. If this box is checked, the USPTO will not be providing a participating foreign IP office with any documents and information identified in subsection 1A above.

☐ B. Applicant **DOES NOT** authorize the USPTO to transmit to the EPO any search results from the instant patent application. If this box is checked, the USPTO will not be providing the EPO with search results from the instant application.

NOTE: Once the application has published or is otherwise publicly available, the USPTO may provide access to the application in accordance with 37 CFR 1.14.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	533055US
		Application Number	
Title of Invention	ARCHITECTURE AND METHOD FOR NAND MEMORY OPERATION		

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.				
Applicant	1	Remove		
If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.				
Clear				
☒ Assignee	Legal Representative under 35 U.S.C. 117	Joint Inventor		
Person to whom the inventor is obligated to assign.		Person who shows sufficient proprietary interest		
If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:				
Name of the Deceased or Legally Incapacitated Inventor:				
If the Applicant is an Organization check here. ☒				
Organization Name	Yangtze Memory Technologies Co., Ltd.			
Mailing Address Information For Applicant:				
Address 1	No.88 Weilai 3rd Road			
Address 2	East Lake High-tech Development Zone			
City	Wuhan, Hubei	State/Province		
Country	CN	Postal Code		
Phone Number		Fax Number		
Email Address				
Additional Applicant Data may be generated within this form by selecting the Add button.				
Add				

Assignee Information including Non-Applicant Assignee Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	533055US
		Application Number	
Title of Invention	ARCHITECTURE AND METHOD FOR NAND MEMORY OPERATION		

Assignee	1		
Complete this section if assignee information, including non-applicant assignee information, is desired to be included on the patent application publication. An assignee-applicant identified in the "Applicant Information" section will appear on the patent application publication as an applicant. For an assignee-applicant, complete this section only if identification as an assignee is also desired on the patent application publication.			
			Remove
If the Assignee or Non-Applicant Assignee is an Organization check here. ☒			
Organization Name	Yangtze Memory Technologies Co., Ltd.		
Mailing Address Information For Assignee including Non-Applicant Assignee:			
Address 1	No.88 Weilai 3rd Road		
Address 2	East Lake High-tech Development Zone		
City	Wuhan, Hubei	State/Province	
Country ⁱ	CN	Postal Code	
Phone Number		Fax Number	
Email Address			
Additional Assignee or Non-Applicant Assignee Data may be generated within this form by selecting the Add button.			Add

Signature:

NOTE: This Application Data Sheet must be signed in accordance with 37 CFR 1.33(b). However, if this Application Data Sheet is submitted with the INITIAL filing of the application and either box A or B is not checked in subsection 2 of the "Authorization or Opt-Out of Authorization to Permit Access" section, then this form must also be signed in accordance with 37 CFR 1.14(c).

This Application Data Sheet must be signed by a patent practitioner if one or more of the applicants is a **juristic entity** (e.g., corporation or association). If the applicant is two or more joint inventors, this form must be signed by a patent practitioner, all joint inventors who are the applicant, or one or more joint inventor-applicants who have been given power of attorney (e.g., see USPTO Form PTO/AIA/81) on behalf of all joint inventor-applicants.

See 37 CFR 1.4(d) for the manner of making signatures and certifications.

Signature	/Leonidas Boutsikaris/		Date (YYYY-MM-DD)	2021-03-04	
First Name	Leonidas	Last Name	Boutsikaris, Ph.D.	Registration Number	61,377
Additional Signature may be generated within this form by selecting the Add button.				Add	

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	533055US
		Application Number	
Title of Invention	ARCHITECTURE AND METHOD FOR NAND MEMORY OPERATION		

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

- 1 The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
- 3 A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Patent Application Fee Transmittal				
Application Number:				
Filing Date:				
Title of Invention:		ARCHITECTURE AND METHOD FOR NAND MEMORY OPERATION		
First Named Inventor/Applicant Name:		Changhyun LEE		
Filer:		Philippe Jean-Claude Signore/Kimberly Ashwell		
Attorney Docket Number:		533055US		
Filed as Large Entity				
Filing Fees for Utility under 35 USC 111(a)				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
UTILITY APPLICATION FILING	1011	1	320	320
UTILITY SEARCH FEE	1111	1	700	700
UTILITY EXAMINATION FEE	1311	1	800	800
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				1820

Electronic Acknowledgement Receipt	
EFS ID:	42084780
Application Number:	17191768
International Application Number:	
Confirmation Number:	5157
Title of Invention:	ARCHITECTURE AND METHOD FOR NAND MEMORY OPERATION
First Named Inventor/Applicant Name:	Changhyun LEE
Customer Number:	22850
Filer:	Philippe Jean-Claude Signore/Kimberly Ashwell
Filer Authorized By:	Philippe Jean-Claude Signore
Attorney Docket Number:	533055US
Receipt Date:	04-MAR-2021
Filing Date:	
Time Stamp:	09:01:09
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	\$ 1820
RAM confirmation Number	E202134001383892
Deposit Account	
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:	

File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		533055USNewApp1.pdf	12807171	yes	64
			89a1f883b3723a3c0cecacf5378657ffd205e3f		
	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Transmittal of New Application		1	1	
	Specification		2	35	
	Claims		36	45	
	Abstract		46	46	
	Drawings-only black and white line drawings		47	57	
	Oath or Declaration filed		58	62	
	Power of Attorney		63	64	
Warnings:					
Information:					
2	Application Data Sheet	533055USNewApp2.pdf	1256104	no	9
			98597f53b9b757419aa83e208fb057c4538db1da		
Warnings:					
Information:					
3	Fee Worksheet (SB06)	fee-info.pdf	35133	no	2
			8851a07fb9578526b38e4c7d28d59b309edf9176		
Warnings:					
Information:					
Total Files Size (in bytes):			14098408		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875						Application or Docket Number 17/191,768	
APPLICATION AS FILED - PART I							
(Column 1)		(Column 2)		SMALL ENTITY		OTHER THAN SMALL ENTITY	
FOR	NUMBER FILED	NUMBER EXTRA	RATE(\$)	FEE(\$)		RATE(\$)	FEE(\$)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	320
SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A	N/A			N/A	700
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	800
TOTAL CLAIMS (37 CFR 1.16(i))	20	minus 20 = *				x 100 =	0.00
INDEPENDENT CLAIMS (37 CFR 1.16(h))	3	minus 3 = *				x 480 =	0.00
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	1820
APPLICATION AS AMENDED - PART II							
(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY	
AMENDMENT A	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)		RATE(\$)
	Total (37 CFR 1.16(i))	*	Minus **	=	x =		x =
	Independent (37 CFR 1.16(h))	*	Minus ***	=	x =		x =
	Application Size Fee (37 CFR 1.16(s))						
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
			TOTAL ADD'L FEE			TOTAL ADD'L FEE	
(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY	
AMENDMENT B	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)		RATE(\$)
	Total (37 CFR 1.16(i))	*	Minus **	=	x =		x =
	Independent (37 CFR 1.16(h))	*	Minus ***	=	x =		x =
	Application Size Fee (37 CFR 1.16(s))						
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
			TOTAL ADD'L FEE			TOTAL ADD'L FEE	
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.							



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO.	TOT CLAIMS	IND CLAIMS
17/191,768	03/04/2021	2827	1820	533055US	20	3

CONFIRMATION NO. 5157

FILING RECEIPT

22850

OBLON, MCCLELLAND, MAIER & NEUSTADT, L.L.P.
1940 DUKE STREET
ALEXANDRIA, VA 22314



0000000124084352

Date Mailed: 03/16/2021

Receipt is acknowledged of this non-provisional utility patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF FIRST INVENTOR, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection.

Please verify the accuracy of the data presented on this receipt. If an error is noted on this Filing Receipt, please submit a written request for a corrected Filing Receipt, including a properly marked-up ADS showing the changes with strike-through for deletions and underlining for additions. If you received a "Notice to File Missing Parts" or other Notice requiring a response for this application, please submit any request for correction to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections provided that the request is grantable.

Inventor(s)

Changhyun LEE, Wuhan, CHINA;
Xiangnan ZHAO, Wuhan, CHINA;
Haibo LI, Wuhan, CHINA;

Applicant(s)

Yangtze Memory Technologies Co., Ltd., Wuhan, CHINA;

Assignment For Published Patent Application

Yangtze Memory Technologies Co., Ltd., Wuhan, CHINA

Power of Attorney: The patent practitioners associated with Customer Number 22850

Domestic Priority data as claimed by applicant

This application is a CON of PCT/CN2020/136482 12/15/2020

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see <http://www.uspto.gov> for more information.) - None.

Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

Permission to Access Application via Priority Document Exchange: Yes

Permission to Access Search Results: Yes

Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

If Required, Foreign Filing License Granted: 03/15/2021

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 17/191,768**

Projected Publication Date: 06/16/2022

Non-Publication Request: No

Early Publication Request: No

Title

ARCHITECTURE AND METHOD FOR NAND MEMORY OPERATION

Preliminary Class

365

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at <http://www.uspto.gov/web/offices/pac/doc/general/index.html>.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, <http://www.stopfakes.gov>. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific

page 2 of 4

countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

LICENSE FOR FOREIGN FILING UNDER
Title 35, United States Code, Section 184
Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign Assets Control, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

SelectUSA

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The U.S. offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to promote and facilitate business investment. SelectUSA provides information assistance to the international investor community; serves as an ombudsman for existing and potential investors; advocates on behalf of U.S. cities, states, and regions competing for global investment; and counsels U.S. economic development organizations on investment attraction best practices. To learn more about why the United States is the best country in the world to develop

technology, manufacture products, deliver services, and grow your business, visit <http://www.SelectUSA.gov> or call +1-202-482-6800.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN RE APPLICATION OF: Changhyun LEE, et al.

SERIAL NO: 17/191,768

GAU: 2827

FILED: March 4, 2021

EXAMINER:

FOR: ARCHITECTURE AND METHOD FOR NAND MEMORY OPERATION

INFORMATION DISCLOSURE STATEMENT UNDER 37 CFR 1.97

COMMISSIONER FOR PATENTS
ALEXANDRIA, VIRGINIA 22313

Commissioner:

Applicant(s) wish to disclose the following information.

REFERENCES

- ☒ The applicant(s) wish to make of record the reference(s) listed on the attached form PTO-1449 and/or accompanying documents from a corresponding foreign application. Copies of the listed reference(s) are attached, where required, as are either statements of relevancy, English translations of the categories of cited documents for foreign search reports or English translations of foreign Office Actions which provide the statement of relevancy for the foreign language references cited therein, or any readily available partial or full English translations of pertinent portions of any non-English language reference(s).
- ☐ Credit card payment is being made online (if electronically filed), or is attached hereto (if paper filed), in the amount required under 37 CFR §1.17(p).

CERTIFICATION

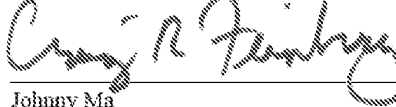
- ☐ Each item of information contained in this information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this statement.
- ☐ No item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application and, to the knowledge of the undersigned, having made reasonable inquiry, was known to any individual designated in 37 CFR §1.56(c) more than three months prior to the filing of this statement.

DEPOSIT ACCOUNT

- ☒ Please charge any additional fees for the papers being filed herewith and for which no payment is enclosed herewith, or credit any overpayment to deposit account number 15-0030.

Respectfully submitted,

OBLON, McCLELLAND,
MAIER & NEUSTADT, L.L.P.



Johnny Ma

Registration No. 59,976

Craig R. Feinberg

Registration No.: 62,116

Customer Number

22850

Tel. (703) 413-3000
Fax. (703) 413-2220
(OMMIN 02/12)

Form PTO 1449 (Modified)		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		ATTY DOCKET NO. 533055US		SERIAL NO. 17/191,768	
LIST OF REFERENCES CITED BY APPLICANT				INVENTOR(S) Changhyun LEE, et al.			
				FILING DATE March 4, 2021		GROUP 2827	
U.S. PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
	AA	2019/0316928 A1	10/17/2019	MIGNOT, Y., et al.			
	AB	2020/0152654 A1	05/14/2020	HWANG, S.-M., et al.			
	AC						
	AD						
	AE						
	AF						
	AG						
	AH						
	AI						
	AJ						
	AK						
	AL						
	AM						
	AN						
FOREIGN PATENT DOCUMENTS							
		DOCUMENT NUMBER	DATE	COUNTRY	TRANSLATION		
					YES	NO	
	AO	111758162 A	10/09/2020	China		x	
	AP	111279465 A	06/12/2020	China		x	
	AQ	111180418 A	05/19/2020	China (corresponds to US 2020/0152654 A1)		x	
	AR						
	AS						
	AT						
	AU						
	AV						
OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, etc.)							
	AW	International Search Report issued September 22, 2021 in PCT/CN2020/136462, citing documents AA and AO through AQ therein, 4 pages					
	AX						
	AY						
	AZ					☐ Additional References sheet(s) attached	
Examiner					Date considered		
*Examiner: Initial if reference is considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.							

PATENT COOPERATION TREATY

PCT

INTERNATIONAL SEARCH REPORT

(PCT Article 18 and Rules 43 and 44)

Applicant's or agent's file reference P2020TC1319	FOR FURTHER ACTION see Form PCT/ISA/220 as well as, where applicable, item 5 below.	
International application No. PCT/CN2020/136482	International filing date <i>(day/month/year)</i> 15 Dec. 2020 (15. 12. 2020)	(Earliest)Priority date <i>(day/month/year)</i>
Applicant YANGTZE MEMORY TECHNOLOGIES CO., LTD.		
This international search report has been prepared by this International Searching Authority and is transmitted to the applicant according to Article 18. A copy is being transmitted to the International Bureau. This international search report consists of a total of <u>4</u> sheets. ☐ It is also accompanied by a copy of each prior art document cited in this report.		
1. Basis of the report a. With regard to the language, the international search was carried out on the basis of: ☒ the international application in the language in which it was filed ☐ a translation of the international application into _____, which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b)) b. ☐ This international search report has been established taking into account the rectification of an obvious mistake authorized by or notified to this Authority under Rule 91 (Rule 43.6bis(a)). c. ☐ With regard to any nucleotide and /or amino acid sequence disclosed in the international application, see Box No. I. 2. ☐ Certain claims were found unsearchable (see Box No. II) 3. ☐ Unity of invention is lacking (see Box No. III) 4. With regard to the title, ☒ the text is approved as submitted by the applicant. ☐ the text has been established by this Authority to read as follows: 5. With regard to the abstract, ☒ the text is approved as submitted by the applicant. ☐ the text has been established, according to Rule 38.2(b), by this Authority as it appears in Box IV. The applicant may, within one month from the date of mailing of this international search report, submit comments to this Authority. 6. With regard to the drawings, a. The figure of the drawings to be published with the abstract is Figure No. 10 ☒ as suggested by the applicant ☐ as selected by this Authority, because the applicant failed to suggest a figure ☐ as selected by this Authority, because this figure better characterizes the invention b. ☐ none of the figures is to be published with the abstract		

INTERNATIONAL SEARCH REPORT

International application No.
PCT/CN2020/136482

A. CLASSIFICATION OF SUBJECT MATTER

H01L 27/1157 (2017.01) i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC: H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
WPI, EPDOC, CNPAT, CNKI: memory, tsg, bsg, top, select, gate, bottom, transistor, voltage, cell, verify, adjacent, string, terminal, second, program*

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	CN 111758162A (YANGTZE MEMORY TECHNOLOGIES CO., LTD.) 09 Oct.2020(09.10.2020) description, paragraphs [0033]-[0063]	1-20
A	CN 111279465A (YANGTZE MEMORY TECHNOLOGIES CO., LTD.) 12 Jun.2020(12.06.2020) the whole document	1-20
A	CN 111180418A (SAMSUNG ELECTRONICS CO., LTD.) 19 May 2020(19.05.2020) the whole document	1-20
A	US 2019318928A1 (INTERNATIONAL BUSINESS MACHINES CORPORATION) 17 Oct.2019(17.10.2019) the whole document	1-20

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

INTERNATIONAL SEARCH REPORT

International application No.
PCT/CN2020/136482

* Special categories of cited documents: "A" document defining the general state of the art which is not considered to be of particular relevance "E" earlier application or patent but published on or after the international filing date "L" document which may throw doubts on priority claim (S) or which is cited to establish the publication date of another citation or other special reason (as specified) "O" document referring to an oral disclosure, use, exhibition or other means "P" document published prior to the international filing date but later than the priority date claimed	"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art "&" document member of the same patent family
Date of the actual completion of the international search 27 Aug. 2021 (27. 08. 2021)	Date of mailing of the international search report 22 Sep. 2021 (22. 09. 2021)
Name and mailing address of the ISA/CN National Intellectual Property Administration, PRC 6, Xitucheng Rd., Jimen Bridge, Haidian District, Beijing 100088, China Facsimile No. (86-10)62019451	Authorized officer TIAN, Jing Telephone No.: 86- (10)-53961334

INTERNATIONAL SEARCH REPORT

International application No.
PCT/CN2020/136482

Patent Documents referred in the Report	Publication Date	Patent Family	Publication Date
CN111758162A	09.10.2020	None	
CN111279465A	12.06.2020	None	
CN111180418A	19.05.2020	KR2020055186A	21.05.2020
		US20200152654A1	14.05.2020
US2019318928A1	17.10.2019	None	



(12) 发明专利申请

(10) 申请公布号 CN 111758162 A

(43) 申请公布日 2020.10.09

(21) 申请号 202080001107.1

H01L 27/11573 (2017.01)

(22) 申请日 2020.05.15

H01L 27/11582 (2017.01)

(85) PCT国际申请进入国家阶段日
2020.06.24

(86) PCT国际申请的申请数据
PCT/CN2020/090411 2020.05.15

(71) 申请人 长江存储科技有限责任公司
地址 430223 湖北省武汉市东湖新技术开
发区未来三路88号

(72) 发明人 张中 孙中旺 周文辉 夏志良

(74) 专利代理机构 北京永新新闻知识产权代理
有限公司 11376

代理人 林锦辉 刘景峰

(51) Int. Cl.

H01L 27/1157 (2017.01)

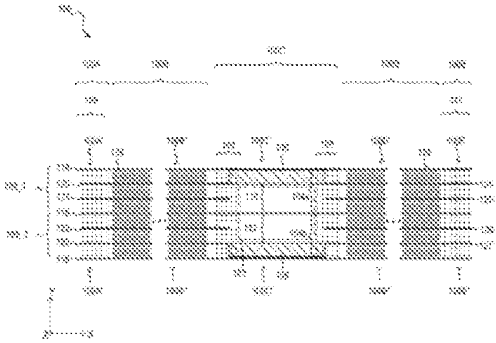
权利要求书4页 说明书16页 附图10页

(54) 发明名称

三维NAND存储器件及其形成方法

(57) 摘要

在制造半导体器件的方法中,形成初始堆叠体。初始堆叠体由交替设置在衬底之上的牺牲层和绝缘层形成,并且包括依次设置的第一连接区、第一阵列区和第二连接区。第一初始阶梯形成在第一连接区中并且形成在第一组牺牲层和绝缘层中。第一顶部选择栅阶梯形成在第二连接区中,并且形成在第二组牺牲层和绝缘层中。随后在第一连接区中执行蚀刻工艺,以使第一初始阶梯沿垂直于衬底的垂直方向朝衬底移动,从而形成第一底部选择栅阶梯。



1. 一种用于制造半导体器件的方法, 包括:

形成交替地设置在衬底之上的牺牲层和绝缘层的初始堆叠体, 所述初始堆叠体包括沿所述衬底的第一方向依次设置的第一连接区、第一阵列区和第二连接区;

在所述初始堆叠体的所述第一连接区中形成第一初始阶梯, 所述第一初始阶梯形成在第一组所述牺牲层和所述绝缘层中;

在所述初始堆叠体的所述第二连接区中形成第一顶部选择栅 (TSG) 阶梯, 所述第一 TSG 阶梯形成在第二组所述牺牲层和所述绝缘层中; 以及

在所述第一连接区中执行蚀刻工艺, 以使所述第一初始阶梯沿垂直于所述衬底的垂直方向朝所述衬底移动, 从而形成第一底部选择栅 (BSG) 阶梯。

2. 根据权利要求1所述的方法, 还包括:

在所述初始堆叠体上形成至少一个停止层, 所述至少一个停止层在所述初始堆叠体中限定所述第一连接区、所述第一阵列区和所述第二连接区; 以及

基于所述至少一个停止层执行修整蚀刻工艺以形成多个壁结构以及所述第二连接区中的初始连接阶梯, 所述壁结构被所述至少一个停止层覆盖, 并且所述初始连接阶梯未被覆盖并沿所述衬底的垂直于所述第一方向的第二方向布置在所述壁结构之间。

3. 根据权利要求2所述的方法, 其中, 执行所述蚀刻工艺包括:

在所述第一组所述牺牲层和所述绝缘层以及所述第二组所述牺牲层和所述绝缘层上执行所述蚀刻工艺, 以将所述第一初始阶梯移动到一个或多个最底部牺牲层和最底部绝缘层, 并使所述初始连接阶梯沿所述垂直方向朝所述衬底移动以形成连接阶梯, 每个所述连接阶梯形成在所述初始堆叠体的相应的牺牲层和绝缘层中。

4. 根据权利要求3所述的方法, 其中, 执行所述蚀刻工艺还包括:

依次执行多个切削工艺, 以使所述第一连接区中的所述第一初始阶梯朝所述衬底移动, 以形成所述第一BSG阶梯, 其中:

所述切削工艺中的第一切削工艺使所述第一初始阶梯朝所述衬底移动第一数量的台阶; 并且

所述切削工艺中的在所述第一切削工艺之后的第二切削工艺使所述第一初始阶梯移动第二数量的台阶, 所述第二数量的台阶是所述第一数量的台阶的两倍。

5. 根据权利要求4所述的方法, 其中, 将所述切削工艺进一步施加到所述第二连接区中的所述初始连接阶梯上, 以使所述初始连接阶梯朝所述衬底移动, 以便形成所述连接阶梯, 每个所述初始连接阶梯接受相应数量的切削工艺, 以使每个所述初始连接阶梯在相应的牺牲层和绝缘层中移动。

6. 根据权利要求5所述的方法, 还包括:

形成延伸穿过所述第一连接区、所述第一阵列区和所述第二连接区的第一分隔结构, 所述第一分隔结构沿所述第一方向形成并延伸穿过所述初始堆叠体进入到所述衬底中。

7. 根据权利要求6所述的方法, 还包括:

在所述第一阵列区中形成第二分隔结构, 所述第二分隔结构沿所述第一方向设置, 并定位于所述第一分隔结构之间, 所述第二分隔结构延伸穿过所述初始堆叠体进入到所述衬底中, 并进一步延伸穿过所述第一BSG阶梯和所述第一TSG阶梯。

8. 根据权利要求1所述的方法, 还包括:

在所述初始堆叠体的所述第一阵列区中形成沟道结构,所述沟道结构沿所述垂直方向延伸穿过所述初始堆叠体进入到所述衬底中。

9. 根据权利要求6所述的方法,其中,

所述初始堆叠体还包括第二阵列区和第三连接区,所述第二阵列区定位于所述第二连接区和所述第三连接区之间;并且

所述方法还包括:

在所述第三连接区中形成第二初始阶梯,并且在所述第二连接区中形成第二TSG阶梯,所述第一初始阶梯和所述第二初始阶梯形成在所述第一组所述牺牲层和所述绝缘层中,所述第一TSG阶梯、所述第二TSG阶梯和所述初始连接阶梯形成在所述第二组所述牺牲层和所述绝缘层中;以及

执行所述蚀刻工艺,以使所述第一初始阶梯、所述第二初始阶梯和所述初始连接阶梯沿所述垂直方向朝所述衬底移动,从而在所述第一连接区中形成所述第一BSG阶梯,在所述第三连接区中形成第二BSG阶梯,并且在所述第二连接区中形成所述连接阶梯。

10. 根据权利要求9所述的方法,其中:

所述第一TSG阶梯、所述连接阶梯和所述第二TSG阶梯沿所述第一方向延伸,所述连接阶梯设置于所述第一TSG阶梯和所述第二TSG阶梯之间;并且

所述第一分隔结构进一步延伸穿过所述第二阵列区和所述第三连接区。

11. 根据权利要求9所述的方法,还包括:

在所述第二阵列区中形成第三分隔结构,所述第三分隔结构沿所述第一方向设置,并定位于所述第一分隔结构之间,所述第三分隔结构延伸穿过所述初始堆叠体进入到所述衬底中,并进一步延伸穿过所述第二BSG阶梯和所述第二TSG阶梯。

12. 一种用于制造半导体器件的方法,包括:

形成交替设置在衬底之上的牺牲层和绝缘层的初始堆叠体,所述初始堆叠体包括沿所述衬底的第一方向依次设置的第一连接区、第一阵列区、第二连接区、第二阵列区和第三连接区;

在所述第一连接区中形成第一初始阶梯,并且在所述第三连接区中形成第二初始阶梯,所述第一初始阶梯和所述第二初始阶梯形成在第一组所述牺牲层和所述绝缘层中;

沿所述第一阵列区在所述第二连接区中形成第一顶部选择栅(TSG)阶梯,并沿所述第二阵列区在所述第二连接区中形成第二TSG阶梯,所述第一TSG阶梯和所述第二TSG阶梯形成在第二组所述牺牲层和所述绝缘层中;以及

在所述第一连接区和所述第三连接区中执行蚀刻工艺,以使所述第一初始阶梯和所述第二初始阶梯沿垂直于所述衬底的垂直方向朝所述衬底移动,从而在所述第一连接区中形成第一底部选择栅(BSG)阶梯并且在所述第三连接区中形成第二BSG阶梯。

13. 根据权利要求12所述的方法,还包括:

在所述初始堆叠体上形成至少一个停止层,所述至少一个停止层在所述初始堆叠体中限定所述第一连接区、所述第一阵列区、所述第二连接区、所述第二阵列区和所述第三连接区;以及

基于所述至少一个停止层执行修整蚀刻工艺以形成多个壁结构以及所述第二连接区中的初始连接阶梯,所述初始连接阶梯定位于所述第一阵列区和所述第二阵列区之间,所

述壁结构被所述至少一个停止层覆盖,并且所述初始连接阶梯未被覆盖并进一步布置在所述壁结构之间。

14. 根据权利要求13所述的方法,执行所述蚀刻工艺包括:

在所述第一初始阶梯和所述第二初始阶梯的所述第一组所述牺牲层和所述绝缘层上执行所述蚀刻工艺,以将所述第一初始阶梯和所述第二初始阶梯移动到一个或多个最底部牺牲层和最底部绝缘层;以及

在所述第二组所述牺牲层和所述绝缘层上执行所述蚀刻工艺,以使所述初始连接阶梯沿所述垂直方向朝所述衬底移动,以形成连接台阶,每个所述连接台阶形成在所述初始堆叠体的相应的牺牲层和绝缘层中。

15. 根据权利要求14所述的方法,其中,执行所述蚀刻工艺还包括:

依次执行多个切削工艺,以使所述第一初始阶梯和所述第二初始阶梯朝所述衬底移动,以分别形成所述第一BSG阶梯和所述第二BSG阶梯,其中:

所述切削工艺中的第一切削工艺分别使所述第一初始阶梯和所述第二初始阶梯朝所述衬底移动第一数量的台阶;并且

所述切削工艺中的在所述第一切削工艺之后的第二切削工艺分别使所述第一初始阶梯和所述第二初始阶梯移动第二数量的台阶,所述第二数量的台阶是所述第一数量的台阶的两倍。

16. 根据权利要求15所述的方法,其中,在所述第二连接区中的所述初始连接阶梯上进一步施加所述切削工艺,以使所述初始连接阶梯朝所述衬底移动,从而形成所述连接阶梯,每个所述初始连接阶梯接受相应数量的切削工艺,以使每个所述初始连接阶梯在相应的牺牲层和绝缘层中移动。

17. 一种半导体器件,包括:

形成为堆叠体并且沿衬底的第一方向依次设置的第一底部选择栅(BSG)阶梯、第一阵列区、连接区、第二阵列区和第二BSG阶梯,其中:

所述堆叠体由交替地设置在所述衬底之上的字线层和绝缘层形成;

所述第一BSG阶梯形成在第一组所述字线层和所述绝缘层中,并且所述第二BSG阶梯形成在第二组所述字线层和所述绝缘层中;

所述连接区包括沿所述第一阵列区定位的第一顶部选择栅(TSG)阶梯和沿所述第二阵列区定位的第二TSG阶梯,所述第一TSG阶梯形成在第三组所述字线层和所述绝缘体中,并且所述第二TSG阶梯形成在第四组所述字线层和所述绝缘层中;以及

所述第一TSG阶梯和所述第二TSG阶梯定位于所述第一BSG阶梯和所述第二BSG阶梯上方。

18. 根据权利要求17所述的半导体器件,还包括:

延伸穿过所述第一BSG阶梯、所述第一阵列区、所述连接区、所述第二阵列区和所述第二BSG阶梯的第一分隔结构,所述第一分隔结构进一步延伸穿过所述堆叠体进入到所述衬底中并沿所述第一方向延伸;

延伸穿过所述第一阵列区的第二分隔结构,所述第二分隔结构沿所述第一方向设置,并定位于所述第一分隔结构之间,所述第二分隔结构延伸穿过所述堆叠体进入到所述衬底中,并进一步延伸穿过所述第一BSG阶梯和所述第一TSG阶梯;以及

延伸穿过所述第二阵列区的第三分隔结构,所述第三分隔结构沿所述第一方向设置,并定位于所述第一分隔结构之间,所述第三分隔结构延伸穿过所述堆叠体,并进一步延伸穿过所述第二BSG阶梯和所述第二TSG阶梯。

19. 根据权利要求18所述的半导体器件,其中,所述连接区还包括多个壁结构和连接阶梯,其中:

所述连接阶梯沿所述衬底的垂直于所述第一方向的第二方向布置在所述壁结构之间;
所述连接阶梯沿所述第一方向布置在所述第一TSG阶梯和所述第二TSG阶梯之间;并且
每个所述连接阶梯形成在所述堆叠体的相应的字线层和绝缘层中。

20. 根据权利要求19所述的半导体器件,其中:

所述连接阶梯中的至少一个包括第一组梯级和第二组梯级;

所述第一组梯级沿所述第一方向延伸;并且

所述第二组梯级沿第三方向延伸,所述第一方向与所述第三方向相反。

三维NAND存储器件及其形成方法

背景技术

[0001] 闪存存储器件最近已经得到快速发展。闪存存储器件能够在不施加电压的情况下长时间保存存储的数据。此外,闪存存储器件的读取速率相对较高,并且容易擦除存储的数据并将数据重新写入到闪存存储器件中。因此,闪存存储器件已被广泛用于微型计算机、自动控制系统等中。为了增加闪存存储器件的位密度并降低闪存存储器件的位成本,已经开发了三维(3D) NAND(与非)闪存存储器件。

发明内容

[0002] 在本公开中,提供了针对制造3D NAND器件的方法的实施例。实施例包括一种方法,该方法与连接阶梯同时地形成底部选择栅(BSG)阶梯和顶部选择栅(TSG)阶梯。

[0003] 在本公开中,提供了一种用于制造半导体器件的方法。在该方法中,可以形成初始堆叠体。初始堆叠体由牺牲字线层(也称为牺牲层)和交替设置在衬底之上的绝缘层形成。初始堆叠体可以包括沿衬底的第一方向依次设置的第一连接区、第一阵列区和第二连接区。第一初始阶梯然后可以设置在牺牲字线层和绝缘层的初始堆叠体的第一连接区中,并形成在第一组牺牲字线层和绝缘层中。第一顶部选择栅(TSG)阶梯可以设置在牺牲字线层和绝缘层的初始堆叠体的第二连接区中,并形成在第二组牺牲字线层和绝缘层中。随后可以在第一连接区中执行蚀刻工艺,以将第一初始阶梯沿垂直于衬底的垂直方向朝衬底移动,从而形成第一底部选择栅(BSG)阶梯。

[0004] 在该方法中,至少一个停止层可以形成在初始堆叠体上,其中至少一个停止层可以在初始堆叠体中限定第一连接区、第一阵列区和第二连接区。随后可以基于至少一个停止层来执行修整蚀刻工艺以形成多个壁结构以及第二连接区中的初始连接阶梯。壁结构可以被至少一个停止层覆盖,并且初始连接阶梯可以不被覆盖并且沿衬底的垂直于第一方向的第二方向布置在壁结构之间。

[0005] 在一些实施例中,可以在第一初始阶梯的第一组牺牲字线层和绝缘层以及第二组牺牲字线层和绝缘层上执行蚀刻工艺以将第一初始阶梯移动到一个或多个最底部牺牲字线层和最底部绝缘层,并将初始连接阶梯沿垂直方向朝衬底移动,以形成连接阶梯。每个阶梯可以形成在初始堆叠体的相应的牺牲层和绝缘层中。

[0006] 在该方法中,可以依次执行多个切削工艺以将第一连接区中的第一初始阶梯朝衬底移动以形成第一BSG阶梯。切削工艺中的第一切削工艺可以使第一初始阶梯朝衬底移动第一数量的台阶。切削工艺中的在第一切削工艺之后的第二切削工艺可以使第一初始阶梯移动第二数量的台阶,该第二数量的台阶是第一数量的台阶的两倍。

[0007] 在该方法中,可以在第二连接区中的初始连接阶梯上进一步施加切削工艺,以使初始连接阶梯朝衬底移动,以形成连接阶梯,其中每个初始连接阶梯可以接受相应数量的切削工艺,以使每个初始连接阶梯可以在相应的牺牲层和绝缘层中移动。

[0008] 在该方法中,可以形成第一分隔结构。第一分隔结构可以延伸穿过第一连接区、第一阵列区和第二连接区。第一分隔结构可以沿第一方向形成,并且延伸穿过初始堆叠体进

入到衬底中。另外,可以在第一阵列区中形成第二分隔结构。第二分隔结构可以沿第一方向设置,并定位于第一分隔结构之间。第二分隔结构可以进一步延伸穿过初始堆叠体进入到衬底中,并且延伸穿过第一BSG阶梯和第一TSG阶梯。

[0009] 在该方法中,可以在初始堆叠体的第一阵列区中形成沟道结构。沟道结构可以沿垂直方向延伸穿过初始堆叠体进入到衬底中。

[0010] 在一些实施例中,初始堆叠体还可以包括第二阵列区和第三连接区。第二阵列区可以定位于第二连接区和第三连接区之间。因此,第二初始阶梯可以形成在第三连接区中,并且第二TSG阶梯可以形成在第二连接区中。第一初始阶梯和第二初始阶梯可以形成在第一组牺牲字线层和绝缘层中。第一TSG阶梯、第二TSG阶梯和初始连接阶梯可以形成在第二组牺牲字线层和绝缘层中。因此,可以执行蚀刻工艺以使第一初始阶梯、第二初始阶梯和初始连接阶梯沿垂直方向朝衬底移动,从而在第一连接区中形成第一BSG阶梯,在第三连接区中形成第二BSG阶梯,并且在第二连接区中形成连接阶梯。

[0011] 因此,第一TSG阶梯、连接阶梯和第二TSG阶梯可以沿第一方向延伸,并且连接阶梯可以设置在第一TSG阶梯和第二TSG阶梯之间。第一分隔结构可以进一步延伸穿过第二阵列区和第三连接区。

[0012] 在该方法中,第三分隔结构可以形成在第二阵列区中。第三分隔结构可以沿第一方向设置,并且定位于第一分隔结构之间。第三分隔结构可以进一步延伸穿过初始堆叠体进入到衬底,并且延伸穿过第二BSG阶梯和第二TSG阶梯。

[0013] 根据本公开的另一方面,提供了一种用于制造半导体器件的方法。在该方法中,可以形成初始堆叠体。初始堆叠体由牺牲字线层和绝缘层形成,所述牺牲字线层和绝缘层交替地设置在衬底之上。牺牲字线层和绝缘层的初始堆叠体可以包括沿衬底的第一方向依次设置的第一连接区、第一阵列区、第二连接区、第二阵列区和第三连接区。第一初始阶梯可以形成在第一连接区中,并且第二初始阶梯可以形成在第三连接区中。第一初始阶梯和第二初始阶梯可以形成在第一组牺牲字线层和绝缘层中。另外,第一顶部选择栅(TSG)阶梯可以沿第一阵列区形成在第二连接区中,并且第二TSG阶梯可以沿第二阵列区形成在第二连接区中。第一TSG阶梯和第二TSG阶梯可以形成在第二组牺牲字线层和绝缘层中。随后可以在第一连接区和第三连接区中执行蚀刻工艺,以使第一初始阶梯和第二初始阶梯沿垂直于衬底的垂直方向朝衬底移动,从而在第一连接区中形成第一底部选择栅(BSG)阶梯,并且在第三连接区中形成第二BSG阶梯。

[0014] 在该方法中,至少一个停止层可以形成在初始堆叠体上,其中该至少一个停止层可以在初始堆叠体中限定第一连接区、第一阵列区、第二连接区、第二阵列区和第三连接区。此外,可以基于至少一个停止层来执行修整蚀刻工艺以形成多个壁结构以及第二连接区中的初始连接阶梯。壁结构和初始连接阶梯可以定位于第一阵列区和第二阵列区之间。壁结构可以被至少一个停止层覆盖,并且初始连接阶梯可以不被覆盖并且进一步布置在壁结构之间。

[0015] 在一些实施例中,可以在第一初始阶梯和第二初始阶梯的第一组牺牲字线层和绝缘层上执行蚀刻工艺。因此,蚀刻工艺可以将第一初始阶梯和第二初始阶梯移动到一个或多个最底部牺牲字线层和最底部绝缘层。也可以在第二组牺牲层和绝缘层上执行蚀刻工艺,以使初始连接阶梯沿垂直方向朝衬底移动以形成连接阶梯,其中每个所述连接阶梯可

以形成在初始堆叠体的相应的牺牲层和绝缘层中。

[0016] 在一些实施例中,可以依次执行多个切削工艺以将第一初始阶梯和第二初始阶梯朝衬底移动,以分别形成第一BSG阶梯和第二BSG阶梯。切削工艺中的第一切削工艺可以使第一初始阶梯和第二初始阶梯分别朝衬底移动第一数量的台阶。切削工艺中的在第一切削工艺之后的第二切削工艺可以分别将第一初始阶梯和第二初始阶梯移动第二数量的台阶,其中第二数量的台阶是第一数量的台阶的两倍。

[0017] 还可以在第二连接区中的初始连接阶梯上施加切削工艺,以将初始连接阶梯朝衬底移动,以形成连接阶梯,其中,每个所述初始连接阶梯可以接受相应数量的切削工艺,以使每个所述初始连接阶梯在相应的牺牲层和绝缘层中移动。

[0018] 根据本公开的又一方面,提供了一种半导体器件。半导体器件可以具有第一底部选择栅(BSG)阶梯、第一阵列区、连接区、第二阵列区和第二BSG阶梯,它们形成为堆叠体并且沿衬底的第一方向依次设置。堆叠体可以由交替地设置在衬底之上的字线层和绝缘层形成。第一BSG阶梯可以形成在第一组字线层和绝缘层中,并且第二BSG阶梯可以形成在第二组字线层和绝缘层中。连接区包括沿第一阵列区定位的第一顶部选择栅(TSG)阶梯和沿第二阵列区定位的第二TSG阶梯。第一TSG阶梯可以形成在第三组字线层和绝缘层中,并且第二TSG阶梯可以形成在第四组字线层和绝缘层中。第一TSG阶梯和第二TSG阶梯定位于第一BSG阶梯和第二BSG阶梯上方。

[0019] 在半导体器件中,第一分隔结构可以延伸穿过第一BSG阶梯、第一阵列区、连接区、第二阵列区和第二BSG阶梯。第一分隔结构可以进一步延伸穿过所述堆叠体进入到衬底中并沿第一方向延伸。半导体器件可以具有延伸穿过第一阵列区的第二分隔结构。第二分隔结构可以沿第一方向设置,并定位于第一分隔结构之间。第二分隔结构可以延伸穿过堆叠体进入到衬底中,并且进一步延伸穿过第一BSG阶梯和第一TSG阶梯。半导体器件还可以包括第三分隔结构。第三分隔结构可以延伸穿过第二阵列区。第三分隔结构可以沿第一方向设置,并且定位于第一分隔结构之间。第三分隔结构可以延伸穿过堆叠体,并且进一步延伸穿过第二BSG阶梯和第二TSG阶梯。

[0020] 在一些实施例中,连接区还可以包括多个壁结构和连接阶梯。连接阶梯可以沿衬底的垂直于第一方向的第二方向布置在壁结构之间。连接阶梯可以沿第一方向设置在第一TSG阶梯和第二TSG阶梯之间。每个连接阶梯可以形成在堆叠体的相应的字线层和绝缘层中。

[0021] 在半导体器件中,连接阶梯中的至少一个包括第一组梯级和第二组梯级。第一组梯级可以沿第一方向延伸,并且第二组梯级可以沿第三方向延伸,其中第一方向与第三方向相反。

附图说明

[0022] 当与附图一起阅读时,根据以下具体实施方式可以最好地理解本公开的各方面。注意,根据行业中的标准实践,各种特征未按比例绘制。实际上,为了清楚起见,各种特征的尺寸可以任意增加或减小。

[0023] 图1是根据本公开的示例性实施例的3D NAND器件的俯视图。

[0024] 图2是根据本公开的示例性实施例的3D NAND器件的三维视图。

[0025] 图3是根据本公开的示例性实施例的3D NAND器件的放大的三维视图。

[0026] 图4、图5、图6、图7、图8、图9A、图9B和图10包括根据本公开的示例性实施例的制造3D NAND器件的各个中间步骤的截面图、俯视图和三维视图。

[0027] 图11是根据本公开的示例性实施例的用于制造3D NAND器件的工艺的流程圖。

具体实施方式

[0028] 以下公开内容提供了用于实施所提供的主题的不同特征的许多不同的实施例或示例。以下描述了部件和布置的特定示例以简化本公开。当然,这些仅仅是示例,而无意于进行限制。例如,在下面的描述中,在第二特征之上或上的第一特征的形成可以包括第一特征和第二特征可以直接接触的实施例,并且还可以包括其中可以在第一和第二特征之间形成附加特征使得第一和第二特征可以不直接接触的实施例。另外,本公开可以在各个示例中重复附图标记的数字和/或字母。该重复是由于简单和清楚的目的,并且其本身并不指示所讨论的各种实施例和/或配置之间的关系。

[0029] 此外,为了便于描述,本文中可以使用诸如“在...下面”、“在...下方”、“下部”、“在...上方”、“上部”之类的空间相对术语,以描述一个元件或特征相对于另一个或多个元件或特征的如图所示的关系。除了在图中描述的取向之外,空间相对术语还意图涵盖器件在使用或操作中的不同取向。装置可以以其他方式定向(旋转90度或以其他取向),并且本文使用的空间相对描述语可以相应地以类似方式解释。

[0030] 3D NAND器件可以包括一个或多个存储平面,并且一个或多个存储平面中的每个可以包括多个存储块。一个或多个存储块中的每个可以具有定位于两个阵列区之间的连接区。连接区和阵列区形成在交替设置在衬底之上的字线层和绝缘层的堆叠体中。字线层可以包括依次设置在衬底之上的底部选择栅(BSG)层、栅极层(或字线层)和顶部选择栅(TSG)层。阵列区可以包括多个沟道结构。每个沟道结构可以耦合到字线层以形成相应的垂直NAND存储单元串。垂直NAND存储单元串可以包括一个或多个底部选择晶体管(BST)、多个存储单元(MC)以及一个或多个顶部选择晶体管(TST),它们沿衬底的高度方向(或Z方向)依次并串联地设置在衬底之上。BST可以由沟道结构和BSG层形成,MC可以由沟道结构和字线层形成,并且TST可以由沟道结构和TSG层形成。

[0031] 在这样的3D NAND器件中,连接区可以包括可以形成在BSG层、字线层和TSG层中的梯级。字线触点可以进一步形成在所述梯级上以连接到BSG层、字线层和TSG层。在3D NAND器件中,字线层中的梯级(也称为连接阶梯)可以通过梯级划分方案(SDS)形成,其中梯级可以具有一个或多个下台阶方向以节省处理时间。但是,TSG层中的梯级(也称为TSG阶梯)和BSG层中的梯级(也称为BSG阶梯)无法通过SDS形成,因为一个或多个TSG切割结构和BSG切割结构通常分别形成在TSG层和BSG层中,以将TSG层和BSG层分别划分为子TSG层和子BSG层。因此,通常分别形成TSG层和BSG层中的梯级以及字线层中的梯级。

[0032] 在本公开中,提供了一种制造方法。在该方法中,可以通过一个或多个修整蚀刻工艺在堆叠体中同时形成初始BSG阶梯、初始连接阶梯和TSG阶梯。随后可以施加一个或多个去除工艺(例如,诸如均厚干法蚀刻工艺的切削工艺)以将初始BSG阶梯移动到一个或多个底部字线层(例如,最底部字线层)和底部绝缘层(例如,最底部绝缘层)以形成BSG阶梯。去除工艺还可以将初始连接阶梯朝衬底移动以形成连接阶梯,其中连接阶梯中的每个可以形

成在堆叠体的相应的字线层和绝缘层中。本公开的方法不仅可以获得产量提升,而且可以获得成本降低。

[0033] 图1是根据本公开的示例性实施例的3D NAND器件100(也称为器件100)的俯视图。如图1所示,器件100可以具有沿衬底(未示出)的第一方向(例如,X方向)依次设置的第一连接区100A、第一阵列区100B、第二连接区100C、第二阵列区100D和第三连接区100E。第一连接区100A、第一阵列区100B、第二连接区100C、第二阵列区100D和第三连接区100E可以形成在交替设置在衬底之上的字线层和绝缘层的堆叠体中。第一连接区100A可以包括第一BSG阶梯109,该第一BSG阶梯109形成在与衬底相邻的第一组字线层和绝缘层中,例如,形成在与衬底相邻的一个或多个最底部字线层和最底部绝缘层中。类似地,第三连接区100E可以包括第二BSG阶梯111,第二BSG阶梯111也可以形成在与衬底相邻的第一组字线层和绝缘层中。

[0034] 第二连接区100C可以定位于第一阵列区100B和第二阵列区100D之间。第二连接区100C可以包括定位为与第一阵列区100B相邻的第一TSG阶梯102和定位为与第二阵列区100D相邻的第二TSG阶梯104。第二连接区100C还可以包括第一壁结构106、第二壁结构108和多个连接阶梯103。第一TSG阶梯102、连接阶梯103和第二TSG阶梯104沿X方向依次布置。第一TSG阶梯102、连接阶梯103和第二TSG阶梯104还沿衬底的Y方向设置在第一壁结构106和第二壁结构108之间。第一TSG阶梯102和第二TSG阶梯104可以形成在第二组字线层和绝缘层中,例如,形成一个或多个顶部字线层和顶部绝缘层中。另外,连接阶梯103中的每个可以形成在堆叠体的相应的字线层和绝缘层中。

[0035] 器件100可以包括沿第一连接区100A、第一阵列区100B、第二连接区100C、第二阵列区100D和第三连接区100E的第一侧定位的第一分隔结构114。第一分隔结构114可以延伸穿过堆叠体进入到衬底中并且沿第一方向(例如,X方向)延伸。如图1所示,第一连接区100A的第一侧可以是100A',第一阵列区100B的第一侧可以是100B',第二连接区100C的第一侧可以是100C',第二阵列区100D的第一侧可以是100D',并且第三连接区100E的第一侧可以是100E'。

[0036] 器件100可以具有延伸穿过第一连接区100A、第一阵列区100B、第二连接区100C、第二阵列区100D和第三连接区100E的第二分隔结构116。第二分隔结构116可以沿第一方向形成并且延伸穿过堆叠体进入到衬底。在一些实施例中,连接阶梯103可以由第二分隔结构116分隔成第一连接阶梯110和第二连接阶梯112。第二分隔结构116可以进一步将第一BSG阶梯109划分为BSG阶梯109_1和BSG阶梯109_2。

[0037] 器件100可以包括沿第一连接区100A、第一阵列区100B、第二连接区100C、第二阵列区100D和第三连接区100E的第二侧定位的第三分隔结构118。第三分隔结构118可以进一步延伸穿过堆叠体进入到衬底并沿第一方向延伸。如图1所示,第一连接区100A的第二侧可以是100A'',第一阵列区100B的第二侧可以是100B'',第二连接区100C的第二侧可以是100C'',第二阵列区100D的第二侧可以是100D'',并且第三连接区100E的第二侧可以是100E''。

[0038] 在一些实施例中,第一分隔结构114、第二分隔结构116和第三分隔结构118可以是栅缝隙(GLS)结构。在一些实施例中,GLS结构可以由导电材料制成并且定位于阵列公共源(ACS)区上以用作触点,其中ACS区形成在衬底中以用作公共源极。在一些实施例中,GLS结

构可以由电介质材料制成以用作分隔结构。在一些实施例中,使用后栅极制造技术来形成器件100。因此,形成GLS结构以帮助去除牺牲字线层(也称为牺牲层)以及形成真正的栅极。

[0039] 器件100可以包括第一阵列区100B中的第一阵列分隔结构(或第一阵列GLS结构)120-123。第一阵列分隔结构120-123可以沿第一方向(例如,X方向)设置,并且定位于第一分隔结构114和第三分隔结构118之间。第一阵列分隔结构120-123可以延伸穿过堆叠体进入到衬底中,并进一步延伸穿过第一BSG阶梯109和第一TSG阶梯102。器件100还可以包括沿第一方向设置并定位在第一分隔结构114和第三分隔结构118之间的第二阵列分隔结构(或第二阵列GLS结构)124-127。第二阵列分隔结构124-127可延伸穿过堆叠体进入到衬底中,并进一步延伸穿过第二BSG阶梯111和第二TSG阶梯104。

[0040] 器件100还可以包括定位于第一阵列区100B和第二阵列区100D中的多个沟道结构128。沟道结构128可以延伸穿过堆叠体进入到衬底。沟道结构128中的每个还可以包括沟道层、围绕沟道层的隧道层、围绕隧道层的电荷陷阱层以及围绕电荷陷阱层的阻挡层。此外,沟道结构128可以与字线层直接接触。在一些实施例中,诸如HfO₂或AlO的高K层可以设置在字线层和阻挡层之间。

[0041] 在一些实施例中,可以在图1中形成两个存储块,其中可以在第一分隔结构114和第二分隔结构116之间限定第一存储块,并且可以在第二分隔结构116和第三分隔结构118之间限定第二存储块。例如,如图1所示,第一壁结构106、第一连接阶梯110和BSG阶梯109_1被包括在第一存储块中。第二壁结构108、第二连接阶梯112和BSG阶梯109_2包括在第二存储块中。另外,第一阵列分隔结构120-121和第二阵列分隔结构124-125可以将第一存储块划分成三个子块(或三个指状结构)。第一阵列分隔结构122-123和第二阵列分隔结构126-127可以将第二存储块划分成三个子块(或三个指状结构)。

[0042] 图2是根据本公开的示例性实施例的器件100的三维视图。为了简单和清楚起见,在图2中示出了第一连接区100A、第一阵列区100B和第二连接区100C。在图2中,提供了四个存储块,并且图1中的两个存储块被定位于四个存储块的中间。如图2所示,第一分隔结构114定位于第一连接区100A、第一阵列区100B和第二连接区100C中。第三分隔结构118定位于第一连接区100A、第一阵列区100B和第二连接区100C中。第二分隔结构116沿X方向延伸穿过第一连接区100A、第一阵列区100B和第二连接区100C。分隔结构(例如,第一分隔结构114、第二分隔结构116和第三分隔结构118)可以将器件100划分成多个存储块。例如,图2中示出了四个存储块,其中第一BSG阶梯109被第一分隔结构114、第二分隔结构116和第三分隔结构118分隔成四个阶梯(或四个子BSG阶梯)109_1至109_4。四个阶梯109_1至109_4中的每个可以被包括在相应的存储块中。

[0043] 仍参考图2,第一BSG阶梯109可以形成在一个或多个底部字线层和底部绝缘层中,例如与衬底相邻的最底部字线层和最底部绝缘层。第一TSG阶梯102沿第一阵列区100B定位,并且形成在一个或多个顶部字线层和顶部绝缘层中。第二TSG阶梯104沿第二阵列区100D(未示出)定位,并且也形成在一个或多个顶部字线层和顶部绝缘层中。连接阶梯103定位于第一TSG阶梯102和第二TSG阶梯104之间。连接阶梯103中的每个形成在相应的字线层和绝缘层中。

[0044] 图3是根据本公开的示例性实施例的器件100中的第二TSG阶梯104的放大立体图。如图3所示,第二TSG阶梯104可以通过第二分隔结构116被分成两个TSG阶梯104a和104b。

TSG阶梯104a可以被包括在第一存储块中并且TSG阶梯104b可以被包括在第二存储块中。第二TSG阶梯104可以包括一个或多个梯级,并且每个梯级可以包括相应的一对字线层和绝缘层。在图3的示例性实施例中,第二TSG阶梯104可以包括七个梯级。

[0045] 图4-图11包括根据本公开的示例性实施例的制造3D NAND器件的各种中间步骤的截面图、俯视图和三维视图。如图4所示,提供了半导体结构200(也称为结构200)。半导体结构200可以包括初始堆叠体,该初始堆叠体由衬底101之上的牺牲字线层(或牺牲层)105和绝缘层107形成,如图5所示。可以在结构200上沉积多个掩模层(也称为阻挡层或停止层)202和204。掩模层202可以沿衬底101的Y方向定位,并且掩模层204可以沿衬底101的X方向定位。在一些实施例中,可以基于结构200的被掩模层202覆盖的部分来形成阵列区(例如,第一阵列区100B),并且连接区(例如,第二连接区100C)可以形成在掩模层202之间。另外,可以基于结构200的被掩模层204覆盖的部分来形成壁结构(例如,第一壁结构106)。可以在掩模层202和掩模层204之间的间隙208中形成TSG阶梯(例如,第一TSG阶梯102)。可以在掩模层204之间的间隙210中形成连接阶梯(例如,连接阶梯103)。此外,分隔结构(例如,第一分隔结构114)可以形成在虚线206中。因此,可以通过分隔结构来限定多个存储块。

[0046] 图5是从与包含图4中的线A-A'的垂直平面相同的平面获得的结构200的截面图。如图所示,结构200可以包括交替地设置在衬底101之上的牺牲字线层105和绝缘层107的初始堆叠体。初始堆叠体可以包括与衬底101相邻的最下面的牺牲字线层和最下面的绝缘层。初始堆叠体还可以包括与掩模层202相邻的顶部牺牲字线层和顶部绝缘层。初始堆叠体可以根据3D NAND器件的结构包括任何数量的牺牲字线层和绝缘层。掩模层202可以定位于初始堆叠体的顶表面上。在一些实施例中,在干法蚀刻工艺期间,掩模层202和204可以包括TiN、多晶硅、高K电介质材料或另一种合适的阻挡材料。例如,牺牲字线层105可以由SiN制成,并且绝缘层107可以由SiO制成。可以施加任何合适的制造工艺来形成牺牲字线层105、绝缘层107以及掩模层202和204,诸如化学气相沉积(CVD)工艺、物理气相沉积(PVD)工艺、原子层沉积(ALD)工艺、扩散工艺、溅射工艺或其组合。

[0047] 在图6中,可以沿X方向进行多个修整蚀刻工艺以形成多个阶梯。如图6所示,为了进行修整蚀刻工艺,可以通过还可以包括光致抗蚀剂涂覆(例如,旋转涂覆)、软烘烤、掩模对准、曝光、曝光后烘烤、光致抗蚀剂显影、冲洗、干燥(例如,旋转干燥和/或硬烘烤)、其他合适的光刻技术和/或其组合的光刻工艺(例如,光刻或电子束光刻)在初始堆叠体以及掩模层202和204上形成抗蚀剂层212。抗蚀剂层212可以沿衬底101的Y方向定位并且进一步覆盖掩模层204。在一些实施例中,抗蚀剂层212可以沿X方向依次形成,并且相应地可以沿X方向依次进行修整蚀刻工艺以形成阶梯。在一些实施例中,可以通过光刻工艺同时形成抗蚀剂层212,并且因此可以同时进行修整蚀刻工艺以形成阶梯。

[0048] 图7是连接区(例如,第二连接区100C)中的结构200的三维视图。如图7所示,当修整蚀刻工艺完成时,可以形成多个阶梯。例如,第一TSG阶梯102可以形成在第二连接区100C的与第一阵列区100B(未示出)相邻的第一端,第二TSG阶梯104可以形成在第二连接区100C的相对的第二端,并且多个初始连接阶梯130可以定位于第一TSG阶梯102和第二TSG阶梯104之间。

[0049] 图8是连接区(例如,第二连接区100C)中的结构200的放大的三维视图。如图8所示,初始连接阶梯130可以定位在包括例如第一壁结构106和第二壁结构108的壁结构之间。

初始连接阶梯130可以沿X方向延伸并且定位在第一TSG阶梯102(未示出)和第二TSG阶梯104之间。在一些实施例中,第一TSG阶梯102、初始连接阶梯130和第二TSG阶梯104可以形成一个或多个顶部牺牲字线层和顶部绝缘层中。在图8的实施例中,第一TSG阶梯102、初始连接阶梯130和第二TSG阶梯104可以形成在七对顶部牺牲字线层和顶部绝缘层中。因此,可以在第一TSG阶梯102、初始连接阶梯130中的每个和第二TSG阶梯104中分别形成七个梯级。

[0050] 在一些实施例中,第一TSG阶梯102可以具有沿X方向延伸的梯级,并且第二TSG阶梯104可以具有沿与X方向相反的-X方向延伸的梯级。初始连接阶梯130中的每个可以具有沿X方向延伸的第一组梯级(例如,第一个七个梯级)和沿-X方向延伸的第二组梯级(例如,第二个七个梯级)。

[0051] 在图8的示例中,第一组梯级可以沿X方向具有七个梯级,并且第二组梯级也可以沿-X方向具有七个梯级。应当注意,也可以在一个或多个顶部牺牲字线层和顶部绝缘层中形成第一初始BSG阶梯(未示出)和第二初始BSG阶梯(未示出)。第一初始BSG阶梯可以被定位为与第一阵列区100B相邻,并且第二初始BSG阶梯可以被定位为与第二阵列区100D相邻。

[0052] 随后可以在第一初始BSG阶梯、第二初始BSG阶梯和初始连接阶梯上施加多个去除工艺(或切削工艺)以沿垂直方向(例如Z方向)朝衬底101移动第一初始BSG阶梯、第二初始BSG阶梯和初始连接阶梯。在一些实施例中,去除工艺(或切削工艺)可以是干法蚀刻工艺,例如可以垂直地转移图案的均厚等离子蚀刻工艺。图9A和图9B是示出去除工艺的示意图,该去除工艺用于将第一初始BSG阶梯从初始堆叠体中的一个或多个顶部牺牲字线层和顶部绝缘层移动到一个或多个最底部牺牲字线层和最底部绝缘层。

[0053] 如图9A所示,第一初始BSG阶梯可以定位于第一连接区100A中,并且包括形成在初始堆叠体的七个顶部台阶中的七个梯级(或台阶)。每个梯级/台阶可以包括一对牺牲字线层和绝缘层。如图9B所示,可以在第一初始BSG阶梯上施加多个去除工艺(或切削工艺)以去除第一连接区100A中的牺牲字线层和绝缘层的部分,并且第一初始BSG阶梯的图案可以沿Z方向朝衬底101转移。应当注意的是,当在第一初始BSG阶梯上施加去除工艺时,掩模层(未示出)可以定位在第一阵列区100B之上。

[0054] 在本公开的示例中,第一去除工艺可以去除七个台阶的牺牲字线层和绝缘层。在第一去除工艺之后的第二去除工艺可以去除14个台阶的牺牲字线层和绝缘层。在第二去除工艺之后的第三去除工艺可以去除28个台阶的牺牲字线层和绝缘层。在第三去除工艺之后的第四去除工艺可以去除56个台阶的牺牲字线层和绝缘层。在第四去除工艺之后的第五去除工艺可以去除112个台阶的牺牲字线层和绝缘层。因此,通过施加多个去除工艺,第一初始BSG阶梯可以从初始堆叠体中的一个或多个顶部牺牲字线层和顶部绝缘层移动到一个或多个最底部牺牲字线层和最底部绝缘层。另外,可以在初始连接区上施加去除工艺,从而通过接收适当数量的去除工艺,可以在初始堆叠体的相应牺牲字线层和绝缘层中移动初始连接阶梯130中的每个。

[0055] 图10是在去除工艺完成之后的半导体结构200的三维视图。如图10所示,当去除工艺完成时,可以在第一连接区100A中形成第一BSG阶梯109。另外,第一TSG阶梯102、连接阶梯103和第二TSG阶梯104可以形成在第二连接区100C中。第一BSG阶梯109可以定位于一个或多个底部(例如,最底部)牺牲字线层和底部绝缘层中。第一TSG阶梯102和第二TSG阶梯104可以定位于一个或多个顶部牺牲字线层和顶部绝缘层中。连接阶梯103中的每个可以定

位于相应的牺牲字线层和绝缘层中。因此,第一阵列区100B可以定位于第一BSG阶梯109和第一TSG阶梯102之间。

[0056] 此外,沟道结构(例如,沟道结构128)可以形成在第一阵列区100B和第二阵列区100D(未示出)中。多个GLS沟槽可以形成在半导体结构200中。然后可以用字线层代替牺牲字线层105。例如,可以通过GLS沟槽将湿酸倒入结构200中以去除牺牲字线层105并在绝缘层107之间形成空位。然后字线层可以形成在绝缘层107之间的空位中。字线层可以由诸如W或多晶硅的第一导电材料制成。

[0057] 在一些实施例中,GLS沟槽可以包括沿第一连接区100A、第一阵列区100B、第二连接区100C、第二阵列区100D和第三连接区100E的第一侧延伸的第一GLS沟槽。GLS沟槽可以包括延伸穿过第一连接区100A、第一阵列区100B、第二连接区100C、第二阵列区100D和第三连接区100E的第二GLS沟槽。GLS沟槽还可以包括沿第一连接区100A、第一阵列区100B、第二连接区100C、第二阵列区100D和第三连接区100E的第二侧延伸的第三GLS沟槽。GLS沟槽可以包括第一阵列GLS沟槽,该第一阵列GLS沟槽定位于第一阵列区100B中并且平行于第一GLS沟槽和第二GLS沟槽延伸。GLS沟槽还可以包括第二阵列GLS沟槽,该第二阵列GLS沟槽定位于第二阵列区100D中并且平行于第一GLS沟槽和第二GLS沟槽延伸。

[0058] 然后,可以用诸如多晶硅之类的第二导电材料填充GLS沟槽。因此,可以在第一GLS沟槽中形成第一分隔结构(例如,第一分隔结构114),可以在第二GLS沟槽中形成第二分隔结构(例如,第二分隔结构116),可以在第三GLS沟槽中形成第三分隔结构(例如,第三分隔结构118)。另外,第一阵列分隔结构120-123和第二阵列分隔结构124-127可以分别形成在第一阵列区100B和第二阵列区100D中。

[0059] 在本公开中,随后可以沿垂直方向(例如,Z方向)形成多个字线触点(未示出),其中,字线触点可以从第一TSG阶梯102、第二TSG阶梯104、第一BSG阶梯109、第二BSG阶梯111和连接阶梯103延伸以耦合到字线层。当形成字线触点时,如图10所示,可以基于半导体结构200来形成3D NAND器件100。图10中所示的3D NAND器件100可以具有与图1和图2中所示的3D NAND器件100类似的构造。

[0060] 图11是根据本公开的一些实施例的用于制造所公开的3D NAND器件的工艺1100的流程图。工艺1100开始于步骤S1102,其中可以在3D NAND器件的衬底之上形成牺牲字线层和绝缘层的初始堆叠体。初始堆叠体可以包括沿衬底的第一方向依次设置的第一连接区、第一阵列区和第二连接区。在一些实施例中,步骤S1102可以如参考图4-5所示执行。

[0061] 在步骤S1104,可以在初始堆叠体的第一连接区中形成第一初始阶梯。可以在第一组牺牲字线层和绝缘层中形成第一初始阶梯。在步骤S1106,可以在初始堆叠体的第二连接区中形成第一顶部选择栅(TSG)阶梯。第一TSG阶梯可以形成在第二组牺牲字线层和绝缘层中。在一些实施例中,步骤S1104和S1106可以如参考图6-8所示执行。

[0062] 然后,工艺1100进行到步骤S1108,其中,可以在第一连接区中执行蚀刻工艺,以使第一初始阶梯沿垂直于衬底的垂直方向朝衬底移动,从而形成第一底部选择栅(BSG)阶梯。在一些实施例中,步骤S1108可以如参考图9A、图9B和图10所示执行。

[0063] 应当注意,可以在工艺1100之前、期间和之后提供附加步骤,并且对于工艺1100的附加实施例,可以替换、消除或以不同的依次执行所描述的一些步骤。在步骤S1106,可以在第二连接区中形成多个初始连接阶梯。在步骤S1108,可以通过蚀刻工艺将初始连接阶梯朝

衬底移动以形成连接阶梯,其中连接阶梯中的每个可以形成在相应的牺牲字线层和绝缘层中。

[0064] 另外,可以在形成BSG阶梯和连接阶梯之后形成沟道结构。牺牲字线可以进一步被字线层代替,并且随后可以形成多个分隔结构(或GLS结构)。此外,可以在3D NAND器件的第一和第二接触结构之上形成各种附加的互连结构(例如,具有导线和/或过孔的金属化层)。这样的互连结构将3D NAND器件与其他接触结构和/或有源器件电连接以形成功能电路。也可以形成附加的器件特征,例如钝化层、输入/输出结构等。

[0065] 本文描述的各种实施例提供了优于现有技术的3D NAND器件的若干优点。例如,在现有技术的3D NAND器件中,BSG阶梯和TSG阶梯通常与连接阶梯分开形成。在本公开中,可以通过修整蚀刻工艺同时形成初始BSG阶梯、TSG阶梯和初始连接阶梯。随后可以施加去除工艺(例如,切削工艺)以将初始BSG阶梯移动到一个或多个字线层和绝缘层(例如,最底部字线层和最底部绝缘层),以形成BSG阶梯。该工艺还可以将初始连接阶梯朝衬底移动以形成连接阶梯,其中每个连接阶梯可以形成在堆叠体的相应的字线层和绝缘层中。因此,本发明的方法允许BSG阶梯、TSG阶梯和/或连接阶梯同时形成。本发明的方法既可以获得产量提升,又可以获得成本降低。

[0066] 前述内容概述了几个实施例的特征,使得本领域技术人员可以更好地理解本公开的各方面。本领域技术人员应当理解,他们可以容易地将本公开用作设计或修改其他工艺和结构的基础,以完成与本文介绍的实施例相同的目的和/或实现相同的优点。本领域技术人员还应该认识到,这样的等同构造不脱离本公开的精神和范围,并且本领域技术人员可以在本文中进行各种改变、替换和变更,而不脱离本公开的精神和范围。

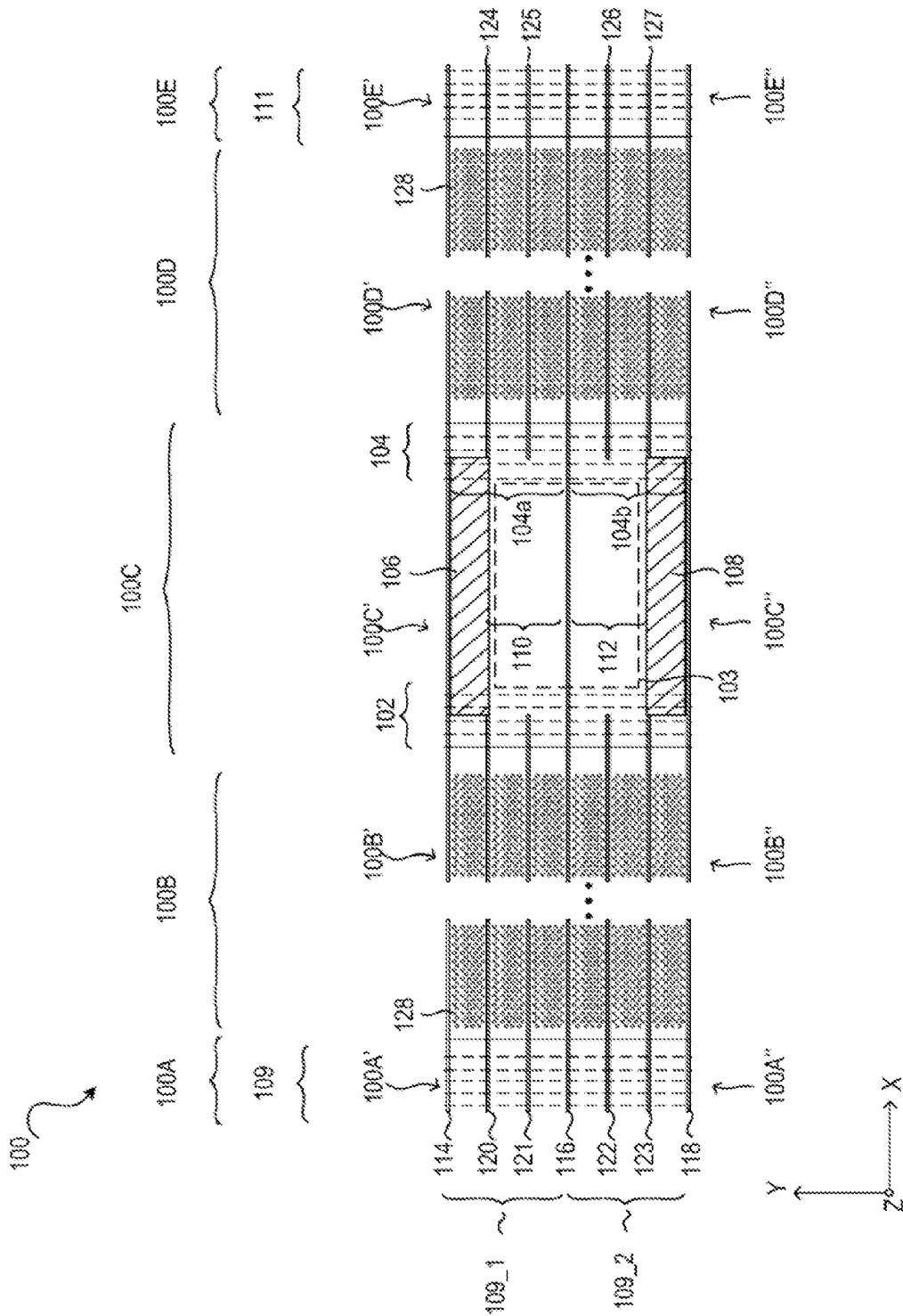


图 1

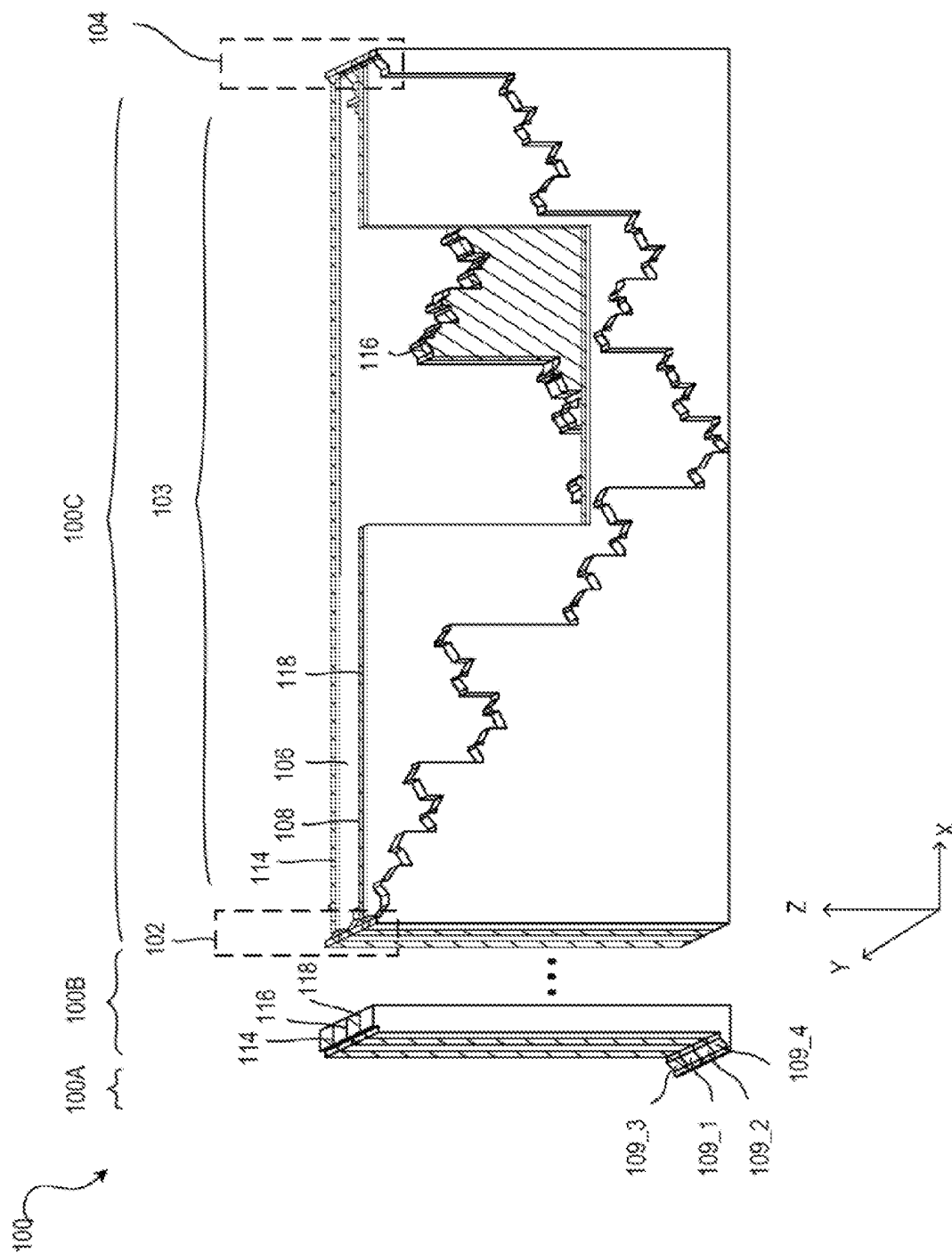


图2

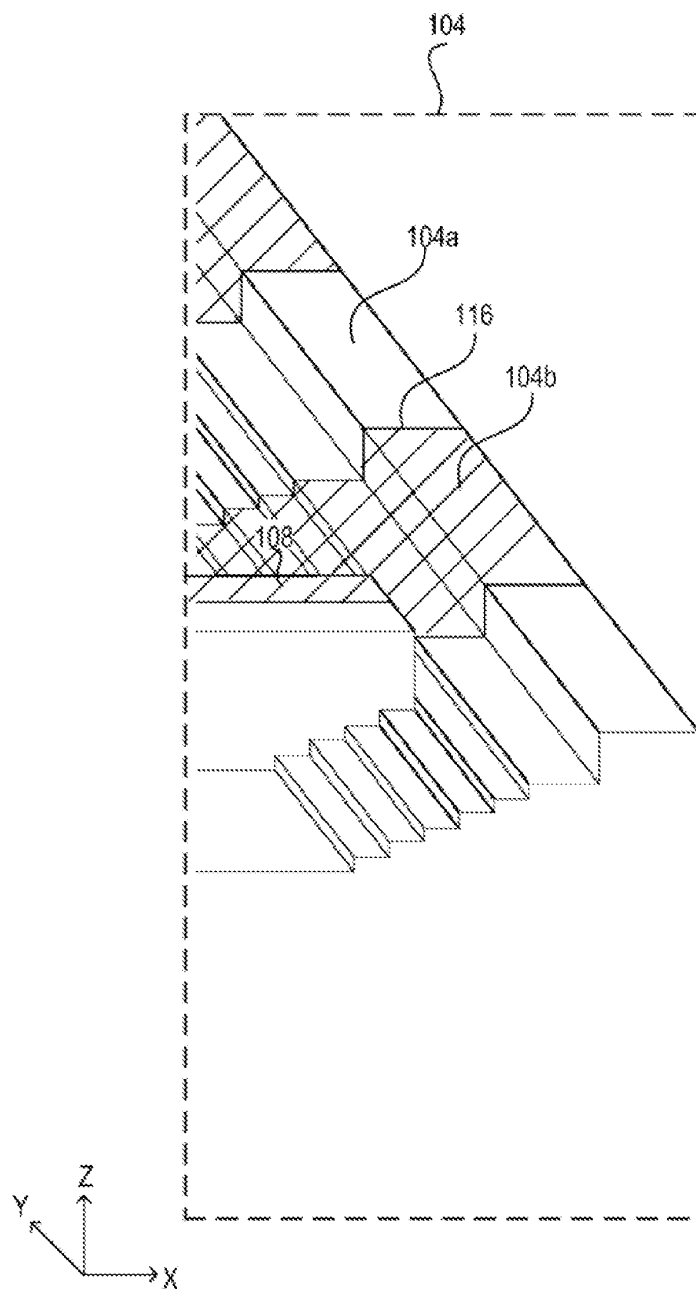


图3

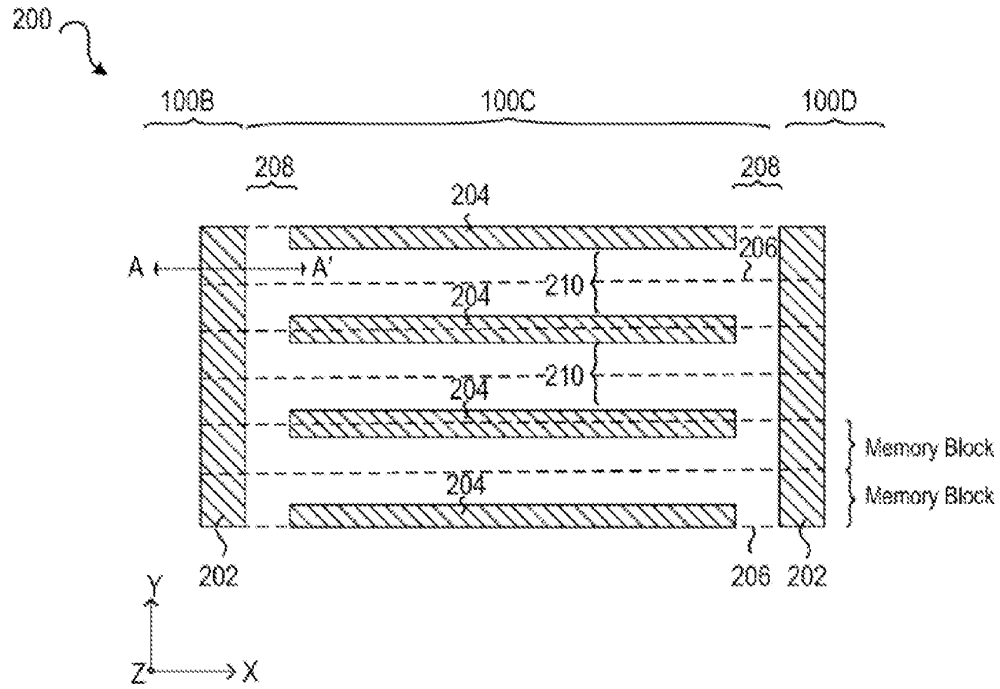


图4

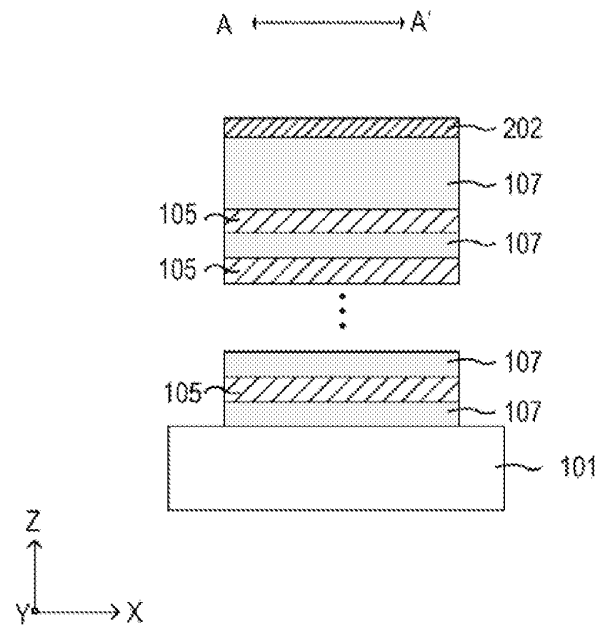


图5

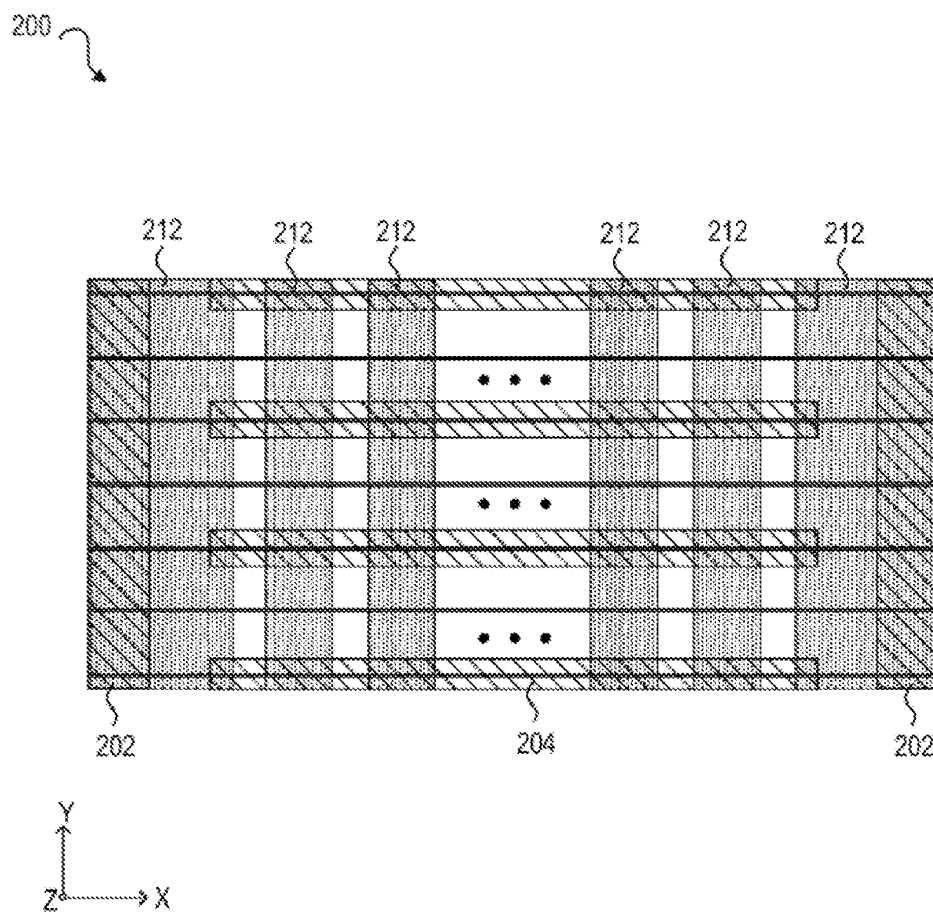


图6

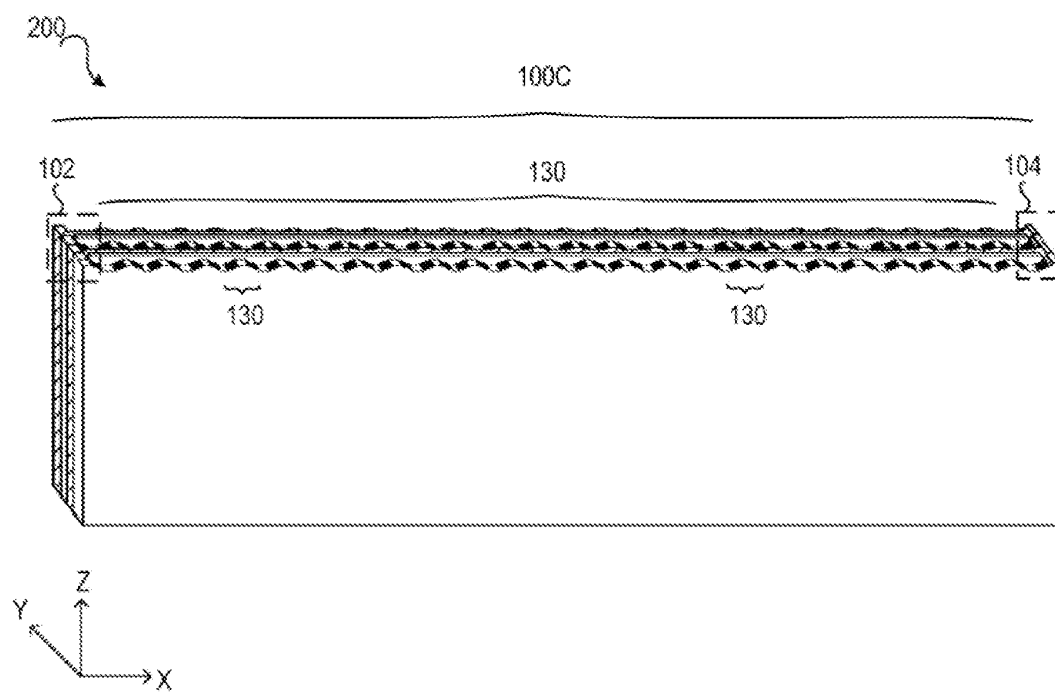


图7

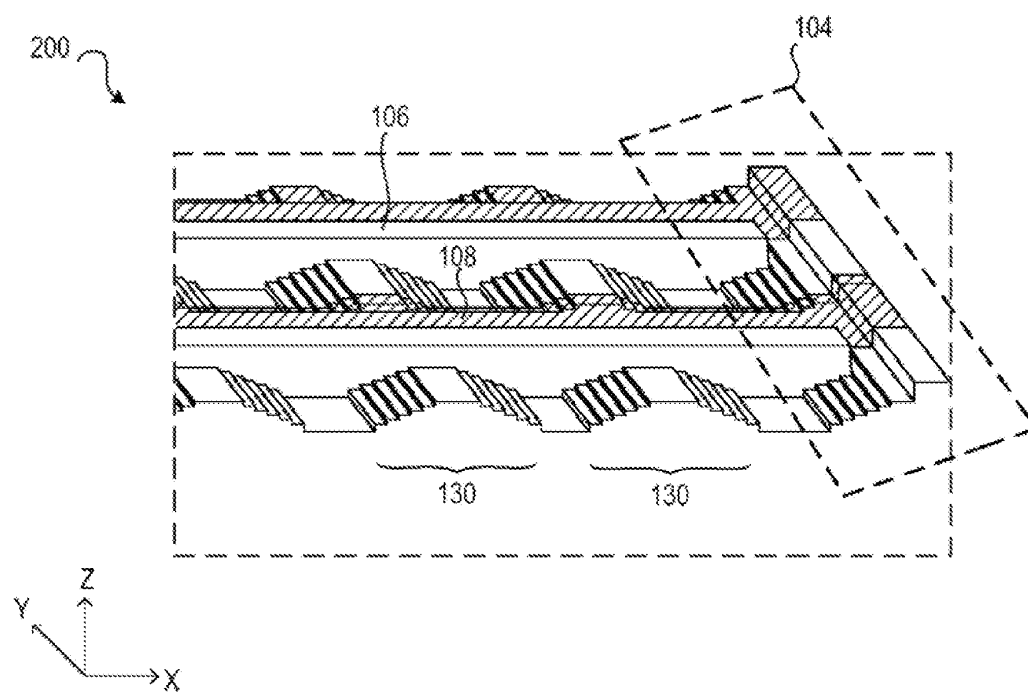


图8

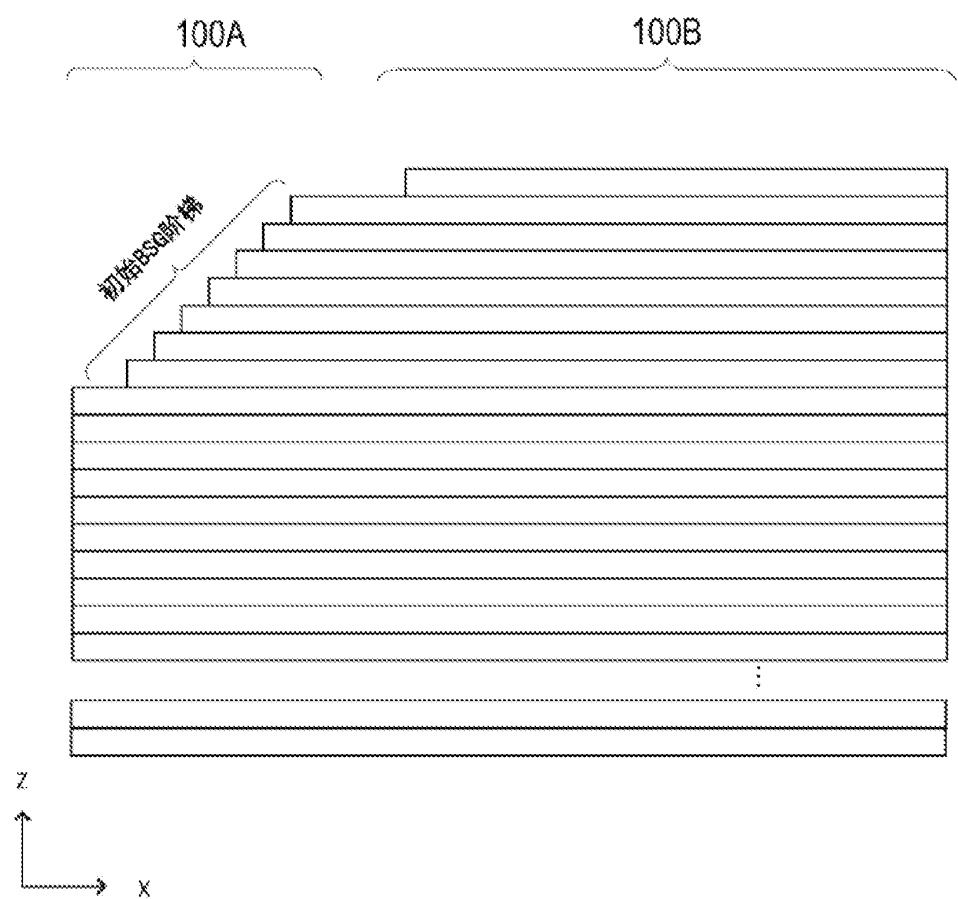


图9A

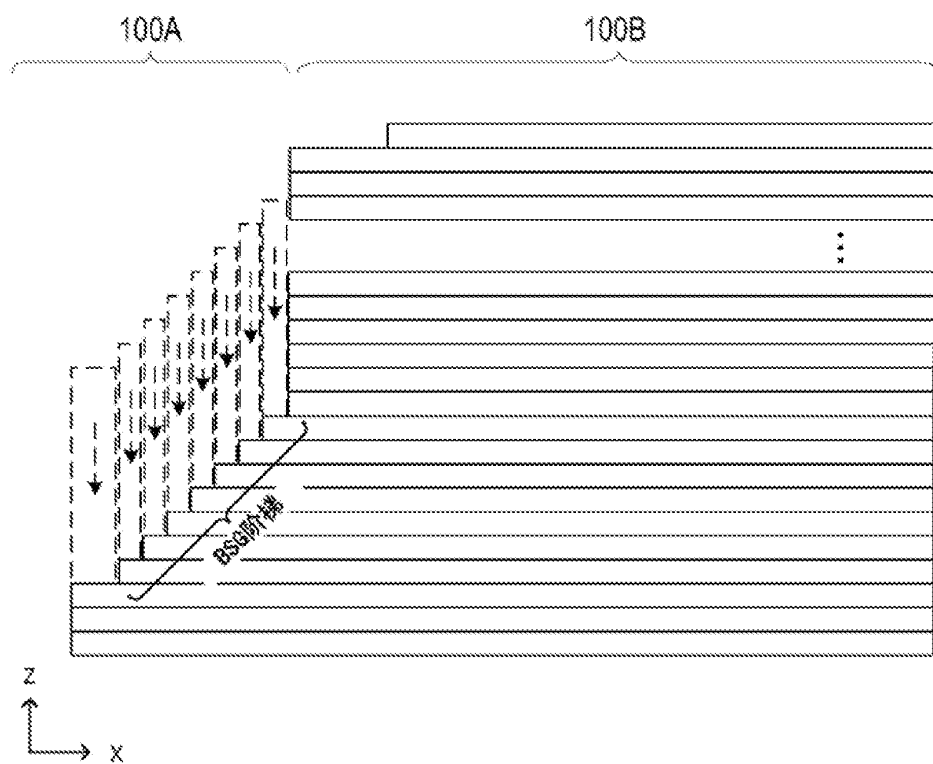


图9B

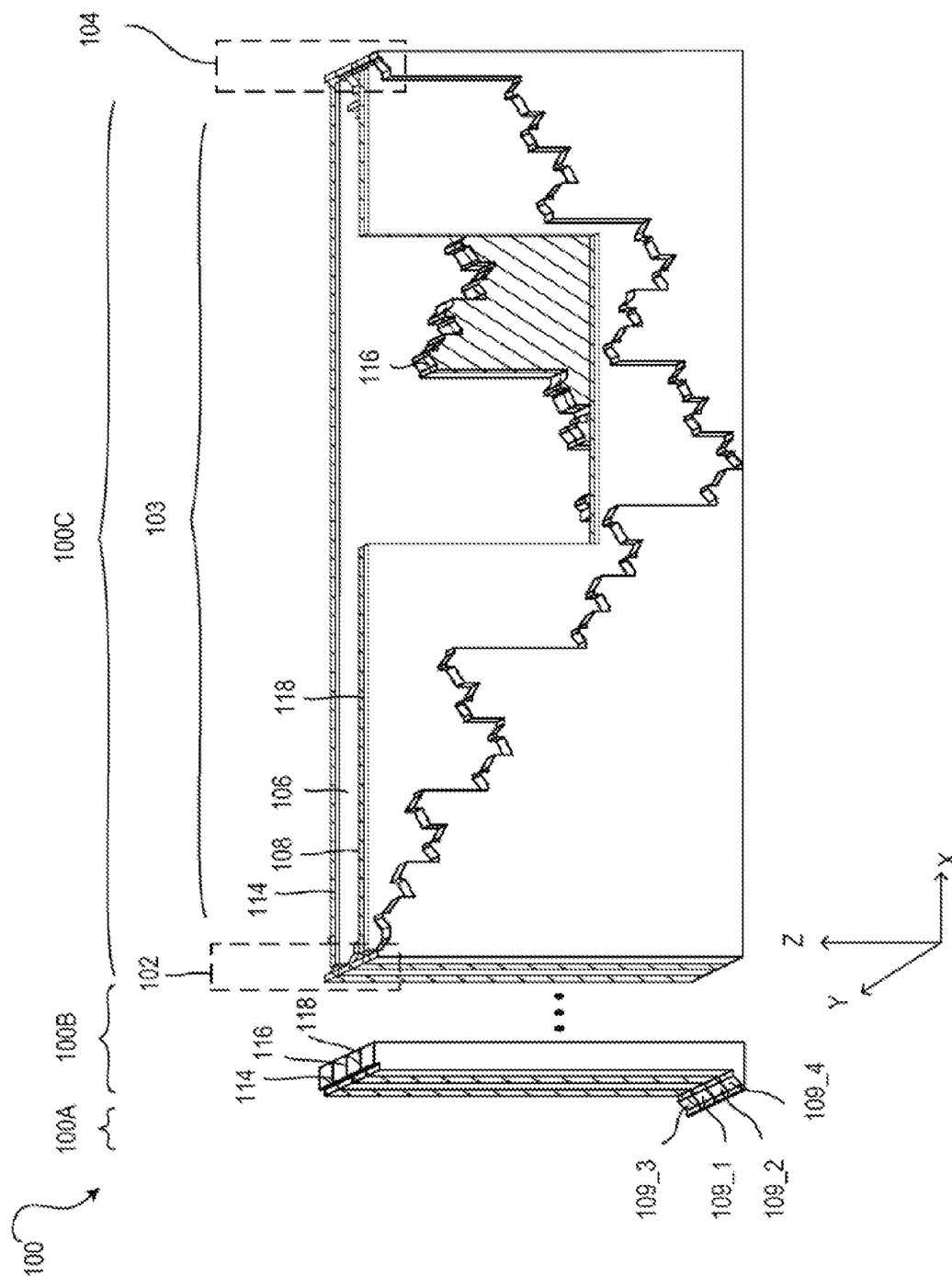


Figure 10

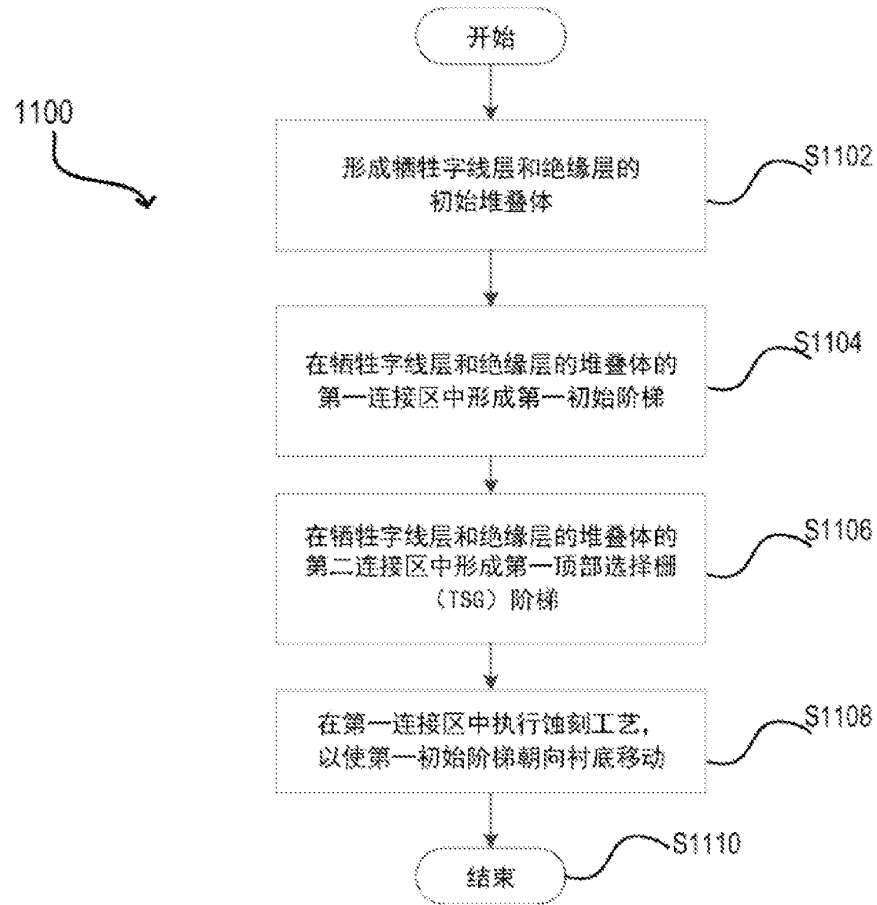


图11



(21)申请号 202080000228.4

H01L 27/11582(2017.01)

(22)申请日 2020.01.21

H01L 27/1157(2017.01)

(85)PCT国际申请进入国家阶段日
2020.03.06

(86)PCT国际申请的申请数据
PCT/CN2020/073438 2020.01.21

(71)申请人 长江存储科技有限责任公司
地址 430223 湖北省武汉市东湖新技术开
发区未来三路88号

(72)发明人 孙中旺 苏睿 周文辉 夏志良

(74)专利代理机构 北京永新新闻知识产权代理
有限公司 11376
代理人 张殿慧 刘健

(51)Int. Cl.
H01L 21/762(2006.01)

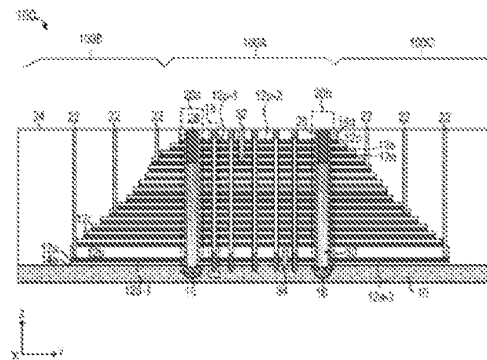
权利要求书3页 说明书14页 附图12页

(54)发明名称

三维NAND存储器件及形成其的方法

(57)摘要

提供了一种半导体器件。所述半导体器件包括交替地堆叠在衬底上的字线层和绝缘层的堆叠。所述半导体器件还包括第一电介质沟槽结构。所述第一电介质沟槽结构被放置在所述字线层中的底部选择栅(BSG)层中以分隔所述BSG层并且在衬底的第一方向上延伸。所述半导体器件还包括第二电介质沟槽结构。所述第二电介质沟槽结构被放置在所述字线层中的顶部选择栅(TSG)层中以分隔所述TSG层并且在所述衬底的所述第一方向上延伸。所述第二电介质沟槽结构在垂直于所述第一方向的所述衬底的第二方向上与所述第一电介质沟槽结构偏离。



1. 一种半导体器件, 包括:
交替地堆叠在衬底上的字线层和绝缘层的堆叠;
被放置在所述字线层中的底部选择栅 (BSG) 层中以分隔所述BSG层并且在所述衬底的第一方向上延伸的第一电介质沟槽结构; 以及
被放置在所述字线层中的顶部选择栅 (TSG) 层中以分隔所述TSG层并且在所述衬底的所述第一方向上延伸的第二电介质沟槽结构, 所述第二电介质沟槽结构在垂直于所述第一方向的所述衬底的第二方向上与所述第一电介质沟槽结构偏离。
2. 根据权利要求1所述的半导体器件, 还包括:
被放置在所述堆叠的第一边界处的第一缝隙结构, 所述第一缝隙结构贯穿所述堆叠地延伸并且沿所述衬底的所述第一方向延伸; 以及
被放置在所述堆叠的第二边界处的第二缝隙结构, 所述第二缝隙结构贯穿所述堆叠地延伸并且沿所述衬底的所述第一方向延伸。
3. 根据权利要求2所述的半导体器件, 其中, 所述第一电介质沟槽结构和所述第二电介质沟槽结构在所述衬底的所述第二方向上被安排在所述第一缝隙结构和所述第二缝隙结构之间。
4. 根据权利要求3所述的半导体器件, 其中, 所述第一电介质沟槽结构、所述第二电介质沟槽结构、所述第一缝隙结构和所述第二缝隙结构在所述衬底的所述第一方向上平行于彼此地延伸。
5. 根据权利要求4所述的半导体器件, 还包括:
被形成在所述衬底上并且还贯穿所述堆叠地延伸的多个沟道结构, 所述沟道结构被安排在所述第一缝隙结构和所述第二缝隙结构之间。
6. 根据权利要求5所述的半导体器件, 还包括:
被形成在所述衬底上并且还贯穿所述堆叠地延伸的多个虚拟沟道结构, 所述虚拟沟道结构被安排在所述第一缝隙结构和所述第二缝隙结构之间。
7. 根据权利要求6所述的半导体器件, 其中, 所述第一电介质沟槽结构跨越所述虚拟沟道结构的第一集合地延伸, 并且所述第二电介质沟槽结构跨越所述虚拟沟道结构的第二集合地延伸。
8. 根据权利要求7所述的半导体器件, 其中, 所述TSG层是所述字线层中的最高的字线层。
9. 根据权利要求8所述的半导体器件, 其中, 所述BSG层是所述字线层中的最低的字线层。
10. 根据权利要求9所述的半导体器件, 还包括:
由所述第一缝隙结构和所述第二电介质沟槽结构定义的第一区域;
由所述第一电介质沟槽结构和所述第二电介质沟槽结构定义的第二区域; 以及
由所述第一电介质沟槽结构和所述第二缝隙结构定义的第三区域, 其中, 所述第一区域、所述第二区域和所述第三区域被配置为独立地操作。
11. 根据权利要求10所述的半导体器件, 其中, 所述沟道结构和所述虚拟沟道结构沿所述衬底的所述第二方向被布置在14行中。
12. 一种用于制造半导体器件的方法, 包括:

在衬底上形成多个第一绝缘层和虚拟底部选择栅 (BSG) 层,所述虚拟BSG层被安排在所述第一绝缘层之间;

形成贯穿所述虚拟BSG层并且在所述衬底的第一方向上延伸的第一电介质沟槽结构,所述虚拟BSG层被所述第一电介质沟槽结构分隔;

在所述第一绝缘层上形成多个牺牲字线层和多个第二绝缘层,所述第二绝缘层和所述牺牲字线层被交替地安排;以及

形成贯穿所述牺牲字线层中的牺牲顶部选择栅 (TSG) 层以分隔所述牺牲TSG层并且在所述衬底的所述第一方向上延伸的第二电介质沟槽结构,所述第二电介质沟槽结构在所述衬底的第二方向上与所述第一电介质沟槽结构偏离。

13. 根据权利要求12所述的方法,在所述形成所述第二电介质沟槽结构之前,所述方法还包括:

在所述第一绝缘层、所述虚拟BSG层、所述牺牲字线层和所述第二绝缘层上执行修剪蚀刻过程以在所述衬底上形成阵列区和阶梯区,所述阶梯区被放置在所述阵列区的两侧处。

14. 根据权利要求13所述的方法,还包括:

在所述阵列区中形成沟道结构,所述沟道结构从所述衬底开始延伸,并且贯穿所述第一绝缘层、所述虚拟BSG层、所述牺牲字线层和所述第二绝缘层地延伸;

形成被放置在所述阵列区和所述阶梯区的第一边界处的第一缝隙结构和被放置在所述阵列区和所述阶梯区的第二边界处的第二缝隙结构,所述第一缝隙结构和所述第二缝隙结构贯穿所述第一绝缘层、所述虚拟BSG层、所述牺牲字线层和所述第二绝缘层地延伸,并且还沿所述衬底的所述第一方向延伸;

用BSG层替换所述虚拟BSG层,以及用字线层替换所述牺牲字线层;以及

在所述阶梯区上形成触点结构,所述触点结构被连接到所述阶梯区中的所述BSG层和所述字线层。

15. 根据权利要求14所述的方法,其中,所述第一电介质沟槽结构和所述第二电介质沟槽结构在所述衬底的所述第二方向上被安排在所述第一缝隙结构和所述第二缝隙结构之间。

16. 根据权利要求14所述的方法,其中,所述第一电介质沟槽结构、所述第二电介质沟槽结构、所述第一缝隙结构和所述第二缝隙结构在所述衬底的所述第一方向上平行于彼此地延伸。

17. 一种半导体器件,包括:

包括交替地堆叠在衬底上的字线层和绝缘层的堆叠;

被放置在所述堆叠的第一边界处的第一缝隙结构,所述第一缝隙结构贯穿所述堆叠并且沿所述衬底的第一方向延伸;

被放置在所述堆叠的第二边界处的第二缝隙结构,所述第二缝隙结构贯穿所述堆叠并且沿所述衬底的所述第一方向延伸;

被安排在所述第一缝隙结构和所述第二缝隙结构之间、被放置在所述字线层中的底部选择栅 (BSG) 层中以分隔所述BSG层,并且在所述衬底的所述第一方向上延伸的第一电介质沟槽结构;以及

被安排在所述第一缝隙结构和所述第二缝隙结构之间、被放置在所述字线层中的顶部

选择栅 (TSG) 层中以分隔所述TSG层并且在所述衬底的所述第一方向上延伸的第二电介质沟槽结构,所述第二电介质沟槽结构在所述衬底的第二方向上与所述第一电介质沟槽结构偏离。

18.根据权利要求17所述的半导体器件,其中,所述第一电介质沟槽结构、所述第二电介质沟槽结构、所述第一缝隙结构和所述第二缝隙结构在所述衬底的所述第一方向上平行于彼此地延伸。

19.根据权利要求17所述的半导体器件,还包括:

被形成在所述衬底上并且还贯穿所述堆叠中的所述字线层和所述绝缘层地延伸的多个沟道结构;以及

被形成在所述衬底上并且还贯穿所述堆叠中的所述字线层和所述绝缘层地延伸的多个虚拟沟道结构,所述第一电介质沟槽结构跨越所述虚拟沟道结构的第一集合地延伸,并且所述第二电介质沟槽结构跨越所述虚拟沟道结构的第二集合地延伸。

20.根据权利要求19所述的半导体器件,其中,所述沟道结构和所述虚拟沟道结构沿所述衬底的所述第二方向被布置在14行中。

三维NAND存储器件及形成其的方法

背景技术

[0001] 随着集成电路中的器件的临界尺寸缩小到常见存储单元技术的极限,设计人员已经在展望用于存储单元的堆叠的多个片存储区以达到更大的存储容量和达到更低的每比特成本的技术。3D-NAND存储器件是一种存储单元的堆叠的多个片存储区以达到更大的存储容量和达到更低的每比特成本的示例性器件。随着3D NAND技术向更高密度和大容量迁移,特别是从64L向128L架构迁移,垂直于衬底的纵向上的字线层(或者栅控制层)的数量已经在显著增长。增长的字线层数量引起3D-NAND存储器件的块大小的急剧增长,这接着可以导致更长的读和擦除时间、更长的数据传输时间和更低的存储效率。

发明内容

[0002] 根据本公开内容的一个方面,提供了一种半导体器件。所述半导体器件包括交替地堆叠在衬底上的字线层和绝缘层的堆叠。所述半导体器件还包括第一电介质沟槽结构。所述第一电介质沟槽结构被放置在所述字线层中的底部选择栅(BSG)层中以将所述BSG层分隔成两个部分,并且在衬底的第一方向上延伸。所述半导体器件进一步包括第二电介质沟槽结构。所述第二电介质沟槽结构被放置在所述字线层中的顶部选择栅(TSG)层中以将所述TSG层分隔成两个部分,并且在所述衬底的所述第一方向(例如,长度方向)上延伸。所述第二电介质沟槽结构在垂直于所述第一方向的所述衬底的第二方向(例如,宽度方向)上与所述第一电介质沟槽结构偏离。

[0003] 所述半导体器件可以包括第一缝隙结构和第二缝隙结构。所述第一缝隙结构可以被放置在所述堆叠的第一边界处,其中,所述第一缝隙结构贯穿所述堆叠地延伸,并且沿所述衬底的所述第一方向延伸。所述第二缝隙结构可以被放置在所述堆叠的第二边界处,其中,所述第二缝隙结构贯穿所述堆叠地延伸,并且沿所述衬底的所述第一方向延伸。

[0004] 在一些实施例中,所述第一电介质沟槽结构和所述第二电介质沟槽结构可以在所述衬底的所述第二方向上被安排在所述第一缝隙结构和所述第二缝隙结构之间。另外,所述第一电介质沟槽结构、所述第二电介质沟槽结构、所述第一缝隙结构和所述第二缝隙结构可以在所述衬底的所述第一方向上平行于彼此地延伸。

[0005] 所述半导体器件可以包括被形成在所述衬底上并且进一步贯穿所述堆叠地延伸的多个沟道结构,其中,所述沟道结构被安排在所述第一缝隙结构和所述第二缝隙结构之间。所述半导体器件可以进一步包括被形成在所述衬底上并且进一步贯穿所述堆叠地延伸的多个虚拟沟道结构,其中,所述虚拟沟道结构被安排在所述第一缝隙结构和所述第二缝隙结构之间。

[0006] 在一些实施例中,所述第一电介质沟槽结构跨越所述虚拟沟道结构的第一集合地延伸,并且所述第二电介质沟槽结构跨越所述虚拟沟道结构的第二集合地延伸。

[0007] 在一些实施例中,所述TSG层可以是所述字线层中的最高的字线层,并且所述BSG层可以是所述字线层中的最低的字线层。

[0008] 在一些实施例中,所述半导体器件可以包括第一区域、第二区域和第三区域。所述

第一区域由所述第一缝隙结构和所述第二电介质沟槽结构定义的。所述第二区域由所述第一电介质沟槽结构和所述第二电介质沟槽结构定义。所述第三区域由所述第一电介质沟槽结构和所述第二缝隙结构定义。所述第一区域、所述第二区域和所述第三区域被配置为独立地操作。

[0009] 根据本公开内容的另一个方面,提供了一种用于制造半导体器件的方法。在所公开的方法中,在衬底上形成多个第一绝缘层和虚拟底部选择栅(BSG)层。所述虚拟BSG层被安排在所述第一绝缘层之间。随后形成第一电介质沟槽结构。所述第一电介质沟槽结构贯穿所述虚拟BSG层,并且在所述衬底的第一方向(例如,长度方向)上延伸。所述虚拟BSG层被所述第一电介质沟槽结构分隔成两个部分。然后在所述第一绝缘层上形成多个牺牲字线层和多个第二绝缘层,其中,所述第二绝缘层和所述牺牲字线层被交替地安排。进一步地,形成第二电介质沟槽结构,其中,所述第二电介质沟槽结构贯穿所述牺牲字线层中的牺牲顶部选择栅(TSG)层以将所述牺牲TSG层分隔成两个部分,并且在所述衬底的所述第一方向上延伸。所述第二电介质沟槽结构在所述衬底的第二(或者宽度)方向上与所述第一电介质沟槽结构偏离。

[0010] 在一些实施例中,在形成所述第二电介质沟槽结构之前,可以在所述第一绝缘层、所述虚拟BSG层、所述牺牲字线层和所述第二绝缘层上执行修剪蚀刻过程以在所述衬底上形成阵列区和阶梯区,其中,所述阶梯区被放置在所述阵列区的两侧处。

[0011] 在一些实施例中,可以在所述阵列区中形成沟道结构,其中,所述沟道结构从所述衬底开始延伸,并且贯穿所述第一绝缘层、所述虚拟BSG层、所述牺牲字线层和所述第二绝缘层地在所述阵列区中延伸。此外,可以将第一缝隙结构形成为被放置在所述阵列区和所述阶梯区的第一边界处,并且可以将第二缝隙结构形成为被放置在所述阵列区和所述阶梯区的第二边界处。所述第一缝隙结构和所述第二缝隙结构贯穿所述第一绝缘层、所述虚拟BSG层、所述牺牲字线层和所述第二绝缘层地延伸,并且进一步沿所述衬底的所述第一方向延伸。随后,可以用BSG层替换所述虚拟BSG层,并且可以用字线层替换所述牺牲字线层。可以在所述阶梯区上形成触点结构,其中,所述触点结构被连接到所述阶梯区中的所述BSG层和所述字线层。

[0012] 在所公开的方法中,所述第一电介质沟槽结构和所述第二电介质沟槽结构在所述衬底的所述第二方向上被安排在所述第一缝隙结构和所述第二缝隙结构之间。另外,所述第一电介质沟槽结构、所述第二电介质沟槽结构、所述第一缝隙结构和所述第二缝隙结构在所述衬底的所述第一方向上平行于彼此地延伸。

[0013] 根据本公开内容的又另一个方面,提供了一种半导体器件。所述半导体器件包括被形成在堆叠中的阵列区和阶梯区,其中,所述阶梯区被放置在所述阵列区的两侧处,并且所述堆叠包括交替地堆叠在衬底上的字线层和绝缘层。所述半导体器件包括第一缝隙结构和第二缝隙结构。所述第一缝隙结构被放置在所述阵列区和所述阶梯区的第一边界处,并且贯穿所述堆叠并且沿所述衬底的第一(或者长度)方向延伸。所述第二缝隙结构被放置在所述阵列区和所述阶梯区的第二边界处,并且贯穿所述堆叠并且沿所述衬底的所述第一方向延伸。

[0014] 所述半导体器件进一步具有第一电介质沟槽结构和第二电介质沟槽结构。所述第一电介质沟槽结构被安排在所述第一和第二缝隙结构之间、被放置在所述字线层中的底部

选择栅 (BSG) 层中以将所述BSG层分隔成两个部分并且在所述衬底的所述第一方向上延伸。所述第二电介质沟槽结构被安排在所述第一和第二缝隙结构之间、被放置在所述字线层中的顶部选择栅 (TSG) 层中以将所述TSG层分隔成两个部分并且在所述衬底的所述第一方向上延伸。所述第二电介质沟槽结构在所述衬底的第二方向上与所述第一电介质沟槽结构偏离。

[0015] 在一些实施例中,所述第一电介质沟槽结构、所述第二电介质沟槽结构、所述第一缝隙结构和所述第二缝隙结构在所述衬底的所述第一方向上平行于彼此地延伸。

[0016] 在一些实施例中,所述半导体器件包括多个沟道结构和多个触点结构。所述沟道结构被形成在所述衬底上并且进一步贯穿所述堆叠的所述阵列区中的所述字线层和所述绝缘层地延伸。所述触点结构被形成在所述阶梯区上,并且被连接到所述阶梯区中的所述字线层。

[0017] 所述半导体器件进一步包括多个虚拟沟道结构。所述虚拟沟道结构被形成在所述衬底上并且进一步贯穿所述堆叠的所述阵列区中的所述字线层和所述绝缘层地延伸,其中,所述第一电介质沟槽结构跨越所述虚拟沟道结构的第一集合地延伸,并且所述第二电介质沟槽结构跨越所述虚拟沟道结构的第二集合地延伸。

附图说明

[0018] 在结合附图阅读时,从以下详细描述内容中最好地理解本公开内容的方面。应当指出,根据产业中的标准实践,各种特征不是按比例绘制的。实际上,为了讨论的清楚性,可以增大或者减小各种特征的尺寸。

[0019] 图1A是根据本公开内容的示例性实施例的一个示例性3D-NAND存储器件的横截面图。

[0020] 图1B是根据本公开内容的示例性实施例的一个示例性3D-NAND存储器件的俯视图。

[0021] 图1C是根据本公开内容的示例性实施例的一个示例性3D-NAND存储器件的三维视图。

[0022] 图2是根据本公开内容的示例性实施例的一个示例性3D-NAND存储器件中的沟道结构的横截面图。

[0023] 图3A是第一3D-NAND存储器件的俯视图。

[0024] 图3B是第二3D-NAND存储器件的俯视图。

[0025] 图4A、4B、5、6、7A、7B、8A、8B、9A、9B和10是制造根据本公开内容的示例性实施例的一个示例性3D-NAND存储器件的各种中间步骤的横截面图和俯视图。

[0026] 图11是用于制造根据本公开内容的示例性实施例的一个示例性3D-NAND存储器件的过程的流程图。

具体实施方式

[0027] 以下公开内容提供用于实现所提供的主题的不同特征的许多不同的实施例或者示例。下面描述部件和安排的具体的示例以简化本公开内容。当然,这些仅是示例,而不旨在是限制性的。例如,随后的描述内容中的在第二特征之上或者上面形成第一特征可以包

括在其中第一和第二特征是被形成的可以有直接接触的特征的实施例,并且还可以包括在其中可以在第一和第二特征之间形成额外的特征以使得第一和第二特征可以没有直接接触的实施例。另外,本公开内容可以在各种示例中重复标号和/或字母。该重复是出于简单和清楚的目的,并且其自身不指示所讨论的各种实施例和/或配置之间的关系。

[0028] 进一步地,为了易于描述,可以在本文中使用空间相对术语(诸如“在……之下”、“在……下面”、“较低”、“在……上面”、“较高”等)以便描述如附图中说明的一个元素或者特征与另一个(些)元素或者特征的关系。除了附图中描绘的朝向之外,空间相对术语旨在还包括处在使用或者操作中的设备的不同的朝向。装置可以被另外地定向(被旋转90度或者被定向在其它的朝向处),并且同样可以相应地解释本文中使用的空间相对描述语。

[0029] 概念涉及例如3D-NAND存储器件的形成,所述3D-NAND存储器件具有经划分的存储块结构,并且所述经划分的存储块结构中的每个经划分的存储块结构可以被独立地操作(例如,编程、擦除或者读)。

[0030] 一个3D-NAND存储器件可以包括多个存储单元存储块(或者存储块)。存储块中的每个存储块可以包括多个纵向NAND存储单元串。纵向NAND存储单元串中的每个纵向NAND存储单元串可以具有沿衬底的高度方向(或者Z方向)被顺序地并且连续地安排在衬底上的一个或多个底部选择晶体管(BST)、一个或多个虚拟BST、多个存储单元(MC)、一个或多个虚拟顶部选择晶体管(TST)以及一个或多个TST。纵向NAND存储单元串中的每个纵向NAND存储单元串中的最低的BST的源区被连接到共源极线(CSL),并且纵向NAND存储单元串中的每个纵向NAND存储单元串中的最高的TST的漏区被连接到分别的位线。在3D-NAND存储器件中,同一个存储块的纵向NAND存储单元串可以共享一个或多个顶部选择栅(TSG)。被共享的一个或多个TSG相应地在操作相关的3D-NAND存储器件(诸如对3D-NAND存储器件进行编程或者读取)期间同时控制相同的存储块中的纵向NAND存储单元串的TST。

[0031] 在3D-NAND存储器件中,相同的存储块的纵向NAND存储单元串可以共享一个或多个底部选择栅(BSG)。被共享的一个或多个BSG相应地在操作3D-NAND存储器件(诸如擦除3D-NAND存储器件)期间同时控制相同的存储块中的纵向NAND存储单元串的BST。随着3D-NAND存储器件向具有增大的存储块大小的更高容量迁移,被共享的一个或多个TSG或者BSG可以导致更长的操作时间、更长的数据传输时间和更低的存储效率。

[0032] 在相关3D-NAND存储器件中,可以通过利用一个或多个电介质沟槽结构将一个或多个被共享的TSG划分成多个子TSG来将一个存储块分隔成多个子存储块。可以独立地操作子存储块以使得可以相应地减少操作时间和数据传输时间。在第一示例中,可以应用一个电介质沟槽结构以将存储块分隔成两个子存储块。然而,这样的配置可能导致产生低的存储单元密度。在第二示例中,可以应用两个电介质沟槽结构以将存储块分隔成三个子存储块。然而,两个电介质沟槽结构之间的子存储块可能不起作用,这是因为不可以例如如下面就图3B描述的那样用字线层替换该子存储块中的牺牲字线层。

[0033] 在所公开的3D-NAND存储器件中,一个存储块可以具有被放置在底部选择栅(BSG)层中的用于将BSG层分隔成两个部分的第一电介质沟槽结构和被放置在顶部选择栅(TSG)层中的用于将TSG层分隔成两个部分的第二电介质沟槽结构。第二电介质沟槽结构是与第一电介质沟槽结构偏离的。所公开的配置通过将存储块划分成三个独立的并且起作用的子存储块而允许存储块中的更高的沟道结构密度。

[0034] 图1A是一个示例性3D-NAND存储器件100的横截面图,以及图1B是示例性3D-NAND存储器件100的俯视图,其中,图1A中的3D-NAND存储器件100的横截面图是从图1B中的沿衬底的Z方向(或者高度方向)的线A-A'获得的。图1B中的虚线指示透视图。图1C是示例性3D-NAND存储器件100的3D视图。为了简单和清楚起见,在图1A、1B和1C中提供了3D-NAND存储器件100的仅一个存储块。

[0035] 如在图1A中示出的,3D-NAND存储器件100可以具有衬底10。多个字线层和多个绝缘层被交替地堆叠在衬底10上。在图1A的示例性实施例中,包括了16个字线层和17个绝缘层。然而,图1A仅是一个示例,并且可以基于器件结构包括任意数量的字线层和绝缘层。在一些实施例中,最低字线层12a可以充当被连接到BST的栅极的底部选择栅(BSG)层。在一些实施例中,BSG层12a之上的字线层中的一个或多个字线层(诸如字线层12b-12c)可以是被连接到虚拟存储单元(虚拟MC)的栅极的虚拟字线层(或者虚拟BSG层)。BST和虚拟MC一起可以控制阵列共源(ACS)区16与存储单元之间的数据传输。在一些实施例中,最高字线层12p可以充当被连接到TST的栅极的顶部选择栅(TSG)层。在一些实施例中,TSG层12p之下的字线层中的一个或多个字线层(诸如字线层12n-12o)可以是被连接到虚拟存储单元(虚拟MC)的栅极的虚拟字线层(或者虚拟TSG层)。TST和虚拟MC一起控制位线(未示出)与存储单元之间的数据传输。

[0036] 绝缘层被放置在衬底10上,并且与字线层交替地被布置。通过绝缘层将字线层与彼此分隔开。另外,通过绝缘层中的最低绝缘层14a将字线层与衬底10分隔开。

[0037] 在一些实施例中,首先使用牺牲字线层(例如,SiN)形成图1A中说明的字线层。可以移除并且用高K层、粘合层和一个或多个金属层替换牺牲字线层。高K层可以由氧化铝(Al_2O_3)和/或氧化铪(HfO_2)和/或氧化钽(Ta_2O_5)和/或另一种高K(介电常数)材料制成的。金属层可以由例如钨(W)、钴(Co)制成的。根据产品规范、设备操作、制造能力等的要求,字线可以具有从10nm到100nm的范围中的厚度。在图1A的实施例中,绝缘层可以由具有从5nm到50nm的厚度的 SiO_2 制成的。

[0038] 在一些实施例中,3D-NAND存储器件100可以具有阵列区100A和两个阶梯区100B-100C。阶梯区100B-100C可以被放置在阵列区100A的两侧处。字线层和绝缘层可以延伸到阶梯区100B-100C中,具有阶梯式剖面或者步梯式剖面。

[0039] 3D-NAND存储器件100可以包括阵列区100A中的多个沟道结构18。沟道结构18沿衬底的Z方向(或者高度方向)被形成在衬底10上。如图1A中示出的,包括了五个沟道结构18。然而,图1A仅是一个示例,并且可以在3D-NAND存储器件100中包括任意数量的沟道结构18。沟道结构18可以贯穿字线层和绝缘层地延伸,并且进一步延伸到衬底10中以形成纵向存储单元串的阵列。纵向存储单元串中的每个纵向存储单元串可以包括相对应的沟道结构,所述相对应的沟道结构被耦合到字线层以形成一个或多个底部选择晶体管(BSG)、多个存储单元(MC)和一个或多个顶部选择晶体管(TST)。BST、MC和TST被顺序地并且连续地安排在衬底上。另外,沟道结构18中的每个沟道结构18可以进一步包括沟道层、隧穿层、电荷捕获层和阻隔层,这在图3中被进一步详细地示出。

[0040] 3D-NAND存储器件100可以具有多个缝隙结构。例如,在图1A中包括两个缝隙结构20a-20b。在一些实施例中,使用后栅极制造技术来形成3D-NAND存储器件100,因此,形成缝隙结构以辅助移除牺牲字线层和形成真正的栅极。在一些实施例中,缝隙结构可以由导

电材料制成的并且被放置在阵列共源(ACS)区16上以充当触点,其中,ACS区被形成在衬底10上以充当共源极。在一些实施例中,缝隙结构可以是由电介质材料制成的以充当分隔结构。在图1A的示例性实施例中,缝隙结构20a-20b被放置在阵列区100A的两个相对的边界处,并且被连接到ACS区16。

[0041] 在一些实施例中,缝隙结构20a-20b可以贯穿字线层和绝缘层地延伸,并且进一步沿衬底10的第一方向(也被称为长度方向或者X方向)延伸。在一些实施例中,缝隙结构20a-20b可以具有电介质间隙壁26、导电层30和触点28。电介质间隙壁26沿缝隙高度的侧壁被形成,并且与字线层和绝缘层有直接接触。沿电介质间隙壁26并且在ACS区16上形成导电层30。沿电介质间隙壁26并且在导电层30上形成触点28。在图1A的实施例中,电介质间隙壁26是由SiO₂制成的,导电层30是由多晶硅制成的,并且触点28是由钨制成的。

[0042] 3D-NAND存储器件100可以具有多个触点结构22。触点结构22被形成在电介质层24中,并且被放置在字线层上以连接到字线层。为了简单和清楚起见,在阶梯区100B和100C中的每个阶梯区中说明了仅三个触点结构22。触点结构22可以进一步被耦合到栅电压。可以通过字线层对BST、MC和TST的栅极施加栅电压以相对应地操作BST、MC和TST。

[0043] 3D-NAND存储器件100可以具有在衬底10的第一方向上延伸的第一电介质沟槽结构34。在一些实施例中,第一电介质沟槽结构34可以被放置在BSG层12a中以将BSG层12a分隔成两个部分(或者子BSG层)12a-1和12a-2。在一些实施例中,根据器件设计,第一电介质沟槽结构34可以进一步贯穿一个或多个虚拟字线层(诸如12b-12c)地延伸以将虚拟字线层分隔成两个部分(或者子虚拟字线层)。在图1A的示例性实施例中,第一电介质沟槽结构34仅被放置在BSG层12a中以将BSG层12a分隔成两个子BSG层12a-1和12a-2。

[0044] 仍然参考图1A,第二电介质沟槽结构32被放置在顶部选择栅(TSG)层12p和虚拟字线层12n-12o中以将TSG层12p和虚拟字线层12n-12o分隔成两个部分。例如,在引入第二电介质沟槽结构32时,TSG层12p变成12p-1和12p-2。第二电介质沟槽结构32在衬底10的第一方向上延伸。相应地,TSG层12p和虚拟字线层12n-12o沿衬底的第一方向被划分成两个子TSG层和两个子虚拟字线层。应当指出,图1A仅是一个示例,并且第二电介质沟槽结构32可以在3D-NAND存储器件100的顶部分隔任意数量的字线层。

[0045] 第一电介质沟槽结构34在垂直于第一方向的衬底10的第二方向(也被称为宽度方向或者Y方向)上与第二电介质沟槽结构32偏离。还通过一个或多个字线层和绝缘层沿衬底10的Z方向(或者高度方向)将第一电介质沟槽结构34与第二电介质沟槽结构32分隔开。

[0046] 在一些实施例中,第一和第二电介质沟槽结构34和32可以具有从50nm到150nm的临界尺寸(CD)。在一些实施例中,第一和第二电介质沟槽结构34和32可以是空的结构。在一些实施例中,可以用SiN、SiO₂、SiON、SiOCN、SiCN或者其它合适的电介质材料填充第一和第二电介质沟槽结构34和32。在一些实施例中,第一和第二电介质沟槽结构34和32可以以10nm到100nm之间的深度沿衬底10的第一方向延伸。在一些实施例中,第一电介质沟槽结构34和第二电介质沟槽结构32在衬底10的第二方向上被安排在缝隙结构20a-20b之间。在一些实施例中,第一电介质沟槽结构34、第二电介质沟槽结构32和缝隙结构20a-20b在衬底10的第一方向上平行于彼此地延伸。

[0047] 通过在3D-NAND存储器件100中引入第一和第二电介质沟槽结构34和32,BSG层和TSG层可以被分隔成多个子BSG层和子TSG层。子BSG层和子TSG层可以将3D-NAND存储器件

100划分成多个子存储块。子存储块中的每个子存储块可以具有分别的子BSG层和分别的子TSG层。相应地,可以通过控制分别的子BSG层和分别的子TSG层独立地操作子存储块中的每个子存储块。相对应地,3D-NAND存储器件100可以精确地控制期望的子存储块(或者子阵列区)以便有效地减少编程时间、读时间、擦除时间和数据传输时间,并且大大提升数据存储效率。

[0048] 图1B是根据本公开内容的一些实施例的3D-NAND存储器件100的俯视图。如图1B中示出的,3D-NAND存储器件100可以具有四个边界1-4。两个缝隙结构20a-20b分别被放置在第一边界1和第二边界2处,并且进一步沿衬底10的第一方向(或者长度方向)延伸。缝隙结构20a被安排在阵列区100A和阶梯区100B-100C的第一边界(或者顶部边界)处。缝隙结构20b被安排在阵列区100A和阶梯区100B-100C的第二边界(或者底部边界)处。根据一些实施例,第二边界是与第一边界相对的。缝隙结构20a-20b可以充当用于连接3D-NAND存储器件100的ACS区16的触点,并且进一步将3D-NAND存储器件100与相邻的部件隔绝开。

[0049] 仍然参考图1B,第一电介质沟槽结构34和第二电介质沟槽结构32在衬底10的第二方向上被安排在缝隙结构20a-20b之间。第一电介质沟槽结构34、第二电介质沟槽结构32和缝隙结构20a-20b在衬底10的第一方向上平行于彼此地延伸。在一些实施例中,有意地使第一和第二电介质沟槽结构34和32沿衬底10的第二方向(宽度方向)与彼此偏离。

[0050] 可以通过在第一和第二电介质沟槽结构34和32之间引入未对准的剖面来获得若干好处。首先,第一电介质沟槽结构34和第二电介质沟槽结构32可以将3D-NAND存储器件100划分成三个子存储块102、104和106。可以通过在子BSG层12a-1和12a-2以及子TSG层12p-1和12p-2上施加合适的控制电压独立地操作三个子存储块102、104和106。在一个示例中,为了对子存储块102进行编程,可以对子TSG层12p-1施加Vcc电压(诸如1.0伏),以及可以对子BSG层12a-1施加零电压。在另一个示例中,为了擦除子存储块104,子TSG层12p-2可以是处在上浮阶段的,并且可以将子BSG层12a-1从地阶段(例如,零伏)切换到上浮阶段。

[0051] 第二,第一和第二电介质沟槽结构34和32之间的未对准的剖面允许用字线层替换每个子存储块中的牺牲字线层。在将牺牲字线层替换成字线层期间,湿式蚀刻化学品可以从缝隙结构被引入,并且流向第一和第二电介质沟槽结构34和32。湿式蚀刻化学物在牺牲字线层和绝缘层之间具有良好的蚀刻选择性。于是,可以移除牺牲字线层以形成空的空间,并且绝缘层仍然保留。可以随后引入沉积过程以填充空的空间以形成字线层。

[0052] 3D-NAND存储器件100可以进一步包括被形成在衬底上并且沿衬底的2方向(或者高度方向)贯穿字线层和绝缘层地延伸的多个虚拟沟道结构36。在一些实施例中,仅在阶梯区100B和100C中形成虚拟沟道结构。在一些实施例中,可以在阶梯区100B和100C以及阵列区100A两者中形成虚拟沟道结构36。虚拟沟道结构充当用于在牺牲字线层被移除时支撑阶梯区和/或阵列区的支撑部件。在图1B的实施例中,在阵列区100A中形成虚拟沟道结构36。在一些实施例中,虚拟沟道结构36可以是与沟道结构18一起被形成的,并且具有与沟道结构18相似的结构。因此,虚拟结构也可以包括阻隔层、捕获层、隧穿层和沟道层。在一些实施例中,虚拟沟道结构36具有与沟道结构18不同的结构。例如,虚拟沟道结构36是由电介质材料(诸如SiO₂、SiN或者其它合适的电介质材料)制成的。

[0053] 如在图1B中示出的,沟道结构18被形成在衬底10上,并且进一步贯穿字线层和绝缘层地延伸。沟道结构18被安排在缝隙结构20a-20b之间。虚拟沟道结构36也被安排在第一

缝隙结构和第二缝隙结构之间。在一些实施例中,第一电介质沟槽结构34跨越虚拟沟道结构的第一集合地延伸,并且第二电介质沟槽结构32跨越虚拟沟道结构的第二集合地延伸。进一步地,触点结构22被放置在阶梯区100B和100C中的字线层上。应当理解,图1B仅是一个示例。3D-NAND存储器件100可以包括任意数量的沟道结构18、任意数量的触点结构22和任意数量的虚拟沟道结构36。

[0054] 图1C是根据本公开内容的示例性实施例的3D-NAND存储器件100的三维视图。如在图2中示出的,字线层和绝缘层被交替地堆叠在衬底10上。第二电介质沟槽结构32被放置在字线层中的顶部选择栅(TSG)层12p和虚拟字线层12n-12o中以将TSG层12p和虚拟字线层12n-12o分隔成两个部分。第二电介质沟槽结构32进一步在衬底10的第一方向(或者X方向)上延伸。第一电介质沟槽结构34被放置在字线层中的底部选择栅(BSG)层12a中以将BSG层12a分隔成两个部分,并且在衬底10的第一方向上延伸。第一电介质沟槽结构34在衬底10的第二方向(或者Y方向)上与第二电介质沟槽结构32偏离。

[0055] 图2是3D-NAND存储器件100中的沟道结构18的横截面图。如在图2中示出的,沟道结构18可以具有圆柱形状,该圆柱形状具有侧壁和底部区域。当然,其它的形状是可能的。沟道结构18沿垂直于衬底10的Z方向被形成,并且经由被放置在沟道结构的底部区域处的底部沟道触点202与衬底10电耦合在一起。沟道结构18进一步包括沟道层206、隧穿层208、电荷捕获层210和阻隔层212。阻隔层212沿沟道结构18的侧壁并且在底部沟道触点202上被形成。阻隔层212与字线和绝缘层有直接接触。电荷捕获层210沿阻隔层212并且在底部沟道触点202上被形成,并且隧穿层208沿电荷捕获层210并且在底部沟道触点202上被形成。沟道层206具有沿隧穿层208被形成的侧部,并且具有贯穿被放置在底部沟道触点202上的隧穿层208、电荷捕获层210和阻隔层212的底部地延伸的T形底部。沟道层206的T形底部进一步被放置在底部沟道触点202上,并且与底部沟道触点202有直接接触。另外,隧穿层208、电荷捕获层210和阻隔层212可以在沟道结构18中形成“L脚”配置。L脚配置可以包括沿沟道结构18的侧壁被形成的侧部和位于底部沟道触点202之上的底部。

[0056] 沟道结构18可以还具有沟道绝缘层204,沟道绝缘层204沿沟道层206被形成以填充沟道结构18。沟道绝缘层204可以具有贯穿沟道层206、隧穿层208、电荷捕获层210和阻隔层212的底部地延伸并且在沟道层206上着陆的T形底部。在一些实施例中,沟道绝缘层204可以包括被放置在沟道绝缘层204的中间位置处的孔洞。沟道结构18可以进一步包括沿沟道绝缘层204被形成并且与沟道层206有直接接触的顶部沟道触点214。顶部沟道触点214被放置在TSG层12p之上以防止顶部沟道触点214与TSG层12p之间的任何电气干扰。在沟道结构18中,进一步在BSG层12a与底部沟道触点202之间形成栅电介质层216。栅电介质层216可以被放置在绝缘层14b和14a之间,并且具有环形形状以围绕底部沟道触点202。

[0057] 在图2的实施例中,阻隔层212是由 SiO_2 制成的。在另一个实施例中,阻隔层212可以包括多个层(诸如 SiO_2 和 Al_2O_3)。在图2的实施例中,电荷捕获层210是由 SiN 制成的。在另一个实施例中,电荷捕获层210可以包括多层配置(诸如 $\text{SiN}/\text{SiON}/\text{SiN}$ 多层配置)。在一些实施例中,隧穿层208可以包括多层配置(诸如 $\text{SiO}/\text{SiON}/\text{SiO}$ 多层配置)。在图2的实施例中,沟道层206是由多晶硅经由炉管低压化学气相沉积(CVD)过程制成的。沟道绝缘层204可以是由 SiO_2 制成的,并且顶部和底部沟道触点214和202可以是由多晶硅制成的。

[0058] 如在图2中示出的,沟道结构18可以具有圆柱形状。然而,本公开内容不限于此,并

且沟道结构18可以以其它形状(诸如方柱形、椭圆柱形或者任何其它合适的形状)被形成。

[0059] 图3A是第一相关3D-NAND存储器件300A的俯视图。为了简单和清楚起见,在图3A中说明了3D-NAND存储器件300A的仅一个存储块。如在图3A中示出的,3D-NAND存储器件300A具有被放置在3D-NAND存储器件300A的第一边界处的第一缝隙结构302和被放置在3D-NAND存储器件300A的相对的第二边界处的第二缝隙结构304。第一和第二缝隙结构302和304在3D-NAND存储器件300A的长度(或者X)方向上延伸。多个沟道结构306被安排在第一和第二缝隙结构302和304之间。多个虚拟沟道结构312被安排在第一和第二缝隙结构之间。虚拟沟道结构312可以具有与沟道结构306相同的结构或者与沟道结构306不同的结构。电介质沟槽结构308被放置在3D-NAND存储器件300A中,并且在3D-NAND存储器件300A的长度方向上延伸。电介质沟槽结构308将3D-NAND存储器件300A的TSG层分隔成两个子TSG层,这接着将3D-NAND存储器件300A划分成两个子存储块。电介质沟槽结构308进一步跨越虚拟沟道结构312的集合地延伸。3D-NAND存储器件300A的限制在于高存储块间隔和低沟道结构密度。

[0060] 图3B是第二相关3D-NAND存储器件300B的俯视图。为了简单和清楚起见,在图3B中说明了3D-NAND存储器件300B的仅一个存储块。存储器件300B具有被放置在3D-NAND存储器件300B的第一边界处的第一缝隙结构314和被放置在3D-NAND存储器件300B的第二边界处的第二缝隙结构316。第一和第二缝隙结构314和316在3D-NAND存储器件300B的长度(或者X)方向上延伸。多个沟道结构322被安排在第一和第二缝隙结构314和316之间。多个虚拟沟道结构324被安排在第一和第二缝隙结构314和316之间。虚拟沟道结构324可以具有与沟道结构322相同的结构或者与沟道结构322不同的结构。第一电介质沟槽结构318和第二电介质沟槽结构320被放置在3D-NAND存储器件300B中,并且在3D-NAND存储器件300B的长度方向上延伸。第一和第二电介质沟槽结构318和320将3D-NAND存储器件300B的TSG层分隔成三个子TSG层,这接着将3D-NAND存储器件300B划分成三个子存储块326-328。3D-NAND存储器件300B可以具有比3D-NAND存储器件300A更大的沟道结构密度。然而,在子存储块327中被安排在第一和第二电介质沟槽结构318和320之间的牺牲字线层可能不能够通过蚀刻过程来移除,因为第一和第二电介质沟槽结构318和320可以阻隔蚀刻化学物以避免蚀刻过程。相应地,子存储块327可能不起作用。

[0061] 图4A、4B、5、6、7A、7B、8A、8B、9A、9B和10是根据本公开内容的示例性实施例的制造3D-NAND存储器件100的各种中间步骤的横截面图和俯视图。

[0062] 图4A和4B说明了第一电介质沟槽结构34的形成。图4A是衬底10的横截面图,并且图4B是衬底10的俯视图,其中,图4A中的横截面图是从图4B中的沿衬底10的Z方向(或者高度方向)的线A-A'获得的。如在图4A中示出的,一个或多个底部选择栅(BSG)层和多个第一绝缘层可以被形成并且被交替地放置在衬底10上。在图4A的示例性实施例中,BSG层12a和两个第一绝缘层14a-14b被形成在衬底10上。因此,最低第一绝缘层14a被形成在衬底10上,并且BSG层12a被布置在第一绝缘层14a-14b之间。

[0063] BSG层12a可以是由SiN制成的虚拟BSG层。可以在随后的制造步骤中移除并且用高K层和金属层替换虚拟BSG层。BSG层12a可以具有从10nm到100nm的范围中的厚度。第一绝缘层可以包括SiO₂、SiCN、SiOCN或者其它合适的材料。第一绝缘层14a-14b可以具有从5nm到50nm的厚度。可以应用任何合适的沉积过程来形成BSG层、第一绝缘层,诸如化学气相沉积(CVD)、物理气相沉积(PVD)、原子层沉积(ALD)、扩散或者其任意组合。

[0064] 仍然参考图4A,可以在BSG层12a中形成第一电介质沟槽结构34以将BSG层12a分隔成两个部分(或者子BSG层)12a-1和12a-2。第一电介质沟槽结构34在衬底10的第一方向(也被称为长度方向或者X方向)上延伸。尽管第一电介质沟槽结构34被说明为是被形成在最低BSG层中的,但在其它实施例中,第一电介质沟槽结构34可以被形成在另一个BSG层中。第一电介质沟槽结构34可以具有从50nm到150nm的CD。第一电介质沟槽结构34可以是由SiCN、SiO₂、SiON、SiOCN、SiN或者其它合适的电介质材料制成的。在一些实施例中,第一电介质沟槽结构34可以以10nm到100nm之间的深度延伸到衬底10中。为了形成第一电介质沟槽结构34,可以通过光刻过程在第一绝缘层14b上形成成像掩模堆叠。随后可以引入蚀刻处理以贯穿第一绝缘层、BSG层地进行蚀刻,并且进一步延伸到衬底10中以形成沟槽缺口(未示出)。然后可以通过应用CVD、PVD、ALD、扩散或者其任意组合利用电介质材料(诸如SiO₂、SiON、SiOCN、SiN、SiCN或者其它合适的材料)填充沟槽缺口,可以执行表面平坦化过程(诸如化学机械研磨(CMP)过程)以移除第一绝缘层14b上的任何过多的电介质材料。保留在沟槽缺口中的电介质材料变成第一电介质沟槽结构34。在一些实施例中,一旦形成了沟槽缺口,则沟槽缺口可以保持是空的,并且变成第一电介质沟槽结构34。相应地,第一电介质沟槽结构34可以是空的结构。

[0065] 在图5中,在第一绝缘层14b上沉积多个字线层和多个第二绝缘层。字线层,第二绝缘层、第一绝缘层14a-14b和BSG层12a相应地形成堆叠500。交替地放置字线层和第二绝缘层以使得通过第二绝缘层将字线层与彼此间隔开。例如,如在图5中示出的,字线层12b被放置在第一绝缘层14b上,并且第二绝缘层14c被放置在字线层12b上。将最高字线层12p放置在最高第二绝缘层14q和第二绝缘层14p之间。在一些实施例中,字线层中的最高字线层12p可以充当TSG层。在其它实施例中,TSG层可以是不同于最高字线层12p的字线层(诸如被放置在字线层12p之下的字线层12n或者字线层12o)。在一些实施例中,字线层12p充当TSG层,并且字线层12n-12o可以是虚拟字线层。在其它的实施例中,BSG层12a之上的字线层中的一个或多个字线层(诸如字线层12b-12c)可以是虚拟字线层。

[0066] 字线层还可以是牺牲层,这些牺牲层是由SiN制成的,并且具有从10nm到100nm的范围中的厚度。可以在随后的制造步骤中移除并且用高K层和金属层替换牺牲层。第二绝缘层可以具有5nm到50nm之间的厚度,并且包括SiO₂、SiCN、SiOCN或者其它合适的材料。可以应用任何合适的沉积过程来形成字线层和第二绝缘层,诸如CVD、PVD、ALD、扩散或者其任意组合。

[0067] 在图6中,在堆叠500中形成两个阶梯区100B和100C。可以通过修剪蚀刻过程来形成对两个阶梯区100B和100C的形成。可以对第二绝缘层、字线层、BSG层12a和第一绝缘层14a-14b应用修剪蚀刻过程以形成两个阶梯区100B和100C。一旦形成了阶梯区100B和100C,则阵列区100A被放置在阶梯区100B和100C之间。

[0068] 图7A和7B说明了形成堆叠500中的第二电介质沟槽结构32。图7A是衬底10的横截面图,并且图7B是衬底10的俯视图,其中,图7A中的横截面图是从图7B中的沿衬底10的Z方向(或者高度方向)的线A-A'获得的。如在图7A中示出的,可以在字线层12n-12p中形成第二电介质沟槽结构32。在一些实施例中,字线层12p可以是3D-NAND存储器件100的TSG层,并且字线层12n-12o可以是两个虚拟字线层。第二电介质沟槽结构32在衬底10的第一方向上延伸以将TSG层12p和虚拟字线层12n-12o分隔成两个部分。例如,可以在图7A中形成两个子

TSG层12p-1和12p-2。在一些实施例中,第二电介质沟槽结构32可以是在衬底10的第二方向(也被称为宽度方向,或者Y方向)上与第一电介质沟槽结构34偏离的。在一些实施例中,第二电介质沟槽结构32可以具有从50nm到150nm的CD,并且包括SiO₂、SiON、SiOCN、SiN、SiCN或者其它合适的电介质材料。在一些实施例中,第二电介质沟槽结构32可以是空的结构。可以基于与上面提到的用于形成第一电介质沟槽结构34的过程类似的过程形成第二电介质沟槽结构32。

[0069] 应当指出,图7A和7B仅是示例,第一电介质沟槽结构34可以进一步沿Z方向延伸以便被放置在BSG层12a之上的任意数量的字线层中。根据器件结构,第二电介质沟槽结构32可以进一步向衬底延伸以便被放置在字线层12n之下的任意数量的字线层中。

[0070] 图8A和8B说明了形成堆叠500中的沟道结构18和虚拟沟道结构36。图8A是衬底10的横截面图,并且图8B是衬底10的俯视图,其中,图8A中的横截面图是从图8B中的沿衬底10的Z方向(或者高度方向)的线A-A'获得的。为了形成沟道结构18,首先可以形成多个沟道缺口。可以通过用于形成成像掩模的光刻过程和随后的用于转移掩模的图案的蚀刻过程来形成沟道缺口。所形成的沟道缺口可以贯穿字线层、BSG层12a以及第一和第二绝缘层,并且进一步延伸到衬底10中。沟道缺口中的每个沟道缺口可以具有用于暴露衬底10的侧部和底部。在形成沟道缺口时,可以在沟道缺口的底部处形成多个底部沟道触点(诸如图2中说明的底部沟道触点202)。沟道缺口中的每个沟道缺口可以具有分别的位于底部处的底部触点。底部沟道触点可以从BSG层12a伸出,并且底部沟道触点中的每个底部沟道触点的顶面可以被放置在BSG层12a和字线层12b之间。

[0071] 仍然参考图8A,一旦形成了底部沟道触点,可以沿沟道缺口的侧部并且在底部沟道触点之上顺序地形成阻隔层、电荷捕获层和隧穿层。可以应用随后的非等向性等离子体蚀刻来移除被安排在底部沟道触点之上的阻隔层、电荷捕获层和隧穿层的部分以形成多个互连缺口。每个互连缺口暴露分别的底部沟道触点。沟道层可以随后沿沟道缺口的侧部被形成,并且进一步贯穿互连缺口地延伸以连接底部沟道触点。

[0072] 一旦形成了沟道层,则沟道层可以具有沿隧穿层被形成的侧部和贯穿被放置在底部沟道触点之上的隧穿层、电荷捕获层和阻隔层的底部地延伸的T形底部。沟道层的T形底部与底部沟道触点有直接接触,这可以在图2中示出。另外,隧穿层、电荷捕获层和阻隔层可以在沟道缺口中形成L脚配置。L脚配置可以包括沿沟道缺口的侧壁被形成的侧部和位于底部沟道触点之上的底部。

[0073] 在一些实施例中,一旦形成了沟道层,则可以应用随后的退火过程以释放晶圆应力并且还减少缺陷(悬空键)。在一些情况下,退火过程还用于将沟道层变换成多晶的。在一些实施例中,沟道结构的形成进一步包括在沟道层上形成沟道绝缘层以填充沟道缺口,以及在沟道绝缘层上形成顶部沟道触点以使得顶部沟道触点与沟道层有直接接触。可以在图2中说明详细的沟道结构。

[0074] 图8B是用于说明沟道结构18的形成的俯视图。如在图8B中示出的,可以在阵列区100A中形成沟道结构18。另外,还可以在阵列区100A中形成多个虚拟沟道结构36。在一些实施例中,虚拟沟道结构36可以是与沟道结构18一起被形成的,并且具有与沟道结构18相似的结构。因此,虚拟结构也可以包括阻隔层、捕获层、隧穿层和沟道层。在一些实施例中,虚拟沟道结构36具有与沟道结构18不同的结构。例如,虚拟沟道结构36是由电介质材料(诸如

SiO₂、SiN或者我们合适的电介质材料)制成的。在一些实施例中,第二电介质沟槽结构32可以跨越虚拟沟道结构的第一集合地延伸,并且第一电介质沟槽结构34可以跨越虚拟沟道结构的第二集合的延伸。在一些实施例中,可以远离第一和第二电介质沟槽结构34和32地放置虚拟沟道结构36。在一些实施例中,可以进一步在阶梯区100B和100C中形成虚拟沟道结构36。在图8B的实施例中,沟道结构18和虚拟沟道结构36可以沿衬底的第二方向(例如,Y方向)被布置到14行中,其中,虚拟沟道结构36可以被放置在第5和10行中。进一步地,四行(例如,第6-9行)沟道结构可以被布置在第一电介质沟槽结构34和第二电介质沟槽结构32之间。

[0075] 图9A和9B说明了形成堆叠500中的缝隙结构20a和20b。图9A是衬底10的横截面图,并且图9B是衬底10的俯视图,其中,图9A中的横截面图是从图9B中的沿衬底10的Z方向(或者高度方向)的线A-A'获得的。为了形成缝隙结构20a和20b,可以通过光刻过程将成像掩模放置在堆叠500的最高第二绝缘层14q上,并且随后的蚀刻过程可以将成像掩模的图案转移到堆叠500的字线层以及第一和第二绝缘层中以形成缝隙缺口(未示出)。堆叠500可以具有四个边界1-4。缝隙缺口可以被放置在堆叠500的第一边界1和第二边界2处。缝隙缺口可以贯穿字线层、第二绝缘层、第一绝缘层14a-14b和BSG层12a。缝隙缺口可以进一步延伸到衬底10中。缝隙缺口中的每个缝隙缺口可以具有延伸到衬底10中的侧部和底部。缝隙缺口可以进一步沿衬底的第一方向(或者长度方向)延伸,并且被安排得与第一和第二电介质沟槽结构34和32平行。

[0076] 在形成缝隙缺口之后,随后的用于完成对缝隙结构的形成的制造步骤(例如,在栅极最先制造流程与栅极最后制造流程之间)可以是不同的。在栅极最先制造流程中,可以随后应用离子注入以在缝隙缺口中的每个缝隙缺口的底部处形成掺杂区,诸如,掺杂区(也被称为阵列共源区)16。可以沿缝隙缺口的侧部并且在掺杂区之上形成电介质间隙壁(诸如电介质间隙壁26)。可以实现非等向性等离子蚀刻以移除被形成在掺杂区16上的电介质间隙壁26的底部以暴露掺杂区16。导电层(诸如导电层30)可以是沿电介质间隙壁26被沉积的,并且填充缝隙缺口。之后可以通过蚀刻过程使导电层30凹陷,以及可以沿电介质间隙壁26并且在导电层30之上形成触点(诸如触点28)。在形成触点时,完成了具有与图9A中的缝隙结构20a和20b相同的剖面的缝隙结构。相应地,在堆叠500的第一边界1和第二边界2处形成两个缝隙结构20a和20b。

[0077] 然而,在栅极最后制造流程中,在形成缝隙缺口时,随后由通过缝隙缺口被引入的湿式蚀刻化学物移除字线层和BSG层12a以形成多个空位(或者空的空间)。之后可以应用离子注入以在缝隙缺口中的每个缝隙缺口的底部处形成掺杂区(例如,ACS区16)。在注入步骤之后,经由通过缝隙缺口用高K层加金属层填充空位改造字线层和BSG层12a。接下来,可以沿缝隙缺口的侧部并且在掺杂区16之上形成电介质间隙壁(诸如电介质间隙壁26)。随后,可以实现非等向性等离子蚀刻以移除被形成在掺杂区16之上的电介质间隙壁26的底部以暴露掺杂区16。导电层(诸如导电层30)可以是沿电介质间隙壁26被沉积的,并且填充共源缺口。之后可以通过蚀刻过程使导电层30凹陷,以及可以沿电介质间隙壁26并且在导电层30之上形成触点(诸如触点28)。在形成触点时,完成了具有与图9A中的缝隙结构20a和20b相同的剖面的缝隙结构。

[0078] 在图10中,可以在阶梯区100B和100C中形成多个触点结构22。在一些实施例中,在

形成触点结构22之前,可以在衬底10上形成电介质层24。电介质层24可以进一步覆盖阶梯区100B和100C。可以应用成像过程以在电介质层24中形成多个触点缺口。触点缺口可以在第一和第二绝缘层上着陆,并且进一步贯穿第一和第二绝缘层地延伸以暴露字线层和BSG层12a。随后可以应用沉积过程以将导电材料沉积到触点缺口中,并且可以应用CMP过程以移除电介质层24的顶面上的任何过多的导电材料。在完成CMP过程时,仍然留在触点缺口中的导电材料变成触点结构22。在形成触点结构22之后,形成了图10中的最后的3D-NAND存储器件100(诸如图1A中说明的3D-NAND存储器件100)。

[0079] 图11是用于制造根据一些实施例的3D-NAND存储器件100的过程1100的流程图。过程1100在步骤S1104处开始,在该处,可以在衬底上形成多个第一绝缘层和虚拟底部选择栅(BSG)层。虚拟BSG层被安排在第一绝缘层之间。在过程1100的步骤S1106中,可以形成第一电介质沟槽结构。第一电介质沟槽结构贯穿虚拟BSG层,并且在衬底的第一方向上延伸以使得虚拟BSG层被第一电介质沟槽结构分隔成两个部分。在一些实施例中,可以如参考图4A和4B说明的那样执行步骤S1104和S1106。

[0080] 过程1100然后前进到步骤S1108,在该处,在第一绝缘层上形成多个牺牲字线层和多个第二绝缘层。交替地安排第二绝缘层和牺牲字线层。在一些实施例中,可以如参考图5说明的那样执行步骤S1108。

[0081] 在步骤S1110中,可以形成第二电介质沟槽结构。第二电介质沟槽结构可以贯穿牺牲字线层中的牺牲顶部选择栅(TSG)层以将牺牲TSG层分隔成两个部分,并且在衬底的第一方向上延伸。第二电介质沟槽结构在衬底的第二方向上与第一电介质沟槽结构偏离。在一些实施例中,在形成第二电介质沟槽结构之前,可以对第一绝缘层、虚拟BSG层、第二绝缘层和牺牲字线层应用修剪蚀刻过程以形成阵列区和阶梯区。在一些实施例中,可以如参考图6、7A和7B说明的那样执行步骤S1110。

[0082] 过程1100前进到步骤S1112,在该处,可以形成沟道结构、虚拟沟道结构和缝隙结构。在一些实施例中,在形成缝隙结构之前,可以分别用BSG层和字线层替换虚拟BSG层和牺牲字线层。在一些实施例中,可以如参考图8A、8B、9A、9B和10说明的那样执行步骤S1112。

[0083] 应当指出,可以在过程1100之前、期间和之后提供额外的步骤,并且,对于过程1100的额外的实施例,可以替换、排除或者按照不同的次序执行所描述的步骤中的一些步骤。在一个示例中,可以在形成第二电介质沟槽结构之后形成阶梯区。在另一个示例中,可以在形成阶梯区之前形成沟道结构。在一些实施例中,可以在阶梯区中形成虚拟沟道结构。

[0084] 在过程1100的随后的过程步骤中,可以在3D-NAND存储器件100上形成各种额外的互连结构(例如,具有导线和/或过孔的金属化层)。这样的互连结构将3D-NAND存储器件100与其它的触点结构和/或有源器件电气连接在一起以形成功能电路。还可以形成额外的器件特征(诸如钝化层、输入/输出结构等)。

[0085] 本文中描述的各种实施例提供优于相关存储器件的若干优点。例如,相关存储器件或者具有较低存储单元密度,或者具有不起作用的子存储块。在所公开的3D-NAND存储器件中,存储单元的存储块可以具有被放置在底部选择栅(BSG)层中的用于将BSG层分隔成两个部分的第一电介质沟槽结构和被放置在顶部选择栅(TSG)层中的用于将TSG层分隔成两个部分的第二电介质沟槽结构。第二电介质沟槽结构是与第一电介质沟槽结构偏离的。所公开的配置通过将存储块划分成三个独立的并且起作用的子存储块而允许存储块中的更

高的沟道结构密度。

[0086] 前述内容概述了若干实施例的特征以使得本领域的技术人员可以更好地理解本公开内容的方面。本领域的技术人员应当认识到,他们可以容易地将本公开内容用作设计或者修改其它的用于实现与本文中介绍的实施例相同的目的和/或达到与本文中介绍的实施例相同的优点的过程和结构的基础。本领域的技术人员还应当认识到,这样的等价构造不脱离本公开内容的精神和范围,并且他们可以在本文中作出各种变更、替换和改变,而不脱离本公开内容的精神和范围。

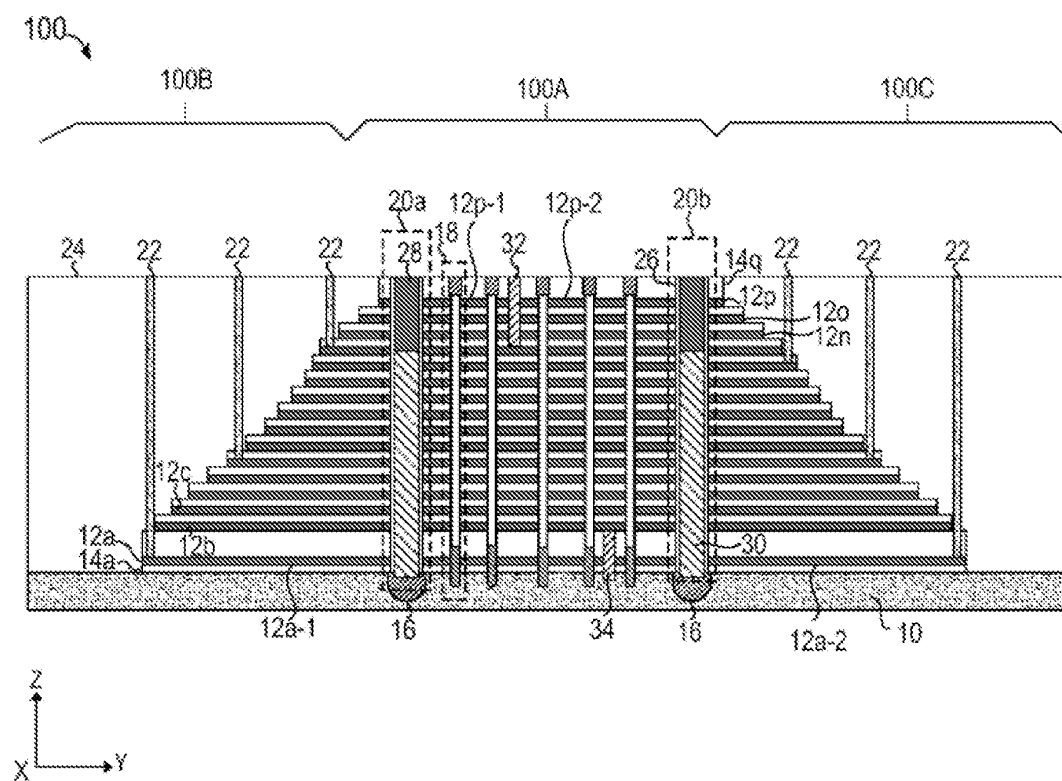


Figure 1A

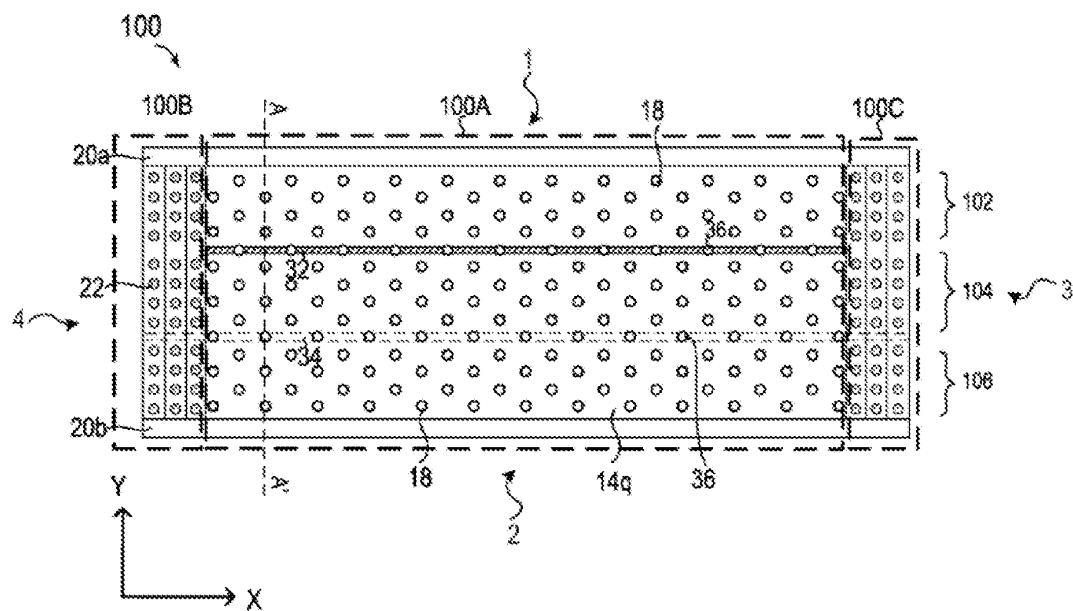


图1B

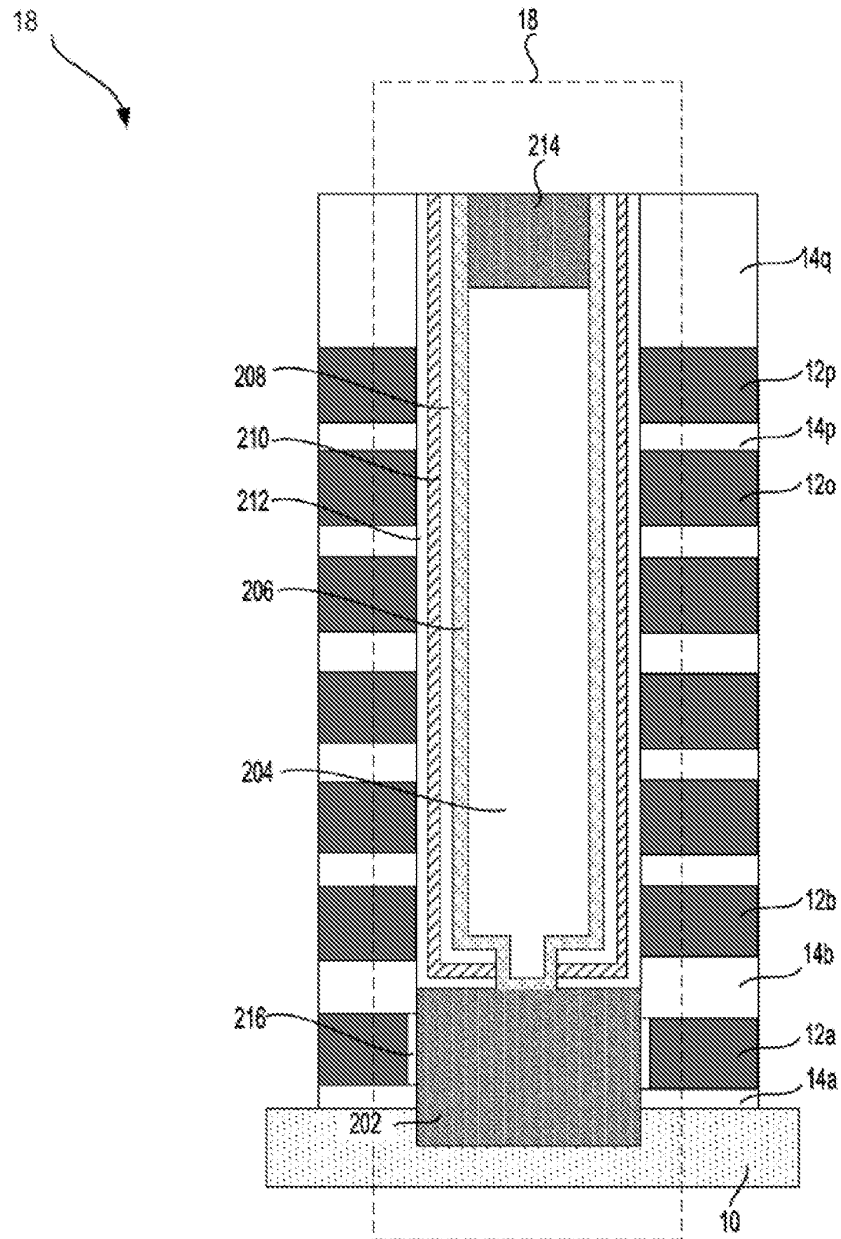


图2

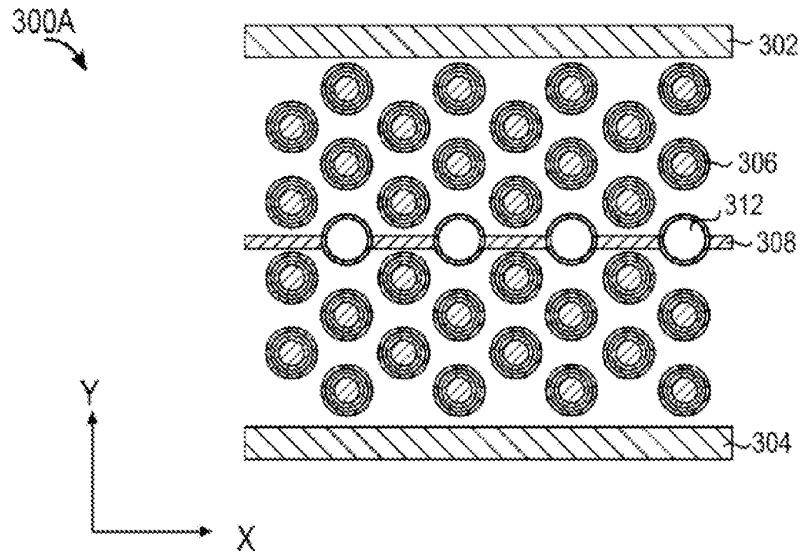


图3A

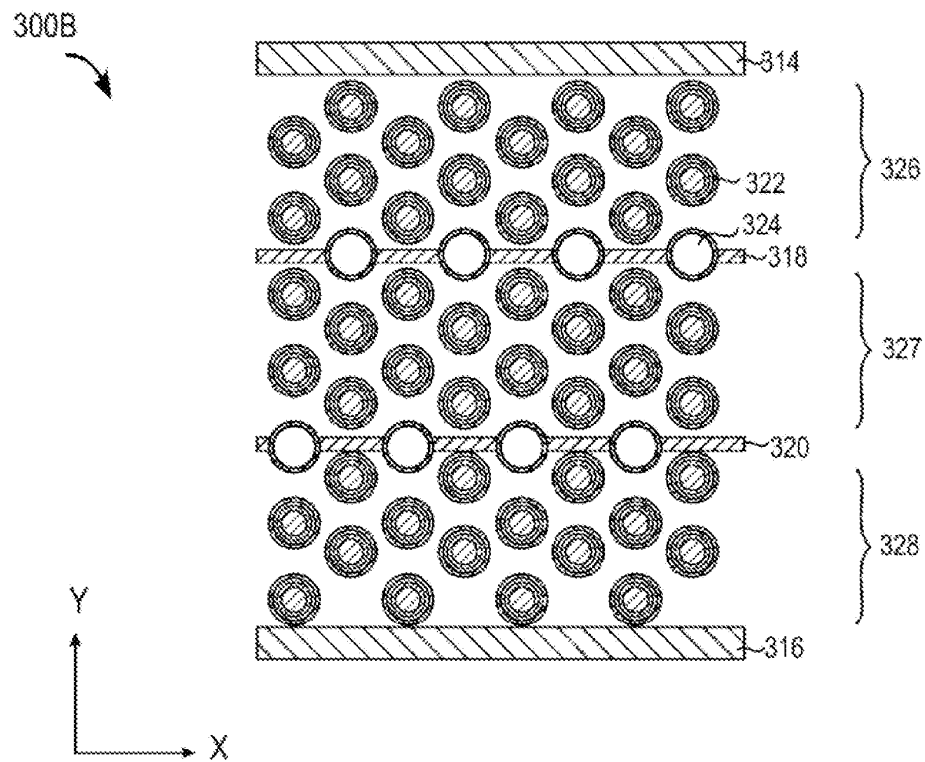


图3B

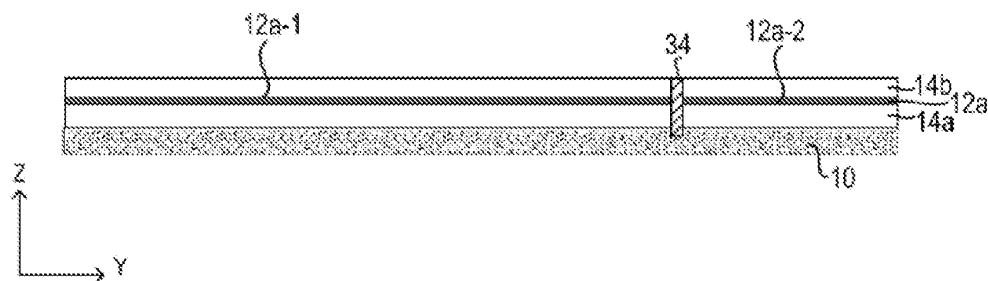


图4A

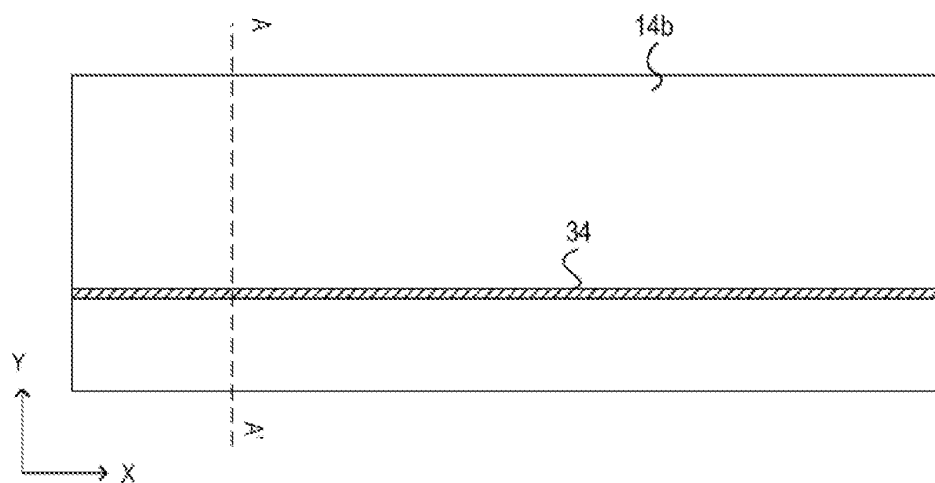


图4B

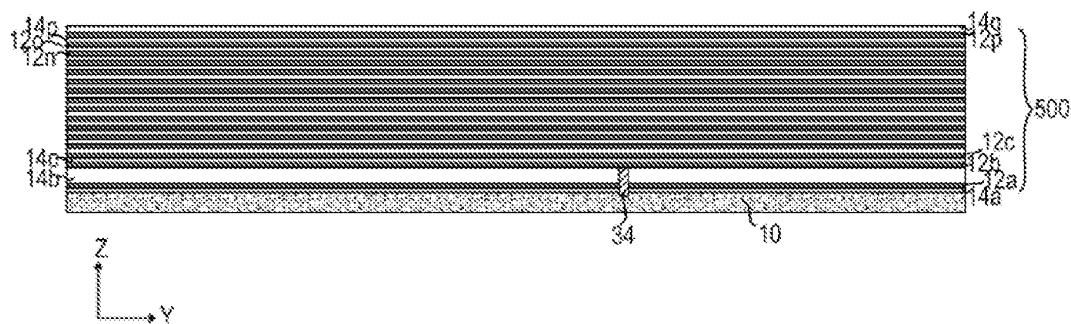


图5

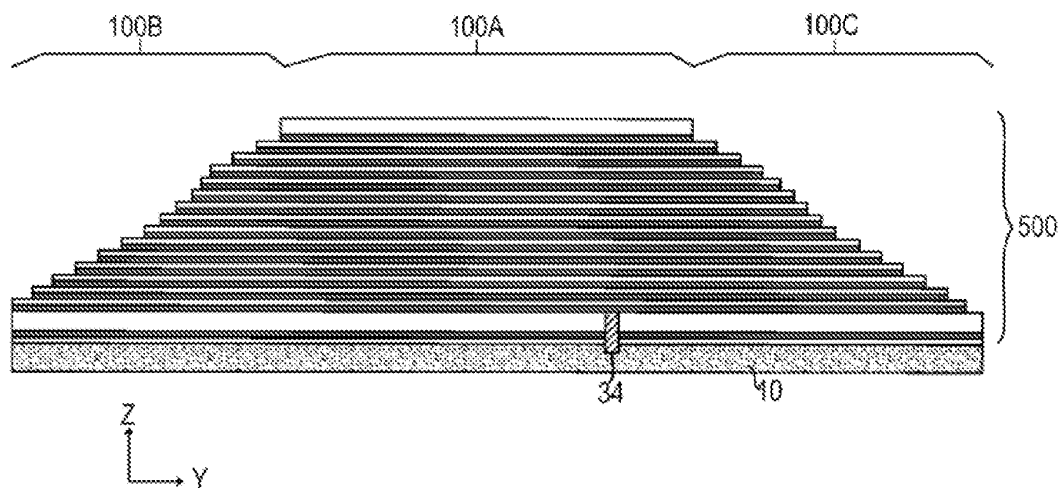


图6

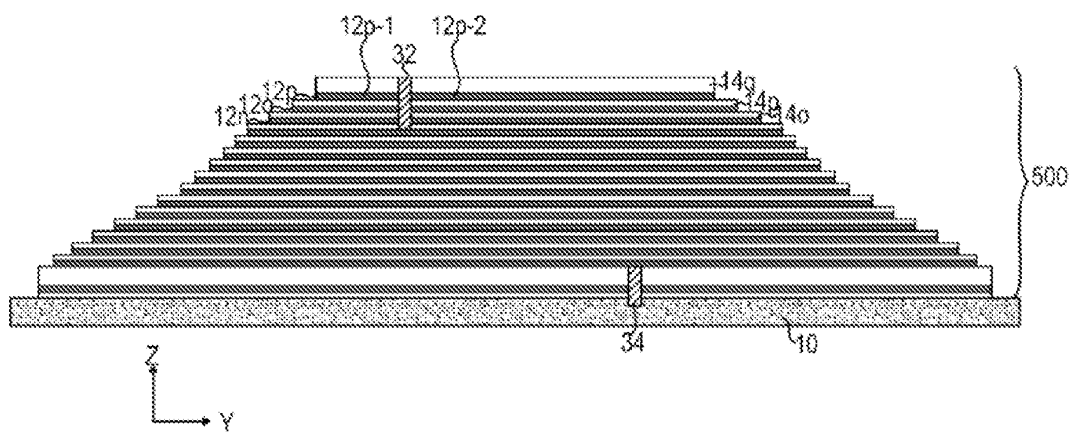


图7A

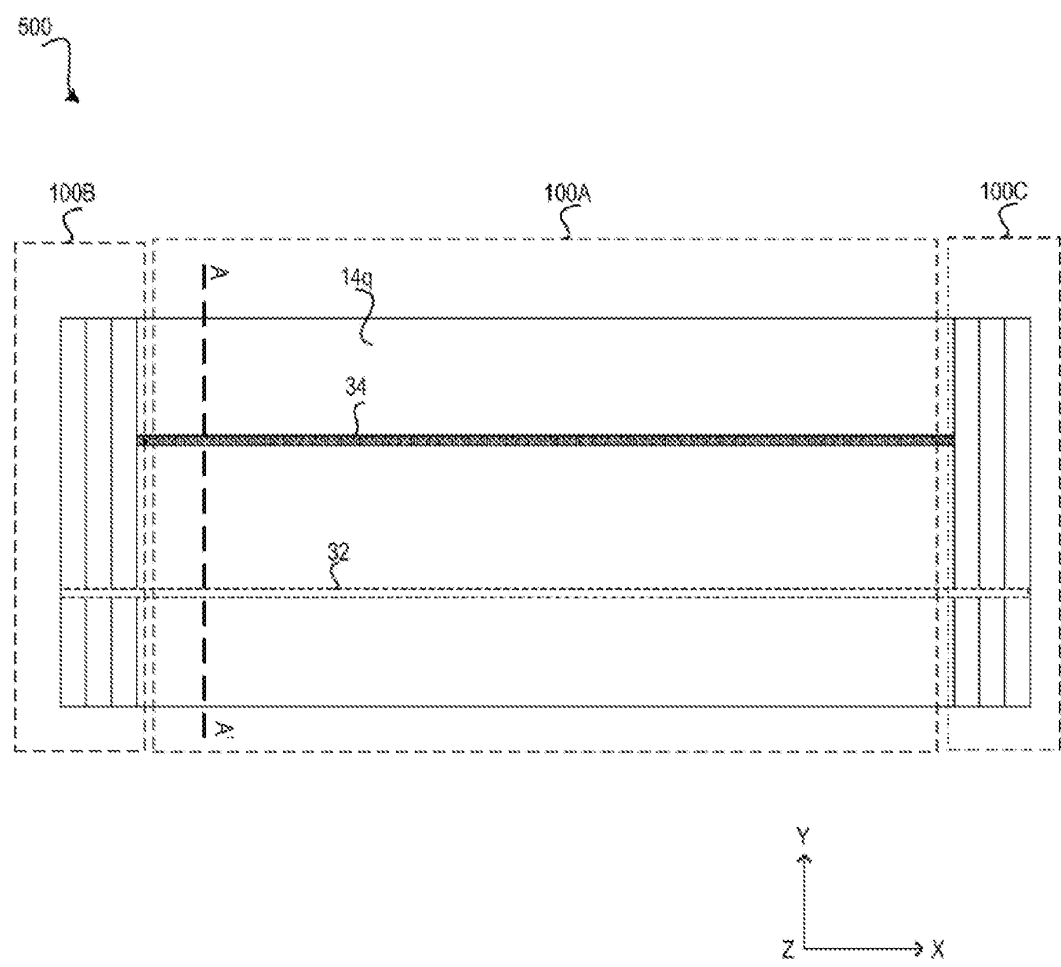


图7B

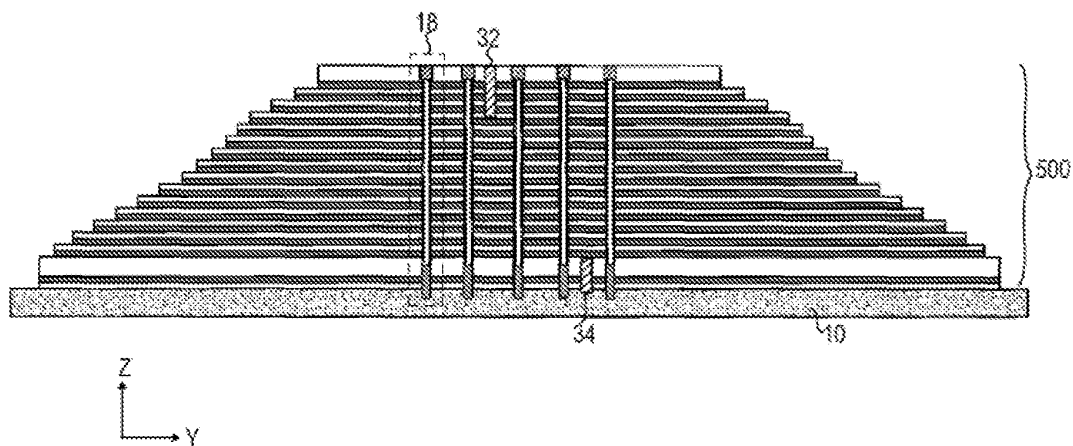


图8A

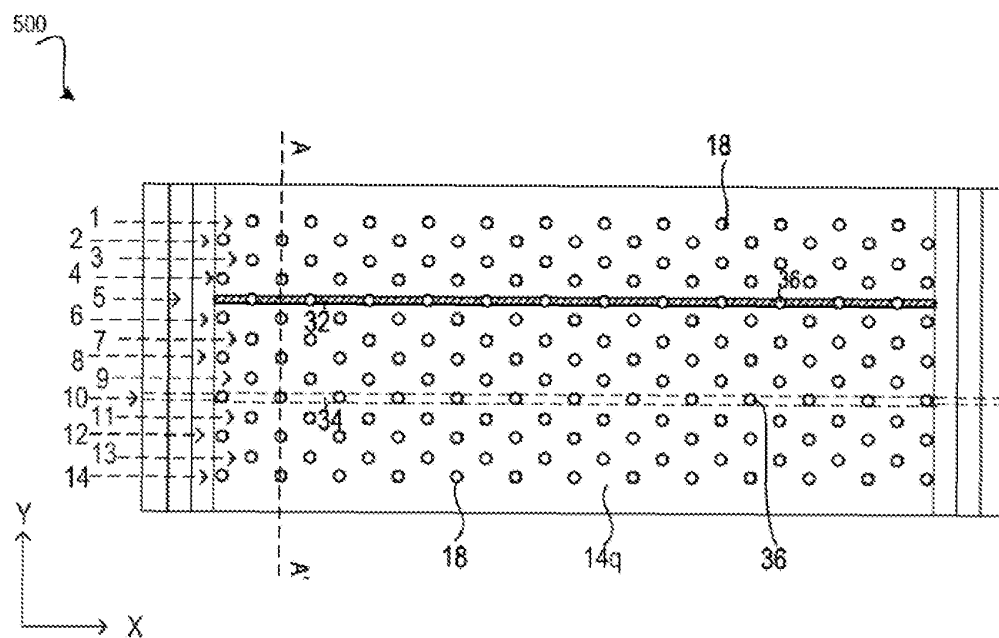
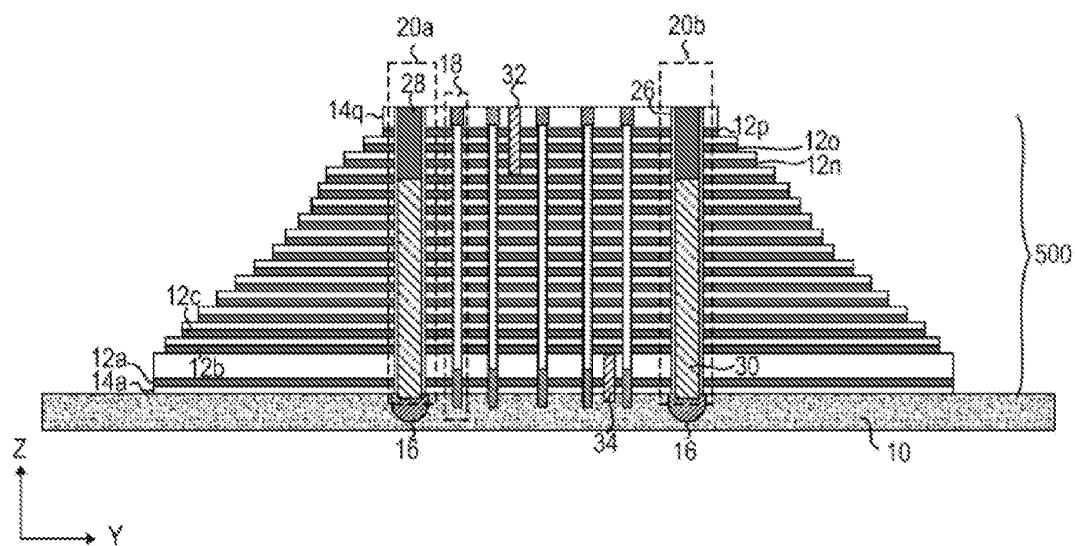


图8B



X19A

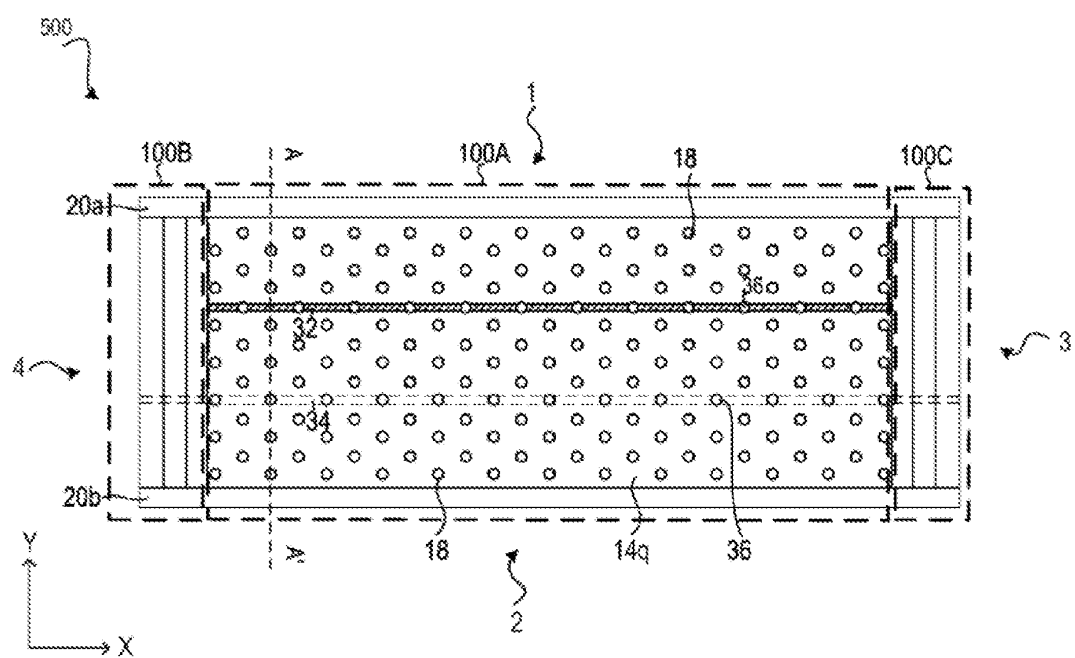


Figure 9B

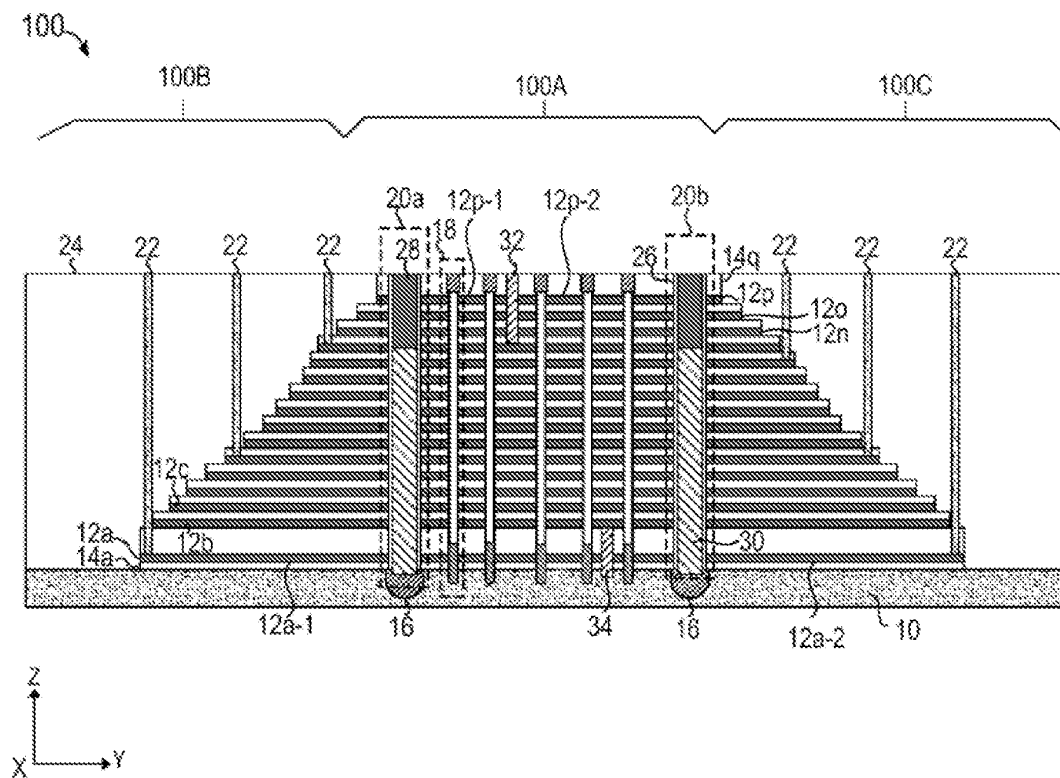


图 10

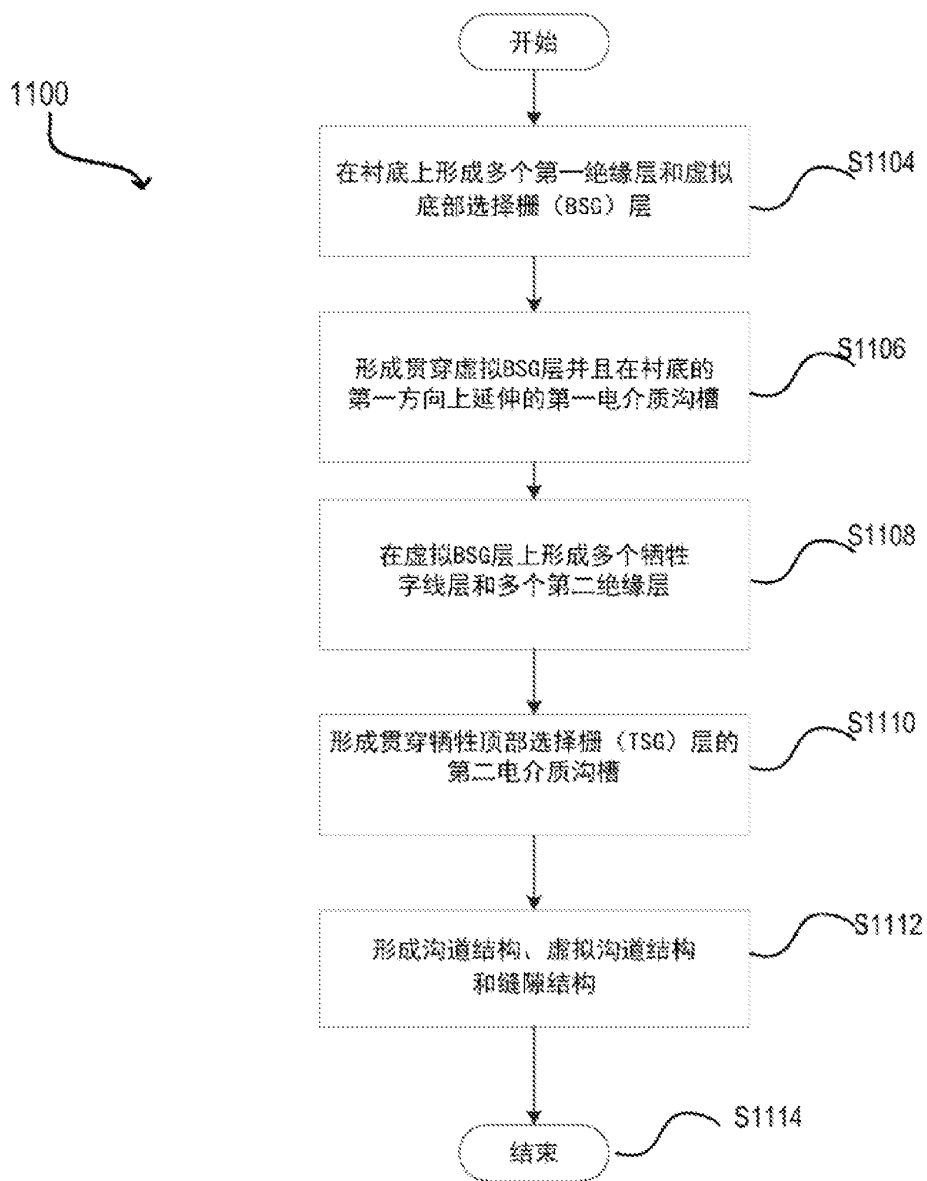


图11



(12)发明专利申请



(10)申请公布号 CN 111180418 A

(43)申请公布日 2020.05.19

(21)申请号 201911105606.0

H01L 21/768(2006.01)

(22)申请日 2019.11.12

(30)优先权数据

10-2018-0138049 2018.11.12 KR

(71)申请人 三星电子株式会社

地址 韩国京畿道

(72)发明人 黄盛珉 任峻成 金志荣 金智源
梁宇成

(74)专利代理机构 中科专利商标代理有限责任
公司 11021

代理人 范心田

(51)Int. Cl.

H01L 23/538(2006.01)

H01L 27/11524(2017.01)

H01L 27/11551(2017.01)

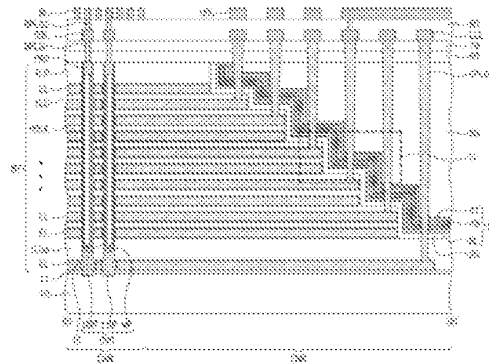
权利要求书3页 说明书14页 附图45页

(54)发明名称

三维半导体存储器件及其制造方法

(57)摘要

公开了三维半导体存储器件及其制造方法。可以提供一种三维半导体存储器件,包括:衬底,包括单元阵列区和连接区;电极结构,包括交替堆叠在衬底上的多个电极和多个介电层,电极结构在连接区上具有阶梯部分;蚀刻停止结构,在电极结构的阶梯部分上;以及多个接触插塞,在连接区上,接触插塞穿透蚀刻停止结构并且分别连接到电极的对应焊盘部分。蚀刻停止结构可以包括蚀刻停止图案和水平介电层,水平介电层具有均匀的厚度并且覆盖蚀刻停止图案的顶表面和底表面。



CN 111180418 A

1. 一种三维半导体存储器件, 包括:
衬底, 包括单元阵列区和连接区;
电极结构, 包括交替堆叠在所述衬底上的多个电极和多个介电层, 所述电极结构在所述连接区上具有阶梯部分;
蚀刻停止结构, 在所述电极结构的阶梯部分上; 以及
多个接触插塞, 在所述连接区上, 所述多个接触插塞穿透所述蚀刻停止结构并分别连接到所述电极的对应焊盘部分,
其中所述蚀刻停止结构包括蚀刻停止图案和水平介电层, 所述水平介电层具有均匀的厚度并且覆盖所述蚀刻停止图案的顶表面和底表面。
2. 根据权利要求1所述的器件, 其中所述水平介电层包括:
覆盖所述蚀刻停止图案的所述顶表面的第一部分; 以及
覆盖所述蚀刻停止图案的所述底表面的第二部分,
其中所述第一部分和所述第二部分包括相同的材料。
3. 根据权利要求1所述的器件, 其中所述蚀刻停止图案包括与所述水平介电层的介电材料和所述介电层的介电材料不同的介电材料。
4. 根据权利要求1所述的器件, 还包括:
竖直结构, 在所述单元阵列区上, 所述竖直结构穿透所述电极结构; 以及
水平阻挡介质层, 覆盖所述电极的顶表面和底表面二者,
其中所述水平阻挡介质层的第一部分覆盖所述电极的第一侧壁, 所述电极的所述第一侧壁与所述竖直结构相邻。
5. 根据权利要求4所述的器件, 其中所述水平介电层包括:
覆盖所述蚀刻停止图案的所述顶表面的第一部分; 以及
覆盖所述蚀刻停止图案的所述底表面的第二部分,
其中所述水平介电层的所述第一部分和所述第二部分的厚度均小于所述水平阻挡介电层的所述第一部分的厚度。
6. 根据权利要求1所述的器件, 还包括:
缓冲介电层, 在所述蚀刻停止图案和所述水平介电层之间。
7. 根据权利要求6所述的器件, 其中所述缓冲介电层包括与所述蚀刻停止图案的介电材料和所述水平介电层的介电材料不同的介电材料。
8. 根据权利要求6所述的器件, 还包括:
公共源极插塞, 穿透所述电极结构, 所述公共源极插塞沿第一方向延伸并与所述电极结构平行,
其中所述缓冲介电层的一部分在所述公共源极插塞与所述电极的第二侧壁之间, 所述电极的所述第二侧壁与所述公共源极插塞相邻。
9. 根据权利要求8所述的器件, 其中所述缓冲介电层在所述蚀刻停止图案与所述水平介电层之间的厚度大于所述缓冲介电层在所述电极的所述第二侧壁上的厚度。
10. 根据权利要求1所述的器件, 还包括:
公共源极插塞, 穿透所述电极结构, 所述公共源极插塞沿第一方向延伸并与所述电极结构平行; 以及

侧壁间隔物,在所述公共源极插塞与所述电极结构之间,
其中所述侧壁间隔物覆盖所述蚀刻停止图案的侧壁。

11.根据权利要求10所述的器件,其中,

所述电极的侧壁与所述公共源极插塞的侧壁间隔开第一水平距离,
所述蚀刻停止图案的侧壁与所述公共源极插塞间隔开第二水平距离,并且
所述第二水平距离大于所述第一水平距离。

12.根据权利要求1所述的器件,其中,

所述电极中的每一个沿垂直于所述衬底的顶表面的第二方向具有第一厚度,以及
所述蚀刻停止结构在所述阶梯部分上沿所述第二方向具有第二厚度,所述第二厚度大于所述第一厚度。

13.根据权利要求1所述的器件,还包括:

焊盘介电层,在所述蚀刻停止结构与所述电极结构的所述阶梯部分之间,
其中所述焊盘介电层包括与所述蚀刻停止图案的介电材料不同的介电材料。

14.一种三维半导体存储器件,包括:

衬底,包括单元阵列区和连接区;

电极结构,包括沿垂直于所述衬底的顶表面的第一方向交替堆叠的多个电极和多个介电层,所述电极结构沿平行于所述衬底的所述顶表面的第二方向延伸,所述电极结构在所述连接区上具有阶梯部分;

蚀刻停止图案,覆盖所述电极结构的所述阶梯部分;以及

公共源极插塞,沿所述第一方向穿透所述电极结构并沿所述第二方向延伸,

其中所述公共源极插塞的侧壁与所述蚀刻停止图案的侧壁之间的第一距离不同于所述公共源极插塞的侧壁与所述电极的侧壁之间的第二距离。

15.根据权利要求14所述的器件,还包括:

多个竖直结构,穿透所述电极结构;

水平阻挡介电层,覆盖所述竖直结构、所述电极的所述侧壁以及所述电极的顶表面和底表面;以及

水平介电层,覆盖所述蚀刻停止图案的顶表面和底表面二者,

其中所述水平介电层包括与所述水平阻挡介电层相同的材料,

所述电极具有与所述竖直结构相邻的第一侧壁,以及

所述水平介电层包括,

覆盖所述电极的所述第一侧壁的第一部分,

覆盖所述蚀刻停止图案的所述顶表面的第二部分,以及

覆盖所述蚀刻停止图案的所述底表面的第三部分,所述第二部分和所述第三部分的厚度均小于所述第一部分的厚度。

16.根据权利要求15所述的器件,还包括:

缓冲介电层,在所述蚀刻停止图案与所述水平介电层之间,

其中所述缓冲介电层的一部分在所述公共源极插塞与所述电极的所述侧壁之间,以及

所述缓冲介电层在所述蚀刻停止图案与所述水平介电层之间的厚度大于所述缓冲介电层在所述电极的所述侧壁上的厚度。

17. 根据权利要求14所述的器件, 其中所述蚀刻停止图案具有与所述公共源极插塞相邻的圆形侧壁。

18. 根据权利要求14所述的器件, 还包括:

侧壁间隔物, 在所述公共源极插塞与所述电极结构之间,

其中所述侧壁间隔物包括朝向所述蚀刻停止图案的所述侧壁水平突出的突出部。

19. 根据权利要求14所述的器件, 其中所述蚀刻停止图案包括与所述介电层的介电材料不同的介电材料。

20. 根据权利要求14所述的器件, 还包括:

焊盘介电层, 在所述蚀刻停止图案与所述电极结构的所述阶梯部分之间,

其中所述焊盘介电层包括与所述蚀刻停止图案的介电材料不同的介电材料。

21. 一种三维半导体存储器件, 包括:

衬底, 包括单元阵列区和连接区;

电极结构, 包括交替堆叠在所述衬底上的多个电极和多个介电层, 所述电极结构在所述连接区上具有阶梯部分;

蚀刻停止结构, 覆盖所述电极结构的所述阶梯部分; 以及

多个接触插塞, 在所述连接区上, 所述接触插塞穿透所述蚀刻停止结构并分别连接到所述电极的对应焊盘部分,

其中所述蚀刻停止结构包括蚀刻停止图案, 所述蚀刻停止图案包括与所述介电层的介电材料不同的介电材料, 并且其中具有沿所述阶梯部分限定的界面。

22. 根据权利要求21所述的器件, 其中所述蚀刻停止图案的界面包括接缝。

23. 根据权利要求21所述的器件, 还包括:

水平阻挡介电层, 覆盖所述电极的顶表面和底表面二者,

其中所述蚀刻停止结构还包括水平介电层, 所述水平介电层在所述连接区上并且覆盖所述蚀刻停止图案的顶表面和底表面二者,

所述水平介电层包括与所述水平阻挡介电层的材料相同的材料, 以及

所述蚀刻停止图案比所述水平介电层厚。

24. 根据权利要求23所述的器件, 其中所述水平介电层包括与所述介电层的介电材料和所述蚀刻停止图案的介电材料不同的介电材料。

25. 根据权利要求24所述的器件, 还包括:

缓冲介电层, 在所述蚀刻停止图案与所述水平介电层之间,

其中所述缓冲介电层包括与所述蚀刻停止图案的所述介电材料和所述水平介电层的所述介电材料不同的介电材料。

三维半导体存储器件及其制造方法

[0001] 相关申请的交叉引用

[0002] 本申请要求于2018年11月12日在韩国知识产权局提交的 No.10-2018-0138049韩国专利申请的优先权,其全部内容通过引用合并于此。

技术领域

[0003] 本发明构思涉及半导体器件和/或其制造方法,更具体地,涉及高度集成的三维半导体存储器件和/或其制造方法。

背景技术

[0004] 半导体器件已经高度集成,以满足客户对高性能和低制造成本的需求。由于半导体器件的集成是决定产品价格的重要因素,因此对高集成度的需求日益增加。因此,已经提出了其中存储器单元是三维地布置的三维半导体存储器件。

发明内容

[0005] 本发明构思的一些示例实施例提供了具有增加的集成度的三维半导体存储器件和/或其制造方法。

[0006] 根据本发明构思的示例实施例,一种三维半导体存储器件可以包括:衬底,包括单元阵列区和连接区;电极结构,包括交替地堆叠在衬底上的多个电极和多个介电层,电极结构在连接区上具有阶梯部分;蚀刻停止结构,在阶梯部分上;以及多个接触插塞,在连接区上,所述多个接触插塞穿透蚀刻停止结构并且分别连接到电极的对应焊盘部分。蚀刻停止结构可以包括蚀刻停止图案和水平介电层,水平介电层具有均匀的厚度并且覆盖蚀刻停止图案的顶表面和底表面。

[0007] 根据本发明构思的示例实施例,一种三维半导体存储器件可以包括:衬底,包括单元阵列区和连接区;电极结构,包括沿垂直于衬底的顶表面的第一方向交替地堆叠的多个电极和多个介电层,电极结构沿平行于衬底的顶表面的第二方向延伸,电极结构在连接区上具有阶梯部分;蚀刻停止图案,覆盖阶梯部分;以及公共源极插塞,沿第一方向穿透电极结构并沿第二方向延伸。公共源极插塞的侧壁与蚀刻停止图案的侧壁之间的第一距离可以不同于公共源极插塞的侧壁与电极的侧壁之间的第二距离。

[0008] 根据本发明构思的示例实施例,一种三维半导体存储器件可以包括:衬底,包括单元阵列区和连接区;电极结构,包括交替地堆叠在衬底上的多个电极和多个介电层,电极结构在连接区上具有阶梯部分;蚀刻停止结构,覆盖阶梯部分;以及多个接触插塞,在连接区上,接触插塞穿透蚀刻停止结构并且分别连接到电极的对应焊盘部分。蚀刻停止结构可以包括蚀刻停止图案,所述蚀刻停止图案包括与介电层的介电材料不同的介电材料,并且在其中具有沿阶梯部分限定的界面。

[0009] 根据本发明构思的示例实施例,一种三维半导体存储器件可以包括:衬底,包括单元阵列区和连接区;电极结构,包括交替地堆叠在衬底上的多个电极和多个介电层,电

极结构在连接区上具有阶梯部分；水平阻挡介电层，覆盖电极的顶表面和底表面二者；蚀刻停止结构，在阶梯部分上；以及多个接触插塞，在连接区上，接触插塞穿透蚀刻停止结构并且分别连接到电极的对应焊盘部分。蚀刻停止结构可以包括蚀刻停止图案和水平介电层，水平介电层覆盖蚀刻停止图案的顶表面和底表面二者，并且包括与水平阻挡介电层的材料相同的材料。

[0010] 根据本发明构思的示例实施例，一种制造三维半导体存储器件的方法可以包括：设置包括单元阵列区和连接区的衬底；在衬底上形成模制结构，模制结构包括交替地彼此堆叠的多个牺牲层和多个介电层，模制结构在连接区上具有阶梯部分；形成焊盘牺牲层以共形地覆盖模制结构的阶梯部分；用电极替换牺牲层；以及用蚀刻停止层替换焊盘牺牲层。

[0011] 一些示例实施例的细节包括在说明书和附图中。

附图说明

[0012] 图1示出了根据本发明构思的示例实施例的三维半导体存储器件的平面视图。

[0013] 图2A、图2B和图2C示出了沿图1的IIA-IIA'线、IIB-IIB'线和IIC-IIC'线截取的、示出根据本发明构思的示例实施例的三维半导体存储器件的截面视图。

[0014] 图3A、图3B、图3C和图3D示出了图2A中所示的截面III的放大视图。

[0015] 图4A、图4B和图4C示出了图2B中所示的截面IV的放大视图。

[0016] 图5A和图5B示出了图2C中所示的截面V的放大视图。

[0017] 图6至图12示出了示出根据本发明构思的一些示例实施例的三维半导体存储器件的截面视图。

[0018] 图13A至图21A、图13B至图21B和图13C至图21C示出了沿图1的IIA-IIA'线、IIB-IIB'线和IIC-IIC'线截取的、示出根据本发明构思的示例实施例的制造三维半导体存储器件的方法的截面视图。

具体实施方式

[0019] 在下文中将结合附图详细讨论根据本发明构思的一些示例实施例的三维半导体存储器件及其制造方法。

[0020] 尽管在示例实施例的描述中使用了术语“相同”或“完全相同”，但应理解可能存在一些不精确性。因此，当一个元件被称为与另一个元件相同时，应当理解，一个元件或值是在期望的制造或操作公差范围（例如， $\pm 10\%$ ）内与另一个元件相同。

[0021] 当在本说明书中结合数值使用术语“大约”或“基本”时，旨在相关数值包括围绕所述数值的制造或操作公差（例如， $\pm 10\%$ ）。此外，当词语“大体上”和“基本”与几何形状结合使用时，不旨在要求该几何形状的精度，而在对该形状的宽容度在本公开的范围之内。

[0022] 图1示出了示出根据本发明构思的示例实施例的三维半导体存储器件的平面视图。图2A、图2B和图2C示出了沿图1的IIA-IIA'线、IIB-IIB'线和IIC-IIC'线截取的、示出根据本发明构思的示例实施例的三维半导体存储器件的截面图。

[0023] 图3A、图3B、图3C和图3D示出了图2A中所示的截面III的放大视图。图4A、图4B和图4C示出了图2B中所示的截面IV的放大视图。图5A和图5B示出了图2C中所示的截面V的放

大视图。

[0024] 参照图1、图2A、图2B和图2C,衬底10可以包括单元阵列区 CAR和与单元阵列区CAR相邻的连接区CNR。衬底10可以是半导体材料(例如,硅晶片)、介电材料(例如,玻璃)和覆盖有介电材料的半导体或导体中的一种。例如,衬底10可以是具有第一导电类型的硅晶片。

[0025] 单元阵列区CAR可以包括由多个三维地布置的存储器单元组成的存储器单元阵列。连接区CNR可以包括将存储器单元阵列电连接到行解码器的连接线结构。

[0026] 在某些示例实施例中,三维半导体存储器件可以是垂直NAND闪存器件。单元阵列区CAR上可以设置有沿垂直于第一方向D1和第二方向D2的第三方向D3延伸的单元串。每个单元串可以包括串联连接的串选择晶体管、存储单元晶体管和地选择晶体管。每个存储单元晶体管可以包括数据存储元件。

[0027] 电极结构ST可以设置在衬底10上并且可以包括沿垂直于衬底10的顶表面的第三方向D3交替地堆叠的介电层ILD和电极EL。电极结构ST可以沿第一方向D1从单元阵列区CAR朝向连接区CNR延伸。缓冲介电层11可以包括在电极结构ST与衬底10之间的氧化硅层。

[0028] 电极EL可以具有相同或基本相似的厚度,介电层ILD可以具有取决于半导体存储器件的特性而改变的厚度。每个介电层ILD可以比每个电极EL更薄。在介电层ILD中,覆盖最下面的电极EL的一个介电层ILD(下文中被称为最下面的介电层ILDa)可以比其他的介电层ILD厚。

[0029] 电极EL可以例如包括选自掺杂半导体(例如,掺杂硅)、金属(例如,钨、铜或铝)、导电金属氮化物(例如,氮化钛或氮化钽)或过渡金属(例如,钛或钽)中的至少一种。介电层ILD可以例如包括氧化硅层。

[0030] 电极结构ST可以在连接区CNR上具有阶梯部分,每个电极EL可以在连接区CNR上具有焊盘部分。当在平面视图中时,电极EL的焊盘部分可以沿彼此相交的第一方向D1和第二方向D2布置,并且可以位于与衬底10的顶表面不同的水平高度处。

[0031] 电极EL可以具有沿第一方向D1的长度,该长度随着距衬底10的距离的增加而减小。电极EL可以具有沿第一方向D1以规则的间距间隔开的侧壁。在连接区CNR上,每个电极EL的侧壁可以与直接覆盖介电层ILD的侧壁竖直对齐。另外,两个竖直相邻的电极EL的侧壁可以彼此对齐。在某些示例实施例中,电极结构ST的阶梯部分可以改变成多种形状。

[0032] 在连接区CNR上,平坦化掩埋介电层55可以覆盖电极结构ST的阶梯部分。例如,平坦化掩埋介电层55可以覆盖电极EL的焊盘部分。平坦化掩埋介电层55可以具有基本平坦的顶表面,并且包括单个介电层或多个堆叠的介电层。平坦化掩埋介电层55可以包括氧化硅层。

[0033] 在某些示例实施例中,在连接区CNR上,蚀刻停止结构ES可以设置在平坦化掩埋介电层55与电极结构ST之间。焊盘介电层25也可以设置在蚀刻停止结构ES与电极结构ST之间。

[0034] 蚀刻停止结构ES和焊盘介电层25可以沿第一方向D1延伸,并且可以共形地覆盖电极结构ST的阶梯部分。蚀刻停止结构ES可以包括相对于电极结构ST的电极EL和介电层ILD、焊盘介电层25和平坦化掩埋介电层55具有蚀刻选择性的材料。焊盘介电层25可以包括与电极结构ST的介电层ILD的介电材料相同的介电材料。

[0035] 参照图4A和图5A,蚀刻停止结构ES可以包括蚀刻停止图案45、水平介电层HL和第一缓冲介电层41。

[0036] 蚀刻停止图案45可以包括相对于电极结构ST的介电层ILD具有蚀刻选择性的材料。在电极EL的焊盘部分上,蚀刻停止图案45的厚度可以大于介电层ILD的厚度。蚀刻停止图案45的厚度可以大于电极EL的厚度。蚀刻停止图案45可以包括与水平介电层HL的介电材料不同的介电材料。例如,蚀刻停止图案45可以包括氮化硅层或氮氧化硅层。

[0037] 蚀刻停止图案45可以在其内部具有不连续的界面S。在本说明书中,术语“不连续界面S”可以表示在材料的成分差异、材料的颗粒差异或空隙方面通过分析工具(例如,透射电子显微镜(TEM)或扫描电子显微镜(SEM))检测到的材料或边界的存在。蚀刻停止图案45的不连续界面S可以沿电极结构ST的阶梯部分形成。例如,蚀刻停止图案45的不连续界面S可以是接缝。又例如,蚀刻停止图案45可以包括在其内部的部分中形成的空隙。

[0038] 水平介电层HL可以具有基本均匀的厚度,并且可以覆盖蚀刻停止图案45的顶表面和底表面。例如,水平层HL可以具有在焊盘介电层25与蚀刻停止图案45的底表面之间的下部区段以及在平坦化掩埋介电层55与蚀刻停止图案45的顶表面之间的上部区段。水平介电层HL的上部区段和下部区段可以包括相同的材料。

[0039] 水平阻挡介电层HBLK可以覆盖电极EL的顶表面和底表面,并且还覆盖电极EL的第一侧壁,其与将在下面时论的单元竖直结构CVS和虚设竖直结构DVS相邻。水平介电层HL的上部区段和下部区段的厚度均可以小于电极EL的第一侧壁上的水平阻挡介电层HBLK的厚度。

[0040] 水平介电层HL可以包括与水平阻挡介电层HBLK的材料相同的材料。水平介电层HL和水平阻挡介电层HBLK可以包括相对于平坦化掩埋介电层55、焊盘介电层25和蚀刻停止图案45具有蚀刻选择性的介电材料。在一些示例实施例中,水平介电层HL和水平阻挡介电层HBLK可以包括与第一缓冲介电层41的介电材料不同的介电材料。例如,水平介电层HL和水平阻挡介电层HBLK可以包括高k介电层,例如氧化铝层或氧化铪层。

[0041] 第一缓冲介电层41可以设置在蚀刻停止图案45与水平介电层HL之间。类似地,水平介电层HL、第一缓冲介电层41可以具有基本均匀的厚度,并且可以覆盖蚀刻停止图案45的顶表面和底表面。

[0042] 第一缓冲介电层41可以包括相对于蚀刻停止图案45和水平介电层HL具有蚀刻选择性的介电材料。例如,第一缓冲介电层41可以包括氧化硅层。

[0043] 第一缓冲介电层41可以延伸到电极结构ST的侧壁上。例如,参照图3A、图3B、图3C和图5A,第一缓冲介电层41可以延伸到电极EL的侧壁和介电层ILD的侧壁上,并且可以直接接触电极EL的侧壁。在这种情况下,第一缓冲介电层41的一部分可以设置在公共源极插塞CSP和与公共源极插塞CSP相邻的电极EL的第二侧壁之间。第一缓冲介电层41在蚀刻停止图案45与水平介电层HL之间的厚度可以大于第一缓冲介电层41在电极EL的第二侧壁上的厚度。第一缓冲介电层41的厚度可以大于水平阻挡介电层HBLK的厚度。

[0044] 参照图5A,公共源极插塞CSP与蚀刻停止图案45的一个侧壁之间的第一水平距离A1可以不同于公共源极插塞CSP和与公共源极插塞CSP相邻的电极EL的第二侧壁之间的第二水平距离A2。例如,第一水平距离A1可以大于第二水平距离A2。蚀刻停止图案45可以具有与图1中所示的第一分离结构SS1和第三分离结构SS3相邻的圆形侧壁。

[0045] 参照图3D、图4B和图5B,蚀刻停止结构ES可以不包括第一缓冲介电层41。例如,蚀刻停止结构ES可以包括蚀刻停止图案45和水平介电层HL,水平介电层HL可以直接接触蚀刻停止图案45的顶表面和底表面。

[0046] 参照图4C,包括与电极EL的导电材料相同的导电材料的残留导电图案REL可以部分地设置在蚀刻停止图案45和第一缓冲介电层41之间。残留导电图案REL可以局部地定位在电极结构ST的一个或多个阶梯上。

[0047] 在某些示例实施例中,在单元阵列区CAR上,多个单元竖直结构VS可以穿透电极结构ST并且与衬底10连接。当在平面视图中时,单元竖直结构CVS可以沿一个方向或呈Z字形布置。单元竖直结构CVS可以具有圆形顶表面。

[0048] 单元竖直结构CVS可以包括半导体材料,例如硅(Si)、锗(Ge)或其混合物。包括半导体材料的单元竖直结构CVS可以用作被包括在垂直NAND闪存器件的单元串中的地选择晶体管、串选择晶体管和存储单元晶体管的沟道。

[0049] 每个单元竖直结构CVS可以包括下半导体图案LSP、上半导体图案USP和垂直介电图案VP。位线接触焊盘PAD可以位于上半导体图案USP的顶端上。位线接触焊盘PAD可以包括掺杂杂质的半导体材料。

[0050] 下半导体图案LSP可以直接接触衬底10,并且可以包括从衬底10生长的柱状外延层。栅极介电层15可以设置在下半导体图案LSP的侧壁的一部分上。栅极介电层15可以设置在最下面的电极EL与下半导体图案LSP之间。栅极介电层15可以包括氧化硅层(例如,热氧化物层)。

[0051] 上半导体图案USP可以直接接触下半导体图案LSP或衬底10,并且形状可以是带有封闭底端的“U”形或管形。如图3A至图3D中所示,上半导体图案USP可以具有填充有包括介电材料的掩埋介电图案VI的内部。垂直介电图案VP可以围绕上半导体图案USP的侧壁。

[0052] 上半导体图案USP可以包括半导体材料,例如硅(Si)、锗(Ge)或其混合物。上半导体图案USP可以具有与下半导体图案LSP的晶体结构不同的晶体结构;例如,上半导体图案USP可以具有选自单晶结构、非晶结构和多晶结构中的至少一种。

[0053] 参照图3A、图3B、图3C和图3D,垂直介电图案VP可以包括隧道介电层TIL、电荷存储层CIL和阻挡介电层BLK,并且构成NAND闪存器件的数据存储结构。电荷存储层CIL可以是陷阱介电层、浮栅电极或包括导电纳米点的介电层。例如,电荷存储层CIL可以包括氮化硅层、氮氧化硅层、富硅氮化物层、纳米晶硅层和层叠陷阱层中的一个或多个。隧道介电层TIL可以是其带隙大于电荷存储层CIL的带隙的材料之一,阻挡介电层BLK可以是高k介电层(例如,氧化铝层或氧化铪层)。

[0054] 参照图3A、图3B和图3C,第一缓冲介电层41可以直接覆盖电极EL的侧壁。参照图3B和图3C,残留侧壁牺牲图案43R可以设置在第一缓冲介电层41与公共源极插塞CSP之间。残留侧壁牺牲图案43R可以包括与连接区CNR上的蚀刻停止图案45的材料相同的材料。如图3B中所示,残留侧壁牺牲图案43R可以围绕公共源极插塞CSP的侧壁,并且可以围绕公共源极插塞CSP的一部分。在一些示例实施例中(例如,图3D),在公共源极插塞CSP和电极EL的侧壁之间可以不存在第一缓冲介电层41,残留侧壁牺牲图案43R可以填充公共源极插塞CSP与电极EL的侧壁之间的空间。

[0055] 水平阻挡介电层HBLK可以设置在垂直介电图案VP与电极EL的侧壁之间。水平阻

挡介电层HBLK可以覆盖电极EL的侧壁,并且还可以覆盖电极EL的顶表面和底表面。水平阻挡介电层HBLK可以是NAND闪存器件的数据存储结构的一部分,并且可以包括由诸如氧化铝层或氧化钪层等高k介电层组成的阻挡介电层。

[0056] 水平阻挡介电层HBLK可以在公共源极插塞CSP与介电层ILD的侧壁之间连续延伸。参照图4A和5A,水平阻挡介电层HBLK可以连接到水平介电层HL。

[0057] 在连接区CNR上,虚设竖直结构DVS可以穿透平坦化掩埋介电层55、蚀刻停止结构ES、焊盘介电层25和电极结构ST。随着虚设竖直结构DVS变得更远离单元阵列区CAR,虚设竖直结构DVS穿透的电极EL的数量可以减少。

[0058] 虚设竖直结构DVS可以具有与单元竖直结构CVS的堆叠结构和材料相同或基本相似的堆叠结构和材料。例如,像单元竖直结构CVS一样,每个虚设竖直结构DVS可以包括下半导体图案、上半导体图案和竖直介电图案。

[0059] 虚设竖直结构DVS可以具有与单元竖直结构CVS的竖直长度相同或基本相似的竖直长度。例如,虚设竖直结构DVS的顶表面可以位于与单元竖直结构CVS的顶表面相同或基本相似的水平高度处。虚设竖直结构DVS的宽度可以大于单元竖直结构CVS的宽度。例如,虚设竖直结构DVS的每个顶表面的形状可以是条形或具有长轴和短轴的椭圆形。

[0060] 多个虚设竖直结构DVS可以穿透每个电极EL的焊盘部分。例如,四个虚设竖直结构DVS可以穿透每个电极EL的焊盘部分,但是本发明构思不限于此。虚设竖直结构DVS的布置和数量可以有多种改变。

[0061] 第一层间介电层60可以设置在平坦化掩埋介电层55上,并且可以覆盖单元竖直结构CVS的顶表面和虚设竖直结构DVS的顶表面。第一层间介电层60还可以覆盖蚀刻停止结构ES的最上顶表面和焊盘介电层25的最上顶表面。

[0062] 当在平面视图中时,电极结构ST可以设置在沿第一方向D1延伸并且与电极结构ST平行地设置的第一分离结构SS1之间。第一分离结构SS1可以从单元阵列区CAR朝向连接区CNR延伸,并且可以穿透第一层间介电层60、平坦化掩埋介电层55、蚀刻停止结构ES、焊盘介电层25以及电极结构ST。

[0063] 在单元阵列区CAR上,第二分离结构SS2可以设置在第一分离结构SS1之间并且沿第二方向D2以规则的间距彼此间隔开。第二分离结构SS2可以穿透第一层间介电层60和电极结构ST,而沿第一方向D1延伸。

[0064] 在连接区CNR上,第三分离结构SS3可以设置在第一分离结构SS1之间并且沿第二方向D2彼此间隔开。第三分离结构SS3可以穿透第一层间介电层60、平坦化掩埋介电层55、蚀刻停止结构ES、焊盘介电层25和电极结构ST,而沿第一方向D1延伸。第三分离结构SS3可以沿第一方向D1与第二分离结构SS2间隔开。

[0065] 第一分离结构SS1、第二分离结构SS2和第三分离结构SS3均可以包括公共源极插塞CSP和在公共源极插塞CSP与电极结构ST之间的侧壁间隔物SP,公共源极插塞CSP包括导电材料。

[0066] 侧壁间隔物SP可以包括不同于蚀刻停止图案45的介电材料,并且可以直接接触连接区CNR上的蚀刻停止图案45的侧壁。侧壁间隔物SP可以包括朝向蚀刻停止图案45和电极EL水平突出的突出部。参照图5A,第一缓冲介电层41可以设置在侧壁间隔物SP和电极结构ST之间。侧壁间隔物SP可以包括与第一缓冲介电层41的介电材料相同的介电材料。

[0067] 公共源极插塞CSP可以耦合到衬底10中形成的公共源极区CSR。公共源极区CSR可以沿第一方向D1并且平行于电极结构ST延伸。公共源极区CSR可以包括衬底10中掺杂的第二导电类型杂质。公共源极区CSR可以例如包括N型杂质(例如,砷(As)或磷(P))。在其他示例实施例中,第一分离结构SS1、第二分离结构SS2和第三分离结构SS3均可以由介电材料组成的线性柱结构。

[0068] 第一层间介电层60上可以设置有第二层间介电层70,第二层间介电层70覆盖第一分离结构SS1、第二分离结构SS2和第三分离结构SS3的顶表面。

[0069] 在单元阵列区CAR上,第一位线接触插塞BPLG1可以穿透第一层间介电层60和第二层间介电层70,并且与对应的单元竖直结构CVS连接。

[0070] 在连接区CNR上,单元接触插塞CPLG可以穿透第一层间介电层60和第二层间介电层70、平坦化掩埋介电层55和蚀刻停止结构ES,并且可以与电极EL的对应焊盘部分连接。

[0071] 单元接触插塞CPLG可以具有位于相同或基本相似的垂直高度处的顶表面,并且可以具有彼此不同的垂直长度。单元接触插塞CPLG的顶表面可以基本是共面的,单元接触插塞CPLG的垂直长度可以随着接近单元阵列区CAR而减小。

[0072] 每个单元接触插塞CPLG可以与穿透电极EL的每个焊盘部分的虚设竖直结构DVS间隔开。单元接触插塞CPLG的顶表面可以位于比虚设竖直结构DVS的顶表面和第一分离结构SS1、第二分离结构SS2和第三分离结构SS3的顶表面高的垂直高度处。每个单元接触插塞CPLG可以具有一部分与蚀刻停止结构ES直接接触的侧壁。

[0073] 每个单元接触插塞CPLG可以包括阻挡金属层和金属层,其中阻挡金属层包括金属氮化物,例如TiN、Ta₂N或WN,金属层例如包括金属Al、Ti、Ta、Co或Cu。

[0074] 在单元阵列区CAR上,第二层间介电层70上可以设置有辅助位线SBL,其主轴沿第二方向D2延伸。每个辅助位线SBL可以通过第一位线接触插塞BPLG1连接到两个相邻的单元竖直结构CVS。

[0075] 在连接区CNR上,下连接线LCL可以设置在第二层间介电层70上。下连接线LCL可以耦合到对应的单元接触插塞CPLG。下连接线LCL可以通过单元接触插塞CPLG电连接到电极EL的对应焊盘部分。

[0076] 第二层间介电层70上可以设置有覆盖辅助位线SBL和下连接线LCL的第三层间介电层80。

[0077] 在单元阵列区CAR上,位线BL可以设置在第三层间介电层80上,上连接线UCL可以设置在连接区CNR上的第三层间介电层80上。位线BL可以沿第二方向D2延伸,而跨越电极结构ST,并且可以通过第二位线接触插塞BPLG2连接到辅助位线SBL。上连接线UCL可以通过上接触插塞耦合到对应的下连接线LCL。

[0078] 图6至图12示出了示出根据本发明构思的一些示例实施例的三维半导体存储器件的截面视图。为了简化说明,可以省略对与上面参考图3讨论的三维半导体存储器件的技术特征相同的技术特征的详细描述,并且将描述其不同之处。

[0079] 参照图6,蚀刻停止结构ES可以在电极结构ST中形成的每个阶梯的侧壁上以及每个阶梯的顶表面上具有不同的厚度。蚀刻停止结构ES可以在覆盖每个阶梯的部分处具有圆形轮廓。上阶梯上蚀刻停止结构ES的厚度可以不同于下阶梯上蚀刻停止结构ES的厚度。

[0080] 参照图7,蚀刻停止结构ES可以从连接区CNR朝向单元阵列区CAR延伸。例如,在单

元阵列区CAR和连接区CNR上,蚀刻停止结构ES可以共形地覆盖电极结构ST的顶表面。蚀刻停止结构ES可以在单元阵列区CAR的电极结构ST上具有平坦化部分以及在连接区CNR的电极结构ST上具有阶梯部分。

[0081] 平坦化掩埋介电层55可以覆盖蚀刻停止结构ES的阶梯部分,并且其顶表面可以处于与蚀刻停止结构ES的平坦化部分的顶表面相同的水平高度处。虚设层间介电层57可以覆盖蚀刻停止结构ES的平坦化部分和平坦化掩埋介电层55。

[0082] 单元竖直结构CVS可以穿透虚设层间介电层57、蚀刻停止结构ES的平坦化部分和电极结构ST。

[0083] 如上所述,蚀刻停止结构ES可以包括水平介电层HL、第一缓冲介电层41和蚀刻停止图案45。蚀刻停止图案45的顶表面和底表面可以由水平介电层HL和第一缓冲介电层41围绕。

[0084] 参照图8,衬底10可以包括单元阵列区CAR、连接区CNR,并且还包括外围电路区PCR。连接区CNR可以位于单元阵列区CAR与外围电路区PCR之间。

[0085] 在外围电路区PCR上,衬底10上可以设置有诸如行和列解码器、页面缓冲器和控制电路等外围逻辑电路。外围逻辑电路可以例如包括高压和低压晶体管、电阻器和电容器。在外围电路区PCR上,外围栅极堆叠PGS可以设置为在衬底10上彼此间隔开。源极/漏极杂质区13可以设置在衬底10中每个外围栅极堆叠PGS的相对两侧上。在单元阵列区CAR上,衬底10上可以设置有与外围逻辑电路间隔开的电极结构ST。

[0086] 电极结构ST可以沿第一方向D1从单元阵列区CAR朝向连接区CNR延伸,并且可以在连接区CNR上具有阶梯部分。缓冲介电层11可以包括介于电极结构ST与衬底10之间的氧化硅层。缓冲介电层11可以延伸到外围电路区PCR上并且共形地覆盖外围栅极堆叠PGS。

[0087] 电极结构ST可以包括竖直和交替堆叠的电极EL和介电层ILD。在电极结构ST中,覆盖最下面的电极EL的最下面的介电层ILDa可以从单元阵列区CAR朝向外围电路区PCR连续地延伸。最下面的电极EL的顶表面可以低于外围栅极堆叠PGS的顶表面。

[0088] 在外围电路区PCR上,虚设牺牲图案DP可以共形地覆盖外围栅极堆叠PGS。虚设牺牲图案DP可以包括相对于介电层ILD具有蚀刻选择性的介电材料。例如,虚设牺牲图案DP可以包括氮化硅层。虚设牺牲图案DP可以由电极结构ST的最下面的介电层ILDa覆盖。

[0089] 在连接区CNR上,蚀刻停止结构ES可以共形地覆盖电极结构ST。焊盘介电层25可以设置在蚀刻停止结构ES与电极结构ST之间,并且可以延伸到外围电路区PCR的最下面的介电层ILDa上。

[0090] 在某些示例实施例中,残留焊盘牺牲层37可以设置在外围电路区PCR的焊盘介电层25上。残留焊盘牺牲层37可以包括与蚀刻停止图案45的材料相同的材料,并且可以比蚀刻停止图案45厚。水平介电层HL的一部分和第一缓冲介电层41的一部分可以介于残留焊盘牺牲层37与蚀刻停止图案45的一个侧壁之间。

[0091] 在外围电路区PCR上,外围接触插塞PPLG可以穿透第一层间介电层60和第二层间介电层70、平坦化掩埋介电层55、残留焊盘牺牲层37、焊盘介电层25、最下面的介电层ILDa和虚设牺牲图案DP,并且可以连接到源极/漏极杂质区13。当在外围电路区PCR上形成外围接触插塞PPLG时,残留焊盘牺牲层37可以用作蚀刻停止层。

[0092] 在外围电路区PCR上,外围电路连接线PCL可以设置在第二层间介电层70上并且

耦接到外围接触插塞PPLG。

[0093] 参照图9A和图9B,根据本发明构思的示例实施例的三维半导体存储器件可以包括半导体衬底100上的外围逻辑结构PS和外围逻辑结构PS上的单元阵列结构CS。

[0094] 外围逻辑结构PS可以包括集成在半导体衬底100上的外围逻辑电路PTR和覆盖外围逻辑电路PTR的下掩埋介电层150。

[0095] 外围电路连接线33可以通过外围电路接触插塞31电连接到外围逻辑电路PTR。例如,外围电路接触插塞31和外围电路连接线33可以耦接到NMOS和PMOS晶体管。

[0096] 单元阵列结构CS可以包括上面参考图2A、图2B和图2C讨论的三维半导体存储器件。例如,单元阵列结构CS可以包括外围逻辑结构PS上的衬底10、衬底10上的电极结构ST以及共形地覆盖电极结构ST的阶梯部分的蚀刻停止结构ES。单元阵列结构CS可以通过竖直穿透单元阵列结构CS的一部分的直通连接结构TVS连接到外围逻辑结构PS。

[0097] 参照图10、图11和图12,电极结构ST可以设置在衬底10上,并且可以在连接区CNR上具有阶梯部分。阶梯部分的每个阶梯可以包括一个电极EL和一个介电层ILD。

[0098] 参照图10,多个蚀刻停止结构ES1和ES2可以堆叠在连接区CNR上的电极结构ST上。例如,第一蚀刻停止结构ES1和第二蚀刻停止结构ES2可以共形地覆盖电极结构ST的阶梯部分。

[0099] 类似于上面参考图2A、图2B和图2C讨论的蚀刻停止结构ES,第一蚀刻停止结构ES1和第二蚀刻停止结构ES2均可以包括蚀刻停止图案45、水平介电层HL和第一缓冲介电层41。

[0100] 第一蚀刻停止结构ES1和电极结构ST之间可以设置有厚度均匀的第一焊盘介电层25,第一蚀刻停止结构ES1和第二蚀刻停止结构ES2之间可以设置有厚度均匀的第二焊盘介电图案27。

[0101] 参照图10,单元接触插塞CPLG可以穿透连接区CNR上的第一蚀刻停止结构ES1和第二蚀刻停止结构ES2,并且可以分别连接到电极EL的对应焊盘部分。

[0102] 参照图11和图12,第一蚀刻停止结构ES1和第二蚀刻停止结构ES2可以设置在电极结构ST的阶梯部分上,第二蚀刻停止结构ES2可以覆盖第一蚀刻停止结构ES1的一部分(不是整体)。

[0103] 例如,如图11中所示,第二蚀刻停止结构ES2可以共形地覆盖电极结构ST的阶梯部分的上部。因此,耦接到处于相对高水平高度处的电极EL的单元接触插塞CPLG可以穿透第一蚀刻停止结构ES1和第二蚀刻停止结构ES2。耦接到处于相对低水平高度处的电极EL的单元接触插塞CPLG可以仅穿透第一蚀刻停止结构ES1。

[0104] 另一个例子,如图12中所示,第二蚀刻停止结构ES2可以共形地覆盖电极结构ST的阶梯部分的中间部分。因此,耦接到处于中间水平高度处的电极EL的单元接触插塞CPLG可以穿透第一蚀刻停止结构ES1和第二蚀刻停止结构ES2。耦接到处于比所述中间水平高度高和更低的水平高度处的电极EL的单元接触插塞CPLG可以仅穿透第一蚀刻停止结构ES1。

[0105] 图13A至图21A、图13B至图21B和图13C至图21C示出了沿图1的IIA-IIA'线、IIB-IIB'线和IIC-IIC'线截取的、示出根据本发明构思的示例实施例的制造三维半导体存储器件的方法的截面视图。

[0106] 参照图1、图13A、图13B和图13C,衬底10可以设置为包括单元阵列区CAR和连接区CNR。可以形成模制结构110,以包括竖直且交替堆叠在衬底10上的牺牲层SL和介电层ILD。抛光停止层111和虚设介电层113可以顺序地形成在模制结构110上。可选地,可以设置诸如氧化硅等介电材料以在衬底10与模制结构110之间形成缓冲介电层11。

[0107] 当形成模制结构110时,牺牲层SL可以由相对于介电层ILD具有蚀刻选择性的材料形成。牺牲层SL可以包括与介电层ILD的介电材料不同的介电材料。例如,牺牲层SL可以由氮化硅层形成,介电层ILD可以由氧化硅层形成。每个牺牲层SL可以具有相同或基本相似的厚度,介电层ILD可以取决于其位置而具有不同的厚度。

[0108] 在某些示例实施例中,模制结构110可以具有阶梯部分,在阶梯部分中介电层ILD的端部暴露于连接区CNR上。例如,形成模制结构110可以包括在衬底10的整个表面上形成薄层结构(未示出),然后在薄层结构上执行阶梯图案化工艺,在薄层结构中牺牲层SL和介电层ILD竖直且交替堆叠。

[0109] 阶梯图案化工艺可以包括形成掩模图案(未示出)以覆盖单元阵列区CAR和连接区CNR上的薄层结构,然后交替地执行部分蚀刻薄层结构的工艺和缩小掩模图案的水平区域的工艺。阶梯图案化工艺可以在连接区CNR上为模制结构110设置沿第一方向D1的阶梯部分。

[0110] 沿第一方向D1形成的阶梯部分的斜率可以取决于在阶梯图案化工艺中部分蚀刻薄层时蚀刻的牺牲层SL的数量。在一些示例实施例中,当部分蚀刻薄层时,可以蚀刻两个或更多个牺牲层SL。在阶梯图案化工艺之后,可以执行焊盘蚀刻工艺,其中模制结构110被部分地蚀刻在连接区CNR上,以为模制结构110设置沿第二方向D2的阶梯。

[0111] 参照图1、图14A、图14B和图14C,可以顺序地形成焊盘介电层25和焊盘牺牲层35,以共形地覆盖模制结构110的表面。

[0112] 焊盘介电层25可以包括相对于牺牲层SL具有蚀刻选择性的介电材料(例如,氧化硅层)。

[0113] 焊盘牺牲层35可以包括相对于焊盘介电层25具有蚀刻选择性的介电材料。在某些示例实施例中,焊盘牺牲层35可以由与牺牲层SL的材料相同的材料形成。例如,焊盘牺牲层35可以是氮化硅层或氮氧化硅层。

[0114] 在形成焊盘牺牲层35之后,可以在衬底10的整个表面上形成掩埋介电层(未示出)。可以在单元阵列区CAR上沉积掩埋介电层,使其厚度大于模制结构110的厚度。掩埋介电层可以包括相对于焊盘牺牲层35具有蚀刻选择性的介电材料。掩埋介电层可以例如包括PE-TEOS(等离子体增强的原硅酸四乙酯)、O₃-TEOS(O₃-原硅酸四乙酯)、USG(未掺杂的硅酸盐玻璃)、PSG(磷硅酸盐玻璃)、BSG(硼硅酸盐玻璃)、BPSG(硼磷硅酸盐玻璃)、FSG(氟硅酸盐玻璃)、SOG(旋涂玻璃)、TOSZ(东燃硅氮烷)或其组合。

[0115] 然后,掩埋介电层可以经历平坦化工艺以形成平坦化掩埋介电层55。平坦化工艺可以包括化学机械抛光(CMP)工艺和蚀刻工艺,单元阵列区CAR上的抛光停止层111可以用作抛光终点。在平坦化工艺之后,平坦化掩埋介电层55可以在连接区CNR上具有基本平坦的顶表面。

[0116] 在形成平坦化掩埋介电层55期间,可以在单元阵列区CAR上部分地去除焊盘牺牲层35和焊盘介电层25。尽管图14A、图14B和图14C示出其中在形成平坦化掩埋介电层55期

间在单元阵列区CAR上部分地去除焊盘牺牲层35和焊盘介电层25的示例,但是根据一些示例实施例,在形成掩埋介电层之前,焊盘牺牲层35可以经历图案化工艺以去除单元阵列区CAR上的焊盘介电层25和焊盘牺牲层35。

[0117] 在形成平坦化掩埋介电层55之后,可以形成单元竖直结构CVS和虚设竖直结构DVS。虚设竖直结构DVS和单元竖直结构CVS可以同时形成,并且可以具有相同或基本相似的结构。

[0118] 在单元阵列区CAR上,单元竖直结构CVS可以穿透模制结构110和缓冲介电层11,在连接区CNR上,虚设竖直结构DVS可以穿透平坦化掩埋介电层55、焊盘牺牲层35、焊盘介电层25和模制结构110。

[0119] 形成单元竖直结构CVS和虚设竖直结构DVS可以包括形成穿透模制结构110和缓冲介电层11并暴露衬底10的竖直孔,然后在每个竖直孔中形成下半导体图案LSP和上半导体图案USP。

[0120] 在某些示例实施例中,因为焊盘介电层25包括与模制结构110的介电层ILD的材料相同的材料,并且因为焊盘牺牲层35包括与模制结构110的牺牲层SL的材料相同的材料,所以当执行各向异性蚀刻工艺以形成竖直孔时,可以在单元阵列区CAR和连接区CNR上利用相同的蚀刻条件。

[0121] 可以通过执行选择性外延生长(SEG)工艺来形成下半导体图案LSP,在选择性外延生长(SEG)工艺中暴露于竖直孔的衬底10用作籽晶层。因此,可以形成下半导体图案LSP以具有填充竖直孔的下部的柱形。

[0122] 上半导体图案USP可以通过在形成有下半导体图案LSP的竖直孔中沉积半导体层来形成,并且可以与下半导体图案LSP接触。在形成上半导体图案USP之前,可以在竖直孔中形成竖直介电图案VP。竖直介电图案VP可以是数据存储结构的一部分。

[0123] 位线接触焊盘PAD可以形成在每个上半导体图案USP的顶端上。位线接触焊盘PAD可以是杂质掺杂区,或者可以由导电材料形成。

[0124] 参照图1、图15A、图15B和图15C,可以在平坦化掩埋介电层55上形成第一层间介电层60,以覆盖单元竖直结构CVS和虚设竖直结构DVS的顶表面。可以图案化第一层间介电层60、平坦化掩埋介电层55和模制结构110以形成线形沟槽T。沟槽T可以沿第一方向D1延伸并且可以沿与第一方向D1相交的第二方向D2彼此间隔开。沟槽T可以包括从单元阵列区CAR朝向连接区CNR延伸的第一沟槽、单元阵列区CAR上的第一沟槽之间的第二沟槽以及连接区CNR上的第一沟槽之间的第三沟槽。

[0125] 沟槽T可以与单元竖直结构CVS和虚设竖直结构DVS间隔开,并且可以暴露牺牲层SL的侧壁和焊盘牺牲层35的侧壁。形成沟槽T可以允许当在平面视图中观看时模制结构110具有沿第一方向D1延伸的线性形状。

[0126] 参照图1、图16A、图16B和图16C,可以去除暴露于沟槽T的牺牲层SL,以在彼此竖直相邻的介电层ILD之间形成栅极区GR。栅极区GR可以暴露单元竖直结构CVS的部分。

[0127] 在某些示例实施例中,因为焊盘牺牲层35由与牺牲层SL的材料相同的材料形成,所以可以在去除暴露于沟槽T的焊盘牺牲层35并且去除牺牲层SL。因此,蚀刻停止区35R可以与栅极区GR一起形成。蚀刻停止区35R可以是焊盘介电层25和平坦化掩埋介电层55之间的空白空间。蚀刻停止区35R可以具有大于每个栅极区GR的竖直高度H1的竖直高度H2。

[0128] 栅极区GR和蚀刻停止区35R可以通过各向同性蚀刻工艺形成,其中利用相对于介电层ILD、焊盘介电层25和平坦化掩埋介电层55具有蚀刻选择性的蚀刻方案各向同性地蚀刻牺牲层SL和焊盘牺牲层35。例如,当牺牲层SL和焊盘牺牲层35是氮化硅层时,以及当介电层ILD、焊盘介电层25和平坦化掩埋介电层55是氧化硅层时,可以使用包括亚磷酸的蚀刻剂,使得可以各向同性地蚀刻牺牲层SL和焊盘牺牲层35,以形成栅极区GR和蚀刻停止区35R。

[0129] 参照图1、图17A、图17B和图17C,栅极介电层15可以形成在暴露于最下面的一个栅极区GR的下半导体图案LSP的侧壁上。栅极介电层15可以例如通过在包括氧原子的气氛下的退火工艺形成。因此,暴露于栅极区GR的下半导体图案LSP的侧壁可以被热氧化以形成栅极介电层15。

[0130] 可以形成水平阻挡介电层HBLK和水平介电层HL,以分别共形地覆盖栅极区GR的内壁和蚀刻停止区35R的内壁。水平阻挡介电层HBLK和水平介电层HL可以形成为在模制结构110的形成有栅极区GR和蚀刻停止区35R的表面上具有基本均匀的厚度。水平阻挡介电层HBLK和水平介电层HL可以通过化学气相沉积或原子层沉积形成。

[0131] 水平阻挡介电层HBLK和水平介电层HL可以包括单个薄层或多个薄层。在某些示例实施例中,水平阻挡介电层HBLK和水平介电层HL可以是NAND闪存器件中包括的数据存储结构的一部分。例如,水平介电层HL可以包括高k介电层(例如,氧化铝层或氧化铪层)。

[0132] 可以在其中形成有水平阻挡介电层HBLK的栅极区GR中以及其中形成有水平介电层HL的蚀刻停止区35R中形成栅极导电层CL。栅极导电层CL可以例如通过化学气相沉积或原子层沉积形成。

[0133] 因为蚀刻停止区35R的竖直厚度大于栅极区GR的竖直厚度,所以栅极导电层CL可以完全地填充栅极区GR以及部分地填充蚀刻停止区35R。例如,栅极导电层CL可以在蚀刻停止区35R中限定间隙或空白空间。另外,栅极导电层CL可以部分地或完全地填充沟槽T。

[0134] 例如,形成栅极导电层CL可以包括顺序地沉积阻挡金属层和金属层。阻挡金属层可以包括金属氮化物(例如TiN、Ta₂N或WN)。金属层可以包括金属(例如W、Al、Ti、Ta、Co或Cu)。

[0135] 参照图1、图18A、图18B和图18C,可以部分地去除沟槽T中的栅极导电层CL,以在对应的栅极区GR中局部地形成电极EL。

[0136] 例如,可以通过各向异性地蚀刻沉积在沟槽T中的栅极导电层CL来形成电极EL。又例如,可以通过各向同性地蚀刻沉积在沟槽T中的栅极导电层CL来形成电极EL。当蚀刻栅极导电层CL时,水平阻挡介电层HBLK和水平介电层HL可以用作蚀刻阻挡层,并且形成电极EL可以暴露沉积在介电层ILD的侧壁上的水平阻挡介电层HBLK和水平介电层HL。电极EL可以具有相对于介电层ILD的侧壁凹陷的侧壁。

[0137] 从沟槽T部分地去除栅极导电层CL可以形成电极结构ST,在电极结构ST中介电层ILD和电极EL交替和重复地堆叠。电极结构ST可以沿第一方向D1延伸,并且电极结构ST的侧壁可以暴露于沟槽T。衬底10也可以在相邻的电极结构ST之间暴露。

[0138] 在某些示例实施例中,当在沟槽T的侧壁上蚀刻栅极导电层CL时,也可以在蚀刻停止区35R中蚀刻栅极导电层CL以暴露在蚀刻停止区35R中沉积的水平介电层HL。

[0139] 参照图1、图19A、图19B和图19C,可以在沟槽T中顺序地形成第一缓冲介电层41和

蚀刻停止层43,以覆盖电极结构ST的侧壁。第一缓冲介电层41和蚀刻停止层43可以例如通过化学气相沉积或原子层沉积形成。

[0140] 第一缓冲介电层41可以共形地覆盖其中形成有水平介电层HL的蚀刻停止区35R,并且可以在电极结构ST的侧壁上延伸。例如,第一缓冲介电层41可以延伸到介电层ILD的侧壁和暴露于沟槽T的电极EL上。第一缓冲介电层41可以包括与水平介电层HL的介电材料不同的介电材料(例如,氧化硅)。

[0141] 蚀刻停止层43可以填充其中形成有第一缓冲介电层41的蚀刻停止区35R。蚀刻停止层43可以包括相对于第一缓冲介电层41具有蚀刻选择性的介电材料(例如,氮化硅)。蚀刻停止层43可以完全地填充蚀刻停止区35R并且可以覆盖其中形成有第一缓冲介电层41的沟槽T的侧壁。蚀刻停止层43可以部分地或完全地填充沟槽T。

[0142] 因为沉积技术用于形成蚀刻停止层43,所以蚀刻停止层43可以从蚀刻停止区35R的内壁沉积,因此可以在蚀刻停止层43内部形成接缝或空隙。

[0143] 参照图1、图20A、图20B和图20C,可以从沟槽T的内壁去除蚀刻停止层43,使得可以在蚀刻停止区35R中局部地形成蚀刻停止图案45。可以通过在蚀刻停止层43上的各向同性蚀刻工艺来形成蚀刻停止图案45。

[0144] 当在蚀刻停止层43上执行各向同性蚀刻工艺时,覆盖沟槽T的侧壁的第一缓冲介电层41可以用作蚀刻停止层。形成蚀刻停止图案45可以暴露电极EL的侧壁上沉积的第一缓冲介电层41。根据一些示例实施例(例如,图3B和图3C),蚀刻停止层43的一部分可以保留在沟槽T的侧壁上。

[0145] 通过在蚀刻停止区35R中形成蚀刻停止图案45,可以形成包括水平介电层HL、第一缓冲介电层41和蚀刻停止图案45的蚀刻停止结构ES。

[0146] 在形成蚀刻停止图案45之后,可以形成第二缓冲介电层(未示出)以覆盖沟槽T的内壁。第二缓冲介电层可以覆盖暴露于沟槽的蚀刻停止图案45的侧壁。第二缓冲介电层可以由与第一缓冲介电层41的材料相同的材料形成。在一些实施例中,可以不形成第二缓冲介电层。

[0147] 在沉积第二缓冲介电层之后,第二缓冲介电层可以经历回蚀工艺以形成覆盖电极结构ST的侧壁的侧壁间隔物SP并且在相邻的电极结构ST之间暴露衬底10。

[0148] 可以在暴露在电极结构ST之间的衬底10中形成公共源极区CSR。公共源极区CSR可以沿第一方向D1平行地延伸,并且可以沿第二方向D2彼此间隔开。可以通过向衬底10掺杂导电类型不同于衬底10的导电类型的杂质来形成公共源极区CSR。

[0149] 参照图1、图21A、图21B和图21C,可以在其中形成有侧壁间隔物SP的沟槽T中形成公共源极插塞CSP。可以通过沉积导电层以填充其中形成有侧壁间隔物SP的沟槽T,然后执行平坦化工艺直到暴露第一层间介电层60来形成公共源极插塞CSP。公共源极插塞CSP可以沿第一方向D并且与电极EL平行地延伸。

[0150] 可以在第一层间介电层60上形成第二层间介电层70,以覆盖公共源极插塞CSP。在连接区CNR上,可以形成接触孔H以穿透第二层间介电层70,第一层间介电层60和平坦化掩埋介电层55。

[0151] 可以通过在第二层间介电层70上形成蚀刻掩模(未示出),然后执行各向异性蚀刻工艺来形成接触孔H,其中使用等离子体来各向异性地蚀刻第一层间介电层60和第二层

间介电层70以及平坦化掩埋介电层55。在连接区CNR上,接触孔H可以暴露电极EL的对应端部。接触孔H可以具有不同的竖直长度(或者沿垂直于衬底10的顶表面的方向的长度)。

[0152] 当执行使用等离子体的各向异性蚀刻工艺以形成竖直长度彼此不同的接触孔H时,蚀刻停止结构ES可以用作蚀刻停止层,因此能够更早地减轻或防止在竖直长度相对较小的接触孔H中暴露电极EL。

[0153] 在通过使用蚀刻停止结构ES作为蚀刻停止层形成接触孔H之后,可以在蚀刻停止结构ES下方部分地过蚀刻焊盘介电层25和水平介电层HL。因此,电极EL的焊盘部分可以暴露于对应的接触孔H。

[0154] 参照图2A、图2B和图2C,在连接区CNR上,可以在接触孔H中形成单元接触插塞CPLG。形成单元接触插塞CPLG可以包括在接触孔H中顺序地沉积阻挡金属层和金属层以及执行平坦化工艺直到暴露第二层间介电层70的顶表面为止。

[0155] 第一位线接触插塞BPLG1可以与单元接触插塞CPLG同时形成。辅助位线SBL和下连接线LCL可以分别形成在单元阵列区CAR和连接区CNR上,第三层间介电层80可以形成在第二层间介电层70上。位线BL和上连接线UCL可以形成在第三层间介电层80上。

[0156] 根据本发明构思的一些示例实施例,可以形成蚀刻停止结构以共形地覆盖电极结构的阶梯部分,因此不管平坦化掩埋介电层和电极之间的蚀刻选择性如何,能够同时形成对应地耦合到电极的单元接触插塞。此外,当同时形成单元接触插塞以连接到对应的电极时,能够减轻或防止竖直相邻的电极之间的不期望的连接。

[0157] 此外,因为蚀刻停止结构包括介电材料,所以当在连接区上形成穿透电极结构的多个虚设竖直结构时,可以容易地执行蚀刻工艺以形成虚设竖直孔。

[0158] 尽管已经结合附图中示出的一些示例实施例描述了本发明构思,但是本领域技术人员将理解,可以在不脱离本发明构思的技术精神和基本特征的情况下对示例实施例进行各种改变和修改。对于本领域技术人员显而易见的是,在不脱离本发明构思的范围和精神的情况下,可以对其进行各种替换、修改和改变。

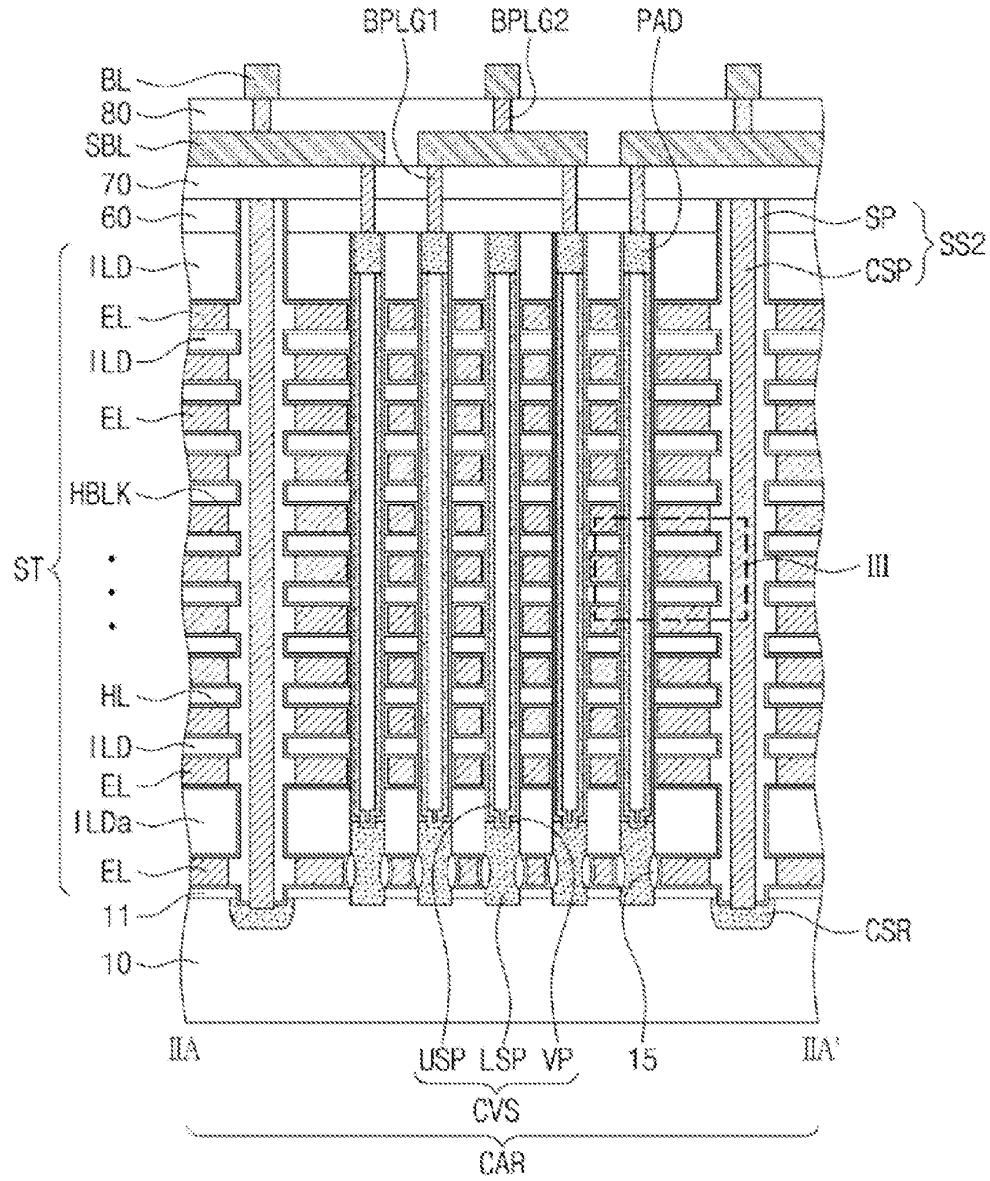


图2A

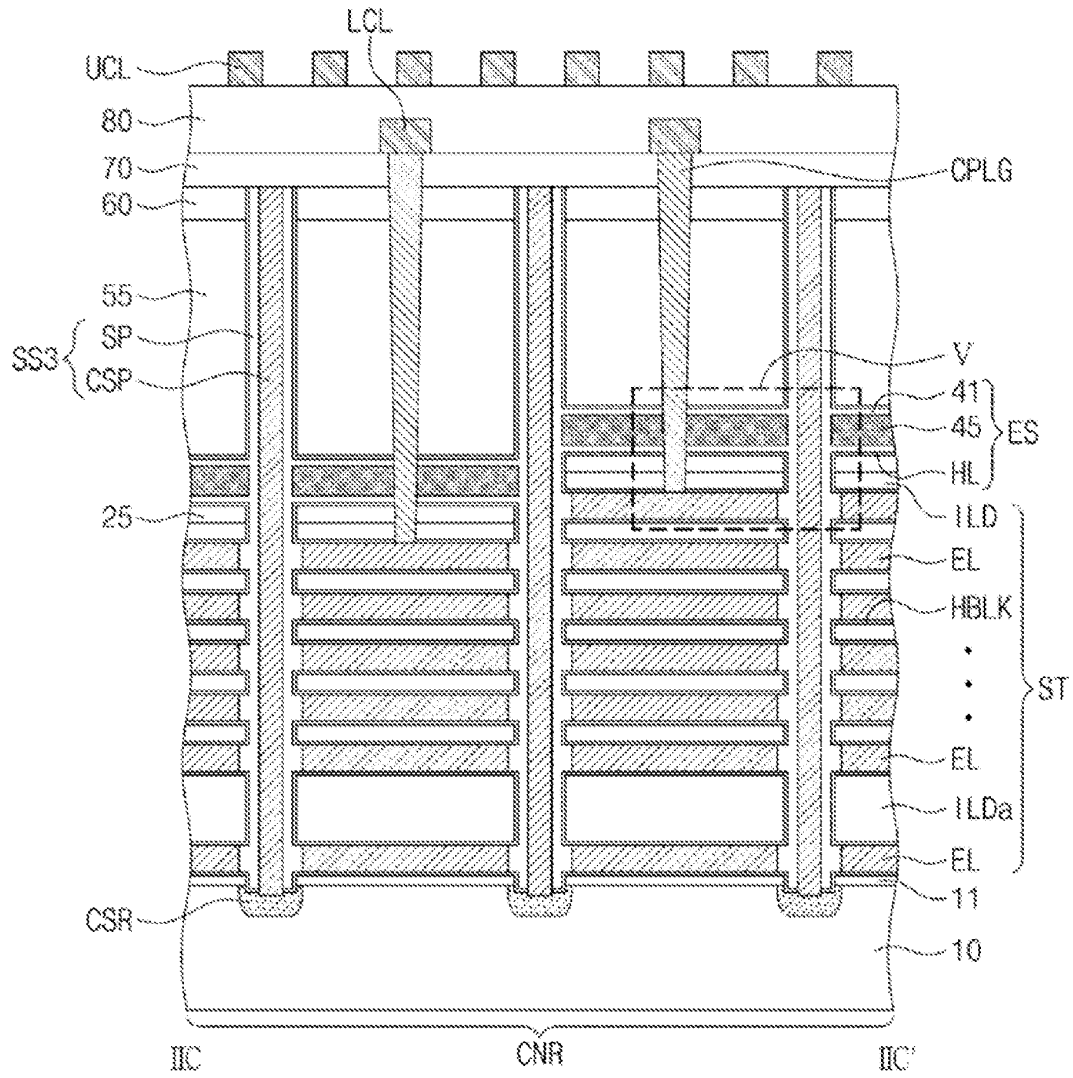


图2C

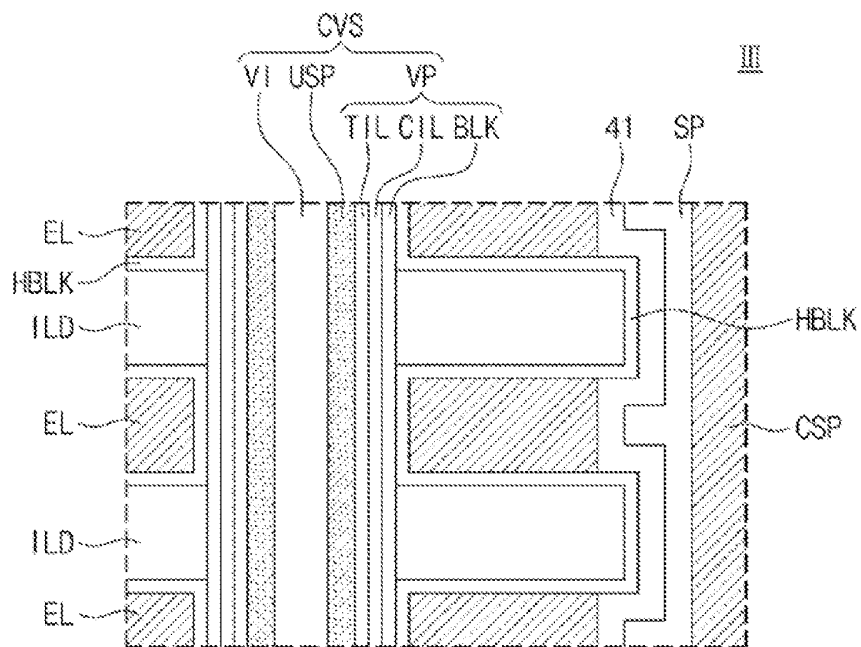


图 3A

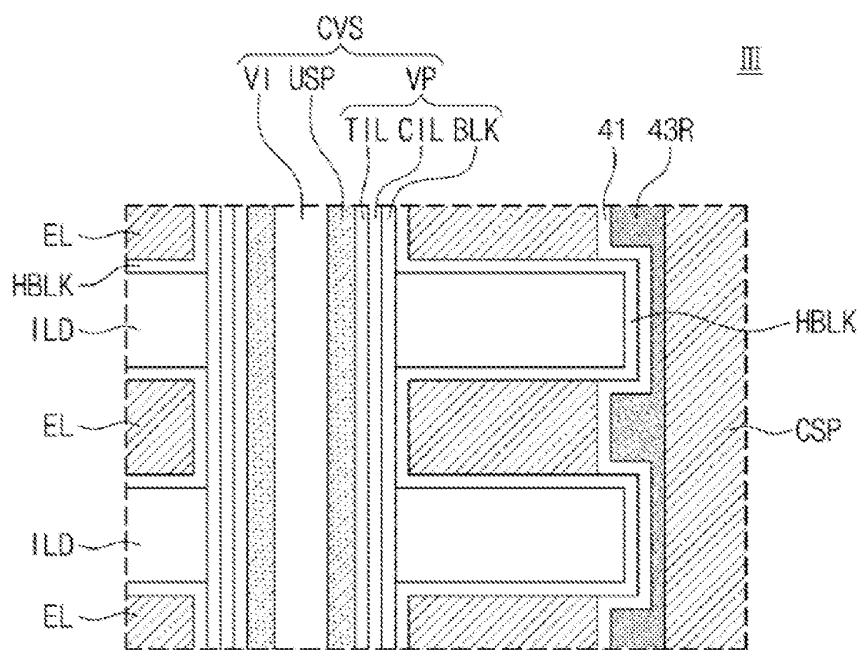


图33

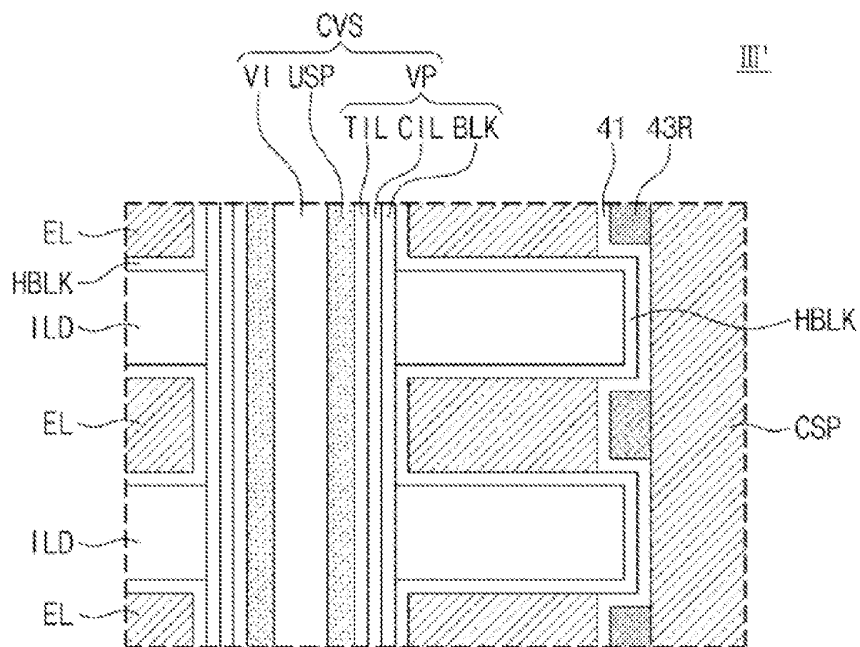


图3C

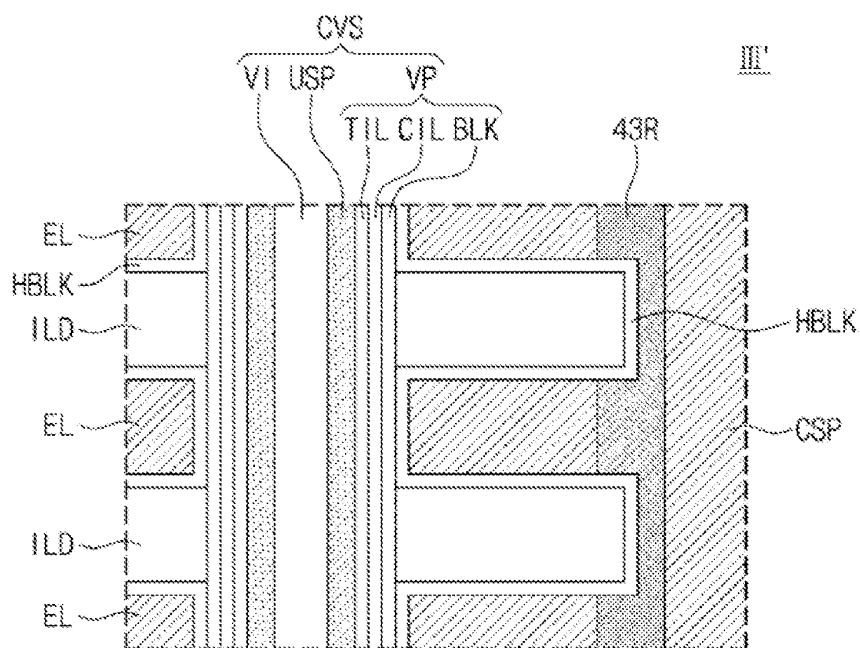


图3D

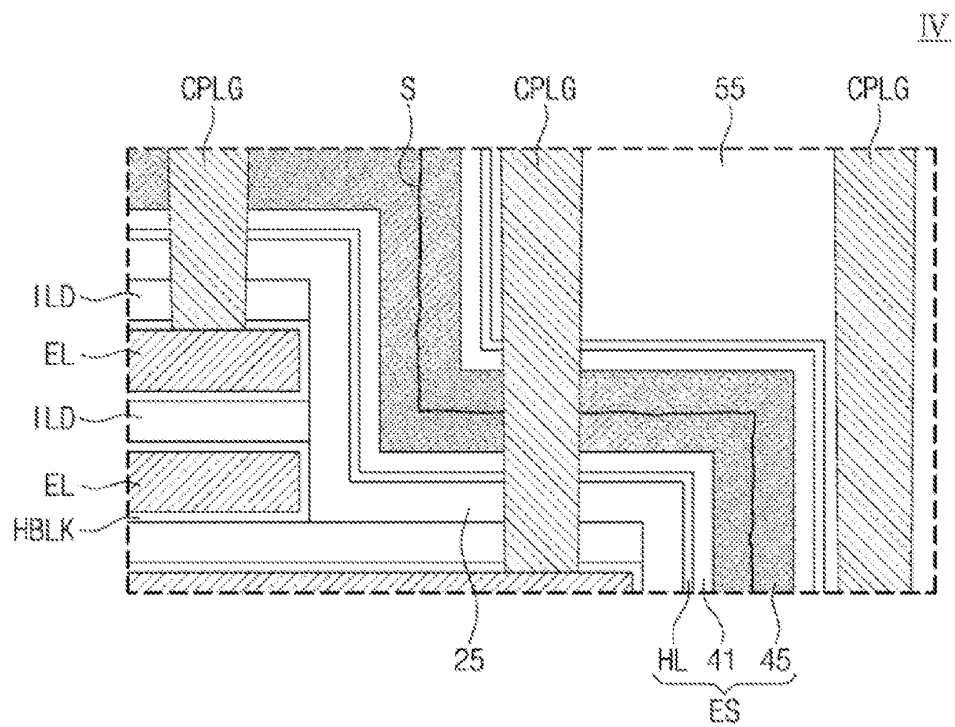


图4A

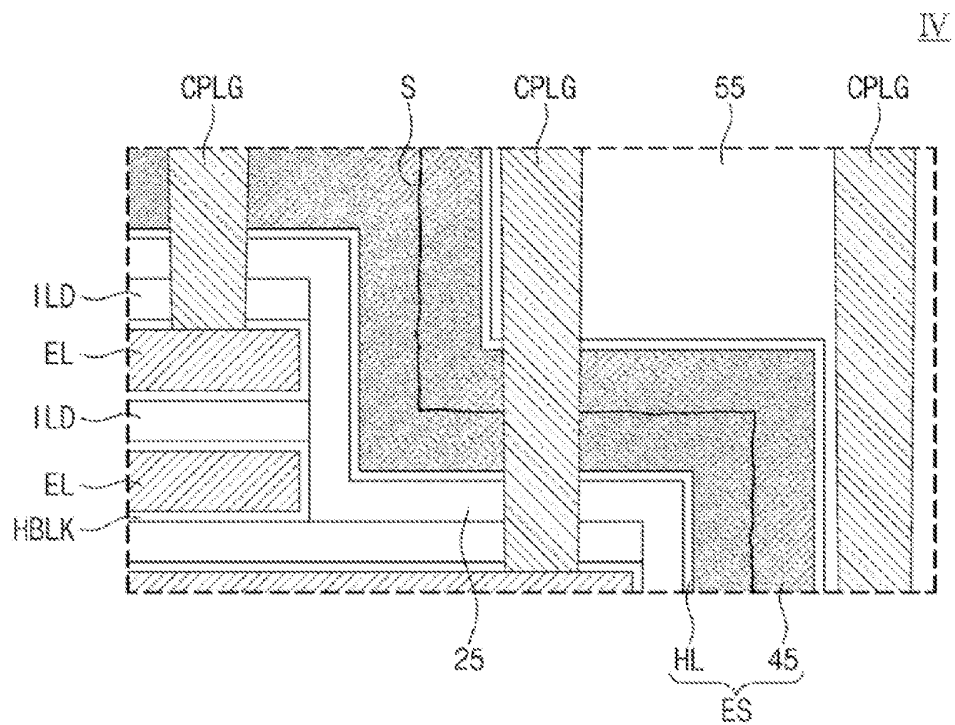


图4B

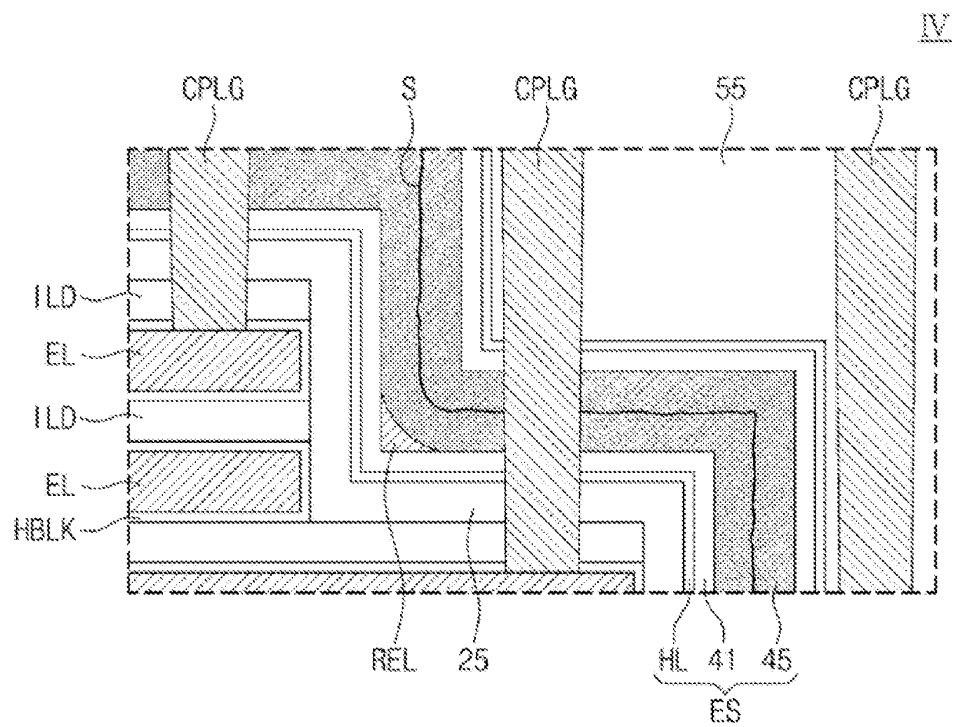


图4C

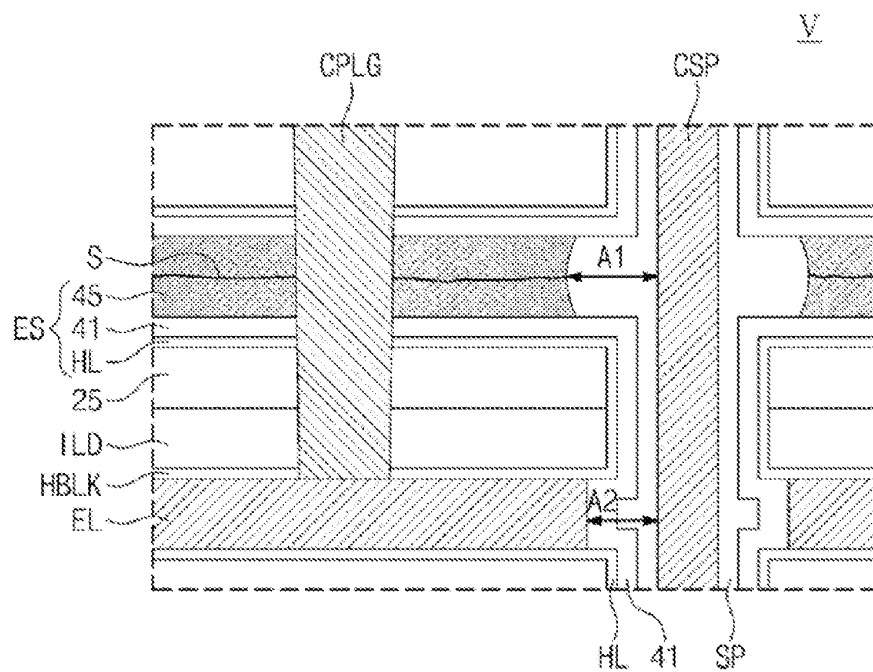


图5A

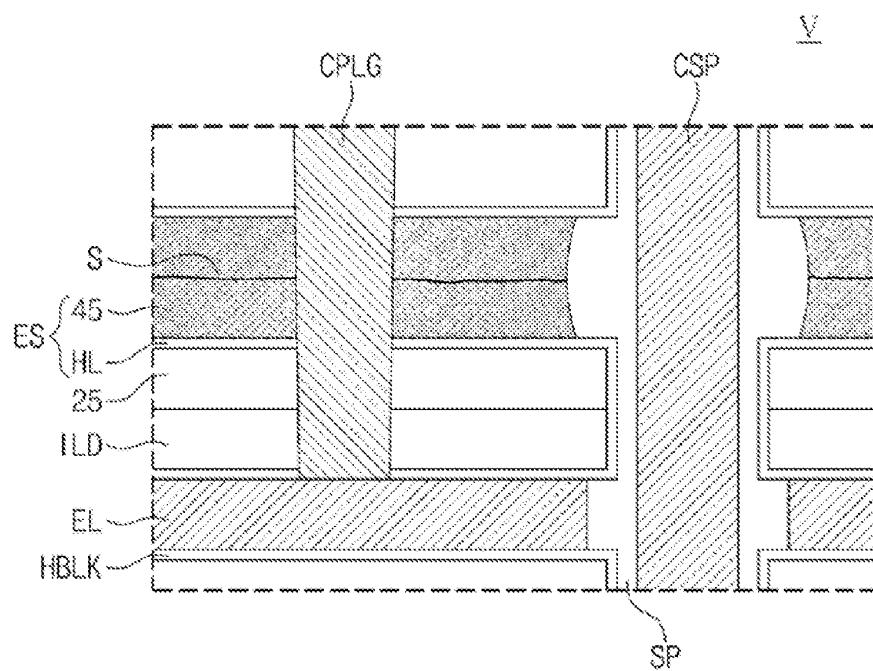


图5B

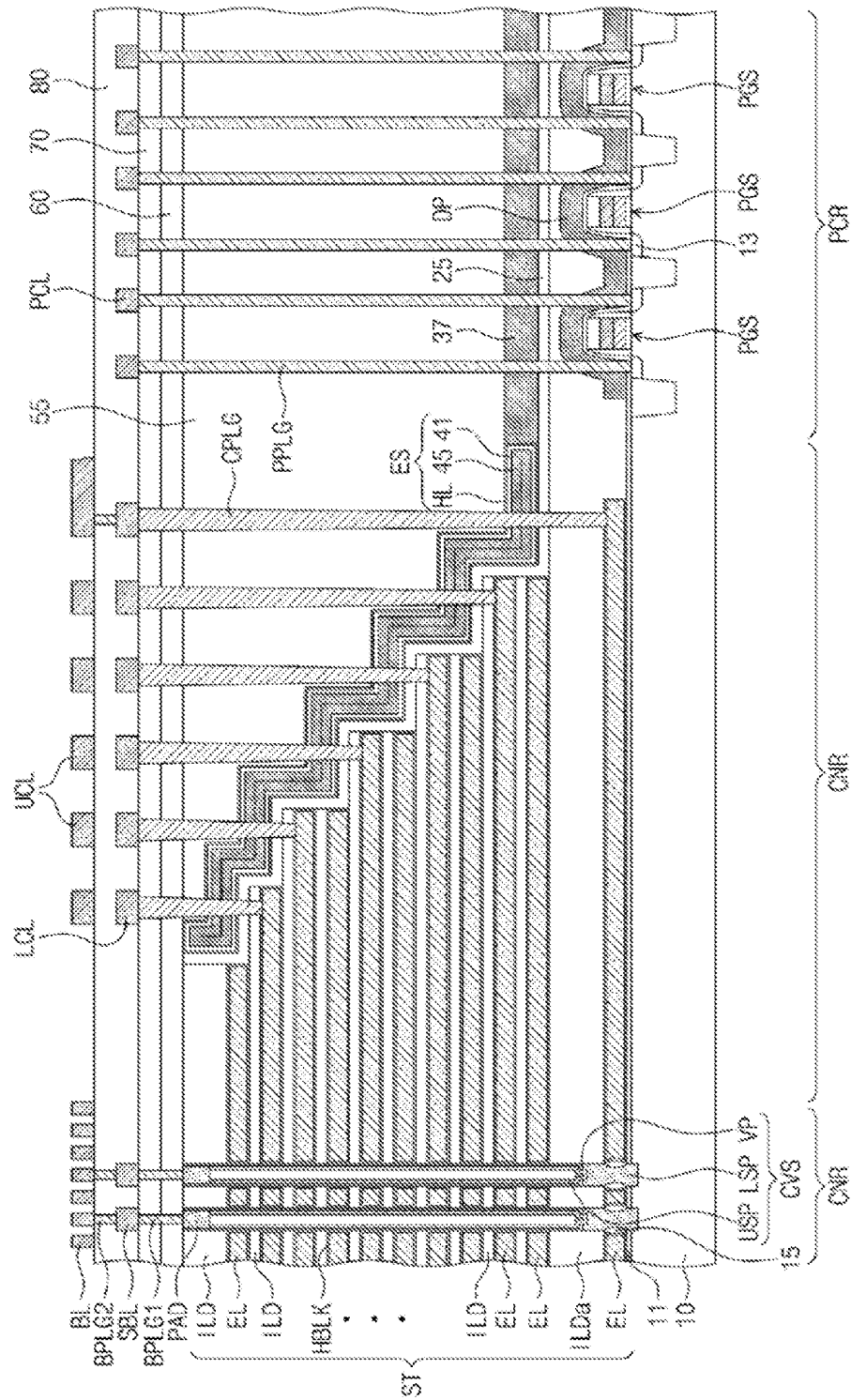


图8

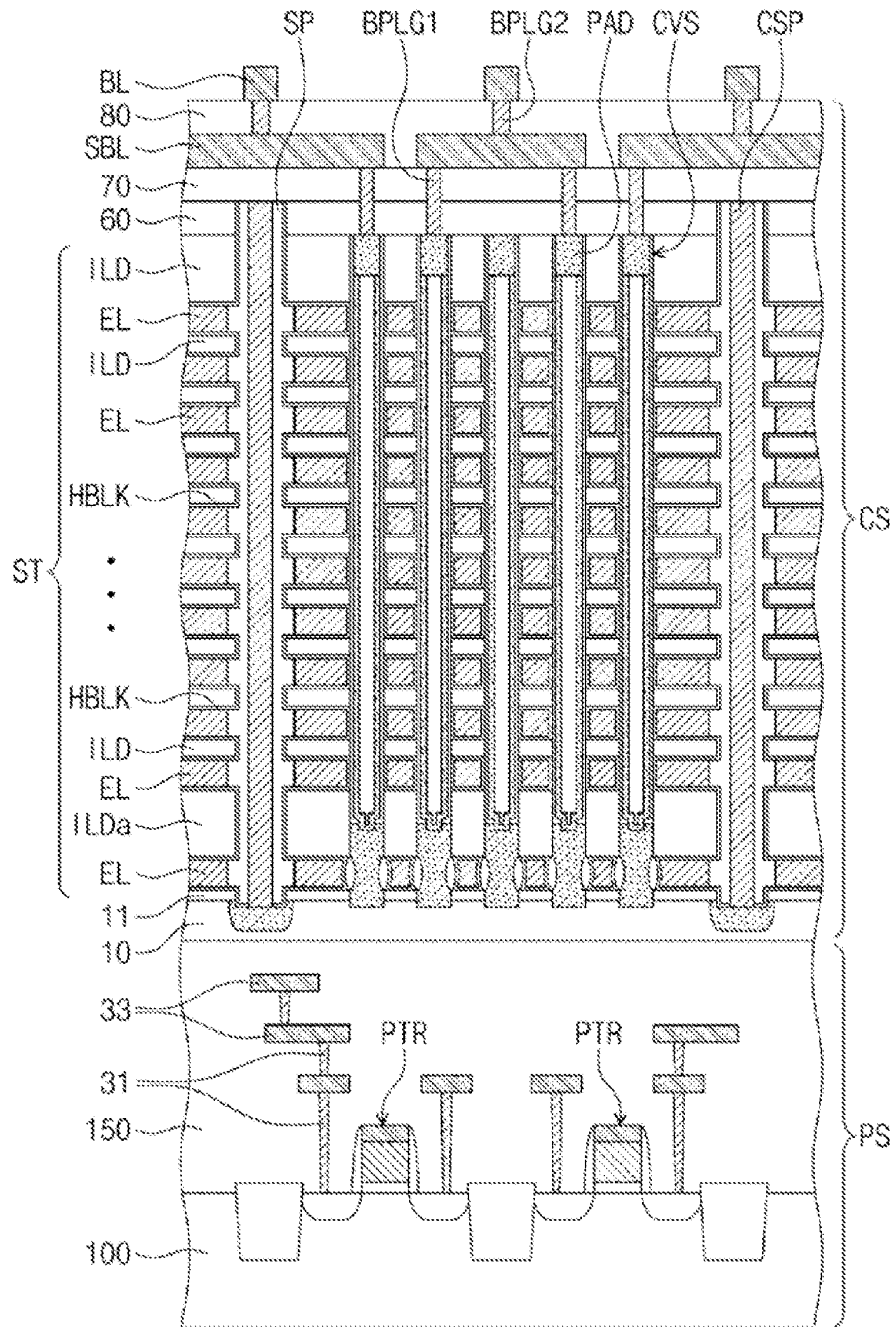


图9A

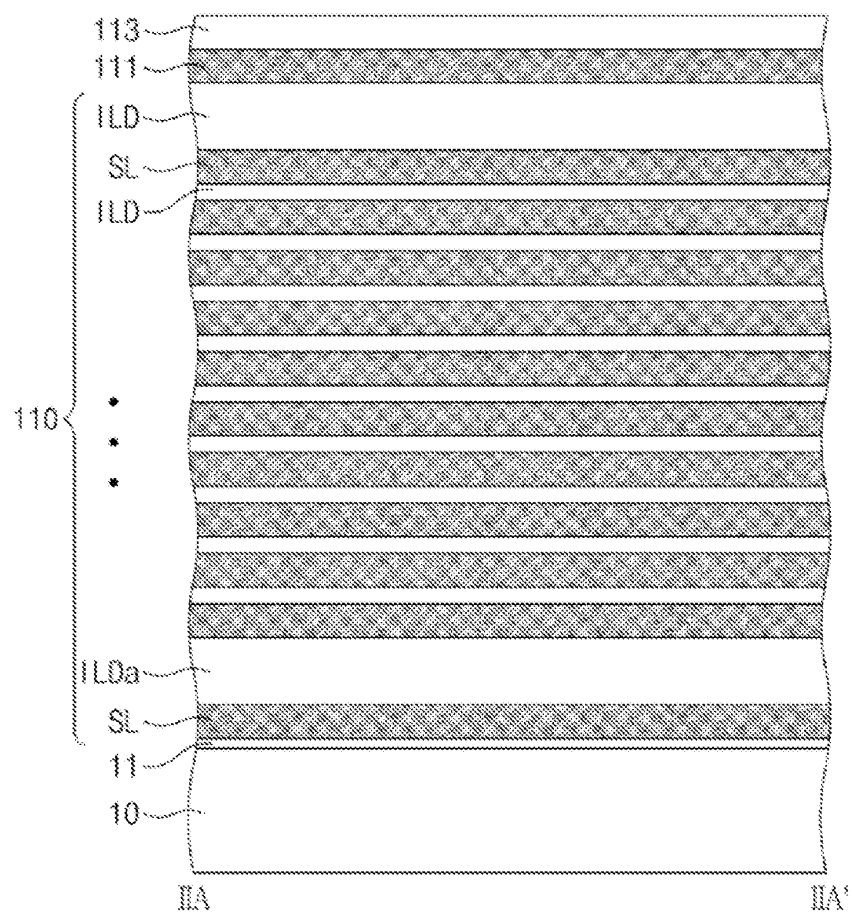


图13A

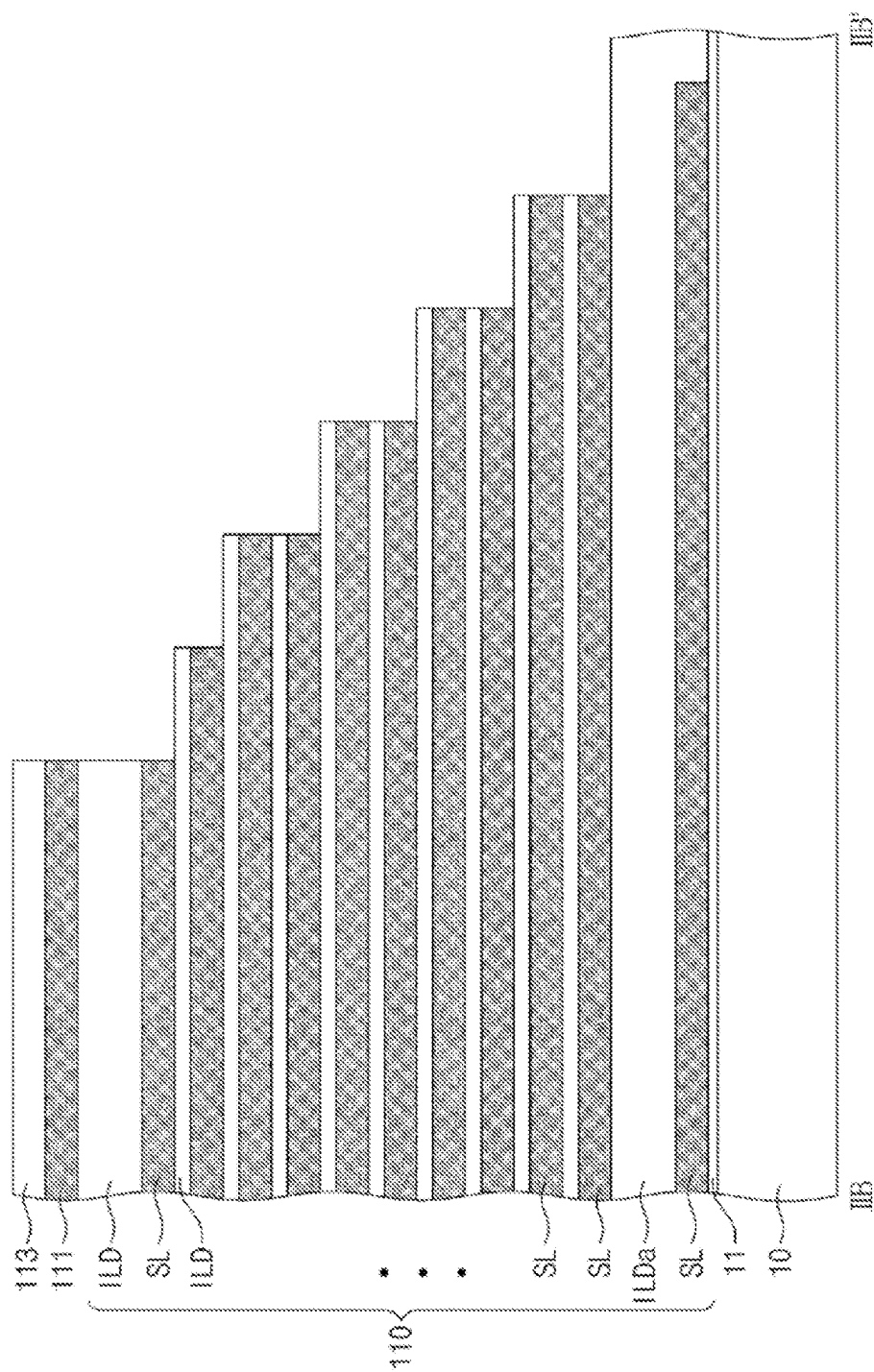


图13B

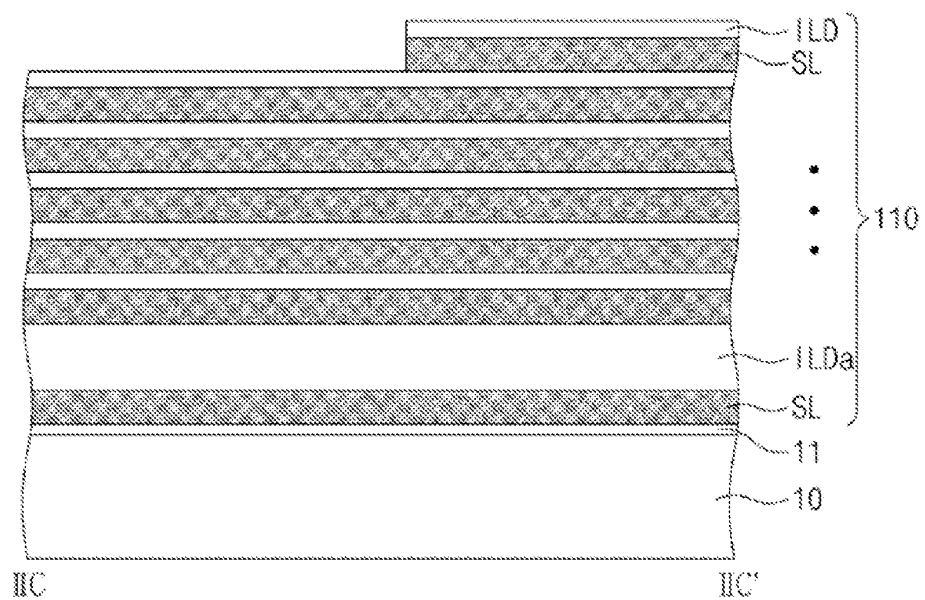


图13C

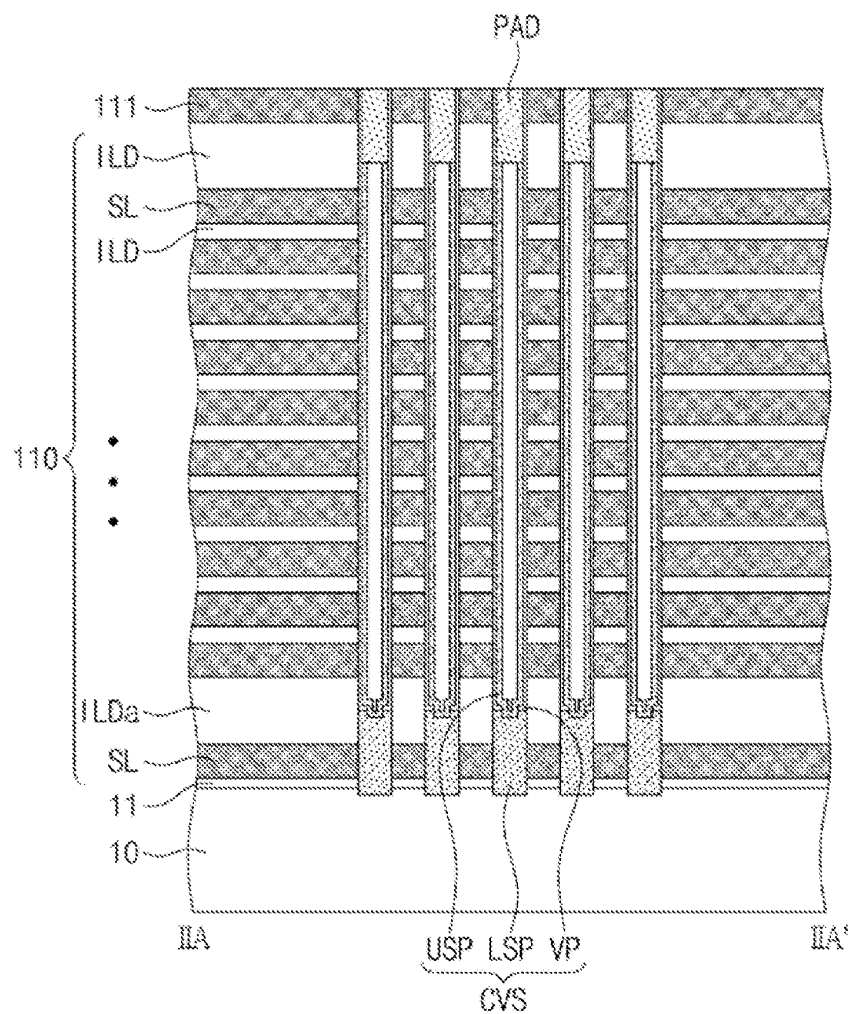


图14A

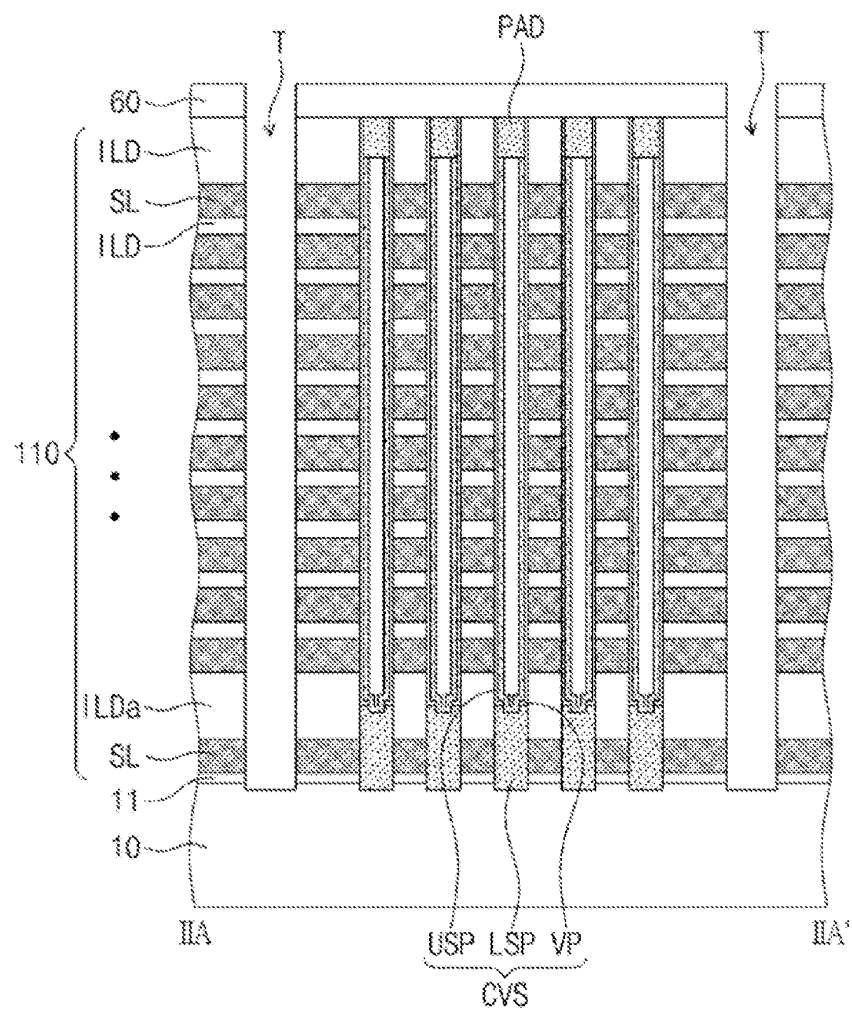


图15A

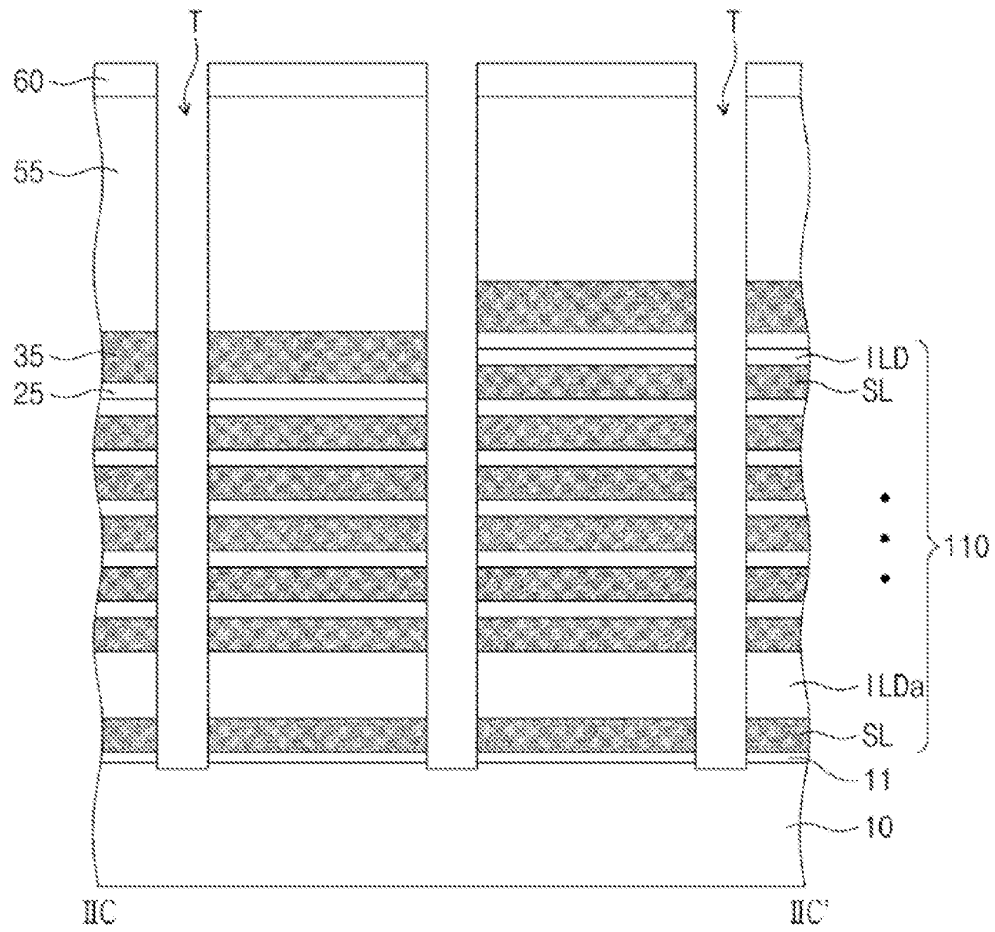


图15C

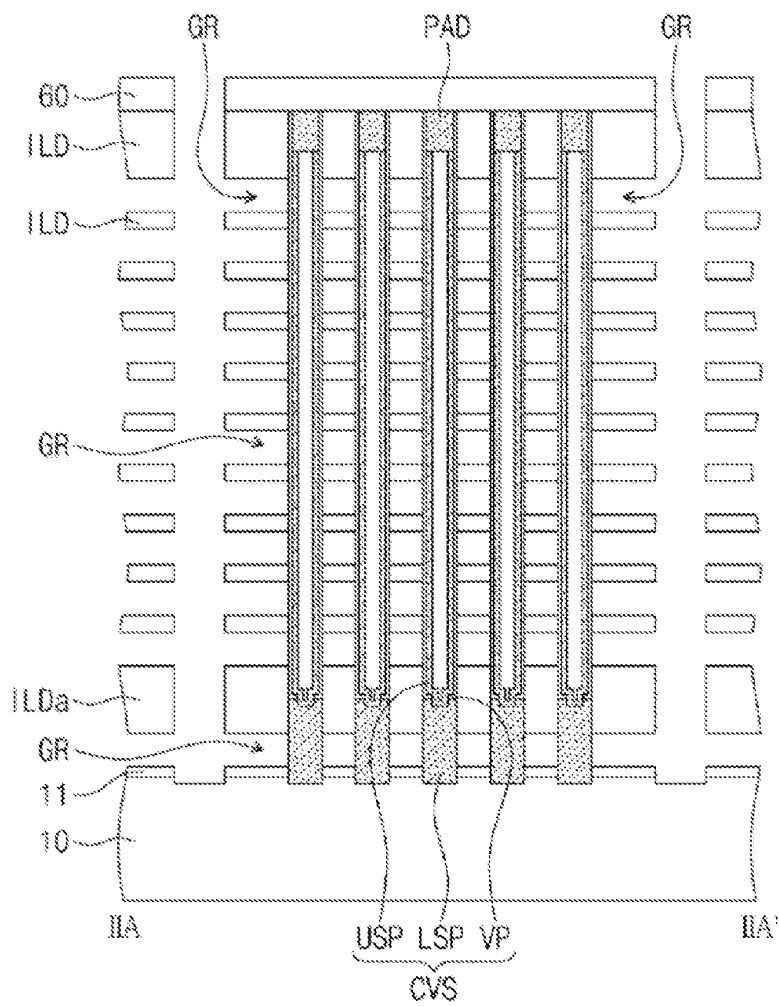


图16A

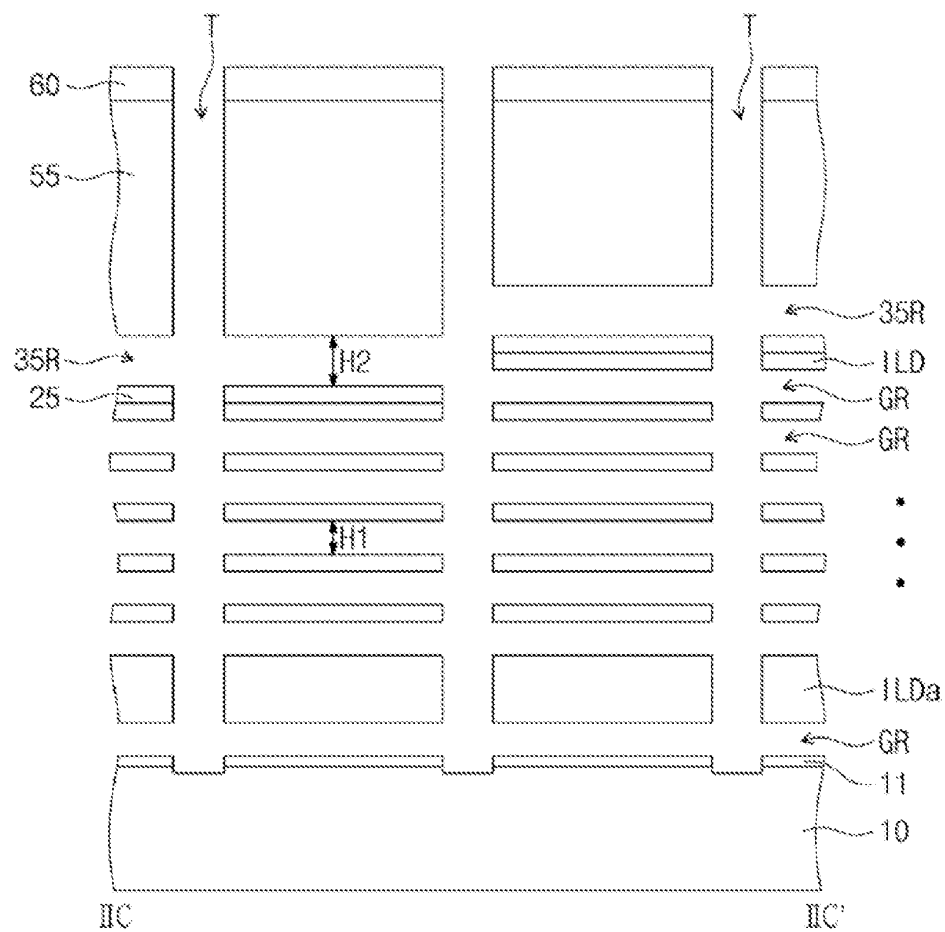


图16C

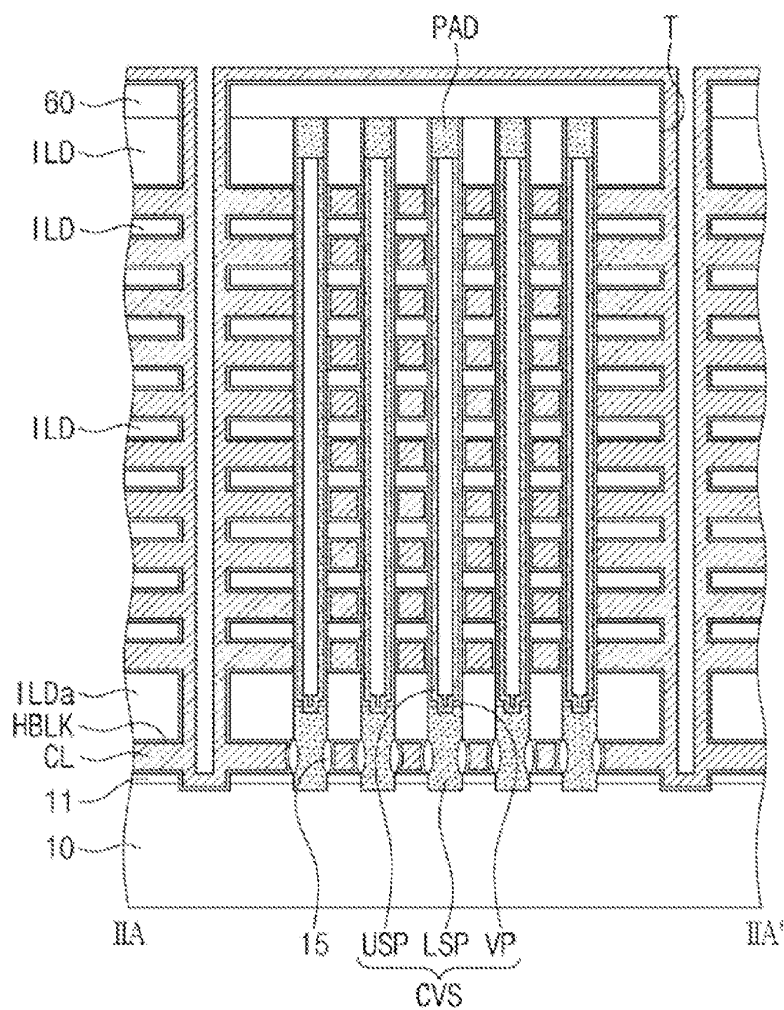


图17A

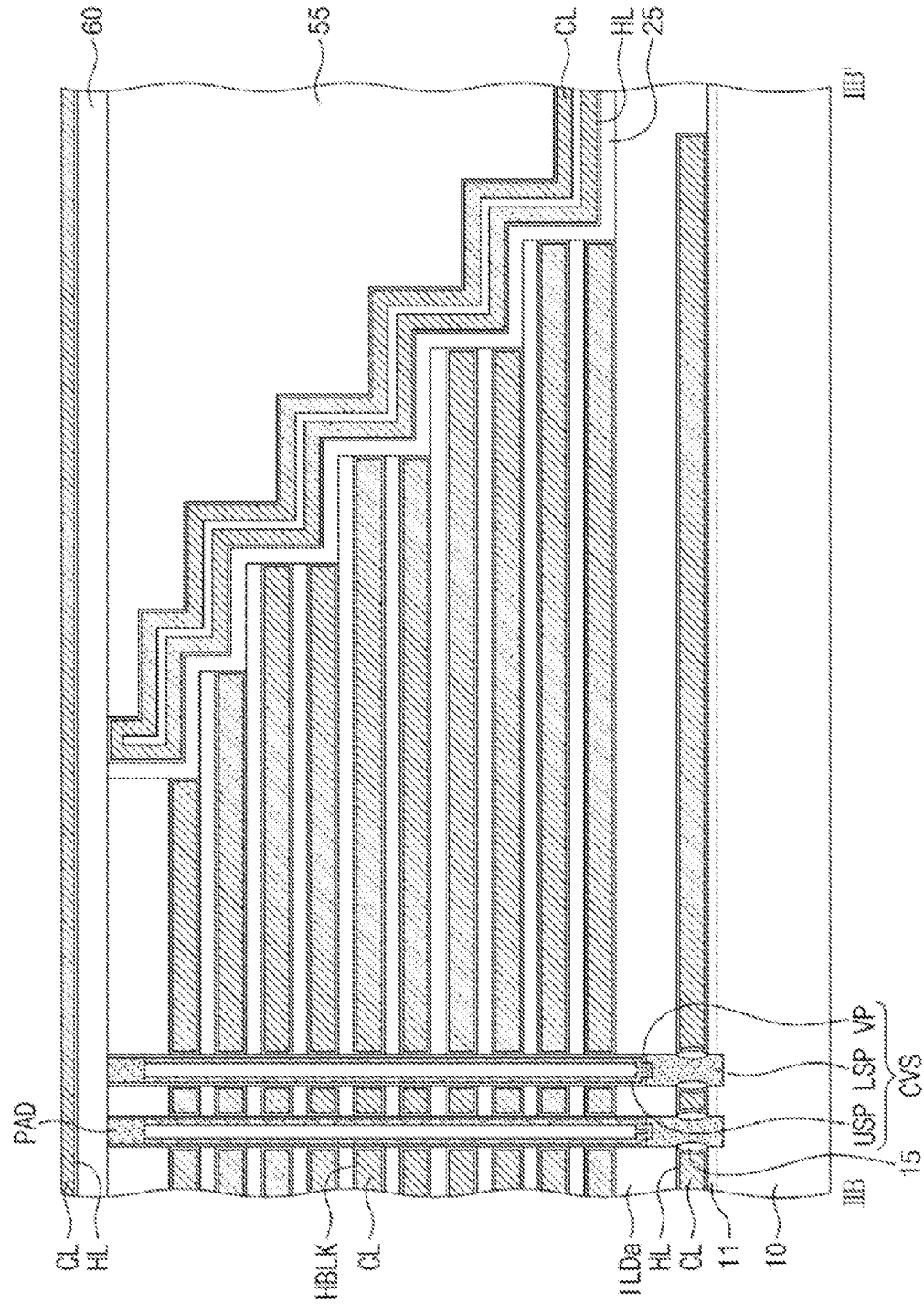


图17B

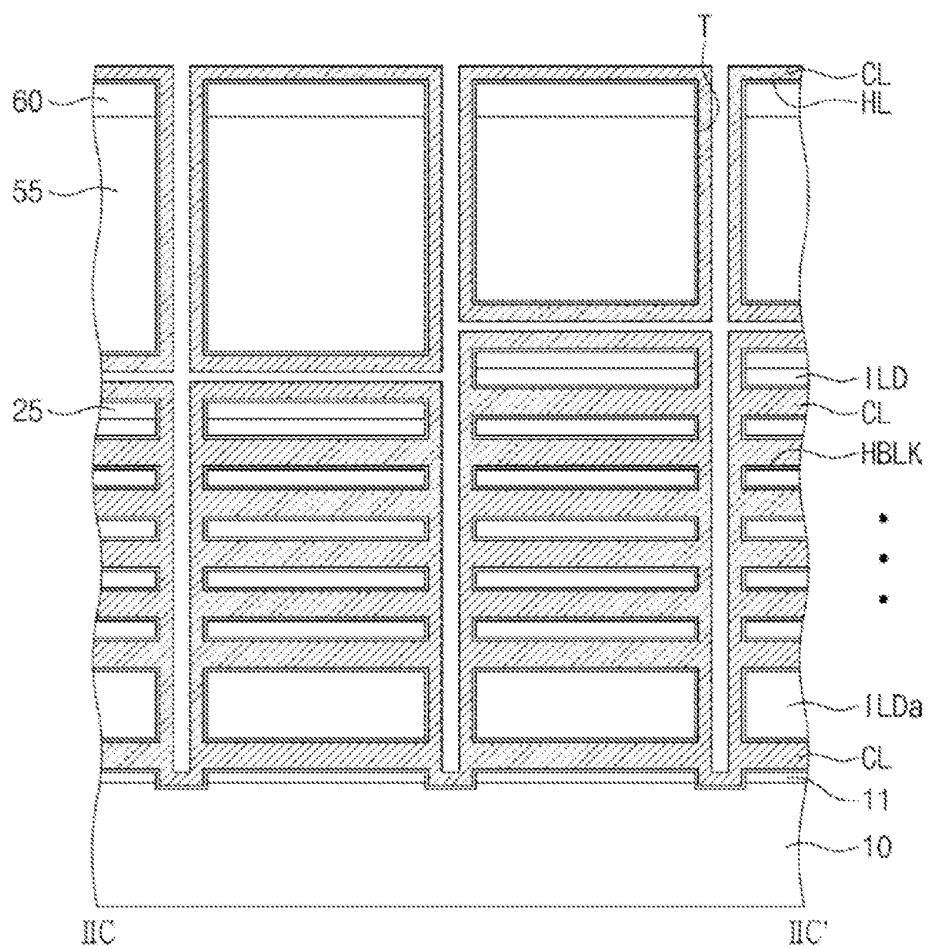


图17C

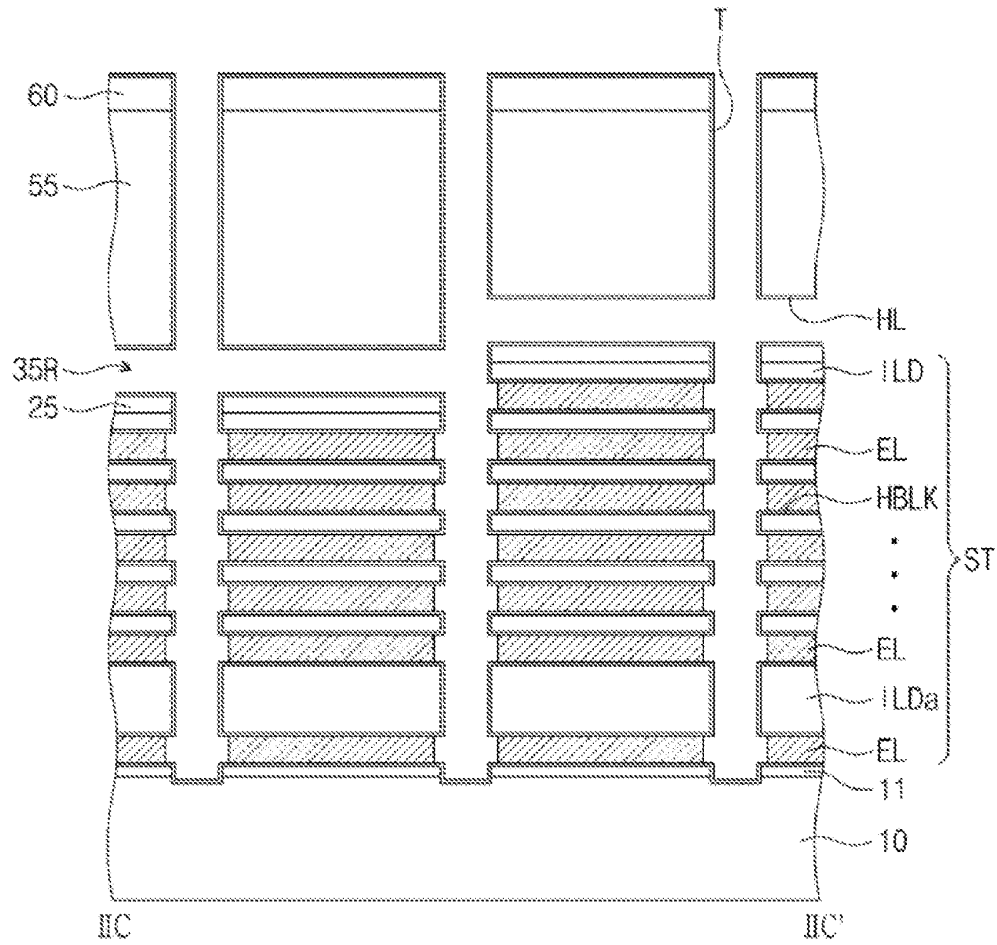


图18C

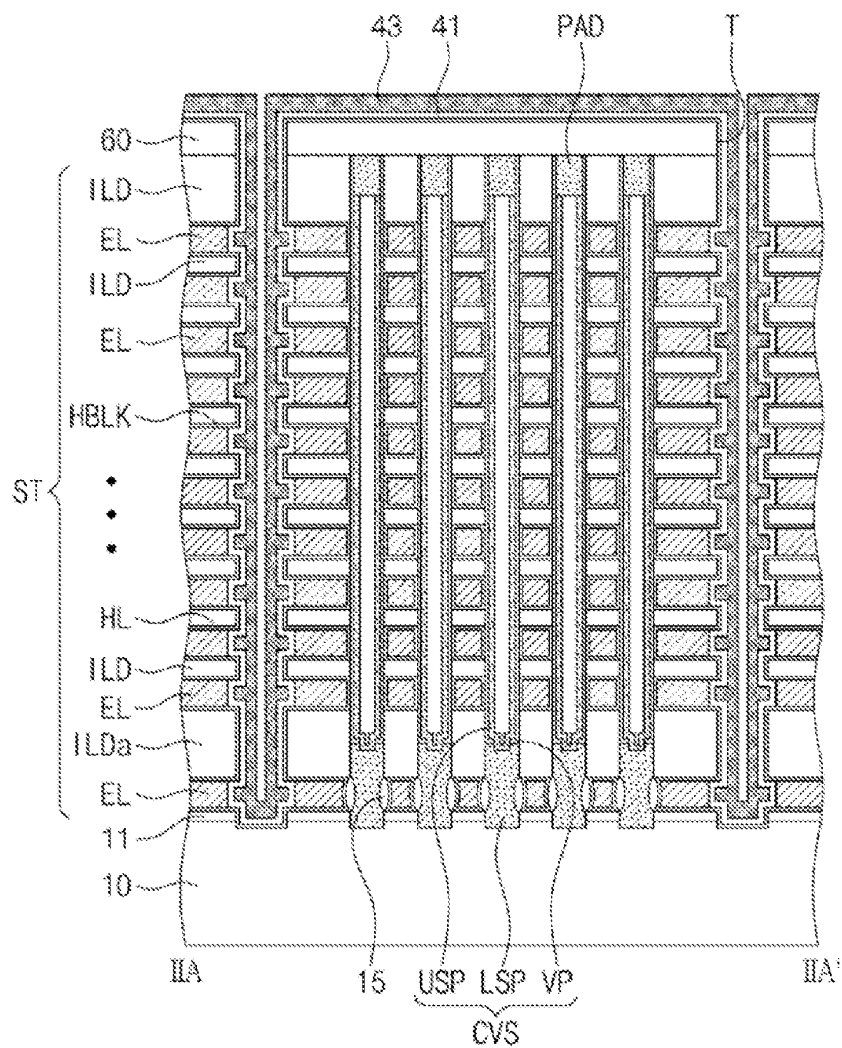


图19A

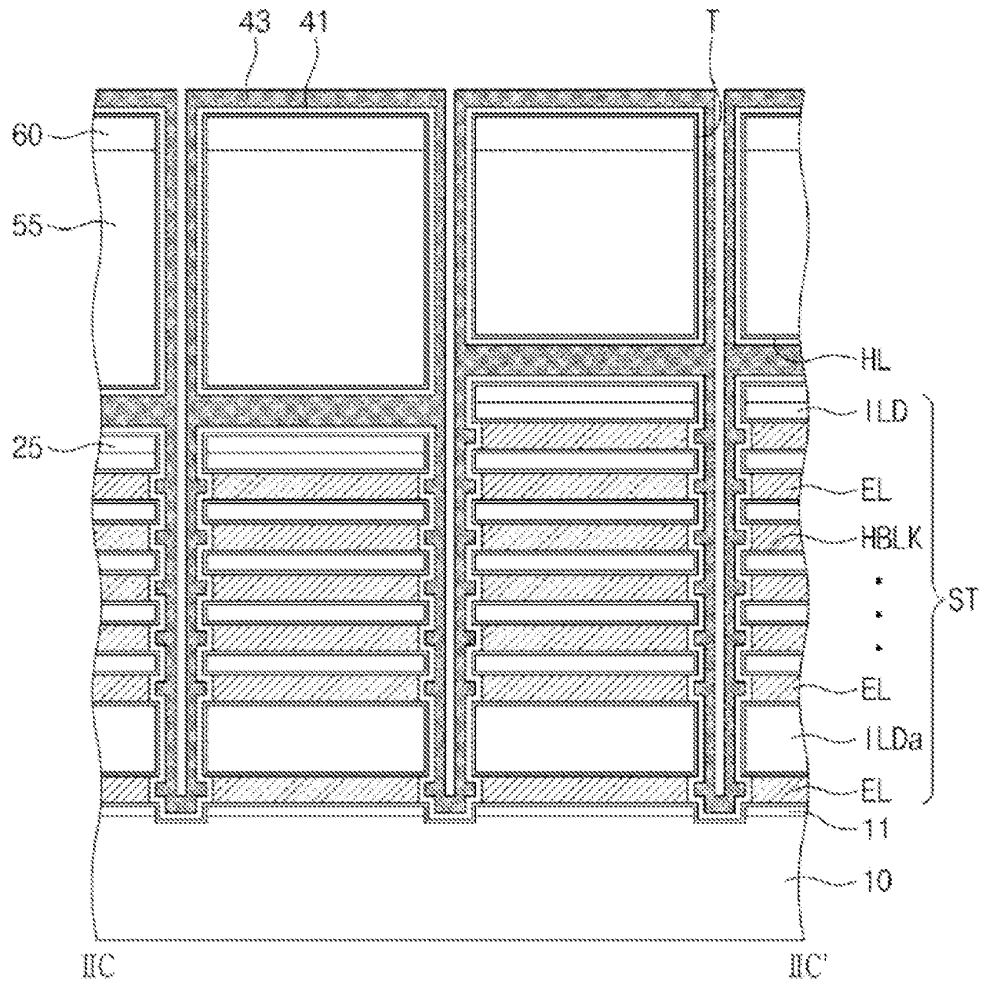


图19C

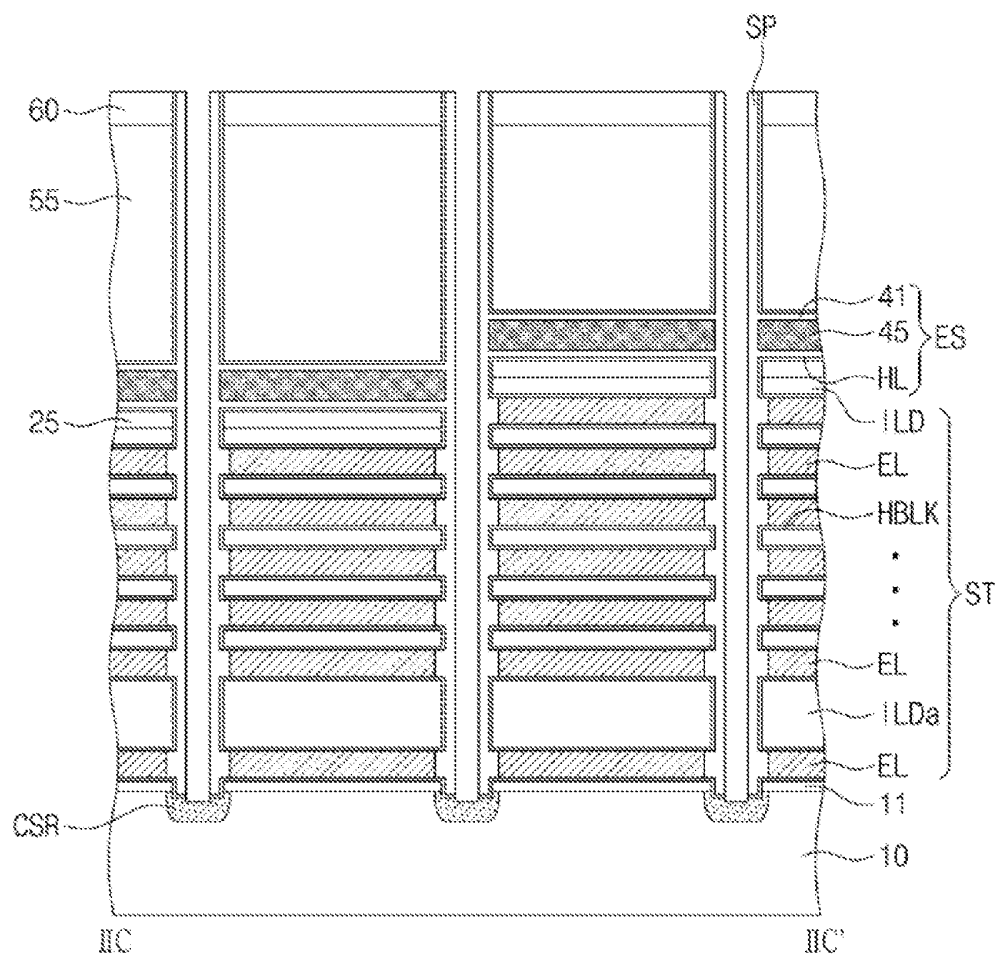


图20C

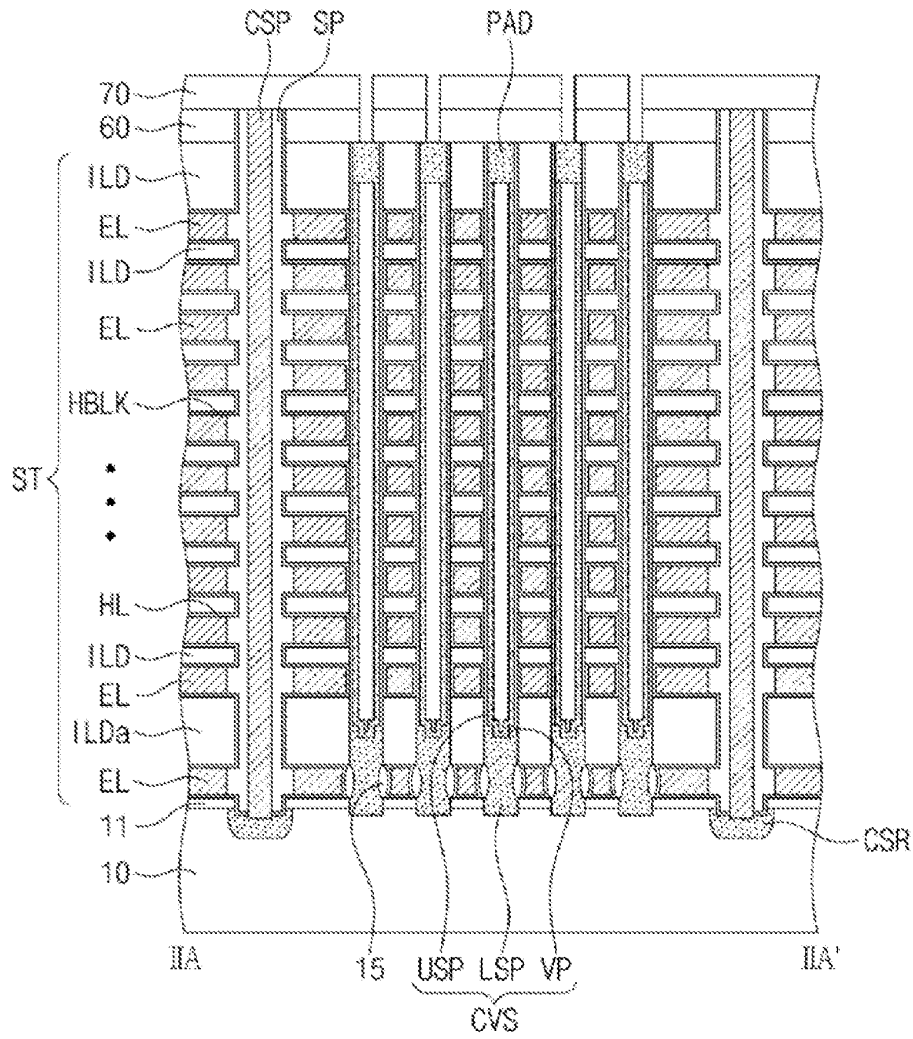


图21A

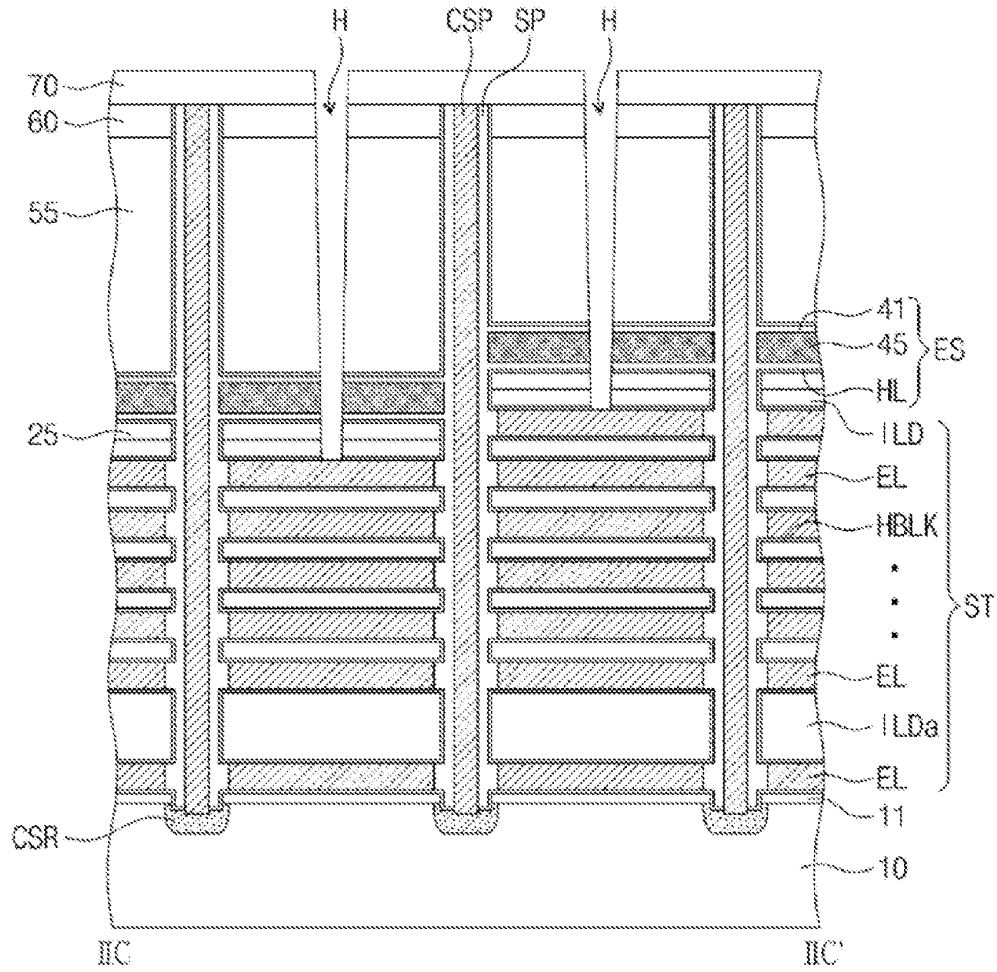


图21C

Electronic Acknowledgement Receipt	
EFS ID:	44174118
Application Number:	17191768
International Application Number:	
Confirmation Number:	5157
Title of Invention:	ARCHITECTURE AND METHOD FOR NAND MEMORY OPERATION
First Named Inventor/Applicant Name:	Changhyun LEE
Customer Number:	22850
Filer:	Philippe Jean-Claude Signore/Yolanda Myles
Filer Authorized By:	Philippe Jean-Claude Signore
Attorney Docket Number:	533055US
Receipt Date:	01-NOV-2021
Filing Date:	04-MAR-2021
Time Stamp:	16:18:40
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment		no			
File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		533055US.pdf	11108781	yes	61
			8b5014ef5d53d54ab8cbf9d64d33c85f4205e6f6		

Multipart Description/PDF files in .zip description					
Document Description			Start	End	
Transmittal Letter			1	1	
Patent Term Adjustment Stmt Under 37CFR1.704(d)			2	2	
Non Patent Literature			3	6	
Foreign Reference			7	31	
Foreign Reference			32	61	
Warnings:					
Information:					
2	Foreign Reference	533055US2.pdf	20939293	no	63
			099bb4d33789539ef197f2dbddcccd492b b149d		
Warnings:					
Information:					
Total Files Size (in bytes):			32048074		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/191,768	03/04/2021	Changhyun LEE	533055US	5157
22850	7590	03/15/2022		
OBLON, MCCLELLAND, MAIER & NEUSTADT, L.L.P. 1940 DUKE STREET ALEXANDRIA, VA 22314			EXAMINER PHAM, LY D	
			ART UNIT	PAPER NUMBER
			2827	
			NOTIFICATION DATE	DELIVERY MODE
			03/15/2022	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

OBLONPAT@OBLON.COM
iahmadi@oblon.com
patentdocket@oblon.com

DETAILED ACTION

Notice of Pre-AIA or AIA Status

1. The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

Election/Restrictions

2. Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1 – 7, drawn to a method for reading a memory device including a first memory cell string and a second memory cell string, the first memory cell string including a bottom-select-gate (BSG) transistor, memory cells, and a top-select-gate (TSG) transistor that are connected in series, the second memory cells string including a BSG transistor, memory cells, and a TSG transistor that are connected in series, the method comprising: applying, in a pre-verify stage, a first verify voltage on a gate terminal of a selected memory cell of the first memory cell string, the selected memory cell being programmed and arranged between a first adjacent memory cell and a second adjacent memory cell; applying, in the pre-verify stage, a first bias voltage on a gate terminal of at least one memory cell of the first memory cell string that is positioned between the first adjacent memory cell of the selected memory cell and the TSG transistor of the first memory cell string; applying, in a verify stage, a second verify voltage on the gate terminal of the selected memory cell of the first memory cell string; and applying, in the verify stage, a second bias voltage on the gate terminal of the at least one memory cell of the first memory cell string that is positioned between the first adjacent memory cell of the selected memory cell and the TSG transistor of the first memory cell string, wherein the second

bias voltage is smaller than the first bias voltage, as illustrated in fig. 6, and classified in G11C16/3459.

II. Claims 8 – 14, drawn to a method for reading a memory device including a first memory cell string and a second memory cell string, the first memory cell string including a bottom-select-gate (BSG) transistor, memory cells, and a top-select-gate (TSG) transistor that are connected in series, the second memory cells string including a BSG transistor, memory cells, and a TSG transistor that are connected in series, the method comprising: applying, in a pre-verify stage, a first verify voltage on a gate terminal of a selected memory cell of the first memory cell string, the selected memory cell being programmed and arranged between a first adjacent memory cell and a second adjacent memory cell; applying, in the pre-verify stage, a first bias voltage on a gate terminal of at least one memory cell of the first memory cell string that is positioned between the second adjacent memory cell of the selected memory cell and the BSG transistor of the first memory cell string; applying, in a verify stage, a second verify voltage on the gate terminal of the selected memory cell of the first memory cell string; and applying, in the verify stage, a second bias voltage on the gate terminal of the at least one memory cell of the first memory cell string that is positioned between the second adjacent memory cell of the selected memory cell and the BSG transistor of the first memory cell string, wherein the second bias voltage is smaller than the first bias voltage (illustrated in fig. 8), classified in G11C16/0433.

III. Claims 15 – 18, drawn to an apparatus for reading a memory device including a first memory cell string and a second memory cell string, the first memory cell string including a bottom- select-gate (BSG) transistor, memory cells, and a top-select-gate (TSG) transistor that are connected in series, the second memory cells string including a BSG transistor, memory cells, and a TSG transistor that are connected in series, the apparatus comprising: processing circuitry configured to: apply, in a pre-verify stage, a first verify voltage on a gate terminal of a selected memory cell of the first memory cell string, the selected memory cell being programmed and arranged between a first adjacent memory cell and a second adjacent memory cell; apply, in the pre-verify stage, a first bias voltage on a gate terminal of at least one memory cell of the first memory cell string that is not programmed; apply, in a verify stage, a second verify voltage on the gate terminal of the selected memory cell of the first memory cell string; and apply, in the verify stage, a second bias voltage on the gate terminal of the at least one memory cell of the first memory cell string that is not programmed, wherein the second bias voltage is smaller than the first bias voltage (illustrated in fig. 9), classified in G11C16/10.

3. The inventions are independent or distinct, each from the other because:

Inventions I, II and III are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct if they do not overlap in scope and are not obvious variants, and if it is shown that at least one subcombination is separately usable. In the instant case, subcombinations I – III each has separate utility such as those underlined above. See MPEP § 806.05(d).

The examiner has required restriction between subcombinations usable together.

Where applicant elects a subcombination and claims thereto are subsequently found allowable, any claim(s) depending from or otherwise requiring all the limitations of the allowable subcombination will be examined for patentability in accordance with 37 CFR 1.104. See MPEP § 821.04(a). Applicant is advised that if any claim presented in a continuation or divisional application is anticipated by, or includes all the limitations of, a claim that is allowable in the present application, such claim may be subject to provisional statutory and/or nonstatutory double patenting rejections over the claims of the instant application.

4. Restriction for examination purposes as indicated is proper because all the inventions listed in this action are independent or distinct for the reasons given above and there would be a serious search and/or examination burden if restriction were not required because one or more of the following reasons apply:

- the inventions have acquired a separate status in the art in view of their different classification
- the inventions have acquired a separate status in the art due to their recognized divergent subject matter
- the inventions require a different field of search (e.g., searching different classes/subclasses or electronic resources, or employing different search strategies or search queries).

Applicant is advised that the reply to this requirement to be complete must include (i) an election of an invention to be examined even though the requirement may be traversed (37 CFR 1.143) and (ii) identification of the claims encompassing the elected invention.

The election of an invention may be made with or without traverse. To reserve a right to petition, the election must be made with traverse. If the reply does not distinctly and

specifically point out supposed errors in the restriction requirement, the election shall be treated as an election without traverse. Traversal must be presented at the time of election in order to be considered timely. Failure to timely traverse the requirement will result in the loss of right to petition under 37 CFR 1.144. If claims are added after the election, applicant must indicate which of these claims are readable upon the elected invention.

Should applicant traverse on the ground that the inventions are not patentably distinct, applicant should submit evidence or identify such evidence now of record showing the inventions to be obvious variants or clearly admit on the record that this is the case. In either instance, if the examiner finds one of the inventions unpatentable over the prior art, the evidence or admission may be used in a rejection under 35 U.S.C. 103 or pre-AIA 35 U.S.C. 103(a) of the other invention.

5. A telephone call was made to Dr. Leonidas Boutsikaris (Reg. no. 61,377) on March 10, 2022 to request an oral election to the above restriction requirement, but did not result in an election being made. The applicant requests a written requirement.

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to LY D PHAM whose telephone number is (571)272-1793. The examiner can normally be reached M-F: 8am-5pm.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is

encouraged to use the USPTO Automated Interview Request (AIR) at
<http://www.uspto.gov/interviewpractice>.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of published or unpublished applications may be obtained from Patent Center. Unpublished application information in Patent Center is available to registered users. To file and manage patent submissions in Patent Center, visit: <https://patentcenter.uspto.gov>. Visit <https://www.uspto.gov/patents/apply/patent-center> for more information about Patent Center and <https://www.uspto.gov/patents/docx> for information about filing in DOCX format. For additional questions, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

LY D. PHAM
Examiner
Art Unit 2827

/LY D PHAM/
Primary Examiner, Art Unit 2827
March 10, 2022

UNITED STATES PATENT AND TRADEMARK OFFICE
COMMISSIONER FOR PATENTS
P.O.BOX 1450
ALEXANDRIA VA 22313-1451

PRESORTED
FIRST-CLASS MAIL
U.S. POSTAGE PAID
POSTEDIGITAL
NNNNN

OBLON, MCCLELLAND, MAIER &
NEUSTADT, L.L.P.
1940 DUKE STREET
ALEXANDRIA, VA 22314



**Courtesy Reminder for
Application Serial No: 17/191,768**

Attorney Docket No: 533055US

Customer Number: 22850

Date of Electronic Notification: 03/15/2022

This is a courtesy reminder that new correspondence is available for this application. If you have not done so already, please review the correspondence. The official date of notification of the outgoing correspondence will be indicated on the form PTOL-90 accompanying the correspondence.

An email notification regarding the correspondence was sent to the following email address(es) associated with your customer number:

patentdocket@oblon.com
OBLONPAT@OBLON.COM
iahmadi@oblon.com

To view your correspondence online or update your email addresses, please visit us anytime at <https://ppair-my.uspto.gov/pair/PrivatePair>. If you have any questions, please email the Electronic Business Center (EBC) at EBC@uspto.gov or call 1-866-217-9197.

DOCKET NO: 533055US

IN THE UNITED STATES PATENT & TRADEMARK OFFICE

IN RE APPLICATION OF :
CHANGHYUN LEE, ET AL. : EXAMINER: PHAM, LY D.
SERIAL NO: 17/191,768 :
FILED: MARCH 4, 2021 : GROUP ART UNIT: 2827
FOR: ARCHITECTURE AND :
METHOD FOR NAND MEMORY
OPERATION

ELECTION-RESTRICTION RESPONSE

COMMISSIONER FOR PATENTS
ALEXANDRIA, VIRGINIA 22313

Commissioner:

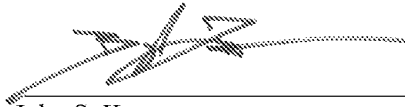
In response to the Restriction-Election Requirement dated March 15, 2022, Applicant elects, without traverse, Invention III, Claims 15-20, drawn to an apparatus for reading a memory device, for examination on the merits. Applicant reserves the right to file one or more divisional applications directed to the nonelected claims.

Applicant respectfully submits that, on page 4 of the Office Action, Invention III is described to correspond to Claims 15-18, which seems to be a typo. Applicant accordingly interprets that the Office Action intends to group Claims 16-20 as Invention III.

Accordingly, examination on the merits of Claims 15-20 is believed to be in order and
an early and favorable action is respectfully requested.

Respectfully Submitted,

OBLON, McCLELLAND,
MAIER & NEUSTADT, L.L.P.



John S. Kern
Attorney of Record
Registration No. 42,719

Customer Number

22850

Tel. (703) 413-3000
Fax. (703) 413-2220
(OMMN 07/09)

Jianping Wu
Registration No. 79,782

Bogdan A. Zinchenko
Registration No.: 57,473

Electronic Acknowledgement Receipt	
EFS ID:	45651711
Application Number:	17191768
International Application Number:	
Confirmation Number:	5157
Title of Invention:	ARCHITECTURE AND METHOD FOR NAND MEMORY OPERATION
First Named Inventor/Applicant Name:	Changhyun LEE
Customer Number:	22850
Filer:	Philippe Jean-Claude Signore/Susie Hockaday
Filer Authorized By:	Philippe Jean-Claude Signore
Attorney Docket Number:	533055US
Receipt Date:	06-MAY-2022
Filing Date:	04-MAR-2021
Time Stamp:	13:15:37
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment		no			
File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		533055US_ELECT_RESTR_RESP ONSE.pdf	1086640 7032c0f26133b27037614efef5cc38c532be a1e5	yes	3

	Multipart Description/PDF files in .zip description		
	Document Description	Start	End
	Miscellaneous Incoming Letter	1	1
	Response to Election / Restriction Filed	2	3
Warnings:			
Information:			
Total Files Size (in bytes):		1086640	
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.			

COMMISSIONER FOR PATENTS
ALEXANDRIA, VIRGINIA 22313

RE: Application Serial No.: 17/191,768
Applicants: Changhyun LEE, et al.
Filing Date: March 4, 2021
For: ARCHITECTURE AND METHOD FOR NAND MEMORY
OPERATION
Group Art Unit: 2827
Examiner: PHAM, LY D.

Commissioner:

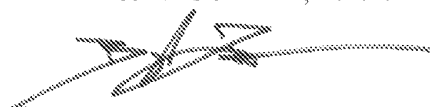
Attached hereto for filing are the following papers:

Election-Restriction Response

Credit card payment is being made online (if electronically filed), or is attached hereto (if paper filed), in the amount of **\$0.00** to cover any required fees. In the event any variance exists between the submitted amount and the U.S. Patent and Trademark Office fees for filing the above-noted documents, including any fees required under 37 C.F.R. 1.136 for any necessary Extension of Time to make the filing of the attached documents timely, please charge or credit the difference to our Deposit Account No. **15-0030**. Further, if these papers are not considered timely filed, then a petition is hereby made under 37 C.F.R. 1.136 for the necessary extension of time.

Respectfully submitted,

OBLON, McCLELLAND,
MAIER & NEUSTADT, L.L.P.



John S. Kern

Registration No. 42,719

Customer Number

22850

(703) 413-3000 (phone)
(703) 413-2220 (fax)
(OMMN 02/12)

Jianping Wu
Registration No. 79,782

Bogdan A. Zinchenko
Registration No.: 57,473

OBLON, McCLELLAND, MAIER & NEUSTADT, L.L.P.
1940 DUKE STREET ■ ALEXANDRIA, VIRGINIA 22314 ■ U.S.A.
TELEPHONE: 703-413-3000 ■ FACSIMILE: 703-413-2220 ■ WWW.OBLON.COM



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

22850 7590 06/08/2022
OBLON, MCCLELLAND, MAIER & NEUSTADT, L.L.P.
1940 DUKE STREET
ALEXANDRIA, VA 22314

EXAMINER	
PHAM, LY D	
ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 06/08/2022

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/191,768	03/04/2021	Changhyun LEE	533055US	5157

TITLE OF INVENTION: ARCHITECTURE AND METHOD FOR NAND MEMORY OPERATION

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$1200	\$0.00	\$0.00	\$1200	09/08/2022

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Maintenance fees are due in utility patents issuing on applications filed on or after Dec. 12, 1980. It is patentee's responsibility to ensure timely payment of maintenance fees when due. More information is available at www.uspto.gov/PatentMaintenanceFees.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), by mail or fax, or via EFS-Web.

By mail, send to: Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

By fax, send to: (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

22850 7590 06/08/2022
OBLON, MCCLELLAND, MAIER & NEUSTADT, L.L.P.
1940 DUKE STREET
ALEXANDRIA, VA 22314

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being transmitted to the USPTO via EFS-Web or by facsimile to (571) 273-2885, on the date below.

(Typed or printed name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/191,768	03/04/2021	Changhyun LEE	533055US	5157

TITLE OF INVENTION: ARCHITECTURE AND METHOD FOR NAND MEMORY OPERATION

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$1200	\$0.00	\$0.00	\$1200	09/08/2022

EXAMINER	ART UNIT	CLASS-SUBCLASS
PHAM, LY D	2827	365-185220

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

☐ Change of correspondence address (or Change of Correspondence Address form PTO/AIA/122 or PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/AIA/47 or PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

- (1) The names of up to 3 registered patent attorneys or agents OR, alternatively, 1 _____
- (2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 2 _____
- 3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. Fees submitted: ☐ Issue Fee ☐ Publication Fee (if required) ☐ Advance Order - # of Copies _____

4b. Method of Payment: (Please first reapply any previously paid fee shown above)

☐ Electronic Payment via EFS-Web ☐ Enclosed check ☐ Non-electronic payment by credit card (Attach form PTO-2038)

☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. _____

5. Change in Entity Status (from status indicated above)

☐ Applicant certifying micro entity status. See 37 CFR 1.29

☐ Applicant asserting small entity status. See 37 CFR 1.27

☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment. **NOTE:** If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/191,768	03/04/2021	Changhyun LEE	533055US	5157
22850	7590	06/08/2022	EXAMINER	
OBLON, MCCLELLAND, MAIER & NEUSTADT, L.L.P.			PHAM, LY D	
1940 DUKE STREET			ART UNIT	PAPER NUMBER
ALEXANDRIA, VA 22314			2827	

DATE MAILED: 06/08/2022

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. **DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.** Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b) (2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 17/191,768	Applicant(s) LEE et al.	
	Examiner LY D PHAM	Art Unit 2827	AIA (FITF) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to Response filed 05 May 2022.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on ____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on ____; the restriction requirement and election have been incorporated into this action.

3. ☒ The allowed claim(s) is/are 15-20. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:
a) ☐ All b) ☐ Some* c) ☐ None of the:

1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892) 2. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 11/01/2021. 3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material _____. 4. ☐ Interview Summary (PTO-413), Paper No./Mail Date. _____.	5. ☒ Examiner's Amendment/Comment 6. ☒ Examiner's Statement of Reasons for Allowance 7. ☐ Other _____.
---	---

DETAILED ACTION

Notice of Pre-AIA or AIA Status

1. The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

EXAMINER'S AMENDMENT

2. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it **MUST** be submitted no later than the payment of the issue fee.

The application has been amended as follows:

Claims 1 – 14 are canceled for being drawn to non-elected invention. Election was made without traverse in the response filed 06 May 2022.

Allowable Subject Matter

3. Claims 15 – 20 are allowed.
4. The following is an examiner's statement of reasons for allowance:

The prior arts of record fail to teach or reasonably suggest, in combination, an apparatus for reading a memory device including a first memory cell string and a second memory cell string, the first memory cell string including a bottom- select-gate (BSG) transistor, memory cells, and a top-select-gate (TSG) transistor that are connected in series, the second memory

cells string including a BSG transistor, memory cells, and a TSG transistor that are connected in series, the apparatus comprising:

processing circuitry configured to:

apply, in a pre-verify stage, a first verify voltage on a gate terminal of a selected memory cell of the first memory cell string, the selected memory cell being programmed and arranged between a first adjacent memory cell and a second adjacent memory cell;

apply, in the pre-verify stage, a first bias voltage on a gate terminal of at least one memory cell of the first memory cell string that is not programmed;

apply, in a verify stage, a second verify voltage on the gate terminal of the selected memory cell of the first memory cell string; and

apply, in the verify stage, a second bias voltage on the gate terminal of the at least one memory cell of the first memory cell string that is not programmed, wherein the second bias voltage is smaller than the first bias voltage.

5. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See additional cited references for related disclosures to the claimed invention.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to LY D PHAM whose telephone number is (571)272-1793. The examiner can normally be reached M-F: 8am-5pm.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at <http://www.uspto.gov/interviewpractice>.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of published or unpublished applications may be obtained from Patent Center. Unpublished application information in Patent Center is available to registered users. To file and manage patent submissions in Patent Center, visit: <https://patentcenter.uspto.gov>. Visit <https://www.uspto.gov/patents/apply/patent-center> for more information about Patent Center and <https://www.uspto.gov/patents/docx> for information about filing in DOCX format. For additional questions, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/LY D PHAM/
Primary Examiner, Art Unit 2827
June 4, 2022

Notice of References Cited	Application/Control No. 17/191,768		Applicant(s)/Patent Under Reexamination LEE et al.	
	Examiner LY D PHAM		Art Unit 2827	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-10861537-B1	12-2020	Lien; Yu-Chung	G11C16/32	1/1
*	B	US-10665299-B1	05-2020	Lu; Ching-Huang	G11C16/0483	1/1
*	C	US-20110134702-A1	06-2011	Imondi; Giuliano G.	G11C11/5628	365/185.19
*	D	US-20220084597-A1	03-2022	MUN; Yeong Jo	G11C16/3418	1/1
*	E	US-20210391026-A1	12-2021	CHOI; Hyung Jin	G11C16/10	1/1
*	F	US-20200258585-A1	08-2020	LEE; Hee Youl	G11C16/16	1/1
*	G	US-20200168279-A1	05-2020	LEE; Sang Min	G11C16/10	1/1
*	H	US-20170025183-A1	01-2017	LEE; Hee Youl	G11C16/10	1/1
	I					
	J					
	K					
	L					
	M					

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

<i>Search Notes</i> 	Application/Control No. 17/191,768	Applicant(s)/Patent Under Reexamination LEE et al.
	Examiner LY D PHAM	Art Unit 2827

CPC - Searched*		
Symbol	Date	Examiner
G11C 16/3459, 16/0433, 16/10, 16/26, 16/30	06/04/2022	LP

CPC Combination Sets - Searched*		
Symbol	Date	Examiner

US Classification - Searched*			
Class	Subclass	Date	Examiner
365	185.22	06/04/2022	LP

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	Date	Examiner
PE2E text search	06/04/2022	LP

Interference Search			
US Class/CPC Symbol	US Subclass/CPC Group	Date	Examiner
G11C	16/3459, 16/0433, 16/10, 16/26, 16/30	06/04/2022	LP

--	--

Issue Classification 	Application/Control No. 17/191,768	Applicant(s)/Patent Under Reexamination LEE et al.
	Examiner LY D PHAM	Art Unit 2827

CPC						
Symbol					Type	Version
G11C	/	16	/	3459	F	2013-01-01
G11C	/	16	/	10	I	2013-01-01
G11C	/	16	/	0433	I	2013-01-01
G11C	/	16	/	30	I	2013-01-01
G11C	/	16	/	26	I	2013-01-01

CPC Combination Sets					
Symbol				Type	Version
	/		/		

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	6	
/LY D PHAM/ Primary Examiner, Art Unit 2827	04 June 2022	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	10

U.S. Patent and Trademark Office

Part of Paper No.: 20220604

Issue Classification 	Application/Control No. 17/191,768	Applicant(s)/Patent Under Reexamination LEE et al.
	Examiner LY D PHAM	Art Unit 2827

INTERNATIONAL CLASSIFICATION			
CLAIMED			
G11C	/	16	/ 34
G11C	/	16	/ 04
G11C	/	11	/ 34
NON-CLAIMED			
/	/		

US ORIGINAL CLASSIFICATION	
CLASS	SUBCLASS
365	185.22

CROSS REFERENCES(S)						
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)					

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	6	
/LY D PHAM/ Primary Examiner, Art Unit 2827	04 June 2022	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	10

Issue Classification 	Application/Control No. 17/191,768	Applicant(s)/Patent Under Reexamination LEE et al.
	Examiner LY D PHAM	Art Unit 2827

☒ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47															
CLAIMS															
Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	15														
2	16														
3	17														
4	18														
5	19														
6	20														

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	6	
/LY D PHAM/ Primary Examiner, Art Unit 2827	04 June 2022	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	10

U.S. Patent and Trademark Office

Part of Paper No.: 20220604

Form PTO 1449 (Modified)		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		ATTY DOCKET NO. 533055US		SERIAL NO. 17/191,768	
LIST OF REFERENCES CITED BY APPLICANT				INVENTOR(S) Changhyun LEE, et al.			
				FILING DATE March 4, 2021		GROUP 2827	
U.S. PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
	AA	2019/0316928 A1	10/17/2019	MIGNOT, Y., et al.			
	AB	2020/0152654 A1	05/14/2020	HWANG, S.-M., et al.			
	AC						
	AD						
	AE						
	AF						
	AG						
	AH						
	AI						
	AJ						
	AK						
	AL						
	AM						
	AN						
FOREIGN PATENT DOCUMENTS							
		DOCUMENT NUMBER	DATE	COUNTRY	TRANSLATION YES NO		
	AO	111758162 A	10/09/2020	China			x
	AP	111279465 A	06/12/2020	China			x
	AQ	111180418 A	05/19/2020	China (corresponds to US 2020/0152654 A1)			x
	AR						
	AS						
	AT						
	AU						
	AV						
OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, etc.)							
	AW	International Search Report issued September 22, 2021 in PCT/CN2020/136462, citing documents AA and AO through AQ therein, 4 pages					
	AX						
	AY						
	AZ					☐ Additional References sheet(s) attached	
Examiner	/LY D PHAM/				Date considered	06/04/2022	
*Examiner: Initial if reference is considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.							

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /L.D.P/

PE2E SEARCH - Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	British Equivalents	Time Stamp
L1	0	17/191,768	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/03/08 09:30 PM
L2	307	((("YANGTZE") near3 ("MEMORY") near3 ("TECHNOLOGIES") near3 ("CO") near3 ("LTD"))).AS,AANM.	(USPAT)	OR	ON	ON	2022/03/08 09:31 PM
L3	316	((("LEE") near3 ("Changhyun")) OR (("ZHAO") near3 ("Xiangnan")) OR (("LI") near3 ("Haibo"))).INV.	(US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT)	OR	ON	ON	2022/03/08 09:32 PM
L4	5936	365/185.22.ccls.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/03/08 09:32 PM
L5	0	(G11C16/3459G11C16/0433G11C16/10G11C16/26G11C16/30)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO,	OR	ON	ON	2022/03/08 09:32 PM

L6	120836	(G11C16/3459 OR G11C16/0433 OR G11C16/10 OR G11C16/26 OR G11C16/30)	NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB) (US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/03/08 09:32 PM
L7	699	(2 3) AND (4 6)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/03/08 09:33 PM
L8	37782	(nand near2 string)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/03/09 08:31 AM
L9	83	((preread preverify pre- read pre-verify) near2 (bias potential voltage))	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY,	OR	ON	ON	2022/03/09 06:51 PM

L10	29303	WITH (selected near2 cell) (voltage bias potential) WITH ((unselected unselected) near2 (wordline (word ADJ line)))	CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB) (US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/03/09 07:51 PM
L11	23	(8 AND 9 AND 10)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/03/09 07:51 PM
L12	9034	(voltage bias potential) WITH (adjacent near2 (wordline (word ADJ line)))	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH,	OR	ON	ON	2022/03/09 07:52 PM

L13	14	11 AND 12	TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB) (US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/03/09 07:52 PM
L14	0	17/191,768	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/06/04 01:52 PM
L15	110	(nand near3 string) AND (preverify pre-verify)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/06/04 02:00 PM
L16	9	(preverify pre-verify) SAME ((bias voltage potential) WITH (adjacent near3 cell))	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA,	OR	ON	ON	2022/06/04 02:00 PM

L17	0	15 AND 16	EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB) (US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/06/04 02:00 PM
L18	4	("20190318928" "20200152654").pn.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/06/04 02:16 PM
L19	8	((preverify (pre-verify)) near2 stage) AND (verify near2 stage)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/06/04 02:19 PM

L20	5	((preverify (pre-verify)) SAME ((voltage bias potential) WITH (selected near3 gate)))	JPO; DERWENT; IBM_TDB) (US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/06/04 02:22 PM
L21	2	((preverify (pre-verify)) SAME ((voltage bias potential) WITH ((unprogrammed non- programmed (not\$1 near2 programmed)) near3 gate)))	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/06/04 02:23 PM
L22	109012	((G11C16/0483 OR G11C16/3459 OR G11C16/3454).cpc. OR (365/185.22 OR 365/185.18).ccls. OR (G11C16/34 OR G11C16/04 OR G11C11/34).ipc.)	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/06/04 02:33 PM
L23	9653	(read\$3 WITH cell) SAME (nand WITH string)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS,	OR	ON	ON	2022/06/04 02:34 PM

L24	0	((preverify (pre-verify)) near3 stage) SAME ((verif\$4 near3 (voltage bias potential level)) WITH (selected near3 cell))	IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB) (US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/06/04 02:35 PM
L25	94	((preverify (pre-verify)) SAME ((voltage bias potential level)) WITH (selected near3 cell))	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/06/04 02:36 PM
L26	0	((preverify (pre-verify)) SAME ((voltage bias potential level)) WITH (unprogrammed near3 cell))	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/06/04 02:36 PM

L27	66	((preverify (pre-verify)) SAME ((voltage bias potential level)) WITH (second near3 cell))	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/06/04 02:36 PM
L28	1082	(verify SAME ((second near3 (voltage bias potential level)) WITH (selected near2 cell)))	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/06/04 02:37 PM
L29	0	(23 AND 25 AND 27 AND 28)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/06/04 02:38 PM
L30	0	(23 AND 25 AND 28)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO,	OR	ON	ON	2022/06/04 02:38 PM

L31	143	(23 AND 28)	MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB) (US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/06/04 02:38 PM
L32	94	((preverify (pre-verify)) SAME ((voltage bias potential level) WITH (selected near3 cell)))	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/06/04 02:39 PM
L33	4	((preverify (pre-verify)) SAME ((voltage bias potential level) WITH (non-selected near3 cell)))	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/06/04 02:40 PM
L34	884	(verify SAME ((voltage bias potential level)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP,	OR	ON	ON	2022/06/04 02:40 PM

		WITH (non-selected near3 cell)))	AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)				
L35	11730	(verify SAME ((voltage bias potential level) WITH (selected near3 cell)))	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/06/04 02:40 PM
L36	4	(32 AND 33 AND 34 AND 35)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/06/04 02:40 PM
L37	4	(32 AND 34 AND 35)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO,	OR	ON	ON	2022/06/04 02:41 PM

L38	94	(32 AND 35)	RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB) (US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/06/04 02:41 PM
L39	102415	((G11C16/26 OR G11C16/3459).cpc. OR (365/185.22 OR 365/185.17 OR 365/185.18).ccls. OR (G11C16/26 OR G11C16/34 OR G11C16/04).ipc.)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/06/04 02:43 PM
L40	25	(32 AND 35).clm.	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/06/04 02:43 PM
L41	1131	(2 3) AND (4 6 22 39)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU,	OR	ON	ON	2022/06/04 02:44 PM

L42	0	38 AND 41	CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB) (US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/06/04 02:44 PM
-----	---	-----------	--	----	----	----	---------------------

PE2E SEARCH - Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	British Equivalents	Time Stamp
N1	1005	((("YANGTZE") near3 ("MEMORY") near3 ("TECHNOLOGIES") near3 ("CO") near3 ("LTD"))).AS,AANM.	(US-PGPUB; USPAT)	OR	ON	ON	2022/06/04 02:28 PM
N2	314	((("LEE") near3 ("Changhyun")) OR ("ZHAO") near3 ("Xiangnan")) OR ("LI") near3 ("Haibo"))).INV.	(US-PGPUB; USPAT)	OR	ON	ON	2022/06/04 02:28 PM
N3	3513	365/185.22.ccls.	(US-PGPUB; USPAT)	OR	ON	ON	2022/06/04 02:29 PM
N4	0	(G11C16/3459G11C16/0433G11C16/10G11C16/26G11C16/30)	(US-PGPUB; USPAT)	OR	ON	ON	2022/06/04 02:29 PM
N5	30237	(G11C16/3459 OR G11C16/0433 OR G11C16/10 OR G11C16/26 OR G11C16/30)	(US-PGPUB; USPAT)	OR	ON	ON	2022/06/04 02:29 PM
N6	38208	((G11C16/0483 OR G11C16/3459 OR	(US-PGPUB; USPAT)	OR	ON	ON	2022/06/04 02:33 PM

N7	36065	G11C16/3454).cpc. OR (365/185.22 OR 365/185.18).ccls. OR (G11C16/34 OR G11C16/04 OR G11C11/34).ipc.) ((G11C16/26 OR G11C16/3459).cpc. OR (365/185.22 OR 365/185.17 OR 365/185.18).ccls. OR (G11C16/26 OR G11C16/34 OR G11C16/04).ipc.)	(US-PGPUB; USPAT)	OR	ON	ON	2022/06/04 02:43 PM
N8	342	(N1 N2) AND (N3 N5 N6 N7)	(US-PGPUB; USPAT)	OR	ON	ON	2022/06/04 02:45 PM
N9	11800	(nand WITH cell WITH read\$3)	(US-PGPUB; USPAT)	OR	ON	ON	2022/06/04 02:50 PM
N10	39	(preverify (pre-verify) near3 stage)	(US-PGPUB; USPAT)	OR	ON	ON	2022/06/04 02:50 PM
N11	2872	(verify near3 stage)	(US-PGPUB; USPAT)	OR	ON	ON	2022/06/04 02:50 PM
N12	72054	(bias potential voltage level) WITH (selected near3 cell)	(US-PGPUB; USPAT)	OR	ON	ON	2022/06/04 02:50 PM
N13	17180	(bias potential voltage level) WITH ((non- selected unselected un- selected nonselected) near3 cell)	(US-PGPUB; USPAT)	OR	ON	ON	2022/06/04 02:51 PM
N14	0	(9 AND 10 AND 11 AND 12 AND 13)	(US-PGPUB; USPAT)	OR	ON	ON	2022/06/04 02:51 PM
N15	42	(9 AND 11 AND 12 AND 13)	(US-PGPUB; USPAT)	OR	ON	ON	2022/06/04 02:51 PM
N16	0	(9 AND 11 AND 12 AND 13).clm.	(US-PGPUB; USPAT)	OR	ON	ON	2022/06/04 02:51 PM
N17	0	(N8 AND N15)	(US-PGPUB; USPAT)	OR	ON	ON	2022/06/04 02:51 PM

Bibliographic Data

Application No: 17/191,768

Foreign Priority claimed: ☐ Yes ☒ No

35 USC 119 (a-d) conditions met: ☐ Yes ☒ No ☐ Met After Allowance

Verified and Acknowledged:

/LY D PHAM/

Examiner's Signature

Initials

Title:

ARCHITECTURE AND METHOD FOR NAND MEMORY
OPERATION

FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
03/04/2021	365	2827	533055US
RULE			

APPLICANTS

Yangtze Memory Technologies Co., Ltd., Wuhan, CHINA

INVENTORS

Changhyun LEE, Wuhan, CHINA

Xiangnan ZHAO, Wuhan, CHINA

Haibo LI, Wuhan, CHINA

CONTINUING DATA

This application is a CON of PCT/CN2020/136482 12/15/2020

FOREIGN APPLICATIONS

IF REQUIRED, FOREIGN LICENSE GRANTED**

03/15/2021

STATE OR COUNTRY

CHINA

ADDRESS

OBLON, MCCLELLAND, MAIER & NEUSTADT, L.L.P.

1940 DUKE STREET

ALEXANDRIA, VA 22314

UNITED STATES

FILING FEE RECEIVED

\$1,820



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
17/191,768	03/04/2021	Changhyun LEE	533055US

CONFIRMATION NO. 5157

PUBLICATION NOTICE

22850
OBLON, MCCLELLAND, MAIER & NEUSTADT, L.L.P.
1940 DUKE STREET
ALEXANDRIA, VA 22314



OC000000134578851

Title:ARCHITECTURE AND METHOD FOR NAND MEMORY OPERATION

Publication No.US-2022-0189566-A1

Publication Date:06/16/2022

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publically available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently <http://www.uspto.gov/patft/>.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Public Records Division. The Public Records Division can be reached by telephone at (571) 272-3150 or (800) 972-6382, by facsimile at (571) 273-3250, by mail addressed to the United States Patent and Trademark Office, Public Records Division, Alexandria, VA 22313-1450 or via the Internet.

In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at www.uspto.gov using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently <https://portal.uspto.gov/pair/PublicPair>. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

Further assistance in electronically accessing the publication, or about PAIR, is available by calling the Patent Electronic Business Center at 1-866-217-9197.

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), by mail or fax, or via EFS-Web.

By mail, send to: Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

By fax, send to: (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

22850 7590 06/08/2022
OBLON, MCCLELLAND, MAIER & NEUSTADT, L.L.P.
1940 DUKE STREET
ALEXANDRIA, VA 22314

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being transmitted to the USPTO via EFS-Web or by facsimile to (571) 273-2885, on the date below.

(Typed or printed name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/191,768	03/04/2021	Changhyun LEE	533055US	5157

TITLE OF INVENTION: ARCHITECTURE AND METHOD FOR NAND MEMORY OPERATION

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$1200	\$0.00	\$0.00	\$1200	09/08/2022

EXAMINER	ART UNIT	CLASS-SUBCLASS
PHAM, LY D	2827	365-185220

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

☐ Change of correspondence address (or Change of Correspondence Address form PTO/AIA/122 or PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/AIA/47 or PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,

(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 Oblon, McClelland,2 Maier & Neustadt, L.L.P.

3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

Yangtze Memory Technologies Co., Ltd.

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Wuhan, CHINA

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. Fees submitted: ☒ Issue Fee ☐ Publication Fee (if required) ☐ Advance Order - # of Copies _____

4b. Method of Payment: (Please first reapply any previously paid fee shown above)

☒ Electronic Payment via EFS-Web ☐ Enclosed check ☐ Non-electronic payment by credit card (Attach form PTO-2038)

☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. 15-0030

5. Change in Entity Status (from status indicated above)

☐ Applicant certifying micro entity status. See 37 CFR 1.29

☐ Applicant asserting small entity status. See 37 CFR 1.27

☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature /Bogdan A. Zinchenko/Date September 6, 2022Typed or printed name Bogdan A. ZinchenkoRegistration No. 57,473

Electronic Patent Application Fee Transmittal				
Application Number:		17191768		
Filing Date:		04-Mar-2021		
Title of Invention:		ARCHITECTURE AND METHOD FOR NAND MEMORY OPERATION		
First Named Inventor/Applicant Name:		Changhyun LEE		
Filer:		Philippe Jean-Claude Signore/Candice Kinard		
Attorney Docket Number:		533055US		
Filed as Large Entity				
Filing Fees for Utility under 35 USC 111(a)				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
UTILITY APPL ISSUE FEE	1501	1	1200	1200

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				1200

Electronic Acknowledgement Receipt	
EFS ID:	46566745
Application Number:	17191768
International Application Number:	
Confirmation Number:	5157
Title of Invention:	ARCHITECTURE AND METHOD FOR NAND MEMORY OPERATION
First Named Inventor/Applicant Name:	Changhyun LEE
Customer Number:	22850
Filer:	Philippe Jean-Claude Signore/Candice Kinard
Filer Authorized By:	Philippe Jean-Claude Signore
Attorney Docket Number:	533055US
Receipt Date:	07-SEP-2022
Filing Date:	04-MAR-2021
Time Stamp:	14:21:41
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	\$ 1200
RAM confirmation Number	E202297E22010115
Deposit Account	
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:	

File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	533055us.pdf	2181448	no	1
			1d65dda23924143098b22e344b1742cf0bcd8ace		
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	37855	no	2
			52346b5d735288539e9857e1215c1e824d61aad8		
Warnings:					
Information:					
Total Files Size (in bytes):			2219303		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/191,768	10/11/2022	11468957	533055US	5157

22850 7590 09/21/2022
OBLON, MCCLELLAND, MAIER & NEUSTADT, L.L.P.
1940 DUKE STREET
ALEXANDRIA, VA 22314

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Patents Stakeholder Experience (OPSE), Stakeholder Support Division (SSD) at (571)-272-4200.

INVENTOR(s) (Please see PAIR WEB site <http://pair.uspto.gov> for additional inventors):

Changhyun LEE, Wuhan, CHINA;
Xiangnan ZHAO, Wuhan, CHINA;
Haibo LI, Wuhan, CHINA;

APPLICANT(s) (Please see PAIR WEB site <http://pair.uspto.gov> for additional applicants):

Yangtze Memory Technologies Co., Ltd., Wuhan, CHINA;

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The USA offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to encourage and facilitate business investment. To learn more about why the USA is the best country in the world to develop technology, manufacture products, and grow your business, visit SelectUSA.gov.

IR103 (Rev. 10/09)