

(19) National Intellectual Property Office of the People's Republic of China



(12) Application for invention patent



(10) Application publication number
CN 109065091 A
(43) Application publication date
2018.12.21

(21) **Application No** . 201810864131.2

(22) **Application Date** 2018.08.01

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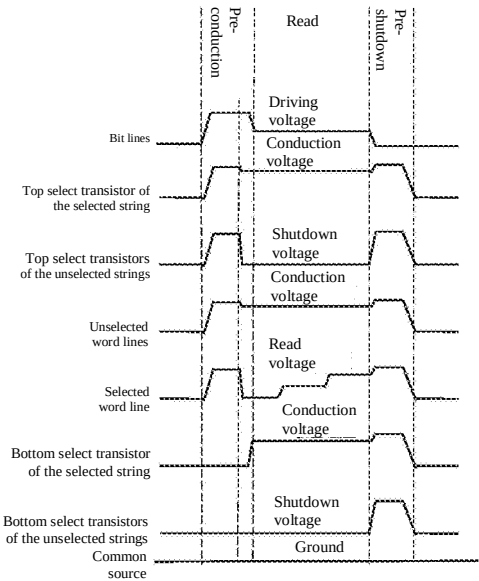
(51) **Int.Cl.**
G11C 16/26 (01/2006)
G11C 16/08 (01/2006)

Claims 1 page Specifications 4 pages Attached
Drawings 3 pages

(54) Name of invention
Reading Method for 3D NAND Flash

(57) Abstract

The invention relates to a reading method of 3D NAND flash memory. The 3D NAND flash memory includes a plurality of memory cells arranged in an array in a three-dimensional space, which constitutes multiple memory strings. The transistor at the top of each memory string is a top select transistor, and the top select transistor is connected to the bit line. The transistor at the bottom of the memory string is a bottom select transistor. Multiple memory cells located in the same layer form a memory row, the gates of the memory cells located in the same memory row are all connected to the same word line, and the memory string where the memory cell to be read is used as the selected string. It is characterized in that the reading method includes a pre-conduction phase and a reading phase performed in sequence, wherein in the pre-conduction phase, a continuous precharge voltage is applied to the bit line; at the same time, the top select transistor of the selected string and the top select transistor of the unselected string are turned on, and the bottom select transistor of the selected string and the bottom select transistor of the unselected string are turned off.



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1.A method of reading 3D NAND flash memory. The 3D NAND flash memory includes multiple memory cells arranged in an array in a three-dimensional space to form multiple memory strings. The transistor at the top of each memory string is a top select transistor. The top select transistor is connected to the bit line, and the transistor at the bottom of the memory string is the bottom select transistor. Multiple memory cells located in the same layer form a memory row. The gates of the memory cells located in the same memory row are all connected to the same word line. The memory string in which the memory cell to be read is located is taken as the selected string, characterized in that the reading method includes a pre-conduction phase and a reading phase performed in sequence, wherein in the pre-conduction phase, a continuous precharge voltage is applied to the bit line; at the same time, the top select transistor of the selected string and the top select transistor of the unselected string are turned on, and the bottom select transistor of the selected string and the bottom select transistor of the unselected string are turned off.

2. The reading method of 3D NAND flash memory according to claim 1, characterized in that, in the reading phase, a driving voltage is applied to the bit line; the precharge voltage is greater than the driving voltage.

3. The reading method of 3D NAND flash memory according to claim 1, characterized in that the pre-conduction phase further includes: Before the end of the pre-conduction phase, the top select transistor of the unselected string is turned off; a precharge voltage is applied to the bit line until the end of the pre-conduction phase.

4. The reading method of 3D NAND flash memory according to claim 1, characterized in that the pre-conduction phase further includes: While a precharge voltage is applied to the bit line, a pre-conduction voltage is applied to the selected word line and the unselected word line.

5. The reading method of 3D NAND flash memory according to claim 1, characterized in that a pre-shutdown phase is located after the read phase; in the pre-shutdown phase, the bit line maintains a low potential.

6. The reading method of 3D NAND flash memory according to claim 5, characterized in that in the pre-shutdown phase, the top select transistor of the selected string, the top select transistor of the unselected string, the bottom select transistor of the selected string and the bottom select transistor of the unselected string are turned on, and a pre-shutdown voltage is applied to both the unselected word line and the selected word line.

Reading method for 3D NAND flash memory

Technical field

[0001] The present invention relates to the field of semiconductor technology, and in particular, to a reading method of 3D NAND flash memory.

Background technology

[0002] In recent years, the development of flash memory (Flash Memory) has been particularly rapid. The main feature of flash memory is that it can retain stored information for a long time without being powered on, and has the advantages of high integration, fast access speed, easy erasure and rewriting, etc. Therefore, it has been widely used in many fields such as microcomputers and automation control. In order to further improve the bit density of flash memory (Bit Density) and reduce the bit cost (Bit Cost), three-dimensional flash memory (3D NAND) technology has been rapidly developed.

[0003] In the 3D NAND flash memory structure, three-dimensional arrangements are performed according to strings and rows. When the existing technology performs a read operation on a certain memory cell, it often causes read interference to other memory cells adjacent to the memory cell, causing data drift.

[0004] How to reduce read interference and improve the accuracy of read data during the reading process is an issue that needs to be solved urgently.

Content of the invention

[0005] The technical problem to be solved by the present invention is to provide a reading method of 3D NAND flash memory to reduce read interference during the reading process.

[0006] The present invention provides a method for reading a 3D NAND flash memory. The 3D NAND flash memory includes a plurality of memory cells arranged in an array in a three-dimensional space to form a plurality of memory strings. The transistor at the top of each memory string is a top select transistor, and the top select transistor is connected to the bit line. The transistor at the bottom of the memory string is a bottom select transistor. Multiple memory cells located in the same layer form a memory row, the gates of the memory cells located in the same memory row are all connected to the same word line, and the memory string in which the memory cell is to be read is used as the selected string. The reading method includes a pre-conduction phase and a reading phase step in sequence, wherein, in the pre-conduction phase, a continuous precharge voltage is applied to the bit line; at the same time, the top select transistor of the selected string and the top select transistor of the unselected string are turned on, and the bottom select transistor of the selected string and the bottom select transistor of the unselected string are turned off.

[0007] Optionally, in the reading phase, a driving voltage is applied to the bit line; the precharge voltage is greater than the driving voltage.

[0008] Optionally, the pre-conduction phase also includes: Before the end of the pre-conduction phase, the top select transistor of the unselected string is turned off; a precharge voltage is applied to the bit line until the end of the pre-conduction phase.

[0009] Optionally, the pre-conduction phase also includes: While a precharge voltage is applied to the bit line, a pre-conduction voltage is applied to the selected word line and the unselected

word line.

[0010] Optionally, it also includes a pre-shutdown phase located after the read phase; in the pre-shutdown phase, the bit line maintains a low potential.

[0011] Optionally, in the pre-shutdown phase, the top select transistor of the selected string, the top select transistor of the unselected string, the bottom select transistor of the selected string, and the bottom select transistor of the unselected string are turned on, and a pre-shutdown voltage is applied to both the unselected word line and the selected word line.

[0012] In the 3D NAND flash memory reading method of the present invention, there is a pre-conduction phase before formal reading. In the pre-conduction phase, a precharge voltage is applied to the bit line, and the top select transistor and bottom select transistor of the unselected string are turned off before the reading phase. This makes the channel potential of the unselected string equal to the precharge voltage during the reading phase, thereby reducing the read interference suffered by the unselected string and reducing reading errors.

Accompanying figure description

[0013] Figure 1 is a diagram of the storage structure of 3D NAND according to a specific embodiment of the present invention;

[0014] Figure 2 is a timing diagram for reading a 3D NAND memory cell according to a specific embodiment of the present invention;

[0015] Figure 3 is a timing diagram for reading a 3D NAND memory cell according to a specific embodiment of the present invention.

Specific embodiments

[0016] The specific embodiment of the reading method of the 3D NAND flash memory provided by the present invention will be described in detail below with reference to the accompanying figures.

[0017] Please refer to Figure 1, which is a diagram of the storage structure of 3D NAND according to a specific embodiment of the present invention. Each black dot represents a memory cell.

[0018] The storage structure of the 3D NAND includes multiple memory cells arranged in an array in a three-dimensional space to form multiple memory strings, and the channels of the memory cells located in the same memory string are physically connected. The transistor at the top of each memory string is a top select transistor, and the top select transistor is connected to the bit line. The transistor at the bottom of the memory string is a bottom select transistor. Different memory strings are distinguished by top select transistors and bottom select transistors. Multiple memory cells located in the same layer form a memory row. The gates of the memory cells located in different memory strings but located in the same memory row are physically connected and are connected to the same word line.

[0019] When performing a read operation on a certain memory cell in the storage structure, it is necessary to determine the memory string and the row where the selected memory cell is located. The memory string where the selected memory cell is located is used as the selected string, and the row where it is located is used as the selected row. For example, to read the information of the selected memory cell circled in Figure 1, it is necessary to apply a driving voltage to bit line 1 and bit line 2, turn on the top select transistor 1 and the bottom select transistor 1 of the selected string

where the selected memory cell is located, apply a conduction voltage to the word line 1 and word line 3 of the unselected rows other than the row where the memory cell is located, thereby turning on the channel of the selected string; in addition, turn off the top select transistor 2 and bottom select transistor 2 of the unselected string, and prevent the channels of other unselected strings from being turned on; apply a read voltage to the word line 2 of the selected row to read the information in the selected memory cell.

[0020] Since a conduction voltage is applied to the word line 1 and word line 3 of the unselected row, during its rising process, this conduction voltage will generate a potential via channel coupling in all memory cells connected to word line 1 and word line 3, causing hot carrier injection crosstalk, which causes the electrons stored in other unselected memory cells to drift, resulting in changes in the data stored in the unselected memory cells, as well as problems such as drift in the data in the selected memory cell that is read.

[0021] Please refer to Figure 2, which is a timing diagram of reading a 3D NAND memory cell in a specific embodiment.

[0022] The memory string where the memory cell to be read is located is used as the selected string, the storage row where the memory cell is to be read is used as the selected row, and the word line connected to the selected row is used as the selected word line. In this specific embodiment, before actually reading the memory cell, there is a pre-conduction phase to turn on the channels of the selected string and the unselected strings.

[0023] Specifically, in the pre-conduction stage, a pre-conduction voltage is applied to both the unselected word line and the selected word line to turn on the channels of the selected string and the unselected string. During the rising period of the voltage of the unselected word line and the selected word line, the voltage applied to the top select transistor of the unselected string and the bottom select transistor of the unselected string also rises. In this way, the top select transistor of the unselected string and the bottom select transistor of the unselected string are both turned on; a pre-conduction voltage is also applied to the top select transistor of the selected string and the bottom select transistor of the selected string, so that the top select transistor of the selected string and the bottom select transistor of the selected string are both turned on; at the same time, the bit line remains at a low potential. In the specific embodiment of the present invention, the low potential is 0V. In other specific embodiments, the low potential can also be other voltage values. The channels of the unselected string and the selected string are connected to the bit line, and the channel potential will remain at the same low potential as the bit line. Therefore, the channels of the unselected string and the selected string will not generate voltage coupling due to changes in the word line voltage, thereby avoiding the problem of hot carrier injection crosstalk caused when a conduction voltage is applied to the word line of an unselected memory cell.

[0024] In the reading phase, a driving voltage is applied to the bit line, and a disconnection voltage is applied to the top select transistor of the unselected string and the bottom select transistor of the unselected string, turning off the top select transistor and the bottom select transistor of the unselected string so that the channel of the unselected string is disconnected from the bit line, and the channel potential of the unselected string is locked to a low potential of 0V. The memory cells in the unselected rows with a conduction voltage applied to the unselected strings are subject to read interference caused by "conduction voltage - 0V", while the memory cells in the selected rows of the unselected strings are subject to read interference caused by "read voltage - 0V", the read voltage is close to the conduction voltage.

[0025] The top select transistor and the bottom select transistor of the selected string are applied with a conduction voltage, so that the channel of the selected string is connected to the bit line, and the channel potential of the selected string is equal to the driving voltage on the bit line. The gates of the unselected memory cells on the selected string are applied with a conduction voltage through the unselected word lines. Therefore, the unselected memory cells on the selected string will withstand read interference caused by "conduction voltage - driving voltage".

[0026] Read interference is positively related to the voltage causing read interference. The greater the voltage, the stronger the read interference. Therefore, the greater the conduction voltage, the greater the read disturbance to the memory cell. Therefore, in this specific embodiment, the read interference caused by the "conduction voltage - driving voltage" suffered by the unselected memory cells on the selected string is smaller than the read interference suffered by the memory cells on the unselected string. In order to improve the accuracy of memory reading, it is necessary to further reduce the read interference suffered by the memory cells on the unselected string.

[0027] In order to further reduce the read interference suffered by the memory cells with conduction voltage on the unselected strings, the inventors of the present invention propose another reading method of 3D NAND flash memory.

[0028] Please refer to Figure 3, which is a timing diagram of reading a 3D NAND memory cell using another reading method in another specific embodiment of the present invention.

[0029] In this specific embodiment, the reading method of the 3D NAND flash memory includes the steps of a pre-conduction phase and a reading phase performed in sequence.

[0030] During the entire reading process, the common source terminals of the memory structure are grounded. What is different from the previous specific embodiment is that in the pre-conduction phase: A continuous precharge voltage is applied to the bit line; at the same time, the top select transistor of the selected string and the top select transistor of the unselected string are pre-conducted, and the bottom select transistor of the selected string and the bottom select transistor of the unselected string are turned off.

[0031] In the pre-conduction phase, it also includes applying a pre-conduction voltage to both the selected row word lines and the unselected row word lines, so that the channel of each memory cell is turned on. Since the top select transistor of the unselected string is turned on, the channel of the unselected string is connected to the bit line, and the channel potential is equal to the precharge voltage on the bit line. The channel potential is consistent with the bit line voltage, so that no voltage coupling is generated when a voltage is applied to the word line, thus avoiding the problem of hot carrier injection crosstalk.

[0032] Since a precharge voltage is applied to the bit line, if the bottom select transistor of the selected string and the bottom select transistor of the unselected string are in a turned-on state, a larger leakage will occur. Therefore, it is necessary to turn off the bottom select transistor of the selected string and the bottom select transistor of the unselected string during the pre-conduction stage. In addition, turning off the bottom select transistor of the selected string and the bottom select transistor of the unselected string allows the channels and bit lines of each memory string to still be connected, and no hot carrier injection interference will occur.

[0033] In this specific embodiment, before the end of the pre-conduction phase, the top select transistor of the unselected string is turned off first, and a precharge voltage is applied to the bit line until the end of the pre-conduction phase. In this way, before the top select transistor of the unselected string is turned off, the channel potential of the unselected string is always equal to the

precharge voltage on the bit line; when the top select transistor of the unselected string is turned off and the bottom select transistor of the unselected string is also turned off, the potential in the channel of the unselected string will remain at the precharge voltage. In other specific embodiments, at the end of the pre-conduction phase, the top select transistor of the unselected string can be turned off while adjusting the bit line voltage from the precharge voltage to the driving voltage.

[0034] In the reading phase, a driving voltage is applied to the bit line, and the top select transistor gate of the selected string and the bottom select transistor gate of the selected string are applied with a conduction voltage; a shutdown voltage is applied to the gates of the top and bottom select transistors of the unselected string; a conduction voltage is applied to the unselected word line, and a read voltage is applied to the selected word line to read the selected memory cell. In the read phase, the channel potential of the unselected string is the precharge voltage. The memory cells of the unselected rows on the unselected string are subject to read interference caused by the "conduction voltage - precharge voltage". The unselected memory cells on the selected row of unselected strings are subject to read interference caused by "read voltage - precharge voltage". Since the precharge voltage is a high voltage, the reading method of this specific embodiment can effectively reduce read disturbance of memory cells on unselected strings.

[0035] For the selected string, since in the reading phase, the top select switch and the bottom select transistor of the selected string are both turned on, therefore, the channel potential of the selected string is equal to the driving voltage on the bit line, and therefore, the unselected memory cells on the selected string are subject to read disturbance caused by "conduction voltage - driving voltage".

[0036] In a specific embodiment, the precharge voltage is greater than the driving voltage, so that the read interference suffered by the memory cells on the unselected string is less than the read interference suffered by the memory cells on the selected string, and thus reducing read errors to a greater extent.

[0037] In a specific embodiment of the present invention, the reading method includes a pre-shutdown phase located after the reading phase. In the pre-shutdown phase, voltage application to the bit line connected to the selected string is stopped, so that the bit line voltage remains low. A conduction voltage is applied to the top select transistor and bottom select transistor of the selected string, and to the top select transistor and bottom select transistor of the unselected string, so that they are all turned on. At the same time, a conduction voltage is applied to both the selected word line and the unselected word line, so that the channels of the selected string and the unselected string are both connected to the bit line, the common source terminal is connected to ground, the electrons in the channels of the selected string and the unselected string are exported, and the channel potential of each memory cell is lowered to 0, in order to facilitate subsequent read or erase operations.

[0038] In the specific embodiment of the present invention, in the process of reading 3D NAND flash memory, there is a pre-conduction phase before formal reading. In the pre-conduction phase, a precharge voltage is applied to the bit line. The top and bottom select transistors of the unselected strings are turned off before the reading phase, so that the channel potential of the unselected strings is equal to the precharge voltage during the reading phase, thereby reducing the read interference suffered by the unselected strings, thereby reducing read errors during reading of 3D NAND flash memory.

[0039] The above are only preferred embodiments of the present invention. It should be pointed out that those of ordinary skill in the art can also make several improvements and modifications without departing from the principles of the present invention. These improvements and modifications should also be regarded as the protection scope of the present invention.

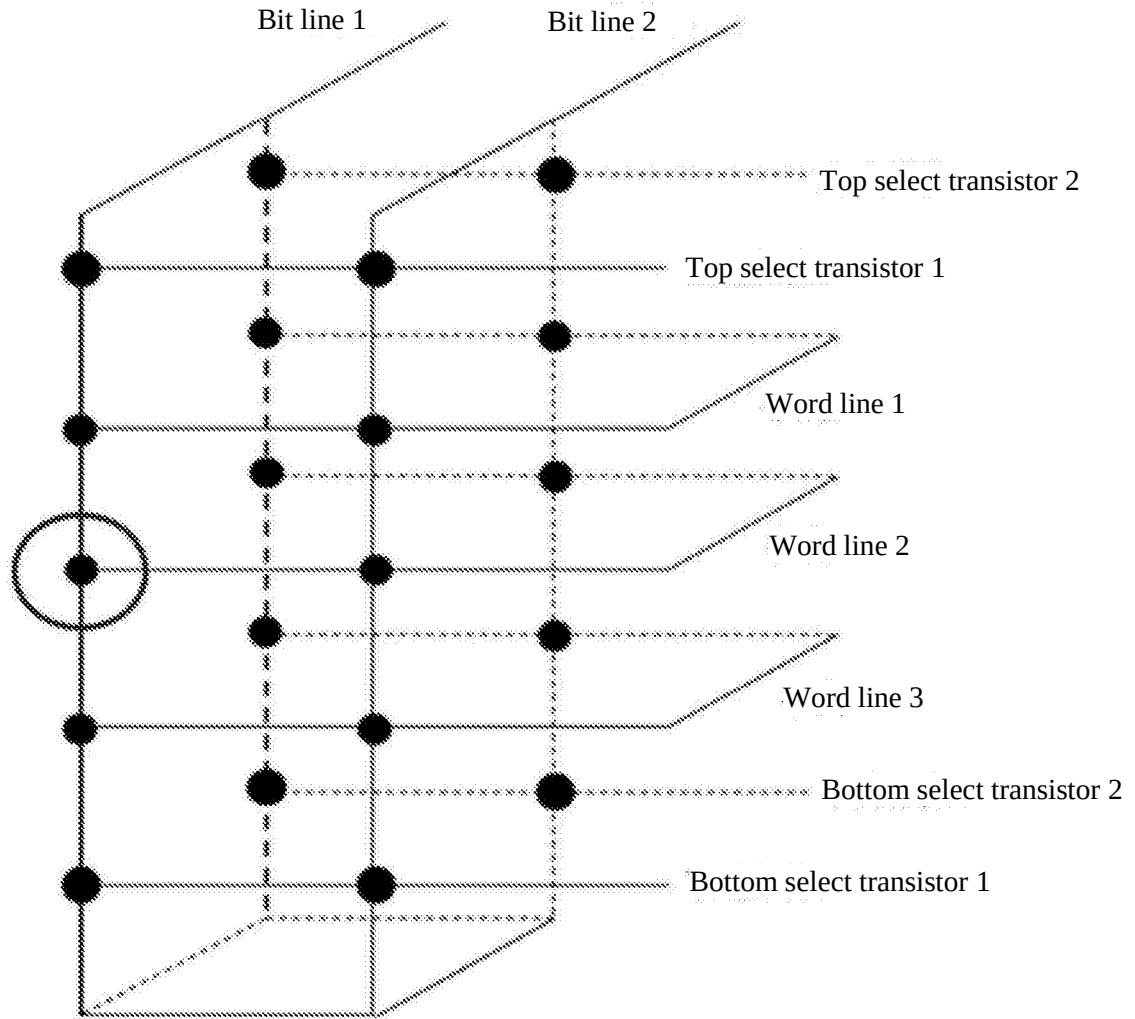


Figure1

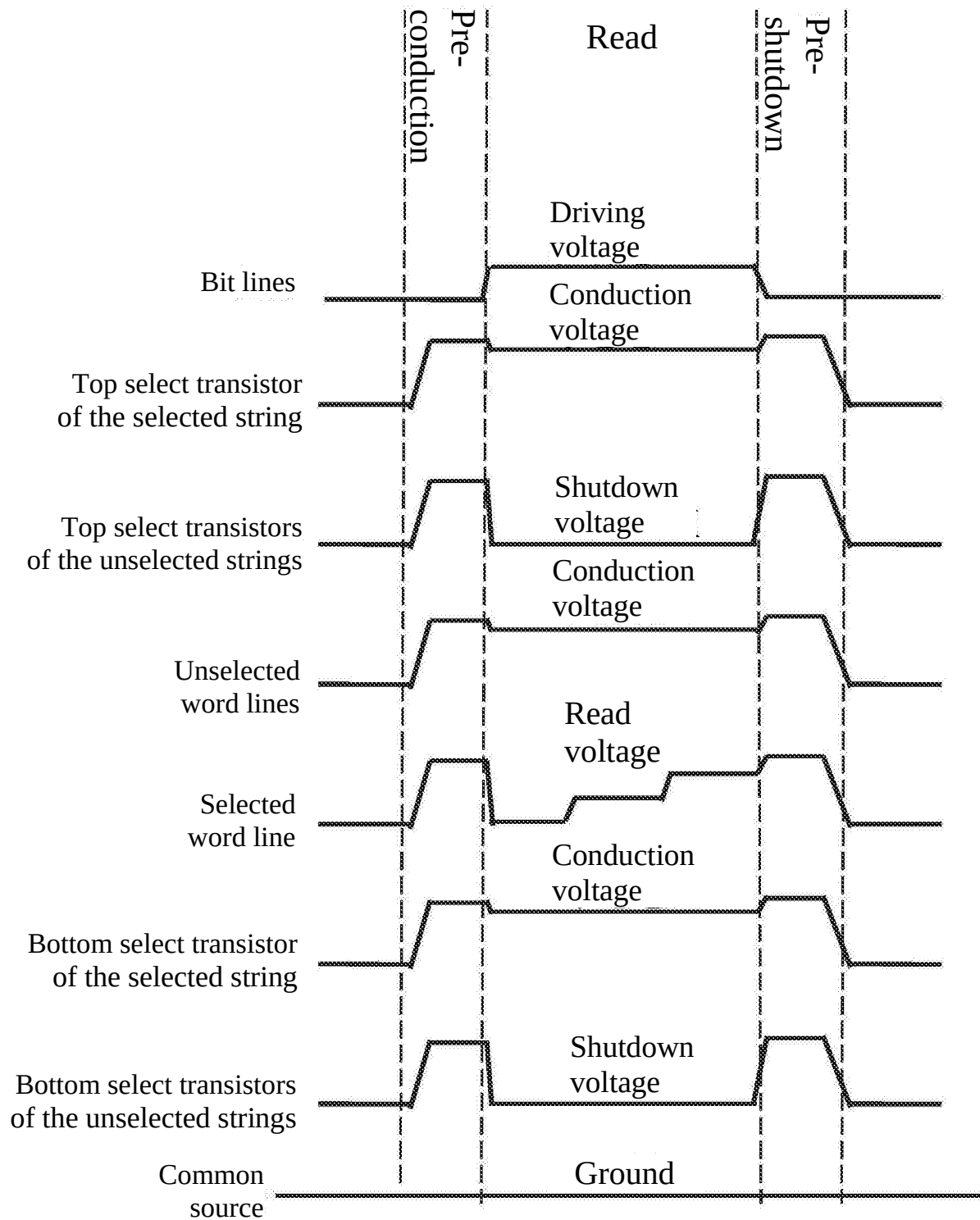


Figure2

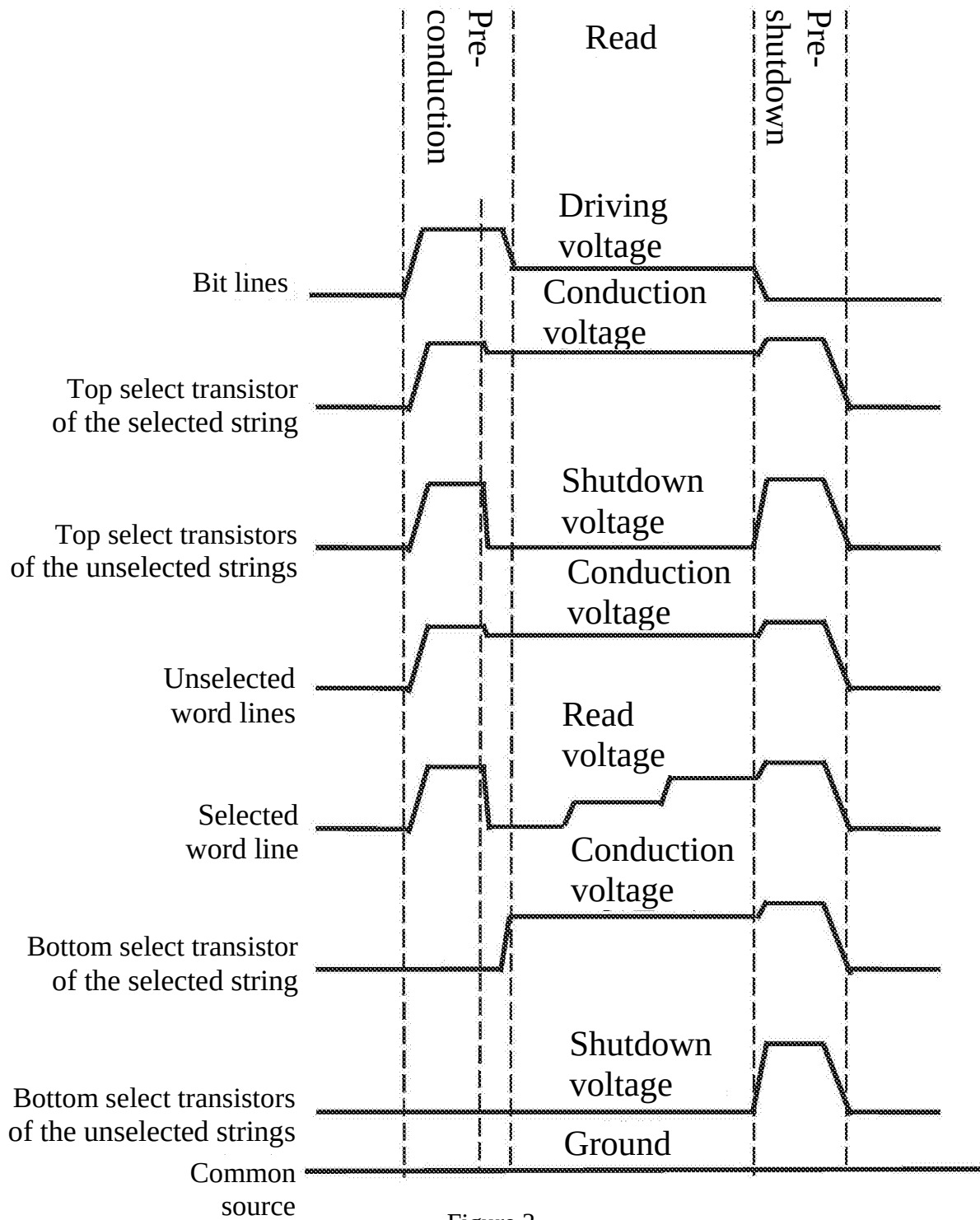


Figure 3



March 26, 2024

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My qualifications are as follows: 8 years of experience as a professional translator/interpreter, studied Mandarin Chinese at New York University.

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Karen Lee

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26th of March 2024

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IPR2024-00792



(12)发明专利申请

(10)申请公布号 CN 109065091 A

(43)申请公布日 2018. 12. 21

(21)申请号 201810864131.2

(22)申请日 2018.08.01

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(51)Int. Cl.

G11C 16/26(2006.01)

G11C 16/08(2006.01)

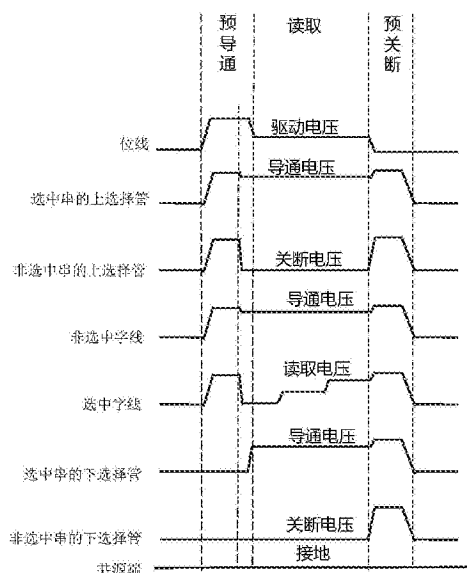
权利要求书1页 说明书4页 附图3页

(54)发明名称

3D NAND闪存的读取方法

(57)摘要

本发明涉及一种3D NAND闪存的读取方法，所述3D NAND闪存包括在三维空间内阵列排布的多个存储单元，构成多个存储串，每一个存储串的顶部的晶体管为上选择管，所述上选择管连接至位线，存储串底部的晶体管为下选择管，位于同一层内的多个存储单元组成存储行，位于同一存储行内的存储单元的栅极均连接至同一字线，待读取存储单元所在的存储串作为选中串，其特征在于，所述读取方法包括依次进行的预导通阶段和读取阶段步骤，其中，在所述预导通阶段中对位线施加持续的预充电电压；同时，导通选中串的上选择管和非选中串的上选择管，关断选中串的下选择管和非选中串的下选择管。



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1. 一种3D NAND闪存的读取方法,所述3D NAND闪存包括在三维空间内阵列排布的多个存储单元,构成多个存储串,每一个存储串的顶部的晶体管为上选择管,所述上选择管连接至位线,存储串底部的晶体管为下选择管,位于同一层内的多个存储单元组成存储行,位于同一存储行内的存储单元的栅极均连接至同一字线,待读取存储单元所在的存储串作为选中串,其特征在于,所述读取方法包括依次进行的预导通阶段和读取阶段步骤,其中,在所述预导通阶段中对位线施加持续的预充电电压;同时,导通选中串的上选择管和非选中串的上选择管,关断选中串的下选择管和非选中串的下选择管。

2. 根据权利要求1所述的3D NAND闪存的读取方法,其特征在于,读取阶段中,对位线施加驱动电压;所述预充电电压大于所述驱动电压。

3. 根据权利要求1所述的3D NAND闪存的读取方法,其特征在于,在所述预导通阶段中还包括:在预导通阶段结束之前,关断所述非选中串的上选择管;对位线施加预充电电压直至预导通阶段结束。

4. 根据权利要求1所述的3D NAND闪存的读取方法,其特征在于,在所述预导通阶段中还包括:在对位线施加预充电电压的同时,对选中字线和非选中字线施加预导通电压。

5. 根据权利要求1所述的3D NAND闪存的读取方法,其特征在于,还包括位于所述读取阶段之后的预关断阶段;所述预关断阶段中,位线保持低电位。

6. 根据权利要求5所述的3D NAND闪存的读取方法,其特征在于,所述预关断阶段中,导通选中串的上选择管、非选中串的上选择管、选择串的下选择管和非选中串的下选择管,以及对非选中字线和选中字线均施加预关断电压。

3D NAND闪存的读取方法

技术领域

[0001] 本发明涉及半导体技术领域,尤其涉及一种3D NAND闪存的读取方法。

背景技术

[0002] 近年来,闪存(Flash Memory)存储器的发展尤为迅速。闪存存储器的主要特点是在不加电的情况下能长期保持存储的信息,且具有集成度高、存取速度快、易于擦除和重写等优点,因而在微机、自动化控制等多项领域得到了广泛的应用。为了进一步提高闪存存储器的位密度(Bit Density),同时减少位成本(Bit Cost),三维的闪存存储器(3D NAND)技术得到了迅速发展。

[0003] 在3D NAND闪存结构中,按照串和行进行三维排列,现有技术在对某一存储单元进行读取操作时,经常会对该存储单元相邻的其他存储单元造成读干扰的问题,造成数据漂移。

[0004] 如何在读取过程中,减少读干扰,提高读取数据的准确性,是目前亟待解决的问题。

发明内容

[0005] 本发明所要解决的技术问题是,提供一种3D NAND闪存的读取方法,在读取过程中减少读干扰。

[0006] 本发明提供一种3D NAND闪存的读取方法,所述3D NAND闪存包括在三维空间内阵列排布的多个存储单元,构成多个存储串,每一个存储串的顶部的晶体管为上选择管,所述上选择管连接至位线,存储串底部的晶体管为下选择管,位于同一层内的多个存储单元组成存储行,位于同一存储行内的存储单元的栅极均连接至同一字线,待读取存储单元所在的存储串作为选中串,所述读取方法包括依次进行的预导通阶段和读取阶段步骤,其中,在所述预导通阶段中对位线施加持续的预充电电压;同时,导通选中串的上选择管和非选中串的上选择管,关断选中串的下选择管和非选中串的下选择管。

[0007] 可选的,读取阶段中,对位线施加驱动电压;所述预充电电压大于所述驱动电压。

[0008] 可选的,在所述预导通阶段中还包括:在预导通阶段结束之前,关断所述非选中串的上选择管;对位线施加预充电电压直至预导通阶段结束。

[0009] 可选的,在所述预导通阶段中还包括:在对位线施加预充电电压的同时,对选中字线和非选中字线施加预导通电压。

[0010] 可选的,还包括位于所述读取阶段之后的预关断阶段;所述预关断阶段中,位线保持低电位。

[0011] 可选的,所述预关断阶段中,导通选中串的上选择管、非选中串的上选择管、选择串的下选择管和非选中串的下选择管,以及对非选中字线和选中字线均施加预关断电压。

[0012] 本发明的3D NAND闪存读取方法中,在正式读取之前具有预导通阶段,在预导通阶段,对位线施加预充电电压,在读取阶段之前关断非选择串的上选择管和下选择管,使得在读

取阶段非选中串的沟道电势等于预充电电压,从而降低非选中串受到的读干扰,减少读取错误。

附图说明

[0013] 图1为本发明一具体实施方式的3D NAND的存储结构示意图;

[0014] 图2为本发明一具体实施方式的对3D NAND的存储单元进行读取的时序图;

[0015] 图3为本发明一具体实施方式的对3D NAND的存储单元进行读取的时序图。

具体实施方式

[0016] 下面结合附图对本发明提供的3D NAND闪存的读取方法的具体实施方式做详细说明。

[0017] 请参考图1,为本发明一具体实施方式的3D NAND的存储结构示意图。其中每个黑点代表一个存储单元。

[0018] 所述3D NAND的存储结构包括在三维空间内阵列排布的多个存储单元,构成多个存储串,位于同一个存储串内的存储单元的沟道在物理上连接。每一个存储串的顶部的晶体管为上选择管,上选择管连接至位线,存储串底部的晶体管为下选择管,不同存储串之间通过上选择管和下选择管区分。位于同一层内的多个存储单元组成存储行,位于不同存储串但位于同一存储行内的存储单元的栅极在物理上相连接,均连接至同一字线。

[0019] 在对所述存储结构中的某一存储单元进行读取操作时,需要确定选中的存储单元所在的存储串以及所在的行,所述选中的存储单元所在的存储串作为选中串,所在行作为选中行。例如,要读取图1中圈出的选中存储单元的信息,需要对位线1和位线2施加驱动电压,打开该选中存储单元所在选中串的上选择管1和下选择管1,将所述存储单元所在行以外的非选中行的字线1和字线3施加导通电压,从而将该选中串的沟道导通;并且关断非选中串的上选择管2和下选择管2,避免其他非选中串的沟道被导通;在选中行的字线2上加读取电压,对选中的存储单元内的信息进行读取。

[0020] 由于在所述非选中行的字线1和字线3上施加导通电压,这个导通电压在上升过程中会在连接至字线1和字线3上的所有存储单元的沟道内耦合出电势,造成热载流子注入串扰,从而导致其他非选中的存储单元内存储的电子发生漂移,从而发生非选中存储单元内存储的数据发生改变,以及读取的选中存储单元内的数据发生漂移等问题。

[0021] 请参考图2,为一个具体实施方式中的对3D NAND的存储单元进行读取的时序图。

[0022] 待读取的存储单元所在的存储串作为选中串,待读取的存储单元所在存储行作为选中行,连接至选中行的字线作为选中字线。该具体实施方式中,在对存储单元进行真正读取之前,会有一个预导通阶段,用来打开选中串和非选中串的沟道。

[0023] 具体的,在预导通阶段,对非选中字线和选中字线均施加预导通电压,以打开选中串和非选中串的沟道,在非选中字线和选中字线电压的上升时期,非选中串的上选择管和非选中串的下选择管施加的电压也跟随上升,这样使得所述非选中串的上选择管、非选中串的下选择管均打开;对所述选中串的上选择管、选中串的下选择管也施加预导通电压,使得所述选中串的上选择管、选中串的下选择管均打开;同时位线保持低电位。本发明的具体实施方式中,低电位均为0V,其他具体实施方式中低电位也可以为其他电压值。非选中串和

选中串的沟道与位线导通,沟道电势会保持和位线同样的低电位,因此非选中串和选中串的沟道不会因为字线电压的变化而耦合出电压,从而避免对非选中存储单元的字线施加导通电压时造成的热载流子注入串扰的问题。

[0024] 到了读取阶段,对位线施加驱动电压,对非选中串的上选择管和非选中串的下选择管施加断开电压,使得非选中串的上选择管和下选择管均关断,使得非选中串的沟道与位线断开,非选中串的沟道电势被锁定为低电位0V。非选中串上加导通电压的非选中行的存储单元受到“导通电压-0V”引起的读干扰,而非选中串的选中行的存储单元则受到“读取电压-0V”引起的读干扰,读取电压与导通电压接近。

[0025] 而选中串的上选择管和下选择管则被施加导通电压,使得选中串的沟道与位线导通,选中串的沟道电势等于位线上的驱动电压。选中串上的非选中存储单元的栅极则通过非选中字线被施加导通电压,因此,选中串上的非选中存储单元会承受“导通电压-驱动电压”引起的读干扰。

[0026] 读干扰和引起读干扰的电压正相关,电压越大,读干扰越强。因此,导通电压越大,对存储单元的读干扰越大。因此,该具体实施方式中,选中串上的非选中存储单元承受“导通电压-驱动电压”引起的读干扰小于非选中串上的存储单元受到的读干扰。为了提高存储器读取的准确性,需要进一步降低非选中串上的存储单元受到的读干扰。

[0027] 为了进一步降低非选中串上的加导通电压的存储单元受到的读干扰,本发明的发明人提出了另一种3D NAND闪存的读取方法。

[0028] 请参考图3为本发明另一具体实施方式中采用另一读取方法对3D NAND的存储单元进行读取的时序图。

[0029] 该具体实施方式中,所述3D NAND闪存的读取方法,包括依次进行的预导通阶段和读取阶段步骤。

[0030] 在整个读取过程中,存储结构的共源端均接地。与上一具体实施方式中不同的是,在所述预导通阶段中:对位线施加持续的预充电压;同时,预导通选中串的上选择管和非选中串的上选择管,关断选中串的下选择管和非选中串的下选择管。

[0031] 在预导通阶段,还包括对选中行字线以及非选中行字线均施加预导通电压,使得各个存储单元的沟道打开。由于所述非选中串的上选择管导通,使得所述非选中串的沟道与位线导通,沟道电势等于位线上的预充电压。沟道电势与位线电压保持一致,使得在对字线施加电压时不会产生耦合电压,可以避免热载流子注入串扰的问题。

[0032] 由于对位线施加预充电压,若选中串的下选择管和非选中串的下选择管为打开状态,会导致较大的漏电,因此在预导通阶段需要关断选中串的下选择管和非选中串的下选择管。并且,关断选中串的下选择管和非选中串的下选择管使得各存储串的沟道和位线依然相通,不会产生热载流子注入干扰。

[0033] 该具体实施方式中,在预导通阶段结束之前,先关断所述非选中串的上选择管,而对位线施加预充电压直至预导通阶段结束。这样,在非选中串的上选择管关断之前,非选中串的沟道电势一直等于位线上的预充电压;当非选中串的上选择管关断,而同时所述非选中串的下选择管也处于关断状态,所述非选中串沟道中的电势会保持为预充电压。在其他具体实施方式中,也可以在预导通阶段结束时,将位线电压由预充电压调整为驱动电压的同时,关断所述非选中串的上选择管。

[0034] 读取阶段中,对位线施加驱动电压,选中串的上选择管栅极和选中串的下选择管栅极均施加导通电压;非选中串的上选择管和下选择管的栅极均施加关断电压;非选中字线施加导通电压,而选中字线施加读取电压,对选中存储单元进行读取。在读取阶段中,非选择串的沟道电势为预充电电压,非选中串上的非选中行的存储单元受到由“导通电压-预充电电压”引起的读干扰,非选中串上的选中行上的非选中存储单元则受到“读取电压-预充电电压”引起的读干扰。由于所述预充电电压为高电压,因此该具体实施方式的读取方法能够有效减少非选择串上的存储单元的读干扰。

[0035] 而对于选中串,由于在读取阶段,选中串的上选择关和下选择管均打开,因此,选中串的沟道电势等于位线上的驱动电压,因此,选中串上的非选中存储单元受到由“导通电压-驱动电压”引起的读干扰。

[0036] 在一个具体实施方式中,所述预充电电压大于所述驱动电压,使得非选择串上的存储单元受到的读干扰小于选中串上的存储单元受到的读干扰,进而更大程度上减少读取错误。

[0037] 本发明的具体实施方式中,所述读取方法包括位于所述读取阶段之后的预关断阶段。在所述预关断阶段中,停止对连接选中串的位线施加电压,使得所述位线电压保持低电位。而对所述选中串的上选择管和下选择管、非选中串的上选择管和下选择管施加导通电压,使它们均被打开,同时对选中字线和非选中字线均施加导通电压,使得选中串和非选中串的沟道均导通至位线,共源端接地,将选中串和非选中串沟道内的电子均导出,将各存储单元沟道电势都拉低为0,以便于进行后续的读取或擦写操作。

[0038] 本发明的具体实施方式在对3D NAND闪存进行读取的过程中,在正式读取之前具有预导通阶段,在预导通阶段,对位线施加预充电电压,在读取阶段之前关断非选择串的上选择管和下选择管,使得在读取阶段非选中串的沟道电势等于预充电电压,从而降低非选中串受到的读干扰,进而减少在对3D NAND闪存进行读取过程中的读取错误。

[0039] 以上所述仅是本发明的优选实施方式,应当指出,对于本技术领域的普通技术人员,在不脱离本发明原理的前提下,还可以做出若干改进和润饰,这些改进和润饰也应视为本发明的保护范围。

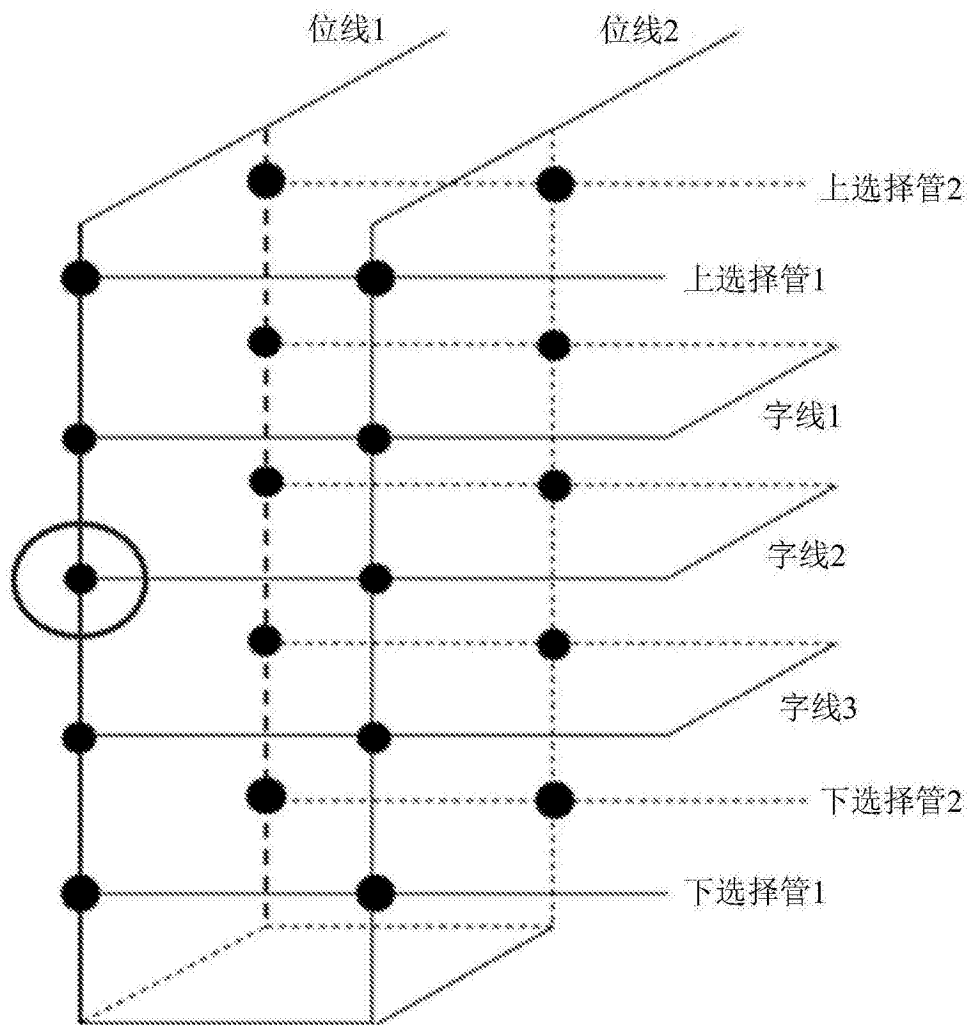


图1

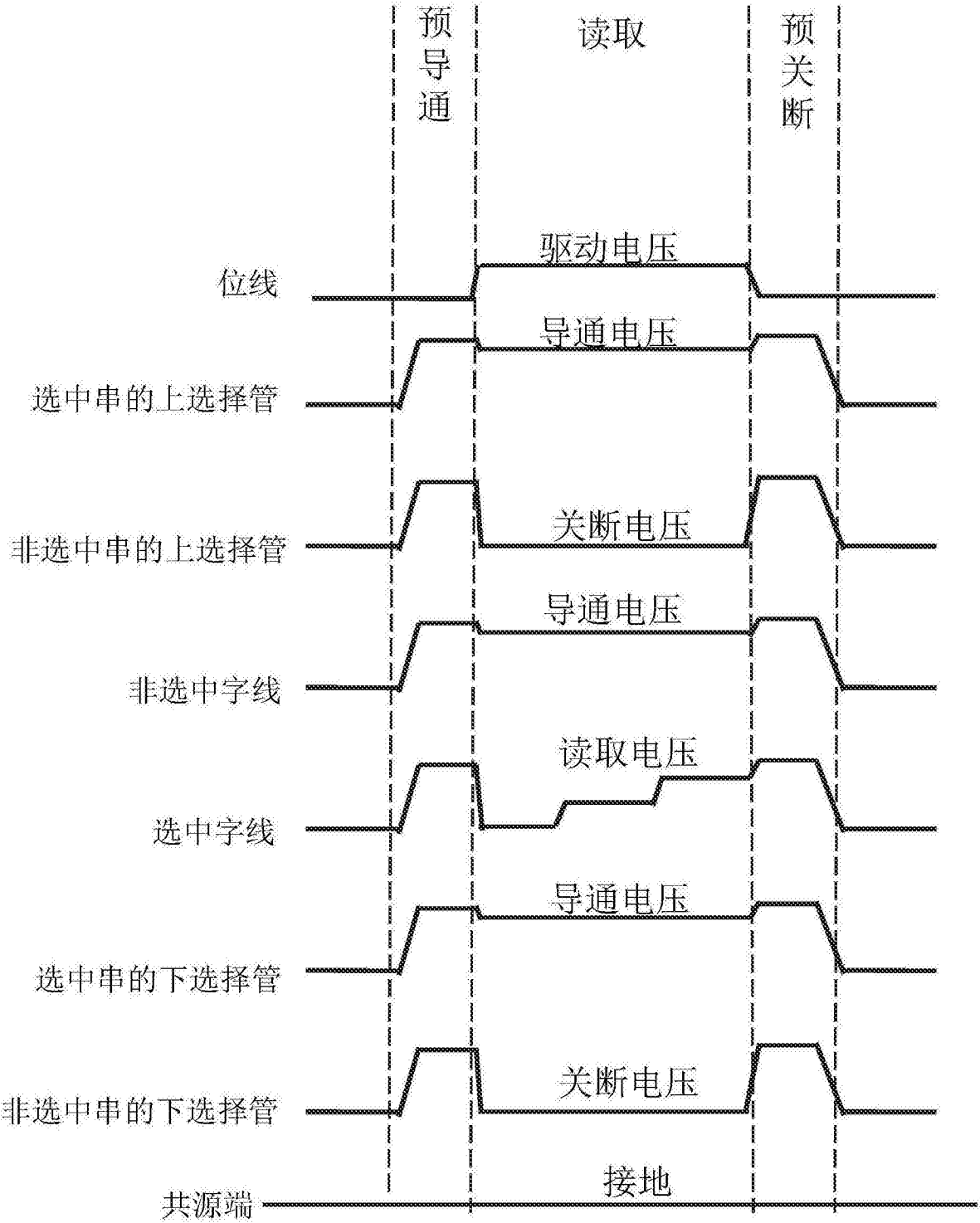


图2

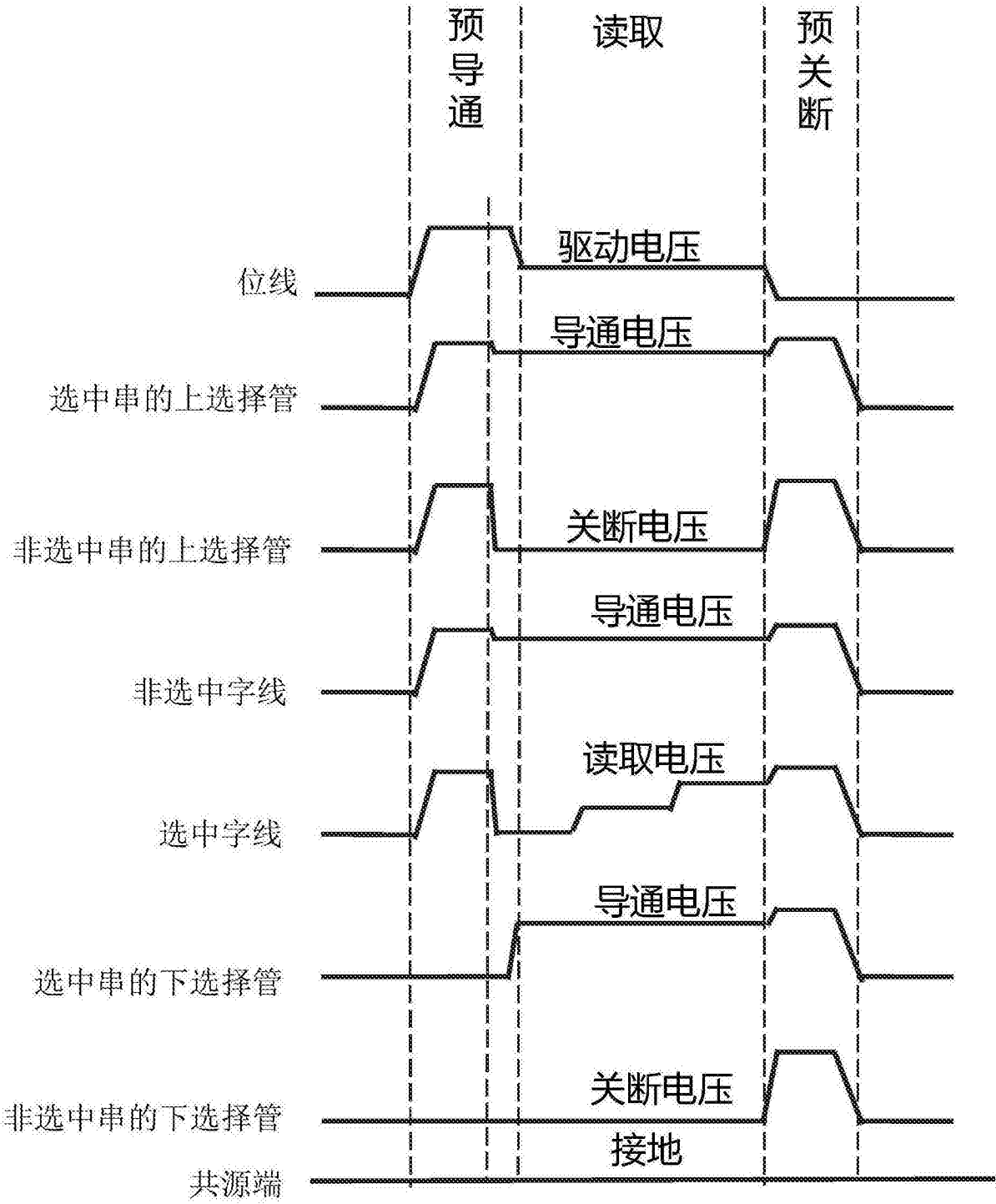


图3