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(54) **MEMORY DEVICE**

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(57) **ABSTRACT**

A memory device includes a memory cell array having a plurality of memory strings and includes a voltage generating circuit configured to generate and apply a plurality of drain select line voltages, a plurality of source select line voltages, and a read voltage to the memory cell array during a read operation. The memory device also includes control logic configured to control the voltage generating circuit to generate a first drain select line voltage applied to a first unselected memory string among unselected memory strings among the plurality of memory strings and a second drain select line voltage applied to second unselected memory strings among the unselected memory strings during the read operation, wherein the second drain select line voltage is different from the first drain select line voltage.

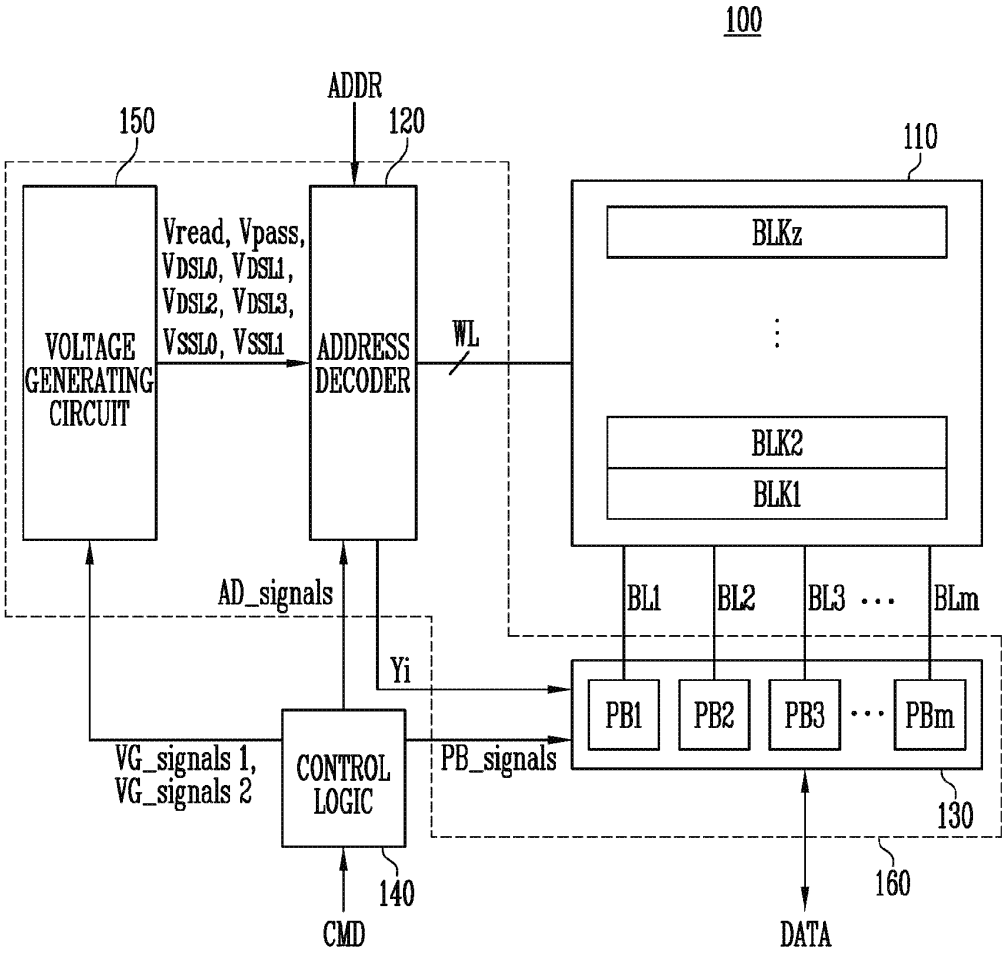


FIG. 1

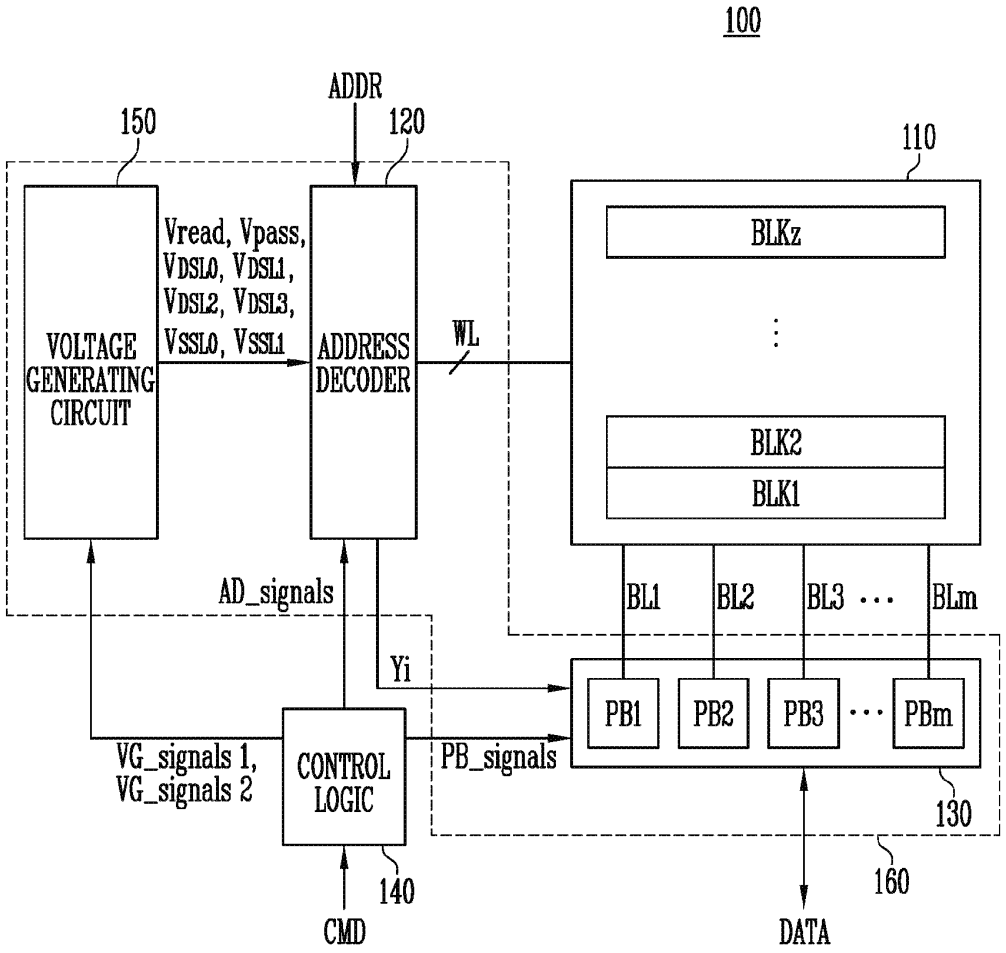

100
ADDR
150
120
110
VOLTAGE GENERATING CIRCUIT
Vread, Vpass, VDSL0, VDSL1, VDSL2, VDSL3, VSSL0, VSSL1
ADDRESS DECODER
WL
BLKz
BLK2
BLK1
AD_signals
BL1
BL2
BL3
BLm
Yi
PB1
PB2
PB3
PBm
VG_signals 1, VG_signals 2
CONTROL LOGIC
PB_signals
130
140
160
CMD
DATA

FIG. 2

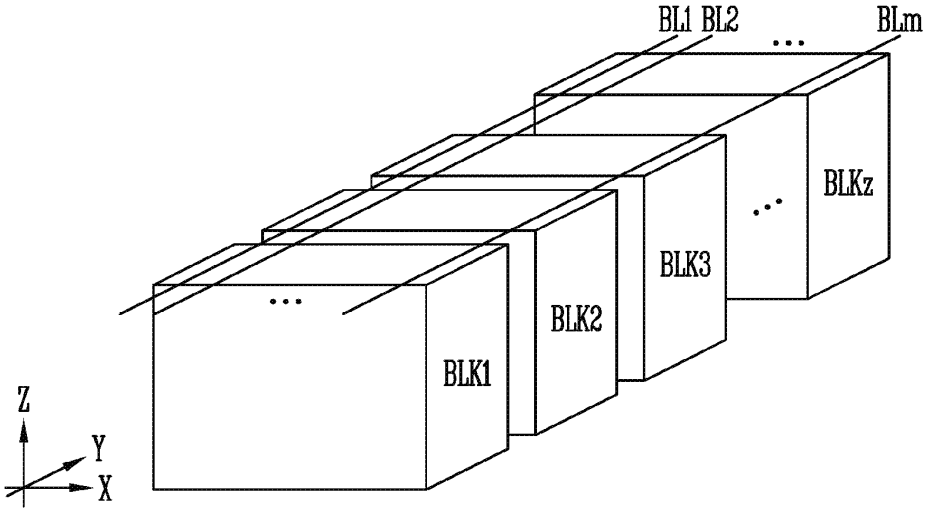


FIG. 3

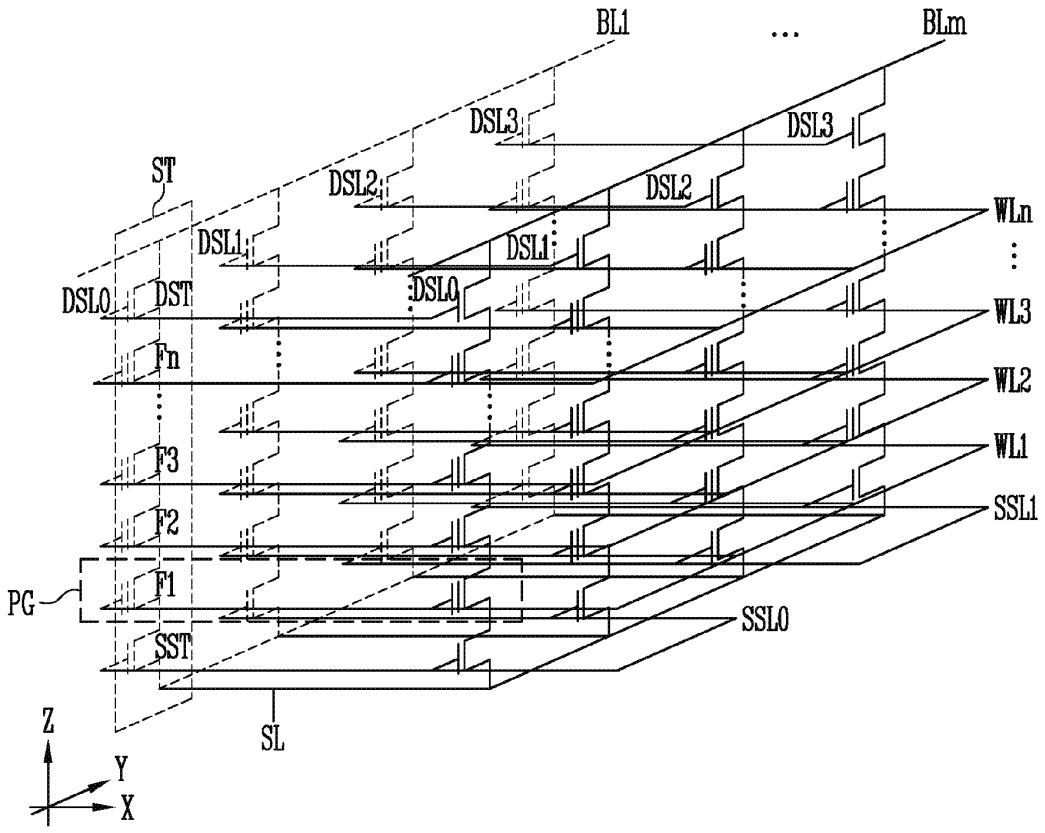

BL1
...
BLm
DSL3
DSL3
ST
DSL2
DSL2
WLn
DSL1
DSL1
DSL0
DSL0
DST
WL3
Fn
WL2
WL1
F3
SSL1
F2
PG
F1
SSL0
SST
SL
Z
Y
X

FIG. 4

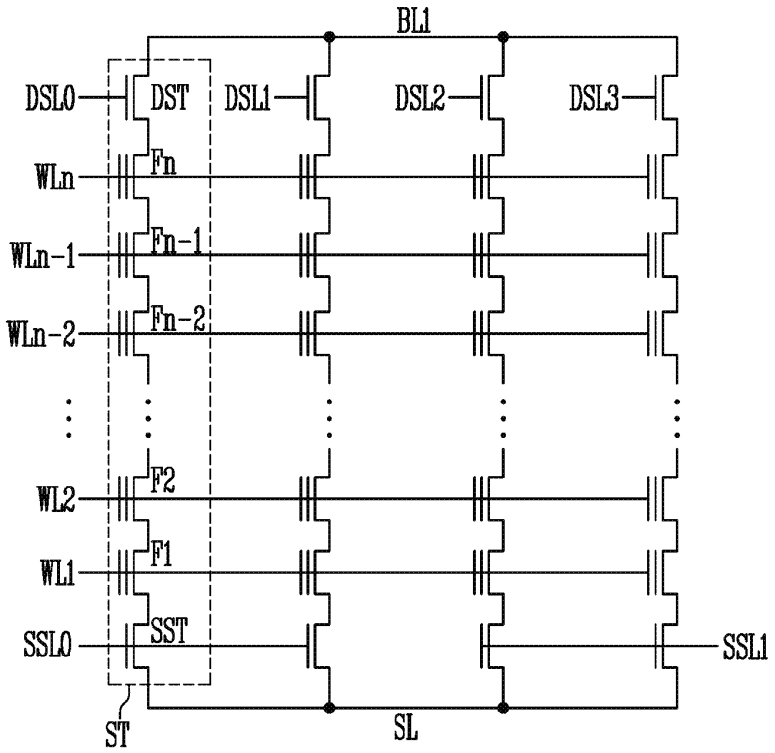

BL1
DSL0
DST
DSL1
DSL2
DSL3
WLn
Fn
WLn-1
Fn-1
WLn-2
Fn-2
WL2
F2
WL1
F1
SSL0
SST
SSL1
ST
SL

FIG. 5

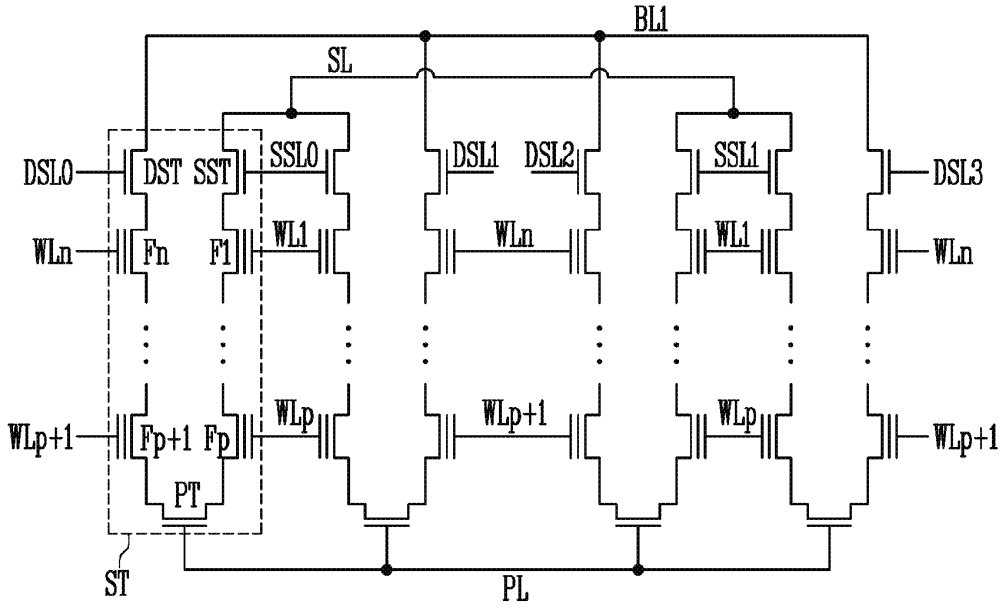

BL1
SL
DSL0
DST
SST
SSL0
DSL1
DSL2
SSL1
DSL3
WLn
Fn
F1
WL1
WLn
WL1
WLn
WLp+1
Fp+1
Fp
WLp
WLp+1
WLp
WLp+1
PT
ST
PL

FIG. 6

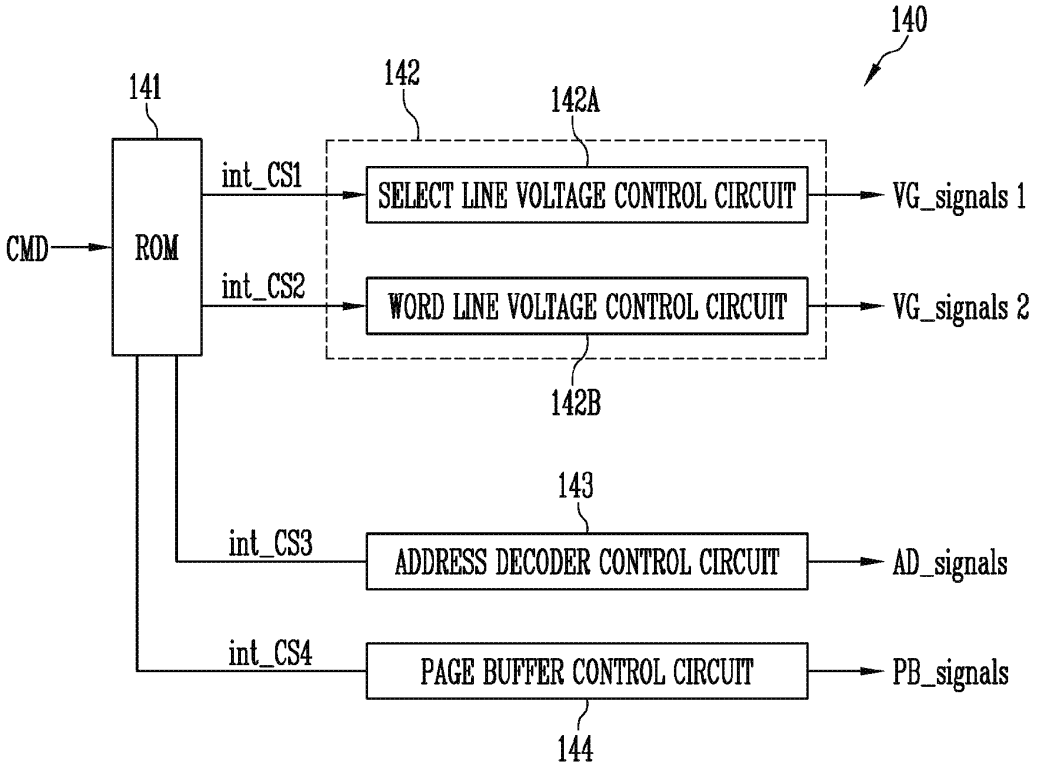

140
141
142
142A
CMD
ROM
int_CS1
int_CS2
SELECT LINE VOLTAGE CONTROL CIRCUIT
WORD LINE VOLTAGE CONTROL CIRCUIT
VG_signals 1
VG_signals 2
142B
143
int_CS3
ADDRESS DECODER CONTROL CIRCUIT
AD_signals
int_CS4
PAGE BUFFER CONTROL CIRCUIT
PB_signals
144

FIG. 7

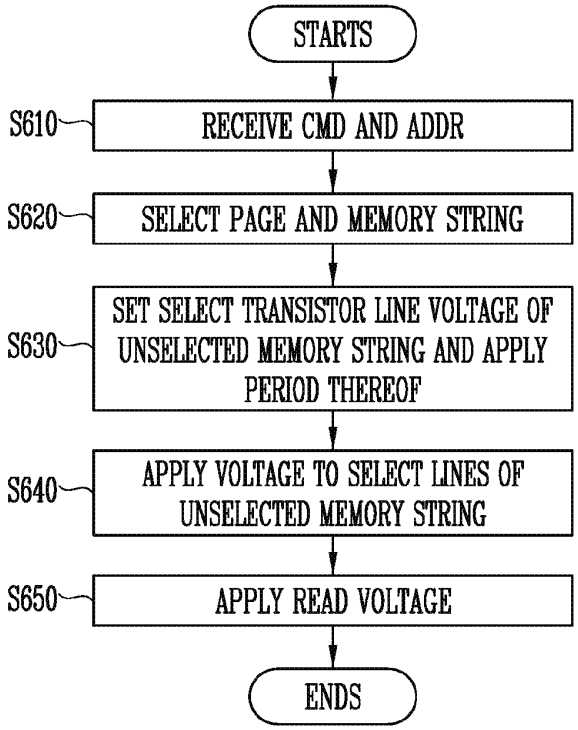

STARTS
S610
RECEIVE CMD AND ADDR
S620
SELECT PAGE AND MEMORY STRING
S630
SET SELECT TRANSISTOR LINE VOLTAGE OF UNSELECTED MEMORY STRING AND APPLY PERIOD THEREOF
S640
APPLY VOLTAGE TO SELECT LINES OF UNSELECTED MEMORY STRING
S650
APPLY READ VOLTAGE
ENDS

FIG. 8

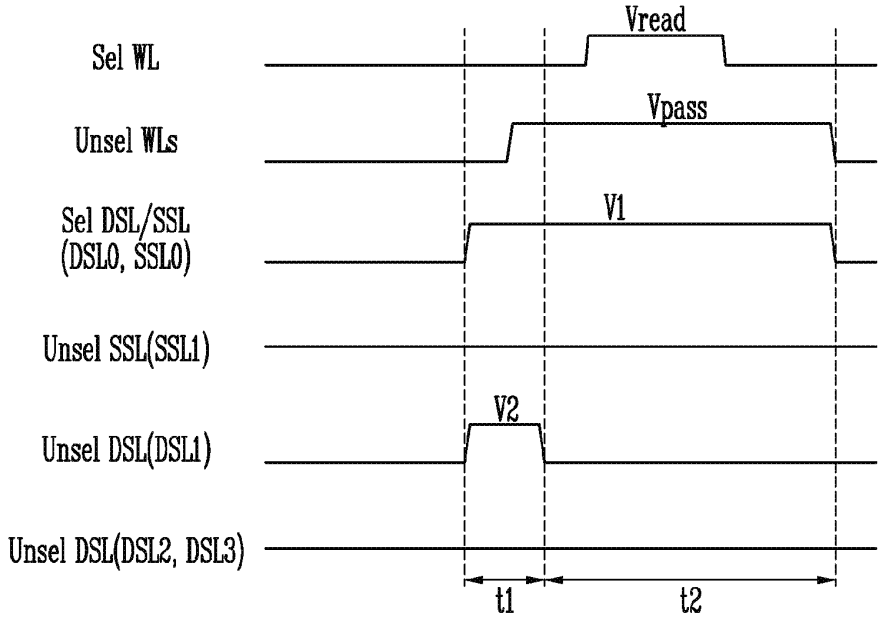

Vread
Sel WL
Vpass
Unsel WLs
V1
Sel DSL/SSL
(DSL0, SSL0)
Unsel SSL(SSL1)
V2
Unsel DSL(DSL1)
Unsel DSL(DSL2, DSL3)
t1
t2

FIG. 9

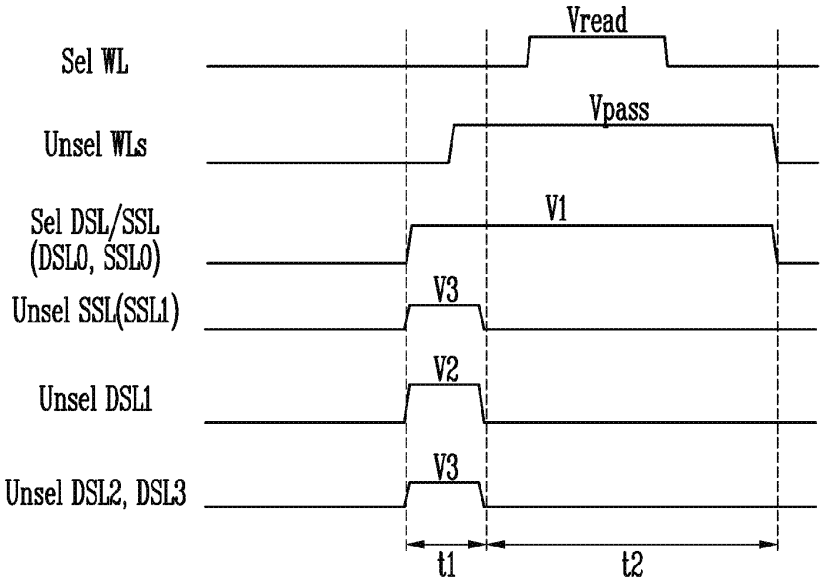

Vread
Sel WL
Vpass
Unsel WLs
V1
Sel DSL/SSL
(DSL0, SSL0)
V3
Unsel SSL(SSL1)
V2
Unsel DSL1
V3
Unsel DSL2, DSL3
t1
t2

FIG. 10

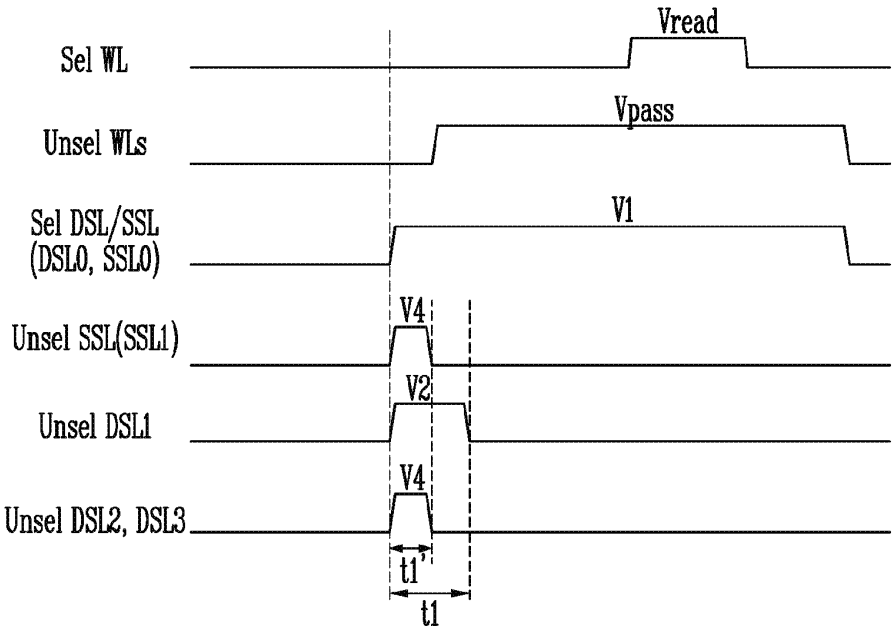

Vread
Sel WL
Vpass
Unsel WLs
V1
Sel DSL/SSL
(DSL0, SSL0)
V4
Unsel SSL(SSL1)
V2
Unsel DSL1
V4
Unsel DSL2, DSL3
t1'
t1

FIG. 11

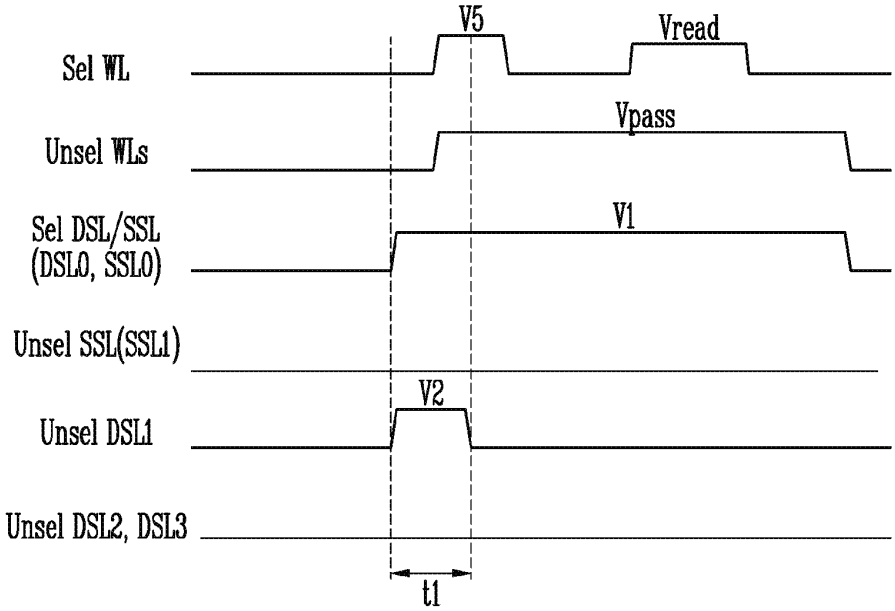

V5
Vread
Sel WL
Vpass
Unsel WLs
V1
Sel DSL/SSL
(DSL0, SSL0)
Unsel SSL(SSL1)
V2
Unsel DSL1
Unsel DSL2, DSL3
t1

FIG. 12

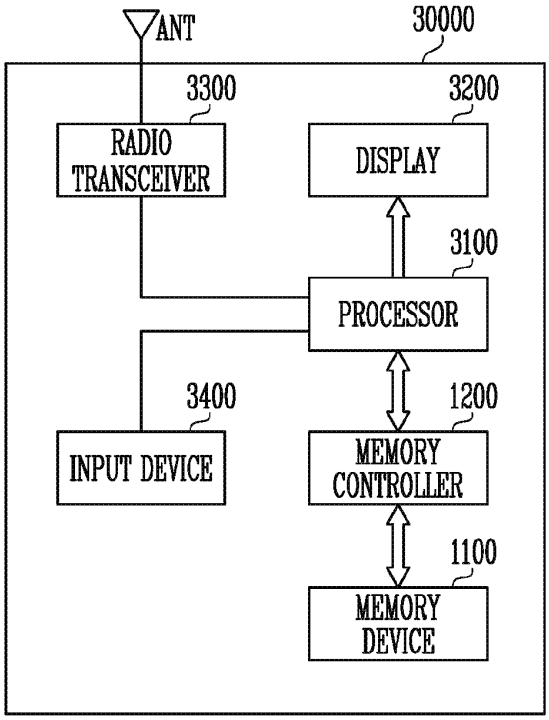

ANT
30000
3300
RADIO TRANSCEIVER
3200
DISPLAY
3100
PROCESSOR
3400
INPUT DEVICE
1200
MEMORY CONTROLLER
1100
MEMORY DEVICE

FIG. 13

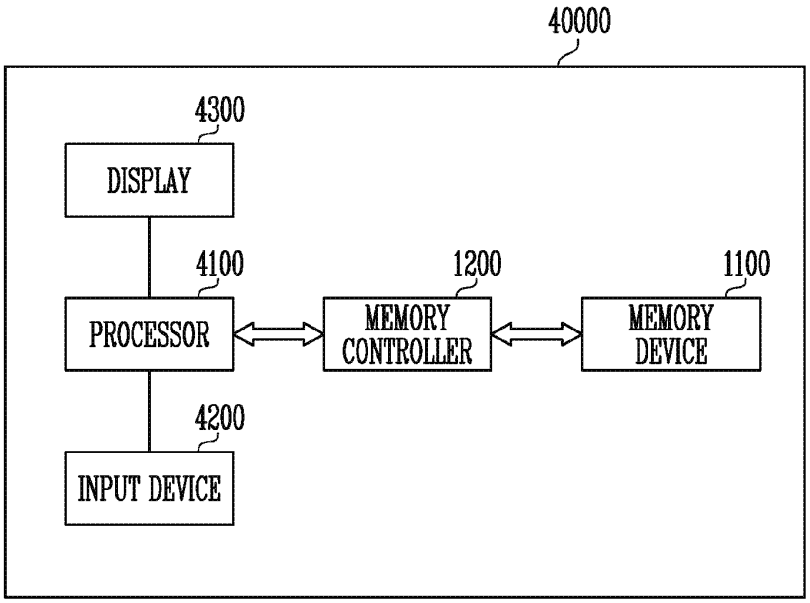

40000
4300
DISPLAY
4100
PROCESSOR
1200
MEMORY CONTROLLER
1100
MEMORY DEVICE
4200
INPUT DEVICE

FIG. 14

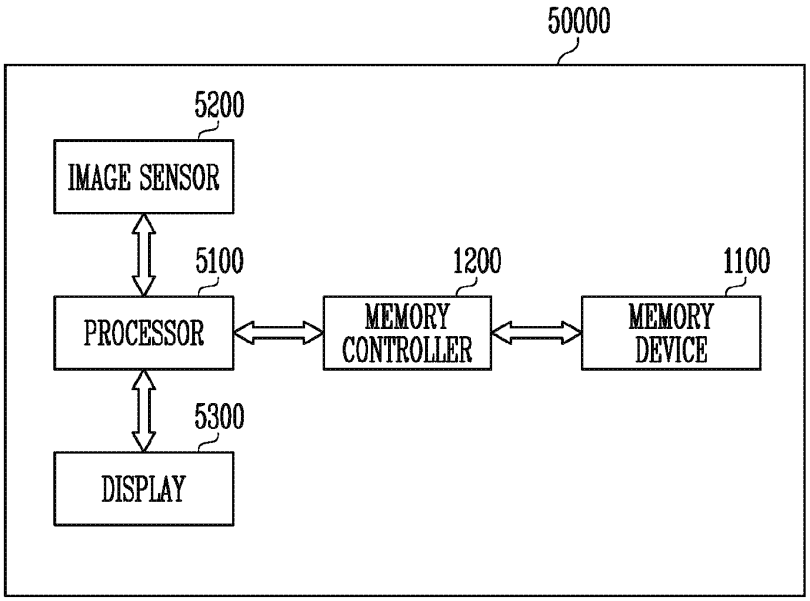
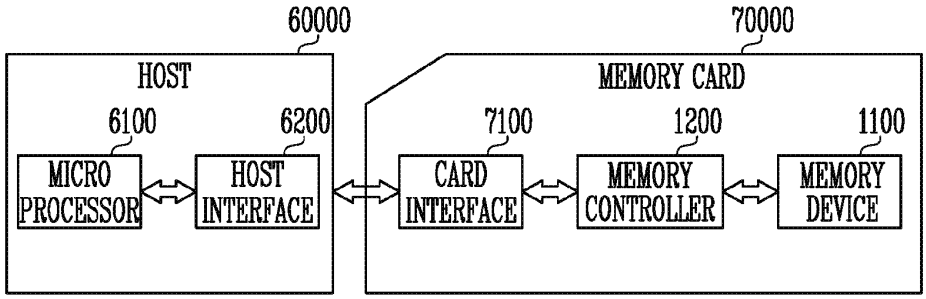

50000
5200
IMAGE SENSOR
5100
PROCESSOR
1200
MEMORY CONTROLLER
1100
MEMORY DEVICE
5300
DISPLAY

FIG. 15


60000
70000
HOST
MEMORY CARD
6100
6200
7100
1200
1100
MICRO PROCESSOR
HOST INTERFACE
CARD INTERFACE
MEMORY CONTROLLER
MEMORY DEVICE

MEMORY DEVICE

CROSS-REFERENCE TO RELATED APPLICATION

[0001] The present application claims priority under 35 U.S.C. § 119(a) to Korean patent application number 10-2019-0089123, filed on Jul. 23, 2019, in the Korean Intellectual Property Office, the entire disclosure of which is incorporated herein by reference.

BACKGROUND

1. Technical Field

[0002] Various embodiments generally relate to an electronic device, and more particularly, to a memory device.

2. Related Art

[0003] Semiconductor devices, in particular, memory devices, may be classified into volatile memory devices and nonvolatile memory devices.

[0004] A nonvolatile memory device may have comparatively low write and read speeds, but may retain stored data in the absence of supplied power. Therefore, the nonvolatile memory device may be used when there is the need for storing data which should be retained regardless of a supply of power. Examples of nonvolatile memory devices include Read Only Memory (ROM), Mask ROM (MROM), Programmable ROM (PROM), Erasable Programmable ROM (EPROM), Electrically Erasable Programmable ROM (EEPROM), flash memory, Phase-change Random Access Memory (PRAM), Magnetic RAM (MRAM), Resistive RAM (RRAM), and Ferroelectric RAM (FRAM). Flash memory may be classified into NOR-type memory and NAND-type memory.

[0005] Among these nonvolatile memory devices, flash memory may have both advantages of RAM, in which data is freely programmable and erasable, and advantages of ROM, in which data stored therein can be retained even without power. Flash memory has been widely used as storage media for portable electronic devices such as digital cameras, Personal Digital Assistants (PDAs), and MP3 players.

[0006] Flash memory devices may be classified into two-dimensional semiconductor devices, in which memory strings are horizontally formed on a semiconductor substrate, and three-dimensional semiconductor devices, in which memory strings are vertically formed on a semiconductor substrate.

[0007] Three-dimensional semiconductor devices are designed to overcome integration limits of two-dimensional semiconductor devices and include a plurality of memory strings vertically formed on a semiconductor substrate. Each of the memory strings may include a drain select transistor, memory cells, and a source select transistor coupled in series between a bit line and a source line.

SUMMARY

[0008] Various embodiments are directed to a memory device capable of improving a disturb phenomenon of an unselected memory string during a read operation.

[0009] According to an embodiment, a memory device may include a memory cell array having a plurality of memory strings and includes a voltage generating circuit configured to generate and apply a plurality of drain select line voltages, a plurality of source select line voltages, and a read voltage to the memory cell array during a read operation. The memory device also includes control logic configured to control the voltage generating circuit to generate a first drain select line voltage applied to a first unselected memory string among unselected memory strings among the plurality of memory strings and a second drain select line voltage applied to second unselected memory strings among the unselected memory strings during the read operation, wherein the second drain select line voltage is different from the first drain select line voltage.

[0010] According to an embodiment, a memory device may include a memory cell array having a plurality of memory strings and include a voltage generating circuit configured to generate and apply a plurality of drain select line voltages, a plurality of source select line voltages, and a read voltage to the memory cell array during a read operation. The memory device may also include a control logic configured to control the voltage generating circuit to apply, during the read operation, a first drain select line voltage applied to a first unselected memory string among unselected memory strings among the plurality of memory strings at a first potential level and a second drain select line voltage applied to second unselected memory strings among the unselected memory strings at a second potential level lower than the first potential level.

[0011] According to an embodiment, a memory device may include a memory cell array having a plurality of memory strings and include a voltage generating circuit configured to generate and apply a plurality of drain select line voltages, a plurality of source select line voltages, and a read voltage to the memory cell array during a read operation. The memory device may also include control logic configured to control the voltage generating circuit to apply, during the read operation, a first drain select line voltage applied to a first unselected memory string among unselected memory strings among the plurality of memory strings during a first period and a second drain select line voltage applied to second unselected memory strings among the unselected memory strings during a second time period shorter than the first time period.

BRIEF DESCRIPTION OF THE DRAWINGS

[0012] FIG. **1** is a block diagram illustrating a memory device according to an embodiment.

[0013] FIG. **2** is a diagram illustrating three-dimensionally structured memory blocks.

[0014] FIG. **3** is a circuit diagram illustrating one of the memory blocks shown in FIG. **2** in detail.

[0015] FIG. **4** is a circuit diagram illustrating memory strings shown in FIG. **3**.

[0016] FIG. **5** is a circuit diagram illustrating memory strings according to another embodiment.

[0017] FIG. **6** is a diagram illustrating control logic of FIG. **1**.

[0018] FIG. **7** is a flowchart illustrating a read operation of a memory device according to an embodiment.

[0019] FIG. **8** is a waveform diagram of signals illustrating a method of performing a read operation of a memory device according to a first embodiment.

[0020] FIG. **9** is a waveform diagram of signals illustrating a method of performing a read operation of a memory device according to a second embodiment.

[0021] FIG. **10** is a waveform diagram of signals illustrating a method of performing a read operation of a memory device according to a third embodiment.

[0022] FIG. **11** is a waveform diagram of signals illustrating a method of performing a read operation of a memory device according to a fourth embodiment.

[0023] FIG. **12** is a diagram illustrating a memory system including the memory device of FIG. **1**.

[0024] FIG. **13** is a diagram illustrating another embodiment of a memory system.

[0025] FIG. **14** is a diagram illustrating another embodiment of a memory system.

[0026] FIG. **15** is a diagram illustrating another embodiment of a memory system.

DETAILED DESCRIPTION

[0027] Hereinafter, specific structural or functional descriptions of examples of embodiments in accordance with concepts which are disclosed in this specification are illustrated only to describe the examples of embodiments in accordance with the concepts and the examples of embodiments in accordance with the concepts may be carried out by various forms but the descriptions are not limited to the examples of embodiments described in this specification.

[0028] Various modifications and changes may be applied to the examples of embodiments in accordance with the concepts so that the examples of embodiments will be illustrated in the drawings and described in the specification. However, the embodiments according to the concept of the present disclosure are not construed as limited to specified disclosures, and include all changes, equivalents, or substitutes that do not depart from the spirit and technical scope of the present disclosure.

[0029] While terms such as "first" and "second" may be used to describe various components, such components should not be understood as being limited to the above terms. The above terminologies are used to distinguish one component from the other component, for example, a first component may be referred to as a second component without departing from a scope in accordance with the concept of the present disclosure and similarly, a second component may be referred to as a first component.

[0030] It will be understood that when an element is referred to as being "connected" or "coupled" to another element, it can be directly connected or coupled to the other element or intervening elements may also be present. In contrast, when an element is referred to as being "directly connected" or "directly coupled" to another element, no intervening elements are present. Meanwhile, other expressions describing relationships between components such as "~ between," "immediately ~ between" or "adjacent to ~" and "directly adjacent to ~" may be construed similarly.

[0031] The terms used in the present application are merely used to describe particular embodiments, and are not intended to limit the present disclosure. Singular forms in the present disclosure are intended to include plural forms as well, unless the context clearly indicates otherwise. In the present specification, it should be understood that terms "include" or "have" indicate that a feature, a number, a step, an operation, a component, a part or the combination those of described in the specification is present, but do not exclude a possibility of presence or addition of one or more other features, numbers, steps, operations, components, parts or combinations thereof, in advance.

[0032] So far as not being differently defined, all terms used herein including technical or scientific terminologies have meanings that they are commonly understood by those skilled in the art to which the present disclosure pertains. The terms defined in generally used dictionaries should be construed as having the same meanings as would be construed in the context of the related art, and unless clearly defined otherwise in this specification, should not be construed as having idealistic or overly formal meanings.

[0033] In some embodiments, well-known processes, device structures, and technologies will not be described in detail to avoid ambiguousness of the present teachings. This intends to disclose the gist of the present disclosure more clearly by omitting unnecessary description.

[0034] Hereinafter, embodiments will be described in detail with reference to the accompanying drawings in order for those skilled in the art to be able to readily implement the technical spirit of the present disclosure.

[0035] FIG. **1** is a block diagram illustrating a memory device **100** according to an embodiment.

[0036] Referring to FIG. **1**, the memory device **100** may include a memory cell array **110**, an address decoder **120**, a read and write circuit **130**, control logic **140**, and a voltage generating circuit **150**. The address decoder **120**, the read and write circuit **130**, and the voltage generating circuit **150** may be defined as a peripheral circuit **160** configured to perform a read operation on the memory cell array **110**.

[0037] The memory cell array **110** may include a plurality of memory blocks BLK**1** to BLKz. The plurality of memory blocks BLK**1** to BLKz may be coupled to the address decoder **120** through word lines WLs. The plurality of memory blocks BLK**1** to BLKz may be coupled to the read and write circuit **130** through bit lines BL**1** to BLm. Each of the plurality of memory blocks BLK**1** to BLKz may include a plurality of memory cells. According to an embodiment, the plurality of memory cells may be nonvolatile memory cells. Memory cells coupled to the same word line among the plurality of memory cells may be defined as one page. In other words, the memory cell array **110** may include a plurality of pages.

[0038] Each of the plurality of memory blocks BLK**1** to BLKz of the memory cell array **110** may include a plurality of memory strings. Each of the plurality of memory strings may include a drain select transistor, a plurality of memory cells, and a source select transistor coupled in series between a bit line and a source line. In addition, each of the plurality of memory strings may include pass transistors between a source select transistor and memory cells and between a drain select transistor and memory cells, respectively, and may further include a pipe gate transistor between memory cells. The memory cell array **110** will be described in detail below.

[0039] The address decoder **120** may be coupled to the memory cell array **110** through the word lines WLs. The address decoder **120** may be configured to operate in response to address decoder control signals AD_signals generated in the control logic **140**. The address decoder **120** may receive an address ADDR through an input/output buffer (not illustrated) in the memory device **100**.

[0040] The address decoder **120** may decode a row address among the received address ADDR and apply a plurality of operating voltages including a read voltage Vread, a pass voltage Vpass, a plurality of drain select line voltages V_{DSL0}, V_{DSL1}, V_{DSL2}, and V_{DSL3}, and a plurality of

source select line voltages V_{SSL0} and V_{SSL1} generated in the voltage generating circuit **150** to the plurality of memory cells, the drain select transistors, and the source select transistors of the memory cell array **110** according to the decoded row address during the read operation.

[0041] The address decoder **120** may be configured to decode a column address among the received address ADDR during the read operation. The address decoder **120** may transfer the decoded column address Yi to the read and write circuit **130**.

[0042] The address ADDR received during the read operation may include a block address, a row address, and a column address. The address decoder **120** may select one memory block and one word line according to the block address and the row address. The column address may be decoded by the address decoder **120** and provided to the read and write circuit **130**.

[0043] The address decoder **120** may include a block decoder, a row decoder, a column decoder, and an address buffer.

[0044] The read and write circuit **130** may include a plurality of page buffers PB**1** to PBm. The plurality of page buffers PB**1** to PBm may be coupled to the memory cell array **110** through the bit lines BL**1** to BLm. Each of the plurality of page buffers PB**1** to PBm may perform a read operation by precharging the bit lines BL**1** to BLm to a set level during a precharge operation of the read operation and by sensing a potential level or an amount of current of the bit lines BL**1** to BLm during a read voltage apply operation.

[0045] The read and write circuit **130** may operate in response to page buffer control signals PB_signals output from the control logic **140**.

[0046] According to an embodiment, the read and write circuit **130** may include page buffers (or page registers), a column select circuit, or the like.

[0047] The control logic **140** may be implemented as hardware, software, or a combination of hardware and software. For example, the control logic **140** may be a control logic circuit operating in accordance with an algorithm and/or a processor executing control logic code. The control logic **140** may be coupled to the address decoder **120**, the read and write circuit **130**, and the voltage generating circuit **150**. The control logic **140** may receive a command CMD through the input/output buffer (not illustrated) of the memory device **100**. The control logic **140** may be configured to control the general operations of the memory device **100** in response to the command CMD. For example, the control logic **140** may receive the command CMD corresponding to the read operation, generate and output the address decoder control signals AD_signals to control the address decoder **120**, the page buffer control signals PB_signals to control the read and write circuit **130**, and voltage generating circuit control signals VG_signals **1** and VG_signals **2** to control the voltage generating circuit **150** in response to the received command CMD.

[0048] The control logic **140** according to an embodiment may control a voltage applied to a drain select transistor of an unselected memory string which shares a source select line with a selected memory string and a voltage applied to a drain select transistor of an unselected memory string which does not share a source select line with a selected memory string such that these voltages are different from each other during the read operation. Accordingly, a disturb phenomenon caused by Hot Carrier Injection (HCI) during a read operation may be prevented by adjusting a channel potential level of unselected memory strings.

[0049] The voltage generating circuit **150** may generate and output the read voltage Vread, the pass voltage Vpass, the plurality of drain select line voltages V_{DSL0}, V_{DSL1}, V_{DSL2}, and V_{DSL3}, and the plurality of source select line voltages V_{SSL0} and V_{SSL1} to the address decoder **120** in response to the control of the voltage generating circuit control signals VG_signals **1** and VG_signals **2** output from the control logic **140** during the read operation.

[0050] FIG. **2** is a diagram illustrating three-dimensionally structured memory blocks.

[0051] Referring to FIG. **2**, the three-dimensionally structured memory blocks BLK**1** to BLKz may be arranged to be spaced apart from each other in a direction Y in which the bit lines BL**1** to BLm extend. For example, the first to z memory blocks BLK**1** to BLKz may be arranged to be spaced apart from each other in the second direction Y and may include a plurality of memory cells stacked in a third direction Z. The configuration of one of the first to z memory blocks BLK**1** to BLKz will be described later in detail with reference to FIGS. **3**, **4**, and **5**.

[0052] FIG. **3** is a circuit diagram illustrating one of the memory blocks shown in FIG. **2** in detail.

[0053] FIG. **4** is a circuit diagram illustrating the memory strings shown in FIG. **3**.

[0054] Referring to FIGS. **3** and **4**, respective memory strings ST may be coupled between the bit lines BL**1** to BLm and a source line SL. The memory string ST coupled between the first bit line BL**1** and the source line SL will be described below as an example.

[0055] The memory string ST may include a source select transistor SST, memory cells F**1** to Fn, and a drain select transistor DST coupled in series between the source line SL and the first bit line BL**1**, where n is a positive integer. Gates of the source select transistors SST included in different memory strings ST coupled to different bit lines BL**1** to BLm may be coupled to a first source select line SSL**0** and a second source select line SSL**1**. For example, source select transistors adjacent to each other in the second direction Y among the source select transistors SST may be coupled to the same source select line. For example, on the assumption that the source select transistors SST are sequentially arranged, gates of the source select transistors SST arranged in a first direction X from the first source select transistor SST and included in different strings ST and gates of the source select transistors SST arranged in the first direction X from the second source select transistor SST and included in different strings ST may be coupled to the first source select line SSL**0**. In addition, gates of the source select transistors SST arranged in the first direction X from the third source select transistor SST and included in different strings ST and gates of the source select transistors SST arranged in the first direction X from the fourth source select transistor SST and included in different strings ST may be coupled to the second source select line SSL**1**.

[0056] Gates of the memory cells F**1** to Fn may be coupled to word lines WL**1** to WLn and gates of the drain select transistors DST may be coupled to one of first, second, third, and fourth drain select lines DSL**0**, DSL**1**, DSL**2**, and DSL**3**.

[0057] Gates of transistors arranged in the first direction X among the drain select transistors DST may be coupled to the same drain select line (for example, DSL**0**) in common, but gates of transistors arranged in the second direction Y

among the drain select transistors DST may be coupled to the different drain select lines DSL**1**, DSL**2**, and DSL**3**. For example, on the assumption that the drain select transistors DST are sequentially arranged in the second direction Y, gates of the drain select transistors DST arranged in the first direction X from the first drain select transistor DST and included in different strings ST may be coupled to the first drain select line DSL**0**. The drain select transistors DST arranged in the second direction Y from the drain select transistors DST coupled to the first drain select line DSL**0** may be sequentially coupled to the second, third, and fourth drain select lines DSL**1**, DSL**2**, and DSL**3**. Accordingly, the memory strings ST coupled to a selected drain select line may be selected and the memory strings ST coupled to remaining unselected drain select lines might not be selected in the selected memory block.

[0058] Memory cells coupled to the same word line may form a page PG. The page PG may refer to a physical page. For example, a group of memory cells coupled to the same word line in the first direction X among the strings ST coupled to the first bit line BL**1** to the mth bit line BLm may refer to the page PG. For example, memory cells arranged in the first direction X among the first memory cells F**1** coupled to the first word line WL**1** may form one page PG. Memory cells arranged in the second direction Y among the first memory cells F**1** coupled to the first word line WL**1** in common may define different pages. Accordingly, when the first drain select line DSL**0** is a selected drain select line and the first word line WL**1** is a selected word line, a page coupled to the first drain select line DSL**0** among the plurality of pages PG coupled to the first word line WL**1** may be a selected page. Pages coupled to the first word line WL**1** in common, but coupled to the unselected second, third, and fourth drain select lines DSL**1**, DSL**2**, and DSL**3** may be unselected pages.

[0059] In FIGS. **3** and **4**, it is illustrated that one source select transistor SST and one drain select transistor DST are included in one string ST. However, a plurality of source select transistors SST and the plurality of drain select transistors DST may be included in one string ST depending on a memory device. In addition, dummy cells may be further included between the source select transistor SST, the memory cells F**1** to Fn, and the drain select transistor DST depending on a memory device. Dummy cells might not store user data unlike general memory cells F**1** to Fn but may be used to improve electrical characteristics of each string ST.

[0060] FIG. **5** is a circuit diagram illustrating memory strings according to another embodiment.

[0061] Referring to FIG. **5**, a plurality of memory strings ST may be coupled between one bit line (for example, BL**1**) and the source line SL, and each of the memory strings ST may have a 'U' shape.

[0062] Each of the plurality of memory strings ST may include at least one source select transistor SST, first to nth memory cells F**1** to Fn, a pipe transistor PT, and at least one drain select transistor DST. The pipe transistor PT may be coupled between the pth memory cell Fp and the (p+1)th memory cell Fp+1 and a gate of the pipe transistor PT may be coupled to a pipe line PL. The first to pth memory cells F**1** to Fp and the (p+1)th to nth memory cells Fp+1 to Fn may be coupled to each other through the pipe transistor PT.

[0063] The structure of the memory strings illustrated in FIG. **5** corresponds to the structure of the memory strings illustrated in FIG. **4** to which the pipe transistor PT is further included.

[0064] FIG. **6** is a diagram illustrating the control logic **140** of FIG. **1**.

[0065] Referring to FIG. **6**, the control logic **140** may include ROM **141**, a voltage generation control circuit **142**, an address decoder control circuit **143**, and a page buffer control circuit **144**.

[0066] The ROM **141** may store an algorithm to perform general operations of a memory device and generate a plurality of internal control signals int_CS**1**, int_CS**2**, int_CS**3**, and int_CS**4** in response to the command CMD input from an external device, for example, a host coupled to the memory device.

[0067] The voltage generation control circuit **142** may include a select line voltage control circuit **142**A and a word line voltage control circuit **142**B. The select line voltage control circuit **142**A may generate the first voltage generating circuit control signals VG_signals **1** to control the voltage generating circuit **150** shown in FIG. **1** to generate the select line voltages V_{DSL0}, V_{DSL1}, V_{DSL2}, V_{DSL3}, V_{SSL0}, and V_{SSL1} applied to a selected memory block during a read operation of the memory device in response to the internal control signal int_CS**1**. The word line voltage control circuit **142**B may generate the second voltage generating circuit control signals VG_signals **2** to control the voltage generating circuit **150** shown in FIG. **1** to generate the read voltage Vread and the pass voltage Vpass applied to a selected memory block during the read operation of the memory device in response to the internal control signal int_CS**2**.

[0068] The address decoder control circuit **143** may output the address decoder control signals AD_signals to control the address decoder **120** of FIG. **1** during the general operations of the memory device in response to the internal control signal int_CS**3**.

[0069] The page buffer control circuit **144** may output the page buffer control signals PB_signals to control the read and write circuit **130** of FIG. **1** during the general operations of the memory device in response to the internal control signal int_CS**4**.

[0070] FIG. **7** is a flowchart illustrating a read operation of a memory device according to an embodiment.

[0071] A read operation of a memory device according to an embodiment is described below with reference to FIGS. **1** to **7**.

[0072] The memory device **100** may receive (S**610**), from an external device, the command CMD corresponding to the read operation and the address ADDR corresponding to the memory cells to be read.

[0073] The memory device **100** may select (S**620**) one of the plurality of memory blocks **110**, e.g., BLK**1** to BLKz, included in the memory cell array **110** in response to the received command CMD and address ADDR, and select a page and memory strings to perform the read operation of the selected memory block (for example, BLK**1**).

[0074] According to an embodiment, for convenience of explanation, a case will be described where the memory strings ST coupled to the first drain select line DSL**0** among each of the bit lines BL**1** to BLm shown in FIG. **3** are selected and the page PG corresponding to the word line WL**3** among the plurality of pages PG is selected.

[0075] The memory device **100** may set (S**630**) the plurality of drain select line voltages V_{DSL1}, V_{DSL2}, and V_{DSL3} applied to the unselected memory strings during the read operation and set a time period during which the voltages are applied. The memory device may set the drain select line voltage (for example, V_{DSL1}) of the unselected memory string which shares the source select line with the selected memory string among the plurality of unselected memory strings to be different from the drain select line voltages (for example, V_{DSL2} and V_{DSL3}) of the remaining unselected memory strings. For example, the drain select line voltage (for example, V_{DSL1}) of the unselected memory string which shares the source select line with the selected memory string may be set to a voltage to turn on the drain select transistor DST, that is, a turn-on voltage. The drain select line voltages (for example, V_{DSL2} and V_{DSL3}) of the remaining unselected memory strings may be set to a ground voltage Vss or a voltage lower than a threshold voltage of the drain select transistor DST. In addition, the drain select line voltages (for example, V_{DSL2} and V_{DSL3}) of the remaining unselected memory strings may be set to the turn-on voltage such that the turn-on voltage is applied during a first time period, and the drain select line voltage (for example, V_{DSL1}) of the unselected memory string may be set to the turn-on voltage such that the turn-on voltage is applied during a second time period longer than the first time period. The drain select line voltage applied to the unselected memory string which shares the source select line with the selected memory string and the drain select line voltages applied to the remaining unselected memory strings will be described in detail below with reference to FIGS. **8** to **11**.

[0076] Information regarding a potential level of the turn-on voltage applied to the drain select line of the unselected memory strings described above and a time period during which the turn-on voltage is applied may be stored in the ROM **141** of the control logic **140**.

[0077] The control logic **140** may control the peripheral circuit **160** to perform a read operation in response to the received command CMD.

[0078] First, the ROM **141** of the control logic **140** may output the plurality of internal control signals int_CS**1**, int_CS**2**, int_CS**3**, and int_CS**4** in response to the command CMD.

[0079] The voltage generation control circuit **142** may output the first voltage generating circuit control signals VG_signals **1** and the second voltage generating circuit control signals VG_signals **2** in response to the internal control signals int_CS**1** and int_CS**2**. The voltage generating circuit **150** may generate the drain select line voltage V_{DSL0} applied to the first drain select line DSL**0** corresponding to the selected memory string and the drain select line voltages VDSL**1**, VDSL**2**, and VDSL**3** applied to the second, third, and fourth drain select lines DSL**1**, DSL**2**, and DSL**3** corresponding to the unselected memory strings in response to the first voltage generating circuit control signals VG_signals **1**. In addition, the voltage generating circuit **150** may generate the source select line voltage V_{SSL0} applied to the first source select line SSL**0** corresponding to the selected memory string and the source select line voltage V_{SSL1} applied to the second source select line SSL**1** corresponding to the unselected memory strings in response to the first voltage generating circuit control signals VG_signals **1**.

[0080] The address decoder control circuit **143** may output the address decoder control signals AD_signals in response to the internal control signal int_CS**3**. The address decoder **120** may apply the drain select line voltages V_{DSL0}, V_{DSL1}, V_{DSL2}, and V_{DSL3} to the first, second, third, and fourth drain select lines DSL**0**, DSL**1**, DSL**2**, and DSL**3** of the selected memory block BLK**1** and may apply the source select line voltages V_{SSL0} and V_{SSL1} to the first and second source select lines SSL**0** and SSL**1** in response to the address decoder control signals AD_signals and the address ADDR (S**640**).

[0081] The drain select line voltage V_{DSL1} having the turn-on voltage may be applied to the unselected memory string which shares the source select line SSL**0** with the selected memory string to turn on the drain select transistor DST.

[0082] The voltage generating circuit **150** may generate the read voltage Vread and the pass voltage Vpass applied to the word lines WL of the selected memory block BLK**1** in response to the second voltage generating circuit control signals VG_signals **2**.

[0083] The address decoder control circuit **143** may output the address decoder control signals AD_signals in response to the internal control signal int_CS**3**. The address decoder **120** may apply the pass voltage Vpass to the unselected word lines (for example, WL**1**, WL**2**, and WL**4** to WLn) of the selected memory block BLK**1** in response to the address decoder control signals AD_signals and the address ADDR. Because the drain select line voltage V_{DSL1} having the turn-on voltage is applied to the unselected memory string which shares the source select line SSL**0** with the selected memory string and the drain select transistor DST is turned on, a local boosting phenomenon might not occur in a channel of the memory cells F**4** to Fn even when the pass voltage Vpass is applied to the unselected word lines WL**4** to WLn. Accordingly, because the local boosting phenomenon of the unselected memory string which shares the first source select line SSL**0** with the selected memory string is prevented, a disturb phenomenon caused by Hot Carrier Injection (HCI) may be improved.

[0084] Subsequently, the address decoder **120** may apply (S**650**) the read voltage Vread to the selected word line WL**3** in response to the address decoder control signals AD_signals and the address ADDR. Subsequently, the page buffer control circuit **144** may output the page buffer control signals PB_signals in response to the internal control signal int_CS**4** and the read and write circuit **130** may sense a potential level or a current level of the bit lines BL**1** to BLm of the selected memory block BLK**1** and perform a read operation in response to the page buffer control signals PB_signals.

[0085] Read data DATA sensed by the read and write circuit **130** may be output to an external device.

[0086] FIG. **8** is a waveform diagram of signals illustrating a method of performing a read operation of a memory device according to a first embodiment.

[0087] The method of performing a read operation of a memory device according to the first embodiment is described below with reference to FIGS. **3** to **8**.

[0088] First, a first voltage V**1** may be applied to the first drain select line DSL**0** and the first source select line SSL**0** corresponding to a selected memory string ST. The first voltage V**1** may be a voltage to turn on the drain select transistor DST and the source select transistor SST. In addition, a second voltage V**2** may be applied to the second drain select line DSL**1** corresponding to the unselected memory string which shares the first source select line SSL**0**

with the selected memory string during a first time period t1. For an embodiment, the second voltage V2 may have the same potential level as the first voltage V1. Accordingly, the source select transistor SST and the drain select transistor DST included in the unselected memory string which shares the first source select line SSL0 with the selected memory string may be turned on.

[0089] Subsequently, the pass voltage Vpass may be applied to unselected word lines Unsel WLs. Even when the pass voltage Vpass is applied to the unselected memory string which shares the first source select line SSL0 with the selected memory string, because the source select transistor SST and the drain select transistor DST are turned on, a local boosting phenomenon might not occur in a channel of the pass voltage Vpass of the unselected memory string which shares the first source select line SSL0 with the selected memory string. Accordingly, a disturb phenomenon caused by Hot Carrier Injection (HCI) may be improved.

[0090] Subsequently, the read voltage Vread may be applied to a selected word line Sel WL during a second time period t2.

[0091] FIG. 9 is a waveform diagram of signals illustrating a method of performing a read operation of a memory device according to a second embodiment.

[0092] The method of performing a read operation of a memory device according to the second embodiment is described below with reference to FIGS. 3 to 9.

[0093] First, the first voltage V1 may be applied to the first drain select line DSL0 and the first source select line SSL0 corresponding to the selected memory string ST. The first voltage V1 may be a voltage to turn on the drain select transistor DST and the source select transistor SST. In addition, the second voltage V2 may be applied to the second drain select line DSL1 corresponding to the unselected memory string which shares the first source select line SSL0 with the selected memory string during the first time period t1. For an embodiment, the second voltage V2 may have the same potential level as the first voltage V1. Accordingly, the source select transistor SST and the drain select transistor DST included in the unselected memory string which shares the first source select line SSL0 with the selected memory string may be turned on. In addition, a third voltage V3 may be applied to the second source select line SSL1, the third drain select line DSL2, and the fourth drain select line DSL3 corresponding to the remaining unselected memory strings. The third voltage V3 may be lower than the second voltage V2. The third voltage V3 may be lower than a threshold voltage of each of the source select transistor SST and the drain select transistor DST. Accordingly, the drain select transistor DST and the source select transistor SST of the remaining unselected memory strings might not be turned on. However, a leakage current may be incurred by the third voltage V3.

[0094] Subsequently, the pass voltage Vpass may be applied to the unselected word lines Unsel WLs. Even when the pass voltage Vpass is applied to the unselected memory string which shares the first source select line SSL0 with the selected memory string, because the source select transistor SST and the drain select transistor DST are turned on, a local boosting phenomenon might not occur in a channel of the pass voltage Vpass of the unselected memory string which shares the first source select line SSL0 with the selected memory string. Accordingly, a disturb phenomenon caused by Hot Carrier Injection (HCI) may be improved. In addition, a leakage current may occur from the drain select transistor DST and the source select transistor SST of the remaining unselected memory strings, such that a potential level of a channel of the remaining unselected memory strings may be decreased. Accordingly, a disturb phenomenon of the remaining unselected memory strings caused by Hot Carrier Injection (HCI) may be improved.

[0095] Subsequently, the read voltage Vread may be applied to the selected word line Sel WL during the second time period t2.

[0096] FIG. 10 is a waveform diagram of signals illustrating a method of performing a read operation of a memory device according to a third embodiment.

[0097] The method of performing a read operation of a memory device according to the third embodiment is described below with reference to FIGS. 3 to 10.

[0098] First, the first voltage V1 may be applied to the first drain select line DSL0 and the first source select line SSL0 corresponding to the selected memory string ST. The first voltage V1 may be a voltage to turn on the drain select transistor DST and the source select transistor SST. In addition, the second voltage V2 may be applied to the second drain select line DSL1 corresponding to the unselected memory string which shares the first source select line SSL0 with the selected memory string during the first time period t1. For an embodiment, the second voltage V2 may have the same potential level as the first voltage V1. Accordingly, the source select transistor SST and the drain select transistor DST included in the unselected memory string which shares the first source select line SSL0 with the selected memory string may be turned on. In addition, a fourth voltage V4 may be applied to the second source select line SSL1, the third drain select line DSL2 and the fourth drain select line DSL3 corresponding to the remaining unselected memory strings. The fourth voltage V4 may be applied during a shorter time period t1' than the time period t1 during which the second voltage V2 is applied. The fourth voltage V4 may have a potential level the same as or lower than the second voltage V2. Accordingly, the drain select transistor DST and the source select transistor SST of the remaining unselected memory strings may be turned on during a time period shorter than a time period during which the drain select transistor DST and the source select transistor SST of the unselected memory string which shares the source select line with the selected memory string, or a leakage current may occur.

[0099] Subsequently, the pass voltage Vpass may be applied to the unselected word lines Unsel WLs. Even when the pass voltage Vpass is applied to the unselected memory string which shares the first source select line SSL0 with the selected memory string, because the source select transistor SST and the drain select transistor DST are turned on, a local boosting phenomenon might not occur in a channel of the pass voltage Vpass of the unselected memory string which shares the first source select line SSL0 with the selected memory string. Accordingly, a disturb phenomenon caused by Hot Carrier Injection (HCI) may be improved. In addition, the drain select transistor DST and the source select transistor SST of the remaining unselected memory strings may be turned on during the shorter time period t1' than the time period t1 or a leakage current may occur, such that a potential level of a channel of the remaining unselected memory strings may be decreased. Accordingly, a disturb

phenomenon of the remaining unselected memory strings caused by Hot Carrier Injection (HCI) may be improved.

[0100] Subsequently, the read voltage Vread may be applied to the selected word line Sel WL.

[0101] FIG. **11** is a waveform diagram of signals illustrating a method of performing a read operation of a memory device according to a fourth embodiment.

[0102] The method of performing a read operation of a memory device according to the fourth embodiment is described below with reference to FIGS. **3** to **11**.

[0103] First, the first voltage V**1** may be applied to the first drain select line DSL**0** and the first source select line SSL**0** corresponding to the selected memory string ST. The first voltage V**1** may be a voltage to turn on the drain select transistor DST and the source select transistor SST. In addition, the second voltage V**2** may be applied to the second drain select line DSL**1** corresponding to the unselected memory string which shares the first source select line SSL**0** with the selected memory string during the first time period t**1**. For an embodiment, the second voltage V**2** may have the same potential level as the first voltage V**1**. Accordingly, the source select transistor SST and the drain select transistor DST included in the unselected memory string which shares the first source select line SSL**0** with the selected memory string may be turned on.

[0104] Subsequently, the pass voltage Vpass may be applied to the unselected word lines Unsel WLs. A fifth voltage V**5** may be applied to the selected word line Sel WL during a predetermined time period. For an embodiment, the fifth voltage V**5** may have the same potential level as the pass voltage Vpass. Accordingly, hot carriers which may be present in a channel of the unselected memory string which shares the source select line SSL**0** with the selected memory string may be removed through the bit line BL**1** and the source line SL. Accordingly, a disturb phenomenon caused by Hot Carrier Injection (HCI) may be improved.

[0105] Subsequently, the read voltage Vread may be applied to the selected word line Sel WL.

[0106] The fourth embodiment as stated above may correspond to the first embodiment to which removing the hot carriers in the channel by applying the fifth voltage V**5** to the selected word line Sel WL is added. The fourth embodiment may also be applied to the second embodiment and the third embodiment described above. In other words, the hot carriers in the channel of the memory strings may be removed by applying the fifth voltage V**5** to the selected word line Sel WL in a state where the third voltage V**3** is applied to the second source select line SSL**1**, the third drain select line DSL**2**, and the fourth drain select line DSL**3** corresponding to the remaining unselected memory strings in the second embodiment. In addition, the hot carriers in the channel of the memory strings may be removed by applying the fifth voltage V**5** to the selected word line Sel WL in a state where the fourth voltage V**4** is applied to the second source select line SSL**1**, the third drain select line DSL**2**, and the fourth drain select line DSL**3** corresponding to the remaining unselected memory strings in the third embodiment.

[0107] FIG. **12** is a diagram illustrating a memory system **30000** including the memory device of FIG. **1**.

[0108] Referring to FIG. **12**, the memory system **30000** may be embodied into a cellular phone, a smartphone, a tablet PC, a personal digital assistant (PDA), or a wireless communication device. The memory system **30000** may include a memory device **1100** and a memory controller **1200** controlling the operations of the memory device **1100**. The memory controller **1200** may control a data access operation of the memory device **1100**, for example, a program operation, an erase operation, or a read operation in response to control of a processor **3100**.

[0109] The memory controller **1200** may control data programmed into the memory device **1100** to be output through a display **3200** in response to control of the memory controller **1200**. The memory device **1100** may be configured and operated in the same manner as the memory device **100** shown in FIG. **1**.

[0110] A radio transceiver **3300** may exchange a radio signal through an antenna ANT. For example, the radio transceiver **3300** may change the radio signal received through the antenna ANT into a signal which can be processed by the processor **3100**. Therefore, the processor **3100** may process the signal output from the radio transceiver **3300** and transfer the processed signal to the memory controller **1200** or the display **3200**. The memory controller **1200** may program the signal processed by the processor **3100** into the memory device **1100**. In addition, the radio transceiver **3300** may change a signal output from the processor **3100** to a radio signal and output the radio signal to an external device through the antenna ANT. A control signal for controlling the operations of the processor **3100** or data to be processed by the processor **3100** may be input by an input device **3400**, and the input device **3400** may include a pointing device, such as a touch pad and a computer mouse, a keypad, or a keyboard. The processor **3100** may control the operations of the display **3200** so that data output from the memory controller **1200**, data output from the radio transceiver **3300**, or data output from the input device **3400** may be output through the display **3200**.

[0111] According to an embodiment, the memory controller **1200** controlling the operations of the memory device **1100** may be part of the processor **3100**, or be formed as a separate chip from the processor **3100**.

[0112] FIG. **13** is a diagram illustrating another embodiment of a memory system **40000**.

[0113] Referring to FIG. **13**, the memory system **40000** may be embodied into a personal computer (PC), a tablet PC, a net-book, an e-reader, a personal digital assistant (PDA), a portable multimedia player (PMP), an MP3 player, or an MP4 player.

[0114] The memory system **40000** may include the memory device **1100** and the memory controller **1200** controlling a data processing operation of the memory device **1100**. The memory device **1100** may be configured and operated in the same manner as the memory device **100** shown in FIG. **1**.

[0115] A processor **4100** may output data stored in the memory device **1100** through a display **4300** according to data input through an input device **4200**. Examples of the input device **4200** may include a pointing device such as a touch pad or a computer mouse, a keypad, or a keyboard.

[0116] The processor **4100** may control the general operations of the memory system **40000** and control the operations of the memory controller **1200**. According to an embodiment, the memory controller **1200** controlling the operations of the memory device **1100** may be part of the processor **4100**, or be formed as a separate chip from the processor **4100**.

[0117] FIG. **14** is a diagram illustrating another embodiment of a memory system **50000**.

[0118] Referring to FIG. **14**, the memory system **50000** may be embodied into an image processor, for example, a digital camera, a cellular phone with a digital camera attached thereto, a smartphone with a digital camera attached thereto, or a tablet PC with a digital camera attached thereto.

[0119] The memory system **50000** may include the memory device **1100** and the memory controller **1200** controlling a data processing operation of the memory device **1100**, for example, a program operation, an erase operation, or a read operation. The memory device **1100** may be configured and operated in the same manner as the memory device **100** shown in FIG. **1**.

[0120] An image sensor **5200** of the memory system **50000** may convert an optical image into digital signals, and the digital signals may be transferred to a processor **5100** or the memory controller **1200**. In response to control of the processor **5100**, the digital signals may be output through a display **5300** or stored in the memory device **1100** through the memory controller **1200**. In addition, the data stored in the memory device **1100** may be output through the display **5300** according to control of the processor **5100** or the memory controller **1200**.

[0121] According to an embodiment, the memory controller **1200** controlling the operations of the memory device **1100** may be part of the processor **5100**, or be formed as a separate chip from the processor **5100**.

[0122] FIG. **15** is a diagram illustrating another embodiment of a memory system **70000**.

[0123] Referring to FIG. **15**, the memory system **70000** may include a memory card or a smart card. The memory system **70000** may include the memory device **1100**, the memory controller **1200**, and a card interface **7100**. The memory device **1100** may be configured and operated in the same manner as the memory device **100** shown in FIG. **1**.

[0124] The memory controller **1200** may control data exchange between the memory device **1100** and the card interface **7100**. According to an embodiment, the card interface **7100** may be, but is not limited to, a secure digital (SD) card interface or a multi-media card (MMC) interface.

[0125] The card interface **7100** may interface data exchange between a host **60000** and the memory controller **1200** according to a protocol of the host **60000**. According to an embodiment, the card interface **7100** may support a Universal Serial Bus (USB) protocol and an InterChip (IC)-USB protocol. The card interface may refer to hardware capable of supporting a protocol which is used by the host **60000**, software installed in the hardware, or a signal transmission method.

[0126] When the memory system **70000** is connected to an host interface **6200** of the host **60000** such as a PC, a tablet PC, a digital camera, a digital audio player, a cellular phone, console video game hardware, or a digital set-top box, the host interface **6200** may perform data communication with the memory device **1100** through the card interface **7100** and the memory controller **1200** in response to control of a microprocessor **6100**.

[0127] As described above, according to the present disclosure, a read disturb phenomenon may be improved by adjusting an initial turn-on time period of select transistors of unselected memory strings during a read operation of a memory device.

[0128] It will be apparent to those skilled in the art that various modifications can be made to the above-described embodiments of the present teachings without departing from the spirit or scope of the present teachings. Thus, it is intended that the present teachings cover all such modifications provided they come within the scope of the appended claims and their equivalents.

[0129] As described above, although the present teachings are described with the limited embodiments and drawings, the present teachings are not limited to the above-stated embodiments. It would be possible for those skilled in the art to which the present teachings pertain to make many modifications and variations as still be consistent with the present teachings described above.

[0130] In the above-described embodiments, all steps may be selectively performed or skipped. In addition, the steps in each embodiment need not always be performed in regular order. Furthermore, the embodiments disclosed in the present specification and the drawings aim to help those with ordinary knowledge in this art more clearly understand the present disclosure rather than aiming to limit the bounds of the present disclosure. In other words, one of ordinary skill in the art to which the present disclosure belongs will understand that various modifications are possible based on the technical scope of the present disclosure.

[0131] Embodiments of the present disclosure have been described with reference to the accompanying drawings, and specific terms or words used in the description should be construed in accordance with the spirit of the present disclosure without limiting the subject matter thereof. It should be understood that many variations and modifications of the teachings described herein will still fall within the spirit and scope of the present disclosure as defined in the accompanying claims and equivalents thereof.

What is claimed is:

1. A memory device, comprising:

a memory cell array including a plurality of memory strings;

a voltage generating circuit configured to generate and apply a plurality of drain select line voltages, a plurality of source select line voltages, and a read voltage to the memory cell array during a read operation; and

control logic configured to control the voltage generating circuit to generate a first drain select line voltage applied to a first unselected memory string among unselected memory strings among the plurality of memory strings and a second drain select line voltage applied to second unselected memory strings among the unselected memory strings during the read operation, wherein the second drain select line voltage is different from the first drain select line voltage.

2. The memory device of claim **1**, wherein the plurality of memory strings included in the memory cell array are coupled between one bit line and a source line, and

wherein the plurality of memory strings share one source select line per at least two memory strings and the at least two memory strings are coupled to different drain select lines, respectively.

3. The memory device of claim **2**, wherein the first unselected memory string shares a source select line with a selected memory string, and

wherein the second unselected memory strings represent the unselected memory strings with the exception of the first unselected memory string.

4. The memory device of claim **1**, wherein the voltage generating circuit applies the first drain select line voltage

applied to the first unselected memory string at a level of a turn-on voltage during a first time period before applying the read voltage to the memory cell array during the read operation.

5. The memory device of claim **4**, wherein the voltage generating circuit applies the turn-on voltage to a drain select line and a source select line of a selected memory string sharing a source select line with the first unselected memory string when the first drain select line voltage having the level of the turn-on voltage is applied to the first unselected memory string.

6. The memory device of claim **4**, wherein the voltage generating circuit applies the first drain select line voltage having the level of the turn-on voltage to the first unselected memory string and applies a pass voltage to unselected word lines of the memory cell array.

7. The memory device of claim **4**, wherein the voltage generating circuit applies the turn-on voltage to a selected word line during a predetermined time period when a pass voltage is applied to unselected word lines of the memory cell array.

8. The memory device of claim **7**, wherein a channel of the first unselected memory string is electrically coupled to a bit line and a source line during a time period in which the first time period and the predetermined time period overlap each other to remove a hot carrier in the channel.

9. A memory device, comprising:

a memory cell array including a plurality of memory strings;

a voltage generating circuit configured to generate and apply a plurality of drain select line voltages, a plurality of source select line voltages, and a read voltage to the memory cell array during a read operation; and

control logic configured to control the voltage generating circuit to apply, during the read operation, a first drain select line voltage applied to a first unselected memory string among unselected memory strings among the plurality of memory strings at a first potential level and a second drain select line voltage applied to second unselected memory strings among the unselected memory strings at a second potential level lower than the first potential level.

10. The memory device of claim **9**, wherein the plurality of memory strings included in the memory cell array are coupled between one bit line and a source line, and

wherein the plurality of memory strings share one source select line per at least two memory strings, and the at least two memory strings are coupled to different drain select lines, respectively.

11. The memory device of claim **10**, wherein the first unselected memory string shares a source select line with a selected memory string, and

wherein the second unselected memory strings represent the unselected memory strings with the exception of the first unselected memory string.

12. The memory device of claim **9**, wherein the first potential level is higher than a threshold voltage of select transistors included in the unselected memory strings.

13. The memory device of claim **9**, wherein the voltage generating circuit applies the first drain select line voltage having the first potential level and the second drain select line voltage having the second potential level to the first unselected memory string and the second unselected memory strings, respectively, during a first time period before applying the read voltage to the memory cell array during the read operation.

14. The memory device of claim **13**, wherein the voltage generating circuit applies a turn-on voltage to a selected word line of the memory cell array during a predetermined time period after the first time period starts and before the read voltage is applied to the selected word line.

15. A memory device, comprising:

a memory cell array including a plurality of memory strings;

a voltage generating circuit configured to generate and apply a plurality of drain select line voltages, a plurality of source select line voltages, and a read voltage to the memory cell array during a read operation; and

control logic configured to control the voltage generating circuit to apply, during the read operation, a first drain select line voltage applied to a first unselected memory string among unselected memory strings among the plurality of memory strings during a first time period and a second drain select line voltage applied to second unselected memory strings among the unselected memory strings during a second time period shorter than the first time period.

16. The memory device of claim **15**, wherein the plurality of memory strings included in the memory cell array are coupled between one bit line and a source line, and

wherein the plurality of memory strings share one source select line per at least two memory strings and the at least two memory strings are coupled to different drain select lines, respectively.

17. The memory device of claim **16**, wherein the first unselected memory string shares a source select line with a selected memory string, and

wherein the second unselected memory strings represent the unselected memory strings with the exception of the first unselected memory string.

18. The memory device of claim **15**, wherein the voltage generating circuit applies the first drain select line voltage to the first unselected memory string and a pass voltage to unselected word lines of the memory cell array.

19. The memory device of claim **18**, wherein the voltage generating circuit applies a turn-on voltage to a selected word line of the memory cell array during a predetermined time period before the pass voltage is applied to the unselected word lines and the read voltage is applied to the selected word line.

20. The memory device of claim **15**, wherein the second drain select line voltage has a lower level of potential than the first drain select line voltage.

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