

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,

Petitioner,

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,

Patent Owner.

Case IPR2024-00792

Patent 11,468,957

**PATENT OWNER'S PRELIMINARY RESPONSE
UNDER 37 C.F.R. § 42.107**

TABLE OF CONTENTS

I. INTRODUCTION	1
II. THE CLAIMED INVENTION OF THE '957 PATENT	4
III. FILE HISTORY	11
IV. CLAIM CONSTRUCTION	12
V. BACKGROUND OF THE ASSERTED PRIOR ART	14
A. Chinese Pat. No. 109065091 (“Hongtao”) (Ex. 1005).....	14
B. U.S. Patent Pub. No. 2019/0198117 (“Yu”) (Ex. 1006).....	16
C. U.S. Pat. Pub. No. 2021/0082505 (“Suzuki”) (Ex. 1007).....	17
D. U.S. Pat. Pub No. 2018/0012667 (“Costa”) (Ex. 1008).....	19
E. U.S. Pat. Pub. No. 2021/0027848 (“Seo”) (Ex. 1009).....	20
VI. PETITIONER FAILS TO ESTABLISH A REASONABLE LIKELIHOOD THAT IT WOULD PREVAIL WITH RESPECT TO THE CHALLENGED CLAIMS	22
A. Ground 1 (Obviousness): Hongtao in View of Yu Does Not Disclose or Render Obvious Applying “a First Bias Voltage” and “a Second Bias Voltage” on the Gate Terminal of a Not Programmed Memory Cell “Wherein the Second Bias Voltage Is Smaller than the First Bias Voltage”	24
B. Ground 2 (Anticipation): Suzuki Does Not Disclose Applying a First Verify Voltage and First Bias Voltage in a “Pre-Verify” Stage, or Applying a Second Bias Voltage in a “Verify” Stage “Wherein the Second Bias Voltage Is Smaller than the First Bias Voltage”	32
C. Ground 3 (Obviousness): Costa in View of Seo Does Not Disclose or Render Obvious Applying “a First Bias Voltage” and “a Second Bias Voltage” on the Gate Terminal of a Not Programmed Memory Cell “Wherein the Second Bias Voltage Is Smaller than the First Bias Voltage”	36
VII. CONCLUSION.....	43

TABLE OF AUTHORITIES

Cases	Page(s)
<i>Phillips v. AWH Corp.</i> , 415 F.3d 1303 (Fed. Cir. 2005) (<i>en banc</i>)	12
<i>Netflix, Inc. v. DivX, LLC</i> , 80 F.4th 1352 (Fed. Cir. 2023)	3, 37
<i>Cheese Sys., Inc. v. Tetra Pak Cheese & Powder Sys., Inc.</i> , 725 F.3d 1341 (Fed. Cir. 2013)	3, 37
<i>PlaSmart, Inc. v. Kappos</i> , 482 F. App'x 568 (Fed. Cir. 2012)	28
<i>Verdegaal Bros. v. Union Oil Co. of California</i> , 814 F.2d 628 (Fed. Cir. 1987)	34

LIST OF EXHIBITS

Exhibit	Description
Ex. 2001	Micron 4-2 Claim Construction Disclosure
Ex. 2002	YMTC 4-2 Claim Construction Disclosure

LIST OF ABBREVIATIONS

Abbreviation	Term
'957	U.S. Pat. No. 11,468,957
'957FH	File History of U.S. Pat. No. 11,468,957
Challenged Claims	'957, Claims 1-6
Hongtao	C.N. Pat No. 109065091
Yu	U.S. Pat. No. 20190198117
Suzuki	U.S. Pat. No.. 20210082505
Costa	U.S. Pat. No. 20180012667
Seo	U.S. Pat. No. 20210027848
Office	U.S. Patent and Trademark Office
Petition or Pet.	Petition for <i>Inter Partes</i> Review of U.S. Patent No. 11,468,957 (IPR2024-00792, Paper 1)
Parallel district court litigation	<i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc.</i> , NDCA-3-23-cv-05792 (N.D. Cal.)
Patent Owner	Yangtze Memory Technologies Co. Ltd.
Petitioner	Micron Technology, Inc.
POSITA	Person of ordinary skill in the art

Pursuant to §42.107,¹ Patent Owner submits this Preliminary Response to the above-captioned Petition, which should be denied in its entirety based on Petitioner's failure to show a reasonable likelihood of prevailing on any asserted ground as to any Challenged Claim.

I. INTRODUCTION

U.S. Patent No. 11,468,957 is directed to an improved technique for performing verification operations on a selected memory cell of a memory cell string within a 3D NAND flash memory device that advantageously mitigates hot carrier injection ("HCI"), reduces edge summation ("ESUM") losses, and limits power consumption. *See* '957, 1:44-49. By comparison, the prior art at the time of the filing of the '957 performed verify operations in a way that that risked creating HCI and ESUM effects that increase the risk of read errors.

The new approach taught by '957 and recited in the claims is characterized by several features not found in or rendered obvious by the prior art, including the application of distinct verify voltages on a gate terminal of a selected memory cell during a pre-verify stage and a verify stage, and applying a first bias voltage in the

¹ All emphasis and color annotations herein are added, and all statutory and regulatory citations are to either 35 U.S.C. or 37 C.F.R., as the context indicates, unless otherwise stated.

pre-verify stage on a gate terminal of a memory cell that is not programmed, and a second smaller bias voltage to the gate terminal of the memory cell that is not programmed during the verify stage. By virtue of selectively applying these different verify and bias voltages during the pre-verify stage and the verify stage, the device is able to read and verify the programmed value of the selected memory cell while avoiding the effects of HCI and ESUM, and overcoming the drawbacks of the prior art. *See, e.g., '957, 1:44-49; see also id., 17:7-17.*

Institution should be denied because the Petition fails to establish a reasonable likelihood of prevailing with respect to any of the Challenged Claims.

Petitioner contends that the Challenged Claims are anticipated or obvious based on the supposed prior art. *See* Pet. 7-8. However, Petitioner's arguments mischaracterize the references and rely on a mix of unsupported assumptions, conclusory testimony from Dr. Liu, and hindsight rationalizations.

Petitioner's Ground 1 relies on the purported combination of Hongtao and Yu as supposedly rendering obvious the Challenged Claims. Petitioner's arguments incorrectly rely on Fig. 2 of Hongtao as showing the use of distinct bias voltages being applied to a gate terminal of a memory cell during a two-stage read operation, and improperly conflates the voltages in Fig. 2 of Hongtao with voltages applied on memory cell gate terminals. Yu does not address this deficiency in Hongtao, nor has

Petitioner presented a rationale why this missing subject matter would have been obvious to a POSITA.

Petitioner's Ground 2 incorrectly argues that Suzuki anticipates the Challenged Claims. Petitioner improperly attempts to conflate Suzuki's use of a data recovery operation with the claimed "pre-verify" stage, and incorrectly suggests that it would have been obvious to apply Suzuki's teachings to operations performed in a pre-verify stage. Suzuki does not disclose or render obvious the use of distinct voltages during a "pre-verify stage" and a "verify stage" as required by the Challenged Claims.

Petitioner's Ground 3 relies on a purported combination of Costa and Seo. Petitioner's arguments fail to show that the purported combination discloses or otherwise renders obvious the application of two distinct bias voltages as required by the Challenged Claims. Petitioner also does not show that the voltages in Costa and Seo are applied to a gate terminal of a memory cell. Moreover, Petitioner has not shown that a POSITA would have been motivated to combine the references in the manner suggested by the Petition, and the proposed combination does little more than try to impermissibly "reconstruct the applicant's invention only with the benefit of hindsight." *See Netflix, Inc. v. DivX, LLC*, 80 F.4th 1352, 1359 (Fed. Cir. 2023); *see also Cheese Sys., Inc. v. Tetra Pak Cheese & Powder Sys., Inc.*, 725 F.3d 1341, 1352 (Fed. Cir. 2013) (obviousness "cannot be based on the hindsight combination

of components selectively culled from the prior art to fit the parameters of the patented invention”).

Because each of Petitioner’s Grounds fails to disclose or render obvious the Challenged Claims, the Board should deny institution.

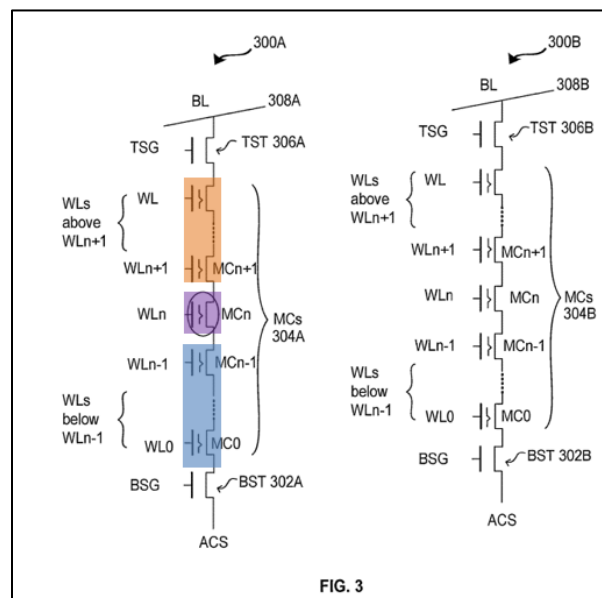
II. THE CLAIMED INVENTION OF THE ’957 PATENT

The claimed invention of the ’957 is directed to an improved technique for performing verify operations in Flash memory devices that mitigates hot-carrier injection (“HCI”) and induced edge summation (“ESUM”) losses, thus improving the overall reliability of the device, as well as reducing power consumption. *See* ’957, 1:44-49, 17:7-30.

As explained by the ’957, three-dimensional (3D) NAND flash memory was developed to “increase bit density and reduce the bit cost of flash memory devices.” ’957, 1:12-25. A “3D-NAND memory device can include a plurality of memory cell strings,” which in turn include “a bottom-select-gate (BSG) transistor, memory cells, and a top-select-gate (TSG) transistor that are connected in series.” ’957, 1:24-40; *see also id.* 8:27-43, 9:3-30, 14:31-34. Memory cells within the string are either “programmed in the forward order” going “from a bottom MC adjacent to the BSG transistor to a top MC adjacent to the TSG transistor” (*id.* at 9:57-10:7) or they are “programmed in a reverse order” going “from a top memory

cell adjacent to the TSG transistor to a bottom memory cell (e.g., MC0) adjacent to the BSG transistor” (*id.* at 14:31-42).

For example, as shown in Fig. 3, “the string 300A can include a bottom select transistor (BST) or bottom-select-gate (BSG) transistor 302A, a plurality of memory cells (MCs) 304A, and a top select transistor (TST) or top-select-gate (TSG) transistor 306A that are disposed sequentially and in series over the substrate along the height direction (e.g., Z direction) of the substrate 10.” ’957, 9:3-30. During programming operations, the **selected memory cell** that is being programmed is surrounded by the already **programmed memory cells** to one side of the string, and **not-programmed memory cells** (i.e., memory cells within the programming order that have yet to be programmed) on the other side of the string.

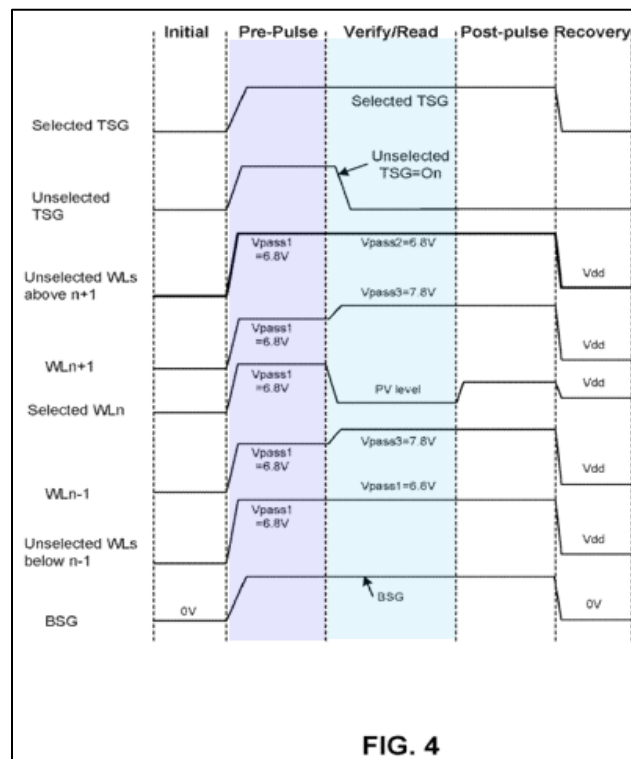


Id. Fig. 3 (annotations showing “**programmed**” and “**not-programmed**” memory cells when a forward programming order is used).

As discussed in the '957, traditional approaches for performing verify operations suffered from “hot carrier injection” (HCI) between the selected memory cell that is having its programmed state being verified and neighboring memory cells, which could result in “induced edge summation (ESUM) loss.” '957, 1:44-49, *see also id.* 7:66-12. The claimed invention of the '957 helps to address these issues by subdividing the verification operation into multiple distinct stages (e.g., a “pre-verify” stage and a “verify” stage), and selectively applying different voltages to the gate terminals of the selected memory cell and other not-programmed memory cells during each stage. *See* '957, 7:13-32.

The claimed invention of the '957 is explicitly directed to the bias voltages and verify voltages applied “on a gate terminal” of the memory cells within the memory cell string, as distinct from the voltages applied to corresponding word lines. *See, e.g.,* '957, Claim 1, 1:50-2:8, 6:37-49, 15:31-16, Fig. 10. As explained by the '957, bias and verify voltages “can be applied on the gate terminal (or gate) of the selected memory cell MC_n through a WL layer (e.g., WL_n) that is coupled to the selected memory cell MC_n.” '957, 9:31-56. But the applied bias voltages on the memory cell gate terminals may differ from the applied word line voltages, as they need time to fully “develop” to the desired target values. *See, e.g.,* '957, 6:37-7:12. As illustrated in Figs. 4 and 5, this distinction becomes particularly important depending on the duration of the “pre-verify” period. *See* '957, 11:58-12:27.

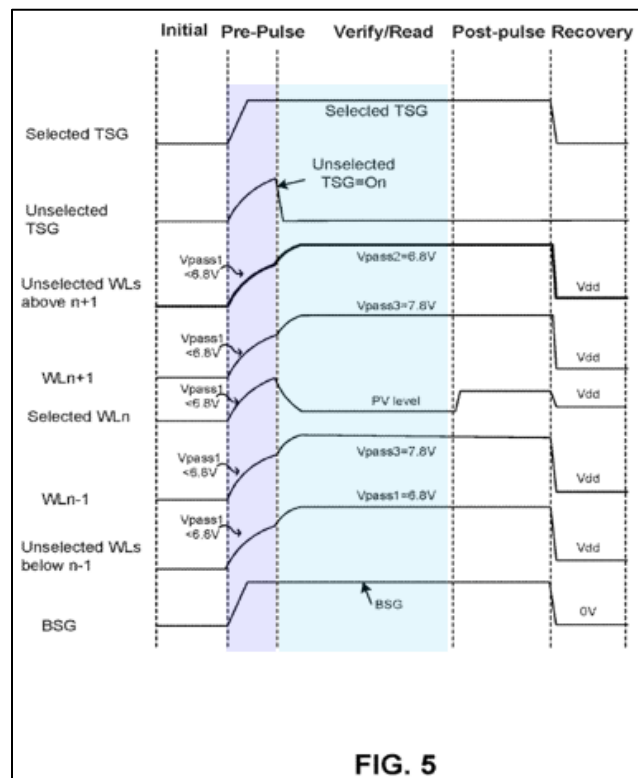
Fig. 4 shows how bias voltages may be applied using “a long pre-pulse time,” while Fig. 5 shows the challenges of using a “short pre-pulse time.” *Compare* ’957, 11:58-12:9 *with* 12:10-27. In Fig. 4, “appropriate bias voltages can be applied on the selected TSG layer, the unselected TSG layer, the WLs ($>n+1$), the $WLn+1$, the WLn , the WLs ($<n-1$), and the BSG layer in the **pre-pulse stage**.” ’957, 10:57-11:15. For example, a bias voltage of 6.8 volts can be applied on each word line. *See id.* During the subsequent “**verify/read stage**,” “[t]he bias voltage applied on the WLs ($>n+1$) can be maintained,” and the “bias voltage (or verify voltage) applied on the selected word line layer WLn can be reduced.” ’957, 11:16-57.



As explained by the ’957, “the long pre-pulse time” of Fig. 4 may be “sufficient for the bias voltages to be developed fully before the TSG transistor is switched off,”

meaning the applied bias voltages on the transistor gates will reach the desired values that were applied through the word lines. '957, 11:68-12:1; *see also id.* 13:13-15.

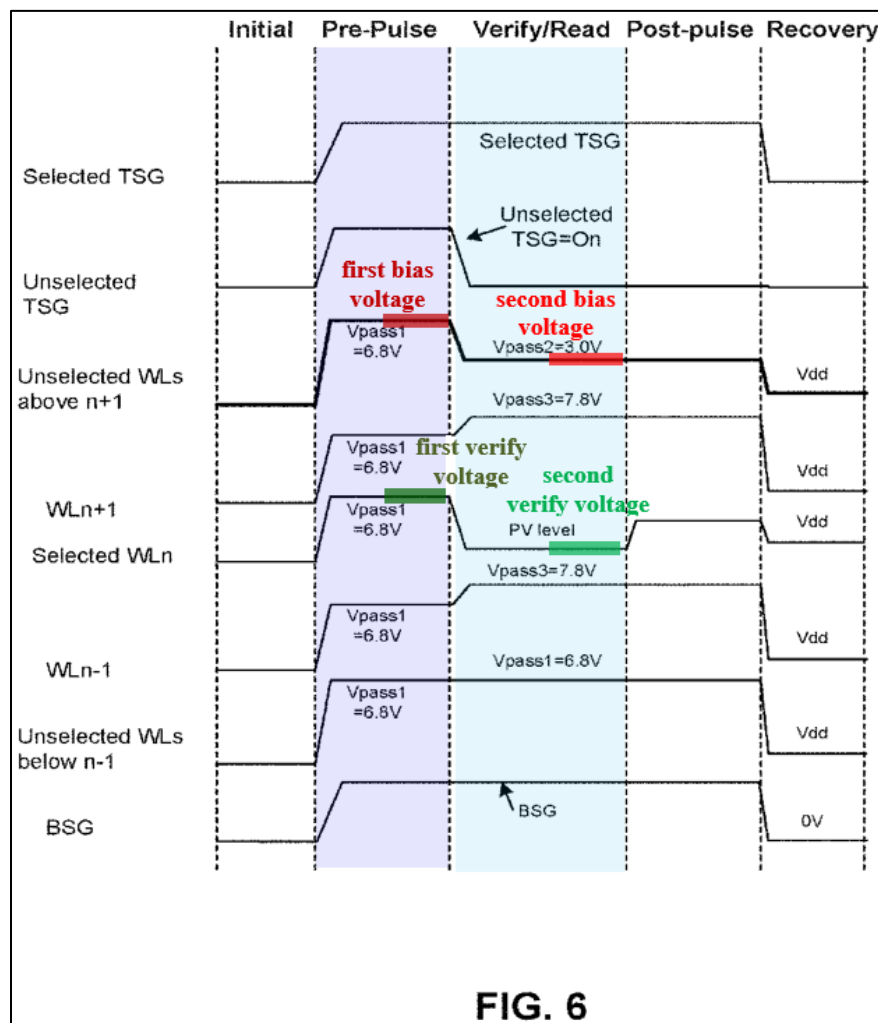
By comparison, Fig. 5 illustrates “a short pre-pulse time” that is “insufficient for the bias voltages applied on the WLs ($>n+1$), $WLn+1$, WLn , $WLn-1$, and WLs ($<n-1$) to be developed fully in the **pre-pulse stage**.” '957 12:10-27. As shown by the curved lines in Fig. 5, “the bias voltages are less than a target value, such as 6.8 volts,” because insufficient time is provided for the bias voltages to charge up during the **pre-pulse stage**. *Id.* Instead, the bias voltages are only “developed to the target value, such as 6.8 volts, in the **verify/read stage**.” *Id.*



Accordingly, depending on the duration of the pre-pulse stage, additional techniques are needed to ensure that bias voltages that actually appear on the memory cell gate

terminals are able to fully develop to the desired target values. *Compare* '957, 11:58-12:9, 12:28-39, 14:31-41, Figs. 4, 6, 8 (using a long pre-pulse time) *with* 12:10-38, 13:5-25, 14:63-15:17, Figs. 5, 7, 9 (using a short pre-pulse time).

For example, Fig. 6 is a '957 embodiment that uses a "long pre-pulse period" similar to Fig. 4, meaning that the bias voltages applied on the gate terminals will fully develop and reach the values applied on the word lines. '957, 12:28-42; *see also id.* 11:48-12:9. But unlike Fig. 4, the bias voltages applied to the WLs above $WLn+1$ are smaller in the **verify stage** than the **pre-verify stage**. '957 12:39-42.



As a result, in the embodiment of Fig. 6 a **first verify voltage** is applied to the gate of a selected memory cell in the **pre-verify stage**. '957, 1:58-2:8. At the same time, a **first bias voltage** is applied to the gate of a memory cell of the memory cell string that is not yet programmed. '957, 6:37-49. Subsequently, in a **verify stage**, a **second verify voltage** is applied to the gate of the selected memory cell, and a **second bias voltage** smaller than the **first bias voltage** is applied to the gate of the memory cell of the first memory cell string that is not programmed. '957, 17:32-56.

The '957 explains that by applying “a lower bias voltage” in the verify stage as compared to the pre-verify stage “the gradient of the channel potential of the selected memory cell string can be reduced,” and as a result “HCI cannot be generated from the selected memory cell to the upper adjacent memory cell of the selected in the selected memory cell string.” '957, 12:63-13:4. The claimed approach therefore not only lowers power consumption, but by mitigating HCI the invention of the '957 prevents ESUM loss and improves device performance as compared to conventional systems. *See* '957, 6:50-65, 17:7-17.

Independent Claim 1 of the '957 is an apparatus claim directed to aspects of the above-described invention:

[1.pre] An apparatus for reading a memory device including a first memory cell string and a second memory cell string, the first memory cell string including a bottom-select-gate (BSG) transistor, memory cells, and a top-select-gate (TSG) transistor that are connected in series, the second memory cells string including a BSG transistor, memory cells, and a TSG transistor

that are connected in series, the apparatus comprising: processing circuitry configured to:

[1.a] apply, in a pre-verify stage, a first verify voltage on a gate terminal of a selected memory cell of the first memory cell string, the selected memory cell being programmed and arranged between a first adjacent memory cell and a second adjacent memory cell;

[1.b] apply, in the pre-verify stage, a first bias voltage on a gate terminal of at least one memory cell of the first memory cell string that is not programmed;

[1.c] apply, in a verify stage, a second verify voltage on the gate terminal of the selected memory cell of the first memory cell string; and

[1.d] apply, in the verify stage, a second bias voltage on the gate terminal of the at least one memory cell of the first memory cell string that is not programmed, wherein the second bias voltage is smaller than the first bias voltage.

III. FILE HISTORY

The '957 claims remain patentable over the prior art of record. The '957 was filed on March 4, 2021 as a continuation of PCT application No. PCT/CN2020/136482 (published as WO 2022/126368), which itself was filed on December 15, 2020.

The Examiner issued a restriction requirement on March 15, 2022, identifying several distinct groups of claims in the pending application. Ex. 1002, 211-218. Applicant responded on May 6, 2022, electing to pursue prosecution claims 15-20 drawn to “an apparatus for reading a memory device.” Ex. 1002, 220-222.

The Examiner issued a subsequent notice of allowance on June 8, 2022, and issued an Examiner amendment cancelling the unelected claims. Ex. 1002, 225-232. In the statement for the reasons for allowance, the Examiner found that the claim limitations taken as a whole were allowable over the prior art of record, stating that “[t]he prior arts fail to teach or reasonably suggest, in combination,” claim 1 of the ’957 patent. Ex. 1002, 230-231.

IV. CLAIM CONSTRUCTION

The Board construes claim terms “using the same claim construction standard that would be used to construe the claim in a civil action.” §42.100(b). Under this standard, claim terms are “generally given their ordinary and customary meaning” to a person of ordinary skill in the art (“POSITA”). *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312 (Fed. Cir. 2005) (*en banc*). A POSITA ascertains the meaning of the claims based on the claim language, specification, prosecution history, and relevant extrinsic evidence, although the claims and patent specification are the primary sources for construing claims. *Id.*, 13:14-16.

In the parallel district court proceeding, the parties have set forth the following proposed constructions for the ’957, but neither side had exchanged claim construction briefs, and Markman proceedings have not yet taken place:

Term	Patent Owner Proposed Construction	Petitioner's Proposed Construction
“in [a/the] preverify stage” (claims 1, 4-5)	Plain and Ordinary Meaning	The plain and ordinary meaning is “a time period before the verify stage in which voltages are applied to prepare for the verify stage”
“in [a/the] verify stage” (claims 1, 4-5)	Plain and Ordinary Meaning	The plain and ordinary meaning is “a time period before any post-pulse and post-recovery stages in which the target memory cell is read to verify the success of a program operation”

See Exs. 2001 (“Micron 4-2 Claim Construction Disclosure”); 2002 (“YMTC 4-2 Claim Construction Disclosure”). Patent Owner submits that the Board does not need to resolve the disputes raised in the parallel district court proceedings for the purposes of institution, as the Grounds set forth in the Petition fail under either party’s proposed interpretation of the terms “pre-verify stage” and “verify stage.”

The Petition raises an added argument regarding the scope of “pre-verify stage” and “verify stage” that need not be resolved for purposes of deciding whether to institute IPR. Specifically, the Petition argues that the claims are satisfied even if “the first bias ... [is] not applied throughout the pre-pulse (preverify) stage,” and that “claim 1’s limitation that ‘the second bias voltage is smaller than the first bias voltage’ does not require the second bias voltage during the verify stage to be smaller than the first bias voltage for the entire duration of the pre-verify stage.” Pet. 18-19.

In order to resolve the arguments raised in this Preliminary Response, it is not necessary for the Board to resolve whether the “first bias voltage” may be applied for only a limited portion of the pre-verify stage (or whether the second bias voltage must be smaller than the first bias voltage for the entire duration of the pre-verify stage). Even under Petitioner’s proposed interpretation, each of the Grounds fails at least because the claimed “first bias voltage” and “first verify voltage” recited by Claim 1 must still be applied during a “pre-verify stage” (*see* Section VI.B, addressing Ground 2), and the claims still require applying a second bias voltage on a memory cell gate that is “smaller than the first bias voltage” (*see* Sections VI.A, VI.C; addressing Ground 1 and 3).

Patent Owner reserves the right to raise claim construction issues if the Board institutes IPR and in the underlying district court proceedings.

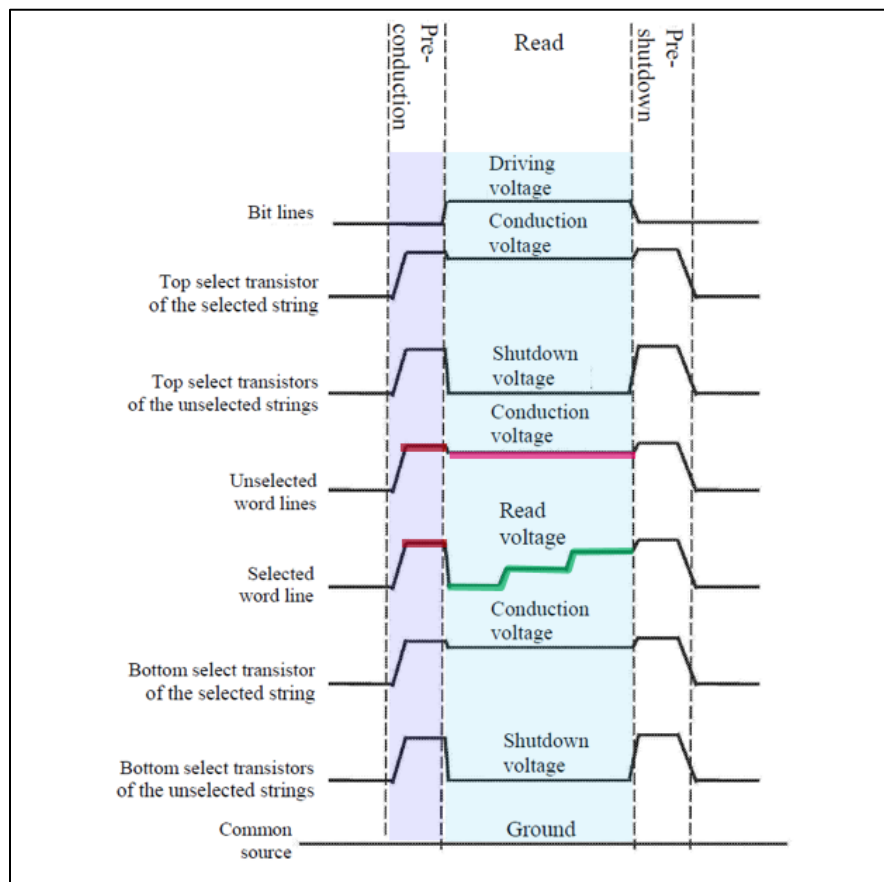
V. BACKGROUND OF THE ASSERTED PRIOR ART

A. Chinese Pat. No. 109065091 (“Hongtao”) (Ex. 1005)

Petitioner does not contend that Hongtao anticipates the Challenged Claims, and instead argues only that the combination of Hongtao and Yu (Ground 1) renders obvious the Challenged Claims. *See* Pet., 27-40. Hongtao purportedly discloses a multi-step method for reading memory cells in a 3D NAND flash memory device that includes a “**pre-conduction phase**” followed by a “**reading phase step**,” which Petitioner analogizes with the claimed “pre-verify stage” and “verify stage.” *See*

Hongtao, [0006]; Pet. 20-22, 30-40. But unlike the '957, Hongtao does not recognize the importance of long versus short pre-pulse periods, or directly address the actual voltages applied on the “gate terminal” of the various memory cells.

Hongtao states that during the **pre-conduction phase** a “**pre-conduction voltage**” is applied to both the unselected word line and the selected word line to turn on the channels of the selected string and the unselected string.” *See* Hongtao, [0023]. In the **reading phase**, “the unselected memory cells on the selected string are applied with a **conduction voltage** through the unselected word lines,” while the selected memory cell receives a series of **read voltages**. Hongtao, [0025].



Petitioner argues that Hongtao’s “**pre-conduction voltage**” is equivalent to the claimed “a first bias voltage on a gate terminal,” and that Hongtao’s “**conduction voltage**” is equivalent to the claimed “second bias voltage on the gate terminal.” *See* Pet. 30-40. Based solely on the above figure, Petitioner argues that this mapping teaches “[a] second bias voltage is smaller than [a] first bias voltage” applied on a gate terminal of a memory cell that is not programmed, as required by the Challenged Claims. *See* Pet. 39-40. But Figure 2 of Hongtao illustrates voltages that are applied to word line layers, not the bias voltages applied on gate terminals of the memory cells. *See* Hongtao [0023], [0025]. Moreover, Hongtao does not provide the necessary details to infer how the resulting voltages on the gate terminals of the memory cells would develop over time, nor has the Petitioner presented any arguments that it would have been obvious to implement Hongtao’s system such that the voltages applied to the gate terminals of the memory cells develop fully so as to match the values illustrated in Figure 2. *C.f.* ’957, 11:58-12:9, 12:10-27 (discussing that bias voltages need sufficient time to develop fully).

B. U.S. Patent Pub. No. 2019/0198117 (“Yu”) (Ex. 1006)

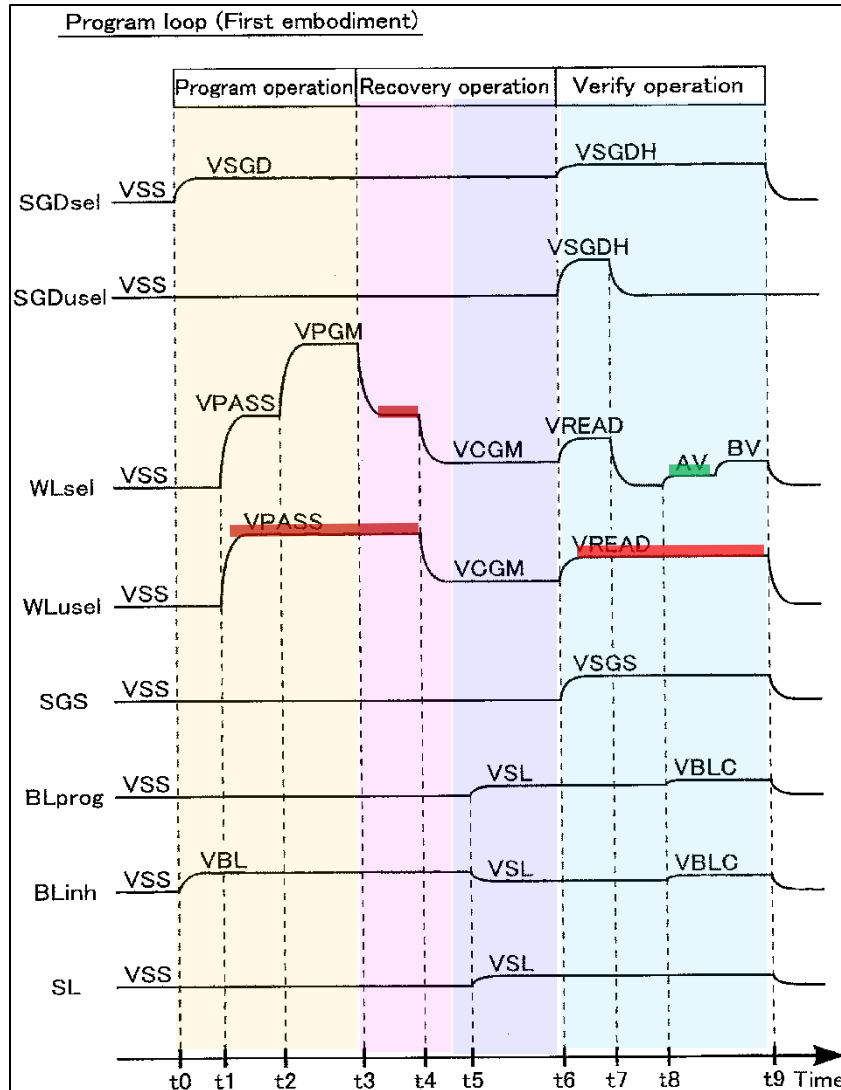
Petitioner does not contend that Yu anticipates the Challenged Claims, and instead argues only that the combination of Yu and Hongtao (Ground 1) renders obvious the Challenged Claims. Pet., 27-40. Yu does not teach—and Petitioner does not contend that it teaches—the use of distinct bias voltages during a “pre-verify”

and “verify” stage, with a second bias voltage that is smaller than a first bias voltage, as recited by the Challenged Claims.

C. U.S. Pat. Pub. No. 2021/0082505 (“Suzuki”) (Ex. 1007)

Petitioner contends that Suzuki (Ground 2) anticipates the Challenged Claims. Pet., 7-8, 74-102. Suzuki purportedly discloses different embodiments of a “program loop,” which is divided into a distinct “program operation,” “recovery operation,” and “verify operation” that are preformed in sequence. *See*, Suzuki, [0028].

As illustrated in Fig. 11, the program loop is divided into ten different time periods, where “time t0 to time t3 corresponds to a **program operation**,” “time t3 to time t6 corresponds to a recovery operation,” and “time t6 to time t9 corresponds to a **verify operation**.” Suzuki, [0131]. As explained in Suzuki, the recovery operation is a combination of “**an end operation of the program operation** and the **ready operation of the verify operation**.” Suzuki, [0131].



At time t3, the first part of the recovery operation (i.e., the “**end operation of the program operation**”), “**VPASS**” is applied to the selected word line “WLsel,” and “**VPASS**” continues to be applied to the unselected word line “WLusel.” Suzuki, [0134], [0137]. During the latter part of the recover operation (i.e., the “**ready operation of the verify operation**”), the voltage “VCGM... lower than VPASS” is applied instead. *Id.* [0138]. During the start of the **verify operation** at time t6, “**VREAD** is applied to each of the word lines” (Suzuki, [0114]), and “verify voltages

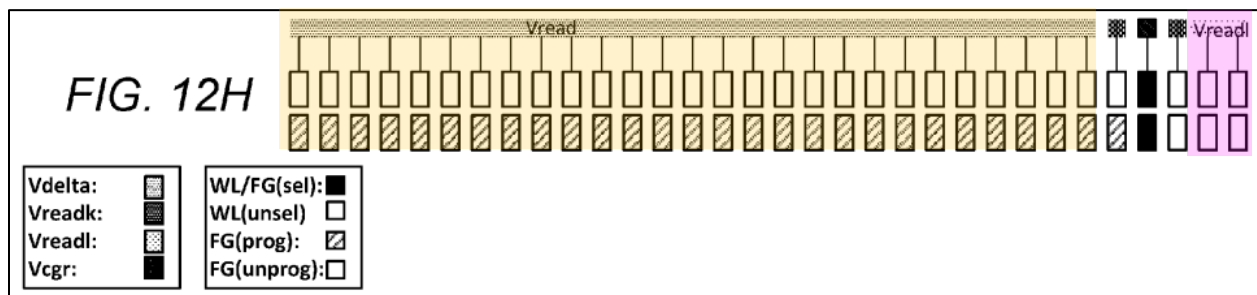
AV and BV” are applied to the selected word line WLsel at time t8 (Suzuki, [0145]). As shown, VCGM applied during the “**ready operation of the verify operation**” is lower than **VREAD**.

Petitioner argues that Suzuki’s “**VPASS**” is a “first bias voltage” applied during a “pre-verify stage,” and that the subsequent “**VREAD**” is a “second bias voltage” applied in a verify stage and is smaller than the first bias voltage. However, the time period t3-t4 when “**VPASS**” (i.e., the purported “first bias voltage”) is being applied is not a “pre-verify” stage as required by the Challenged Claims. Instead, Suzuki discloses that t3-t4 is “**an end operation of the program operation.**” Suzuki, [0131]. Thus, **VPASS** is applied during the program operation, and is not applied in a pre-verify stage to prepare the memory string for a subsequent verification operation.

D. U.S. Pat. Pub No. 2018/0012667 (“Costa”) (Ex. 1008)

Petitioner does not contend that Costa anticipates the Challenged Claims, and instead argues only that the combination of Costa and Seo (Ground 3) renders obvious the Challenged Claims. *See* Pet. 7-8, 103-126. Costa is purportedly directed to a technology for “reducing errors when sensing in non-volatile memory” by using different reading voltages. Costa, [0028]. Specifically, Costa discloses that a lower “pass voltage” can be used for unprogrammed memory cells as compared to programmed memory cells. *See* Costa [0121]-[0122], [0147]. As explained by Costa,

programming a memory cell increases the threshold voltage (*see* Costa [0082]), and because the unprogrammed cells are in an erased state, “lower read pass voltage VreadL can be used while still ensuring that these memory cells operate as pass gates” (Costa [0122]). For example, as shown in Figure 12H, a generic “**Vread**” value is used for already programmed memory cells, and a lower “**VreadL**” value is used for memory cells that are still unprogrammed:



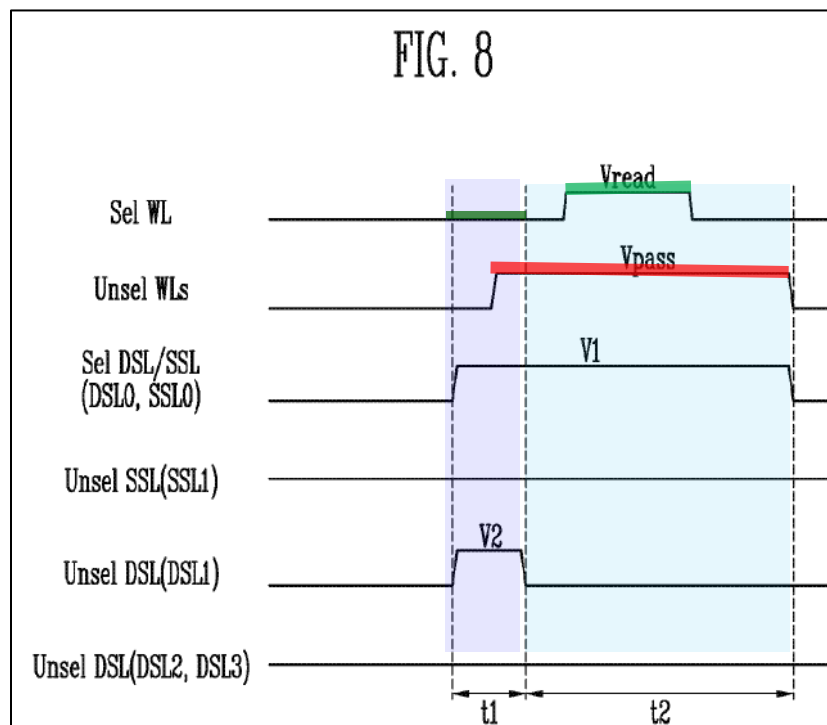
However, Costa does not disclose the use of separate “verify” and “pre-verify” stages for a verify operation, nor does Costa disclose that different voltage levels would be used during a “verify” and a “pre-verify” stage as required by the ’957. At most, Costa discloses applying different “pass voltages” to different memory cells, but the pass voltage applied to any given memory cell is constant throughout the entire sensing process.

E. U.S. Pat. Pub. No. 2021/0027848 (“Seo”) (Ex. 1009)

Similarly, Petitioner does not contend that Seo anticipates the Challenged Claims, and instead argues only that the combination of Seo and Costa (Ground 3) renders obvious the Challenged Claims. Seo purportedly discloses a memory device

“read” operation is divided into a “first time period t1” and a “second time period t2” with different voltages applied in each period. Seo [0011]. But similar to Costa, Seo fails to disclose multiple different pass voltages (or any other type of purported bias voltage) being applied to an unselected word line at different times.

As shown by Fig. 8, Seo discloses different voltages being applied to unselected word lines, “Unsel WLs,” and selected word lines “Sel WL.” *See* Seo, [0086]-[0090]. With respect to “Sel WL,” some **unspecified voltage** is applied during time period t1, which is replaced by “the read voltage **Vread** ... during a second time period t2.” *Seo* [0090]. With respect to the “Unsel WLs,” “the pass voltage **Vpass** may be applied to unselected word lines” during both a portion of time period t1 as well as time period t2.



But Seo does not disclose that the voltages applied to the word lines would also be applied to the gate terminals of the memory cells. *C.f.* '957, 11:58-12:9, 12:10-27 (discussing that bias voltages need sufficient time to develop fully). Moreover, as shown in Figure 8, Seo does not disclose that the value of V_{pass} applied to a given word line would change between “time period t1” and “time period t2.” Petitioner seemingly concedes that Seo does not disclose the use of distinct bias voltages during a “pre-verify stage” and a “verify stage,” as required by the Challenged Claims. *See* Pet. 26, 103-126.

VI. PETITIONER FAILS TO ESTABLISH A REASONABLE LIKELIHOOD THAT IT WOULD PREVAIL WITH RESPECT TO THE CHALLENGED CLAIMS

Petitioner fails to establish a reasonable likelihood that it would prevail with respect to the Challenged Claims because Petitioner has failed to show that the cited references disclose or render obvious the features [1.a]-[1.d] of independent claim 1. As explained below, Petitioner argues three grounds: (1) obviousness based on Hongtao in view of Yu; (2) anticipation based on Suzuki; and (3) obviousness based on Costa in view of Seo. Each of Petitioner's arguments fails.

First, Hongtao in view of Yu does not disclose or render obvious applying two different bias voltages on a gate terminal of a unprogrammed memory cell in a pre-verify stage and a verify stage, “wherein the second bias voltage is smaller than the first bias voltage.” Petitioner relies only on Fig. 2 of Hongtao for this subject

matter, but that figure addresses word line voltages—not voltages at the gate terminal of the memory cell. And neither Hongtao nor petitioner ever addresses whether the time the voltages are applied would be sufficient for the gate terminal to reach a particular voltage.

Second, Petitioner’s anticipation argument based on Suzuki fails because the purported “first bias voltage” and “first verify voltage” identified by Petitioner are not applied during a “pre-verify stage” as required by the Challenged Claims. Rather, Suzuki discloses that the identified voltages relate to the “end operation of the program operation,” rather than a pre-verify operation. *See* Suzuki, [0131].

Third, Costa in view of Seo does not disclose or render obvious applying two different bias voltages on a gate terminal of an unprogrammed memory cell in a pre-verify stage and a verify stage, “wherein the second bias voltage is smaller than the first bias voltage.” Neither of the references discloses that the voltages applied to a given word line (or the voltages applied on a gate terminal of a memory cell that would develop over time as a result) are smaller during a verify stage, and the combination likewise provides no such teaching. Moreover, Petitioner has failed to present a cogent argument other than hindsight as to why a POSITA would have been motivated to combine the reference in the manner suggested by the Petition.

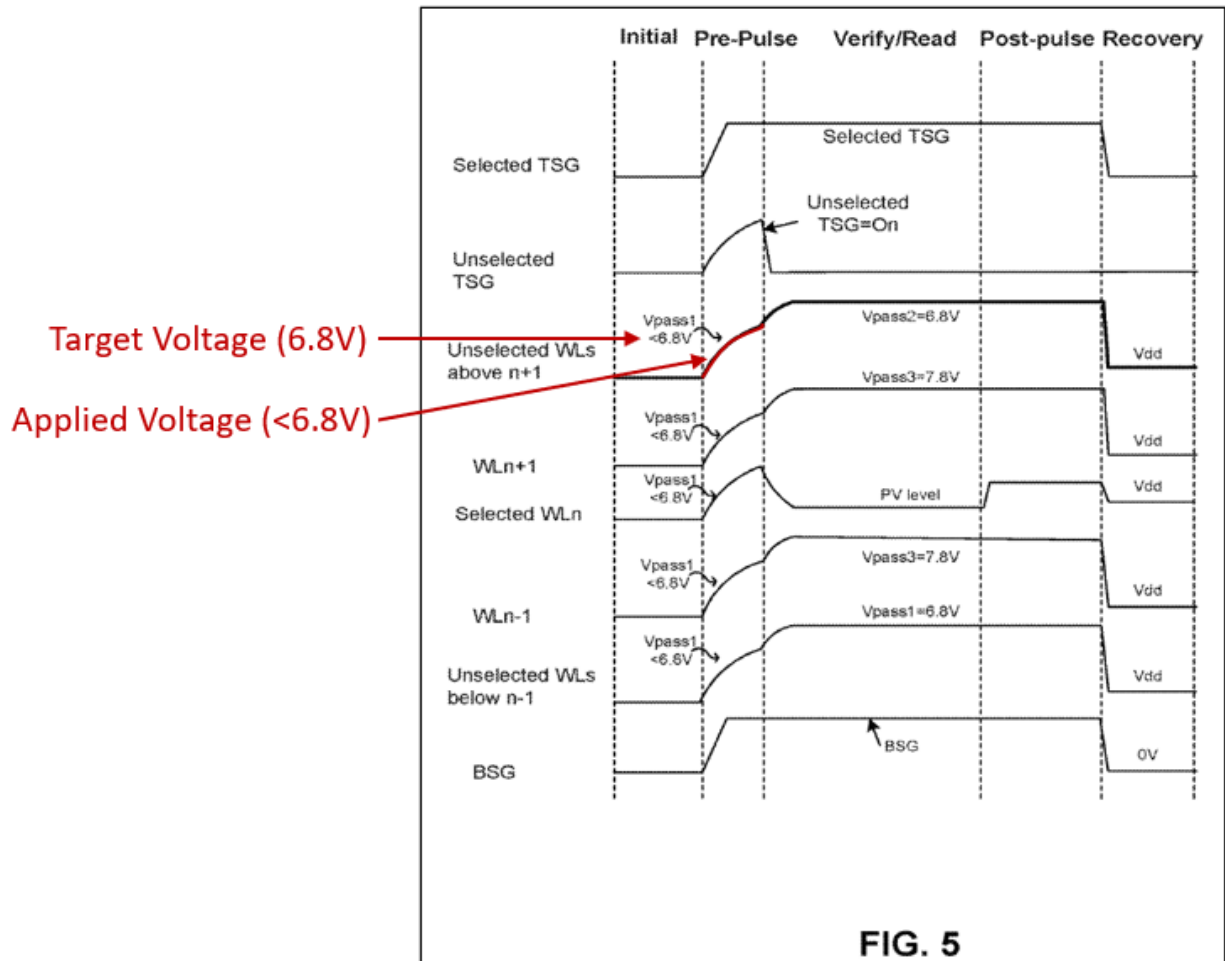
A. Ground 1 (Obviousness): Hongtao in View of Yu Does Not Disclose or Render Obvious Applying “a First Bias Voltage” and “a Second Bias Voltage” on the Gate Terminal of a Not Programmed Memory Cell “Wherein the Second Bias Voltage Is Smaller than the First Bias Voltage”

Hongtao in view of Yu does not disclose or render obvious limitations [1.b] and [1.d] because Fig. 2 of Hongtao would not have suggested to a POSITA that an applied “second bias voltage on a gate terminal” is smaller than an applied “first bias voltage on a gate terminal” as required by the ’957. *See* Pet., 39-40. Petitioner relies exclusively on Fig. 2 of Hongtao as purportedly disclosing this limitation (*id.*), but Figure 2 of Hongtao depicts voltages applied to word lines, not the resulting voltages that are applied on gate terminals of the memory cells. The ’957 draws a key distinction between an applied “bias voltage on a gate terminal,” as distinct from a value which may be applied to the coupled word lines, which the Petition fails to address. In ignoring this distinction, Petitioner misinterprets Hongtao, and has failed to show that a POSITA would have understood Fig. 2 of Hongtao to disclose or render obvious that an applied “second bias voltage on a gate terminal” is smaller than an applied “first bias voltage” as required by the Challenged Claims.

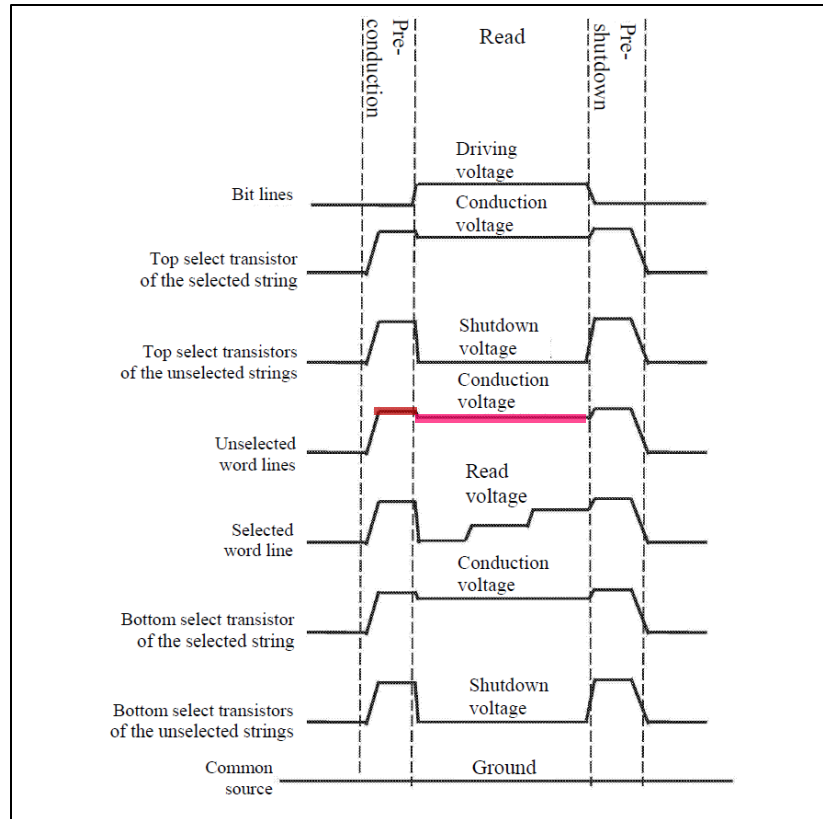
Claim 1 of the ’957 recites processing circuitry configured to **“apply, in the pre-verify stage, a first bias voltage on a gate terminal of at least one memory cell of the first memory cell string that is not programmed”** (Element [1.b]); and **“apply, in the verify stage, a second bias voltage on the gate terminal of the at**

least one memory cell of the first memory cell string that is not programmed,
wherein the second bias voltage is smaller than the first bias voltage” (Element [1.d]). These limitations are common to each of the Challenged Claims by virtue of their dependency on claim 1 of the ’957.

As explained in Section II, the claimed invention of the ’957 improves over conventional systems in part because, by applying “a lower bias voltage” on a gate terminal of an unprogrammed memory cell in the verify stage as compared to the pre-verify stage, “the gradient of the channel potential of the selected memory cell string can be reduced,” which prevents hot carrier injection (HCI) between the selected memory cell and neighboring memory cells. ’957, 12:63-13:4 (“HCI cannot be generated from the selected memory cell to the upper adjacent memory cell of the selected in the selected memory cell string.”). The ’957 also distinguishes between the voltages that may be applied through word line layers during a pre-pulse stage, and the bias voltages applied on the gate terminals of the memory cells that develop over time as a result. *See, e.g.*, ’957, 11:68-12:9, 12:10-27. For example, Fig. 5 of the ’957 illustrates an example where a short pre-pulse period prevents the applied “bias voltages” from developing fully, resulting in them being “less than a target value, such as 6.8 volts” during the pre-pulse period. ’957, 12:18-19.



Petitioner seemingly concedes that Hongtao’s text does not describe applying a “second bias voltage” that is smaller than a “first bias voltage” to the gate terminal of an unprogrammed memory cell, and instead argues that this subject matter is disclosed solely by the depiction of the “**pre-conduction voltage**” and “**conduction voltage**” in Figure 2 of Hongtao (reproduced below). *See* Pet. 39-40.



Petitioner incorrectly suggests that this figure, standing alone, discloses the use of processing circuitry configured to “**apply, in the pre-verify stage, a first bias voltage on a gate terminal of at least one [not programmed] memory cell,**” and “**apply, in the verify stage, a second bias voltage on the gate terminal of the at least one [not programmed] memory cell** ... wherein the second bias voltage is smaller than the first bias voltage,” as required by the Challenged Claims. Pet. 39-40. Petitioner’s argument ignores the relevant legal standard and mischaracterizes Hongtao’s actual disclosure.

Specifically, the Petition argues that Fig. 2 of Hongtao satisfies these claims because “the voltage signal applied to the unselected word lines ramps down from

the pre-conduction voltage to reach the conduction voltage,” but that is not what the Challenged Claims require. Pet. 39-40. Rather, the claims are explicitly directed to the actual voltages applied *on a gate terminal* of the memory cell itself.

By comparison, Fig. 2 of Hongtao describes voltages applied through word lines, rather than the resulting voltages applied to the gate terminals of corresponding memory cells. Moreover, drawings can be relied on for invalidity purposes “only if the prior art features are clearly disclosed,” and Fig. 2 of Hongtao does not disclose or otherwise suggest the claimed subject matter of the ’957. *PlaSmart, Inc. v. Kappos*, 482 F. App’x 568, 572 (Fed. Cir. 2012) (emphasis added); *see also* MPEP 2125 (“drawings must be evaluated for what they reasonably disclose and suggest to one of ordinary skill in the art”). Indeed, Hongtao explicitly states that the conduction and read voltages shown are applied to the “unselected word line and the selected word line.” Hongtao [0023], [0025]. Hongtao does not disclose the resulting bias voltages applied on the gate terminals of the memory cells, nor does Hongtao provide the necessary details, such as the duration of the pre-conduction period, to infer how the resulting voltages on the gate terminals of the memory cells would develop over time. *Cf.* ’957, 11:58-12:9, 12:10-27 (discussing that bias voltages need sufficient time to develop fully).

Similarly, the Petitioner has not even attempted to address what—if anything—a POSITA could have determined about the applied bias voltages on the

gate terminals of the unprogrammed memory cells from the target values depicted in Fig. 2 of Hongtao. Petition and Dr. Liu have simply overlooked the distinction drawn in the '957 between voltages that may be applied through word line layers, and the actual bias voltages applied on the gate terminals of the memory cells that develop over time as a result. *See generally* Section II.

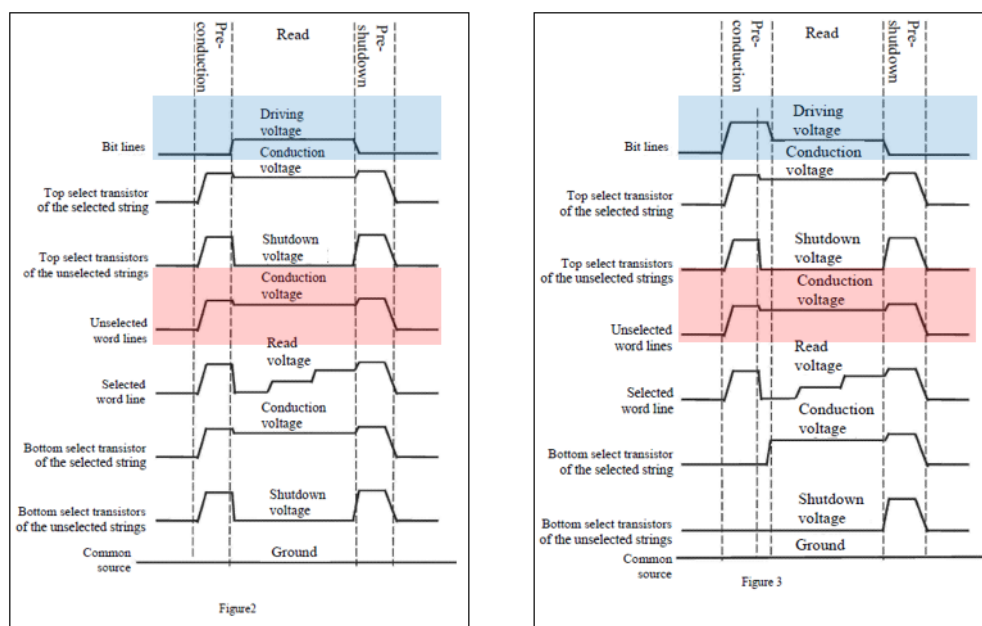
The Petition's citation to paragraph [0026] of Hongtao does not address this fundamental deficiency, or otherwise suggest that a POSITA would have understood Fig. 2 of Hongtao to be illustrating applied bias voltages "on a gate terminal of a [not programmed] memory cell," rather than a voltage applied to the word line layer. *See* Pet. 40.

Petitioner and Dr. Liu also mischaracterize paragraph [0026] of Hongtao as disclosing that the voltage signal illustrated in Figure 2 for the unselected word lines is lowered because "the greater the conduction voltage, the greater the read disturbance." *See* Pet. 22, 40; Liu ¶120 (citing Hongtao [0026]). That quote, which the Petition presents out of context, says nothing about the bias voltages that develop on the gate terminals of the memory cells within the device. Rather, it describes problems in the embodiment of Figure 2 arising from having a large difference between a "conduction voltage" and a bit line "driving voltage":

Read interference is positively related to the voltage causing read interference. The greater the voltage, the stronger the read interference. Therefore, the greater the conduction voltage, the greater the read

disturbance to the memory cell. Therefore, in this specific embodiment, *the read interference caused by the "conduction voltage - driving voltage" suffered by the unselected memory cells on the selected string is smaller than the read interference suffered by the memory cells on the unselected string. In order to improve the accuracy of memory reading, it is necessary to further reduce the read interference suffered by the memory cells on the unselected string.*

Hongtao [0026]. Hongtao proceeds to describe the alternative embodiment of Figure 3 to "further reduce the read interference" as compared to the embodiment of Figure 2. Hongtao [0027]-[0028], Fig. 3. But the **conduction voltage applied to the unselected word lines**—i.e., the voltage that Petitioner relies on—is depicted exactly the same in both Figures 2 and 3, confirming that Hongtao [0026] is not suggesting lowering the conduction voltage to address the interference problems of Figure 2. *Compare Hongtao Fig. 2 and Fig. 3.*



The above quote from Paragraph 26 does not support Petitioner's purported interpretation and is irrelevant because it says nothing about the resulting voltages on the gate terminals of the memory cells.

Yu likewise does not disclose applying multiple different bias voltages, and Petitioner does not allege that it does. Therefore, Yu is unable to address the deficiencies in Hongtao. Petitioner relies on Yu as allegedly teaching certain aspects of programming operations, including the use of a programming order. *See* Pet. 22, 29, 31, 33-34. But Yu is silent as to the bias voltages applied during a pre-verify and verify stage of a verification operation, and the Petition fails to identify any disclosure in Yu that would teach or otherwise suggest applying different bias voltages on a gate terminal of an unprogrammed memory cell, "wherein the second bias voltage is smaller than the first bias voltage," as required by the Challenged Claims.

For at least the reasons provided above, Petitioner's Ground 1 fails because Hongtao and Yu, alone or in combination, fail to disclose or render processing circuitry configured to "apply ... a first bias voltage on a gate terminal of at least one memory cell of the first memory cell string that is not programmed," and "a second bias voltage on the gate terminal of the at least one memory cell of the first memory cell string that is not programmed, wherein the second bias voltage is

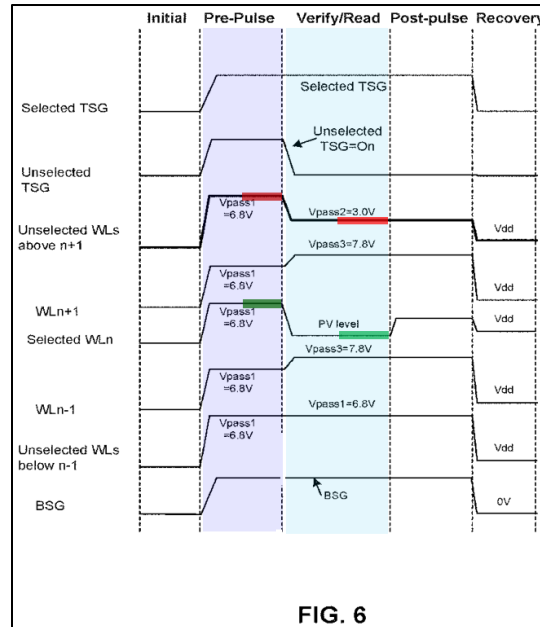
smaller than the first bias voltage” as required by elements [1.b] and [1.d] of the Challenged Claims.

B. Ground 2 (Anticipation): Suzuki Does Not Disclose Applying a First Verify Voltage and First Bias Voltage in a “Pre-Verify” Stage, or Applying a Second Bias Voltage in a “Verify” Stage “Wherein the Second Bias Voltage Is Smaller than the First Bias Voltage”

Suzuki does not disclose at least limitations [1.b] and [1.d] of the Challenged Claims. Specifically, Suzuki’s “Vpass” voltage, which Petitioner identifies as purportedly equivalent to the claimed “first bias voltage,” is not applied in a “pre-verify stage” as required by the Challenged Claims. *See* Pet. 74-85. Moreover, Petitioner’s assertion that the identified voltages occur during a “pre-verify” stage contradicts both Suzuki’s own disclosure as well as the plain and ordinary meaning of the claim language. Accordingly, Petitioner’s anticipation argument based on Suzuki fails.

Claim 1 recites processing circuitry configured to; **“apply, in a pre-verify stage, a first bias voltage on a gate terminal of at least one memory cell of the first memory cell string that is not programmed”** (Element [1.b]); and **“apply, in the verify stage, a second bias voltage on the gate terminal of the at least one memory cell of the first memory cell string that is not programmed, wherein the second bias voltage is smaller than the first bias voltage”** (Element [1.d]). These limitations are common to each of the Challenged Claims by virtue of their dependency on claim 1 of the ’957.

As explained in Section II, the claimed invention of the '957 recites an improved approach for performing verification operations using a two-stage approach that mitigates HCI and ESUM losses. As illustrated in Fig. 6, that includes preparing the memory string for the verification operation by applying a **first bias voltage** to a not programmed memory cell during a **pre-verify stage**, and then applying a **second bias voltage** (lower than the first verify voltage) during the subsequent **verify stage**. '957, 1:58-2:8, 6:37-49, 17:32-56.

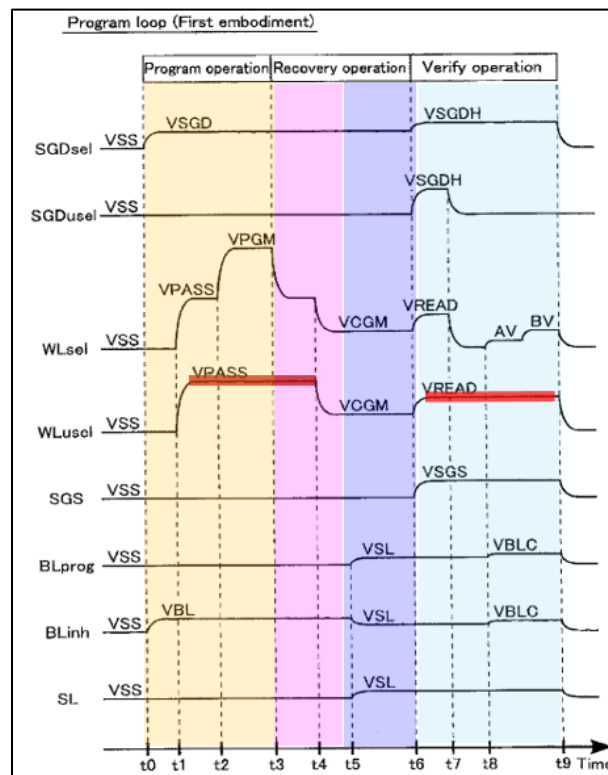


'957, Figure 6 (annotated); *see also* Section II.

Unlike the claimed invention of the '957, Suzuki does not disclose a first bias voltage during a “pre-verify stage,” wherein the first bias voltage is larger than the second bias voltage. Petitioner argues only that Suzuki anticipates the Challenged Claims under 35 U.S.C. §102 and does not raise any obviousness arguments under

§103. *See* Pet. 7-8. “A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference.” *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631 (Fed. Cir. 1987).

Suzuki discloses a programming loop that is divided into multiple distinct time periods. As shown in Fig. 11, “time t0 to time t3 corresponds to a **program operation**,” “time t3 to time t6 corresponds to a recovery operation,” and “time t6 to time t9 corresponds to a **verify operation**.” Suzuki, [0131]. The recovery operation is a combination of “**an end operation of the program operation** and the **ready operation of the verify operation**.” Suzuki, [0131].



Suzuki, Fig. 11 (annotated).

Petitioner incorrectly argues that the “**VPASS**” signal applied from time period t3-t4 is equivalent to the claimed “first bias voltage” applied during a “pre-verify stage.” *See* Pet. 79-82. Petitioner pointed to **VPASS** because it needed to find a voltage larger than **VREAD** in order to satisfy Element [1.d]. Petitioner’s argument fails at least because the time period from t3-t4 is not part of Suzuki’s “**ready operation of the verify operation**” (i.e., is not part of a pre-verify operation as the Petition seems to suggest). Rather, the time period from t3-t4 is described by Suzuki as an “**end operation of the program operation.**” Suzuki, [0131]. Petitioner does not address this disclosure.

Suzuki’s program operation—including the end operation at t3-t4—does not qualify as a “pre-verify stage” under any reasonable interpretation of that term. For example, “**VPASS**” of the program operation does not prepare the device for the purported “verify stage” from t6-t9. *See* Suzuki [0131], Fig. 11. A comparison between Suzuki and the ’957 illustrates the stark difference between the two approaches. In the ’957, the bias voltage during the verify/read stage is preceded by a *larger* bias voltage. ’957, Fig. 6. In Suzuki, in contrast, the VREAD voltage is preceded by a *smaller* VCGM voltage during the “read operation of the verify operation.” Suzuki, Fig. 11, [0131].

Even if Petitioner had instead tried to map the claimed “first bias voltages” to Suzuki’s “VCGM” voltage that is applied during the “**ready operation of the verify**

operation,” Suzuki still would not anticipate the Challenged Claims. *See* Suzuki, [0131], [0138]-[0139]. The Challenged Claims require applying “a second bias voltage” during the verify stage that is “smaller than the first bias voltage.” But Suzuki discloses the opposite, explicitly stating that “**VREAD**” (i.e., the purported “second bias voltage” identified by Petitioner) “is a higher voltage than VCGM.” Suzuki, [0142].

For at least the reasons provided above, Petitioner’s proposed mapping of Suzuki fails to show a “first bias voltage” applied during a “pre-verify stage” as required by the Challenged Claims. Moreover, even if Petitioner had modified its proposed mapping to point to voltages that are applied during Suzuki’s ready operation immediately prior to the purported verification stage (e.g., if Petitioner had pointed to VCGM from t5 to t6), Suzuki still fails to disclose “wherein the second bias voltage is smaller than the first bias voltage” as required by Element [1.d]. Accordingly, Petitioner has failed to show that Suzuki anticipates the Challenged Claims.

C. Ground 3 (Obviousness): Costa in View of Seo Does Not Disclose or Render Obvious Applying “a First Bias Voltage” and “a Second Bias Voltage” on the Gate Terminal of a Not Programmed Memory Cell “Wherein the Second Bias Voltage Is Smaller than the First Bias Voltage”

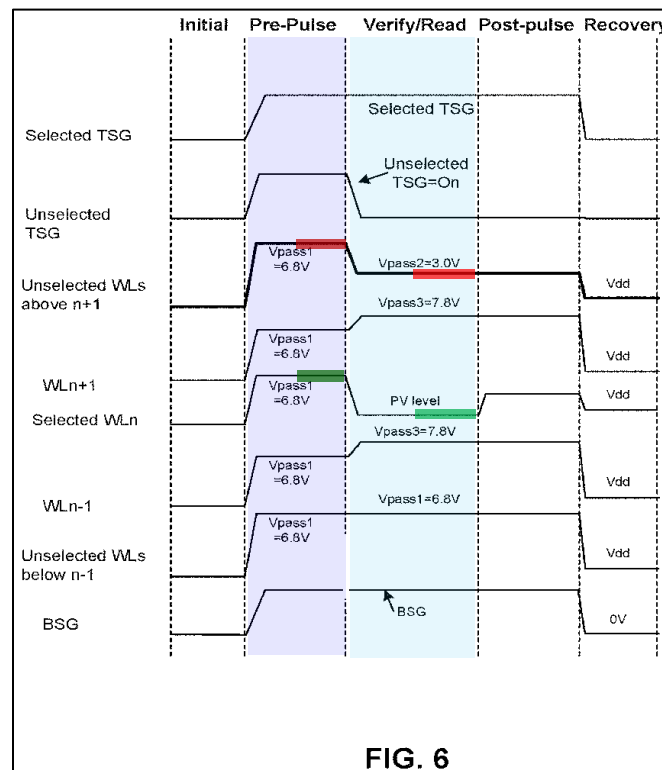
Costa in view of Seo does not disclose or render obvious limitations [1.b] and [1.d] because the references, both alone or in combination, do not disclose or render

obvious applying distinct bias voltages on a gate terminal of a not-programmed memory cell such that “the second bias voltage is smaller than the first bias voltage” as required by the Challenged Claims. Petitioner does not show that the voltages disclosed in Costa and Seo are applied to a gate terminal of a memory cell. Moreover, Petitioner and Dr. Liu’s conclusory assertion that a POSITA would have been motivated to selectively apply Costa’s purported teachings to only a verify stage (and not a pre-verify stage) is inconsistent with Costa’s disclosure and contradicts the basic operating principles NAND memory strings. *See* Pet. 103-112. Petitioner’s argument is an attempt to impermissibly “reconstruct the applicant’s invention only with the benefit of hindsight.” *See Netflix*, 80 F.4th at 1359; *see also Cheese Sys.*, 725 F.3d at 1352 (obviousness “cannot be based on the hindsight combination of components selectively culled from the prior art to fit the parameters of the patented invention”).

Claim 1 of the ’957 recites processing circuitry configured to “**apply, in the pre-verify stage, a first bias voltage on a gate terminal of at least one memory cell of the first memory cell string that is not programmed**” (Element [1.b]); and “**apply, in the verify stage, a second bias voltage on the gate terminal of the at least one memory cell of the first memory cell string that is not programmed, wherein the second bias voltage is smaller than the first bias voltage**” (Element

[1.d]). These limitations are common to each of the Challenged Claims by virtue of their dependency on claim 1 of the '957.

As explained in Section II, the '957 distinguishes between the voltages that may be applied through word line layers during a pre-pulse stage, and the bias voltages applied on the gate terminals of the memory cells that develop over time as a result. *See, e.g., '957, 11:68-12:9, 12:10-27.* Within that context, the claimed invention of the '957 improves over conventional systems, in part, by applying a **first bias voltage** on a gate terminal of a not-programmed memory cell during a **pre-verify stage**, and then applying a **second bias voltage** that is smaller than the first bias voltage during a later **verify stage**. '957, 1:58-2:8, 6:37-49, 17:32-56, Fig. 6.

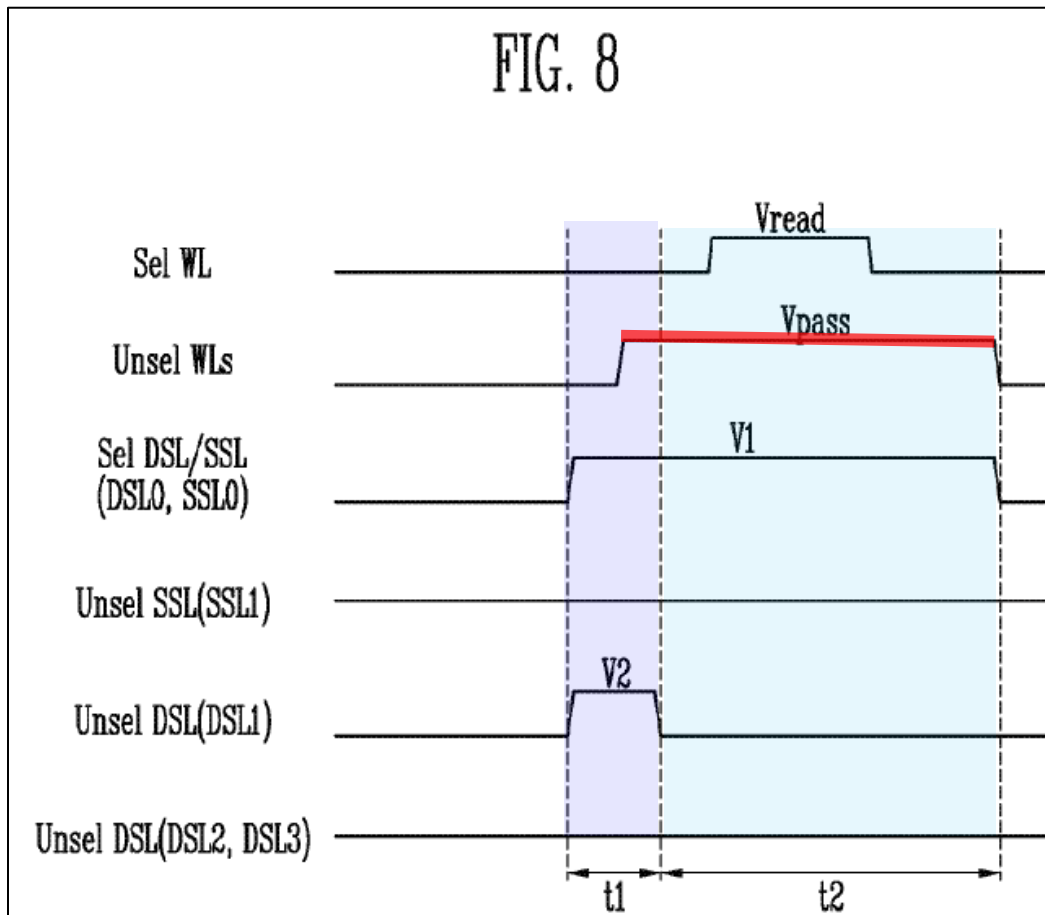


But unlike the '957, neither Costa nor Seo teaches or otherwise suggests that the bias voltage applied on a gate terminal of a not-programmed memory cells changes over time—nor does the proposed combination.

First, Costa does not disclose the use of separate “verify” and “pre-verify” stages for a verify operation, or that different voltage levels would be used during a “verify” and a “pre-verify” stage as required by the '957. While Costa discloses that a lower “pass voltage” can be used for *unprogrammed memory cells* as compared to *programmed memory cells*, Costa fails to disclose any difference in the “pass voltage” applied to any given memory cell *at different stages of a verification process*. See Costa [0121]-[0122], [0147]. As explained by Costa, programming a memory cell increases the threshold voltage (*see* Costa [0082]), and because the unprogrammed cells are in an erased state, “lower read pass voltage VreadL can be used while still ensuring that these memory cells operate as pass gates” (Costa [0122]). But that does not teach separate “verify” and “pre-verify” stages, let alone using different voltage levels during a “verify” and a “pre-verify” stage. In Costa, the “pass voltage” applied to a given memory cell is always constant.

Second, Seo similarly fails to disclose the use of distinct bias voltages during a “pre-verify stage” and a “verify stage,” as required by the Challenged Claims. Seo discloses that a “read” operation can be divided into “time period t1” and “time

period t2,” and that a “pass voltage **V_{pass}** may be applied to unselected word lines” during both a portion of time period t1 as well as time period t2.” Seo, [0087]-[0090].



Petitioner seemingly concedes that Seo does not disclose the use of distinct values of “**V_{pass}**” during these different time periods, and that Seo fails to demonstrate the use of two distinct bias voltages on not-programmed word lines. *See* Pet. 26-27, 103. Instead, Petitioner improperly points to Seo’s use of “**V_{pass}**” during time period t1 as equivalent to the claimed “first bias voltage,” and incorrectly asserts that it would have been obvious in view of Costa for a distinct value of **V_{pass}**

to be applied to the unselected word lines only during time period t2 (i.e., a distinct “second bias voltage”). *See* Pet. 26-27, 103-126.

Petitioner and Dr. Liu have failed to demonstrate why a POSITA would have been motivated to selectively apply Costa’s purported teachings (i.e., the use of a lower **V_{pass}** value) to only the time period t2, and not the time period t1. The Petition improperly argues that Costa’s purported teachings of using a “low V_{pass} voltage[s]” would apply only in the second time period, while ignoring that Costa itself provides no such teaching of selectively lowering pass voltages based on the time period. *See* Pet. 112, 126-129. Indeed, to the extent that it would be advantageous to use lower V_{pass} voltages as purportedly taught by Costa (i.e., using lower pass voltages on certain unprogrammed memory cells (Costa, [0112])), that purported teaching is equally applicable in both time periods and Petitioner has not shown that adjusting the voltage in only one of the periods would have been obvious.

The Petition attempts to justify its proposed combination with the faulty and unsupported argument that Seo requires a “high V_{pass} voltages” on all unselected memory cells during the first time period. Pet. 128 (citing Liu ¶308). As an initial matter, Seo does not actually state that a “high V_{pass} voltage” must be applied. Moreover, both Petitioner and Dr. Liu fail to articulate why a single value of V_{pass} must be used for all memory cells regardless of their programmed state (i.e., why Costa’s teachings would be ignored during the initial time period, such that a high

Vpass voltage would be applied to even unprogrammed memory cells), or why Costa's teachings would suddenly become inapplicable. At most, Dr. Liu argues that a "full Vpass voltage" would be required during the first time period because "a Vpass voltage on unselected memory cells on the drain side of the selected memory cell needs to be high enough to account and compensate" for voltage building on the "source of [the] transistor" during a pre-conditioning period. Liu ¶308. But Dr. Liu fails to cite any portion of Seo's disclosure for that proposition, and even taking Dr. Liu's argument at face value, Costa's purported teachings (i.e., that a lower value of Vread can be used on unprogrammed memory because of their lower threshold voltage) *would still apply to both time periods equally*, including the first time period—again demonstrating that Petitioner is using hindsight and has not shown that adjusting only the verify voltage would have been obvious.

Thus, contrary to Petitioner's assertions, a POSITA would not have been motivated to selectively apply Costa's teachings as they have proposed. Rather, Petitioner's and Dr. Liu's selective application of Costa's teachings is unsupported, has no justification in the references themselves, and is little more than an attempt to impermissible hindsight to reconstruct the claimed invention.

Additionally, unlike the '957, Costa and Seo do not distinguish between the voltages that may be applied through word line layers during a pre-pulse stage, and the bias voltages applied on the gate terminals of the memory cells that develop over

time as a result. *See, e.g.*, '957, 11:68-12:9, 12:10-27. To the extent that Costa and Seo purportedly disclose certain voltages applied to word lines, they do not disclose that those voltages are also applied to the gate terminals of the corresponding memory cells, nor does Petitioner present any arguments to suggest that the two would have obviously been the same.

VII. CONCLUSION

The Petition should be denied institution, as Petitioner has failed to establish a likelihood that it would prevail with respect to any of the Challenged Claims based on the grounds presented in the petition.

Dated: August 12, 2024

Respectfully submitted,

ROPES & GRAY LLP

By: /James L. Davis, Jr./

James L. Davis, Jr.

Reg. No. 57,325

ROPES & GRAY LLP

1900 University Avenue, 6th Floor

East Palo Alto, CA 94303-2284

Telephone: +1-650-617-4794

James.L.Davis@ropesgray.com

Andrew T. Radsch

(*pro hac vice* forthcoming)

ROPES & GRAY LLP

1900 University Avenue, 6th Floor

East Palo Alto, CA 94303-2284

Telephone: +1-650 617 4763

Andrew.Radsch@ropesgray.com

Christopher M. Bonny

Reg. No. 63,307

ROPES & GRAY LLP

1900 University Ave., 6th Floor

East Palo Alto, CA 94303-2284

Telephone: +1-650-617-4011

Christopher.Bonny@ropesgray.com

Abed R. Balbaky
Reg. No. 76,154
ROPES & GRAY LLP
1211 Avenue of the Americas
New York, NY 10036-0003
Telephone: +1-212-841-5797
Abed.Balbaky@ropesgray.com

*Attorneys for Patent Owner, Yangtze
Memory Technologies Co. Ltd.*

CERTIFICATE OF WORD COUNT

The undersigned certifies that the foregoing PATENT OWNER'S PRELIMINARY RESPONSE UNDER 37 C.F.R. § 42.107 complies with the type-volume limitation in 37 C.F.R. § 42.24(b)(1). According to the word-processing system's word count, the brief contains 8,517 words, excluding the parts of the brief exempted by 37 C.F.R. § 42.24.

Dated: August 12, 2024

Respectfully submitted,

By: /Abed R. Balbaky/
Abed R. Balbaky
Reg. No. 76,154
ROPES & GRAY LLP

CERTIFICATE OF SERVICE

The undersigned certifies that the foregoing PATENT OWNER'S PRELIMINARY RESPONSE UNDER 37 C.F.R. § 42.107 was served in its entirety by filing through the Patent Trial and Appeal Case Tracking System (P-TACTS), as well as providing a courtesy copy via e-mail to the following attorneys of record for Petitioner listed below:

Lead Counsel	Back-up Counsel
Jeremy Jason Lang Registration No. 73,604 (jlang@orrick.com) Postal & Hand-Delivery Address: Orrick, Herrington & Sutcliffe LLP 1000 Marsh Road Menlo Park, CA 94025 T: 650-614-7400; F: 650-614-7401 P52PTABDocket@orrick.com PTABDocketJL2@orrick.com PTABDocketJ3B3@orrick.com T61PTABDocket@orrick.com PTABDocketJ1H1@orrick.com micron-ymtc_ohs@orrick.com	Jared Bobrow <i>Pro Hac Vice</i> (jbobrow@orrick.com) K. Patrick Herman Registration No. 75,018 (pherman@orrick.com) Travis Jensen Registration No. 60,087 (tjensen@orrick.com) Johannes Hsu Registration No. 74,689 (johanneshsu@orrick.com)
<i>Counsel for Petitioner Micron Technology, Inc.</i>	

Dated: August 12, 2024

By: /Jonathan Bradford/
Name: Jonathan Bradford

ROPES & GRAY LLP