

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner,

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,
Patent Owner.

IPR2024-00792
Patent 11,468,957 B2

Before JO-ANNE M. KOKOSKI, KIMBERLY McGRAW, and
MICHAEL T. CYGAN, *Administrative Patent Judges*.

KOKOSKI, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

Micron Technology, Inc. (“Petitioner”) filed a Petition to institute an *inter partes* review of claims 1–6 of U.S. Patent No. 11,468,957 B2 (“the ’957 patent,” Ex. 1001). Paper 1 (“Pet.”). Yangtze Memory Technologies Company, Ltd. (“Patent Owner”) filed a Preliminary Response. Paper 11 (“Prelim. Resp.”).

Institution of an *inter partes* review is authorized by statute when “the information presented in the petition . . . and any response . . . shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” 35 U.S.C. § 314 (2018); *see also* 37 C.F.R. § 42.4 (2023). For the reasons discussed below, we determine that Petitioner establishes a reasonable likelihood of prevailing with respect to the unpatentability of at least one claim of the ’957 patent. Accordingly, we institute an *inter partes* review of claims 1–6 of the ’957 patent.

A. *Real Parties in Interest*

Petitioner identifies “Micron Technology, Inc. and its subsidiaries, including Micron Consumer Products Group LLC” as the real parties in interest. Pet. 4. Patent Owner identifies itself as the real party in interest. Paper 3 (Mandatory Notice), 2.

B. *Related Matters*

The parties indicate that the ’957 patent is asserted in *Yangtze Memory Techs. Co., Ltd. v. Micron Tech. Inc.*, Case No. 3:23-cv-05792-RFL (N.D. Cal.). Pet. 4; Paper 4, 2.

C. *The ’957 Patent*

The ’957 patent, titled “Architecture and Method for NAND Memory Operation,” relates to “apparatuses and methods for verifying/reading

memory cells of a 3D-NAND memory device to reduce hot carrier injection (HCI)-induced edge summation (ESUM) loss, and reduce power consumption during verifying/reading the memory cells of the 3D-NAND memory device.” Ex. 1001, code (54), 1:44-49. The memory device includes a first memory cell string and second memory cell string, each of which includes a bottom-select-gate (“BSG”) transistor, memory cells, and a top-select-gate (“TSG”) transistor connected in series. *Id.* at 4:12–20. The ’957 patent teaches that processing circuitry is configured to apply, in a pre-verify stage, a first verify voltage on a gate terminal of a selected memory cell of the first memory cell string, where the selected memory cell can be programmed and arranged between a first adjacent memory cell and a second adjacent memory cell. *Id.* at 4:20–25. The processing circuitry also applies, in the pre-verify stage, a first bias voltage on a gate terminal of at least one memory cell of the first memory cell string that is not programmed. *Id.* at 4:25–29. The ’957 patent further teaches that, in the verify stage, the processing circuitry applies a second verify voltage on the gate terminal of the selected memory cell of the first memory cell string, and a second bias voltage on the gate terminal at the at least one memory cell of the first memory cell string that is not programmed. *Id.* at 4:29–35. The second bias voltage can be smaller than the first bias voltage. *Id.* at 4:35–36.

D. Illustrative Claim

Petitioner challenges claims 1–6 of the ’957 patent. Claim 1, the only independent claim challenged, is illustrative of the claimed subject matter and is reproduced below.

1. [1.PRE] An apparatus for reading a memory device including a first memory cell string and a second memory cell string, the first memory cell string including a bottom-select gate (BSG) transistor, memory cells, and top-select gate (TSG)

transistor that are connected in series, the second memory cells string including a BSG transistor, memory cells, and a TSG transistor that are connected in series, the apparatus comprising:

[1.A] processing circuitry configured to:

- [1.A.i] apply, in a pre-verify stage, a first verify voltage on a gate terminal of a selected memory cell of the first memory cell string, the selected memory cell being programmed and arranged between a first adjacent memory cell and a second adjacent memory cell;
- [1.A.ii] apply, in the pre-verify stage, a first bias voltage on a gate terminal of at least one memory cell of the first memory cell string that is not programmed;
- [1.A.iii] apply, in a verify stage, a second verify voltage on the gate terminal of the selected memory cell of the first memory cell string; and
- [1.A.iv] apply, in a verify stage, a second bias voltage on the gate terminal of the at least one memory cell of the first memory cell string that is not programmed, wherein the second bias voltage is smaller than the first bias voltage.

Ex. 1001, 17:32–56 (bracketed material added).

E. Asserted Grounds

Petitioner asserts that claims 1–6 would have been unpatentable on the following grounds:

Claim(s) Challenged	35 U.S.C. §	Reference(s)/Basis
1–6	103 ¹	Hongtao, ² Yu ³
1–6	102	Suzuki ⁴
1–6	103	Costa, ⁵ Seo ⁶

Pet. 8. Petitioner relies on the Declaration of David Kuan-Yu Liu (Ex. 1003) in support of its contentions.

II. ANALYSIS

A. Level of Ordinary Skill in the Art

Petitioner contends that a person of ordinary skill in the art (“POSITA”) would have had “a bachelor of science degree in electrical engineering or a similar discipline” with “4–5 years of professional experience working with (e.g., researching, designing, or developing) NAND flash memory devices (including issues relating to the operation, e.g., reading of said devices), or an equivalent level of skill, knowledge, and experience (e.g., an advanced degree may replace some of the professional experience).” Pet. 19–20 (citing Ex. 1003 ¶¶ 35–39). At this stage of the proceeding, Patent Owner neither responds to Petitioner’s proposed

¹ The Leahy-Smith America Invents Act (“AIA”), Pub. L. No. 112–29, 125 Stat. 284 (2011), revised 35 U.S.C. §§ 102 and 103 effective March 16, 2013. Because the ’957 patent has an effective filing date after March 16, 2013 (Ex. 1001, codes (22), (63)), we refer to the AIA version of Sections 102 and 103.

² Hongtao, CN 109065091 A, published Dec. 21, 2018 (Ex. 1005).

³ Yu, US 2019/0198117 A1, published June 27, 2019 (Ex. 1006).

⁴ Suzuki, US 2021/0082505 A1, published Mar. 18, 2021 (Ex. 1007).

⁵ Costa, US 2018/0012667 A1, published Jan. 11, 2018 (Ex. 1008).

⁶ Seo, US 2021/0027848 A1, published Jan. 28, 2021 (Ex. 1009).

definition, nor provides a definition of its own. *See generally*, Prelim. Resp. Petitioner’s undisputed proposed definition appears to be consistent with the cited prior art and the disclosure of the ’957 patent, and we adopt it for purposes of this Decision. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001) (explaining that specific findings regarding ordinary skill level are not required “where the prior art itself reflects an appropriate level and need for testimony is not shown” (quoting *Litton Indus. Prods., Inc. v. Solid State Sys. Corp.*, 755 F.2d 158, 163 (Fed. Cir. 1985))).

B. Claim Construction

We construe each claim “in accordance with the ordinary and customary meaning of such claim as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent.” 37 C.F.R. § 42.100(b). Under this standard, claim terms are generally given their plain and ordinary meaning as would have been understood by a person of ordinary skill in the art at the time of the invention and in the context of the entire patent disclosure. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1313 (Fed. Cir. 2005) (en banc). Only those terms in controversy need to be construed, and only to the extent necessary to resolve the controversy. *Realtime Data, LLC v. Iancu*, 912 F.3d 1368, 1375 (Fed. Cir. 2019).

Based on the record before us, we determine that no claim term requires express construction for purposes of this Decision.

C. Asserted Obviousness over Hongtao and Yu

Petitioner contends that claims 1–6 would have been obvious over Kim. Pet. 27–74.

1. Overview of Hongtao

Hongtao relates to a reading method of 3D NAND flash memory that reduces read interference and improves the accuracy of read data during the reading process. Ex. 1005 ¶¶ 1, 4.

Figure 1 is reproduced below.

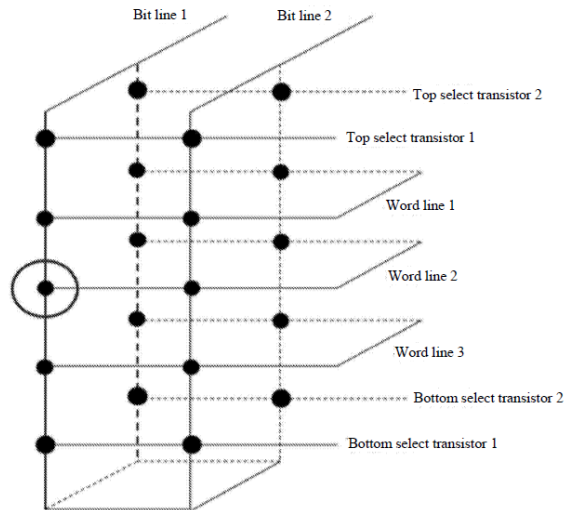


Figure1

Figure 1 is a diagram of one embodiment of the 3D NAND storage structure described in Hongtao. Ex. 1005 ¶ 13. Hongtao's 3D NAND storage structure includes multiple memory cells (black dots) arranged in an array to form multiple memory strings, with a top select transistor connected to the bit line at the top of each memory string. *Id.* ¶ 18. The transistor at the bottom of the memory string is a bottom select transistor. *Id.* Multiple memory cells located in the same layer form a memory row, and the gates of the memory cells located in different memory strings but the same memory row are physically connected and are connected to the same word line. *Id.*

Hongtao teaches that, to read the information of the memory cell circled in Figure 1 above, a driving voltage is applied to bit lines 1 and 2, top select transistor 1 and bottom select transistor 1 of the selected string where

the memory cell is located are turned on, and a conduction voltage is applied to word lines 1 and 3 of the unselected rows other than the row where the memory cell is located in order to run on the channel of the selected string. Ex. 1005 ¶ 19. Top select transistor 2 and bottom select transistor 2 of the unselected string are turned off, the channels of the other unselected string are prevented from being turned on. *Id.* A read voltage is applied to word line 2 of the selected row to read the information in the selected memory cell. *Id.* Hongtao explains that the conduction voltage applied to word lines 1 and 3 of the unselected row will generate a potential via channel coupling in all memory cells connected to word lines 1 and 3, causing hot carrier injection crosstalk that “causes the electrons stored in other unselected memory cells to drift, resulting in changes in the data stored in the unselected memory cells, as well as problems such as drift in the data in the selected memory cell that is read.” *Id.* ¶ 20.

Hongtao describes an embodiment in which there is pre-conduction phase to turn on the channels of the selected and unselected strings before reading the memory cell. *Id.* ¶ 22. In the pre-conduction stage, a pre-conduction voltage is applied to both the selected and unselected word line to turn on the channels of the selected and unselected strings. *Id.* ¶ 23. The top select transistor and the bottom select transistor of both the selected and unselected strings are both turned on, and, at the same time, the bit line remains at a low potential, for example, 0 V. *Id.* The channels are connected to the bit line, and the channel potential will remain at the same low potential as the bit line. *Id.* In this way, Hongtao teaches, the channels of the selected and unselected strings will not generate voltage coupling due to changes in the word line voltage, “thereby avoiding the problem of hot

carrier injection crosstalk caused when a conduction voltage is applied to the word line of an unselected memory cell.” *Id.*

Hongtao further teaches that, in the reading phase, a driving voltage is applied to the bit line, and a disconnection voltage is applied to the top select transistor and bottom select transistor of the unselected string to disconnect the channel of the unselected string from the bit line, and the channel potential of the unselected string is locked to a low potential of 0 V.

Ex. 1005 ¶ 24. A conduction voltage is applied to the top select transistor and the bottom select transistor of the selected string, so that the channel of the selected string is connected to the bit line, and the channel of the selected string is equal to the driving voltage on the bit line. *Id.* ¶ 25. The conduction voltage is applied to the gates of the unselected memory cells on the selected string through the unselected word lines, and the unselected memory cells will withstand read interference caused by the “conduction voltage – driving voltage.” *Id.*

Hongtao explains the read interference is positively related to the voltage causing read interference, such that the read interference is stronger when the voltage is greater. Ex. 1005 ¶ 26. In the embodiment described above, “the read interference caused by the ‘conduction voltage – driving voltage’ suffered by the unselected memory cells on the selected string is smaller than the read interference suffered by the memory cells on the unselected string.” *Id.*

2. Overview of Yu

Yu relates generally to semiconductor integrated circuits, and more particularly describes a method of programming in a nonvolatile memory device, as well as a nonvolatile memory device, capable of reducing disturbance on unselected memory cells during a program operation.

Ex. 1006, ¶¶ 2, 5, 6. Yu describes a memory block provided with a plurality of sub blocks disposed in a vertical direction, which includes a plurality of cell strings each including a plurality of memory cells connected in series. *Id.* ¶ 7. A plurality of intermediate switching transistors are disposed in a boundary portion between two adjacent sub blocks in the vertical direction, each of which is selectively activated based on a program address during a program operation. *Id.* Yu teaches that the program operation can be performed in an upward direction from a lowest word line, such that as the data stored in the memory block increase, the data may be filled in erased cells in the upward direction from bottom to top. *Id.* ¶ 115. Yu also teaches the converse; that is, as the data stored in the memory block increase, the data may be filled in erased cells in the downward direction from top to bottom. *Id.* ¶ 130.

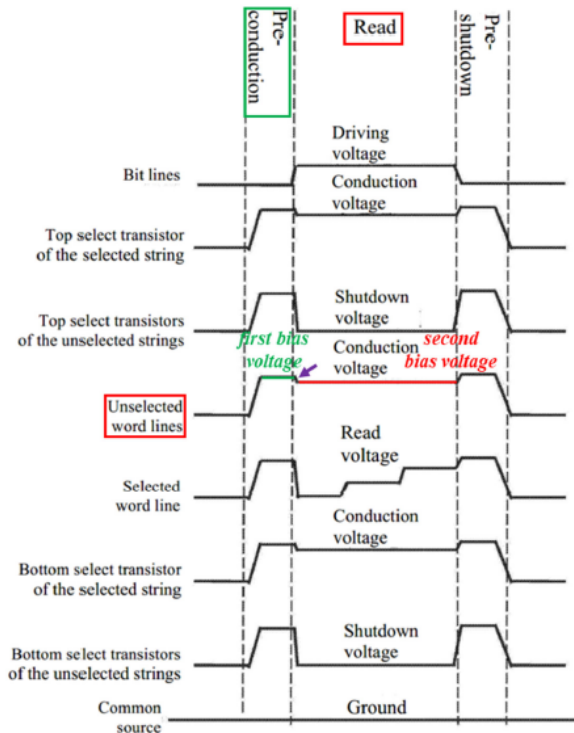
3. *Claim 1*

Petitioner contends that Hongtao and Yu teach all of the limitations of independent claim 1. Pet. 27–40. Patent Owner disagrees, and argues that Hongtao and Yu do not teach or suggest a first bias voltage and a second bias voltage “wherein the second bias voltage is smaller than the first bias voltage” as recited in claim 1. Prelim. Resp. 24–32.

With respect to the “apply, in the pre-verify stage, a first bias voltage on a gate terminal of at least one memory cell of the first memory cell string that is not programmed” limitation of claim 1, Petitioner contends that Hongtao teaches “applying ‘a pre-conduction voltage ... to ... unselected word line[s]’ ‘in the pre-conduction stage.’” Pet. 33 (citing Ex. 1005 ¶ 23) (alterations in original). Petitioner also contends that Hongtao’s “unselected word lines, e.g., word lines 1 and 3, are coupled to unselected cells in the selected memory string.” *Id.* (citing Ex. 1005 ¶ 19). Petitioner also

contends that “Yu discloses ‘the program operation may be performed in an upward direction from a lowest word line ... from bottom to top (B2T program order,)’” so that when the selected memory cell undergoes programming verification, the cells below it have been programmed, and the cells above it are unprogrammed and in an erased state. *Id.* at 34 (citing Ex. 1006 ¶ 115; Ex. 1003 ¶¶ 111–113) (alterations in original). Because “Hongtao would have been understood to disclose longer memory strings (or it would have been obvious),” “additional unprogrammed cells above the adjacent memory cell would also receive the” pre-conduction voltage. *Id.* at 35–36 (citing Ex. 1003 ¶ 113).

Petitioner also contends that “Hongtao further discloses applying a *second bias voltage* (a conduction voltage) on the same cell through the same unselected word lines *in the verify stage* (the read phase).” Pet. 39 (citing Ex. 1006 ¶¶ 19, 25, Fig. 2). Petitioner provides an annotated version of Hongtao’s Figure 2, reproduced below, to illustrate its contentions. *Id.*



Annotated Figure 2 is a timing diagram for reading a 3D NAND memory cell described in Hongtao, with Petitioner’s additions of a green box around the “Pre-conduction” label and a red box around the “Read” label at the top of the diagram, a red box around the “Unselected word lines” label on the left of the diagram, a green line labeled “first bias voltage” and red line labeled “second bias voltage” on portions of the line labeled “Unselected word lines,” and a purple arrow pointing to where the green “first bias voltage” line meets the red “second bias voltage” line. Ex. 1006 ¶ 14. Petitioner contends that, “[a]s indicated by the purple arrow, the voltage signal applied to the unselected word lines ramps down from the pre-conduction voltage to reach the conduction voltage,” and, “[t]hus, *the second bias voltage is smaller than the first bias voltage.*” Pet. 40 (citing Ex. 1003 ¶ 120). Petitioner further contends that “Hongtao explains that ‘the greater the conduction voltage, the greater the read disturbance to the memory

cell,” and “[a]ccordingly, the conduction voltage is reduced during the read phase to reduce read disturbance.” *Id.* (citing Ex. 1006 ¶¶ 24–26; Ex. 1003 ¶¶ 118–120).

Patent Owner responds that “Fig. 2 of Hongtao would not have suggested to a POSITA that an applied ‘second bias voltage on a gate terminal’ is smaller than an applied ‘first bias voltage on a gate terminal’ as required by the ’957” patent. Prelim. Resp. 24. Patent Owner argues that “Fig. 2 of Hongtao describes voltages applied through word lines, rather than the resulting voltages applied to the gate terminals of corresponding memory cells.” *Id.* at 28. Patent Owner argues that “Hongtao does not disclose the resulting bias voltages applied on the gate terminals of the memory cells, nor does Hongtao provide the necessary details, such as the duration of the pre-conduction period, to infer how the resulting voltages on the gate terminals of the memory cells would develop over time.” *Id.*

Hongtao teaches that there is a pre-conduction phase before reading the memory cell in which “a pre-conduction voltage is applied to both the unselected word line and the selected word line to turn on the channels of the selected string and the unselected string.” Ex. 1005 ¶¶ 22–23. Hongtao also teaches that, in the reading phase, “[t]he gates of the unselected memory cells on the selected string are applied with a conduction voltage through the unselected word lines.” *Id.* ¶ 25. Referring to annotated Figure 2 of Hongtao (reproduced above), Dr. Liu explains that, “[a]s indicated by the purple arrow, the voltage applied to the unselected word lines ramps down from the pre-conduction voltage to reach the conduction voltage.” Ex. 1003 ¶ 120. Dr. Liu further explains:

I note Hongtao explains why the unselected word lines voltage is dropped. Specifically, Hongtao discloses that ‘the greater the

conduction voltage, the greater the read disturbance to the memory cell.” [Ex. 1005], [0026]; *see also id.*, [0024]-[0025]. Accordingly, the conduction voltage is reduced during the read phase to reduce read disturbance. I note that Hongtao discloses this read disturbance is a function of the (conductance voltage – *channel* voltage), with the channel voltage being the driving voltage for the selected string and 0V for the unselected string. Lowering the conduction voltage on the unselected word lines alleviates the read disturbance of the unselected memory cell for both the selected string and the unselected string during the longer period of the read phase. Of course, this voltage cannot be dropped to zero, because it has to turn on the transistor. And this is why it drops only slightly.

Id. We are persuaded, on this record, Hongtao’s teachings and Dr. Liu’s explanations adequately establish that the conduction voltage (“second bias voltage”) applied on the gates of the unselected memory cells in the read phase through the unselected word lines in the read stage (“the verify stage”) is smaller than Hongtao’s pre-conduction voltage (“first bias voltage”) applied to the unselected word lines in the pre-conduction phase (“the pre-verify stage”).

In this regard, Patent Owner’s argument that a POSITA would not have understood Hongtao to teach that “the second bias voltage is smaller than the first bias voltage” is based upon attorney argument rather than testimony from the vantage point of one having ordinary skill in the art. Prelim. Resp. 24–31. Moreover, although Patent Owner argues that “Hongtao discloses voltages applied through word lines, rather than the resulting voltages applied to the gate terminals of corresponding memory cells” (*id.* at 28), we note that Hongtao states that “[t]he gates of the unselected memory cells on the selected string are applied with a conduction voltage through the unselected word lines” (Ex. 1005 ¶ 25). *See also* Ex. 1003 ¶ 56 (Dr. Liu testifying, with respect to claim 1 of the ’957 patent’s

recitation of applying a voltage on a gate terminal of a memory cell, “[l]ike its reference to applying a voltage to a memory cell, the respective voltage is applied through a conductor coupled to the corresponding cell or transistor, i.e., a word line coupled to a corresponding memory cell (which in 3D memories, is actually a conductive gate layer).”).

At this stage of the proceeding, Patent Owner does not address Petitioner’s specific contentions with respect to the other limitations of claim 1, or Petitioner’s contentions regarding the motivation to combine Hongtao and Yu. We reviewed Petitioner’s contentions for all the elements of independent claim 1 and the motivation to combine Hongtao and Yu, as well as the supporting evidence. Pet. 27–40, 70–74. Based on the record before us, we are persuaded that Petitioner’s discussions of the particular structures and methods in Hongtao and Yu establish a reasonable likelihood that the combination of Hongtao and Yu teaches or suggests all of the limitations of independent claim 1. *Id.* at 27–40. We are also persuaded that Petitioner adequately establishes, on this record, that a POSITA would have been motivated to combine the teachings of Hongtao and Yu as proposed with a reasonable expectation of success. *Id.* at 70–74.

4. *Claims 2–6*

Petitioner also contends that the combination of Hongtao and Yu teaches all of the elements of claims 2–6 that depend, directly or indirectly, from claim 1. Pet. 40–69. At this stage of the proceeding, Patent Owner does not address Petitioner’s contentions with respect to dependent claims 2–6. We reviewed Petitioner’s contentions with regard to claims 2–6, and are persuaded that Petitioner establishes a reasonable likelihood that the combination of Hongtao and Yu teaches or suggests all of the limitations of these dependent claims as well. *Id.*

D. Asserted Anticipation by Suzuki

Petitioner contends that claims 1–6 are anticipated by Suzuki.

Pet. 74–103. Patent Owner responds that Suzuki does not disclose a first bias voltage during a “pre-verify stage” or the second bias voltage is smaller than the first bias voltage as recited in limitations [1.A.ii] and [1.A.iv] of claim 1. Prelim. Resp. 32–36. Having already determine that Petitioner establishes a reasonable likelihood showing that claims 1–6 would have been obvious over the combination of Hongtao and Yu, we need not address this ground in full. We offer the following comments in response to the parties’ argument and evidence to provide guidance to the parties.

1. Overview of Suzuki

Suzuki “relate[s] generally to a semiconductor memory device.”

Ex. 1007 ¶ 2. Suzuki’s semiconductor memory device includes first and second drain select transistors, first and second source select transistors, first through fourth memory cell transistors, first and second bit lines, first through third select gate line, first and second word lines, and a controller.

Id. ¶ 28. Suzuki teaches that “[t]he controller is configured to execute a write operation including multiple iterations of a program loop,” and “is configured to execute, in the program loop, a program operation, a recovery operation and a verify operation in sequence.” *Id.*

Figure 11 is reproduced below.

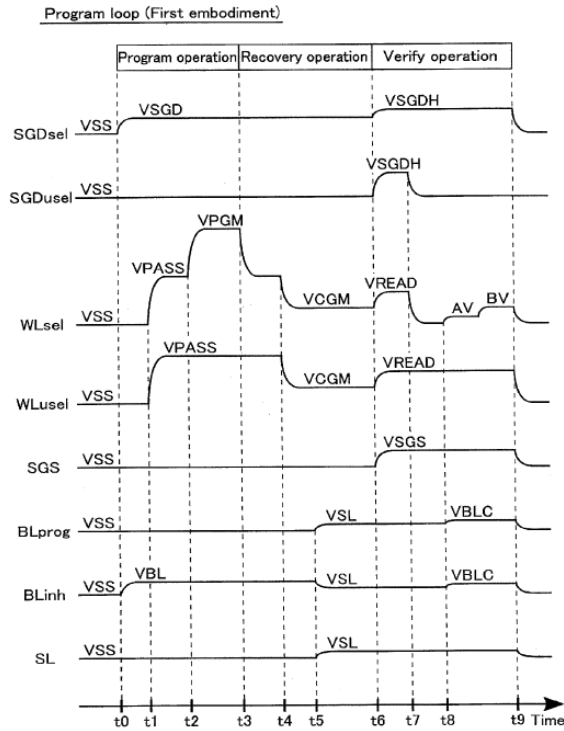


Figure 11 is a timing chart illustrating an example program loop in a write operation of a semiconductor memory device described in Suzuki. Ex. 1007 ¶¶ 14, 130. Suzuki explains that, specifically, Figure 11 shows “changes in respective voltages of the select gate lines SGDsel and SGDusel, the word lines WLsel and WLusel, the select gate line SGS, the bit lines BLprog and BLinh, and the source line SL, in a program loop.” *Id.* ¶ 130. Suzuki further explains that “[i]t is assumed that the respective voltages of the select gate lines SGD and SGS, word line WL, bit line BL, and source line SL before the processing of the program loop are VSS (e.g., 0V).” *Id.*

In the program loop, a sequencer executes the process of t0 to t9 in sequence, where time t0 to t3 corresponds to a program operation, time t3 to t6 corresponds to a recovery operation, and time t6 to t9 corresponds to a verify operation. *Id.* ¶ 130. At time t0, voltage VSGD is applied to select

gate line SGDsel, and voltage VBL is applied to a program-inhibited bit line BLinh. *Id.* ¶ 131. VGSD and VBL are at higher voltages than VSS; for example VGSD is 4V, and VBL is 2V. *Id.* ¶ 133. At time t1, voltage VPASS (which is higher than VGSD and is, for example, 10V) is applied to each of the word lines WLsel and WLusel. *Id.* ¶ 134. At time t2, program voltage VPGM (which is, for example, 20V) is applied to word line WLsel. *Id.* ¶ 135. At time t3, VPASS is applied to word line WLsel, and the voltage of WLsel drops; at t4, voltage VGCM, which is lower than VPASS and is, for example, 3V–5V, is applied to each of the word lines WLsel and WLusel. *Id.* ¶ 138. Voltage VSL, which, for example, is 1v, is applied to bit lines BLsel and BLinh and source line SL at time t5. *Id.* ¶ 139. At time t6, voltage VGSDH is applied to select gate lines SGDsel and SDGusel, voltage VREAD is applied to word lines WLsel and WLusel, and voltage VSGS is applied to select gate line SGS. *Id.* ¶ 142. VSGDH is a higher voltage than VGSD and is, for example, 6V; VREAD is a higher voltage than VCGM and is, for example, 8V; and VSGS is a voltage higher than VSS and is, for example, 6V. *Id.* At time t7, VSS is applied to select gate line SGDusel and word line WLsel. *Id.* ¶ 143. At time t8, verify voltages AV and BV in order to word line WLsel, and voltage VBLC (for example, 1.5V) is applied to bit line BL. *Id.* ¶ 144. At time t9, VSS is applies to select gate line SGDsel, word lines WLsel and WLusel, bit lines BLprog and BLinh, and source line SL, which allows the voltage of each interconnect to return to the state before the start of the program loop. *Id.* ¶ 145. Suzuki teaches that the recovery operation “has a period in which at minimum VGSD is applied to the select gate line SGDsel and VSL is applied to the bit line BLprog,” and “[t]he type and number of verify voltages used in the

verify operation can vary based on the write data and the progress status of the program loop.” *Id.* ¶ 146.

2. Claim 1

Limitation [1.A.ii] recites “apply, in a pre-verify stage, a first bias voltage on a gate terminal of at least one memory cell of the first memory cell string that is not programmed.” Ex. 1001, 17:46–48. Petitioner contends that Suzuki teaches that voltage VPASS (the recited “first bias voltage”) is applied to non-selected word lines (“WLuse1”) “in the pre-verify stage.” Pet. 81 (citing Ex. 1007 ¶ 134, Fig. 11). Petitioner also contends that “[t]he unselected word lines are coupled to, e.g., unselected memory cells MT5 through MT7” in Suzuki’s first embodiment, and, “[t]hus, Suzuki discloses applying a *first bias voltage (VPASS) on ... at least one memory cell (e.g., MT6 or MT7) of the first memory cell string (the selected string).*” *Id.* at 81–82 (emphases and alterations in original). Petitioner further contends that, “[i]n Suzuki’s embodiment, memory cell MT0 is at the end of the source line side” and “the program operation may proceed ‘from cell units CU on the source line SL side in sequence’” such that when memory cell “MT4 is selected for programming verification, MT6 and MT7 are not programmed.” *Id.* at 82 (citing Ex. 1007 ¶¶ 116, 140, Fig. 2; Ex. 1003 ¶¶ 207–208).

Limitation [1.A.iv] recites “apply, in the verify stage, a second bias voltage on the gate terminal of the at least one memory cell of the first memory cell string that is not programmed, wherein the second bias voltage is smaller than the first bias voltage.” Ex. 1001, 17:52–56. Petitioner contends that “Suzuki discloses applying a *second bias voltage (VREAD)* through the same unselected word lines to *the at least one memory cell in the verify stage.*” Pet. 84 (citing Ex. 1007 ¶ 142, Fig. 11). Petitioner contends

that “VREAD may be 8V” and “VPASS may be 10V,” and “[t]hus, *the second bias voltage (VREAD) is smaller than the first bias voltage (VPASS).*” *Id.* (citing Ex. 1007 ¶¶ 134, 142, Fig. 11; Ex. 1003 ¶ 210).

Patent Owner argues that Suzuki’s VPASS voltage “is not applied in a ‘pre-verify stage’ as required by the Challenged Claims.” Prelim. Resp. 32. Patent Owner states that “Petitioner incorrectly argues that the ‘VPASS’ signal applied from time period t3-t4 is equivalent to the claimed ‘first bias voltage’ applied during a ‘pre-verify stage,’” but “the time period from t3-t4 is not part of Suzuki’s ‘ready operation of the verify operation’ (i.e., is not part of a pre-verify operation as the Petition seems to suggest).” *Id.* at 35. Instead, Patent Owner argues, time period t3 to t4 “is described by Suzuki as an ‘end operation of the program operation’” and “Petitioner does not address this disclosure.” *Id.* (citing Ex. 1007 ¶ 131). Suzuki, however, describes time period t3–t6 as the “recovery operation,” which Suzuki explains is “an operation in which an end operation of the program operation and the ready operation of the verify operation are combined.” Ex. 1007 ¶ 131. Petitioner contends that “[a]t t3, the program operation is complete” and “[t]he recovery operation functions to recover from the program operation and prepare for what follows, namely, a verify operation.” Pet. 80 (citing Ex. 1007 ¶ 131). Because Suzuki explains that the recovery operation combines both the end operation of the program operation and the ready operation of the verify operation, we question Patent Owner’s assertion that time period t3 to t4 is not part of the ready operation of the verify operation, i.e., the recited “pre-verify stage.”

Patent Owner further argues that “‘VPASS’ of the program operation does not prepare the device for the purported ‘verify’ stage from t6-t9.” Prelim. Resp. 35 (citing Ex. 1007 ¶ 131). Patent Owner argues that Suzuki’s

VREAD voltage in the verify stage “is preceded by a *smaller* VCGM voltage during the ‘read operation of the verify operation.’” *Id.* (citing Ex. 1007 ¶ 131, Fig. 11). On this record, we find that Patent Owner’s arguments in this regard have merit. Suzuki teaches that voltage VCGM is applied at time t4 to word lines WLsel and WLusel. Ex. 1007 ¶ 138. Thus, both VPASS and VCGM are applied to word lines WLusel during the recovery operation in time period t3-t6. *Id.*, Fig. 11. Suzuki teaches that VCGM is a lower voltage than VPASS, and VREAD is a higher voltage than VCGM. *Id.* ¶¶ 138, 142. Suzuki also teaches that VCGM can be 3 to 5V, VPASS can be 10V, and VREAD can be 8V. *Id.* ¶¶ 134, 138, 142. Petitioner, however, does not address the application of voltage VCGM to WLusel in time period t4–t6, between the application of voltage VPASS in time period t3–t4 and the application of voltage VREAD in time period t6–t9.

Because both VPASS and VCGM are applied to WLusel during the recovery operation in time period t3–t6, and the recovery operation is a combination of both the end operation of the program operation and the ready operation of the verify operation, it is not clear that VPASS is a “first bias voltage” applied “in the pre-verify stage” as required by claim 1.

We invite the parties to develop these arguments further at trial, to the extent permitted by our rules.

E. Asserted Obviousness over Costa and Seo

Petitioner contends that claims 1–6 would have been obvious over the combined teachings of Costa and Seo. Pet. 103–131. Patent Owner responds that Costa and Seo, “both alone or in combination, do not disclose or render obvious applying distinct bias voltages on a gate terminal of a not-programmed memory cell such that ‘the second bias voltage is smaller than

the first bias voltage’ as required by the Challenged Claims.” Prelim. Resp. 36–41. Patent Owner also argues that Petitioner does not establish that a POSITA would have been motivated to combine Costa and Seo as proposed. *Id.* at 41–43. Having already determined that Petitioner establishes a reasonable likelihood showing that claims 1–6 would have been obvious over the combination of Hongtao and Yu, we need not address this ground in full. We offer the following comments in response to the parties’ argument and evidence to provide guidance to the parties.

1. Overview of Costa

Costa “is directed to reducing errors when sensing in non-volatile memory.” Ex. 1008 ¶ 28. Costa teaches that “[r]ead or verify operations are performed using bias conditions that are dependent on the position of a selected memory cell within a group of non-volatile memory cells.” *Id.* Costa explains that “[d]uring sensing, the selected memory cell receives a read or verify voltage, referred to as a reference voltage, while the remaining memory cells receive a read or verify pass voltage” and, “[f]or at least a subset of the memory cells in the group, the pass voltage is applied dependent upon the position of the selected memory cell in the group.” *Id.* In particular, Costa teaches “the disclosed technology varies the pass voltage applied to at least a subset of the memory cells of the group during sensing based on the memory cell selected for programming.” *Id.* ¶ 30. As an example, Costa teaches that, during program verification, the pass voltage “is increased as programming progresses from memory cells nearest a first select gate, such as a source select gate coupled to a source line, toward a second select gate, such as a drain select gate coupled to a bit line for the group.” *Id.* According to Costa, “[t]he increased pass voltage increases the channel conductance when programming later programmed memory cells”

so that “the final distribution of threshold voltages for the group of memory cells may be more consistent and narrow,” and “causes the channel to have a similar resistance when programming all of the memory cells of the group.” *Id.*

Costa describes an embodiment where “a group of memory cells, or group of word lines for a block of memory cells including the group, is partitioned into ranges or zones of one or more memory cells of the group.” Ex. 1008 ¶ 32. Costa teaches that “[o]ne or more control circuits apply bias conditions for sensing to the group that are based on the zone associated with the selected memory cell or word line.” *Id.* Costa further teaches that “[g]enerally, a lower pass voltage is applied to these memory cells when the selected word line is a lower zone corresponding to earlier programmed memory cells closer to a first select line,” and “[t]he pass voltage is increased for higher zones corresponding to later programmed memory cells closer to a second select line.” *Id.* Costa also describes an embodiment where “the system applies a pass voltage to the subset of memory cells that is dependent upon the reference voltage applied to the selected word lines.” *Id.* ¶ 35. “For example, the system may use a lower pass voltage for the subset of memory cells when applying a higher read or verify reference voltage to a selected word line and a higher pass voltage when applying a lower read or verify reference voltage.” *Id.* Costa teaches that “[t]he higher reference voltage applied to the selected word line may increase the channel conductance such that a lower pass voltage can be applied to the subset of memory cells while maintaining sufficient channel conductance for sensing.” *Id.*

2. *Overview of Seo*

Seo is “directed to a memory device capable of improving a disturb phenomenon of an unselected memory string during a read operation.”

Ex. 1009 ¶ 8. The memory device includes a memory cell array having a plurality of memory strings, a voltage generating circuit configured to generate and apply a plurality of drain select line voltages, a plurality of source select line voltages, and a read voltage to the memory cell array during a read operation. *Id.* ¶ 9. “The memory device also includes control logic configured to control the voltage generating circuit to generate” first and second drain select line voltage applied to first and second unselected memory strings “among the unselected memory strings during the read operation, wherein the second drain select line voltage is different from the first drain select line voltage.” *Id.* Seo teaches that the “second drain select line voltage can be applied to second unselected memory strings among the unselected memory strings at a potential level lower than the first potential level.” *Id.* ¶ 10.

Seo describes a read operation where a first voltage V1 is applied to first drain select line DSL0 and first source select line SSL0 corresponding to a selected memory string ST, and a second voltage V2 is applied to second drain select line DSL1 corresponding to the unselected memory string that shares first select source line SSL0, during a first time period t1. *Id.* ¶ 88. Seo teaches that “second voltage V2 may have the same potential level as the first voltage V1.” *Id.* Seo further teaches that “[s]ubsequently, the pass voltage Vpass may be applied to unselected word lines Unsel WLs,” then “the read voltage Vread may be applied to a selected word line Sel WL during a second time period t2.” *Id.* ¶¶ 89–90.

3. *Claim 1*

With respect to the “apply, in the pre-verify stage, a first bias voltage on a gate terminal of at least one memory cell of the first memory cell string that is not programmed” limitation of claim 1, Petitioner contends that “Seo discloses applying a ‘pass voltage V_{pass} ... to the unselected word lines’ during a first time period t_1 .” Pet. 108 (citing Ex. 1009 ¶¶ 88–89, Fig. 8) (alteration in original). In particular, Petitioner contends that “Seo discloses *applyi[ing], in the pre-verify stage (the first time period t_1), a first bias voltage (V_{pass}) on ... at least one memory cell (via the Unsel WLs) of the first memory cell string.*” *Id.* at 109 (emphases and alteration in original). Petitioner contends that Costa teaches that “unprogrammed cells are typically positioned between the selected word line and a select line,” and “[a]pplying Seo’s first bias voltage V_{pass} on unselected word lines of Costa’s memory device, V_{pass} is applied on unprogrammed memory cells such as those at WL29-31 in this illustrated scenario.” *Id.* at 109–110 (citing Ex. 1008 ¶ 33, Fig. 12H; Ex. 1003 ¶¶ 252–256).

With respect to the “apply, in the verify stage, a second bias voltage on the gate terminal of the at least one memory cell of the first memory cell string that is not programmed, wherein the second bias voltage is smaller than the first bias voltage” limitation of claim 1, Petitioner contends Costa teaches applying voltage V_{readL} on unselected word lines WL30 and WL31 in the sensing phase. Pet. 111 (citing Ex. 1008 ¶ 147, Fig. 12H). Petitioner contends that Costa also teaches that V_{readL} “may be several millivolts less” than the standard read pass voltage V_{read} , and V_{readL} may be used on WL30 and WL31 because they have not undergone programming and have a low threshold voltage. *Id.* at 111–112 (citing Ex. 1008 ¶ 122; Ex. 1003 ¶¶ 260–261).

Patent Owner argues that “Costa does not disclose the use of separate ‘verify’ and ‘pre-verify’ stages for a verify operation, or that different voltage levels would be used during a ‘verify’ and a ‘pre-verify’ stage as required by the ’957” patent. Prelim. Resp. 39. Patent Owner argues that “[w]hile Costa discloses that a lower ‘pass voltage’ can be used for *unprogrammed memory cells* as compared to *programmed memory cells*, Costa fails to disclose any difference in the ‘pass voltage’ applied to any given memory cell *at different stages of a verification process.*” *Id.* (citing Ex. 1008 ¶¶ 121, 122, 147). Patent Owner argues that Costa’s teaching that programming a memory cell increases the threshold voltage and that lower read pass voltage V_{readL} can be used on unprogrammed cells in an erased state “does not teach separate ‘verify’ and ‘pre-verify’ stages, let alone using different voltage levels during a ‘verify’ and a ‘pre-verify’ stage.” *Id.* (citing Ex. 1008 ¶ 122). Patent Owner also argues that “Seo discloses that a ‘read’ operation can be divided into ‘time period t1’ and ‘time period t2,’ and that a ‘pass voltage V_{pass} may be applied to unselected word lines’ during both a portion” of time periods t1 and t2, but “Seo fails to demonstrate the use of two distinct bias voltages on not-programmed word lines.” Prelim. Resp. 39–40 (citing Ex. 1009 ¶¶ 87–90).

On this record, Patent Owner’s arguments have merit. As Patent Owner notes, Seo describes a read operation divided into time periods t1 and t2 wherein a constant V_{PASS} voltage is applied to unselected word lines from mid-way through time period t1 to about the end of time period t2. Ex. 1009 ¶¶ 87–90, Fig. 8. Petitioner identifies time period t1 as a pre-verify stage, but Seo only describes time periods t1 and t2 with respect to performing a read operation that includes the steps selecting a page and memory string, setting the select transistor line voltage of the unselected

memory string and apply period thereof, applying voltage to the select lines of the unselected memory string, and applying the read voltage. *Id.* ¶¶ 87–90, Fig. 7. In light of the disclosures in Seo, it is not clear that time period t1 is a “pre-verify stage” as claimed. Nor is it clear, on this record, that Costa’s “sensing phase” is a “verify stage” or voltage VreadL is a second bias voltage that is smaller than the first bias voltage (Seo’s VPASS).

The parties are invited to develop these arguments further at trial, to the extent permitted under our rules.

III. CONCLUSION

Based on the arguments in the Petition and the Preliminary Response, and the evidence of record, we determine that Petitioner establishes a reasonable likelihood that it will prevail on its challenge to at least one claim of the ’957 patent. Accordingly, we institute an *inter partes* review of all the challenged claims on all the challenged grounds.

The factual findings set forth in this Decision are preliminary and provided for the sole purpose of deciding whether to institute a review. Any final findings will be based on the full trial record, including any information presented in a timely filed response to the Petition. *See Trivascular, Inc. v. Samuels*, 812 F.3d 1056, 1068 (Fed. Cir. 2016) (noting that “there is a significant difference between a petitioner’s burden to establish a ‘reasonable likelihood of success’ at institution, and actually proving invalidity by a preponderance of the evidence at trial”) (quoting 35 U.S.C. § 314(a); comparing *id.*, with § 316(e)).

IV. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that an *inter partes* review is instituted with respect to all of the grounds asserted in the Petition; and

FURTHER ORDERED that, pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is hereby given of the institution of a trial, which shall commence on the entry date of this Decision.

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