UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,

Petitioner,

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,

Patent Owner.

Case IPR2024-00792
Patent 11,468,957

PATENT OWNER'S RESPONSE UNDER 37 C.F.R. § 42.107

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LIST OF EXHIBITS

Exhibit	Description
Ex. 2001	Micron 4-2 Claim Construction Disclosure
Ex. 2002	YMTC 4-2 Claim Construction Disclosure
Ex. 2003	Declaration of Steven Przybylski ("Przybylski")
Ex. 2004	U.S. 2024/0295960 ("Li")
Ex. 2005	U.S. 2023/0343398 ("Dong")
Ex. 2006	Transcript of December 17, 2024 Deposition of Dr. Liu for IPR2024-00795 in Connection with Patent U.S. 11,501,822 ("Liu822 Tr.")
Ex. 2007	U.S. 10,726,920 ("Yang")
Ex. 2008-09	Reserved
Ex. 2010	Declaration of Jonathan Bradford

LIST OF ABBREVIATIONS

Abbreviation	Term
’957	U.S. Pat. No. 11,468,957
’957FH	File History of U.S. Pat. No. 11,468,957
Challenged Claims	’957, Claims 1-6
Liu	Declaration of Dr. Liu (Ex. 1003)
Hongtao	Chinese Pat. App. Pub. No. 109065091 (Ex. 1005)
Yu	U.S. Pat. No. 20190198117 (Ex. 1006)
Suzuki	U.S. Pat. No. 20210082505 (Ex. 1007)
Costa	U.S. Pat. No. 20180012667 (Ex. 1008)
Seo	U.S. Pat. No. 20210027848 (Ex. 1009)
Li	U.S. 2024/0295960 (Ex. 2004)
Dong	U.S. 2023/0343398 (Ex. 2005)
Liu822 Tr.	Transcript of December 17, 2024 Deposition of Dr. Liu for IPR2024-00795 in Connection with Patent U.S. 11,501,822 (Ex. 2006)
Yang	U.S. 10,726,920 (Ex. 2007)
Office	U.S. Patent and Trademark Office
Petition or Pet.	Petition for *Inter Partes* Review of U.S. Patent No. 11,468,957 (IPR2024-00792, Paper 1)
Parallel district court litigation	*Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc.*, NDCA-3-23-cv-05792 (N.D. Cal.)

Patent Owner	Yangtze Memory Technologies Co. Ltd.
Petitioner	Micron Technology, Inc.
POSITA	Person of ordinary skill in the art
Przybylski	Declaration of Steven Przybylski

I. INTRODUCTION

The references in Petitioner's Grounds, either alone (Ground 2) or in combination (Grounds 1, 3), fail to disclose or render obvious the Challenged Claims of U.S. Patent No. 11,468,957 ("'957," Ex. 1001). None of the Grounds discloses or renders obvious applying a "first bias voltage" in a "pre-verify stage" and a smaller "second bias voltage" in a "verify stage" as required by the Challenged Claims. Further, Petitioner fails to present evidence that the modifications necessary for its proposed Grounds were suggested or otherwise motivated at the time of the invention, or that there was a reasonable expectation of success. Instead, Petitioner relies on conclusory expert testimony, misrepresentations, and hindsight. As set forth herein, the Grounds presented in the Petition fail to make the required showings of anticipation or obviousness. This Patent Owner Response is supported by the declaration of Dr. Steven Przybylski. Ex. 2003 ("Przybylski"), ¶¶1-26.

II. THE '957 PATENT

The '957 discloses an improved technique for performing verify operations in flash memory devices that mitigates hot-carrier injection ("HCI") and induced edge summation ("ESUM") losses, thus improving the overall reliability of the device and reducing power consumption. '957, 1:44-49, 17:7-30. Przybylski, ¶27.

As explained by the '957, three-dimensional (3D) NAND flash memory was developed to increase density and reduce cost. '957, 1:12-25. A 3D-NAND device

may be formed by a stack of "alternating **word line layers** … and insulating layers" with vertically arranged "channel structures" that each "**form a respective vertical NAND memory cell string**." '957, 7:60-8:9, 8:27-43.

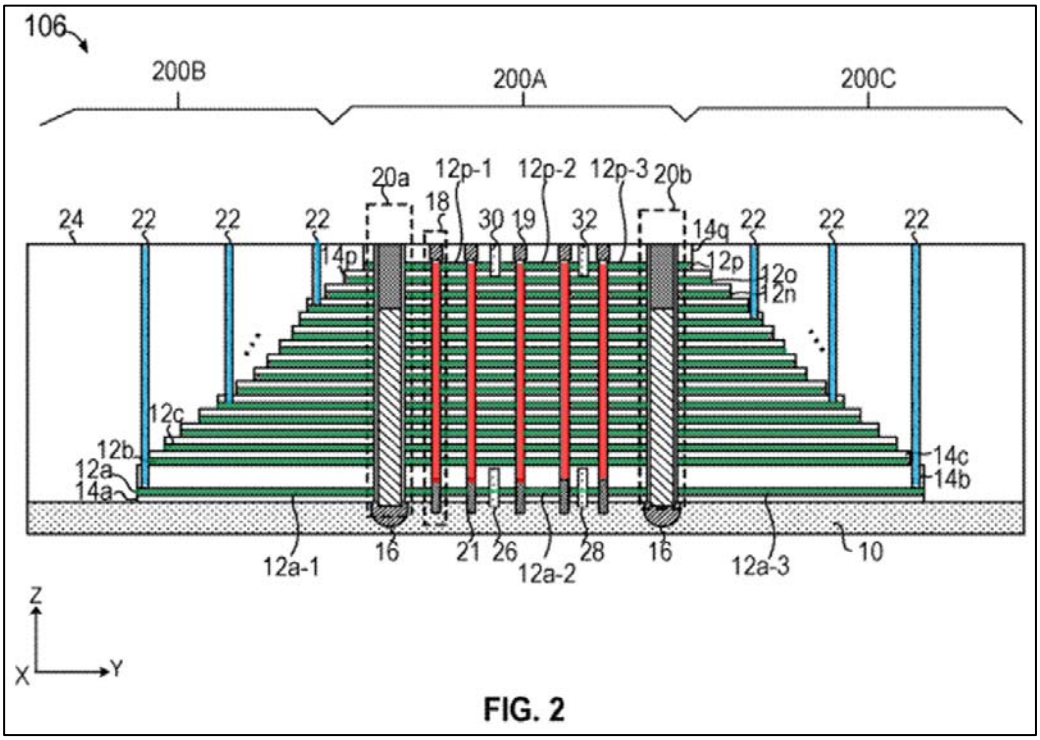


FIG. 2

'957, Fig. 2. The location where each word line layer intersects with a memory cell string forms a transistor that acts as a memory cell, and to apply voltages to the different portions of the memory strings, "**word line contacts**" are formed such that "gate voltages can be applied on gates of the memory cell transistors through the word line contacts … that are coupled to the word line layers." '957, 8:50-51. In general, word lines have an RC time-constant arising from large capacitances that arise from the stacked structure. *See, e.g.*, Ex. 1014 ("Aritome"), 350-353 (discussing "RC (resistance-capacitance) delay" in word lines, and that in a "stacked

word-line (WL) structure in 3D NAND cells … a WL capacitance is greatly increased from 2D cells"). And as recognized by the '957, the target voltages applied to word lines via the contacts differ from the resulting voltages that develop on the gate terminals of the memory cells over time. *See* '957, 11:58-12:1, 12:10-27, Figs. 4-5. Przybylski, ¶28.

As shown in Fig. 2, the device "can include a plurality of memory cell strings," which each include "a bottom-select-gate (BSG) transistor, memory cells, and a top-select-gate (TSG) transistor that are connected in series." '957, 1:24-40, 8:27-43, 9:3-30, 14:31-34. Each transistor gate is connected to a different word line layer, which is used to apply voltages to the corresponding transistor gates. Word line layers can include "bottom select gate (BSG) layers, gate layers … [and] top select gate (TSG) layers" to apply voltages to the gate terminals of BSG transistors, memory cells, and TSG transistors respectively. '957, 7:60-8:8. Przybylski, ¶29.

For example, as shown in Fig. 3, "the string 300A can include a bottom select transistor (BST) or bottom-select-gate (BSG) transistor 302A, a plurality of memory cells (MCs) 304A, and a top select transistor (TST) or top-select-gate (TSG) transistor 306A that are disposed sequentially and in series." '957, 9:3-30. During programming operations, the **selected memory cell** being programmed is surrounded by the already **programmed memory cells** to one side of the string, and **not-programmed memory cells** (i.e., memory cells that have yet to be programmed)

on the other side of the string. Memory cells within the string are typically "programmed in the forward order" going "from a bottom MC adjacent to the BSG transistor to a top MC adjacent to the TSG transistor" (*id.* at 9:57-10:7) or they are "programmed in a reverse order" going "from a top memory cell adjacent to the TSG transistor to a bottom memory cell (e.g., MC0) adjacent to the BSG transistor" (*id.* at 14:31-42). Przybylski, ¶30.

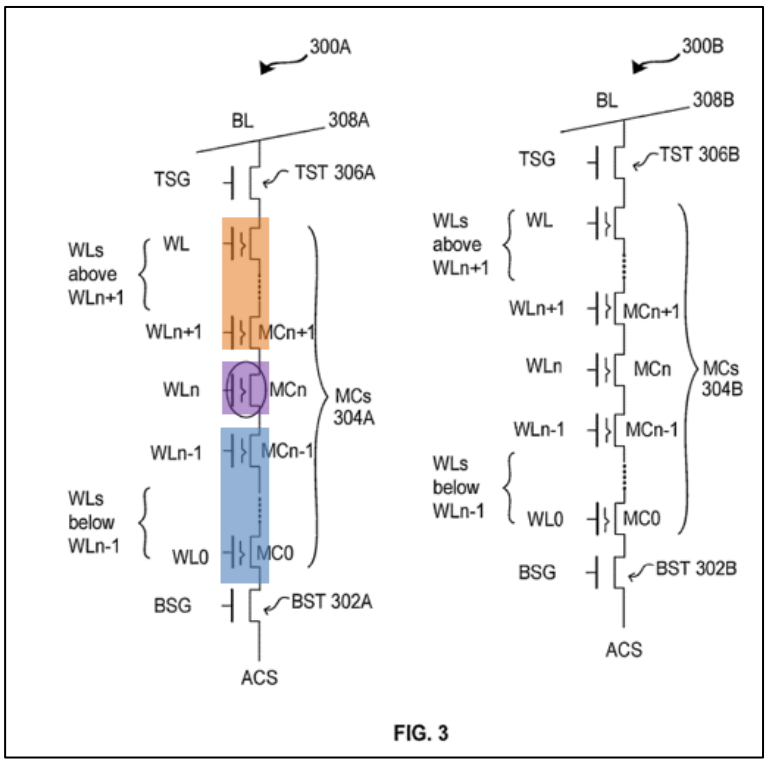


FIG. 3

Id., Fig. 3 (showing "**programmed**" and "**not-programmed**" memory cells when a forward programming order is used). Przybylski, ¶30.

After programming each cell, the value is "verified" to make sure it was programmed correctly. As discussed in the '957, traditional approaches for performing verify operations suffered from "hot carrier injection" (HCI) between

the selected memory cell that is having its programmed state be verified and neighboring memory cells, which could result in "induced edge summation (ESUM) loss." '957, 1:44-49, 6:66-7:12. Hot carrier injection occurs when, due to potential differences across the channel of the selected memory cell, hot electrons at the selected memory cell are inadvertently injected into neighboring memory cells. *See* Aritome, 235-238, 244-248. This causes the threshold voltages of the neighboring memory cells to drift over time and creates "edge summation (ESUM)" losses, which relates to the number of different programmed states within each memory cell that the device can reliably distinguish between. *See* Ex. 2004 ("Li"), [0056] ("ESUM" is the sum of the "voltage interval[s] between threshold voltage distributions corresponding to two adjacent data states that can be used to read data on a memory cell"); Ex. 2005 ("Dong"), [0085] (describing ESUM). Przybylski, ¶31.

The claimed invention of the '957 helps to address these issues by subdividing the verification operation into multiple stages that occur after programming (e.g., a "pre-verify stage" where voltages are applied to prepare the device for a subsequent "verify stage"), and selectively applying different voltages to the gate terminals of the selected memory cell and other not-programmed memory cells during each stage. *See* '957, 7:13-32. Przybylski, ¶32.

The '957 claims are explicitly directed to voltages applied "***on a gate terminal***" of the memory cells within the memory cell string, as distinct from target voltages

applied to corresponding word lines. *See* '957, Claim 1, 1:50-2:8, 6:37-49, 15:31-16, Fig. 10. As explained by the '957, bias and verify voltages "can be applied on the gate terminal (or gate) of the selected memory cell MCn through a WL layer (e.g., WLn) that is coupled to the selected memory cell MCn." '957, 9:31-56. But the applied voltages on the memory cell gate terminals may differ from the applied word line voltages, as they need time to fully "develop" to the desired target values. *See* '957, 6:37-7:12. These differences become more pronounced the shorter the duration of the "pre-verify" period. *See* '957, 11:58-12:27. Przybylski, ¶33.

Fig. 4 shows how bias voltages may be applied using "a long pre-pulse time," while Fig. 5 shows the challenges of using a "short pre-pulse time." *Compare* '957, 11:58-12:9 *with* 12:10-27. In Fig. 4, "appropriate bias voltages can be applied on the selected TSG layer, the unselected TSG layer, the WLs … and the BSG layer in the **pre-pulse stage**." '957, 10:57-11:15. For example, a bias voltage of 6.8 volts can be applied on each word line. *Id.* During the subsequent "**verify/read stage**," "[t]he bias voltage applied on the WLs (>n+1) can be maintained," and the "bias voltage (or verify voltage) applied on the selected word line layer WLn can be reduced." '957, 11:16-57. Przybylski, ¶34.

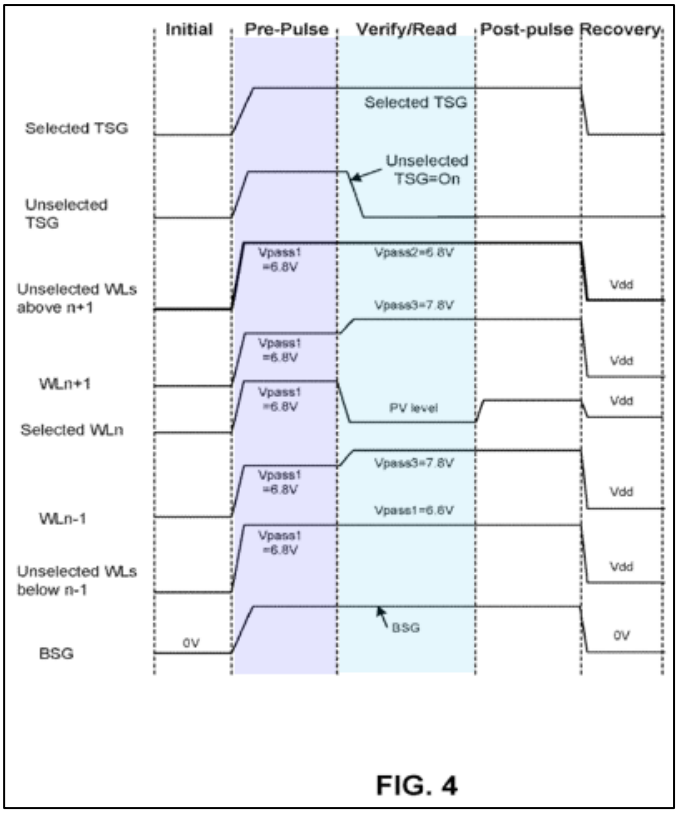


FIG. 4

As explained by the ’957, “the long pre-pulse time” of Fig. 4 may be “sufficient for the bias voltages to be developed fully before the TSG transistor is switched off,” meaning the applied bias voltages on the transistor gates will reach the desired values that were applied through the word lines. ’957, 11:68-12:1; *see also id.* 13:13-15. Przybylski, ¶34.

By comparison, Fig. 5 illustrates “a short pre-pulse time” that is “insufficient for the bias voltages applied on the WLs (>n+1), WLn+1, WLn, WLn−1, and WLs (<n−1) to be developed fully in the pre-pulse stage.” ’957 12:10-27. As shown by the curved lines in Fig. 5, “the bias voltages are less than a target value, such as 6.8 volts,” because insufficient time is provided for the bias voltages to charge up during

the pre-pulse stage. *Id.* Instead, the bias voltages are only "developed to the target value, such as 6.8 volts, in the verify/read stage." *Id.* Przybylski, ¶35.

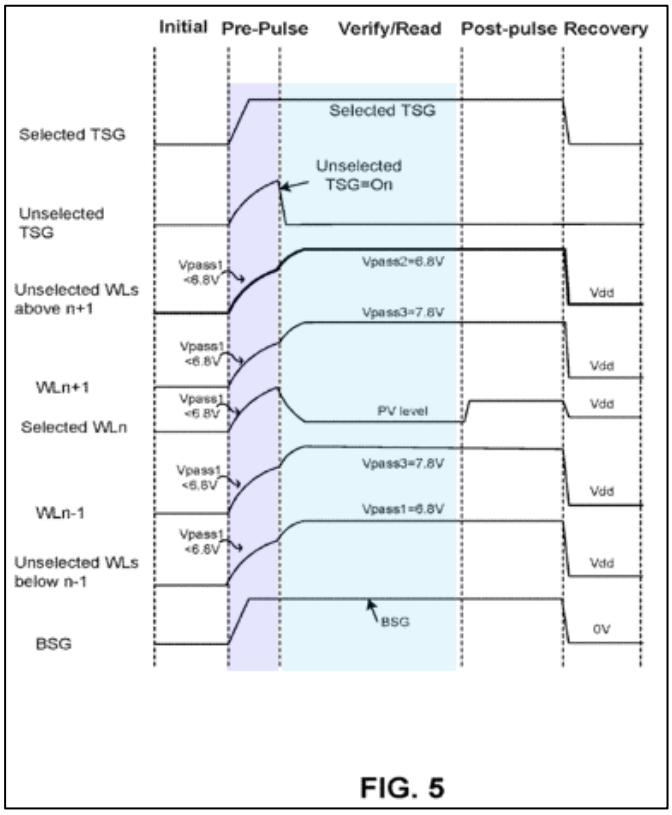


FIG. 5

Accordingly, depending on the duration of the pre-pulse stage, additional techniques are needed to ensure that bias voltages applied on the memory cell gate terminals can fully develop to the desired target values needed for device operation. *Compare* '957, 11:58-12:9, 12:28-39, 14:31-41, Figs. 4, 6, 8 (using a long pre-pulse time) *with* 12:10-38, 13:5-25, 14:63-15:17, Figs. 5, 7, 9 (using a short pre-pulse time). Przybylski, ¶36.

For example, Fig. 6 is a '957 embodiment that uses a "long pre-pulse period" similar to Fig. 4, meaning that the bias voltages applied on the gate terminals will

fully develop and reach the target values applied on the word lines. '957, 12:28-42; *see also id.* 11:48-12:9. But unlike Fig. 4, the bias voltages applied to the WLs above WLn+1 are smaller in the **verify stage** than the **pre-verify stage**. '957 12:39-42.

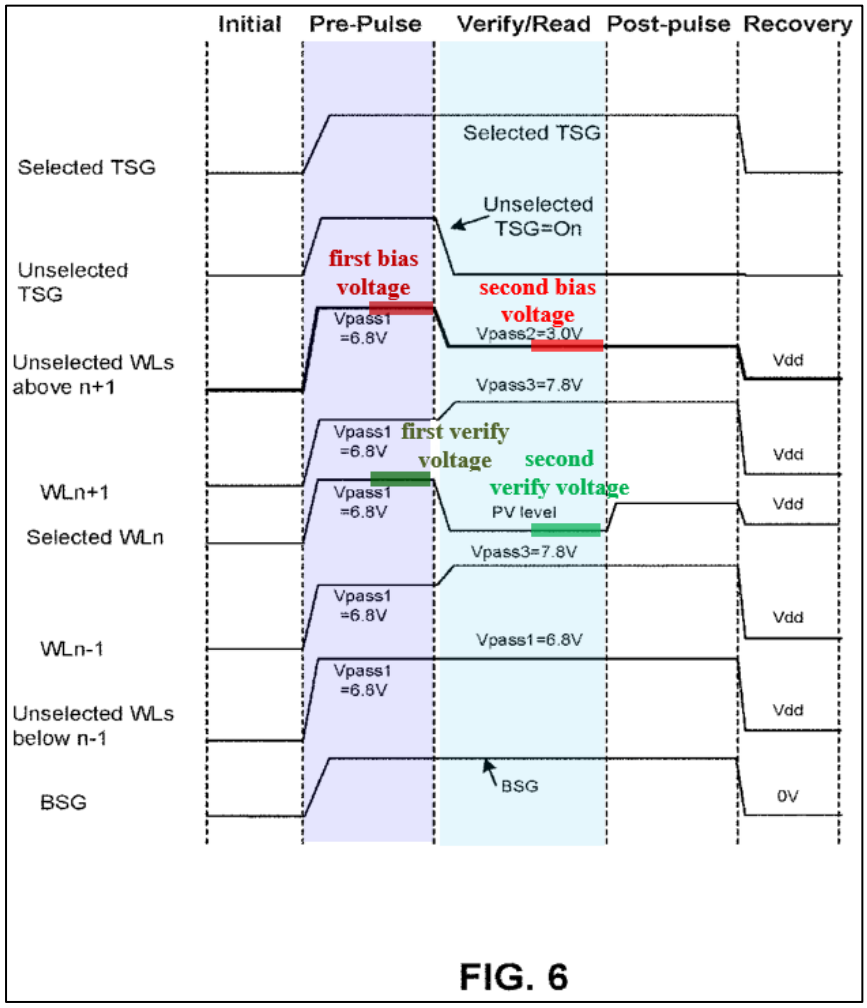


FIG. 6

As a result, in the embodiment of Fig. 6 a **first verify voltage** is applied to a selected word line (WLn), which fully develops on the gate of a selected memory cell in the **pre-verify stage**. '957, 1:58-2:8. At the same time, a **first bias voltage** is applied to unselected word lines above n+1, which fully develops on the gate of a memory cell of the memory cell string that is not yet programmed. '957, 6:37-49.

Subsequently, in a **verify stage**, the first verify voltage is replaced with a **second verify voltage**, and the first bias voltage is replaced with a **second bias voltage** that is smaller. '957, 17:32-56. Przybylski ¶37.

The '957 explains that by applying "a lower bias voltage" in the verify stage as compared to the pre-verify stage "the gradient of the channel potential of the selected memory cell string can be reduced," and as a result "HCI cannot be generated from the selected memory cell to the upper adjacent memory cell … in the selected memory cell string." '957, 12:63-13:4. The claimed approach therefore not only lowers power consumption, but by helping mitigate HCI the invention of the '957 prevents ESUM loss and improves device performance as compared to conventional systems. *See* '957, 6:50-65, 17:7-17. Przybylski, ¶¶38-39.

Independent Claim 1 of the '957 is an apparatus claim directed to aspects of the above-described invention:

> [1.pre] An apparatus for reading a memory device including a first memory cell string and a second memory cell string, the first memory cell string including a bottom-select-gate (BSG) transistor, memory cells, and a top-select-gate (TSG) transistor that are connected in series, the second memory cells string including a BSG transistor, memory cells, and a TSG transistor that are connected in series, the apparatus comprising: processing circuitry configured to:
>
> > [1.a] apply, in a pre-verify stage, a first verify voltage on a gate terminal of a selected memory cell of the first memory cell string, the selected memory cell being programmed and arranged between a first adjacent memory cell and a second adjacent memory cell;

> [1.b] apply, in the pre-verify stage, a first bias voltage on a gate terminal of at least one memory cell of the first memory cell string that is not programmed;
>
> [1.c] apply, in a verify stage, a second verify voltage on the gate terminal of the selected memory cell of the first memory cell string; and
>
> [1.d] apply, in the verify stage, a second bias voltage on the gate terminal of the at least one memory cell of the first memory cell string that is not programmed, wherein the second bias voltage is smaller than the first bias voltage.

III. LEVEL OF ORDINARY SKILL IN THE ART

For purposes of this proceeding only, Patent Owner does not object to the definition of a person of ordinary skill in the art ("POSITA") proffered by Petitioner—i.e., a person with "a master's degree in electrical engineering or a similar discipline, along with 4-5 years of professional experience working with … NAND memory devices" or the equivalent. Pet. 19-20. The Challenged Claims are valid regardless of the precise definition of a POSITA. Przybylski, ¶¶40-44.

IV. CLAIM CONSTRUCTION

Other than the terms identified below, Patent Owner submits that constructions of the claim terms are not necessary to resolve the invalidity arguments raised in the Petition. Patent Owner reserves the right to modify or elaborate on its proposed constructions and to raise further claim construction issues in the parallel district court proceedings. Przybylski, ¶45.

A. "Apply, in a [Pre-Verify]/[Verify] Stage, a [First/Second] [Verify/Bias] Voltage"

Claim 1 of the '957 recites circuitry configured to "apply" voltages "in a pre-verify stage" or "in a verify stage." The Petition argues that these limitations "do not require applying these voltages throughout the given stage." *See* Pet. 18-19. For the purposes of this proceeding, Patent Owner submits that this issue does not need to be addressed by the Board, because it is not necessary to resolve the invalidity arguments raised in the Petition. *See Realtime Data, LLC v. Iancu*, 912 F.3d 1368, 1375 (Fed. Cir. 2019) (the Board construes terms "only to the extent necessary to resolve the controversy"). Even under Petitioner's proposed interpretation, the Grounds presented in the Petition fail. Przybylski, ¶46.

As discussed in Sections VI and VIII, Grounds 1 (Hongtao in view of Yu) and 3 (Costa in view of Seo) fail at least because the references do not disclose or render obvious applying a distinct "first bias voltage" and "second bias voltage" on a gate terminal of a not programmed memory cell. Additionally, as discussed in Section VII, Ground 2 (Suzuki) fails at least because the purported "first bias voltage" identified in the Petition is not applied during a "pre-verify stage" and does not prepare the device for a verify stage. Przybylski, ¶47.

B. "Apply a [Top/Bottom] Bias Voltage on a Gate Terminal of the [TSG/BSG] Transistor of the First Memory Cell String in the Pre-Verify Stage and the Verify Stage"

Because the Grounds raised in the Petition fail to disclose or render obvious independent claim 1, the Board does not need to construe any dependent claim terms. But if the Board reaches the issue of whether the added limitations of dependent claims 5 and 6 are disclosed or rendered obvious, the plain and ordinary meaning of the term "apply a [top/bottom] bias voltage on a gate terminal of the [TSG/BSG] transistor of the first memory cell string ***in the pre-verify stage and the verify stage***" requires a single voltage level be applied in ***both*** the pre-verify stage and the verify stage. That construction is consistent with the '957, the plain and ordinary meaning, and basic principles of claim interpretation. By comparison, the Petition incorrectly argues that the claimed "[top/bottom] bias voltage" may have different values in the pre-verify stage and the verify stage (i.e., that the claims are satisfied by different voltages being applied in each stage). Pet. 61-64, 96-98. Przybylski, ¶¶48-49.

The plain meaning of applying "a [top/bottom] bias voltage … in the pre-verify stage and the verify stage" requires that the same voltage level be applied in ***both*** the pre-verify stage and the verify stage. That plain meaning is consistent with the '957 specification. For example, as shown in Fig. 4, the '957 states a "**bias voltage (or bottom bias voltage), such as 5 volts**" is applied to the BSG layer, and "**bias voltage (or top bias voltage), such as 5 volts**" is applied to the selected TSG

layer during the "**pre-pulse stage**," and those voltages "can be maintained to keep the channel of the selected memory cell string conductive" during the subsequent **verify/read stage**.

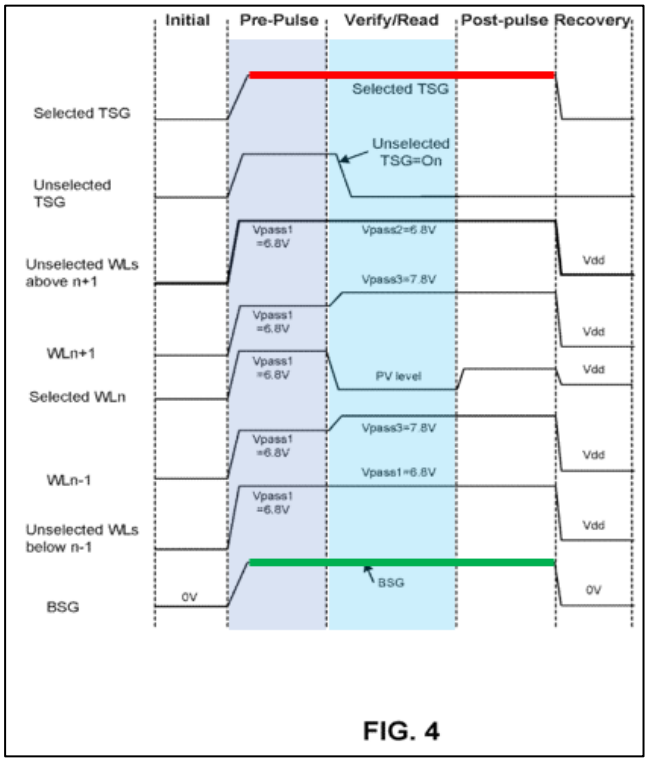


FIG. 4

'957, 10:57-11:15 (describing the pre-pulse stage), 11:16-57 (describing the verify/read stage), Fig. 4. The other embodiments of the '957 similarly illustrate the top bias voltage and bottom bias voltage having a constant value that is applied in both a pre-verify stage and a verify stage. *See* '957 Figs. 5-9. Przybylski, ¶50.

By comparison, Petitioner's arguments implicitly read out the requirement that the claimed bias voltages are applied in both the "pre-verify stage ***and*** the verify stage." *See* Pet. 61-64, 96-98. Specifically, the Petition argues that claims 5 and 6 are met by a "top bias voltage" and "bottom bias voltage" that have a first voltage

level in a pre-verify stage, and a different voltage level in the verify stage. *See* Pet. 61-69, 96-102. To support this incorrect interpretation, Petitioner makes two flawed arguments, neither of which establishes that the claimed bias voltages may have different values in the pre-verify stage and the verify stage. Przybylski, ¶51.

First, Petitioner makes a legally flawed argument by suggesting the claims would be satisfied by two different values because the limitation recites "***a*** [top/bottom] bias voltage on ***a*** gate terminal of the [TSG/BSG] transistor," and the term "***a***" is understood in patent law to mean "more than one." *See* Pet. 62, citing *Elkay Mfg. Co. v. Ebco Mfg. Co.*, 192 F.3d 973, 977 (Fed. Cir. 1999). Petitioner's argument misapplies basic tenants of claim interpretation. The use of the term "***a***" in the claim language allows for multiple bias voltages (and multiple gate terminals) to be present in the claimed apparatus, but it does not remove the requirement that the ***claimed*** "bias voltage" must be applied "***in the pre-verify stage and the verify stage***." "[T]he indefinite article a means one or more in open-ended claims containing the transitional phrase comprising … But that is a separate issue from whether the claims require the same component to perform multiple functions or satisfy multiple limitations of a claim." *Finjan LLC* v *SonicWall, Inc.,* 84 F.4th 963, 974-975 (Fed. Cir. 2023). Regardless of how many bias voltages are present, the claim language requires at least one of them to be applied in both "the pre-verify stage and the verify stage." *See, e.g.*, *Salazar v. AT&T Mobility LLC*, 64 F.4th 1311,

1318 (Fed. Cir. 2023) ("[I]t does not suffice to have multiple [claimed elements], each able to perform just one of the recited functions; the claim language requires at least one [claimed element] capable of performing each of the recited functions."). Przybylski, ¶52.

Second, Petitioner suggests that requiring a single bias voltage to be applied in both the "pre-verify stage and the verify stage" is inconsistent with the embodiment of Fig. 7. *See* Pet. 62. That argument is also misplaced. Like the other '957 figures, Fig. 7 shows a constant **bottom bias voltage** applied to the BSG layer and a constant **top bias voltage** applied to the TSG layer in both the **pre-pulse stage** and the subsequent **verify/read stage**. Przybylski, ¶52.

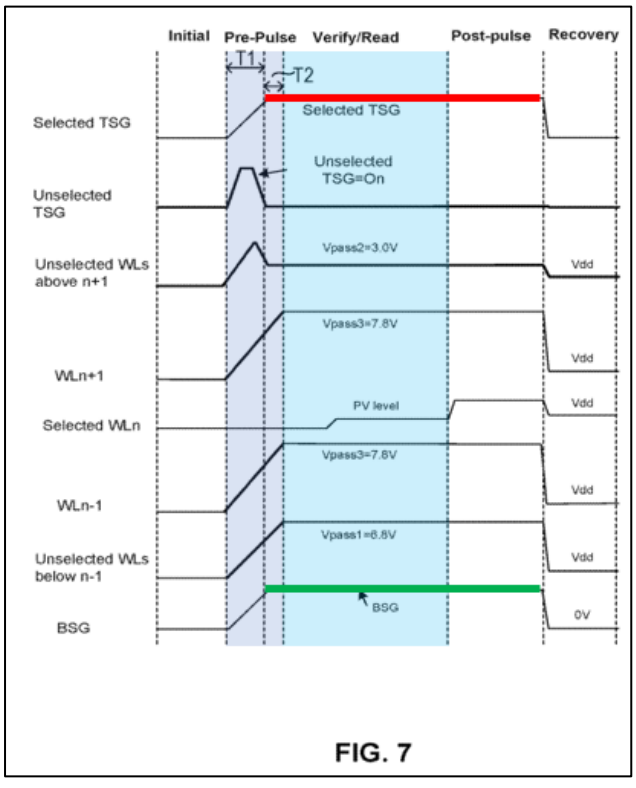


FIG. 7

Thus, contrary to what Petitioner argues, the plain meaning of the claims and the '957 specification confirm that limitation "apply a [top/bottom] bias voltage on a gate terminal of the [TSG/BSG] transistor of the first memory cell string ***in the pre-verify stage and the verify stage***" as recited in claims 5 and 6 requires a single voltage level be applied in ***both*** the pre-verify stage and the verify stage. Przybylski, ¶53.

V. THE PRIOR ART REFERENCES RELIED UPON[1]

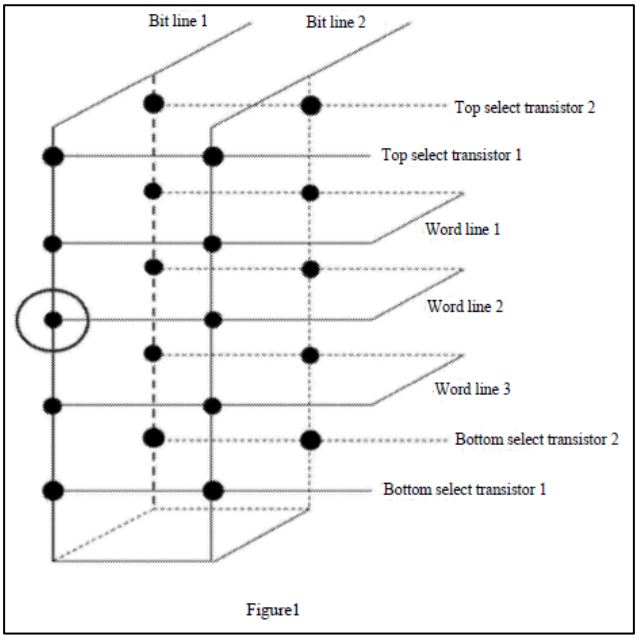
A. Chinese Pat. App. Pub. 109065091 ("Hongtao") (Ex. 1005)

Petitioner contends that the combination of Hongtao and Yu (Ground 1) renders obvious the Challenged Claims. Pet., 27-40. Hongtao purportedly discloses a method for reading memory cells in a 3D NAND flash memory device with a "pre-conduction phase" followed by a "reading phase step," which Petitioner analogizes with the claimed "pre-verify stage" and "verify stage." Hongtao, [0006]; Pet. 20-22, 30-40. But Hongtao is concerned with only a "reading method" for 3D NAND. Hongtao, Abstract. Hongtao does not disclose any type of verify operation, nor does Hongtao suggest using a similar multi-step approach to create a verify operation with distinct "pre-verify" and "verify" stages. Unlike the '957, Hongtao also does not

[1] For the purposes of the present IPR proceeding only, Patent Owner does not contest that Hongtao, Yu, Suzuki, Costa, and Seo qualify as prior art to the '957.

recognize the importance of long versus short pre-pulse periods, and to extent Hongtao illustrates target voltages being applied to word lines, Hongtao does not address the resulting voltages actually applied on the "gate terminals" of the memory cells. Przybylski, ¶55.

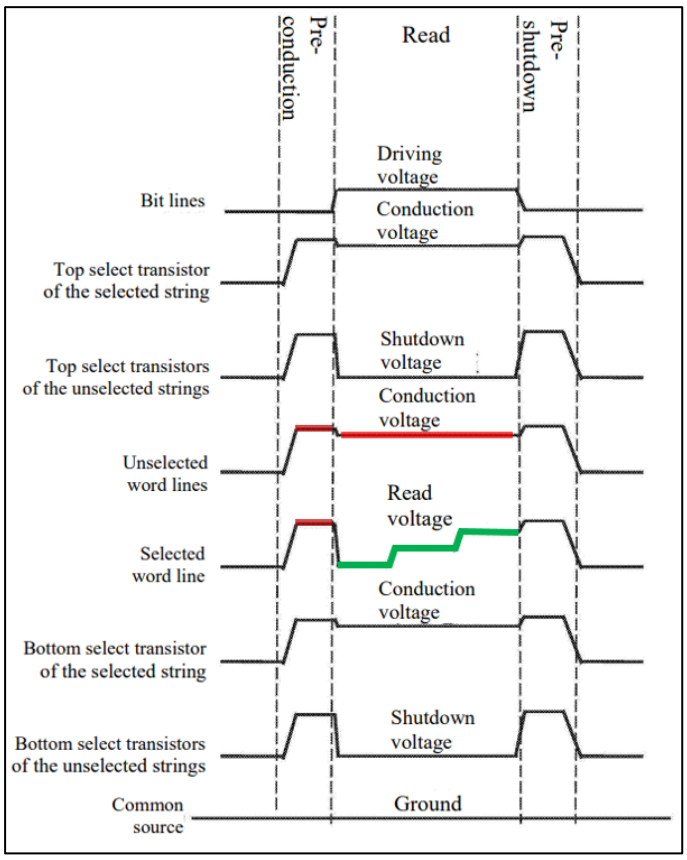
As shown below, Hongtao describes a device with an array of "memory strings" formed by "memory cells."



Hongtao, [0018], Fig. 1.[2] To apply voltages during a reading operation, the "gates of the memory cells" are each "connected" to a "word line." *Id.* Przybylski, ¶56.

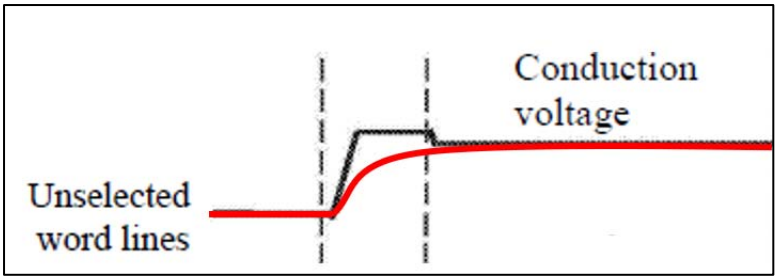
[2] The Petition inconsistently points to the memory cell connected to word line 1 as both the "first adjacent memory cell" and the "not programmed memory cell" recited in claim 1. *See* Pet., 30, 36. Przybylski, ¶56.

Hongtao states that during the pre-conduction phase a "**pre-conduction voltage** is applied to both the unselected word line and the selected word line to turn on the channels of the selected string and the unselected string." *See* Hongtao, [0023]. As shown below in Fig. 2 of Hongtao, in the reading phase, "the unselected memory cells on the selected string are applied with a **conduction voltage** through the unselected word lines," while the selected memory cell receives a series of **read voltages**. Hongtao, [0025]. Przybylski, ¶57.



Petitioner argues that Hongtao's "**pre-conduction voltage**" is equivalent to the claimed "first bias voltage on a gate terminal," and that Hongtao's "**conduction voltage**" is equivalent to the claimed "second bias voltage on the gate terminal." *See*

Pet. 30-40. Based on the above figure, Petitioner argues that this mapping teaches "[a] second bias voltage is smaller than [a] first bias voltage" applied on a gate terminal of a memory cell that is not programmed, as required by the Challenged Claims. *See* Pet. 39-40. But Figure 2 of Hongtao illustrates target voltages applied to word line layers, not the resulting voltages applied on gate terminals of the memory cells, which would be subject to RC time-constants. *See* Hongtao [0023], [0025]; Aritome, 350-353. Hongtao further fails to provide the necessary details to infer how the resulting voltages on the gate terminals of the memory cells would develop over time, nor has the Petitioner presented any arguments or evidence that it would have been obvious to implement Hongtao's system such that the voltages applied to the gate terminals of the memory cells develop fully so as to match the values illustrated in Figure 2. *C.f.* '957, 11:58-12:9, 12:10-27 (discussing that bias voltages need sufficient time to develop fully). Indeed, the **voltages applied on the gate terminals** may be smoothed out similar to the below, and there would be no smaller second bias voltage applied on the gate terminals in the later time period:



Przybylski, ¶¶58-59.

B. U.S. 2019/0198117 ("Yu") (Ex. 1006)

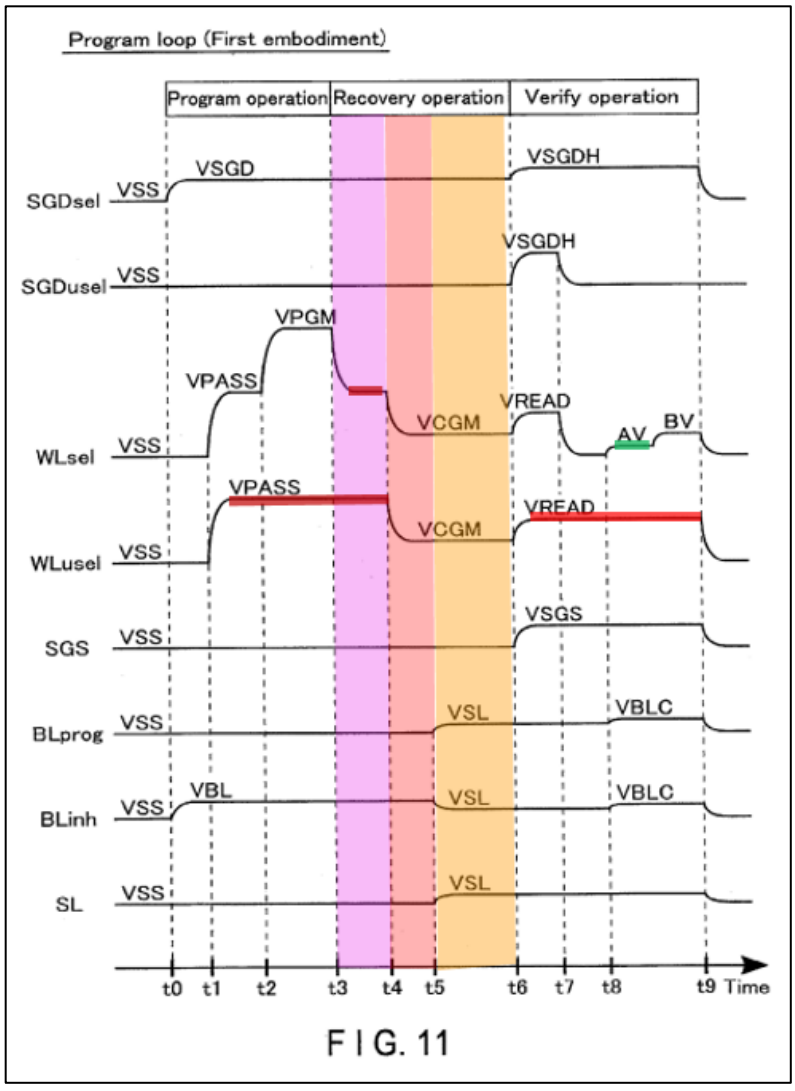
Petitioner contends that the combination of Hongtao and Yu (Ground 1) renders obvious the Challenged Claims. Pet., 27-40. Yu does not teach—and Petitioner does not contend that it teaches—the use of distinct bias voltages during a "pre-verify" and a "verify" stage, with a second bias voltage that is smaller than a first bias voltage, as recited by the Challenged Claims. Furthermore, Yu describes methods for programming and verifying a string of memory cells in a programming order. But Yu does not disclose or suggest that a verification operation includes a separate "pre-verify stage" with a different set of voltages from the "verify stage." Przybylski, ¶60.

C. U.S. 2021/0082505 ("Suzuki") (Ex. 1007)

Petitioner contends that Suzuki (Ground 2) anticipates the Challenged Claims. Pet., 7-8, 74-102. Suzuki purportedly discloses different embodiments of a "program loop," which is divided into a "program operation," "recovery operation," and "verify operation" performed in sequence. *See* Suzuki, [0028]. Przybylski, ¶61.

As illustrated in Fig. 11, the program loop is divided into ten time periods, where "time t0 to time t3 corresponds to a program operation," "time t3 to time t6 corresponds to a recovery operation," and "time t6 to time t9 corresponds to a verify operation." Suzuki, [0131]. As explained in Suzuki, the recovery operation from t3-t6 combines "an end operation of the program operation and the ready operation of

the verify operation." Suzuki, [0131]. Specifically, the recovery operation includes a period from t3-t4 which is an **end operation of the program operation**, a period from t5-t6 with distinct voltages that acts as a **ready operation of the verify operation**, and a period from t4-t5 which is a **transition period** between the two. *See* Suzuki, [0131]. Przybylski, ¶62.



F I G. 11

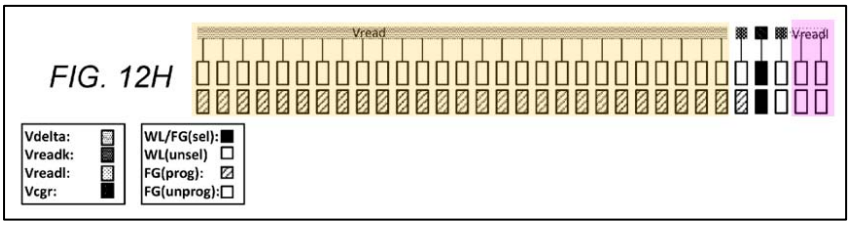
At time t3, the first part of the recovery operation (i.e., the "**end operation of the program operation**"), "**VPASS**" is applied to the selected word line "WLsel,"

and "**VPASS**" continues to be applied to the unselected word line "WLusel." Suzuki, [0134], [0137]. During the latter part of the recovery operation (including the "**ready operation of the verify operation**" from t5-t6), the voltage "VCGM… lower than VPASS" is applied instead. *Id.* [0138]. During the start of the verify operation at time t6, "**VREAD** is applied to each of the word lines" (Suzuki, [0114]), and "verify voltages **AV** and BV" are applied to the selected word line at time t8 (Suzuki, [0145]). The VCGM applied during the "**ready operation of the verify operation**" is lower than **VREAD**. Suzuki, [0141]. Przybylski, ¶63.

Petitioner argues that Suzuki's "**VPASS**" is a "first bias voltage" applied during a "pre-verify stage," and that "**VREAD**" is a smaller "second bias voltage" applied in a verify stage. But the time period t3-t4 when "**VPASS**" (i.e., the purported "first bias voltage") is applied is not a "pre-verify" stage as required by the Challenged Claims. Instead, Suzuki discloses that t3-t4 is "**an end operation of the program operation**." Suzuki, [0131]. The "end operation" is not a "pre-verify" stage at least because it is still part of the programing operation, and it fails to prepare the device for a subsequent "verify stage." Thus, **VPASS** is not applied in a "pre-verify stage" to prepare the memory string for a subsequent verification operation. Przybylski, ¶64.

D. U.S. 2018/0012667 ("Costa") (Ex. 1008)

Petitioner contends that the combination of Costa and Seo (Ground 3) renders obvious the Challenged Claims. *See* Pet. 7-8, 103-126. Costa is purportedly directed to "reducing errors when sensing in non-volatile memory" by using different pass voltages. Costa, [0028]. Specifically, Costa discloses that a lower "pass voltage" can be used for unprogrammed memory cells as compared to programmed memory cells. *See* Costa [0121]-[0122], [0147]. Programming a memory cell increases the threshold voltage, but because the unprogrammed cells are in an erased state, a "lower read pass voltage VreadL can be used while still ensuring that these memory cells operate as pass gates." Costa, [0082], [0122]. For example, as shown in Figure 12H, a generic "**Vread**" value is used for already programmed memory cells, and a lower "**VreadL**" value is used for memory cells that are still unprogrammed:



Przybylski, ¶65.

However, Costa does not disclose the use of separate "verify" and "pre-verify" stages for a verify operation, and Costa only discloses a single bias voltage level being applied to any given memory cell throughout the verification process (e.g., "Vread" for programmed cells, or "VreadL" for unprogrammed cells). At no point

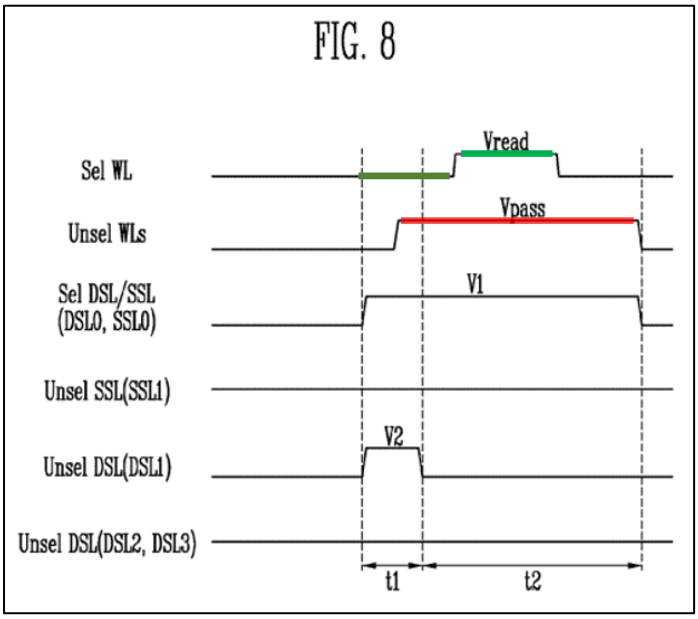
does Costa suggest different bias voltage levels being used for not programmed memory cells in a "verify stage" and a "pre-verify stage" as required by the '957. Moreover, Costa does not teach or otherwise suggest applying a distinct first bias voltage and second bias voltage "on a gate terminal of at least one memory cell of the first memory cell string that is not programmed" during different stages of the verification process. At most, Costa discloses applying different "pass voltages" to different memory cells, but the pass voltage applied to any given memory cell is constant throughout the entire sensing process. Przybylski, ¶66.

E. U.S. 2021/0027848 ("Seo") (Ex. 1009)

Petitioner contends that the combination of Seo and Costa (Ground 3) renders obvious the Challenged Claims. Seo describes a memory device "read" operation is divided into a "first time period t1" and a "second time period t2" with different voltages applied in each period. Seo [0011]. But similar to Costa, Seo fails to disclose multiple different pass voltages (or any other type of purported bias voltage) being applied to an unselected word line at different times. Przybylski, ¶67.

As shown by Fig. 8, Seo discloses different voltages being applied to unselected word lines, "Unsel WLs," and a selected word line "Sel WL." *See* Seo, [0086]-[0090]. With respect to "Sel WL," some **unspecified voltage** is applied during time period t1, which is replaced by "the read voltage **Vread** … during a second time period t2." Seo [0090]. With respect to the "Unsel WLs," "the pass

voltage **Vpass** may be applied to unselected word lines" during both a portion of time period t1 as well as time period t2. Seo [0089]. Przybylski, ¶68.



But Seo does not disclose that the voltages applied to the word lines shown in Fig. 8 result in similar voltages being applied to the gate terminals of the memory cells, nor has Petitioner presented any arguments or evidence that the voltages on the gate terminals would have sufficient time to develop fully and reach the values depicted in Fig. 8. *C.f.* '957, 11:58-12:9, 12:10-27 (discussing that bias voltages need sufficient time to develop fully). But even assuming that the voltages applied to the gate terminals mirror the voltages shown in Fig. 8, Seo does not disclose or render obvious that the value of Vpass applied to a given word line would change between "time period t1" and "time period t2." In fact, Petitioner seemingly concedes that Seo does not disclose the use of distinct bias voltages during a "pre-verify stage"

and a "verify stage," as required by the Challenged Claims. *See* Pet. 26, 103-126. Przybylski, ¶69.

VI. GROUND 1: HONGTAO IN VIEW OF YU DOES NOT DISCLOSE OR RENDER OBVIOUS CLAIMS 1-6

Petitioner has failed to show that Hongtao in view Yu discloses or renders obvious at least limitations [1.a]-[1.b], and [1.d], or the added limitations of dependent claims 5 and 6. Regarding [1.a]-[1.b], Hongtao in view of Yu does not disclose or render obvious applying "first bias" and "first verify" voltages during a "pre-verify" stage. Regarding [1.a] and [1.d], Hongtao in view of Yu further fails to disclose or render obvious applying a "second bias voltage" smaller than a "first bias voltage" on a gate terminal of a not programmed memory cell. As for claims 5 and 6, under Petitioner's interpretation of Hongtao Fig. 2 the purported "top bias voltage" and "bottom bias voltage" identified in the Petition are not applied in "the pre-verify stage and the verify stage" as required by the claims. Przybylski, ¶¶70-73.

A. Independent Claim 1: Hongtao in View of Yu Does Not Disclose or Render Obvious a "Pre-Verify Stage" (Limitations [1.a]-[1.b])

Hongtao in view of Yu does not disclose or render obvious a "pre-verify stage" as required by limitations [1.a]-[1.b]. Hongtao does not disclose or render obvious any type of verify operation, much less one that includes a distinct "pre-verify stage." Similarly, Yu does not disclose or render obvious a verify operation that includes a "pre-verify stage." Moreover, Petitioner's proposed combination fails to show that

a POSITA would have been motivated to apply Hongtao's teachings to Yu to render obvious a verify operation that includes a distinct "pre-verify stage" as required by the Challenged Claims. Przybylski, ¶¶74-75.

Claim 1 of the '957 recites processing circuitry configured to: "**apply, in the pre-verify stage**, a first bias voltage on a gate terminal of at least one memory cell of the first memory cell string that is not programmed" (Element [1.b]); and "**apply, in the pre-verify stage**, a first bias voltage on a gate terminal of at least one memory cell of the first memory cell string that is not programmed" (Element [1.b]). These limitations are common to each of the Challenged Claims by virtue of their dependency on claim 1 of the '957. Przybylski, ¶76.

As explained in Section II, and illustrated in Fig. 6 below, the claimed invention of the '957 improves over conventional systems, in part, by separating a verification operation into a distinct **pre-verify stage** and **verify stage** with distinct voltages applied in each. *See* '957, 1:58-2:8, 6:37-49, 17:32-56. By doing so, "the gradient of the channel potential of the selected memory cell string can be reduced," and as a result "HCI cannot be generated from the selected memory cell to the upper adjacent memory cell … in the selected memory cell string."

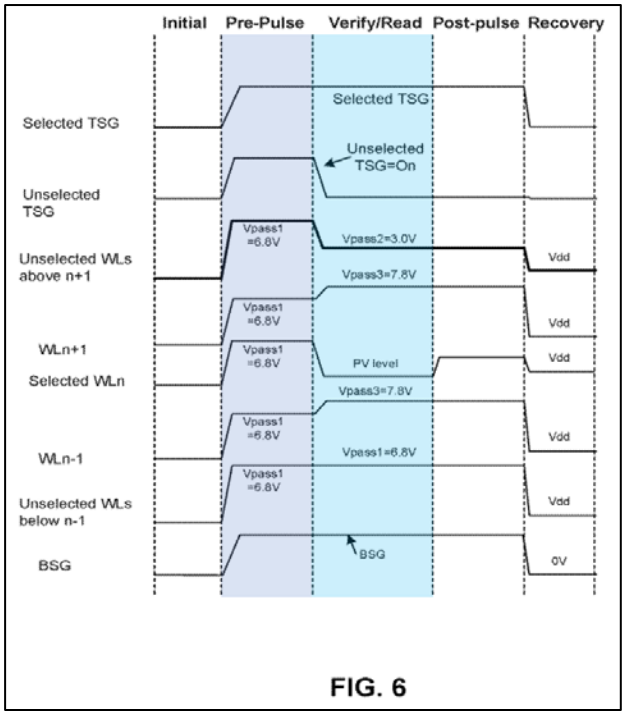


FIG. 6

'957, 12:63-13:4, Fig. 6. By comparison, Hongtao and Yu fail to disclose or render obvious any type of multi-stage verification operation. Przybylski, ¶77.

Hongtao is explicitly directed to a "reading method" for 3D NAND and does not disclose any type of verify operation. *See* Hongtao, Abstract. To the extent Hongtao describes a reading operation with separate pre-conduction and reading phases, it does not teach or suggest applying those teachings to create a verification operation with distinct "pre-verify" and "verify" stages as required by the Challenged Claims. *See* Hongtao, [0005]-[0007]. Przybylski, ¶78.

Yu does not address this deficiency, and similarly fails to disclose a "pre-verify stage." Yu states that "[e]ach program loop may include … a program verification operation" that includes applying "a program verification voltage to the

first word line" and "a verification pass voltage to the unselected word lines." Yu, [0049], [0054]. Yu does not disclose or render obvious a verification operation with a "pre-verify stage" and a "verify stage," nor does Petitioner contend that Yu does. Przybylski, ¶79.

The Petition also fails to show that a POSITA would have combined Hongtao and Yu to create a verification operation with a distinct "pre-verify stage." Specifically, the Petition improperly asserts a POSITA would have been motivated to apply Hongtao's read operations to perform verification operations as described in Yu because "read operations and verify operations are virtually identical" and "fine-tuned read operations" would also be suitable for verifying. *See* Pet. 72-74. That is incorrect. Reading and verifying are distinct operations that each carry their own concerns, and the art is replete with examples of the two being treated differently.[3] *See, e.g.*, Ex. 1021, [0103]; Ex. 1020, 16:16-21; Ex. 1019, 17:10-14; Ex. 1017, 3:21-29. Differences also arise from verification being an iterative check within a programming cycle that follows each programming step, while reading

[3] The '957 itself refers to a "verify/read" operation, but does so in the context of describing the sensing portion of a verify operation that uses a "programming verify (PV) level" to sense when a "selected memory cell is programmed correctly." *See* '957 Fig. 4, 11:35-57. Przybylski, ¶83.

operations are independent processes to check the stored state of a cell. For example, when using a fixed programming order such as in Yu (*see* Yu, [0115]), verify operations are uniquely capable of using lower bias voltages on memory cells above (or below) the selected memory cell because they are known to be unprogrammed beforehand. *See, e.g.*, '957, 12:28-13:4, Fig. 6 (using lower voltages on WLs above n+1 during the verify stage as compared to WLs below n-1); Costa [0122]. The Petition does not address these differences between the two operations, and has presented no arguments or evidence beyond conclusory assertions to show that a POSITA would have been motivated to apply Hongtao's disclosures to Yu's verify operations. Przybylski, ¶¶81-82.

Moreover, as correctly recognized by the Decision to Institute ("DI") in the context of Ground 3, even assuming teachings about reading operations were applicable to verify operations, a read operation divided into two time periods does not necessarily equate to a "pre-verify stage" and "verify stage." DI, 26-27 (the reference "only describes time periods t1 and t2 with respect to performing a read operation … it is not clear that time period t1 is a 'pre-verify stage' as claimed"). Petitioner and Dr. Liu gloss over this deficiency by conflating read and verify operations and misrepresenting Hongtao as disclosing a "read/verify phase" despite that term appearing nowhere in Hongtao. *See* Pet., 32; Liu, ¶105. Hongtao does not disclose a "read/verify phase," and to the extent Hongtao discloses a "pre-conduction

phase" that precedes a reading operation for the purpose of mitigating read disturb, it does not follow that a POSITA would have been motivated to combine Hongtao and Yu to render obvious a verification operation that is divided into distinct "pre-verify" and "verify" stages with separate voltages being applied in each. Przybylski, ¶84.

For at least the reasons above, Hongtao in view of Yu fails to disclose or render obvious applying bias and verify voltages during a "pre-verify stage" as required by limitations [1.a]-[1.b]. Przybylski, ¶85.

Hongtao in view of Yu also fails to disclose or render obvious dependent claims 2-6 for at least the same reasons. Przybylski, ¶86.

B. Independent Claim 1: Hongtao in View of Yu Does Not Disclose or Render Obvious Applying "a First Bias Voltage" and "a Second Bias Voltage" on the Gate Terminal of a Not Programmed Memory Cell "Wherein the Second Bias Voltage Is Smaller than the First Bias Voltage" (Limitations [1.b], [1.d])

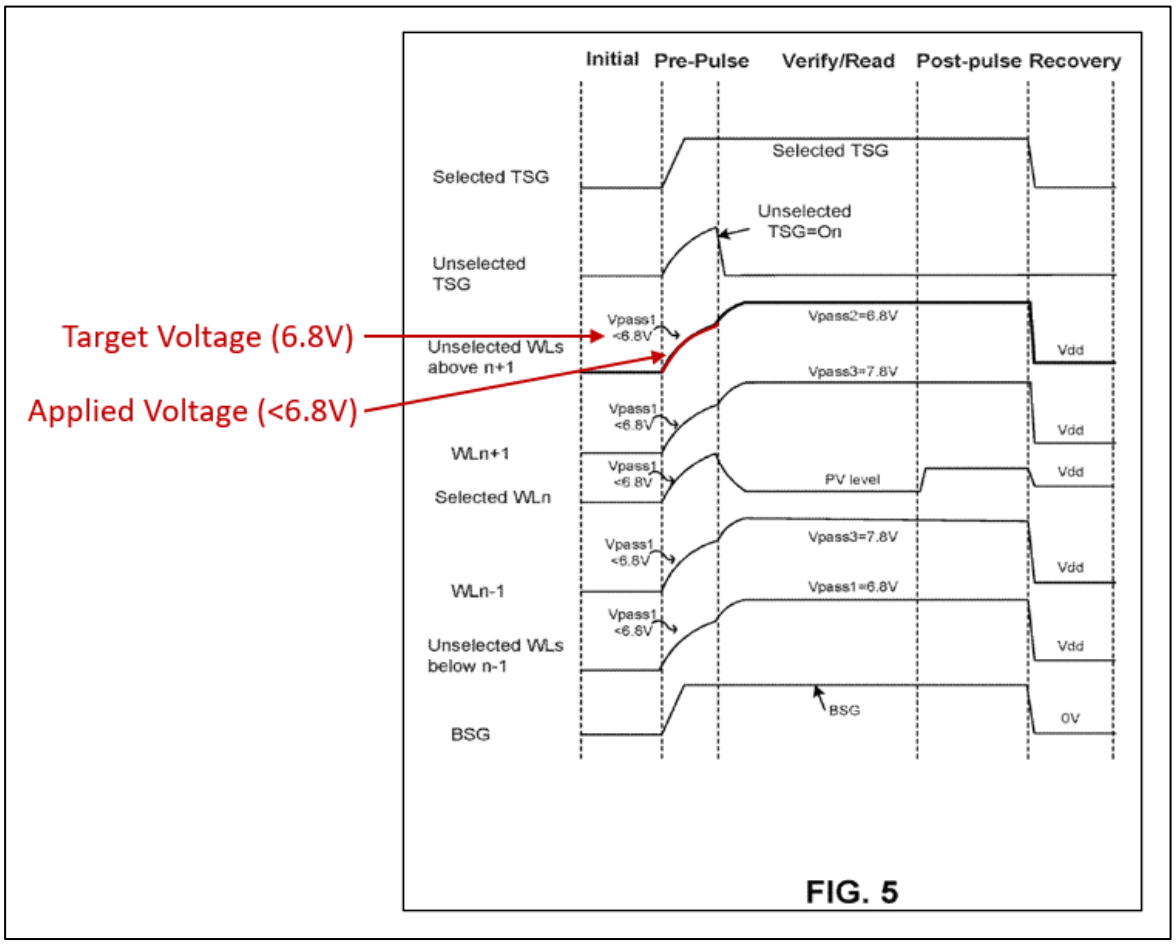
Hongtao in view of Yu does not disclose or render obvious limitations [1.b] and [1.d] because Fig. 2 of Hongtao would not have suggested to a POSITA that an applied "second bias voltage on a gate terminal" is smaller than an applied "first bias voltage on a gate terminal." *See* Pet., 39-40. Petitioner relies on Fig. 2 of Hongtao as purportedly disclosing this limitation (*id.*), but Figure 2 of Hongtao depicts target voltages applied to word lines, not the resulting voltages applied on gate terminals of the memory cells. The Petition ignores this distinction and misrepresents Hongtao

by doing so. Properly interpreted, a POSITA would not have understood Fig. 2 of Hongtao to disclose or render obvious that an applied "second bias voltage on a gate terminal" is smaller than an applied "first bias voltage" as required by the Challenged Claims. Przybylski, ¶¶87-88.

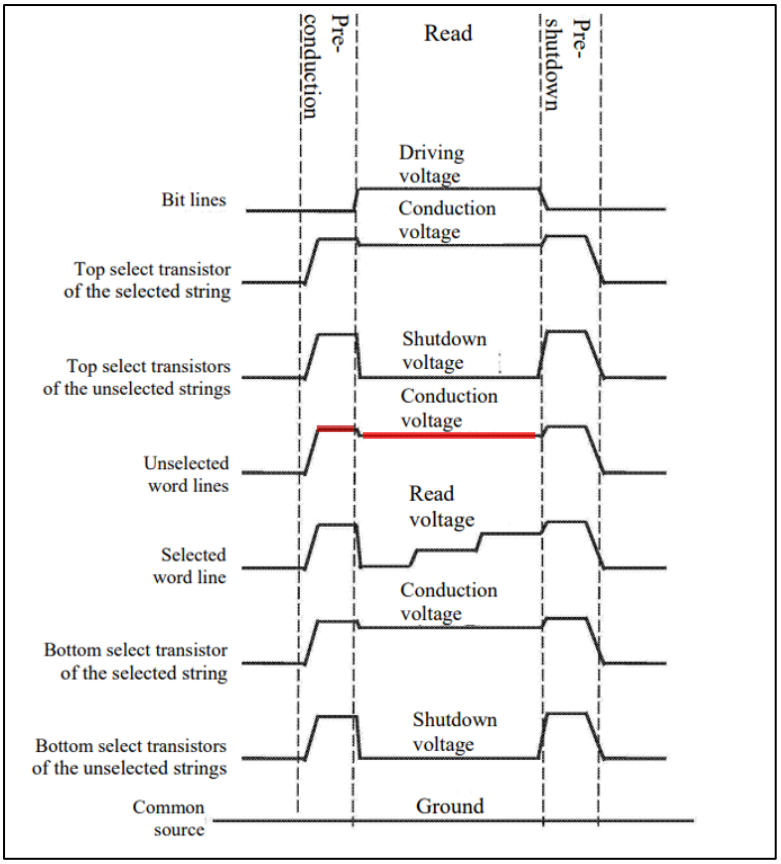
Claim 1 of the '957 recites processing circuitry configured to: "**apply, in the pre-verify stage, a first bias voltage on a gate terminal of at least one memory cell of the first memory cell string that is not programmed**" (Element [1.b]); and "**apply, in the verify stage, a second bias voltage on the gate terminal of the at least one memory cell of the first memory cell string that is not programmed, wherein the second bias voltage is smaller than the first bias voltage**" (Element [1.d]). These limitations are common to each of the Challenged Claims by virtue of their dependency on claim 1 of the '957. Przybylski, ¶89.

As explained in Section II, the '957 improves over conventional systems in part because, by applying "a lower bias voltage" on a gate terminal of an unprogrammed memory cell in the verify stage, "the gradient of the channel potential of the selected memory cell string can be reduced" which helps prevent hot carrier injection (HCI) effects. '957, 12:63-13:4. The '957 also distinguishes between the voltages that may be applied through word line layers during a pre-pulse stage, and the bias voltages applied on the gate terminals of the memory cells that develop over time as a result. *See, e.g.*, '957, 11:68-12:9, 12:10-27. For example,

Fig. 5 of the '957 illustrates how a short pre-pulse period may prevent the applied "bias voltages" experienced by the gates from developing fully, resulting in them being "less than a target value, such as 6.8 volts" during the pre-pulse period. '957, 12:18-19. Przybylski, ¶90.



By comparison, Hongtao's text does not describe applying a "second bias voltage" that is smaller than a "first bias voltage" to the gate terminal of an unprogrammed memory cell. Instead, the Petition argues that this subject matter is disclosed based on the depiction of the "**pre-conduction voltage**" and "**conduction voltage**" in Figure 2 of Hongtao (below). *See* Pet. 39-40. Przybylski, ¶91.



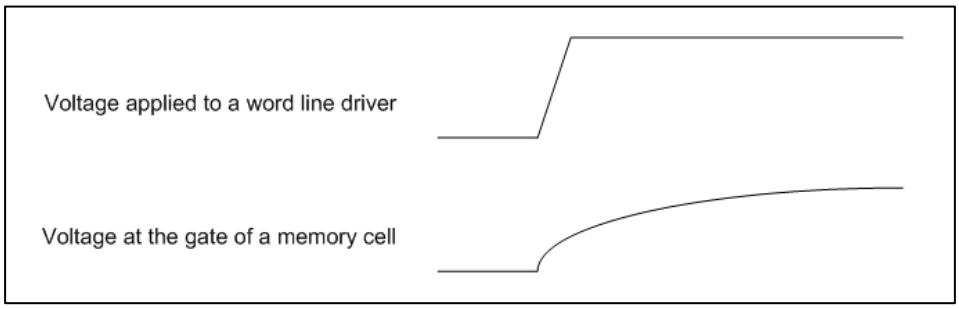
Petitioner incorrectly suggests that this figure discloses processing circuitry configured to "apply, in the pre-verify stage, a first bias voltage on a gate terminal of at least one [not programmed] memory cell," and "apply, in the verify stage, a second bias voltage on the gate terminal of the at least one [not programmed] memory cell … wherein the second bias voltage is smaller than the first bias voltage," as required by the Challenged Claims. Pet. 39-40. Specifically, the Petition argues that Fig. 2 of Hongtao satisfies these limitations because "the voltage signal applied to the unselected word lines ramps down from the pre-conduction voltage to reach the conduction voltage." Pet. 39-40. But that is not what the Challenged Claims

require. Rather, the claims are explicitly directed to the actual voltages applied "***on a gate terminal***" of the memory cell itself. Przybylski, ¶92.

In the Decision to Institute, the Board misinterpreted Fig. 2 of Hongtao as disclosing the voltages applied on gate terminals. *See* DI, 14-15. Specifically, the Board pointed to Hongtao's statement that the "gates of the unselected memory cells on the selected string are applied with a conduction voltage through the unselected word lines," (Hongtao, [0025]), and credited Dr. Liu's testimony that "the respective voltage is applied through a conductor coupled to the corresponding cell or transistor, i.e., a word line coupled to a corresponding memory cell (which in 3D memories, is actually a conductive gate layer)" (Ex. 1003 ("Liu"), ¶56). DI, 14-15. That explanation is incomplete. Rather, a POSITA would have understood Hongtao to be disclosing target voltages rather than actual voltage applied to the gate terminals of the memory cells. Przybylski, ¶93.

In a 3D NAND device, such as the one described by Hongtao or the '957, word lines have an RC time-constant from capacitances arising from the stacked structure. *See* Aritome, 350-353 (discussing "RC (resistance-capacitance) delay" in word lines, and that "[i]n stacked word-line (WL) structure in 3D NAND cells … a WL capacitance is greatly increased from 2D cells"). Drivers, or similar voltage generation circuits, force the word lines to achieve specific target voltages over time. These "target" voltages applied through the word lines will result in distorted

voltages on the gate terminals of the memory cells. For example, as illustrated in the figure prepared by Dr. Pryzbylski below, the actual voltages that develop on the gate terminals of the memory cells will typically appear as curved lines based on the RC time-constant associated with a given word line:



Przybylski, ¶94. The precise RC time-constant, and the waveform that appears on a gate terminal as a result of a given target voltage, depends on several factors including the physical structure of the device and the time scales of the applied waveforms. Przybylski, ¶94.

The fact that actual voltages will be appear distorted and curved was further confirmed by Petitioner's expert, Dr. Liu, during deposition in connection with IPR2024-00795, which involved a challenge to another YMTC patent related to 3D NAND technology. *See* Ex. 2006 ("Liu822 Tr."), 62:16-73:20. When prompted why Fig. 8B of U.S. 10,726,920 ("Yang") (Ex. 2007) show curved waveforms for word line voltages, Dr. Liu explained that the "***signal takes time to go from the voltage generation circuit and be reinserted to the word line***, there would be a parasitic component that causes slight delay in charging the word line." Liu822 Tr., 63:22-

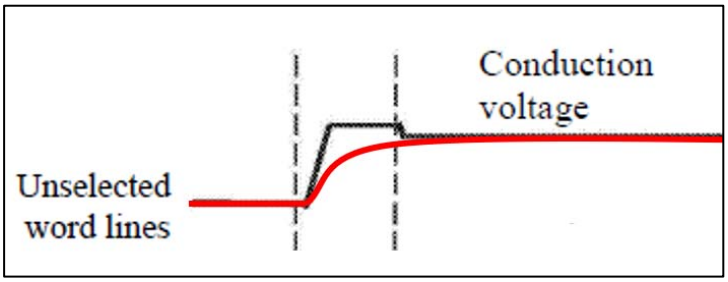
64:3. He also elaborated that "in the real world ***there is always going to be parasitic component[s]***," and that it is "inevitable" there will be "resistance components … [and] capacitor components, so that it's always going to have some type of ramping time." Liu822 Tr., 64:9-22; *see also id.* 65:24-12 (confirming that the curve is determined by an "R and C component," which depends on the "design" and "architecture" of the device). Przybylski, ¶95.

Unlike the '957, Hongtao does not contemplate that voltages need time to develop, and Fig. 2 of Hongtao alone is insufficient to determine the actual voltages that develop on the gate terminals of memory cells. Drawings can be relied on for invalidity purposes only for what they reasonably disclose to a POSITA. *See PlaSmart, Inc. v. Kappos*, 482 F. App'x 568, 572 (Fed. Cir. 2012) (drawings can be relied on for invalidity "only if the prior art features are clearly disclosed"); MPEP 2125 ("drawings must be evaluated for what they reasonably disclose and suggest to one of ordinary skill in the art"). But the traces illustrated in Fig. 2 of Hongtao show steep slew rates (i.e., rates of change of voltage over time), straight lines, and abrupt changes indicative of target voltages. Hongtao does not teach or suggest that the waveforms shown in Fig. 2 are actual voltages applied on the gate terminals of the memory cells, nor does Hongtao provide the necessary details, such as the duration of the pre-conduction period and architecture of the device, to infer how the resulting voltages on the gate terminals of the memory cells would develop over time.

C.f. ’957, 11:58-12:9, 12:10-27 (discussing that bias voltages need sufficient time to develop fully and providing examples). Petitioner and Dr. Liu have also failed to provide evidence or arguments addressing this gap. Przybylski, ¶96.

Contrary to what Dr. Liu suggests in his declaration at ¶120, the supposed “drop” illustrated in Fig. 2 of Hongtao does not correspond to the voltage on the gate terminal of the memory cell being reduced. *See* Hongtao Fig. 2. Indeed, Hongtao does not establish that the voltages on the gate terminals actually reach the target voltages illustrated in Fig. 2 during the pre-conduction phase. *C.f.*, ’957, 12:10-27 (bias voltages that do not fully develop in a given stage can continue to develop and reach the target value in later stages). As explained by Dr. Przybylski, a pre-conduction phase should be long-enough only to precharge the unselected memory strings, as any excess time needlessly adds to the overall device read access time. Given that context, the waveform illustrated in Fig. 2 of Hongtao appears to be a technique to minimize the pre-conduction time by applying a target voltage to the word lines that is somewhat elevated at the start. This causes voltages being applied to ramp up faster, and thus minimize the overall pre-conduction time. Hongtao does not provide sufficient details to know how the corresponding bias voltages applied on the gates of the memory cells develop over time, nor have Petitioner and Dr. Liu provided any explanation or evidence for how the corresponding bias voltages would develop over time. But in typical systems, voltages of the type illustrated in Hongtao

would be expected to result in bias voltages that are smoothed-out and appear as follows:



See Przybylski, ¶98. This is also supported by the fact that, absent good reason, voltages applied in the pre-conduction and reading phases should remain constant in order to avoid creating coupling effects or transient currents along the length of the memory string that could interfere with sensing the state of the selected memory cell. Przybylski, ¶¶97-99.

In evaluating Hongtao, Petitioner and Dr. Liu have overlooked the distinction drawn in the '957 between target voltages applied through word line layers and the actual applied bias voltages on the gate terminals of the memory cells that develop over time as a result. *See* Section II. Petitioner has not even attempted to address what—if anything—a POSITA could have determined about the applied bias voltages on the gate terminals of the unprogrammed memory cells from Fig. 2 of Hongtao. Przybylski, ¶100.

Apart from Fig. 2, the Petition provides one more flawed argument for why Hongtao would suggest applying a lower bias voltage in the reading phase as

compared to the pre-conduction phase. *See* Hongtao Fig. 2. Specifically, the Petition mischaracterizes paragraph [0026] of Hongtao as suggesting that bias voltages should be reduced during a read phase. *See* Pet. 22, 40. But paragraph [0026] of Hongtao says nothing about lowering bias voltages, nor does it suggest that Fig. 2 of Hongtao is illustrating the applied bias voltages that actually develop "on a gate terminal of a [not programmed] memory cell," rather than the target voltages applied to the word line layer. *See* Pet. 40. Przybylski, ¶101.

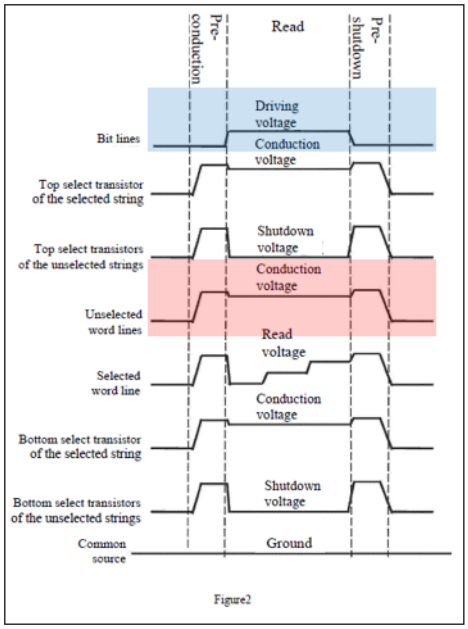
The Petition mischaracterizes the statement from paragraph [0026] of Hongtao that "the greater the conduction voltage, the greater the read disturbance" as explaining why a POSITA might reduce bias voltages in a reading phase (i.e., as purportedly illustrated in Fig. 2). *See* Pet. 22, 40; Liu ¶120. But that quote, which the Petition presents out of context, says nothing about the bias voltages on the gate terminals of the memory cells, or reducing voltages in a reading phase. Rather, [0026] describes ***problems*** in the embodiment of Fig. 2 arising from differences between a "conduction voltage" and a bit line "driving voltage" in order to introduce the embodiment of Fig. 3:

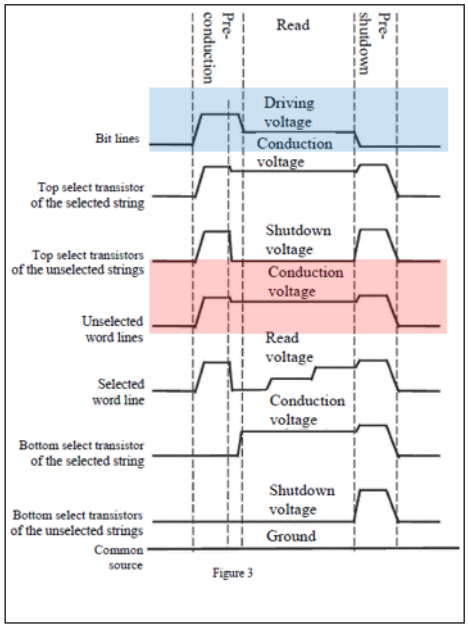
> Read interference is positively related to the voltage causing read interference. The greater the voltage, the stronger the read interference. Therefore, the greater the conduction voltage, the greater the read disturbance to the memory cell. Therefore, in this specific embodiment, ***the read interference caused by the "conduction voltage - driving***

> ***voltage***" suffered by the unselected memory cells on the selected string is smaller than the read interference suffered by the memory cells on the unselected string. In order to improve the accuracy of memory reading, it is necessary to further reduce the read interference suffered by the memory cells on the unselected string.

Hongtao [0026]-[0028]. Przybylski, ¶102.

Hongtao proceeds to describe the embodiment of Fig. 3 to "further reduce the read interference" relative to Fig. 2. Hongtao [0027]-[0028], Fig. 3. Accordingly, Hongtao [0026] is not describing some rationale for reducing the bias voltages in a reading phase as compared to a pre-conduction phase. Rather, it is explaining a problem in Fig. 2, which Hongtao addresses in Fig. 3 by applying a pre-conduction voltage to the bit lines that will "precharge" the unselected strings and "effectively reduce read disturbance." Hongtao [0034], Fig. 2, Fig. 3.





The fact that paragraph [0026] has nothing to do with reducing bias voltages is also confirmed by Fig. 3 depicting the exact same waveforms as Fig. 2 for the unselected waveforms. In short, paragraph [0026] of Hongtao does not support Petitioner's purported interpretation and is irrelevant because it says nothing about the resulting voltages on the gate terminals of the memory cells. Przybylski, ¶103.

Yu likewise does not disclose applying multiple different bias voltages, and Petitioner does not allege that it does. Petitioner relies on Yu as allegedly teaching certain aspects of programming operations, including the use of a programming order. *See* Pet. 22, 29, 31, 33-34. But Yu is silent as to the bias voltages applied during pre-verify and verify stages of a verification operation, and is unable to address the deficiencies in Hongtao. Przybylski, ¶104.

For at least the reasons above, Hongtao and Yu, alone or in combination, fail to disclose or render processing circuitry configured to "apply … a first bias voltage on a gate terminal of at least one memory cell of the first memory cell string that is not programmed," and "a second bias voltage on the gate terminal of the at least one memory cell of the first memory cell string that is not programmed, wherein the second bias voltage is smaller than the first bias voltage" as recited by limitations [1.b] and [1.d]. Rather, Petitioner's arguments have simply ignored the distinction drawn in the '957 between target voltages, and the applied bias voltages that appear on the gate terminals of the memory cells. Przybylski, ¶105.

Hongtao in view of Yu also fails to disclose or render obvious dependent claims 2-6 for at least the same reasons. Przybylski, ¶106.

C. Claims 5 and 6: Hongtao in View of Yu Does Not Disclose or Render Obvious a "Top Bias Voltage" or "Bottom Bias Voltage" Applied "In the Pre-Verify Stage and the Verify Stage"

In addition, Hongtao in view of Yu does not disclose or render obvious the added limitations of claims 5 and 6 requiring that a "top bias voltage" and a "bottom bias voltage" are applied "in the pre-verify stage ***and*** the verify stage." Rather, Petitioner has incorrectly attempted to map these limitations onto multiple different voltages, none of which is applied in both the "pre-verify stage and the verify stage." Przybylski, ¶107.

The added limitations of dependent claim 5 recite processing circuitry further configured to: "**apply a bottom bias voltage on a gate terminal of the BSG transistor … in the pre-verify stage and the verify stage**;" and "**apply a top bias voltage on a gate terminal of the TSG transistor … in the pre-verify stage and the verify stage**." Analogous limitations are also found in dependent claim 6. Przybylski, ¶¶109.

As discussed in Section VI.B (Claim Construction), the plain and ordinary meaning of the term "apply a [top/bottom] bias voltage on a gate terminal of the [TSG/BSG] transistor of the first memory cell string ***in the pre-verify stage and the verify stage***" requires a single voltage level be applied in ***both*** the pre-verify stage

and the verify stage. For example, as illustrated in Fig. 4 of the '957, a "**bias voltage (or bottom bias voltage), such as 5 volts**" is applied to the BSG layer, and "**bias voltage (or top bias voltage), such as 5 volts**" is applied to the selected TSG layer during the "**pre-pulse stage**," and is "maintained" during the subsequent **verify/read stage**.

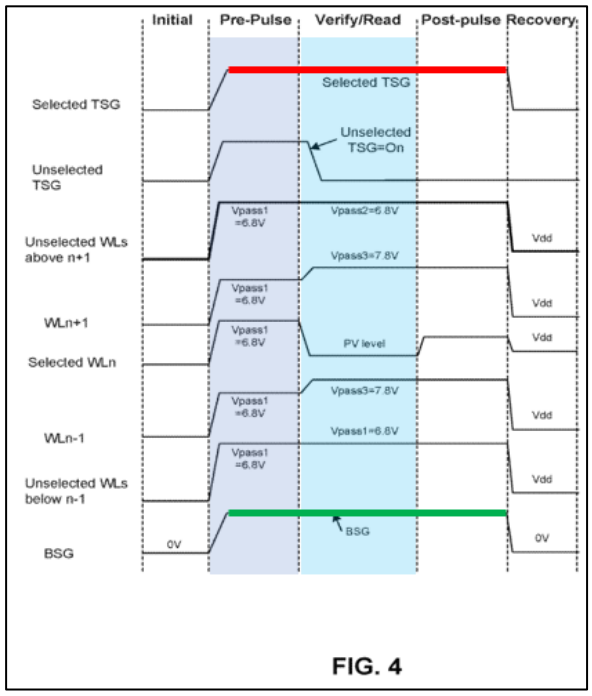
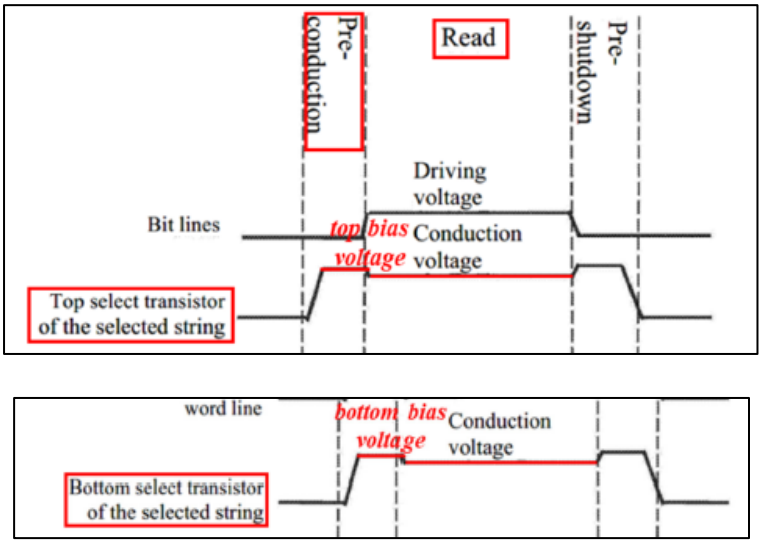


FIG. 4

'957, 10:57-11:15 (describing the pre-pulse stage), 11:16-57 (describing the verify/read stage), Fig. 4. Przybylski, ¶110.

Petitioner relies on Hongtao as purportedly disclosing this subject matter, but under Petitioner's proposed interpretation of Hongtao, there are no top/bottom bias voltages applied in "the pre-verify stage ***and*** the verify stage." As discussed in relation to independent claim 1, Fig. 2 of Hongtao illustrates target voltages rather than the actual voltages applied on the gate terminals of the transistors. *See* Section

VI.B. But if the Board were to find, as Petitioner wrongly asserts, that Fig. 2 of Hongtao illustrates actual gate voltages, Hongtao does not disclose top/bottom bias voltages applied "in the pre-verify stage ***and*** the verify stage" as required by claims 5 and 6. Rather, as shown by the annotated copies of Fig. 2 included in the Petition (reproduced below), Hongtao explicitly shows ***different*** target voltages being applied to the select gates during the different stages. Pet. 61-69. Przybylski, ¶¶111-112.



Petitioner, recognizing this deficiency, incorrectly argues that the claims are nonetheless satisfied because the claimed bias voltages may have "more than one voltage level." *See* Petition 62-64, 96-98. As discussed in Section VI.B (Claim Construction), the plain and ordinary meaning of the term "apply a [top/bottom] bias voltage on a gate terminal of the [TSG/BSG] transistor of the first memory cell string ***in the pre-verify stage and the verify stage***" requires a single voltage level be applied

in ***both*** the pre-verify stage and the verify stage. That understanding is further consistent with all the embodiments in the '957, and basic principles of claim interpretation. Petitioner's arguments to the contrary misrepresent the disclosure in '957 Fig. 7 and contradict Federal Circuit precedent that reciting "***a***" bias voltage "is a separate issue from whether the claims require the same component to perform multiple functions or satisfy multiple limitations of a claim." *Finjan*, 84 F.4th at 974-975. Even if the claims permit multiple distinct bias voltages, at least one of them must be applied in both "the pre-verify stage and the verify stage." *See id.*, at 975 ("Even if an infringing system can use 'one or more computers,' the plain language of the claims requires at least one of those computers to perform all the functions listed in the claims"); *Salazar*, 64 F.4th at 1318 (Fed. Cir. 2023) ("[I]t does not suffice to have multiple [claimed elements], each able to perform just one of the recited functions; the claim language requires at least one [claimed element] capable of performing each of the recited functions."). Przybylski, ¶113.

Yu fails to address these deficiencies. Yu does not disclose or render obvious that bias voltages are applied to TSG and BSG transistors in the pre-verify stage and verify stage, and Petitioner does not allege that it does. *See* Pet. 61-69. Przybylski, ¶114.

For at least the reasons above, Hongtao in view of Yu fails to disclose or render obvious processing circuitry configured to "apply a bottom bias voltage on a

gate terminal of the BSG transistor … in the pre-verify stage and the verify stage" and "apply a top bias voltage on a gate terminal of the TSG transistor … in the pre-verify stage and the verify stage" as required by claims 5 and 6. Przybylski, ¶115.

VII. GROUND 2: SUZUKI DOES NOT DISCLOSE CLAIMS 1-6

Petitioner has failed to show that Suzuki anticipates at least limitations [1.b], and [1.d], or the added limitations of dependent claims 5 and 6.[4] Regarding [1.b] and [1.d], Suzuki does not disclose applying a "first bias voltage" in a "pre-verify stage" and a smaller "second bias voltage" in a "verify stage." Indeed, the purported "first bias voltage" identified in the Petition is not applied in a "pre-verify stage," and the other voltages disclosed in Suzuki would similarly fail to satisfy the claim limitations. As for the added limitations of dependent claims 5 and 6, Suzuki does not disclose a "top bias voltage" or a "bottom bias voltage" that is applied in "the pre-verify stage and the verify stage" as required by the claims. Przybylski, ¶¶116-118.

[4] Ground 2 argues that Suzuki anticipates the Challenged Claims, and does not raise any obviousness arguments. Pet. 7-8. But even if Petitioner had raised obviousness, the '957 would still be valid over Suzuki as its proofs fail for at least the same reasons. Przybylski, ¶119.

A. Independent Claim 1: Suzuki Does Not Disclose Applying a First Verify Voltage and First Bias Voltage in a "Pre-Verify" Stage, or Applying a Second Bias Voltage in a "Verify" Stage "Wherein the Second Bias Voltage Is Smaller than the First Bias Voltage" (Limitations [1.b], [1.d])

Suzuki does not disclose limitations [1.b] and [1.d] because Suzuki's "VPASS" voltage, which Petitioner identifies as equivalent to the claimed "first bias voltage," is not applied in a "pre-verify stage." *See* Pet. 74-85. Petitioner's assertion that the identified voltage occurs during a "pre-verify" stage contradicts Suzuki's own disclosure as well as the plain and ordinary meaning of the claim language. Moreover, even if Suzuki disclosed a pre-verify stage preceding a verify stage, the voltages applied during that period would not satisfy the claim limitations requiring that the "second bias voltage" applied in the verify stage be "smaller than the first bias voltage" applied in the pre-verify stage. Przybylski, ¶¶120-121.

Claim 1 recites processing circuitry configured to: "**apply, in a pre-verify stage, a first bias voltage on a gate terminal of at least one memory cell of the first memory cell string that is not programmed**" (Element [1.b]); and "**apply, in the verify stage, a second bias voltage on the gate terminal of the at least one memory cell of the first memory cell string that is not programmed, wherein the second bias voltage is smaller than the first bias voltage**" (Element [1.d]). These limitations are common to each of the Challenged Claims by virtue of their dependency on claim 1 of the '957. Przybylski, ¶122.

As explained in Section II, the claimed invention of the '957 recites an improved approach for performing verification operations using a two-stage approach that mitigates HCI and resulting ESUM losses. As shown in Fig. 6, that includes preparing the memory string for verification by applying a **first bias voltage** that fully develops on a not programmed memory cell during a **pre-verify stage**, and then applying a **second bias voltage** (lower than the first verify voltage) during the subsequent **verify stage**. '957, 1:58-2:8, 6:37-49, 17:32-56.

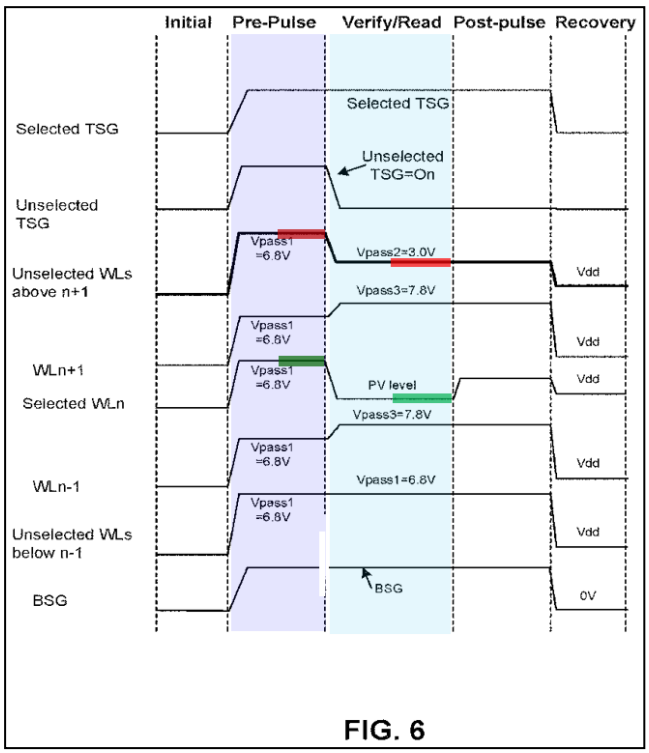


FIG. 6

'957, Figure 6 (annotated); *see also* Section II. Przybylski, ¶123.

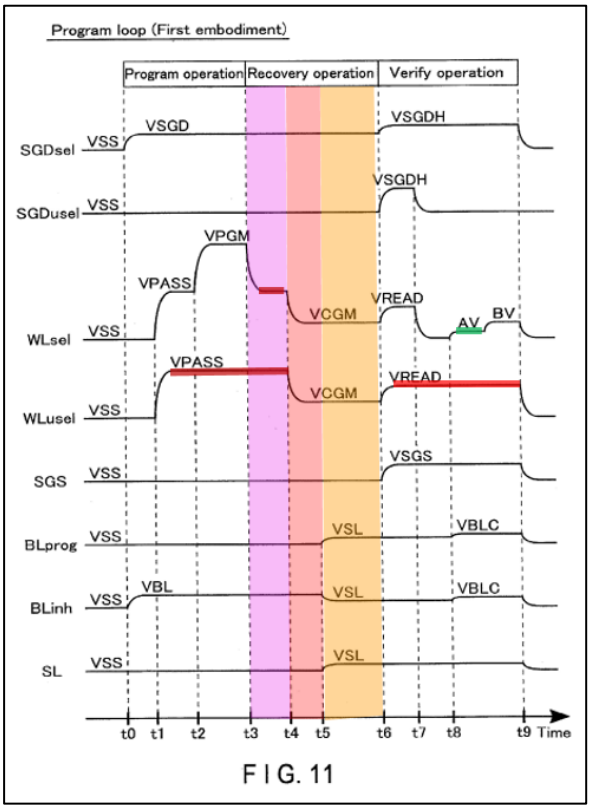
Unlike the claimed invention of the '957, Suzuki does not disclose a first bias voltage during a "pre-verify stage," wherein the first bias voltage is larger than the second bias voltage. Petitioner argues that Suzuki only anticipates the Challenged

Claims under 35 U.S.C. §102 and does not raise any obviousness arguments under §103. *See* Pet. 7-8. "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631 (Fed. Cir. 1987). Przybylski, ¶124.

Suzuki discloses a programming loop that is divided into multiple distinct time periods. As shown in Fig. 11 below, "time t0 to time t3 corresponds to a program operation," "time t3 to time t6 corresponds to a recovery operation," and "time t6 to time t9 corresponds to a verify operation." Suzuki, [0131]. As explained in Suzuki, the recovery operation from t3-t6 combines "an end operation of the program operation and the ready operation of the verify operation." Suzuki, [0131]. Specifically, the recovery operation includes a period from t3-t4 which is an **end operation of the program operation**, a period from t5-t6 with distinct voltages that acts as a **ready operation of the verify operation**, and a period from t4-t5 which is a **transition period** between the two. *See* Suzuki, [0131].[5] These different parts of

[5] In the Decision to Institute, the Board questioned if period t3-t4 also qualified as a "ready operation of the verify operation." DI, 20. Suzuki's "recovery operation" contains an "end operation" and a "ready operation" within it, that does not mean that the ***entirety*** of the recovery operation is itself a "ready operation." Rather, the

the recovery operation are related to the different voltages applied in each one. Przybylski, ¶125.



F I G. 11

For example, the period starting at t3 (i.e., an **end operation of the program operation**) still uses voltages characteristic of a programming phase by lowering the voltage on the selected word line to "VPASS" but otherwise maintaining the

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voltages applied in during the time period t3-t4 are the same as the voltages applied from t1-t2 at the start of the programming operation, confirming that the voltages in t3-t4 are an "end operation of the program operation" and do not themselves ready the device for a verify operation. *See* Suzuki, Fig. 11. Przybylski, ¶126.

voltages used during programming—including a bit line voltage on the "program-inhibited bit line BLinh" that prevents unselected memory strings from inadvertent programming. *See* Suzuki, [0133]-[0135], [0137]. By comparison, the period starting at t5 (i.e., a **ready operation of the verify operation**) is when voltages are applied in anticipation of the verify operation starting at t6, which includes applying "a voltage VSL … to each of the bit lines BLprog and BLinh and the source line SL" as VCGM voltages are maintained on both selected and unselected word lines. Suzuki, [0139]. Unlike Hongtao and Seo, which illustrate target voltages, the curved lines shown in Suzuki are indicative of actual bias voltages applied on gate terminals. However, the voltages illustrated in Suzuki still fail to disclose the features recited in the Challenged Claims. Przybylski, ¶127.

Petitioner incorrectly argues that the "**VPASS**" signal applied from time period t3-t4 is equivalent to the claimed "first bias voltage" applied during a "pre-verify stage." *See* Pet. 79-82. Petitioner pointed to **VPASS** because it needed to find a voltage larger than **VREAD** in order to satisfy Element [1.d]. Petitioner's argument fails at least because the time period from t3-t4 is not part of Suzuki's "**ready operation of the verify operation**" (i.e., is not part of a purported pre-verify operation as the Petition seems to suggest). Rather, the voltages applied in the time period from t3-t4 is an "**end operation of the program operation**," and do not serve to prepare the device for the subsequent verify operation. Suzuki, [0131]. The

Petition does not address this disclosure, or the purposes of the voltages applied throughout the different portions of the recovery operation. Przybylski, ¶128.

Suzuki's program operation—including the "end operation of the program operation" at t3-t4—does not qualify as a "pre-verify stage" under any reasonable interpretation of that term, nor would the "**VPASS**" signal qualify as a first bias voltage applied during a "pre-verify stage." Indeed the "**VPASS**" signal applied to unselected word lines from t1-t4 begins during a programming operation, is maintained for a brief period afterwards, and serves no purpose related to the subsequent "verify operation" from t6-t9. *See* Suzuki [0131], [0133]-[0135], [0137], Fig. 11. The fact that the time period t3-t4 is not a "pre-verify stage" is further confirmed by the fact that the other voltages applied during that t3-t4 period also do not prepare the device for the purported "verify stage." *See id*. Rather, for all of the waveforms described in Fig. 11, the voltages from t3-t4 (i.e., the **end operation of the program operation**) mirror the voltages used during t1-t2 at the start of the programming operation. *See* Suzuki, Fig. 11 (showing the same voltages in t1-t2 and t3-t4). Przybylski, ¶129.

As for Suzuki's "**ready operation of the verify operation**" illustrated from t5-t6, a comparison between Suzuki and the '957 illustrates the stark difference between the two approaches. In the '957, the bias voltage applied during the verify/read stage is ***smaller*** than the preceding bias voltage. '957, Fig. 6. But in

Suzuki, the VREAD voltage is ***larger*** that the VCGM voltage applied during the "ready operation of the verify operation." Suzuki, Fig. 11, [0131], [0142]. Przybylski, ¶130.

Indeed, even if Petitioner presented a different argument and instead tried to map the claimed "first bias voltage" to Suzuki's "VCGM" voltage that is applied during the "**ready operation of the verify operation**," Suzuki still would not anticipate the Challenged Claims. *See* Suzuki, [0131], [0138]-[0139]. The Challenged Claims require applying "a second bias voltage" during the verify stage that is "smaller than the first bias voltage." But Suzuki discloses the opposite, explicitly stating that "**VREAD**" (i.e., the purported "second bias voltage" identified by Petitioner) "is a higher voltage than VCGM." Suzuki, [0142]. Przybylski, ¶131.

For at least the reasons above, Petitioner's proposed mapping of Suzuki fails to disclose a "first bias voltage" applied during a "pre-verify stage" as required by limitation [1.b]. Moreover, even if Petitioner had modified its proposed mapping to point to voltages that are applied during Suzuki's ready operation immediately prior to the purported verification stage (e.g., if Petitioner had pointed to VCGM from t5 to t6), Suzuki still fails to disclose "wherein the second bias voltage is smaller than the first bias voltage" as required by limitations [1.b] and [1.d]. Przybylski, ¶132.

Suzuki also fails to disclose dependent claims 2-6 for at least the same reasons. Przybylski, ¶133.

B. Claims 5 and 6: Suzuki Does Not Disclose a "Top Bias Voltage" or "Bottom Bias Voltage" Applied "In the Pre-Verify Stage and the Verify Stage"

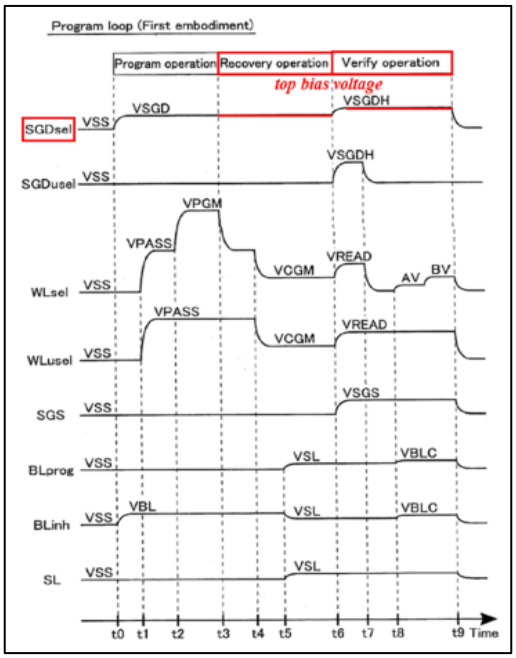
In addition, Suzuki does not disclose the added limitations of claims 5 and 6 requiring that a "top bias voltage" and a "bottom bias voltage" are applied "in the pre-verify stage ***and*** the verify stage." Rather, Petitioner has incorrectly attempted to map these limitations onto multiple different voltages, none of which is applied in both the "pre-verify stage and the verify stage." Przybylski, ¶134.

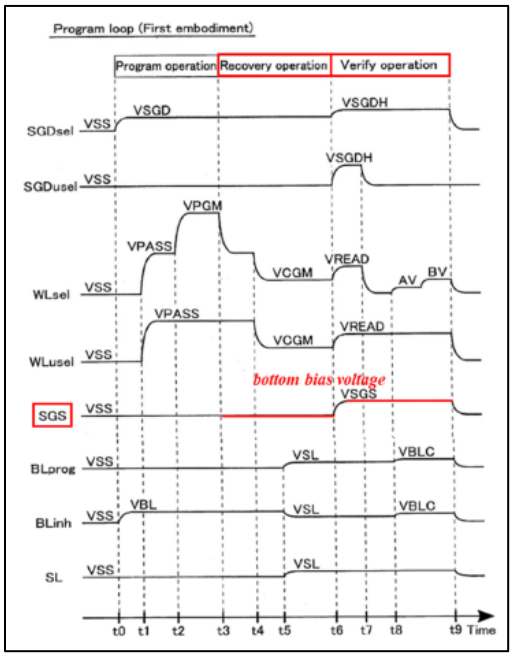
The added limitations of dependent claim 5 recite processing circuitry further configured to: "**apply a bottom bias voltage on a gate terminal of the BSG transistor … in the pre-verify stage and the verify stage**;" and "**apply a top bias voltage on a gate terminal of the TSG transistor … in the pre-verify stage and the verify stage**." Analogous limitations are also found in dependent claim 6. Przybylski, ¶¶135-136.

As discussed in Section VI.B (Claim Construction), the plain and ordinary meaning of the term "apply a [top/bottom] bias voltage on a gate terminal of the [TSG/BSG] transistor of the first memory cell string ***in the pre-verify stage and the verify stage***" requires a single voltage level be applied in ***both*** the pre-verify stage and the verify stage. *See, e.g.*, '957, 10:57-11:15, 11:16-57, Fig. 4. Przybylski, ¶137.

By comparison, none of the purported "top bias voltages" and "bottom bias voltages" in Suzuki identified in the Petition is applied in ***both*** the pre-verify stage

and the verify stage. Unlike Hongtao and Seo, the curved lines illustrated in Suzuki are indicative of actual bias voltages rather than target voltages. But the voltages illustrated in Suzuki as being applied on the select gates are different in the pre-verify and the verify stages. As shown in the annotated images in the Petition (reproduced below), the voltage applied to the purported top select gate changes from a value of "VSGD" to a value of "VSGDH" at the start of the verify stage. Similarly, the voltage applied to the purported bottom select gate changes from a value of "Vss" to a value of "VSGH" at the start of the verify stage.





Pet., 96-102. Neither of these waveforms includes a single voltage level applied in ***both*** the pre-verify stage and the verify stage, as required by claims 5 and 6. *See* Section VI.B (Claim Construction). Przybylski, ¶138.

Similar to Ground 1, Petitioner incorrectly argues that the claims are nonetheless satisfied because the claimed bias voltages may have "more than one voltage level." Petition 62-64, 96-98. But as discussed in Section VI.B (Claim Construction), that arguments contradicts the plain and ordinary meaning of the term "apply a [top/bottom] bias voltage on a gate terminal of the [TSG/BSG] transistor of the first memory cell string ***in the pre-verify stage and the verify stage***," the embodiments of the '957, and basic principles of claim interpretation—and is little more than an attempt to read out limitations of claims 5 and 6. Przybylski, ¶139.

For at least the reasons above, Suzuki fails to disclose processing circuitry configured to "apply a bottom bias voltage on a gate terminal of the BSG transistor … in the pre-verify stage and the verify stage" and "apply a top bias voltage on a gate terminal of the TSG transistor … in the pre-verify stage and the verify stage" as required by claims 5 and 6. Przybylski, ¶140.

VIII. GROUND 3: COSTA IN VIEW OF SEO DOES NOT DISCLOSE OR RENDER OBVIOUS CLAIMS 1-6

Petitioner has failed to show that Costa in view of Seo discloses or renders obvious at least limitations [1.a]-[1.b], and [1.d]. Regarding [1.a]-[1.b], Costa in view of Seo does not disclose or render obvious applying "first bias" and "first verify" voltages during a "pre-verify" stage. Regarding [1.b] and [1.d], Costa in view of Seo further fails to disclose or render obvious applying a "second bias voltage" smaller

than a "first bias voltage" on a gate terminal of a not programmed memory cell. Przybylski, ¶¶141-143.

A. Independent Claim 1: Costa in View of Seo Does Not Disclose or Render Obvious a "Pre-Verify Stage" (Limitations [1.a]-[1.b])

Costa in view of Seo does not disclose or render obvious a "pre-verify stage" as required by limitations [1.a]-[1.b]. Costa does not disclose or render obvious a two-part verify operation that includes a distinct "pre-verify stage." Similarly, Seo does not disclose or render obvious any type of verify operation, much less one that includes a distinct "pre-verify stage." Moreover, Petitioner's proposed combination fails to show that a POSITA would have been motivated to apply Seo's teachings to Costa to render obvious a verify operation that includes a distinct "pre-verify stage" as required by the Challenged Claims. Przybylski, ¶¶144-145.

Claim 1 of the '957 recites processing circuitry configured to: "**apply, in a pre-verify stage**, a first verify voltage on a gate terminal of a selected memory cell of the first memory cell string" (Element [1.a]); and "**apply, in the pre-verify stage**, a first bias voltage on a gate terminal of at least one memory cell of the first memory cell string that is not programmed" (Element [1.b]). These limitations are common to each of the Challenged Claims by virtue of their dependency on claim 1 of the '957. Przybylski, ¶146.

As explained in Section II, the claimed invention of the '957 improves over conventional systems, in part, by separating a verification operation into a distinct

pre-verify stage and **verify stage** with distinct voltages applied in each. *See* '957, 1:58-2:8, 6:37-49, 17:32-56, Fig. 6. By doing so, "the gradient of the channel potential of the selected memory cell string can be reduced," and as a result "HCI cannot be generated from the selected memory cell to the upper adjacent memory cell … in the selected memory cell string." '957, 12:63-13:4. By comparison, Costa and Seo fail to disclose or render obvious any type of two-stage verification operation that includes **pre-verify** and **verify** stages. Przybylski, ¶147.

Costa does not disclose or render obvious that a verify operation includes a distinct "pre-verify stage" and "verify stage." Similarly, Seo does not disclose or render obvious any type of verify operation and is instead concerned with a memory device "read" operation that is divided into a "first time period t1" and a "second time period t2." Seo [0011]. Moreover, Petitioner's proposed combination fails to show that a POSITA would have been motivated to combine Costa and Seo's teachings to render obvious a verify operation that includes a distinct "pre-verify stage" as required by the Challenged Claims. As correctly recognized by the Board, "Seo only describes time periods t1 and t2 with respect to performing a read operation that includes the steps selecting a page and memory string, setting the select transistor line voltage of the unselected, memory string and apply period thereof, applying voltage to the select lines of the unselected memory string, and applying the read voltage." DI, 26-27 (citing Seo [0087]-[0090], Fig. 7). Even

assuming that a POSITA would have been motivated to employ Seo's teachings when performing a verification operation, it does not follow that the time period t1 in Seo would thus be converted to a "pre-verify stage" in the sense of the '957. Przybylski, ¶¶148-149.

For at least the reasons above, Costa in view of Seo fails to disclose or render obvious applying bias verify voltages during a "pre-verify stage" as required by limitations [1.a]-[1.b]. Przybylski, ¶150.

Costa in view of Seo also fails to disclose or render obvious dependent claims 2-6 for at least the same reasons. Przybylski, ¶151.

B. Independent Claim 1: Costa in View of Seo Does Not Disclose or Render Obvious Applying "a First Bias Voltage" and "a Second Bias Voltage" on the Gate Terminal of a Not Programmed Memory Cell "Wherein the Second Bias Voltage Is Smaller than the First Bias Voltage" (Limitations [1.b], [1.d])

Costa in view of Seo does not disclose or render obvious limitations [1.b] and [1.d] because the references, both alone or in combination, do not disclose or render obvious applying distinct bias voltages on a gate terminal of a not-programmed memory cell such that "the second bias voltage is smaller than the first bias voltage" as required by claim 1. Petitioner does not show that the voltages disclosed in Costa and Seo are applied on a gate terminal of a memory cell, and neither reference discloses or renders obvious using two different bias voltages during a verify operation. Moreover, Petitioner and Dr. Liu's conclusory assertion that a POSITA

would have been motivated to selectively apply Costa's purported teachings to only a verify stage (and not a pre-verify stage) is inconsistent with Costa's disclosure and contradicts the basic operating principles of NAND memory strings. *See* Pet. 103-112. Petitioner's argument is an attempt to impermissibly "reconstruct the applicant's invention only with the benefit of hindsight." *See Netflix, Inc. v. DivX, LLC*, 80 F.4th 1352, 1359 (Fed. Cir. 2023); *see also Cheese Sys., Inc. v. Tetra Pak Cheese & Powder Sys., Inc.*, 725 F.3d 1341 (Fed. Cir. 2013) (obviousness "cannot be based on the hindsight combination of components selectively culled from the prior art to fit the parameters of the patented invention"). Przybylski, ¶¶152-153.

Claim 1 of the '957 recites processing circuitry configured to: "**apply, in the pre-verify stage, a first bias voltage on a gate terminal of at least one memory cell of the first memory cell string that is not programmed**" (Element [1.b]); and "**apply, in the verify stage, a second bias voltage on the gate terminal of the at least one memory cell of the first memory cell string that is not programmed, wherein the second bias voltage is smaller than the first bias voltage**" (Element [1.d]). These limitations are common to each of the Challenged Claims by virtue of their dependency on claim 1 of the '957. Przybylski, ¶154.

As explained in Section II, the '957 distinguishes between the target voltages that may be applied through word line layers during a pre-pulse stage, and the bias voltages applied on the gate terminals of the memory cells that develop over time as

a result. *See, e.g.*, '957, 11:68-12:9, 12:10-27. Within that context, the claimed invention of the '957 improves over conventional systems, in part, by applying a **first bias voltage** that fully develops on a gate terminal of a not-programmed memory cell during a **pre-verify stage**, and then applying a **second bias voltage** that is smaller than the first bias voltage during a later **verify stage**. '957, 1:58-2:8, 6:37-49, 17:32-56, Fig. 6.

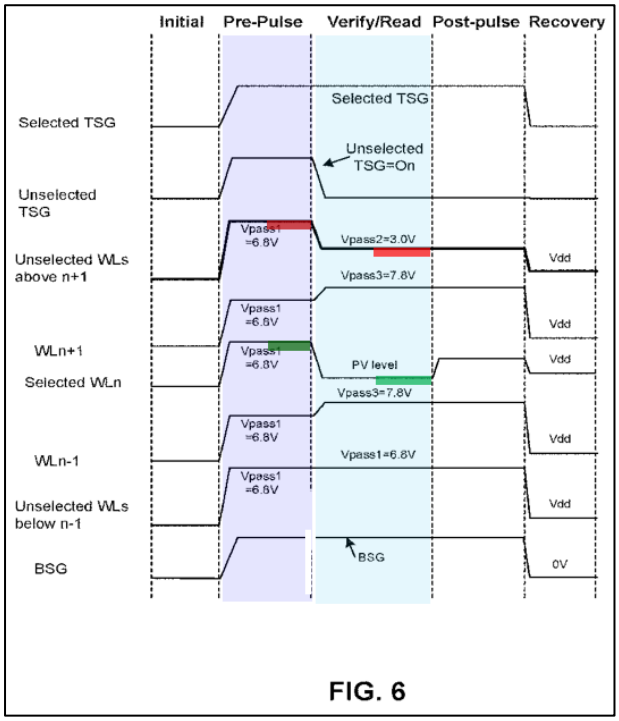


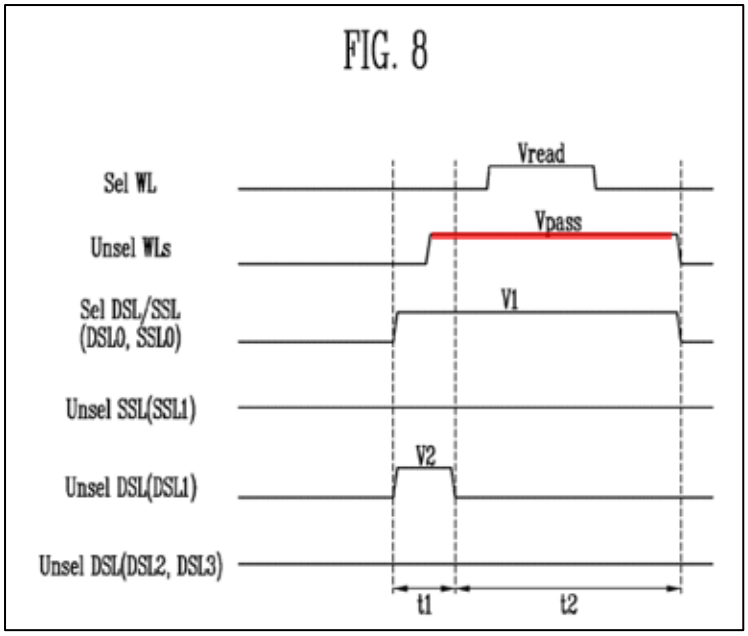
FIG. 6

But unlike the '957, neither Costa nor Seo discloses or otherwise suggests that the bias voltage applied on a gate terminal of a not-programmed memory cell changes over time—nor does the proposed combination. Przybylski, ¶155.

First, Costa does not disclose the use of separate "verify" and "pre-verify" stages for a verify operation, or that different voltage levels would be used during a

"verify" and a "pre-verify" stage as required by the '957. While Costa discloses that a lower "pass voltage" can be used for ***unprogrammed memory cells*** as compared to ***programmed memory cells***, Costa fails to disclose any difference in the "pass voltage" applied to any given memory cell ***at different stages of a verification process***. *See* Costa [0121]-[0122], [0147]. As explained by Costa, programming a memory cell increases the threshold voltage (*see* Costa [0082]), and because the unprogrammed cells are in an erased state, "lower read pass voltage VreadL can be used while still ensuring that these memory cells operate as pass gates" (Costa [0122]). But that does not teach separate "pre-verify" and "verify" stages, let alone using different voltage levels during "pre-verify" and "verify" stages. In Costa, the "pass voltage" applied to a given memory cell is always constant. Przybylski, ¶156.

Second, Seo similarly fails to disclose the use of distinct bias voltages during a "pre-verify stage" and a "verify stage," as required by the Challenged Claims. Seo discloses that a "read" operation can be divided into "time period t1" and "time period t2," and that a "pass voltage **Vpass** may be applied to unselected word lines" during both a portion of time period t1 as well as time period t2." Seo, [0087]-[0090], Fig. 8. Przybylski, ¶157.



Petitioner seemingly concedes that Seo does not disclose the use of distinct values of "**Vpass**" during these different time periods, and that Seo fails to demonstrate the use of two distinct bias voltages on not-programmed memory cells. *See* Pet. 26-27, 103. Instead, Petitioner improperly points to Seo's use of "**Vpass**" during time period t1 as equivalent to the claimed "first bias voltage," and incorrectly asserts that it would have been obvious in view of Costa for a distinct value of **Vpass** to be applied to the unselected word lines during only time period t2 (i.e., a distinct "second bias voltage"). *See* Pet. 26-27, 103-126. Przybylski, ¶158.

Petitioner and Dr. Liu have failed to demonstrate why a POSITA would have been motivated to selectively apply Costa's purported teachings (i.e., the use of a lower **Vpass** value) to only the time period t2, and not the time period t1. The Petition improperly argues that Costa's purported teachings of using a "low Vpass

voltage[s]" would apply only in the second time period, while ignoring that Costa itself provides no such teaching of selectively lowering pass voltages based on the time period. *See* Pet. 112, 126-129. Indeed, to the extent that it would be advantageous to use lower Vpass voltages as purportedly taught by Costa (i.e., using lower pass voltages on certain unprogrammed memory cells (Costa, [0112])), that purported teaching is equally applicable in both time periods, and Petitioner has not shown that selectively adjusting the voltage applied in only one of the periods would have been obvious. Przybylski, ¶159.

The Petition attempts to justify its proposed combination with the faulty and unsupported argument that Seo requires "high Vpass voltages" on all unselected memory cells during the first time period. Pet. 128 (citing Liu ¶308). As an initial matter, Seo does not actually state that a "high Vpass voltage" must be applied. Moreover, both Petitioner and Dr. Liu fail to articulate why a single value of Vpass must be used for all memory cells regardless of their programmed state (i.e., why Costa's teachings would be ignored during the initial time period, such that a high Vpass voltage would be applied to even unprogrammed memory cells), or why Costa's teachings would otherwise become inapplicable. At most, Dr. Liu argues that "a POSITA would have understood that in Seo's bias scheme" a "full Vpass voltage" would be required during the first time period because "a Vpass voltage on unselected memory cells on the drain side of the selected memory cell needs to be

high enough to account and compensate" for voltage building on the "source of [the] transistor" during a pre-conditioning period. Liu ¶308. But Dr. Liu fails to cite any portion of Seo's disclosure for that proposition, and even taking Dr. Liu's argument at face value, Costa's purported teachings (i.e., that a lower voltage value can be used to turn on unprogrammed memory because of their lower threshold voltage) ***would still apply to both time periods equally***, including the first time period—again demonstrating that Petitioner is using hindsight and has not shown that adjusting voltages in only the second time period would have been obvious. Przybylski, ¶160.

Thus, contrary to Petitioner's assertions, a POSITA would not have been motivated to selectively apply Costa's teachings as Petitioner has proposed. Rather, Petitioner's and Dr. Liu's selective application of Costa's teachings is unsupported, has no justification in the references, and is little more than an attempt at using impermissible hindsight to reconstruct the claimed invention. Przybylski, ¶161.

Additionally, unlike the '957, Costa and Seo do not distinguish between target voltages that may be applied through word line layers during a pre-pulse stage, and the bias voltages applied on the gate terminals of the memory cells that develop over time as a result. *See, e.g.*, '957, 11:68-12:9, 12:10-27. To the extent that Costa and Seo purportedly disclose certain voltages applied to word lines, they do not disclose that those voltages are also applied on the gate terminals of the corresponding

memory cells, nor does Petitioner present any arguments or evidence to suggest that the two would have obviously been the same. Przybylski, ¶162.

For at least the reasons above, Costa and Seo, alone or in combination, fail to disclose or render processing circuitry configured to "apply … a first bias voltage on a gate terminal of at least one memory cell of the first memory cell string that is not programmed," and "a second bias voltage on the gate terminal of the at least one memory cell of the first memory cell string that is not programmed, wherein the second bias voltage is smaller than the first bias voltage" as recited by limitations [1.b] and [1.d]. Rather, Petitioner's proposed combination is inconsistent with Costa's and Seo's own teachings, and is little more an attempt to impermissibly "reconstruct the applicant's invention only with the benefit of hindsight." *See Netflix*, 80 F.4th at 1359; *see also Cheese Sys.*, 725 F.3d at 1352. Przybylski, ¶163.

Costa in view of Seo also fails to disclose or render obvious dependent claims 2-6 for at least the same reasons. Przybylski, ¶164.

IX. CONCLUSION

For the reasons above, Petitioner has failed to demonstrate by a preponderance of the evidence that any of the Challenged Claims of the '957 is anticipated or obvious. Accordingly, the Board should find in favor of Patent Owner and uphold the validity of all Challenged Claims.

Dated: January 31, 2025

Respectfully submitted,

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CERTIFICATE OF WORD COUNT

The undersigned certifies that the foregoing PATENT OWNER'S RESPONSE complies with the type-volume limitation in 37 C.F.R. § 42.24(a)-(b). According to the word-processing system's word count, the brief contains 13,998 words, excluding the parts of the brief exempted by 37 C.F.R. § 42.24(c).

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CERTIFICATE OF SERVICE

The undersigned certifies that the foregoing PATENT OWNER'S PRELIMINARY RESPONSE UNDER 37 C.F.R. § 42.107 was served in its entirety by filing through the Patent Trial and Appeal Case Tracking System (P-TACTS), as well as providing a courtesy copy via e-mail to the following attorneys of record for Petitioner listed below:

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