

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,

Petitioner,

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,

Patent Owner.

Case IPR2024-00792
Patent 11,468,957

**DECLARATION OF STEVEN PRZYBYLSKI, PH.D. IN SUPPORT OF
PATENT OWNER'S RESPONSE**

Executed this 31rd day of January, 2025 in Ann Arbor, Michigan.



Steven A. Przybylski, Ph.D.

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LIST OF ABBREVIATIONS

Abbreviation	Term
'957 or '957 Patent	U.S. Pat. No. 11,468,957
'957FH	File History of U.S. Pat. No. 11,468,957
Challenged Claims	'957, Claims 1-6
Liu	Declaration of Dr. Liu (Ex. 1003)
Hongtao	Chinese Pat. App. Pub. No. 109065091 (Ex. 1005)
Yu	U.S. Pat. No. 20190198117 (Ex. 1006)
Suzuki	U.S. Pat. No. 20210082505 (Ex. 1007)
Costa	U.S. Pat. No. 20180012667 (Ex. 1008)
Seo	U.S. Pat. No. 20210027848 (Ex. 1009)
Li	U.S. 2024/0295960 (Ex. 2004)
Dong	U.S. 2023/0343398 (Ex. 2005)
Liu822 Tr.	Transcript of December 17, 2024 Deposition of Dr. Liu for IPR2024-00795 in Connection with Patent U.S. 11,501,822 (Ex. 2006)
Yang	U.S. 10,726,920 (Ex. 2007)
Office	U.S. Patent and Trademark Office
Petition or Pet.	Petition for <i>Inter Partes</i> Review of U.S. Patent No. 11,468,957 (IPR2024-00792, Paper 1)

Parallel district court litigation *Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc.*, NDCA-3-23-cv-05792 (N.D. Cal.)

Patent Owner Yangtze Memory Technologies Co. Ltd.

Petitioner Micron Technology, Inc.

POSITA Person of ordinary skill in the art

I, Steven Przybylski, Ph.D., hereby declare as follows:

I. INTRODUCTION

1. I have been retained by counsel for Yangtze Memory Technologies Company, LTD (“YMTC”) in the above captioned *inter partes* review of U.S. Patent No. 11,468,957 (Ex. 1001, ’957 Patent”). I have been asked to consider the scope and content of the prior art, and respond to certain allegations regarding the prior art, presented by Micron Technology, Inc., (“Petitioner”) in its petition for *inter partes* review of the ’957 Patent (“Petition”) and the April 29, 2024 Declaration of Dr. David Kuan-Yu Liu (Ex. 1003, “Liu”). The arguments raised in Dr. Liu’s declaration are similar to those raised in the Petition. Unless otherwise noted, my opinions with respect to the Petition also apply to the corresponding section of Dr. Liu’s declaration, and vice-versa. As explained in Sections X-XII (discussing the Grounds raised in the Petition) the invalidity arguments raised in the Petition fail to anticipate or render obvious any of the Challenged Claims, and the arguments raised in Dr. Liu’s declaration fail for similar reasons.

2. I am being compensated for my time at my usual consulting rate of \$575 per hour, plus reimbursement for any actual expenses. No part of my compensation depends on the content of the opinions that I herein render or on the outcome of this review proceeding. I have no expectation or promise of additional business with

Patent Owner in exchange for the positions explained herein. I do not have any direct financial interest in any of the parties.

3. Unless otherwise noted, the statements made herein are based on my personal knowledge, and if called to testify about this declaration, I could and would do so competently and truthfully.

II. QUALIFICATIONS

4. My qualifications including cases in which I was an expert are stated more fully in my curriculum vitae which has been provided as **Appendix A**. Here, I provide a brief summary of my qualifications.

5. I earned a Bachelor of Applied Science from the University of Toronto in 1980. I was enrolled in the Engineering Science program, completing a course of study combining the Electrical Engineer and Computer Science options.

6. I earned a Master of Science in Electrical Engineering degree and a Ph.D. in Electrical Engineering in 1982 and 1988 respectively, both from Stanford University.

7. I also earned a Masters of Business Administration from the Haas School of Business at the University of California at Berkeley in 2000.

8. I have extensive experience with memory semiconductor integrated circuits and the memory systems constructed of them. At Stanford, my dissertation was on the optimization of single- and multi-level cache hierarchies to maximize

system-level performance. Also at Stanford, I was a member of the core team that architected, designed, built, and tested the seminal MIPS processor. I was responsible for the design of the instruction decode and control units as well as architecting the virtual memory support. I assembled and debugged the entire microprocessor design and oversaw its fabrication and testing. In 1984 and 1985, I took a leave of absence from Stanford to become a member of the founding team of MIPS Computer Systems, a startup in California that designed, built, and sold processors and computer systems. In 1989, after finishing my doctorate and brief post-doctorate at Stanford, I returned to MIPS Computer Systems. Throughout my two periods of employment at MIPS Computer Systems, I had a number of titles and worked on a variety of projects. Noteworthy were stints as processor architect, systems architect, hardware-software team liaison, and Chief Scientist of the High-End Systems group. During the second period, I also served as a Consulting Assistant Professor in the Department of Electrical Engineering at Stanford. I designed and taught an advanced graduate level course on cache and memory system design.

9. In 1991, I left MIPS to become an independent consultant. In that capacity I have provided technical, strategic, marketing, and intellectual property services to a large number of clients both domestically and internationally.

10. The technical consulting I performed was principally related to advancements in semiconductor memories and their application in systems. Specifically with respect to non-volatile memories and Flash memories in particular, I advised companies on a variety of memory types and on trends in NAND and NOR Flash memories and the processes used in their manufacture. In the 2000's, I helped develop a new NAND Flash architecture and separately a universal memory interface that was optimized for use in heterogeneous memory systems and that was equally applicable to DRAMs and to NAND Flash devices.

11. I am a member of both the Institute of Electrical and Electronics Engineers (IEEE) and the Association of Computing Machinery (ACM). In addition, in 1997 I became a registered patent agent. I am listed as the inventor on 11 domestic patents and their foreign counterparts. The subject matters include memory devices, memory subsystems, networks, error detection and correction codes, processors and cache memories. Between 1994 and approximately 2000, I was a leading independent analyst following, writing, and teaching about both the technical and business aspects of the DRAM industry. Overall, I have written three books and over 25 articles in the areas of memory, processors, and computer systems. In particular, I wrote and revised an 850-page book entitled "New DRAM Technologies: A Comprehensive Analysis of the New Architectures." I have presented many lectures, classes and seminars on semiconductor memories and their memory systems,

processors and computer systems. I have presented full and half-day seminars on discrete and embedded DRAMs to over 2,500 engineers, marketers, managers, and financial analysts.

III. MY ASSIGNMENT AND BASES OF OPINIONS

12. I have been asked to provide my opinions as to the scope and content of the prior art presented by Petitioner and Dr. Liu in the Petition. Specifically, I have been asked to provide my opinions concerning the scope and content of the Hongtao (Ex. 1005), Yu (Ex. 1006), Suzuki, (Ex. 1007), Costa (Ex. 1008), and Seo (Ex. 1009) references as would have been understood by a person of ordinary skill in the art, and to respond to certain assertions by Petitioner and Dr. Liu regarding the four Grounds presented in the Petition.

13. In the course of conducting my analysis and forming my opinions, I have reviewed the references and materials cited in the Petition and herein including those listed below:

Exhibit Number	Description
N/A	Petition for <i>Inter Partes</i> Review of U.S. Patent No. 11,468,957 (IPR2024-00792, Paper 1)
Ex. 1001	U.S. Patent No. 11,468,957 B2 to Lee et al.
Ex. 1002	File History of U.S. Patent No. 11,468,957 to Lee et al.
Ex. 1003	Declaration of David Kuan-Yu Liu, Ph.D. (“Liu”)
Ex. 1004	<i>Curriculum Vitae</i> of David Kuan-Yu Liu, Ph.D.
Ex. 1005	Chinese Patent No. 109065091 A to Hongtao Liu et al. (certified translation and original) (“Hongtao”)
Ex. 1006	U.S. Patent Publ. No. 2019/0198117 A1 to Yu et al. (“Yu”)
Ex. 1007	U.S. Patent Publ. No. 2021/0082505 A1 to Suzuki (“Suzuki”)

Ex. 1008	U.S. Patent Publ. No. 2018/0012667 A1 to Costa (“Costa”)
Ex. 1009	U.S. Patent Publ. No. 2021/0027848 A1 to Seo (“Seo”)
Ex. 1013	U.S. Patent No. 9,589,978 B1 to Yip
Ex. 1014	Aritome, “NAND Flash Memory Technologies” (2016)
Ex. 1015	Silvagni, “3D NAND Flash Based on Planar Cells,” Computers 2017
Ex. 1016	U.S. Patent Publ. No. 2020/0168276 A1 to Yang
Ex. 1017	U.S. Patent No. 9,620,233 B1 to Dong et al.
Ex. 1018	Micheloni, “3D Flash Memories” (2016)
Ex. 1019	U.S. Patent No. 9,361,993 B1 to Chen et al.
Ex. 1020	U.S. Patent No. 10,276,251 B1 to Lobana et al.
Ex. 1021	U.S. Patent Publ. No. 2019/0348122 A1 to Ko et al.
Ex. 1022	U.S. Patent Publ. No. 2013/0077404 A1 to Nawata et al.
Ex. 1023	U.S. Patent No. 10,121,529 B2 to Lee
Ex. 1024	U.S. Patent Publ. No. 2016/0293271 A1 to Won et al.
Ex. 1025	U.S. Patent No. 11,600,342 to Chen et al.
Ex. 2004	U.S. 2024/0295960 (“Li”)
Ex. 2005	U.S. 2023/0343398 (“Dong”)
Ex. 2006	Transcript of December 17, 2024 Deposition of Dr. Liu for IPR2024-00795 in Connection with Patent U.S. 11,501,822 (“Liu822 Tr.”)
Ex. 2007	U.S. 10,726,920 (“Yang”)

14. My opinions in this declaration are based on my review of these documents, as well as upon my education, training, research, knowledge, and experience.

15. All emphases (such as bolding, underlying, or italics) appearing in quotations and citations cited herein have been added by me, unless otherwise stated.

IV. SUMMARY OF MY OPINIONS

16. It is my opinion that:

- Hongtao in view of Yu does not disclose or render obvious a “pre-verify stage” as required by independent claim 1 of the ’957 Patent.
- Hongtao in view of Yu does not disclose or render obvious applying a “first bias voltage” and a “second bias voltage” to the “ gate terminal of the at least one memory cell of the first memory cell string that is not programmed” wherein the “second bias voltage is smaller than the first bias voltage” as required by independent claim 1 of the ’957 Patent.
- Hongtao in view of Yu does not disclose or render obvious a “bottom bias voltage” or a “top bias voltage” that is applied “in the pre-verify stage and the verify stage” as required by dependent claim 5 and dependent claim 6 of the ’957 Patent.
- Suzuki does not disclose or render obvious applying a “first verify voltage” and a “first bias voltage” in a “pre-verify stage” and applying a “second bias voltage” in a “verify stage” “wherein the second bias voltage is smaller than the first bias voltage” as required by independent claim 1 of the ’957 Patent.
- Suzuki does not disclose or render obvious a “bottom bias voltage” or a “top bias voltage” that is applied “in the pre-verify stage and the verify stage” as required by dependent claim 5 and dependent claim 6 of the ’957 Patent.
- Costa in view of Seo does not disclose or render obvious a “pre-verify stage” as required by independent claim 1 of the ’957 Patent.

- Costa in view of Seo does not disclose or render obvious applying a “first bias voltage” in a “pre-verify stage” and applying a “second bias voltage” in a “verify stage” “wherein the second bias voltage is smaller than the first bias voltage” as required by independent claim 1 of the ’957 Patent.

V. APPLICABLE LEGAL STANDARDS

17. I am not a legal expert and offer no opinions on the law. However, I have been informed by counsel of the various legal standards that apply, and I have applied those standards in arriving at my conclusions.

A. Claim Construction

18. I was informed, unless otherwise noted, I should give claim terms their ordinary and customary meaning as understood by a person of skill in the art at the time of the invention. I was informed and I understand that the words of the patent’s claims and the context in which the term is used in the claims can be highly instructive in ascertaining the term’s meaning. I further understand that the terms of a claim are to be interpreted in the context of the entire patent, including the patent’s other claims, its specification and its figures.

19. I have been further instructed that a patent’s “prosecution history” may often provide helpful evidence about how the Patent Office and the applicant understood the patent and its claims. Therefore, I have been instructed that claim terms should also be interpreted in light of the patent’s prosecution history. In

addition to the claims, the specification, the figures, and the prosecution history, I have been instructed that certain “extrinsic evidence” such as scientific or technical references may also help inform the way in which the person of ordinary skill in the art might understand the claim term. I have been instructed that extrinsic evidence must always be considered in the context of the intrinsic evidence.

B. Anticipation

20. I have been informed by counsel that a patent claim is invalid as anticipated if each element of that claim is present either explicitly or inherently in a single prior art reference. I have also been informed that, to be an inherent disclosure, the prior art reference must necessarily disclose the limitation, and the fact that the reference might possibly practice or possibly contain a claimed limitation is insufficient to establish that the reference inherently teaches the limitation.

C. Obviousness

21. I understand that a claim is unpatentable if it would have been obvious to a person of ordinary skill in the art at the time the invention was made. I understand that a claim could have been obvious from a single prior art reference or from a combination of two or more prior art references. I understand that an obviousness analysis requires an understanding of the scope and content of the prior

art, any differences between the invention and the prior art, and the level of ordinary skill in evaluating the pertinent art.

22. I further understand that a claim would have been obvious if it unites old elements with no change to their respective functions or alters prior art by mere substitution of one element for another known in the field, and that combination yields predictable results. Also, I understand that obviousness does not require physical combination or bodily incorporation, but rather consideration of what the combined teachings would have suggested to persons of ordinary skill in the art at the time of the invention.

23. While it may be helpful to identify a reason for this combination, I understand that there is no rigid requirement of finding an express teaching, suggestion, or motivation to combine within the references. When a product is available, design incentives and other market forces can prompt variations of it, either in the same field or a different one. If a person of ordinary skill in the art can implement a predictable variation, obviousness likely bars its patentability. For the same reason, if a technique has been used to improve one device and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique would have been obvious. I understand that a claim would have been obvious if a person of ordinary skill in the art would have had

reason to combine multiple prior art references or add missing features to reproduce the invention recited in the claims.

24. I further understand that certain factors may support or rebut the obviousness of a claim. I understand that such secondary considerations include, among other things, commercial success of the patented invention, skepticism of those having ordinary skill in the art at the time of invention, unexpected results of the invention, any long-felt but unsolved need in the art that was satisfied by the invention, the failure of others to make the invention, praise of the invention by those having ordinary skill in the art, and copying of the invention by others in the field. I understand that there must be a nexus, that is, a connection, between any such secondary considerations and the invention.

25. I understand that in considering obviousness, it is important not to determine obviousness using the benefit of hindsight derived from the patent being considered.

D. Claim Dependency

26. I understand that a patent may include two types of claims, independent claims and dependent claims. An independent claim stands alone and includes only the limitations it recites. A dependent claim can depend from an independent claim or another dependent claim. I understand that a dependent claim includes all the

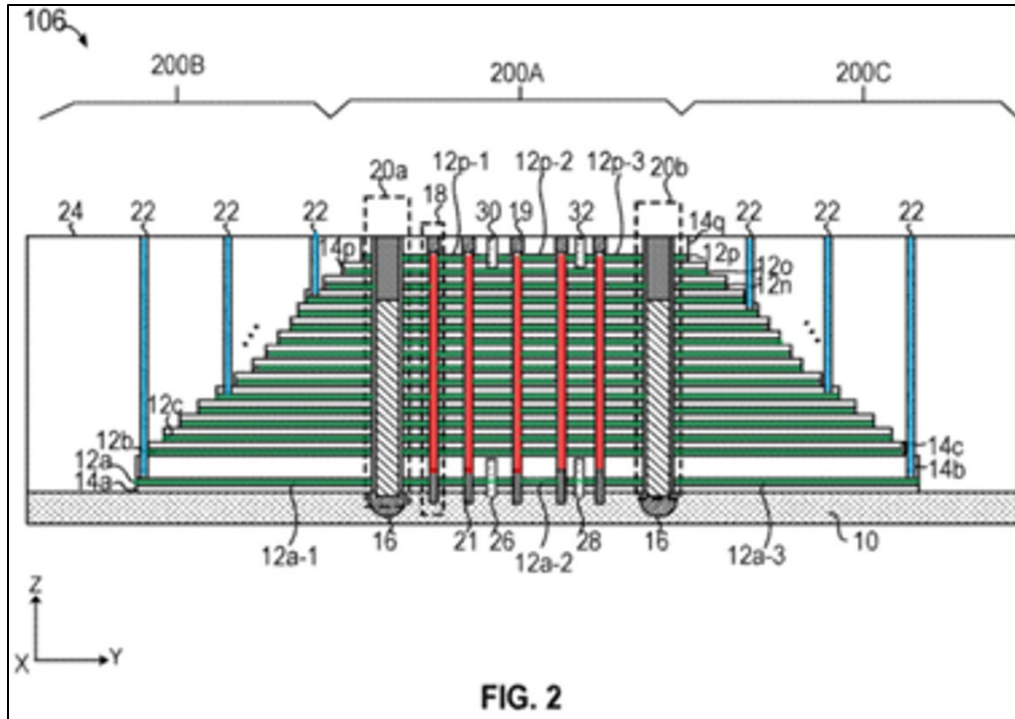
limitations that it recites in addition to all of the limitations recited in the claim from which it depends.

VI. THE '957 PATENT

A. Overview of the '957 Patent

27. The '957 Patent describes an improved approach for carrying out verification operations in flash memory devices, such as 3D NAND devices, that helps to reduce undesirable hot-carrier injection (“HCI”) effects and induced edge summation (“ESUM”) losses. *See* '957 Patent, 1:44-49, 17:7-30. As a result, the systems and methods disclosed in the '957 Patent enhance device reliability, and can decrease overall power usage. *Id.*

28. As described by the '957 Patent, three-dimensional (3D) NAND flash memory was created to “increase bit density and reduce the bit cost of flash memory devices.” '957 Patent, 1:12-25. For example, as illustrated in Figure 2 (annotated below) a 3D-NAND memory may be composed of an array of “alternating **word line layers** ... and insulating layers” with vertically positioned “channel structures” throughout the device that are each used to “**form a respective vertical NAND memory cell string**.” '957 Patent, 7:60-8:9, 8:27-43.



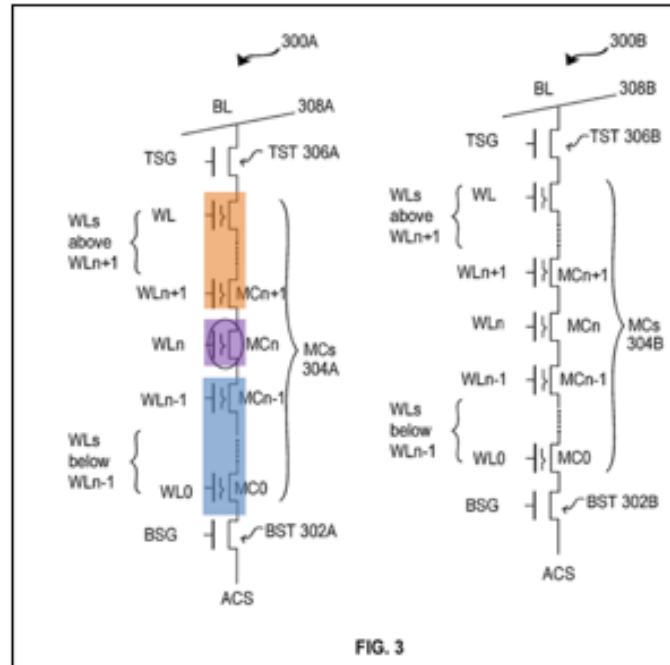
'957 Patent, Fig. 2. In these 3D NAND flash devices, memory cells comprise special transistors formed at the locations where each of the horizontal word line layers intersect with the vertically oriented memory strings, “**word line contacts**” are used so that “gate voltages can be applied on gates of the memory cell transistors through the word line contacts ... that are coupled to the word line layers.” ’957 Patent, 8:50-51. Because of the layered structure of the device, each of the word line layers generally has a large capacitance that results in an RC time-constant for each word line. *See, e.g.,* Ex. 1014 (“Aritome”), 350-353 (describing the “RC (resistance-capacitance) delay” experienced by word lines, and explaining that in a “stacked word-line (WL) structure in 3D NAND cells ... a WL capacitance is greatly increased from 2D cells”). Additionally, as taught by the ’957 Patent, the target

voltages administered to word lines via the word line contacts will differ from the resulting voltages that develop over time on the gate terminals of the memory cells. *See* '957 Patent, 11:58-12:1, 12:10-27, Figs. 4-5.

29. As depicted in Figure 2 (shown above), a “3D-NAND memory device can include a plurality of memory cell strings” that each include “a bottom-select-gate (BSG) transistor, memory cells, and a top-select-gate (TSG) transistor that are connected in series.” '957 Patent, 1:24-40; *see also id.* 8:27-43, 9:3-30, 14:31-34. The gate of every transistor within a given memory string is connected to a distinct word line layer. In turn, these word line layers are used to administer voltages to the transistor gates of the various transistors that form the memory string. For example, the '957 Patent explains that different types of word line layers may include “bottom select gate (BSG) layers” that are used to apply gate voltages to BSG transistors, “gate layers (or word line layers)” that are used to apply voltages to different memory cells, and “top select gate (TSG) layers” that are used to apply voltages to TSG transistors. '957 Patent, 7:60-8:8.

30. For example, as illustrated in Figure 3 (annotated below), “the string 300A can include a bottom select transistor (BST) or bottom-select-gate (BSG) transistor 302A, a plurality of memory cells (MCs) 304A, and a top select transistor (TST) or top-select-gate (TSG) transistor 306A that are disposed sequentially and in series over the substrate along the height direction (e.g., Z direction) of the substrate

10.” ’957 Patent, 9:3-30. In general, one memory cell will be the **selected memory cell** that is being programmed. Because memory cells within the string are typically programmed in order, the **selected memory cell** being programmed is always positioned between the previously **programmed memory cells** to one side of the memory string (i.e., the memory cells in the programming order that have already been programmed), and **not-programmed memory cells** (i.e., memory cells within the programming order that have not yet been programmed) on the other side of the memory string. Each of the memory cells within the memory string can be “programmed in the forward order” going “from a bottom MC adjacent to the BSG transistor to a top MC adjacent to the TSG transistor” (*id.* at 9:57-10:7) or “programmed in a reverse order” going “from a top memory cell adjacent to the TSG transistor to a bottom memory cell (e.g., MC0) adjacent to the BSG transistor” (*id.* at 14:31-42).



Id., Fig. 3 (annotations depicting “**programmed**” and “**not-programmed**” memory cells relative to the “**selected memory cell**” when the memory string is programmed in forward order; the position of the “**programmed**” and “**not-programmed**” memory cells would be reversed if a reverse programming order were used instead).

31. After each memory cell programming operation, the value is “verified” in order to make sure that the memory cell was programmed correctly. As described in the ’957 Patent, traditional techniques for performing verify operations suffered from undesirable “hot carrier injection” (HCI) effects between the selected memory cell that is having its programmed state being verified and neighboring memory cells, which in turn could result in “induced edge summation (ESUM) loss.” ’957 Patent, 1:44-49, 6:66-7:12. Hot carrier injection may occur when, due to a difference in potential between the source and drain of the selected memory cell (i.e., a potential

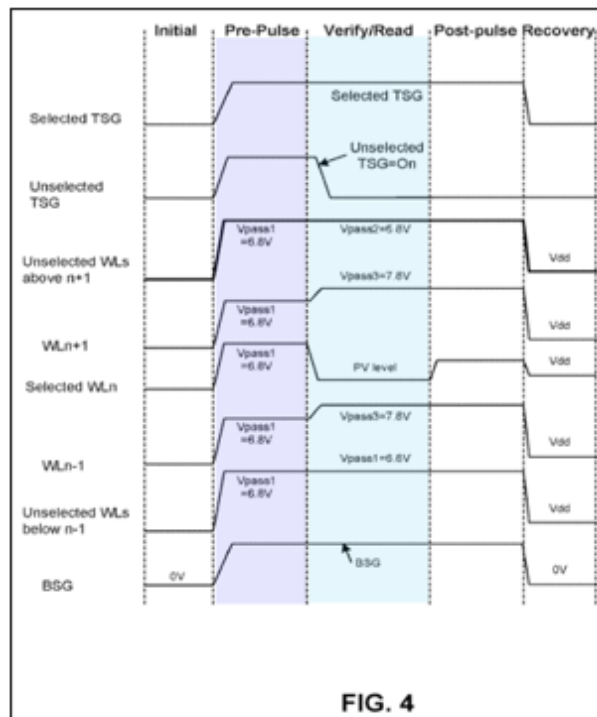
difference along the channel of the memory cell), hot electrons at the selected memory cell are unintentionally injected into the storage layer of adjacent memory cells, thus altering their threshold voltages. *See* Ex. 1014 (“Aritome”), 235-238, 244-248. These HCI effects may cause the threshold voltages of the adjacent memory cells to shift over time as verification operations are performed. Because the programmed state of a given memory cell relates to its threshold voltage, these HCI effects may also indirectly result in “edge summation (ESUM)” losses, which relates to the number of distinct programmed states within each memory cell that the device can reliably differentiate between. *See* Ex. 2004 (U.S. 2024/0295960, “Li”), [0056] (“ESUM” is the summation of the “voltage interval[s] between threshold voltage distributions corresponding to two adjacent data states that can be used to read data on a memory cell”); Ex. 2005 (U.S. 2023/0343398 “Dong”), [0085] (describing ESUM as the sum of the “total readable distributions” of threshold voltages within a given memory cells).

32. The claimed invention of the ’957 Patent helps to mitigate these issues by partitioning the verification operation into multiple different stages, including a “pre-verify stage” and a “verify stage,” and then applying different sets of voltages to the gate terminals of the selected memory cell and other not-programmed memory cells in each of the different stages. *See* ’957 Patent, 7:13-32.

33. As recited by the Challenged Claims, the claimed invention of the '957 Patent is expressly directed to verify voltages applied “*on a gate terminal of a selected memory cell* of the first memory cell string” and bias voltages applied “*on a gate terminal of at least one memory cell* of the first memory cell string that is not programmed,” as opposed to the target voltages that are administered to the corresponding word lines. *See* '957 Patent, Claim 1, 1:50-2:8, 6:37-49, 15:31-16, Fig. 10. As described by the '957 Patent, verify voltages and bias voltages “can be applied on the gate terminal (or gate) of the selected memory cell MC_n through a WL layer (e.g., WL_n) that is coupled to the selected memory cell MC_n.” '957 Patent, 9:31-56. However, these voltages applied to the memory cell gate terminals need time to fully “develop” to the desired target values, and may differ from the target voltages applied to word line layers. *See, e.g.,* '957 Patent, 6:37-7:12. For example, as illustrated in Figures 5 and 4, these differences between target voltages and actual gate terminal voltages depend on the length of the “pre-verify stage,” and become increasingly important when trying to reduce the time needed to perform verification operations. *See* '957 Patent, 11:58-12:27.

34. Figure 4 illustrates how bias voltages may be applied in a system that uses “a long pre-pulse time,” while Figure 5 illustrates the difficulties that may arise from trying to use a “short pre-pulse time” instead. *Compare* '957 Patent, 11:58-12:9 *with* 12:10-27. In Figure 4 (annotated below), “appropriate bias voltages can be

applied on the selected TSG layer, the unselected TSG layer, the WLs ($>n+1$), the $WLn+1$, the WLn , the WLs ($<n-1$), and the BSG layer in the **pre-pulse stage**.” ’957 Patent, 10:57-11:15. For example, an initial bias voltage of 6.8 volts may be administered on each of the individual word lines. *See id.* During the “**verify/read stage**” that follows, “[t]he bias voltage applied on the WLs ($>n+1$) can be maintained,” and the “bias voltage (or verify voltage) applied on the selected word line layer WLn can be reduced.” ’957 Patent, 11:16-57.

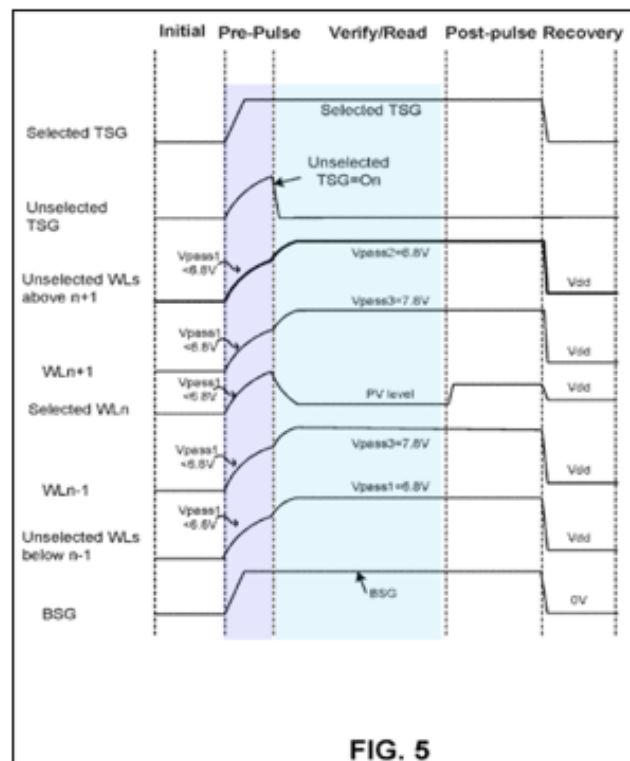


As discussed by the ’957 Patent, “the long pre-pulse time” of Fig. 4 may be “sufficient for the bias voltages to be developed fully before the TSG transistor is switched off,” meaning the applied bias voltages on each of the transistor gates will

reach the desired voltage levels being applied through the corresponding word lines.

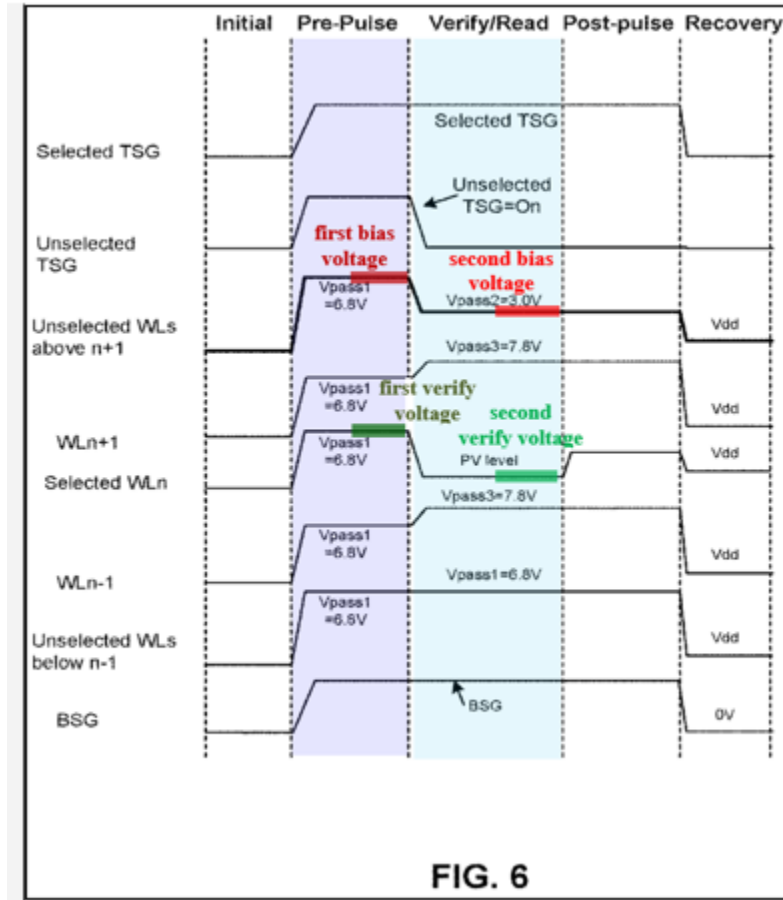
'957 Patent, Fig. 4, 11:68-12:1; *see also id.* 13:13-15.

35. Figure 5 differs from Figure 4 because it depicts “a short pre-pulse time” that is “insufficient for the bias voltages applied on the WLs ($>n+1$), $WLn+1$, WLn , $WLn-1$, and WLs ($<n-1$) to be developed fully in the pre-pulse stage.” '957 Fig. 5, 12:10-27. As shown by the curved portions of the waveforms illustrated Figure 5, “the bias voltages are less than a target value, such as 6.8 volts,” because there is not enough time for the bias voltages to charge up to the full target value in the pre-pulse stage. *Id.* Rather than reaching the desired target value in the pre-pulse stage, the bias voltages will continue to charge up and will only be “developed to the target value, such as 6.8 volts, in the verify/read stage.” *Id.*



36. Therefore, depending on the duration of the pre-pulse stage relative to the RC time constants present on the word lines, different techniques need to be utilized to ensure that the bias voltages being applied on the gate terminals of the memory cells are actually able to fully develop and reach the necessary target values for proper and reliable operation. *Compare* '957 Patent, 11:58-12:9, 12:28-39, 14:31-41, Figs. 4, 6, 8 (describing embodiments with a lengthy pre-pulse duration) *with* 12:10-38, 13:5-25, 14:63-15:17, Figs. 5, 7, 9 (describing embodiments with a brief pre-pulse duration).

37. The example illustrated in Figure 6 (annotated below) is described by the '957 Patent as using a “long pre-pulse period” similar to Figure 4, meaning that the various bias and verify voltages being applied on the gate terminals of the memory cells will be able to fully develop and reach the voltage levels being applied to the word line layers. '957 Patent, Fig. 4, Fig. 6 12:28-42; *see also id.* 11:48-12:9. However, unlike the example illustrated in Figure 4, the bias voltages in Figure 6 being applied to the word lines above $WLn+1$ are larger in the **pre-verify stage** than they are in the **verify stage**. '957 Patent, Fig. 4, 12:39-42.



Therefore, as shown in Figure 6, a **first verify voltage** is applied to selected word line (selected WLn), which fully develops on the gate terminal of the selected memory cell in the **pre-verify stage**. '957 Patent, Fig. 6, 1:58-2:8. Simultaneously, a **first bias voltage** is applied to unselected word lines above n+1, which fully develops on the gate terminals of the unselected memory cells that are not yet programmed in the **pre-verify stage**. '957 Patent, 6:37-49. Afterwards, during the subsequent **verify stage**, the first verify voltage is replaced by a **second verify voltage**, and the first bias voltage is replaced by a smaller **second bias voltage**. '957 Patent, 17:32-56.

38. As explained by the '957 Patent, by administering “a lower bias voltage” in the verify stage as compared to bias voltage applied the pre-verify stage “the gradient of the channel potential of the selected memory cell string can be reduced,” and as a consequence “HCI cannot be generated from the selected memory cell to the upper adjacent memory cell of the selected in the selected memory cell string.” '957 Patent, 12:63-13:4. Accordingly, as explained by the '957 Patent, the claimed approach may be able to lower the power consumption of the device, and by helping to attenuate HCI effects, the '957 Patent also helps to prevent ESUM loss and improve the overall performance of the device relative to conventional systems. *See* '957 Patent, 6:50-65, 17:7-17.

B. Listing of the Challenged Claims

39. For reference, claims 1-6 of the '957 Patent are reproduced below:

[1.pre] An apparatus for reading a memory device including a first memory cell string and a second memory cell string, the first memory cell string including a bottom-select-gate (BSG) transistor, memory cells, and a top-select-gate (TSG) transistor that are connected in series, the second memory cells string including a BSG transistor, memory cells, and a TSG transistor that are connected in series, the apparatus comprising: processing circuitry configured to:

[1.a] apply, in a pre-verify stage, a first verify voltage on a gate terminal of a selected memory cell of the first memory cell string, the selected memory cell being programmed and arranged between a first adjacent memory cell and a second adjacent memory cell;

[1.b] apply, in the pre-verify stage, a first bias voltage on a gate terminal of at least one memory cell of the first memory cell string that is not programmed;

[1.c] apply, in a verify stage, a second verify voltage on the gate terminal of the selected memory cell of the first memory cell string; and

[1.d] apply, in the verify stage, a second bias voltage on the gate terminal of the at least one memory cell of the first memory cell string that is not programmed, wherein the second bias voltage is smaller than the first bias voltage.

2. The apparatus of claim 1, wherein the at least one memory cell of the first memory cell string that receives the first bias voltage and the second bias voltage is positioned between the first adjacent memory cell of the selected memory cell and the TSG transistor of the first memory cell string.

3. The apparatus of claim 1, wherein the at least one memory cell of the first memory cell string that receives the first bias voltage and the second bias voltage is positioned between the second adjacent memory cell of the selected memory cell and the BSG transistor of the first memory cell string.

[4.pre] The apparatus of claim 1, wherein the processing circuitry is further configured to:

[4.a] in the pre-verify stage,

[4.a.i] apply a first gate voltage on a gate terminal of the TSG transistor of the second memory cell string,

[4.a.ii] apply a first pass voltage on a gate terminal of the first adjacent memory cell of the selected memory cell in the first memory cell string, and

[4.a.iii] apply a first read voltage on a gate terminal of the second adjacent memory cell of the selected memory cell in the first memory cell string; and

[4.b] in the verify stage,

[4.b.i] apply a second gate voltage on the gate terminal of the TSG transistor of the second memory cell string,

[4.b.ii] apply a second pass voltage on the gate terminal of the first adjacent memory cell of the selected memory cell in the first memory cell string, and

[4.b.iii] apply a second read voltage on the gate terminal of the second adjacent memory cell of the selected memory cell of the first memory cell string, wherein

[4.c] at least one of the second pass voltage and the second read voltage is larger than the second gate voltage.

[5.pre] The apparatus of claim 2, wherein the processing circuitry is further configured to:

[5.a] apply a bottom bias voltage on a gate terminal of the BSG transistor of the first memory cell string in the pre-verify stage and the verify stage;

[5.b] apply a top bias voltage on a gate terminal of the TSG transistor of the first memory cell string in the pre-verify stage and the verify stage; and

[5.c] apply a positive voltage on gate terminals of any memory cells that are positioned between the second adjacent memory cell of the selected memory cell and the BSG transistor of the first memory cell string in the pre-verify stage and the verify stage.

[6.pre] The apparatus of claim 3, wherein the processing circuitry is further configured to:

[6.a] apply a bottom bias voltage on a gate terminal of the BSG transistor of the first memory cell string in the pre-verify stage and the verify stage;

[6.b] apply a top bias voltage on a gate terminal of the TSG transistor of the first memory cell string in the pre-verify stage and the verify stage; and

[6.c] apply a positive voltage on gate terminals of any memory cells that are positioned between the first adjacent memory cell of the selected memory cell and the TSG transistor of the first memory cell string in the pre-verify stage and the verify stage.

VII. LEVEL OF ORDINARY SKILL IN THE ART

40. My opinions in this declaration are based on the understandings of a person of ordinary skill in the art, which I understand is sometimes referred to as an “ordinary artisan” or by the acronyms “POSITA” (person of ordinary skill in the art) or “POSA,” as of the time of the invention.

41. I have been asked to consider the level of ordinary skill that someone in the field of technology of the '957 Patent would have had at the time the claimed invention disclosed in the '957 Patent was made. In determining the level of ordinary skill in the art, I considered the following: (1) the levels of education and experience of persons working in the field; (2) the types of problems encountered in the field; and (3) the sophistication of the technology.

42. In my opinion, a person of ordinary skill in the art capable of reading and understanding the claims of the '957 Patent at the time of the invention would have had at least a bachelor's degree in electrical engineering, computer engineering, or a similar discipline, along with at least 2 years of professional experience with

semiconductor memory devices, or an equivalent level of knowledge and experience. For example, an advanced degree may replace some of the professional experience, or extensive experience may replace some of the educational requirements.

43. In this case, Dr. Liu has asserted in his declaration that a person of ordinary skill in the art at the time of the invention described in the '957 Patent would have had:

[A] master's degree in electrical engineering or a similar discipline, along with 4-5 years of professional experience working with (e.g., researching, designing, or teaching) NAND memory devices (including issues relating to the operation, e.g., programming, of said devices), or an equivalent level of skill, knowledge, and experience (e.g., an advanced degree may replace some of the professional experience).

Liu ¶37.

44. In view of my educational background and years of experience, including my many years of experience studying NAND Flash architecture, I both met and exceeded the qualifications of a person of ordinary skill in the art as of the earliest possible priority date of the '957 Patent of December 15, 2020. That is true under both my own definition of a POSITA, as well as under Dr. Liu's definition, and my opinions as set forth herein are the same regardless of which definition of a person of ordinary skill in the art is applied.

VIII. CLAIM INTERPRETATION FOR THE '957 PATENT

45. As discussed below, I understand that Patent Owner has addressed the construction of the terms: (1) “apply, in a [pre-verify]/[verify] stage, a [first/second] [verify/bias] voltage,” and (2) “apply a [top/bottom] bias voltage on a gate terminal of the [TSG/BSG] transistor of the first memory cell string in the pre-verify stage and the verify stage.” I also understand that Petitioner proposed a construction for the term “apply, in a [pre-verify]/[verify] stage, a [first/second] [verify/bias] voltage” in the Petition. I have applied Patent Owner’s constructions in rendering my opinions, but my opinions would not change if the claims were instead interpreted in accordance with their ordinary and customary meaning as understood by a person of skill in the art at the time of the invention.

A. “Apply, in a [Pre-Verify]/[Verify] Stage, a [First/Second] [Verify/Bias] Voltage” (All Claims)

46. Claim 1 of the '957 Patent recites processing circuitry configured to apply a “first verify voltage” and a “first bias voltage” in a “pre-verify stage,” and to apply a “second verify voltage” and a “second bias voltage” in a “verify stage.” I understand that the Petition contends that these claim 1 limitations “do not require applying these voltages throughout the given stage.” *See* Pet. 18-19. I have been informed that for the purposes of the present proceeding, Patent Owner submits that this issue does not need to be resolved by the Board in order resolve the invalidity arguments raised in the Petition. Accordingly, I have not been asked to form any

opinions regarding that construction. I agree with the Patent Owner that the Grounds raised in the Petition fail to disclose or render obvious any of the Challenged Claims regardless of whether the claimed voltages applied in “pre-verify stage” and “verify stage” must be applied throughout the entirety of a given stage.

47. As I discuss in greater detail in Sections X (discussing Ground 1) and XII (discussing Ground 3) below, the arguments raised in the Petition for Hongtao in view of Yu (Ground 1) and Costa in view of Seo (Ground 3) fail at least because the references do not disclose or render obvious applying a “first bias voltage” on a gate terminal of a not programmed memory cell that is different from a “second bias voltage.” As I discuss in greater detail in Section XII (discussing Ground 2) below, the arguments raised in the Petition for Suzuki (Ground 2) fail at least because the supposed “first bias voltage” identified in the Petition is not applied during a “pre-verify stage” as required by the Challenged Claims, nor does it prepare the device for a subsequent verify stage.

B. “Apply a [Top/Bottom] Bias Voltage on a Gate Terminal of the [TSG/BSG] Transistor of the First Memory Cell String in the Pre-Verify Stage and the Verify Stage” (Claim 5 and Claim 6)

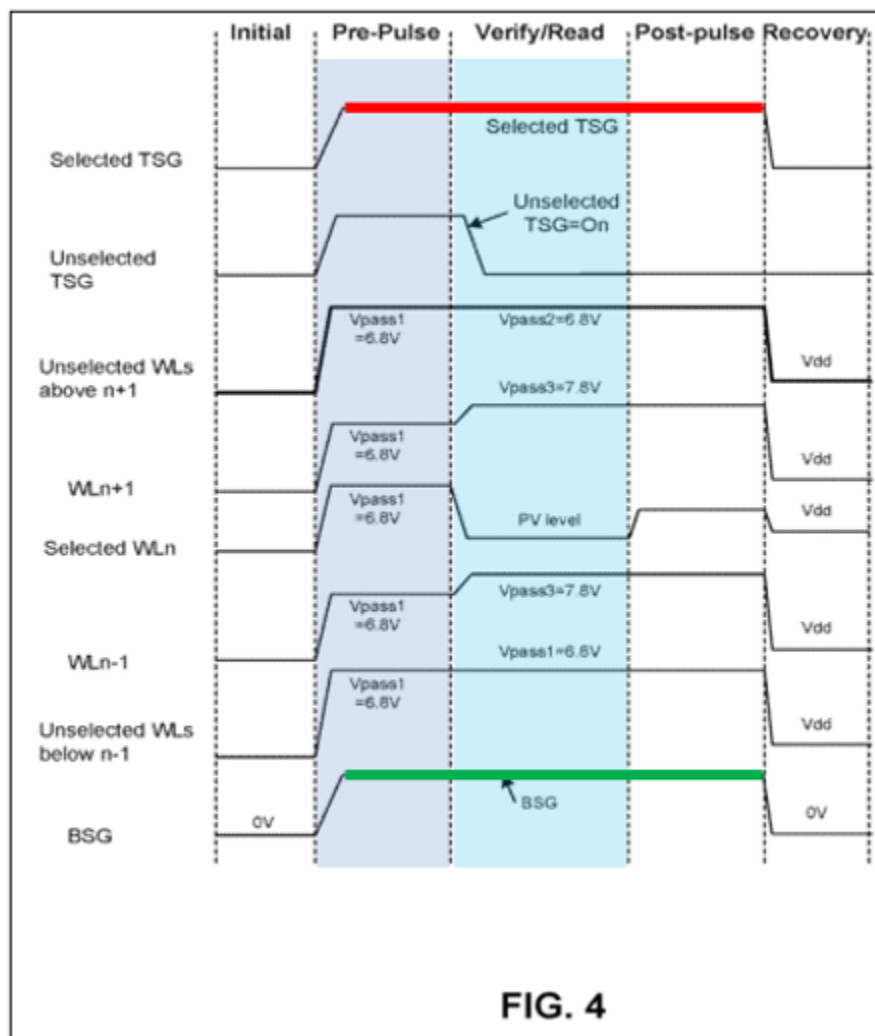
48. Petitioner’s Grounds based on Hongtao, Yu, Suzuki, Costa, and Seo fail to disclose or render obvious the limitations of independent claim 1, and thus fail to disclose or render obvious any of the Challenged Claims. I have been informed that, to the extent it is necessary for the Board to determine if the added limitations of

dependent claims 5 and 6 are disclosed or rendered obvious, Patent Owner argues that the plain and ordinary meaning of the term “apply a [top/bottom] bias voltage on a gate terminal of the [TSG/BSG] transistor of the first memory cell string *in the pre-verify stage and the verify stage*” requires a single voltage level be applied in *both* the pre-verify stage and the verify stage.

49. Patent Owner’s proposed construction, requiring a single voltage level to be applied in the pre-verify stage and the verify stage to the TSG and BSG transistors, is consistent with ’957 Patent specification and the plain and ordinary meaning of the claim language. I have also been informed that Patent Owner’s proposed construction is consistent with basic legal principles of claim interpretation. In contrast, the Petition wrongly argues that the claimed “[top/bottom] bias voltage” can have different values in the pre-verify stage and the verify stage, such that the claims would be satisfied by a top bias voltage and a bottom bias voltage with distinct voltage levels being applied in the pre-verify stage as compared to the verify stage. *See* Pet. 61-64, 96-98.

50. The plain and ordinary meaning of applying “a [top/bottom] bias voltage ... in the *pre-verify stage and the verify stage*” requires a constant voltage value be administered in *both* the pre-verify stage and the verify stage. That understanding is further confirmed by the ’957 Patent specification. For instance, in the example show in Figure 4 (reproduced below), the ’957 Patent notes that a “**bias**

voltage (or top bias voltage), such as 5 volts” is administered to the chosen TSG layer and a **“bias voltage (or bottom bias voltage), such as 5 volts”** is administered to the BSG layer throughout the **“pre-pulse stage,”** and that these same bias voltages “can be maintained to keep the channel of the selected memory cell string conductive” throughout the following **verify/read stage**.



'957 Patent, Fig. 4, 10:57-11:15 (describing the voltages applied in the pre-pulse stage), 11:16-57 (describing the voltages applied in the verify/read stage), Fig. 4.

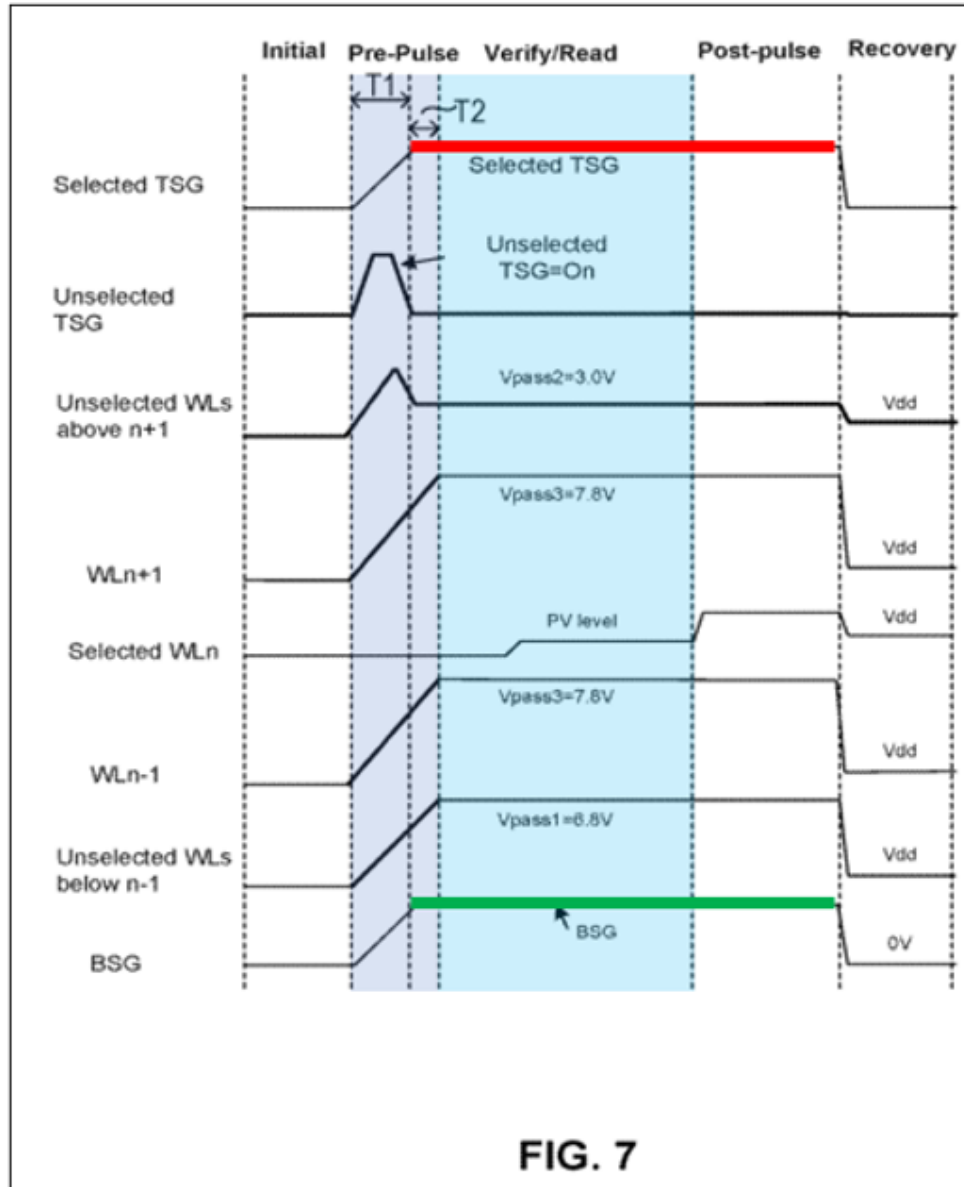
Each of the other embodiments of the '957 Patent, such as those illustrated in Figs. 5-9, likewise portray a top bias voltage and bottom bias voltage with a constant value being applied in both a verify stage and a pre-verify stage. *See, e.g., '957 Patent Figs. 5-9.*

51. By comparison, the arguments presented by Petitioner and Dr. Liu seemingly ignore the requirement that the claimed bias voltages are administered in the “pre-verify stage and the verify stage.” *See, e.g., Pet. 61-64, 96-98.* In particular, the Petition contends that the added limitations of claims 5 and 6 are satisfied by a “top bias voltage” and “bottom bias voltage” that have a first voltage level being applied in the pre-verify stage, and an entirely different voltage level being administered in the subsequent verify stage. *See, e.g., Pet. 61-69, 96-102.* The Petition puts forth two arguments to support that interpretation, neither of which establishes that the “top bias voltage” and “bottom bias voltage” recited in claims 5 and 6 can have wholly different voltage levels in the verify stage and the pre-verify stage.

52. **First Argument:** First, Petitioner cites to legal precedent for the proposition that indefinite article “a” can mean more than one. I am not a lawyer and have no opinions on the merits of this argument. I have been informed by counsel that to the extent the claim language reciting “a top bias voltage” may allow for multiple “top bias voltages” to be present in the device, it does not remove the

requirement for at least one of those “top bias voltages” to be applied in “the pre-verify stage *and* the verify stage” as recited by the claims 5 and 6. Similarly, I have been informed that it does not remove the requirement for at least one “bottom bias voltage” to be applied in “the pre-verify stage *and* the verify stage.” In other words, whether or not multiple bias voltages may be present in the claimed apparatus is a separate issue from whether the voltages must be “applied in the pre-verify stage and the verify stage” as recited in claims 5 and 6.

53. **Second Argument:** Second, Petitioner incorrectly argues that based on the embodiment illustrated in Figure 7 of the '957 Patent, any given “top bias voltage” or “bottom bias voltage” may have different values at different times. Pet. 62. I disagree with Petitioner’s argument. As shown in the annotated version of Figure 7 below, much like the other figures in the '957 Patent, Figure 7 illustrates a **bottom bias voltage** with a fixed voltage level administered to the BSG layer in both the **pre-pulse stage** and the subsequent **verify/read stage**, and similarly illustrates a **top bias voltage** with a fixed voltage level being administered to the TSG layer in both the **pre-pulse stage** and the subsequent **verify/read stage**.



54. For the reasons above, I agree with Patent Owner's interpretation of the claim language, and disagree with Petitioner's proposed interpretation. The plain and ordinary meaning of the claim language and the '957 Patent specification confirm that the limitation "apply a [top/bottom] bias voltage on a gate terminal of the [TSG/BSG] transistor of the first memory cell string *in the pre-verify stage and*

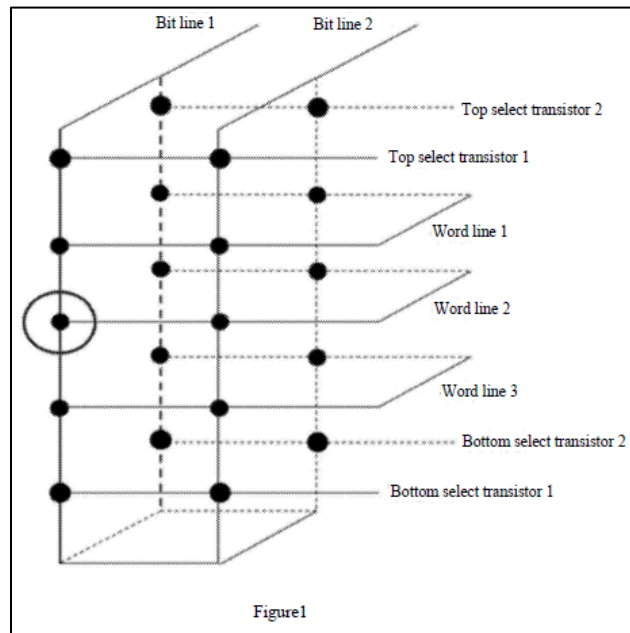
the verify stage” as recited in claims 5 and 6 is properly understood to require a single voltage level be applied in *both* the verify stage and the pre-verify stage.

IX. THE ASSERTED PRIOR ART

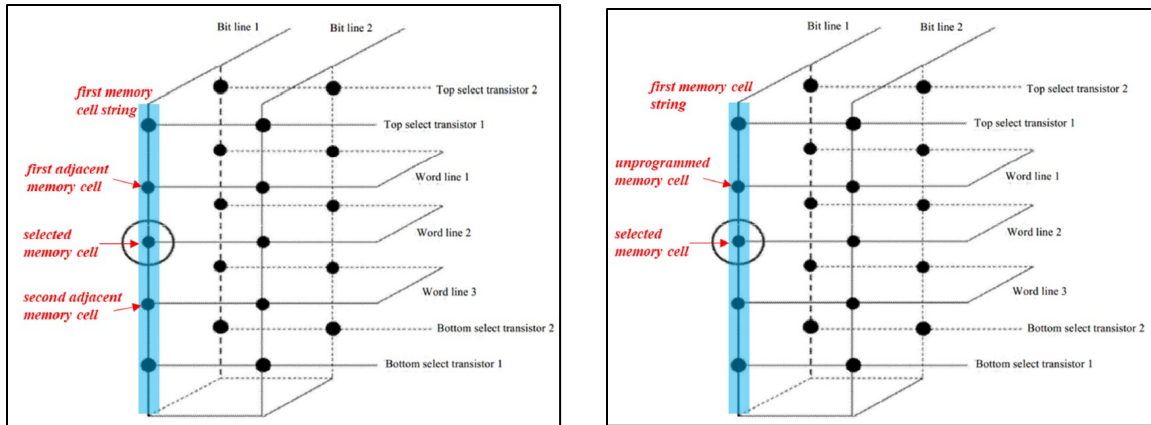
A. Chinese Pat. App. Pub. No. 109065091 (“Hongtao”) (Ex. 1005)

55. Petitioner and Dr. Liu do not argue that Hongtao anticipates the Challenged Claims. Rather, they argue that the combination of Hongtao and Yu (Ground 1) only renders obvious the Challenged Claims. *See* Pet., 27-40. Hongtao generally describes a multi-step process for reading memory cells in a 3D NAND flash memory device by using “a pre-conduction phase and a reading phase step in sequence,” which Petitioner incorrectly equates to the claimed “pre-verify stage” and “verify stage” recited by claim 1 of the ’957 Patent. *See* Hongtao, [0006]; Pet. 20-22, 30-40. In contrast with the ’957 Patent, Hongtao does not contemplate that the voltages being applied to gate terminals of memory cells need time to fully develop, and does not disclose the voltages that are actually applied on the “gate terminal” of memory cells connected to a given word line. Moreover, Hongtao is explicitly concerned with “reading method” for 3D NAND. Hongtao, Abstract. Hongtao does not disclose a “verify” operation, it does not discuss techniques for performing a “verify” operation, and it does not otherwise disclose that the pre-conduction phase described as part of a “reading” operation would also be used in the context of a verify operation to prepare for a subsequent “verify stage.”

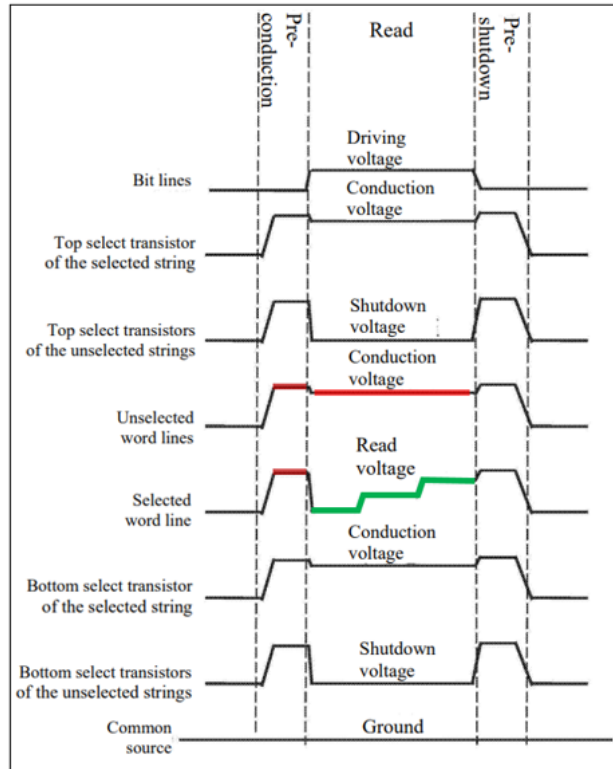
56. As illustrated in Figure 1 of Hongtao (reproduced below), Hongtao describes a 3D NAND device with an array of vertically-oriented “memory strings” formed by “memory cells.”



Hongtao, [0018], Fig. 1. To apply voltages to the memory cell transistors during a reading operation, Hongtao explains “gates of the memory cells” are each “connected” to a “word line.” *Id.* As shown in the annotated versions of Figure 1 of Hongtao included in the Petition (reproduced below), Petitioner equates the circled memory cell with the “selected word line” recited in the Challenged Claims. The Petition also appears to inconsistently identify the memory cell above the circled one as both the “first adjacent memory cell” recited in claim 1, as well as the “not programmed memory cell” recited in claim 1. *See* Pet. 30, 36.



57. Hongtao states that a “**pre-conduction voltage** is administered to both the unselected word line and the selected word line to activate the channels of the selected string and the unselected string” during a pre-conduction phase. *See* Hongtao, [0023]. For example, as depicted in Figure 2 of Hongtao annotated below, in the subsequent reading phase “the unselected memory cells on the selected string are applied with a **conduction voltage** through the unselected word lines” while the selected memory cell accepts a succession of **read voltages**. Hongtao, [0025].

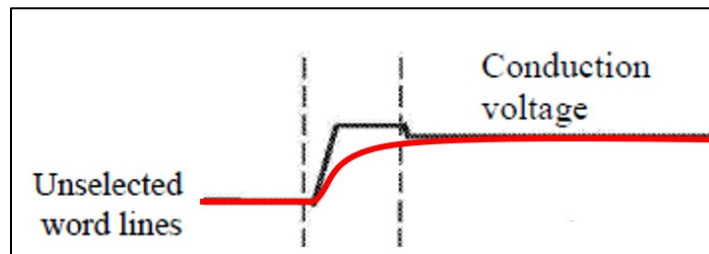


58. The Petition incorrectly argues that the “**pre-conduction voltage**” and the “**conduction voltage**” described in Hongtao are analogous to the claimed “first bias voltage on a gate terminal” and “second bias voltage applied to the gate terminal.” *See* Pet. 30-40. Based on the way that those voltages are illustrated in Figure 2 of Hongtao, Petitioner argues that Hongtao thus discloses a teaches “[a] second bias voltage is smaller than [a] first bias voltage” applied to a gate terminal of a memory cell that is not programmed, as recited by independent claim 1. *See* Pet. 39-40. However, Figure 2 of Hongtao depicts the target voltages that are being administered to the word line layers, and does not reflect the actual bias voltages that are present at any specific time at the gate terminals of the memory cells, which

would be subject to RC time-constant arising from large capacitances within the 3D NAND structure. *See* Hongtao [0023], [0025]. Indeed, as I discuss further in Section X.B, in a 3D NAND memory device such as the one disclosed by Hongtao, each word line has an RC time-constant that arises from the large capacitances produced by the layered structure of the device. *See, e.g.*, Ex. 1014 (“Aritome”), 350-353 (discussing the “RC (resistance-capacitance) delay” in word lines, and describing how “[i]n stacked word-line (WL) structure in 3D NAND cells ... a WL capacitance is greatly increased from 2D cells”). As a result, the voltages applied on the gate terminals of memory cells will be curved and delayed relative to the “target” voltages depicted in Hongtao’s timing diagrams.

59. To the extent that Figure 2 of Hongtao illustrates target voltages being applied to word line layers, it does not disclose or otherwise render obvious the additional details that would be needed in order to determine how the resulting voltages applied to the gate terminals of the connected memory cells would change over time. Petitioner and Dr. Liu have also failed to present any arguments why a POSITA would have found it obvious to implement Hongtao’s design in such a way that the actual voltages being applied on the memory cells would develop fully or otherwise become equivalent to the target voltage levels depicted in Figure 2. This is in contrast to the ’957 Patent itself, which contemplates that the bias voltages being applied to particular memory cells may have insufficient time to fully develop

to a target value within a given stage of the verification operation. *See* '957 Patent, 11:58-12:9, 12:10-27. Thus, a POSITA would understand that the **voltages applied on the gate terminals** could also be smoothed out similar to the below, and there would be no smaller second bias voltage applied on the gate terminals in the later time period:



B. U.S. Pat. Pub. No. 2019/0198117 (“Yu”) (Ex. 1006)

60. Petitioner and Dr. Liu do not argue that Yu anticipates the Challenged Claims. Rather, they argue that the combination of Hongtao and Yu (Ground 1) only renders obvious the Challenged Claims. Pet., 27-40. Yu does not disclose using different bias voltages in a “pre-verify stage” and a “verify stage” wherein the second bias voltage is smaller than the first bias voltage as required by the Challenged Claims, nor does the Petition argue that Yu discloses this subject matter. At most, Yu discusses procedures for programming a string of memory cells in a programming order and verifying the programmed value of memory cell after it has been programmed. But Yu does not disclose or otherwise render obvious that a verification operation has a distinct “pre-verify stage” and “verify stage” with different voltages being used in each stage.

C. U.S. Pat. Pub. No. 2021/0082505 (“Suzuki”) (Ex. 1007)

61. The Petition does not raise any Obviousness arguments based on Suzuki, but instead argues that Suzuki (Ground 2) only anticipates the Challenged Claims. Pet., 7-8, 74-102. Suzuki is generally directed to a “program loop” that is partitioned into a “program operation,” a “recovery operation” (which itself contains a “end operations of the program operation” and a “ready operation of the verify operation”) and “verify operation” which are performed one after the other. *See* Suzuki, [0028].

62. For example, as shown in Figure 11 (annotated below), the program loop is split into ten distinct time periods. The period from “time t0 to time t3 corresponds to a program operation.” Suzuki, [0131]. The period from “time t3 to time t6 corresponds to a recovery operation.” Suzuki, [0131]. Finally, the period from “time t6 to time t9 corresponds to a verify operation.” Suzuki, [0131]. Suzuki further explains that the recovery operation that takes place from t3-t6 “is an operation in which an end operation of the program operation and the ready operation of the verify operation are combined,” meaning that both of those operations are contained within the ready operation. Suzuki, [0131]. As depicted below, the recovery operation starts with an “**end operation of the program operation**” during the period from t3-t4, which mirrors the voltages used during the program operation from t1-t2. The recovery operation also finishes with the “**ready**

operation of the verify operation” during the period from t5-t6, which includes voltages being applied to ready the device for the subsequent verify operation. Finally, the period from t4-t5 in between is a **transition period** between the two. See Suzuki, [0131].

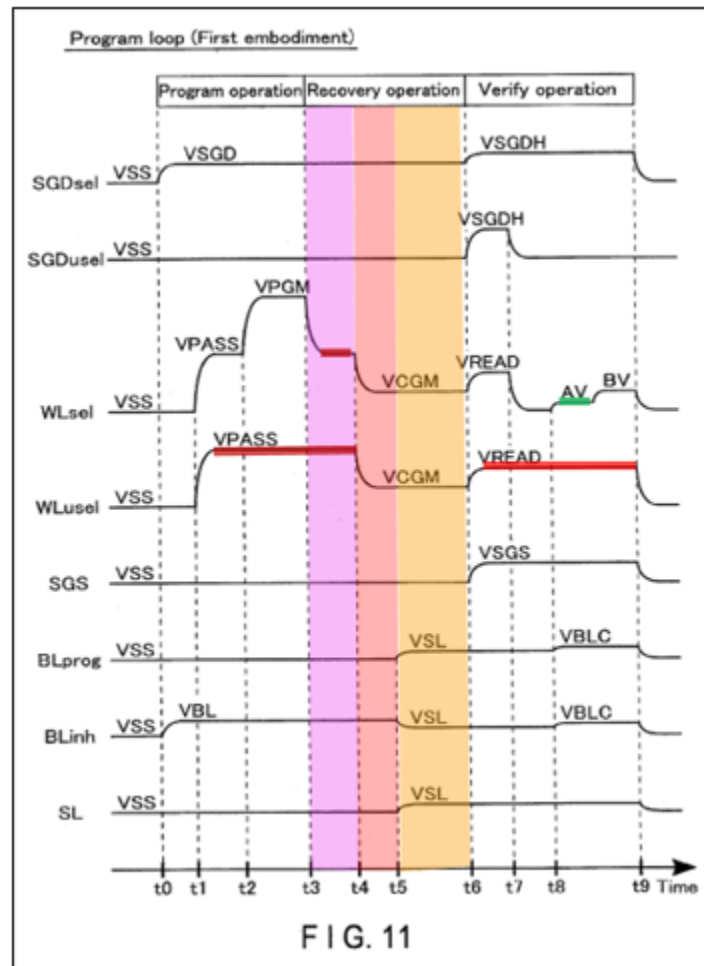


FIG. 11

63. The voltages applied at the start of the recovery operation at time period t3-t4 (i.e., the **“end operation of the program operation”**) mirror the voltages applied during the programming operation from time period t1-t2. As shown in Figure 11, at time t3 **“VPASS”** is administered to the selected word line “WLsel,”

and “**VPASS**” is also administered to the unselected word line “WL_{usel}.” Suzuki, [0134], [0137]. By comparison, during the final part of the recovery operation (including the period from t₅-t₆ that acts as a “**ready operation of the verify operation**”), the voltage “VCGM,” which is described as “lower than VPASS,” is applied to “WL_{sel}” and “WL_{usel}” instead. Suzuki, [0138]. The VCGM voltage applied from period t₅-t₆ (i.e., the **ready operation of the verify operation**) is also lower than the **VREAD** voltage applied during the later verify operation. *See* Suzuki, [0142] (explaining “VREAD is a higher voltage than VCGM”). At the start of the verify operation a time t₆, “**VREAD** is administered to every one of the word lines,” including both WL_{sel} and WL_{usel}. Suzuki, [0114]. Afterwards, starting at time t₈, the “verify voltages **AV** and BV” are administered to the selected word line WL_{sel}. Suzuki, [0145].

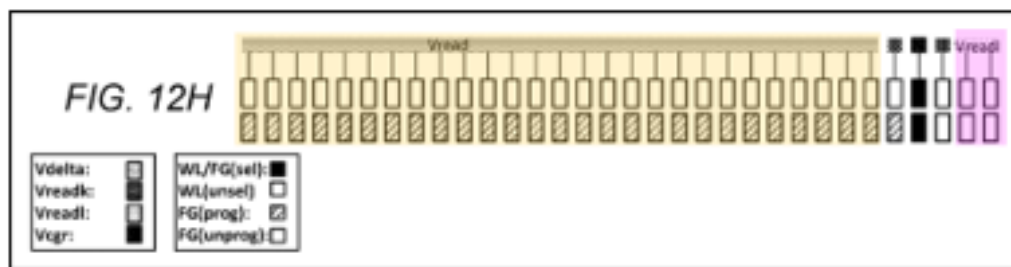
64. The Petition wrongly asserts that Suzuki’s “**VPASS**” is equivalent to the claimed “first bias voltage” applied in a “pre-verify stage,” and that “**VREAD**” is equivalent to the claimed “second bias voltage” less than the first bias voltage which is applied in a “verify stage.” But contrary to what the Petition asserts, the time period from t₃-t₄ when “**VPASS**” is applied to the selected word line (i.e., the alleged “first bias voltage”) is not applied in a “pre-verify” stage as required by the Challenged Claims. That time period from t₃-t₄ is “**an end operation of the program operation**,” which is not a “pre-verify stage” under any reasonable

interpretation of that term. Suzuki, [0131]. Indeed, the “**end operation of the program operation**” cannot reasonably be understood as a “pre-verify” stage for several reasons, including the fact that it is still a part of the programming operation, and because the voltages applied during the “end operation” do not prepare the device for a later “verify stage.” Accordingly, **VPASS** is applied during the program operation (specifically, during **an end operation of the program operation**) rather than a pre-verify stage. Moreover, **VPASS** is never used to prepare the memory string for a subsequent verify stage.

D. U.S. Pat. Pub. No. 2018/0012667 (“Costa”) (Ex. 1008)

65. Petitioner and Dr. Liu do not argue that Costa anticipates the Challenged Claims. Rather, they argue that the combination of Costa in view of Seo (Ground 3) only renders obvious the Challenged Claims. *See* Pet. 7-8, 103-126. Costa generally describes methods that purportedly “reduc[e] errors when sensing in non-volatile memory” by utilizing distinct reading voltages. Costa, [0028]. As part of that disclosure, Costa states that the “pass voltage” used for unprogrammed memory cells can be lower than the pass voltage used for programmed memory cells. *See* Costa [0121]-[0122], [0147]. This is because, as explained by Costa, programming a memory cell might raise the threshold voltage, while the unprogrammed memory cells are known to have a low threshold voltage corresponding to the erased state. *See* Costa [0082]. Accordingly, a “lower read pass

voltage *VreadL* can be used while still ensuring that these memory cells operate as pass gates” because the unprogrammed cells are in an erased state. Costa [0122]. This can be seen in the example shown in Figure 12H, which illustrates a default “*Vread*” value being used for previously programmed memory cells, and a smaller “*Vreadl*” value being used for the unprogrammed memory cells that are known to be in the erased state:



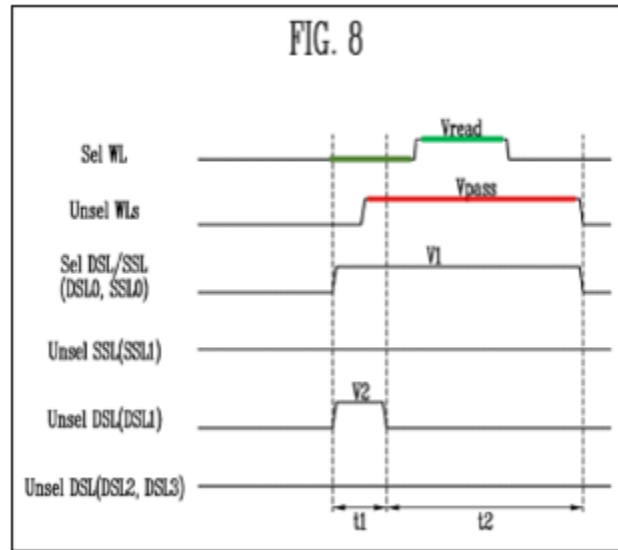
66. But regardless of whether “*Vread*” or “*Vreadl*” is used as the pass voltage for a given memory cell, Costa does not disclose or render obvious that *different* voltages are used on at least one memory cell in a “pre-verify stage” as compared to a “verify stage,” as required by independent claim 1 of the ’957 Patent. Costa also does not contemplate that the voltages being applied to memory cells need time to fully develop, and further fails to disclose or render obvious that distinct bias voltages are applied “*on a gate terminal* of at least one memory cell of the first memory cell string that is not programmed” during different stages of a verification operation. Rather, the most that Costa suggests is that different target “pass voltages” (e.g., “*Vread*” or “*Vreadl*”) can be applied to different memory cells based on whether they have been previously programmed. But regardless of which voltage

level is used for each memory cell, the voltages applied to a given memory cell are fixed throughout the entirety of the sensing operation.

E. U.S. Pat. Pub. No. 2021/0027848 (“Seo”) (Ex. 1009)

67. Petitioner and Dr. Liu do not argue that Seo anticipates the Challenged Claims. Rather, they argue only that the combination of Seo and Costa (Ground 3) renders obvious the Challenged Claims. Seo generally describes a “read” operation for a memory device that is partitioned into a “second time period t2” and a “first time period t1,” with different voltages being administered in each time period. Seo [0011]. But Seo has similar shortcomings as Costa, and does not disclose or render obvious multiple distinct bias voltages (e.g., in the form of different pass voltage levels) being administered to an unselected word line in the different time periods.

68. For example, Figure 8 of Seo illustrates distinct voltage levels being administered to selected word lines “Sel WL,” and unselected word lines, “Unsel WLs” *See* Seo, [0086]-[0090]. Starting with the selected word line (“Sel WL”), an **unspecified voltage** is administered throughout time period t1, and is subsequently replaced with “the read voltage **Vread** ... during a second time period t2.” Seo [0090]. By comparison, for “Unsel WLs,” “the pass voltage **Vpass** may be applied to unselected word lines” in both a part of time period t1 and time period t2. Seo, [0089].



69. To the extent Seo describes voltages being administered to the word lines, Seo does not disclose or render obvious that these voltages illustrated in stylized form in Figure 8 would also result in similar voltages being applied to the gate terminals of the corresponding memory cells connected to those word lines, nor have Petitioner and Dr. Liu presented any arguments or evidence that the voltages being applied on the gate terminals of the memory cells would be able to develop fully and reach values similar to those shown in Figure 8. *C.f.* '957 Patent, 11:58-12:9, 12:10-27 (describing that bias voltages need time to develop fully to target voltage values). Moreover, even if it were assumed that the voltages being applied to the gate terminals of the memory cells actually matched the stylized waveforms as illustrated in Figure 8 above, Seo does not describe that the value of V_{pass} administered to a given word line would shift between “time period t_1 ” and “time period t_2 .” Rather, the Petition seemingly admits that Seo does not describe different

bias voltages being applied to word lines in a “verify stage” and a “pre-verify stage,” as recited by independent Claim 1. *See* Pet. 26, 103-126.

X. PETITIONER’S GROUND 1: HONGTAO IN VIEW OF YU DOES NOT DISCLOSE OR RENDER OBVIOUS CLAIMS 1-6

70. Ground 1 of the Petition alleges that Hongtao in view of Yu discloses or renders obvious claims 1-6.

71. As explained below in Section X.A, Hongtao in view of Yu does not disclose or render obvious a “pre-verify stage” as required by limitations [1.a] and [1.b]. Hongtao and Yu, alone or in combination, do not disclose or render obvious a verification operation with a “pre-verify stage” and a separate “verify” stage. To the extent Hongtao discloses a multi-stage reading operation, reading and verifying are distinct operations, and Hongtao does not itself disclose or render obvious multi-staged verification operations with a separate “pre-verify stage” and “verify stage.”

72. Additionally, as explained below in Section X.B, Hongtao in view of Yu does not disclose or render obvious applying a “first bias voltage” to the gate terminal of a not programmed memory cell, and then applying a “second bias voltage ... smaller than the first bias voltage” to that gate terminal, as required by limitations [1.b] and [1.d]. The Petition mischaracterizes Figure 2 of Hongtao as disclosing this subject matter. But Hongtao illustrates only target voltages applied to word lines, and not the resulting bias voltages that actually develop over time on the gate terminals of the connected memory cells. As such, Hongtao and Yu fail to disclose

or render obvious a “second bias voltage” applied to a gate terminal that is smaller than a “first bias voltage.”

73. Additionally, as explained below in Section X.C, Hongtao in view of Yu does not disclose or render obvious the added limitations of dependent claims 5 and 6 which require, among other things, that a “top bias voltage” and a “bottom bias voltage” are administered in “the pre-verify stage and the verify stage”

A. Independent Claim 1: Hongtao in View of Yu Does Not Disclose or Render Obvious a “Pre-Verify Stage” (Limitations [1.a]-[1.b])

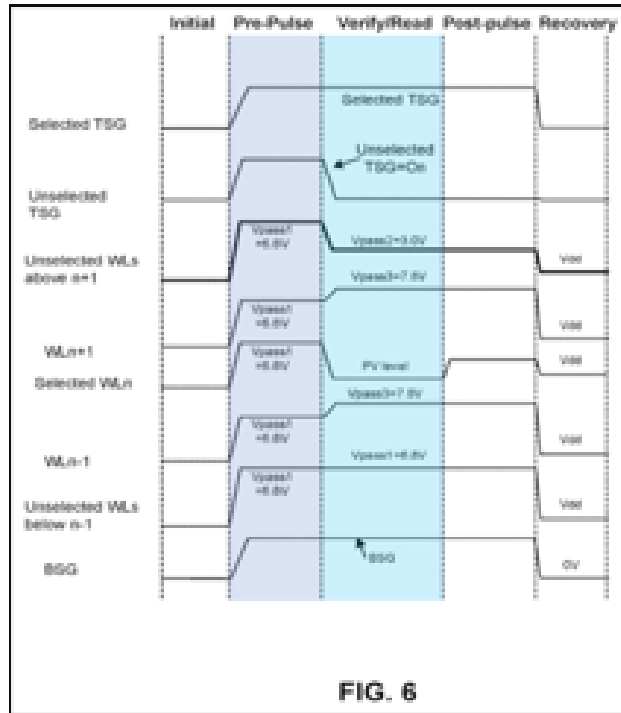
74. Hongtao in view of Yu does not disclose or render obvious a verification operation with a distinct “pre-verify stage,” as recited by limitations [1.a]-[1.b].

75. The Petition mistakenly argues that this subject matter is obvious from the combination of Hongtao in view of Yu. But Hongtao does not disclose or render obvious any type of verification operation, and does not disclose or render obvious that a verification operation would be separated into a distinct “pre-verify stage” and “verify stage.” Yu does not address this deficiency. To the extent Yu discloses that verification operations may be used as part of a programming loop, Yu does not disclose or render obvious that those verification operations include a distinct “pre-verify stage.” The combination of Hongtao and Yu also fails to disclose or render obvious this subject matter, and Petitioner’s proposed combination fails to show that a POSITA would combine the purported teachings of Hongtao and Yu in order to

yield verification operation that has distinct “pre-verify” and “verify” stages as required by the Challenged Claims.

76. Each of the Challenged Claims of the '957 Patent requires processing circuitry configured to: “**apply, in the pre-verify stage**, a first bias voltage on a gate terminal of at least one memory cell of the first memory cell string that is not programmed” (Element [1.b]); and “**apply, in the pre-verify stage**, a first bias voltage on a gate terminal of at least one memory cell of the first memory cell string that is not programmed” (Element [1.b]). These limitations are also required by dependent claims 2-6 by virtue of their dependency on claim 1 of the '957 Patent.

77. As described in Section VI, and depicted in Figure 6 (annotated below), the claimed invention of the '957 Patent describes techniques for performing verification operations that improve over traditional systems, in part, by dividing the operation into a distinct **pre-verify stage** and **verify stage** with different sets of voltages being administered in each one. *See* '957 Patent, Fig. 6, 1:58-2:8, 6:37-49, 17:32-56. In doing so, “the gradient of the channel potential of the selected memory cell string can be reduced,” meaning that “HCI cannot be generated from the selected memory cell to the upper adjacent memory cell of the selected in the selected memory cell string.”



'957 Patent, 12:63-13:4, Fig. 6. In contrast, Hongtao in view of Yu fails to disclose or otherwise render obvious that a verification operation is divided into a distinct **pre-verify stage** and **verify stage**.

78. Reading and verifying are distinct operations, and Hongtao is expressly concerned with techniques to perform a “reading method” for 3D NAND. *See* Hongtao, Abstract. By comparison, Hongtao does not provide any disclosures that are directed to “verification” operations specifically. To the extent Hongtao discloses a “reading method” that includes “a pre-conduction phase and a reading phase step in sequence” that purportedly reduces “read interference during the reading process” (*see* Hongtao, [0005]-[0007]), Hongtao does not disclose or otherwise suggest that a similar approach could be used to create a verify operation

with a separate “pre-verify stage” and “verify stage” as recited by independent claim 1 of the ’957 Patent. To the contrary, Hongtao is directed to only reading operations, and Hongtao does not disclose or render obvious any type of verification operation with “pre-verify” and “verify” stages as required by claim 1 of the ’957 Patent.

79. Yu does not address this deficiency in Hongtao’s disclosure. Like Hongtao, Yu similarly fails to teach or otherwise render obvious that a verification operation has a distinct “pre-verify stage.” Rather, Yu discloses that “[e]ach program loop may include a program operation and a program verification operation,” and offers no additional details apart from the statement that “during the program verification operation, the voltage generator 460 may apply a program verification voltage to the first word line and may apply a verification pass voltage to the unselected word lines.” Yu, [0049], [0054]. Yu does not disclose or otherwise render obvious that a verification operation has a distinct “verify stage” and “pre-verify stage,” and Petitioner and Dr. Liu have not suggested that Yu does.

80. The Petition also fails to demonstrate that a POSITA would have been motivated to apply Hongtao’s purported teachings for a “reading method” to the “verification operation” disclosed in Yu in such a way that it results in a verification operation with a distinct “pre-verify stage” and “verify stage.” Insofar as Hongtao discloses a “reading method” that includes “a pre-conduction phase and a reading phase step in sequence” with the intent of reducing read interference, it does not

follow that the combination of Hongtao and Yu renders obvious a verification operation with a separate “verify stage” and “pre-verify stage.”

81. Petitioner and Dr. Liu incorrectly argue that a POSITA would have been motivated use Hongtao’s reading operations to implement the verification operations described in Yu because “read operations and verify operations are virtually identical” and “fine-tuned read operations” would also be suitable for verifying. *See* Pet. 72-74. That is incorrect. Reading operations and verifying operations are related, but distinct operations. They take place in different contexts, and are often tailored to address different sets of concerns. Indeed, even art included with the Petition is filled with examples of the two operations being treated differently. *See, e.g.*, Ex. 1021, [0103] (distinguishing a “verification read operation” and a “normal read operation”); Ex. 1020, 16:16-21 (distinguishing “verify operations and read operations” which each use different voltage on “the selected word line”) Ex. 1019, 17:10-14 (distinguishing “sensing operations” that “include a read operation” from those that “include a verify test which determines whether the V_{th} of a memory cell exceeds the verify voltage”); Ex. 1017, 3:21-29 (distinguishing a “read” and a “program verify” as different types of sensing operation that use distinct “read reference voltages for a read operation” and a “verify voltage for a program verify operation”).

82. Further differences between reading and verifying also arise from the fact that verification operations are used as an iterative check within a programming cycle after every programming operation (e.g., by repeatedly performing programming operations and verifying operations until each memory cell within the programming order is programmed correctly), while reading operations are independent processes that are instead used to check the stored state of a cell. These differences may be particularly pronounced when using a fixed programming order, such as in Yu. *See* Yu [0115]. For example, when performed on memory cells that are being programmed in a fixed order, all of the memory cells above (or below) the selected memory cell that is being verified are known to be unprogrammed. This allows a lower bias voltage to be used on the gates of the unprogrammed memory cells while still ensuring that the memory cells are turned on. *See, e.g.,* '957, 12:28-13:4, Fig. 6 (using lower voltages on WLs above $n+1$ during the verify/read stage as compared to WLs below $n-1$); Costa [0122] (describing that a “lower read pass voltage” can be used on memory that “have not undergone programming” while “still ensuring that these memory cells operate as pass gates”). Petitioner and Dr. Liu do not account for these distinctions between verify operations and reading operations, and has presented no arguments or evidence—beyond the conclusory statement that functions are somehow identical—to show that a POSITA would have been motivated to combine Hongtao’s reading operation into Yu’s verify operations.

83. To the extent that the '957 Patent itself refers to “verifying/reading” (or “verify/read” operations), it is clear from context that the operation being described is for verifying that a recently programmed memory cell was programmed correctly. For example, this is why the '957 Patent describes the use of “verify” voltages, and why the '957 Patent describes a “programming verify (PV) level” being used to sense when a “selected memory cell is programmed correctly.” *See* '957 Fig. 4, 11:35-57.

84. As the Board correctly recognized with respect to Ground 3 in the Decision to Institute (“DI”), even if it were assumed that teachings related to reading operations could be applied directly to verify operations, it does not follow that any two-stage reading operation would result in a “pre-verify stage” and a “verify stage” when used to implement a verification operation. DI, 26-27 (the reference “only describes time periods t1 and t2 with respect to performing a read operation,” and “[i]n light of the disclosures in [the reference] it is not clear that time period t1 is a ‘pre-verify stage’ as claimed”). Petitioner and Dr. Liu attempt to overcome this deficiency by improperly conflating verify operations with read operations, and by mischaracterizing Hongtao as teaching a “read/verify phase” despite Hongtao making no mention of verification operations (or a “verify” phase) whatsoever. *See* Pet., 32; Liu, ¶105. To the contrary, Hongtao does not disclose a “read/verify phase” or any other type of distinct stages that might occur within a verification operation,

and to the extent Hongtao describes a “read operation” that includes a “pre-conduction phase” to help mitigate read disturb, it does not imply that a POSITA would be motivated to combine Hongtao and Yu to render obvious a verification operation that is partitioned into separate “pre-verify” and “verify” stages with distinct voltages being administered in each.

85. For at least the reasons above, Hongtao in view of Yu fails to disclose or render obvious that distinct verify voltages and bias voltages are applied in a “pre-verify stage,” as recited by limitations [1.a]-[1.b].

86. For at least the same reasons, Hongtao in view of Yu also fails to disclose or render obvious the limitations of dependent claims 2-6.

B. Independent Claim 1: Hongtao in View of Yu Does Not Disclose or Render Obvious Applying “a First Bias Voltage” and “a Second Bias Voltage” on the Gate Terminal of a Not Programmed Memory Cell “Wherein the Second Bias Voltage Is Smaller than the First Bias Voltage” (Limitations [1.b], [1.d])

87. Hongtao in view of Yu does not disclose or render obvious applying “a first bias voltage” and “a second bias voltage” on the gate terminal of a not programmed memory cell “wherein the second bias voltage is smaller than the first bias voltage,” as recited by limitations [1.b] and [1.d].

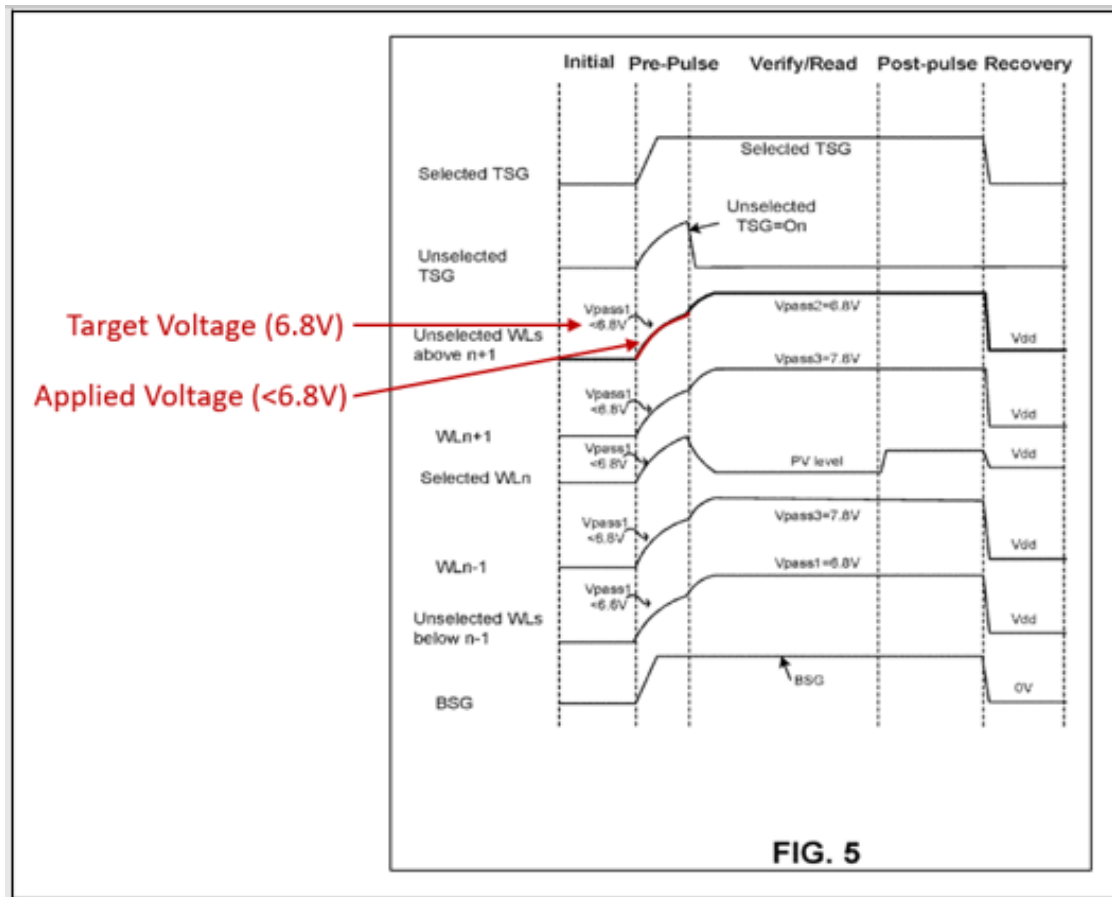
88. Petitioner and Dr. Liu improperly rely on Figure 2 of Hongtao as disclosing that a “first bias voltage” and a smaller “second bias voltage” are applied to a not programmed memory cell. But Figure 2 of Hongtao depicts target voltages

being applied to word lines, rather than the resulting voltages that are applied on the gate terminals of the memory cells. As explained by the '957 Patent, there is a key difference between the target values that are applied onto word lines, and the “bias voltage on a gate terminal” that develops over time as a result. Petitioner and Dr. Liu have ignored this distinction, and mischaracterize Hongtao’s disclosure in the process. Appropriately understood, Figure 2 of Hongtao does not disclose or otherwise render obvious to a POSITA that the applied “second bias voltage on a gate terminal” is smaller than the applied “first bias voltage” as recited by independent claim 1 of the '957 Patent.

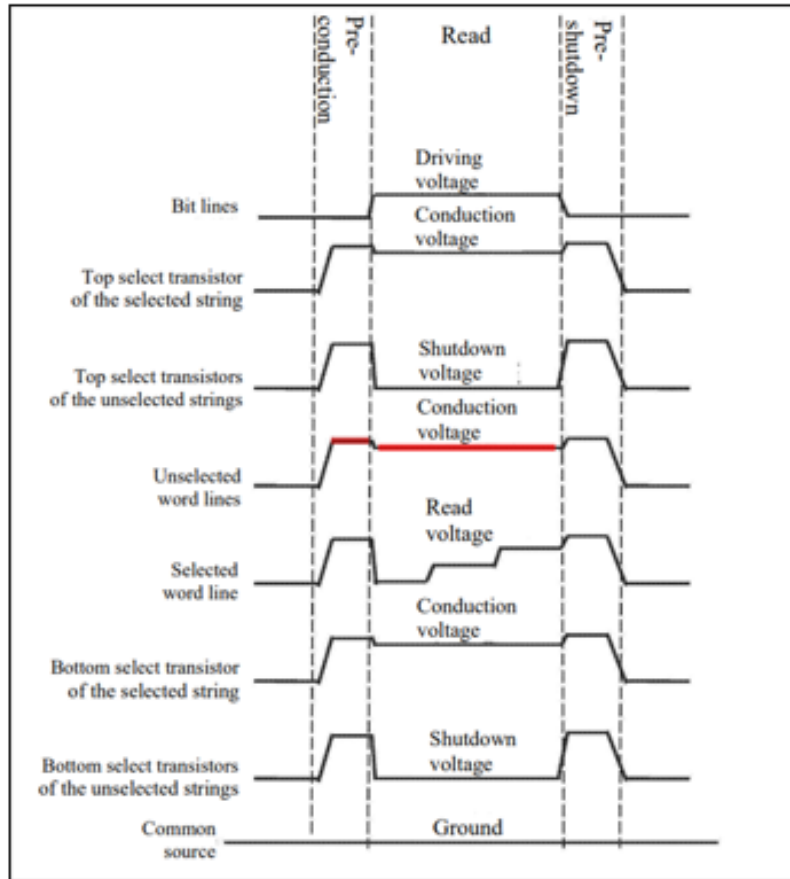
89. Each of the Challenged Claims of the '957 Patent requires processing circuitry configured to: “**apply, in the pre-verify stage, a first bias voltage on a gate terminal of at least one memory cell of the first memory cell string that is not programmed**” (Element [1.b]); and “**apply, in the verify stage, a second bias voltage on the gate terminal of the at least one memory cell of the first memory cell string that is not programmed, wherein the second bias voltage is smaller than the first bias voltage**” (Element [1.d]). These limitations are also required by dependent claims 2-6 by virtue of their dependency on claim 1 of the '957 Patent.

90. As described in Section VI, the '957 Patent describes an approach for performing verification operations that improves over traditional systems, in part, by applying “a lower bias voltage” on a gate terminal of an unprogrammed memory

cell in the verify stage as compared to the preceding pre-verify stage. *See* '957 Patent, 12:63-13:4. By doing so, “the gradient of the channel potential of the selected memory cell string can be reduced,” which helps to mitigate hot carrier injection (HCI) effects between the selected memory cell and its neighbors. '957 Patent, 12:63-13:4 (“HCI cannot be generated from the selected memory cell to the upper adjacent memory cell of the selected in the selected memory cell string.”). As also discussed in Section VI, the '957 Patent differentiates between the voltages applied to word line layers in a pre-pulse stage, and the resulting bias voltages that are applied on the gate terminals of the corresponding memory cells, which develop over time as a result. *See, e.g.*, '957 Patent, 11:68-12:9, 12:10-27. For example, as shown in Figure 5 of the '957 Patent, when a short pre-pulse time is used the bias voltages that are applied may not have sufficient time to develop fully, resulting in the bias voltages being “less than a target value, such as 6.8 volts” during the initial pre-pulse period. '957 Patent, Fig. 5, 12:18-19.



91. Unlike the '957 Patent, the text of Hongtao's specification does not describe applying a "second bias voltage" smaller than a "first bias voltage" to the gate terminal of an unprogrammed memory cell. Instead, Petitioner and Dr. Liu rely on Figure 2 of Hongtao as purportedly disclosing this subject matter. Specifically, the Petition contends that this subject matter is disclosed in Hongtao based on the depiction of the "**pre-conduction voltage**" and "**conduction voltage**" included in Figure 2 of Hongtao (reproduced below). *See* Pet. 39-40.



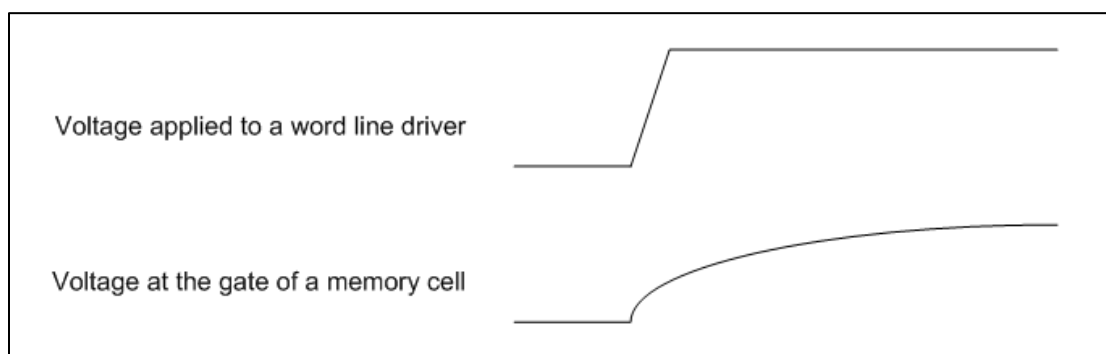
92. The Petition improperly suggests that Figure 2 of Hongtao, on its own, discloses or otherwise renders obvious processing circuitry configured to “apply, in the pre-verify stage, a first bias voltage on a gate terminal of at least one [not programmed] memory cell,” and “apply, in the verify stage, a second bias voltage on the gate terminal of the at least one [not programmed] memory cell ... wherein the second bias voltage is smaller than the first bias voltage,” as recited by independent claim 1 of the ’957 Patent. Pet. 39-40. In particular, the Petition incorrectly argues that Figure 2 of Hongtao meets those claim limitations because “the voltage signal applied to the unselected word lines ramps down from the pre-

conduction voltage to reach the conduction voltage.” Pet. 39-40. But that is not what claim 1 of the ’957 Patent requires. To the contrary, independent claim 1 is directed to the actual bias voltages which are applied “*on a gate terminal*” of the memory cell, rather than the target voltages being applied to the corresponding word lines.

93. In the Decision to Institute, the Board mistakenly interpreted Figure 2 of Hongtao as depicting the actual voltages being applied on the gate terminals of the memory cells. *See* DI, 14-15. The Board cited two pieces of evidence in support. First, the Board cited Hongtao’s disclosure that the “gates of the unselected memory cells on the selected string are applied with a conduction voltage through the unselected word lines.” DI, 14-15 (*citing* Hongtao, [0025]). Second, the Board credited Dr. Liu’s testimony that “the respective voltage is applied through a conductor coupled to the corresponding cell or transistor, i.e., a word line coupled to a corresponding memory cell (which in 3D memories, is actually a conductive gate layer).” DI, 14-15 (*citing* Ex. 1003 (“Liu”), ¶56). But that explanation, which equates applied word line voltages and gate terminal voltages, is incomplete. Properly interpreted, a POSITA would have understood Figure 2 of Hongtao to be describing the target voltages applied to word lines, rather than the resulting bias voltages that are actually applied on the gate terminals of the memory cells.

94. In a 3D NAND memory device, such as the ones disclosed by Hongtao and the ’957 Patent, each word line has an RC time-constant that arises from the

large capacitances produced by the layered structure of the device. *See, e.g.*, Ex. 1014 (“Aritome”), 350-353 (discussing the “RC (resistance-capacitance) delay” in word lines, and describing how “[i]n stacked word-line (WL) structure in 3D NAND cells ... a WL capacitance is greatly increased from 2D cells”). Word line drivers, or analogous voltage generation circuits, operate as voltage sources that charge up the word lines and force them to reach specific target voltages over time. As a result, the “target” voltages being applied to the word lines may differ from the resulting voltages that are applied on the gate terminals of the memory cells, which will appear distorted due to the RC time constants involved. For example, I prepared the figure below to help illustrate this phenomenon. As shown below, when a voltage is applied to a given word line, the resulting voltages applied on the gate terminals of the memory cells will appear as curved lines that charge-up over time based on the RC time-constants associated with a given word line layer:



The value of the RC time-constant, and the shape of the resulting waveforms that are applied to the gate terminals of the memory cells as a result of a given set of target voltages being applied to the word lines, depends on many factors. Those

factors typically including the time scales of the applied waveforms, the materials used to create the device, and the physical structure and layout of the device, each of which impacts at least the capacitances involved and the corresponding RC time constants.

95. The fact that applied voltages will be curved and distorted was also confirmed by Petitioner's expert, Dr. Liu, during his deposition for IPR2024-00795, which I am also involved in, and which relates to another YMTC patent that is similarly directed to 3D NAND technology. *See* Ex. 2006 ("Liu822 Tr."), 62:16-73:20. For example, when Dr. Liu was asked why Figure 8B of U.S. 10,726,920 ("Yang") (Ex. 2007) depicts word line voltages as curved waveforms, Dr. Liu replied that a "signal *takes time to go from the voltage generation circuit and be reinserted to the word line*, there would be a parasitic component that causes slight delay in charging the word line." Liu822 Tr., 63:22-64:3. He further explained that "in the real world *there is always going to be parasitic component[s]*," and that it is "inevitable" there will be "resistance components ... [and] capacitor components, so that it's always going to have some type of ramping time." Liu822 Tr., 64:9-22; *see also id.* 65:24-12 (confirming the curve that appears is determined by an "R and C component," which in turn relies on the device's "architecture" and "design").

96. In contrast with the '957 Patent, Hongtao does not address the fact that that the voltages applied to gate voltages need time to develop over time. Moreover,

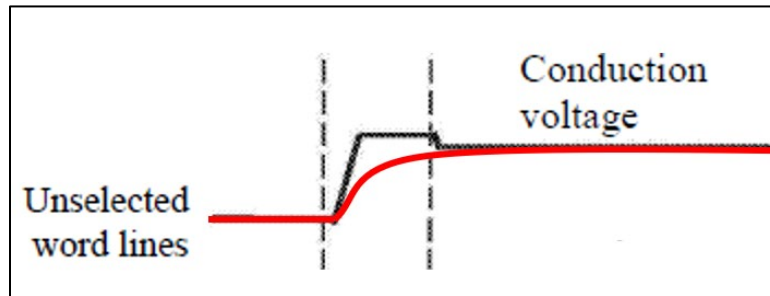
Figure 2 of Hongtao does not provide sufficient information to ascertain the actual bias voltages that will be applied on the gate terminals of the memory cells over time. I have been informed that drawings can only be relied on for purposes of invalidity based on what they would reasonably disclose and suggest to a POSITA. But Hongtao would not disclose or otherwise suggest to a POSITA that Figure 2 is depicting the actual bias voltages applied to gate terminals. Rather, the waveforms illustrated in Figure 2 of Hongtao depict steep slew rates (i.e., change rates of voltage through time), straight lines, and sudden changes signifying target voltages—all of which indicate that Hongtao is illustrating target voltages, rather than the resulting voltages that develop over time on the gate terminals of the memory cells. Furthermore, Hongtao also fails to disclose any of the other details that would be needed to determine how the gate voltages develop over time, such as the architecture of the device and the length of the pre-conduction period. *Cf.* '957 Patent, 11:58-12:9, 12:10-27 (discussing that bias voltages require enough time to progress fully and providing examples). Petitioner and Dr. Liu have also failed to provide any further arguments or evidence to address this missing piece in Hongtao's disclosure.

97. Unlike what Dr. Liu states in his declaration at ¶120, the purported “drop” depicted in Figure 2 of Hongtao does not indicate that the bias voltages being applied to the gate terminals of the memory cells has actually been reduced. *See*

Hongtao Fig. 2. To the contrary, Hongtao does not disclose or otherwise suggest that the voltages applied on the gate terminals of the memory cells actually reach the voltage levels depicted in Figure 2 in the pre-conduction phase. *C.f.*, '957 Patent, 12:10-27 (discussing that bias voltages that are unable to fully develop in a given stage may continue to develop and reach the target value in a subsequent stage).

98. The waveforms depicted in Figure 2 of Hongtao also appear to be consistent with techniques used to decrease the time required to power up the gates of the transistors to a unique target level. In general, it would have been advantageous to minimize the time spent in Hongtao's pre-conduction phase. Any excess time spent in the pre-conduction phase is wasted, as it contributes to the total read access time of the device. Accordingly, the pre-conduction phase should be long enough to pre-charge the unselected memory strings, and no longer. The waveform depicted in Figure 2 of Hongtao appears to be a technique to reduce the time spent in the pre-conduction phase by applying a moderately elevated target voltage to the word line drivers. Applying this larger target voltages causes the resulting voltages that develop on the gate terminals of the memory cells to charge up faster, shorting the overall time spent in the pre-conduction phase. Of course, Hongtao does not actually provide enough detail to determine how the corresponding bias voltages being applied to the gate terminals actually develop over time, and Petitioner and Dr. Liu have not provided any explanation for how those

bias voltages would evolve over time. But in a standard system, voltages of the type illustrated in Figure 2 of Hongtao for the unselected word lines would be expected to result in bias voltages applied to the gate terminals of the memory cells that are smoothed out, similar to the voltages depicted in the figure below:



99. There are other reasons why a POSITA looking at Figure 2 of Hongtao would expect the resulting voltages applied on the gate terminals of the memory cells to remain the same between the pre-conduction phase and the reading phase. Changing the bias voltages can also alter the voltages in the strings of memory cells due to capacitive couplings, and create transient currents running down the length of the string that potentially interfere with normal operation of the memory array. Indeed, these transient currents could create false readings of the selected memory cell. Accordingly, it would be expected that the voltages of the type illustrated in Figure 2 of Hongtao would result in voltages applied on the gate terminals of the memory cell that are maintained at a fixed level when going into a reading phase from the pre-conduction phase.

100. When discussing Hongtao's disclosure, Petitioner and Dr. Liu have seemingly overlooked the distinction made in the '957 Patent between the target voltages that are applied to the word line layers, and the resulting bias voltages that are applied to the gate terminals of the memory cells as a result. *See* Section VI (discussing the '957 Patent disclosure). Petitioner and Dr. Liu have not addressed this distinction, and have not presented any arguments about what—if anything—a POSITA would have been able to conclude from the voltages shown in Figure 2 of Hongtao about the actual bias voltages applied to the gate terminals of unprogrammed memory cells.

101. Apart from the waveforms shown in Figure 2 of Hongtao, Petitioner and Dr. Liu make one other erroneous argument as to why Hongtao would suggest applying a lower bias voltage in the reading phase as compared to bias voltages applied the pre-conduction phase. *See* Hongtao Fig. 2. In particular, the Petition mischaracterizes paragraph [0026] of Hongtao as somehow suggesting that bias voltages should be lowered in a read phase relative to the conduction phase. *See* Pet. 22, 40. But paragraph [0026] of Hongtao says no such thing. It does not address the deficiencies in Hongtao's disclosure, nor does it suggest that a POSITA would have interpreted Figure 2 of Hongtao as depicting an actual bias voltages applied "on a gate terminal of a [not programmed] memory cell," rather than target voltages applied to word line layers. *See* Pet. 40.

102. Contrary to what Petitioner and Dr. Liu have suggested, paragraph [0026] of Hongtao does not state that the voltages depicted in Figure 2 for unselected word lines are reduced in the read phase as compared to the conduction phase because “the greater the conduction voltage, the greater the read disturbance.” See Pet. 22, 40; Liu ¶120 (citing Hongtao [0026]). That excerpt, which Petitioner and Dr. Liu have presented out of context, says nothing about the bias voltages being applied on the gate terminals of the memory cells, or reducing such voltages during different portions of the reading operation. Rather, paragraph [0026] is describing the *problems* that exist in the embodiment of Figure 2 as a result of the difference between a bit line “driving voltage” and the “conduction voltage.” Further, the sentences at the end of paragraph [0026] are used to introduce the embodiment of Figure 3, which purportedly addresses the issues being described in [0026]:

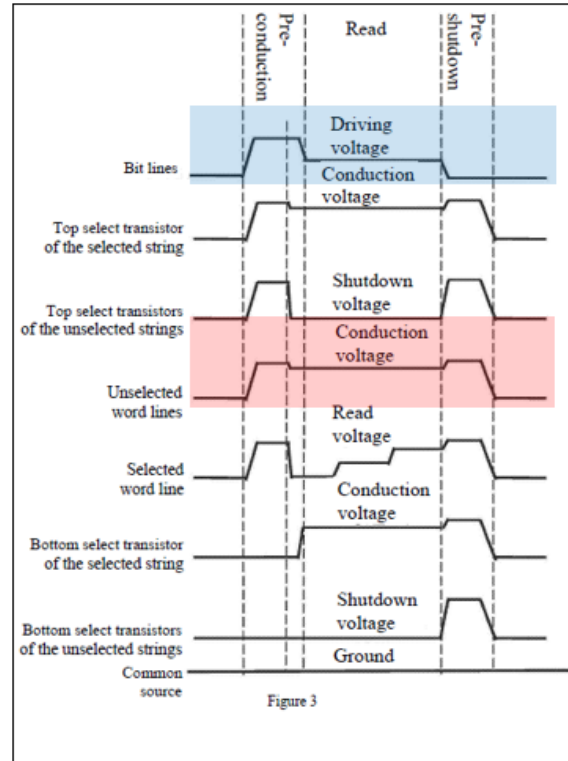
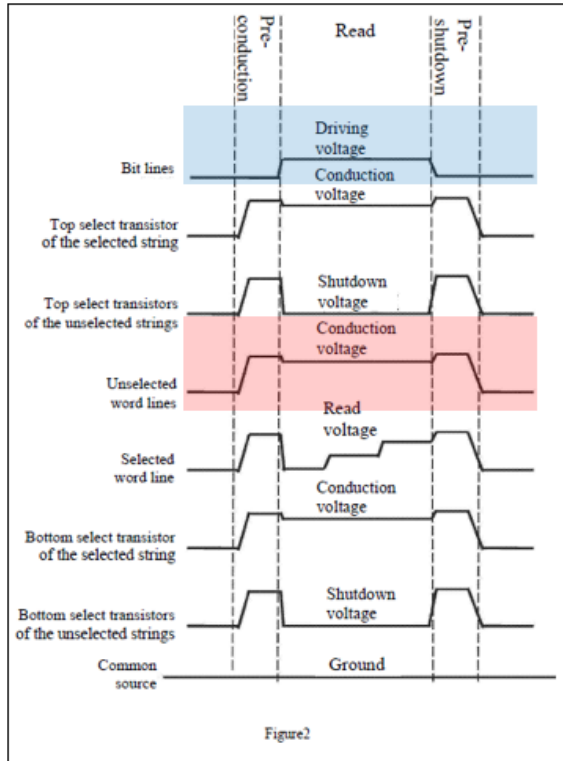
Read interference is positively related to the voltage causing read interference. The greater the voltage, the stronger the read interference. Therefore, the greater the conduction voltage, the greater the read disturbance to the memory cell. Therefore, in this specific embodiment, *the read interference caused by the "conduction voltage - driving voltage"* suffered by the unselected memory cells on the selected string is smaller than the read interference suffered by the memory cells on the unselected string. In order to improve the accuracy of memory reading, it is necessary to further reduce the read interference suffered by the memory cells on the unselected string.

In order to further reduce the read interference suffered by the memory cells with conduction voltage on the unselected strings, the inventors of the present invention propose another reading method of 3D NAND flash memory

Please refer to Figure 3, which is a timing diagram of reading a 3D NAND memory cell using another reading method in another specific embodiment of the present invention.

Hongtao [0026]-[0028].

103. Hongtao goes on to describe the embodiment of Figure 3, which it characterizes as being able to “further reduce the read interference” relative to the embodiment of Figure 2. Hongtao [0027]-[0028], Fig. 3. Accordingly, it is clear from Hongtao’s disclosure that [0026] is not explaining the waveforms illustrated in Figure 2, much less providing a rationale for why a POSITA would want to reduce the bias voltages being applied to unselected word lines in a reading phase as compared to a pre-conduction phase. Rather, paragraph [0026] is explaining a problem with Figure 2, which is being purportedly addressed in Figure 3 by applying a “precharge voltage” to the bit-line in the pre-conduction phase to “precharge” the unselected memory strings and thus “effectively reduce read disturbance.” Hongtao [0034], Fig. 2, Fig. 3.



If Hongtao's description of the Figure 3 embodiment was not enough, a direct comparison between Figure 2 and Figure 3 further confirms that paragraph [0026] has nothing to do with reducing bias voltages applied to unselected word lines during the transition between the pre-conduction phase and the reading phase. Indeed, Figure 3 (which purportedly addresses the issues described in Figure 2) illustrates the exact same waveforms being applied to unselected word lines as Figure 2. In conclusion, there is nothing in paragraph [0026] of Hongtao to suggest that a lower bias voltage should be applied on the gate terminals of the unselected memory during a reading phase as compared to a pre-conduction phase, nor does Hongtao's statement "the greater the conduction voltage, the greater the read disturbance" suggest that a bias voltage applied on the gate terminals of the unselected memory

cells should be reduced during a reading phase. *See* Hongtao, [0026]. Contrary to what the Petition seems to suggest, paragraph [0026] of Hongtao says nothing about why voltages might want to be lowered in different phases of a reading operation, and it is further irrelevant to the ultimate question of what voltages are applied on the gate terminals of the memory cells within the memory string.

104. Yu also fails disclose or render obvious a distinct “first bias voltage” and “second bias voltage” being applied on a gate terminal of an unprogrammed memory cell, and the Petition does not argue that Yu does. Accordingly, Yu is incapable of addressing the deficiencies in Hongtao. Petitioner and Dr. Liu cite to Yu as purportedly disclosing particular aspects of programming operations, such as the use of a distinct programming order and the use of verification operations. *See* Pet. 22, 29, 31, 33-34. But Yu does not disclose any type of multi-stage verification operation, and does not disclose any of the bias voltages that would be used during such an operation. Indeed, the Petition fails to identify portion of Yu’s disclosure that would teach or otherwise render obvious applying distinct bias voltages on the gate terminal of an unprogrammed memory cell, “wherein the second bias voltage is smaller than the first bias voltage,” as recited by independent claim 1.

105. For at least the reasons above, Hongtao in view of Yu fails to disclose or render obvious processing circuitry arranged to “apply ... a first bias voltage on a gate terminal of at least one memory cell of the first memory cell string that is not

programmed,” and “a second bias voltage on the gate terminal of the at least one memory cell of the first memory cell string that is not programmed, wherein the second bias voltage is smaller than the first bias voltage” as recited by limitations [1.b] and [1.d]. Moreover, the arguments presented in the Petition have simply neglected the distinction made in the ’957 Patent between the target voltages applied to word lines, and the resulting voltages that develop over time which are applied on the gate terminals of the associated memory cells.

106. For at least the same reasons, Hongtao in view of Yu also fails to disclose or render obvious the limitations of dependent claims 2-6.

C. Claims 5 and 6: Hongtao in View of Yu Does Not Disclose or Render Obvious a “Top Bias Voltage” or “Bottom Bias Voltage” Applied “In the Pre-Verify Stage and the Verify Stage”

107. Hongtao in view of Yu does not disclose or render obvious a “bottom bias voltage” applied to a BSG (bottom select gate) transistor “in the pre-verify stage and the verify stage,” or a “top bias voltage” applied to a TSG (top select gate) transistor “in the pre-verify stage and the verify stage” as recited by dependent claims 5 and 6. Instead, Petitioner has erroneously tried to map these limitations onto several distinct voltages, none of which is administered in both the “pre-verify stage and the verify stage.”

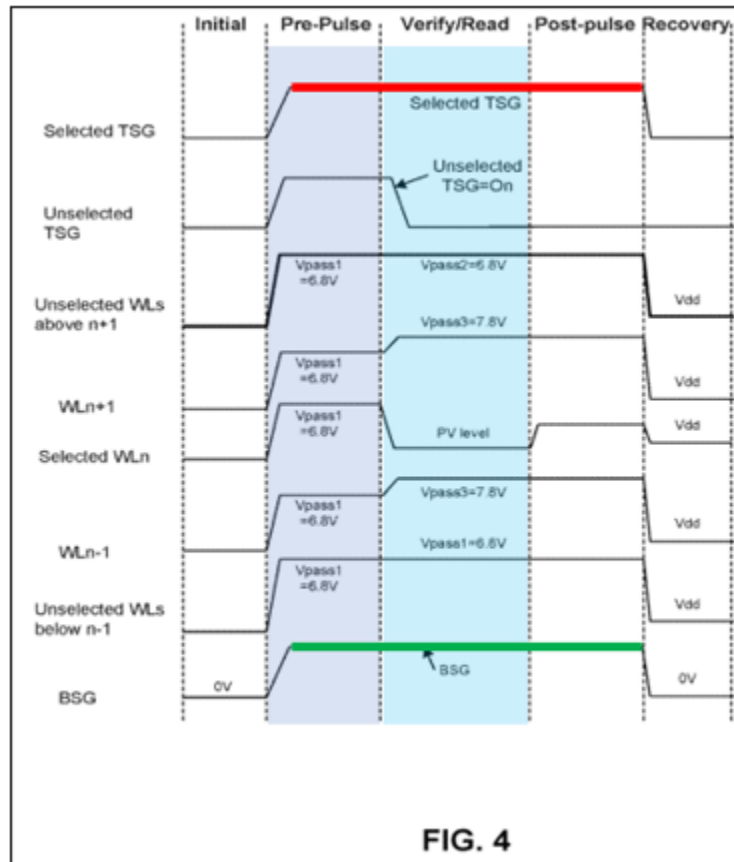
108. Dependent claims 5 recites, among other things, processing circuitry further configured to: “**apply a bottom bias voltage on a gate terminal of the BSG**

transistor of the first memory cell string in the pre-verify stage and the verify stage” (limitation [5.b]); and “**apply a top bias voltage on a gate terminal of the TSG transistor of the first memory cell string in the pre-verify stage and the verify stage**” (limitation [5.c]).

109. Dependent claim 6 also recites, among other things, processing circuitry further configured to: “**apply a bottom bias voltage on a gate terminal of the BSG transistor of the first memory cell string in the pre-verify stage and the verify stage**” (limitation [6.b]); and “**apply a top bias voltage on a gate terminal of the TSG transistor of the first memory cell string in the pre-verify stage and the verify stage**” (limitation [6.c]).

110. The terms “apply a bottom bias voltage on a gate terminal of the BSG transistor of the first memory cell string *in the pre-verify stage and the verify stage*” and “apply a top bias voltage on a gate terminal of the TSG transistor of the first memory cell string *in the pre-verify stage and the verify stage*” require that a single voltage level be applied to the transistors in *both* the verify stage and the pre-verify stage. See Section VI.B (Claim Construction). That interpretation is consistent with the plain and ordinary meaning of the claim language, and the embodiments in the ’957 Patent specification. See, e.g., ’957 Patent, 10:57-11:15, 11:16-57, Fig. 4. For example, as illustrated in Figure 4 of the ’957 Patent, a “**bias voltage (or bottom bias voltage), such as 5 volts**” is administered to the BSG layer, and “**bias voltage**

(or top bias voltage), such as 5 volts” is administered to the selected TSG layer in the “pre-pulse stage,” and is “maintained” throughout the following verify/read stage.

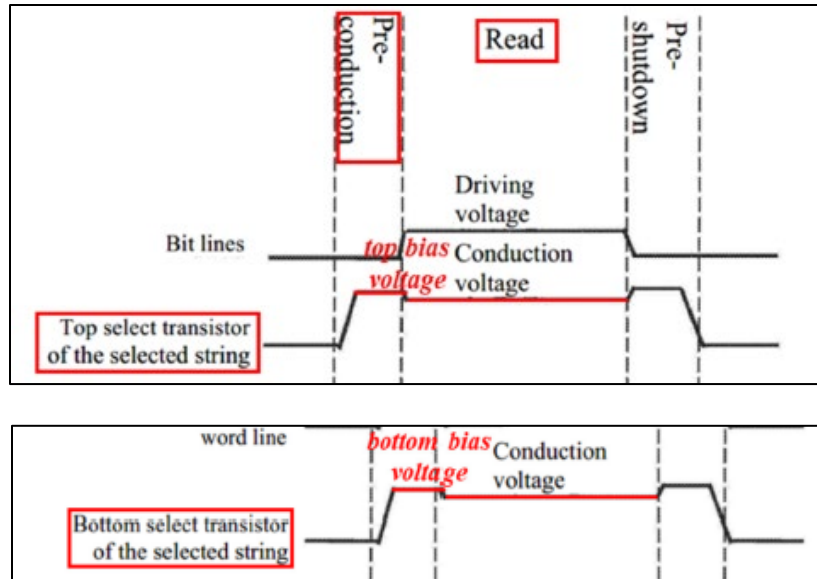


'957 Patent, 10:57-11:15 (discussing the pre-pulse stage), 11:16-57 (discussing the verify/read stage), Fig. 4.

111. Petitioner and Dr. Liu point to Figure 2 of Hongtao as somehow disclosing this material. But even assuming (counterfactually) that Figure 2 of Hongtao is illustrating actual voltages being applied to gate terminals of memory

cells, none of the bias voltages described by Hongtao are applied to a TSG or a BSG in “the pre-verify stage *and* the verify stage” as required by claims 5 and 6.

112. As discussed above in Section X.B, Petitioner and Dr. Liu mischaracterize Figure 2 of Hongtao as disclosing the actual voltages being applied on gate terminals of memory cells. In reality, Figure 2 of Hongtao depicts target voltages, rather than the actual voltages which are applied to gate terminals of the various transistors within the memory string. But even if the Board were to find—as Petitioner and Dr. Liu incorrectly argue—that the waveforms depicted in Figure 2 of Hongtao correspond to actual voltages being applied on gate terminals, Hongtao does not teach bias voltages administered “in the pre-verify stage *and* the verify stage” as necessitated by claims 5 and 6. Instead, as illustrated in the annotated copies of Figure 2 included in the Petition (reproduced below), Hongtao clearly shows *distinct* target voltages being administered to the top select gate and bottom select gate in the pre-conduction stage and the reading stage (i.e., the purported “pre-verify stage” and “verify stage”). Pet. 61-69.



113. Realizing this deficiency, Petitioner and Dr. Liu wrongly argue that claims 5 and 6 can still be satisfied because the “top bias voltage” and “bottom bias voltage” can somehow contain “more than one voltage level.” *See* Petition 62-64, 96-98. I disagree. As I discussed previously in Section VI.B (Claim Construction), the plain and ordinary meaning of “apply a [top/bottom] bias voltage on a gate terminal of the [TSG/BSG] transistor of the first memory cell string *in the pre-verify stage and the verify stage*” requires that a single voltage level be applied in *both* the verify stage and the pre-verify stage. That interpretation is also consistent with all of the embodiments included in the ’957 Patent—including the embodiment of Figure 7 that the Petition mischaracterizes as somehow showing different value in the pre-verify stage and the verify stage. By comparison, Petitioner and Dr. Liu’s proposed interpretation seemingly contradicts the plain and ordinary meaning of the claims, is not supported by the ’957 Patent specification, and does follow the basic principles

of claim interpretation that I have been informed of (e.g., that the recitation of “a” bias voltage does not remove the requirement for at least one of those bias voltages to be applied in “the pre-verify stage *and* the verify stage” as recited by the claims 5 and 6). *See* Section VI.B (Claim Construction). Moreover, the interpretation set forth in the Petition seemingly ignores the requirement that the bias voltages be applied in “the pre-verify stage *and* the verify stage.”

114. Yu does not address the deficiencies in Hongtao. Yu does not disclose or render obvious that a top bias voltage is administered to a TSG in a pre-verify stage and a verify stage, or that a bottom bias voltage is administered to a BSG in a pre-verify stage and a verify stage. Indeed, the Petition does not even attempt to rely on Yu for this subject matter. *See* Pet. 61-69.

115. For at least the reasons provided above, Hongtao in view of Yu fails to disclose or render obvious a “bottom bias voltage” applied to a BSG (bottom select gate) transistor “in the pre-verify stage and the verify stage,” or a “top bias voltage” applied to a TSG (top select gate) transistor “in the pre-verify stage and the verify stage” as recited by dependent claims 5 and 6.

XI. PETITIONER’S GROUND 2: SUZUKI DOES NOT DISCLOSE CLAIMS 1-6

116. Ground 2 of the Petition alleges that Suzuki discloses claims 1-6.

117. As explained below in Section XI.A, Suzuki does not disclose applying “a first bias voltage” in a “pre-verify stage,” and then applying a “second bias voltage

... smaller than the first bias voltage” during a “verify” stage, as required by limitations [1.b] and [1.d]. The purported “pre-bias voltage” identified by Petitioner and Dr. Liu is not administered in a “pre-verify stage,” and even if the Petition were modified to identify some other voltage as a purported “first bias voltage,” all of the other voltages disclosed by Suzuki similarly fail to satisfy limitations [1.b] and [1.d].

118. Additionally, as explained below in Section XI.B, Suzuki does not disclose the added limitations of dependent claims 6 and 5 which require, among other things, that a “top bias voltage” and a “bottom bias voltage” are administered in “the pre-verify stage and the verify stage.”

119. The Petition does not raise any obviousness arguments based on Suzuki, arguing that Suzuki only anticipates the Challenged Claims. However, even if the Petition had raised obviousness arguments, the Challenged Claims would still be valid over Suzuki under an obviousness standard. Suzuki fails to disclose several limitations in the Challenged Claims, and fails to render obvious those limitations for at least the same reasons.

A. Independent Claim 1: Suzuki Does Not Disclose Applying a First Verify Voltage and First Bias Voltage in a “Pre-Verify” Stage, or Applying a Second Bias Voltage in a “Verify” Stage “Wherein the Second Bias Voltage Is Smaller than the First Bias Voltage” (Limitations [1.b], [1.d])

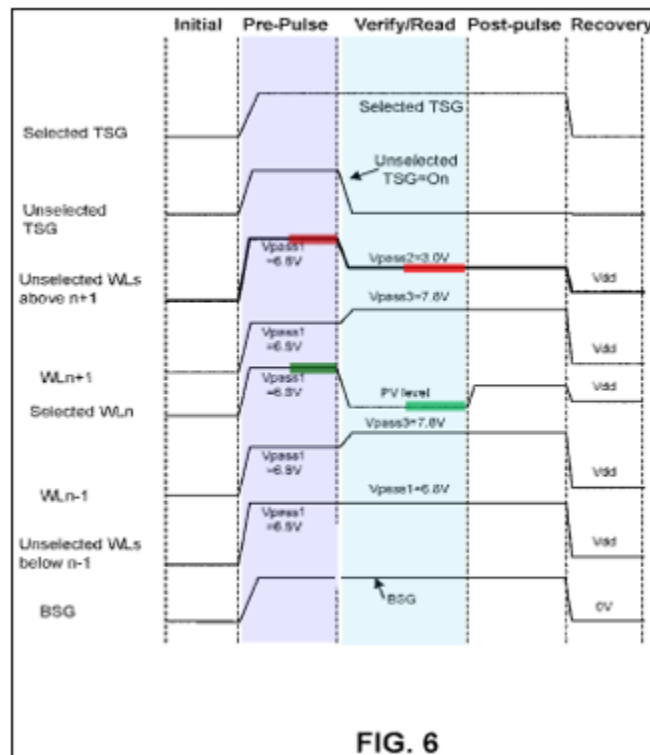
120. Suzuki does not disclose applying a first verify voltage and a first bias voltage in a “pre-verify” stage, or applying a second bias voltage in a “verify” stage

“wherein the second bias voltage is smaller than the first bias voltage,” as recited by limitations [1.b] and [1.d].

121. The Petition argues that Suzuki’s use of a “VPASS” voltage on unselected word lines is equivalent to the “first bias voltage” recited in limitations [1.b] and [1.d]. *See* Pet. 74-85. But Suzuki’s own disclosure, as well as the plain and ordinary meaning of the claim language, makes it clear that the “VPASS” voltage identified in the Petition is not applied during a “pre-verify stage,” as required by the Challenged Claims. Moreover, even assuming that the period preceding Suzuki’s verify operation qualified as a “pre-verify stage,” the bias voltages applied during that period would not satisfy the requirement in limitation [1.d] that the “second bias voltage” applied in the subsequent “verify stage” is “smaller than the first bias voltage” that was applied in the pre-verify stage.

122. Each of the Challenged Claims of the ’957 Patent requires processing circuitry configured to: “**apply, in a pre-verify stage, a first bias voltage on a gate terminal of at least one memory cell of the first memory cell string that is not programmed**” (Element [1.b]); and “**apply, in the verify stage, a second bias voltage on the gate terminal of the at least one memory cell of the first memory cell string that is not programmed, wherein the second bias voltage is smaller than the first bias voltage**” (Element [1.d]). These limitations are also required by dependent claims 2-6 by virtue of their dependency on claim 1 of the ’957 Patent.

123. As discussed in Section II, the claimed invention of the '957 Patent describes an advantageous approach for performing verification operations by separating the operation into distinct “pre-verify” and “verify” stages, thus helping to reduce HCI and resulting ESUM losses. For example, as depicted in Figure 6, the '957 Patent describes preparing the memory string for the verification operation by administering a **first bias voltage** that fully develops on a not programmed memory cell in a **pre-verify stage**. Afterwards, a **second bias voltage** (less than the first verify voltage) is applied in the subsequent **verify stage**. '957 Patent, 1:58-2:8, 6:37-49, 17:32-56.



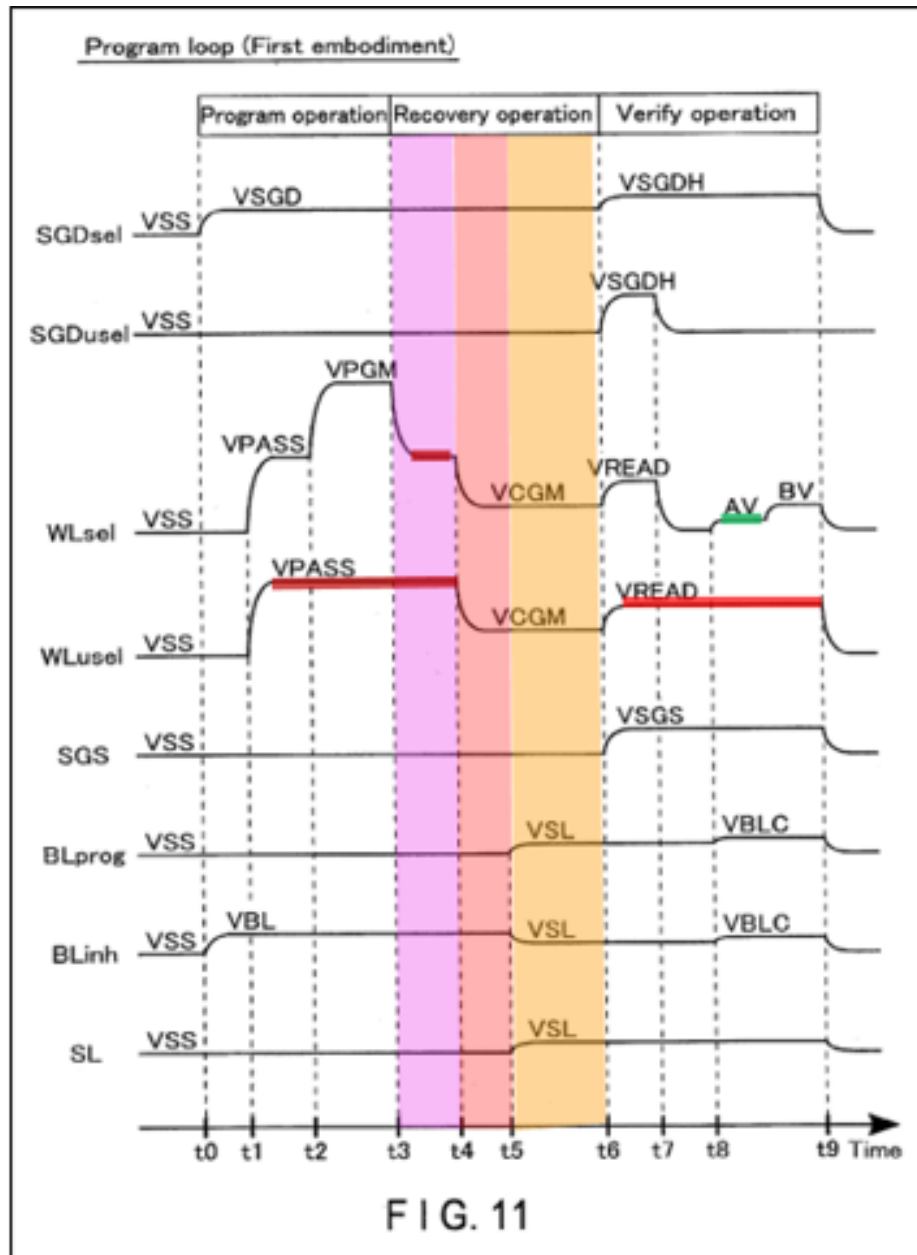
'957 Patent, Figure 6 (annotated).

124. Suzuki does not disclose these features of the '957 Patent. For example, Suzuki fails to disclose a “first bias voltage” being applied in a “pre-verify stage” which is larger than a “second bias voltage” applied in a subsequent “verify stage.” The Petition argues that Suzuki only anticipates the Challenged Claims under 35 U.S.C. §102 and does not include any obviousness arguments based on Suzuki. *See* Pet. 7-8. I understand that a claim is anticipated by a reference only if each and every element is described, either expressly or inherently, in that reference. Because Suzuki does not describe all the elements of claim 1 of the '957 Patent, it is my understanding that Suzuki cannot anticipate the Challenged Claims.

125. Suzuki generally describes a program loop, which describes the process of performing programming and verify operations on different memory cells within the memory string, that is partitioned into several different time periods that are performed on each pass of the loop. As depicted in Figure 11 below, “time t0 to time t3 corresponds to a program operation,” “time t3 to time t6 corresponds to a recovery operation,” and “time t6 to time t9 corresponds to a verify operation.” Suzuki, [0131]. As described in Suzuki, the recovery operation from t3-t6 combines “an end operation of the program operation and the ready operation of the verify operation.” Suzuki, [0131]. In particular, the recovery operation incorporates a period from t3-t4 which is **end operation of the program operation**, a period from t5-t6 with different voltages that perform as a **ready operation of the verify operation**, and a

period from t_4 - t_5 which is a **transition period** between them. See Suzuki, [0131].

These three different parts of the recovery operation are characterized by the different voltages being applied during each part.



126. In the Decision to Institute, the Board questioned if period t_3 - t_4 of Suzuki also qualified as a “ready operation of the verify operation” by virtue of being

included within part of the larger recovery operations. DI, 20. As stated by Suzuki, the recovery operation is “an operation in which an end operation of the program operation and the ready operation of the verify operation are combined.” Suzuki, [0131]. Particularly when read in context, this statement indicates that Suzuki’s “recovery operation” contains both an “end operation of the program operation” and a “ready operation of the verification operation” within it. It does not indicate that the *entirety* of the recovery operation is itself a “ready operation of the verification operation.” The fact that that the period from t3-t4 is not a “ready operation of the verification operation,” and cannot otherwise be a “pre-verify stage” in the sense of the ’957 Patent, is apparent from the voltages being applied during that time period. Notably, the voltages applied during the time period t3-t4, across all the various different word lines, are the same as the voltages applied from t1-t2 at the start of the programming operation when the device begins boosting. *See* Suzuki, Fig. 11. These voltages are indicative of an “end operation of the program operation” which occurs as the device begins to recover from the high VPGM voltages applied during the programming operation. *See* Suzuki, Fig. 11. Moreover, the voltages being applied from the time period t3-t4 do not themselves help to prepare the device for a verify operation, and most of the voltages being applied during that time period—including the voltages applied to the selected word lines, unselected word lines, bit

lines (BLprog and BLinh) and source lines (SL)—are replaced with other values prior to the start of the verify operation that takes place from time period t6-t9.

127. The different sub-parts of the recovery operation each use their own set of voltages. For example, the first part of the recovery operation from t3-t4 is an **end operation of the program operation**. This period has voltages similar to those used during the programming operation, and are functionally identical to those applied during period t1-t2 of the programming operation. At time t3, the only change from the programming operation is that the voltage applied on the selected word line (WLsel) drops from the programming voltage “VPGM” that was used to program the selected word line to the same value “VPASS” that was applied from time period t1-t2. *See* Suzuki, [0133]-[0135], [0137]. The remaining voltages, including the bit line voltage on the “program-inhibited bit line BLinh” that inhibits unselected memory strings from unintentional programming, remain the same. *Id.* In contrast, the period from t5-t6 is a **ready operation of the verify operation**. This is when voltages are applied in order to prepare the device for the verify operation beginning at t6. During this period, “a voltage VSL” is applied to “each of the bit lines BLprog and BLinh and the source line SL” as a voltage VCGM is maintained on both unselected and selected word lines. Suzuki, [0139]. As compared to references like Hongtao and Seo, which illustrate only target voltages for different word lines, Figure 11 of Suzuki has the type of curved lines that are indicative of the actual bias

voltages that would develop over time on the gate terminals of the various transistors connected to the word lines. However, even though Suzuki appears to disclose actual applied voltages, as opposed to target voltages, the voltages disclosed by Suzuki still fail to meet the limitations of the Challenged Claims.

128. The Petition attempts to improperly equate the portion of Suzuki's "**VPASS**" signal applied to the unselected word line (WL_{usel}) from time period t3-t4 with the claimed "first bias voltage" administered throughout a "pre-verify stage." *See* Pet. 79-82. Presumably, the Petition was forced to point "**VPASS**" as a "first bias voltage" because it needed to find a voltage larger than "**VREAD**" (i.e., the purported "second bias voltage") to try satisfying claim 1's requirement that "the second bias voltage is smaller than the first bias voltage." But Suzuki's "**VPASS**" signal applied from time period t3-t4 fails to meet the claim limitations at least because it is not applied in a "pre-verify stage." Indeed, that time period from t3-t4 is not part of the "**ready operation of the verify operation**" which instead occurs between t5-t6. Instead, the voltages administered from t3-t4—including the **VPASS** identified in the Petition—are part of the "**end operation of the program operation**," and do not themselves prepare the device for the subsequent verify stage. Suzuki, [0131]. Petitioner and Dr. Liu do not address the fact that the voltages applied during the different parts of the recovery operation differ from one another, and that these voltages serve different purposes in the context of Suzuki's system.

129. Suzuki's program operation, including both the portion that occurs from time period t0-t3 and the "end operation of the program operation" that takes place from t3-t4, fails to qualify as a "pre-verify stage" in the sense of the '957 Patent. Similarly, the "VPASS" signal applied to unselected word lines from t1-t4 does not qualify as a "first bias voltage" applied "in a pre-verify stage" as required by the Challenged Claims. Indeed, the "VPASS" signal serves no purpose related to the "verify" operation. The "VPASS" signal is first applied to unselected word lines during the middle of the programming operation at time t1, it is continued throughout the remainder of the programming operation from t1-t3, it persists for a short time afterwards during the "end operation of the program operation" that takes place from t3-t4, and it is replaced by other voltages well before the start of the "verify operation" from t6-t9. *See* Suzuki [0131] [0133]-[0135], [0137], Fig. 11. The fact that the time period from t3-t4 is not a "pre-verify stage" is also apparent from the fact that those voltages do not themselves ready the device for the supposed "verify stage." *See id.* To the contrary, for each of the waveform depicted in Figure 11, the voltages being applied from t3-t4 (i.e., the program operation's end operation) mirror the voltages utilized throughout t1-t2 at the beginning of the programming operation, and do not themselves help to prepare the device for the later verify stage that begins at t6. *See* Suzuki, Fig. 11.

130. The Petition does not address the voltages applied during Suzuki's **“ready operation of the verify operation,”** which takes place during the time period from t5-t6 and precedes the “verify operation” that starts at t6. However, a comparison between the '957 Patent and Suzuki shows key differences between the techniques employed by each one when preparing for a verify operation. For example, in the '957 Patent the bias voltages applied to unselected word lines in the verify/read stage are *smaller* than the bias voltages applied in the earlier pre-pulse stage. *See* '957 Patent, Fig. 6. By comparison, Suzuki uses the opposite approach by applying a VREAD voltage to unselected word lines during the verify operation that is *larger* than the VCGM voltage being applied in the preceding “ready operation of the verify operation.” Suzuki, Fig. 11, [0131], [0142] (explicitly stating that “VREAD is a higher voltage than VCGM”).

131. Petitioner and Dr. Liu do not discuss the voltages applied from time period t5-t6 that precede the verify operation. But even if they had attempted to present an alternative argument based on the voltages applied during t5-t6 (i.e., the **“ready operation of the verify operation”**), Suzuki would still fail to disclose all the features of the Challenged Claims. For example, even if Petitioner and Dr. Liu had attempted to map the claimed “first bias voltages” to Suzuki's “VCGM” voltage that is administered throughout the “ready operation of the verify operation” from t5-t6, such a mapping would still disclose all the features independent claim 1. *See*

Suzuki, [0131], [0138]-[0139]. Indeed, claim 1 explicitly requires that the “second bias voltage” applied during the “verify stage” is “smaller than the first bias voltage” applied during the “pre-verify stage.” But this is the exact opposite of what Suzuki discloses. Rather, Suzuki teaches that “VREAD is a higher voltage than VCGM” (i.e., that the supposed “second bias voltage” specified by Petitioner as being applied during the verify stage “is higher” than the VCGM voltage that came before it). Suzuki, [0142].

132. For at least the reasons above, under the proposed mapping set forth in the Petition, the purported “first bias voltage” disclosed by Suzuki (i.e., “**VPASS**”) is not applied during a “pre-verify stage” as required by limitation [1.b]. Moreover, even if Petitioner and Dr. Liu altered the mapping presented in the Petition (e.g., by pointing to the VCGM voltage applied in the t5-t6 period immediately prior to Suzuki’s verification operation as the “first bias voltage”), at no point does Suzuki disclose applying a “first bias voltage” during a pre-verify stage, and then applying a “second bias voltage” during a verify stage “wherein the second bias voltage is smaller than the first bias voltage” as required by limitations [1.b] and [1.d].

133. For at least the same reasons, Suzuki does not disclose the limitations of dependent claims 2-6.

B. Claims 5 and 6: Suzuki Does Not Disclose a “Top Bias Voltage” or “Bottom Bias Voltage” Applied “In the Pre-Verify Stage and the Verify Stage”

134. Suzuki does not disclose a “bottom bias voltage” applied to a BSG (bottom select gate) transistor “in the pre-verify stage and the verify stage,” or a “top bias voltage” applied to a TSG (top select gate) transistor “in the pre-verify stage and the verify stage” as recited by dependent claims 5 and 6. Rather, Suzuki discloses that distinct voltages are applied to BSG and TSG in the pre-verify stage and the verify stage. Petitioner and Dr. Liu erroneously argue that Suzuki nonetheless satisfies the claims by mapping each of the claimed bias voltages onto multiple different voltage levels. But none of the BSG/TSG voltages discussed in Suzuki are applied in both the “pre-verify stage and the verify stage.”

135. Dependent claims 5 recites, among other things, processing circuitry further configured to: “**apply a bottom bias voltage on a gate terminal of the BSG transistor of the first memory cell string in the pre-verify stage and the verify stage**” (limitation [5.b]); and “**apply a top bias voltage on a gate terminal of the TSG transistor of the first memory cell string in the pre-verify stage and the verify stage**” (limitation [5.c]).

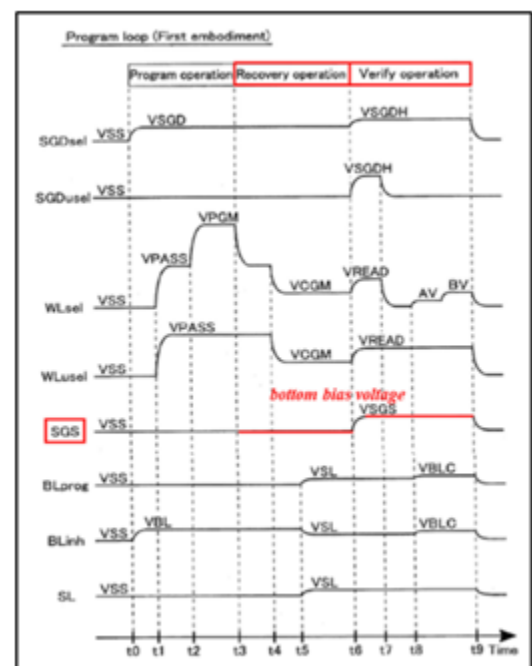
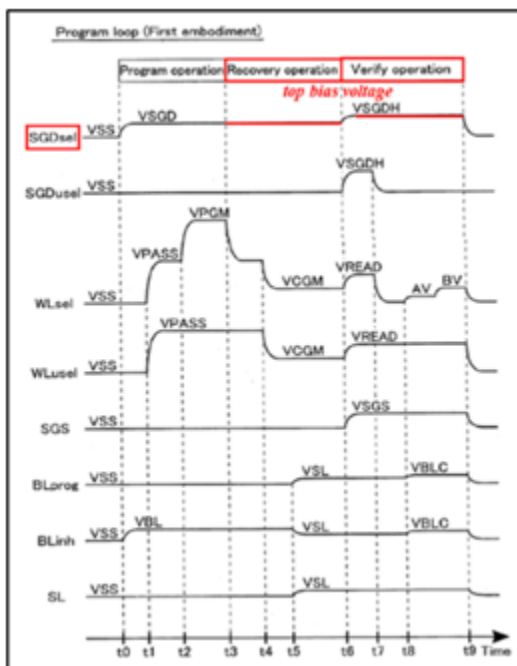
136. Dependent claim 6 also recites, among other things, processing circuitry further configured to: “**apply a bottom bias voltage on a gate terminal of the BSG transistor of the first memory cell string in the pre-verify stage and**

the verify stage” (limitation [6.b]); and “**apply a top bias voltage on a gate terminal of the TSG transistor of the first memory cell string in the pre-verify stage and the verify stage**” (limitation [6.c]).

137. The terms “apply a bottom bias voltage on a gate terminal of the BSG transistor of the first memory cell string *in the pre-verify stage and the verify stage*” and “apply a top bias voltage on a gate terminal of the TSG transistor of the first memory cell string *in the pre-verify stage and the verify stage*” require that a single voltage level be applied to the transistors in *both* the verify stage and the pre-verify stage. *See* Section VI.B (Claim Construction). That interpretation is consistent with the plain and ordinary meaning of the claim language, and all of the embodiments in the ’957 Patent specification. *See, e.g.,* ’957 Patent, 10:57-11:15, 11:16-57, Fig. 4.

138. Under that interpretation, Suzuki fails to disclose the added limitations of dependent claims 5 and 6. Suzuki describes several different voltages being applied to select gates, which Petitioner and Dr. Liu have attempted to characterize as “bottom bias voltages” and “top bias voltages.” Unlike Seo and Hongtao, the curved lines depicted in Suzuki denote actual bias voltages being applied on the gate terminals of the transistors, rather than target voltages. But even so, none of the alleged “bottom bias voltages” and “top bias voltages” identified in the Petition is applied in *both* “the verify stage and the pre-verify stage.” Rather, the voltages

depicted in Figure 11 of Suzuki as being administered to the select gate transistors have distinct voltage levels in the verify stage and the pre-verify stage, with no overlap between them whatsoever. For example, as shown in the annotated images included in the Petition (reproduced below), the voltage being applied to the purported BSG (bottom select gate) changes from a value of “Vss” to a value of “VSHG” at the start of the verify operation at time t6. Similarly, the voltage being applied to the purported TSG (top select gate) changes from a value of “VSGD” to a value of “VSGDH” at the start of the verify operation at time t6.



Pet., 96-102. Neither of these waveforms depicts a single voltage level being applied to the TSG or BSG in **both** “the verify stage and the pre-verify stage,” as required by the added limitations of dependent claims 5 and 6. *See* Section VI.B (Claim Construction).

139. Similar to the arguments raised with respect to Ground 1 (Hongtao in view of Yu) that I discussed above in Section X.C, Petitioner incorrectly asserts that the claims are nevertheless anticipated by Suzuki because the claimed “top bias voltage” and “bottom bias voltage” can each have “more than one voltage level.” *See* Petition 62-64, 96-98. But as discussed in Section VI.B (Claim Construction), Petitioner and Dr. Liu’s proposed interpretation contradicts the plain and ordinary meaning of the term “apply a [top/bottom] bias voltage on a gate terminal of the [TSG/BSG] transistor of the first memory cell string *in the pre-verify stage and the verify stage*,” is not supported by the ’957 Patent specification, and does not appear to abide by the basic principles of claim interpretation that I have been informed of (e.g., that the recitation of “a” bias voltage does not remove the requirement for at least one of those bias voltages to be applied in “the pre-verify stage *and* the verify stage” as recited by the claims 5 and 6). Moreover, under Petitioner’s proposed interpretation, the requirement that the bias voltages be applied “the pre-verify stage *and* the verify stage” is seemingly ignored.

140. For at least the reasons provided above, Suzuki fails to disclose a “bottom bias voltage” applied to a BSG (bottom select gate) transistor “in the pre-verify stage and the verify stage,” or a “top bias voltage” applied to a TSG (top select gate) transistor “in the pre-verify stage and the verify stage” as recited by dependent

claims 5 and 6. At no point does Suzuki disclose voltages applied in both the “pre-verify stage *and* the verify stage” as required by dependent claims 5 and 6.

XII. PETITIONER’S GROUND 3: COSTA IN VIEW OF SEO DOES NOT DISCLOSE OR RENDER OBVIOUS CLAIMS 1-6

141. Ground 3 of the Petition alleges that Costa in view of Seo discloses or renders obvious claims 1-6.

142. As explained below in Section XII.A, Costa in view of Seo does not disclose or render obvious a “pre-verify stage” as required by limitations [1.a]-[1.b]. Costa and Seo, alone or in combination, do not disclose or render obvious a two-part verify operation with a “pre-verify stage” and a separate “verify” stage. Costa does not disclose or render obvious a two-part verify operation that begins with a distinct “pre-verify stage.” Seo does not disclose a verify operation of any kind, and similarly fails to disclose or render obvious a two-part verify operation that begins with a distinct “pre-verify stage.” Moreover, the Petition fails to show that a POSITA would have been motivated to combine Costa and Seo in a way that yields a multi-stage verification operation with a separate “pre-verify stage” and “verify stage.”

143. Additionally, as explained below in Section XII.B, Costa in view of Seo does not disclose or render obvious applying a “first bias voltage” to the gate terminal of a not programmed memory cell, and then applying a “second bias voltage ... smaller than the first bias voltage” to that gate terminal, as required by limitations [1.b] and [1.d]. Neither reference discloses that a second, different, bias voltage is

applied during a “verify stage.” Moreover, to the extent Costa discloses that unprogrammed memory cells may use a lower pass voltage (i.e., a purported bias voltage) to programmed memory cells, there is nothing to suggest that pass voltage being applied to an unprogrammed memory cell would be different during the “pre-verify stage” and “verify stage” of a verification operation.

A. Independent Claim 1: Costa in View of Seo Does Not Disclose or Render Obvious a “Pre-Verify Stage” (Limitations [1.a]-[1.b])

144. Costa in view of Seo does not disclose or render obvious a verification operation with a distinct “pre-verify stage,” as recited by limitations [1.a]-[1.b].

145. The Petition mistakenly argues that this subject matter is obvious from the combination of Costa in view of Seo. But Costa does not disclose or render obvious that a verification operation would be separated into a distinct “pre-verify stage” and “verify stage.” Seo does not address this deficiency. Indeed, Seo does not disclose or render obvious any type of verification operation, and does not disclose or render obvious that a verification operation would be separated into a distinct “pre-verify stage” and “verify stage.” The combination of Costa and Seo also fails to disclose or render obvious this subject matter, and Petitioner’s proposed combination fails to show that a POSITA would combine the purported teachings of Costa and Seo in order to yield verification operation that has distinct “pre-verify” and “verify” stages as required by the Challenged Claims.

146. Each of the Challenged Claims of the '957 Patent requires processing circuitry configured to: “**apply, in a pre-verify stage**, a first verify voltage on a gate terminal of a selected memory cell of the first memory cell string” (Element [1.a]); and “**apply, in the pre-verify stage**, a first bias voltage on a gate terminal of at least one memory cell of the first memory cell string that is not programmed” (Element [1.b]). These limitations are also required by dependent claims 2-6 by virtue of their dependency on claim 1 of the '957 Patent.

147. As described in Section VI, the claimed invention of the '957 Patent describes techniques for performing verification operations that improve over traditional systems, in part, by dividing the operation into a distinct **pre-verify stage** and **verify stage** with different sets of voltages being administered in each one. *See* '957 Patent, Fig. 6, 1:58-2:8, 6:37-49, 17:32-56. In doing so, “the gradient of the channel potential of the selected memory cell string can be reduced,” meaning that “HCI cannot be generated from the selected memory cell to the upper adjacent memory cell of the selected in the selected memory cell string.” '957 Patent, 12:63-13:4. But unlike the '957 Patent, Costa and Seo do not disclose or render obvious any kind of two-stage verification operation that contains both a **pre-verify stage** and a **verify stage**.

148. To the extent Costa describes verification operations, Costa does not disclose or render obvious that such an operation contains a separate “pre-verify

stage” and “verify stage.” Seo cannot address this deficiency, as Seo does not disclose or render obvious any kind of verify operation. Instead, Seo generally describes a memory device “read” operation that is partitioned into a “first time period t1” and a “second time period t2.” Seo [0011]. Petitioner’s proposed combination does not address these deficiencies, and fails to show that a POSITA would have been motivated to combine Costa and Seo’s teachings in such a way as to yield a verification operation that contains a separate “pre-verify stage” and “verify stage” as recited by independent claim 1.

149. As the Board correctly acknowledged, “Seo only describes time periods t1 and t2 with respect to performing a read operation that includes the steps selecting a page and memory string, setting the select transistor line voltage of the unselected, memory string and apply period thereof, applying voltage to the select lines of the unselected memory string, and applying the read voltage.” DI, 26-27 (citing Seo [0087]-[0090], Fig. 7). Even if a POSITA were somehow motivated to apply Seo’s teachings when executing a verification operation—such as the verification operation disclosed by Costa—it does not follow that Seo’s use of a distinct time period t1 would be converted into a “pre-verify stage” in the sense of the ’957 Patent.

150. For at least the reasons above, Costa in view of Seo fails to disclose or render obvious that distinct verify voltages and bias voltages are applied in a “pre-verify stage,” as recited by limitations [1.a]-[1.b].

151. For at least the same reasons, Costa in view of Seo also fail to disclose or render obvious the limitations of dependent claims 2-6.

B. Independent Claim 1: Costa in View of Seo Does Not Disclose or Render Obvious Applying “a First Bias Voltage” and “a Second Bias Voltage” on the Gate Terminal of a Not Programmed Memory Cell “Wherein the Second Bias Voltage Is Smaller than the First Bias Voltage” (Limitations [1.b], [1.d])

152. Costa in view of Seo does not disclose or render obvious applying “a first bias voltage” and “a second bias voltage” on the gate terminal of a not programmed memory cell “wherein the second bias voltage is smaller than the first bias voltage,” as recited by limitations [1.b] and [1.d].

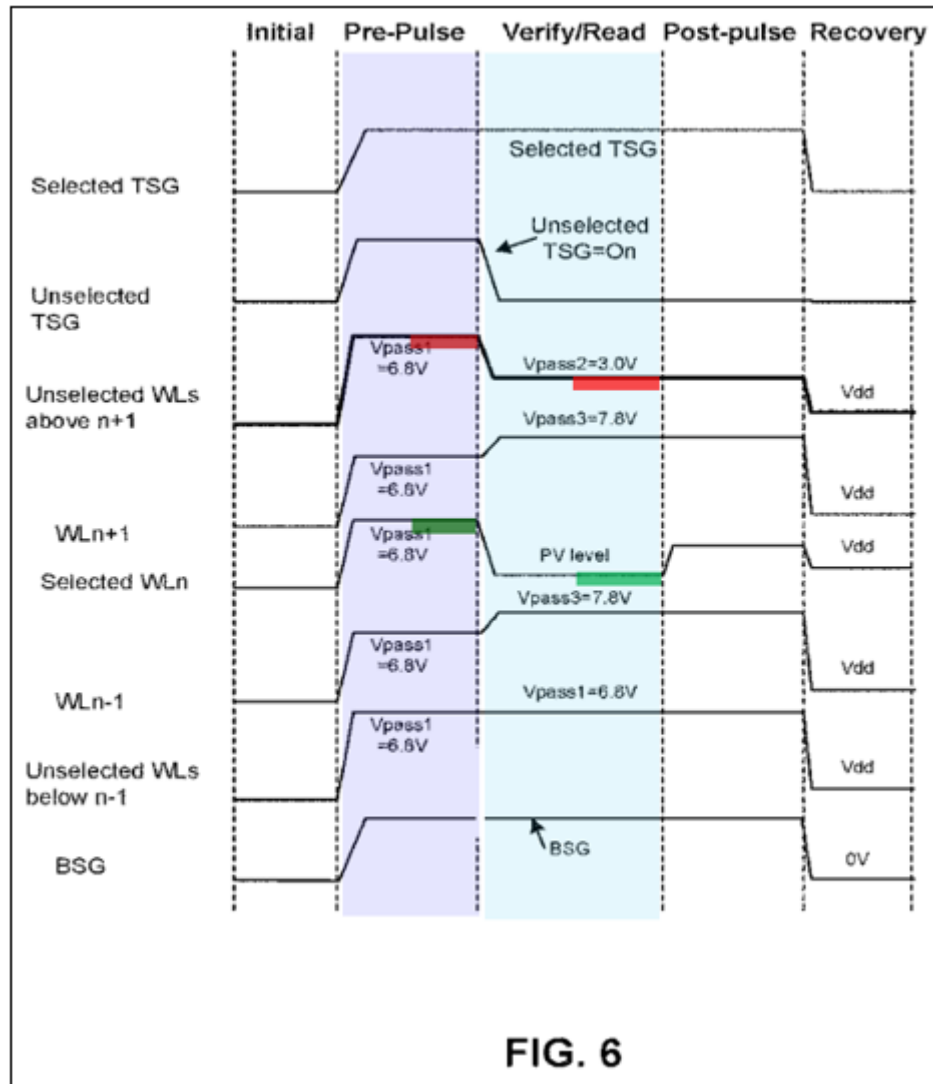
153. Petitioner and Dr. Liu have not demonstrated that the voltages described in Costa and Seo are actually applied to the gate terminal of the memory cell, as compared to target voltages applied to word line layers. Furthermore, both Costa and Seo fail to disclose or render obvious applying different bias voltages to an unprogrammed memory cell in a pre-verify stage and a verify stage. Petitioner and Dr. Liu attempt to address this deficiency by incorrectly asserting a POSITA would have been motivated to selectively apply Costa’s teachings to just a pre-verify stage (and not a verify stage). *See* Pet 103-112. But that argument contradicts Costa’s own disclosure, and the basic principles behind how NAND memory strings operate. Contrary to what Petitioner and Dr. Liu suggest, a POSITA would not have been motivated to combine Costa and Seo together in the manner proposed in the Petition.

Rather, the proposed combination appears to be little more than an attempt to reconstruct the features of the '957 Patent through a mix of strained rationalizations and hindsight.

154. Each of the Challenged Claims of the '957 Patent requires processing circuitry configured to: “**apply, in the pre-verify stage, a first bias voltage on a gate terminal of at least one memory cell of the first memory cell string that is not programmed**” (Element [1.b]); and “**apply, in the verify stage, a second bias voltage on the gate terminal of the at least one memory cell of the first memory cell string that is not programmed, wherein the second bias voltage is smaller than the first bias voltage**” (Element [1.d]). These limitations are also required by dependent claims 2-6 by virtue of their dependency on claim 1 of the '957 Patent.

155. As described in Section VI, the '957 Patent differentiates between the voltages applied to word line layers in a pre-pulse stage, and the resulting bias voltages that are applied on the gate terminals of the corresponding memory cells, which develop over time as a result. *See, e.g., '957 Patent, 11:68-12:9, 12:10-27.* Within that framework, the '957 Patent describes an approach for performing verification operations that improves over traditional systems, in part, by applying a **first bias voltage** that fully develops on a gate terminal of an unprogrammed memory cell in a **pre-verify stage** before applying a **second bias voltage** that is less

than the first bias voltage in a subsequent **verify stage**. '957 Patent, 1:58-2:8, 6:37-49, 17:32-56, Fig. 6.

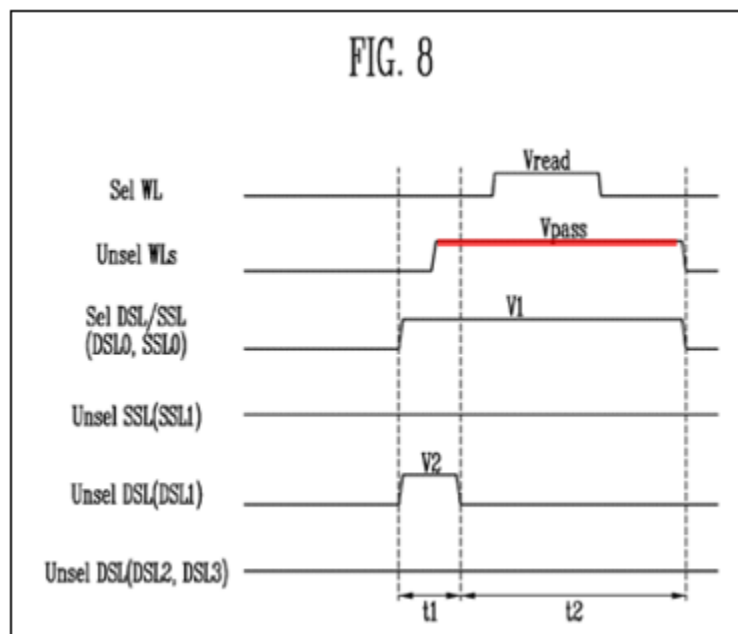


In contrast with the '957 Patent, both Costa and Seo fail to disclose or otherwise render obvious that the bias voltage being administered to a gate terminal of an unprogrammed memory cell changes over time (e.g., as to result in a distinct “first bias voltage” and “second bias voltage” during different stages of a verification

operation), and the proposed combination similarly fails to disclose or render obvious this subject matter.

156. Regarding Costa, it fails to disclose or otherwise render obvious that a verification operation is divided into a separate “pre-verify stage” and “verify stage,” or that distinct voltage levels would be applied during a “pre-verify stage” and a “verify stage” as recited by claim 1. Although Costa teaches that a lower “pass voltage” can be utilized for *unprogrammed memory cells* as compared to the default pass voltage used for *programmed memory cells*, Costa does not teach or otherwise suggest that different “pass voltage” will be applied to any given memory cell in *different stages of a verification operation*. See Costa [0121]-[0122], [0147]. As described by Costa, programming a memory cell raises the threshold voltage of the memory cell (see Costa [0082]), but because unprogrammed memory cells are already known to be in an erased state, a “lower read pass voltage VreadL can be used while still ensuring that these memory cells operate as pass gates” (Costa [0122]). But the fact that Costa employs different pass voltages for programmed and unprogrammed memory cells does not imply the use of a distinct “pre-verify stage” and “verify stage,” nor does it suggest that different voltage levels could be used on a memory cell during a “pre-verify stage” and a “verify stage.” Rather, Costa teaches that the “pass voltage” administered to any particular memory cell is a fixed value.

157. As for Seo, it similarly fails to disclose or otherwise render obvious that distinct voltage levels are applied to the gate terminal of a memory cell during a “pre-verify stage” and a “verify stage,” as recited by claim 1. Seo describes a “read” operation that can be partitioned “time period t1” and “time period t2.” *See* Seo, [0087]-[0090]. But Seo does not describe different bias voltages being used in each time period. Rather, Seo discloses that a “pass voltage **V_{pass}** may be administered to unselected word lines” in a part of time period t1, as well as time period t2.” Seo, [0087]-[0090], Fig. 8.



158. Petitioner and Dr. Liu apparently recognize that Seo does not disclose different values of “**V_{pass}**” being used in time period t1 and time period t2, and that Seo fails to disclose or render obvious two different bias voltages being applied to unprogrammed memory cells. *See* Pet. 26-27, 103. To address this deficiency, the

Petition tries to equate Seo's use of "**Vpass**" in time period t1 as the claimed "first bias voltage," and incorrectly argues that it would have been obvious in view of Costa for a lower value of **Vpass** to be applied only during time period t2, thus producing a smaller "second bias voltage." *See* Pet. 26-27, 103-126.

159. Petitioner and Dr. Liu fail to show that a POSITA would have been motivated to selectively apply Costa's purported teaching (i.e., that a lower **Vpass** value may be used on unprogrammed word lines) in only time period t2, without also applying those purported teachings in time period t1. The Petition wrongly asserts that Costa's disclosure of using "low Vpass voltage[s]" would be applicable only in time period t2, while ignoring the fact that Costa does not teach selectively applying lower pass voltages in different time periods. *See* Pet. 112, 126-129. Moreover, the proposed combination seemingly ignores Costa's own teachings. To the extent it is advantageous to use lower pass voltages on certain unprogrammed memory cells, as purportedly taught by Costa (*see* Costa, [0112]), that supposed teaching would be equally applicable in both time period t1 and time period t2. Petitioner and Dr Liu have failed to show that a POSITA would have been motivated to lower the Vpass voltage used in only one of the two different time periods.

160. The Petition tries to defend its proffered combination with the erroneous and unfounded argument that Seo necessitates "high Vpass voltages" on every unselected memory cell in the first time period. Pet. 128 (citing Liu ¶308). To

begin within, Seo never states that a “high Vpass voltage” needs to be administered. Furthermore, neither Petition nor Dr. Liu explained why a single value of Vpass needs to be used on every memory cell irrespective of whether they are programmed or unprogrammed (i.e., why a POSITA would disregard Costa’s purported teachings, thus applying a larger Vpass voltage than necessary to unprogrammed memory cells), or why Costa’s purported teachings would be somehow inapplicable during that initial time period. The only support provided is Dr. Liu assertion that “a POSITA would have understood that in Seo’s bias scheme” a “full Vpass voltage” would be needed in the first time period because “a Vpass voltage on unselected memory cells on the drain side of the selected memory cell needs to be high enough to account and compensate” for the voltages building on the “source of [the] transistor” in a pre-conditioning period. Liu ¶308. Notably, Dr. Liu does not cite any part of Seo’s disclosure for this assertion, and even if Dr. Liu’s contention was accepted on its face, Costa’s purported teachings (i.e., that you can use a lower value of Vread on unprogrammed memory cells because they are known to have lower threshold voltages) *would still be equally applicable in both time periods*—including the first time period t1. Neither Costa nor Seo provides a rationale for applying different values Vpass in different time periods, and the hindsight-based arguments presented by Petitioner and Dr. Liu fail to show that a POSITA would have found it obvious to modify the pass voltages applied during only the second

time period (i.e., so as to create a “second bias voltage” that is smaller than a “first bias voltage”).

161. Therefore, contrary to what Petitioner and Dr. Liu assert, a POSITA would not have been motivated to selectively apply Costa’s teachings in the manner proposed in the Petition. Petitioner’s and Dr. Liu’s argument that Costa’s teachings would be applied only during one stage of a two-stage operation is unfounded, has no support in either Costa or Seo, and appears to rely on hindsight rationalizations to reconstruct the features of the ’957 Patent after the fact.

162. Furthermore, unlike the ’957 Patent, Costa and Seo do not differentiate between the target voltages applied through word lines, and the voltages applied on the gate terminals of the corresponding memory cells that develop over time in response. *See, e.g.*, ’957 Patent, 11:68-12:9, 12:10-27. To the extent Costa and Seo disclose that certain voltages are being applied to selected and unselected word lines, they fail to teach or otherwise render obvious that those same voltages would be applied on the gate terminals of the corresponding memory cells. Petitioner and Dr. Liu have also failed to provide any explanation or arguments as to why the voltages disclosed by Costa and Seo (i.e., target voltages) as applied to word lines would have obviously been the same as the voltages applied to the gate terminals of corresponding memory cells within the memory string.

163. For at least the reasons above, Costa in view of Seo fails to disclose or render obvious processing circuitry arranged to “apply ... a first bias voltage on a gate terminal of at least one memory cell of the first memory cell string that is not programmed,” and “a second bias voltage on the gate terminal of the at least one memory cell of the first memory cell string that is not programmed, wherein the second bias voltage is smaller than the first bias voltage” as recited by limitations [1.b] and [1.d]. Moreover, the arguments presented in the Petition are inconsistent with Costa’s and Seo’s own teachings, and attempt to reconstruct the features of the ’957 Patent by selectively apply Costa’s teachings without a proper motivation to do so.

164. For at least the same reasons, Costa in view of Seo also fail to disclose or render obvious the limitations of dependent claims 2-6.

XIII. CONCLUSION

165. For at least the reasons discussed above, the Challenged Claims of the ’957 Patent are not anticipated or obvious.

166. Furthermore, as discussed in Section III above, I have used my background and experience in forming my opinions that the Challenged Claims are not anticipated or obvious over the asserted prior art.

167. This declaration represents my opinions that I have formed to date on the specific issues for which I have been asked to opine and based on the material

currently available to me. I understand that the declaration will be filed as evidence in an *inter partes* review proceeding before the Board. I acknowledge that I may be subject to cross examination in the case and that cross examination will take place within the United States. If cross examination is required of me, I will appear for cross examination within the United States during the time allotted for cross examination. I reserve the right to supplement this declaration to address any new information offered by Petitioner or provided by the Board. Also, I reserve the right to supplement this declaration insofar as Petitioner is permitted to supplement the record with any additional opinions or arguments.

168. I hereby declare that all statements made herein of my own knowledge are true and all statements made herein on information and belief were and are believed by me to be true, and that all statements herein were and are made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code and that any such willful false statements may jeopardize the results of these proceedings.

APPENDIX A

Steven A. Przybylski

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Professional Experience

2003 - Present **President, Verdande Group, Inc**

An inventor, registered patent agent, strong communicator and seasoned technical expert, I provide intellectual property services to a diverse set of clients across the digital electronics spectrum. I provide patent, trade secret, and contract dispute litigation support services, and have extensive experience as a testifying and non-testifying expert in matters before district courts, the PTAB, the ITC, and foreign jurisdictions. I have testified by expert report, deposition, and live testimony on matters of claim construction, infringement, and invalidity, and have assisted in evaluations of potential damages and monetization strategies. With strong written and verbal skills, I provide tutorials to those of both technical and non-technical backgrounds, including judges and attorneys. In addition, I offer pre- and post-transaction portfolio evaluations and due diligence analyses.

I have been retained for these services with regard to:

Computer Systems

Processor design
Processor architecture
Multiprocessing
Graphics systems
Graphics/CUDA processors
Cache memories
Memory systems
Memory modules
Floating point computation
Operating systems
I/O systems
System boot issues

Consumer Electronics

Infotainment systems
Video encoding and decoding
Medical equipment
Embedded systems
Portable electronic systems
User interface design
Wired and wireless networking
Power/energy management
Standards development
Display interconnects
Integrated memories
Digital signal processing
Cloud-based content navigation
and serving

Semiconductors

DRAMs
Flash
SRAMs
Other non-volatile memories
Memory controllers
High-speed interconnects
Signal integrity
2D, 2.5D and 3D packaging
Error detection and correction
Clock distribution techniques
Semiconductor processing
IC and system testing
Computer aided design
FPGAs

2000 – 2003 **Manager, SSM Technologies, LLC.**

I managed, developed and sold a significant patent portfolio relating to DRAMs. Recognizing the intrinsic value of a long-neglected portfolio, I negotiated control of the portfolio and developed a new patent prosecution strategy. I oversaw and participated in the implementation of this strategy, culminating in the issue of a new set of broad method and apparatus claims. I then worked to monetarize the portfolio and to maximize return to the inventors and SSM's investors by analyzing the sell/license decision and guiding the stakeholders through the decision-making process. I gathered relevant documentation and analyses, approached likely purchasers, presented interested parties with the collected materials, actively sold the offensive and defensive utility of the portfolio, and orchestrated an auction-style final sales process.

1991 – 2000 **President and Principal Consultant, Verdande Group, Inc**

I have consulted on product strategy, comparative technical analysis, and system-level design in the areas of DRAMs, Flash, SRAMs and other semiconductor memories, computer systems and CPU architecture, and uni- and multi-processor memory hierarchy design. Technical engagements have included serving as memory system architect for Flash and DRAM memory devices and systems. In addition, I offered: general business planning and analysis services to computer and semiconductor companies; intellectual property management, including portfolio evaluation, development and brokering, and litigation support services to IP holders and legal firms; and due-diligence analyses to venture capitalists and securities firms.

My writing and analysis encompasses an extensive range of topics for trade magazines, conferences, and academic journals. As one of the leading independent analysts of the semiconductor memory industry, I wrote (1994) and substantially revised (1996) an 850-page research report entitled *New DRAM Technologies: A Comprehensive Analysis of the New Architectures*, available from the publishers of *The Microprocessor Report*. I have also taught and presented tutorials to both technical and non-technical audiences on subjects including semiconductor memory architecture, memory hierarchy design, and computer systems and CPU architecture. In particular, I have presented over 50 full- and partial-day seminars on these topics to over 2,500 managers, engineers, marketers, and analysts. I have also served on the advisory boards of high-technology start-ups, advising on processor, DRAM and Flash memory trends and general business opportunities.

- 1989 - 1991 **Chief Scientist and Systems Architect, MIPS Computer Systems.**
I played a variety of roles within MIPS, including assistant to the Senior Vice President of Engineering, technical lead for a group of designers that investigated the technical and economic feasibility of developing a companion chip to the R3000 CPU and R3010 FPU, troubleshooter within the High-End Systems Group responsible for taking on any short or long term task that was in need of additional manpower, chief scientist for the group in charge of planning and investigating options for future high-end systems, systems architect for both a new R4000 based symmetrical multi-processor and a low-cost desk-top machine.
- 1990 - 1991 **Consulting Assistant Professor, Dept. of Elect. Eng., Stanford University.**
I designed and taught an advanced graduate level course on cache and memory hierarchy design and supervised the students' research activities. Two groups of students continued their research and ultimately published their efforts under my direction.
- 1989 - 1989 **Postdoctoral Scholar, Department of Electrical Engineering, Stanford University.**
As a postdoctoral scholar, I continued my dissertation research into the analysis of cache behaviour and performance-optimal memory hierarchy design.
- 1984 - 1985 **Computer Architect and Systems Designer, MIPS Computer Systems.**
My main contribution during MIPS' first year was the specification of the architecture and micro-organization of the R2000 VLSI RISC CPU, including the CPU interface and the cache subsystem. I was integrally involved in the implementation of both the CPU and system-level design. My most important role was that of liaison between the VLSI, board-level hardware, compiler and operating system teams.
- 1981 - 1988 **Research Assistant, Department of Electrical Engineering, Stanford University.**
I was a key participant in the MIPS VLSI CPU design team, involved in the design, debugging and testing of the IC design. I also oversaw the development of a prototype CPU board, and subsequently aided in the architectural specification of the MIPS-X VLSI CPU. My dissertation research used analytical and empirical techniques to examine memory hierarchy design from the perspective of optimizing system level performance.

Education

Haas School of Business, University of California at Berkeley, M.B.A. (2000).

Coursework and final project included a combined emphasis on business strategy and financial analysis.

Stanford University, M.S.E.E. (1982), Ph.D. (1988).

Research areas: Computer systems design and VLSI integrated circuit design. Concentrated areas of study spanned the breadth of both electrical engineering and software systems. Topics of extensive coursework included digital systems design, computer architecture, semiconductor devices, error correction codes, control theory, and system software — including user interface design, operating systems, compilers, and I/O systems. Doctoral dissertation title: Performance-Directed Memory Hierarchy Design.

University of Toronto, B.A.Sc. with Honours (1980).

My unique, specially approved course of study within the Engineering Science Programme combined the computer science and electrical engineering degree programs. This provided a broad and deep background in both areas. Coursework and undergraduate thesis covered digital systems design, computer systems, control theory, network analysis, analog circuit design, semiconductor physics, human-computer interfaces, operating systems, compilers, database design, and AI.

Honors and Publications

Awards

Most Influential Paper Award, ACM/IEEE International Symposium on Computer Architecture, 1989, with Mark Horowitz and John Hennessy.

Micro Test-of-Time Award, for one of the ten most influential papers of the first 25 years of the IEEE Micro Symposium, with John Hennessy, Norman Jouppi, Christopher Rowen, Thomas Gross, Forest Baskett, and John Gill. 1994.

Books

S. Przybylski, *New DRAM Technologies*, MicroDesign Resources, 1996, 1994.

S. Przybylski. *Cache and Memory Hierarchy Design: A Performance-Directed Approach*, Morgan Kaufmann, 1990.

J. Hennessy, S. Przybylski. VLSI Processor Design Methodology. Chapter I in *VLSI Electronics, Microstructure Science*, Vol. 14, Einspruch, N. ed., Academic Press, 1986.

Journal Articles

T. Wada, et al. An Analytical Access Time Model For On-Chip Cache Memories, *Journal of Solid-State Circuits*, Vol. 27, No. 8, August 1992.

T. Gross, et al. Measurement and Evaluation of the MIPS Architecture and Processor. *ACM Transactions on Computer Systems*, Vol. 6, No. 3, August 1988.

M. Horowitz, et al. MIPS-X: A 20 MIPS Peak, 32-bit Microprocessor with On-Chip Cache. *Journal of Solid-State Circuits*, Vol. 22, No. 5, October 1987.

C. Rowen, et al. RISC VLSI Design for System-Level Performance. *VLSI Systems Design*, Vol. 7, No. 3, March 1986.

S. Przybylski, et al. The Organization and VLSI Implementation of MIPS. *Journal of VLSI and Computer Systems*, Vol. 1, No. 2, December 1984.

Other Articles

T. Gross, N. Jouppi, J. Hennessy, S. Przybylski, C. Rowen. A Retrospective on "MIPS: A Microprocessor Architecture", *IEEE Micro*, Vol. 36, No. 4, July/August, 2016.

R. Schuetz, H.J. Oh, J.-K. Kim, H.-B. Pyeon, S. Przybylski, P. Gillingham. HyperLink NAND Flash Architecture for Mass Storage Applications, 22nd IEEE Nonvolatile Semiconductor Memory Workshop (NVSMW), August 2007.

S. Przybylski, Intel's RDRAM Strategy a Sure Winner, *Microprocessor Report*, Vol. 11, No. 5, April 21, 1997

S. Przybylski, Intel's Gambles on a Sure Thing, *Electronic Engineering Times*, No. 947, March 31, 1997.

S. Przybylski, Will 1997 be the year of the 64-Mbit DRAM?, *Computer Design*, March 1997.

S. Przybylski, Combining DRAM and System Architecture, *OEM Magazine*, Vol. 4, No. 28, June, 1996.

S. Przybylski, SDRAMs Ready to Enter Mainstream, *Microprocessor Report*, Vol. 10, No. 6, May 6, 1996.

- S. Przybylski, MoSys Reveals MDRAM Architecture, *Microprocessor Report*, Vol. 9, No. 17, December 25, 1995.
- S. Przybylski, New DRAMs Improve Bandwidth, *Microprocessor Report*, Vol. 7, No. 2, February 15, 1993.
- S. Przybylski, DRAMs for New Memory Systems *Microprocessor Report*, Vol. 7, No. 3, March 8, 1993.
- S. Przybylski, DRAMs for New Memory Systems, *Microprocessor Report*, Vol. 7, No. 4, March 29, 1993.
- S. Przybylski. The Performance Impact of Block Sizes and Fetch Strategies. 17th Annual International Symposium on Computer Architecture, May 1990.
- S. Przybylski, J. Hennessy, M. Horowitz. Characteristics of Performance-Optimal Multi-Level Cache Hierarchies. 16th Annual International Symposium on Computer Architecture, June 1989.
- S. Przybylski, M. Horowitz, J. Hennessy. Performance Tradeoffs in Cache Design. 15th Annual International Symposium on Computer Architecture. June 1988.
- M. Horowitz, et al. A 12 MIPS 32b Microprocessor with On-Chip Cache. International Solid State Circuits Conference, February 1987.
- J. Moussouris, et al. A RISC Microprocessor with Integral MMU and Cache Interface. International Conference on Computer Design (ICCD), October 1986.
- J. Moussouris, et al. A CMOS RISC Processor with Integrated System Functions. Proceedings of COMPCON, Spring 1986.
- C. Rowen, et al. A Pipelined 32b nMOS Microprocessor. International Solid State Circuits Conference, February 1984.
- S. Przybylski. The Design Verification and Testing of MIPS. MIT Conference on Advanced Research in VLSI, January 1984.
- J. Hennessy, et al. Performance Issues in VLSI Processor Design. International Conference on Computer Design (ICCD), November 1983.
- J. Hennessy, et al. Design of a High Performance VLSI Processor. Third Caltech Conference on VLSI, March 1983.
- J. Hennessy, et al. MIPS: A Microprocessor Architecture. MICRO-15, October 1982.

Technical Reports

- S. Przybylski. *Performance-Directed Memory Hierarchy Design*. Technical Report No. CSL-TR-88-366, Stanford University, September 1988.
- S. Przybylski. *The Implementation of MIPS*. Internal Technical Report, Computer Systems Laboratory, Stanford University, August 1984.
- J. Gill, et al. *Summary of MIPS Instruction*. CSL Technical Note No. 237, Computer Systems Laboratory, Stanford University, March 1983.
- J. Hennessy, et al. *Hardware/Software Tradeoffs for Increased Performance*. CSL Technical Report No. 228, Computer Systems Laboratory, Stanford University, February 1983.

Seminars, Tutorial, Session Chairs

- PC System Architecture Trends, Panel member, 1999 Microprocessor Forum, San Jose, October 1999.
- An Introduction to Semiconductor Memories, A Verdande Group presentation in cooperation with Citibank Inc, Taipei, Taiwan ROC, June 1998.
- Embedded DRAMs: Today and Toward System-Level Integration, Half-day seminar. Presented more than 10 times to corporations between September 1997 and October 1999
- The New DRAMs for Main Memory and Graphics, Full day Seminar, Verdande Group Seminar Series, Portland, Austin, San Jose, and Boston, September 1997.

Embedded DRAMs: Today and Toward System-Level Integration, Half-day seminar, Verdande Group Seminar Series, Portland, Austin, San Jose, and Boston, September 1997.

Sorting Out the New DRAMs, Half-Day Tutorial, Hot Chips IX, August 1997.

Embedded DRAMs: Today and Toward System-Level Integration, Half-day seminar, Presented at 24th Annual International Symposium on Computer Architecture, May 1997.

The New DRAMs For Main Memory and Graphics, Full day tutorial, 1997 PC Tech Forum, May 1997.

The New DRAM Architectures, DRAM Tutorial, 1996 ISSCC, February 1997.

Selecting the Best Memory Technology for PCs and Graphics, Full day tutorial, 1996 PC Tech Forum, May 1996.

The Changing DRAM and VRAM Marketplace, Full day tutorial, Presented more than 20 times to corporations between September 1995 and October 1999.

The Changing DRAM and VRAM Marketplace, Full day tutorial, Sponsored by Nikkei Microdevices, Tokyo, Japan, March 1996.

The Changing DRAM and VRAM Marketplace, Full day tutorial, 1995 Microprocessor Forum, October 1995.

Cache and Main Memory Options. Lecture. WinHEC, March 1995.

New Graphics Memories. Lecture. WinHEC, March 1995.

Emerging DRAM Architectures. Lecture. WinHEC, February 1994.

New DRAM Organizations. Session chair. Proceedings of COMPCON, Spring 1994.

Computer architecture and organization. Half-day tutorial. OCATE/Oregon State University, August 18, 1993.

DRAM Choices for the 1990s. Half-day tutorial. Hot Chips V, August 1993.

Computer Architecture. Full day tutorial with Normal Jouppi and Mark Horowitz. International Solid State Circuits Conference, February 1993.

Recent Trends in Processor Design, Reclimbing the Complexity Curve. Week-long course with Mark Horowitz and Mike Smith. Western Institute of Computer Science/Stanford University, August 1992 and August 1993.

Tracking the Processor-Memory Bandwidth Problem. Session chair, Microprocessor Forum, October 1992.

Patents

H. Pyeon, H. Oh, J.-K. Kim, S. Przybylski, *ID generation apparatus and method for serially interconnected devices*, Patent No. 8,984,249, March 17, 2015.

S. Przybylski, *Ring-of-clusters network topologies*, Patent No. 8,902,910, December 2, 2014.

S. Przybylski, R. Schuetz, H. Oh, H.B.Pyeon, *System having one or more memory devices*, Patent No. 8,812,768, August 19, 2014.

S. Przybylski, *Error detection and correction codes for channels and memories with incomplete error characteristics*, Patent 8,806,305, August 12, 2014.

J.-K. Kim, H. Oh, H.B. Pyeon, S. Przybylski. *Scalable Memory System*. Patent No. 8,671,252, March 11, 2014.

S. Przybylski, *Ring-of-clusters network topologies*, Patent No. 8,594,110, November 26, 2013.

S. Przybylski, *Error detection and correction codes for channels and memories with incomplete error characteristics*, Patent No. 8,429,495, April 23, 2013.

J.-K. Kim, H. Oh, H. Pyeon, S. Przybylski. *Scalable Memory System*. Patent No. 8,407,395, March 26, 2013.

L. Crudele, J. Moussouris, S. Przybylski. *System Having An Address Generating Unit and a Log Comparator Packaged as an Integrated Circuit Separate From Cache Log Memory and Cache Data Memory*. Patent No. 5,113,506, May 12, 1992.

L. Crudele, J. Moussouris, S. Przybylski. *CPU Chip Having Tag Comparator and Address Translation Unit on Chip and Connected to Off-Chip Cache and Main Memories*. Patent No. 4,953,073, August 28, 1990.

C. Hansen, S. Przybylski, T. Riordan, L. Weber. *Dual Byte Order Computer Architecture*. Patent No. 4,959,779, September 25, 1990.

Foreign counterparts of the above.

Additional Information

Registered US Patent Agent, 1997 - present

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