

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,
Patent Owner

Case No.: IPR2024-00792
U.S. Patent No. 11,468,957

PETITIONER'S REPLY BRIEF

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LISTING OF EXHIBITS

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1001	U.S. Patent No. 11,468,957 B2 to Lee et al.
1002	File History of U.S. Patent No. 11,468,957 to Lee et al.
1003	Declaration of David Kuan-Yu Liu, Ph.D.
1004	<i>Curriculum Vitae</i> of David Kuan-Yu Liu, Ph.D.
1005	Chinese Patent Publ. No. 109065091 A to Hongtao Liu et al. (certified translation and original) (“Hongtao”)
1006	U.S. Patent Publ. No. 2019/0198117 A1 to Yu et al. (“Yu”)
1007	U.S. Patent Publ. No. 2021/0082505 A1 to Suzuki (“Suzuki”)
1008	U.S. Patent Publ. No. 2018/0012667 A1 to Costa (“Costa”)
1009	U.S. Patent Publ. No. 2021/0027848 A1 to Seo (“Seo”)
1010	Minute Order, Dkt. No. 42, dated February 22, 2024 in <i>Yangtze Memory Technologies Company, Ltd. V. Micron Technology, Inc. and Micron Consumer Products Group, LLC</i> , Case No. 3:23-cv-05792-RFL
1011	Combined Civil and Criminal Federal Court Management Statistics (December 31, 2023), available at https://www.uscourts.gov/sites/default/files/data_tables/fcms_na_distcomparison1231.2023.pdf
1012	Docket from <i>Yangtze Memory Technologies Company, Ltd. V. Micron Technology, Inc. and Micron Consumer Products Group, LLC</i> , Case No. 3:23-cv-05792-RFL
1013	U.S. Patent No. 9,589,978 B1 to Yip
1014	Aritome, “NAND Flash Memory Technologies” (2016)
1015	Silvagni, “3D NAND Flash Based on Planar Cells,” <i>Computers</i> 2017
1016	U.S. Patent Publ. No. 2020/0168276 A1 to Yang

Exhibit	Description
1017	U.S. Patent No. 9,620,233 B1 to Dong et al.
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1019	U.S Patent No. 9,361,993 B1 to Chen et al.
1020	U.S Patent No. 10,276,251 B1 to Lobana et al.
1021	U.S. Patent Publ. No. 2019/0348122 A1 to Ko et al.
1022	U.S. Patent Publ. No. 2013/0077404 A1 to Nawata et al.
1023	U.S Patent No. 10,121,529 B2 to Lee
1024	U.S. Patent Publ. No. 2016/0293271 A1 to Won et al.
1025	U.S. Patent No. 11,600,342 to Chen et al.
1026	Declaration of Jared Bobrow in Support of Petitioner’s Motion for Admission <i>Pro Hac Vice</i>
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1030	U.S. Patent No. 10,861,537 to Lien et al.
1031	Transcript of April 17, 2025 Deposition of Dr. Steven Przybylski

I. INTRODUCTION

None of Patent Owner's ("PO's") arguments salvage the '957 patent.

PO contends that Grounds 1–2 do not render claims 5–6 unpatentable because the references disclose top/bottom bias voltages lacking a single voltage level in both pre-verify and verify stages, as PO's proposed construction requires. PO's construction, however, violates multiple claim-construction canons: it attempts to rewrite the claims from "apply[ing] a [top/bottom] bias **voltage**" to "apply[ing] a **single** [top/bottom] bias **voltage level**," and it contradicts the '957 patent's disclosure that these voltages have multiple levels.¹ Further, applying PO's construction to the positive-voltage claim limitations having the same structure also shows that the construction invites legal error. Under the correct construction, Grounds 1–2 render claims 5–6 obvious.

PO alleges that Grounds 1 and 3 do not show voltages applied on gate terminals because the references show piecewise-linear waveforms (allegedly indicating word-line voltages) rather than curved waveforms (allegedly indicating

¹ All emphases and color annotations are added unless noted otherwise.

gate voltages).² PO's argument creates a distinction between gates and word lines that fails on multiple fronts. To start, PO ignores that Hongtao and Costa disclose applying gate voltages, which alone is dispositive. PO further ignores that the '957 patent and prior art refer to the two interchangeably. The '957 patent and the prior art are directed to voltages at gate terminals (which they equate with the overall word-line layers), because it is the gate voltages that effectuate memory-cell operations. PO's distinction leaves the '957 patent without a single claimed embodiment. Further, PO's expert testimony reveals that PO's distinction would create untold complications for real-world devices and would render the '957 patent invalid for inadequate written description and enablement.

PO argues that Grounds 1 and 3 do not render obvious verify operations because each relies on a reference disclosing exemplary read operations. This argument fails, because the '957 patent and the prior art treat verify and read as virtually identical. And for good reason: there is no reasonable dispute that verify operations are read operations with different read (verify) voltages. Nonetheless, PO uses this false distinction to argue that Ground 1's pre-read operation is not a

² The '957 patent uses "gate" and "gate terminal" synonymously. Ex. 1001, 9:35–36, 9:42. This reply does the same and refers to "voltage applied on a gate terminal" as "gate voltage."

pre-verify operation and, for Ground 3, that one would not prepend a pre-read phase to another reference's verify operation. This makes little sense, because these operations are effectively identical. PO simply ignores evidence demonstrating that a POSITA would have understood verify operations to be read operations after program operations.

PO's expert declaration should be given no weight. Despite clear PTAB guidance on this very issue, his declaration simply parrots PO's response, adding little substance to disputed issues. Worse, his deposition confirms that his opinions are unreliable and contradicted by the record.

II. CLAIM CONSTRUCTION

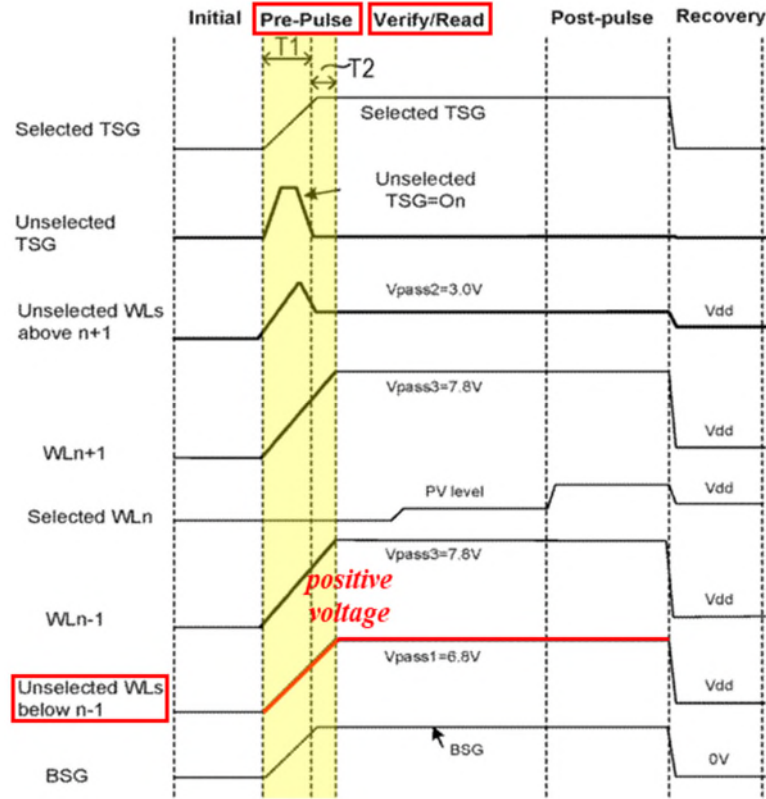
A. “Apply a [Top/Bottom] Bias Voltage ... in the Pre-Verify Stage and the Verify Stage”

PO incorrectly construes the top/bottom-bias-voltage limitations to require “a *single* voltage *level* be applied in both the pre-verify stage and the verify stage.” POR, 13 (emphasis altered). PO's construction violates multiple claim-construction canons and contradicts its “voltage-on-the-gate-terminal” argument. Ex. 1027 (Dr. Liu's Reply Declaration, “Liu2”) ¶ 8.

First, PO's construction impermissibly narrows “apply[ing] a [top/bottom] bias *voltage*” to “apply[ing] a *single* [top/bottom] bias *voltage level*.” PO cites no legal basis to rewrite the claims. What's more, the '957 specification discloses that “*the bottom bias voltage*” and “*the top bias voltage*” can be increased from an initial

level to a target level “(e.g., 5 volts)” during the pre-verify stage. Ex. 1001, 13:43–53; *id.*, 2:56–61, 4:4–9, Fig. 7. Thus, it does not restrict a “voltage” to a particular numerical value; a “voltage” can take on multiple levels. Liu2 ¶ 9. Claim constructions must be consistent with the specification’s disclosure. *Thorner v. Sony Comput. Ent. Am. LLC*, 669 F.3d 1362, 1369 (Fed. Cir. 2012) (reversing construction that is inconsistent with patent’s disclosure). PO’s construction violates this rule.

Second, the Petition undisputably demonstrates that other claim limitations—which have an identical structure as these limitations—**cannot** require a single voltage level across the two stages, because the patent’s embodiment shows the opposite. Pet. at 66–67. For example, the “positive voltage” of claim 5, as shown in Figure 7, does not reach a single level until the verify stage:

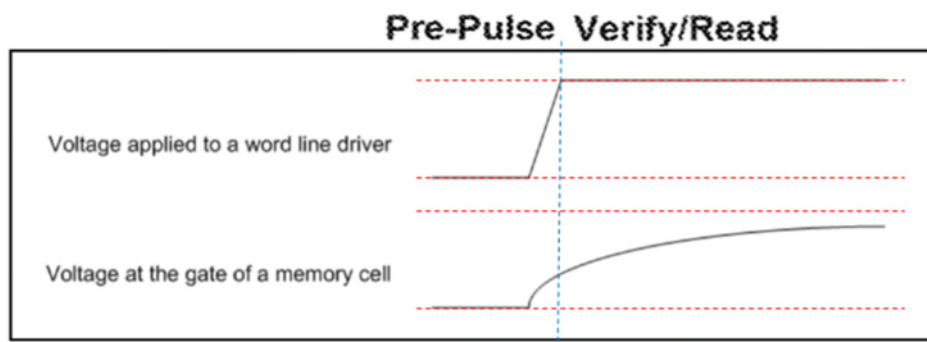


Ex. 1001, Fig. 7. Thus, a single positive-voltage level does not exist in both stages, and PO's construction reads out the very embodiment on which it relies. POR, 16; Liu2 ¶¶ 10–12.

Given their identical structure, the construed terms presumptively have the same meaning as the positive-voltage limitation. *Fin Control Sys. Pty, Ltd. v. OAM, Inc.*, 265 F.3d 1311, 1318 (Fed. Cir. 2001). Because the positive-voltage limitation **requires** more than one voltage level across both stages, so do the construed terms.

Third, PO's incorrect "voltage-on-the-gate-terminal" argument contradicts its construction. That argument alleges that gate-terminal voltages are delayed relative to word-line voltages shown in straight lines. POR, 36–37. But, as just shown,

Figure 7’s straight-line positive voltage does not rise to its target level until the verify stage. With PO’s alleged delay, the curved gate voltage “will be significantly delayed relative to the transition in the target voltage.” Ex. 1031, 204:3–18 (discussing the same figure in Ex. 2003, *see id.*, 199:6–10):



Liu2 ¶¶ 13–14 (PO’s figure annotated to show a gate voltage rising slowly under PO’s theory). Consequently, the positive voltage of Figure 7—PO’s chosen claim-construction embodiment—cannot rise to its target level (dotted red lines above the waveforms)—if at all—until long after the pre-verify stage. Thus, it becomes even more apparent that Figure 7 cannot satisfy PO’s claim construction. PO’s claim construction would read out PO’s chosen embodiment of the claim terms. This “is rarely, if ever, correct.” *See Broadcom Corp. v. Emulex Corp.*, 732 F.3d 1325, 1333 (Fed. Cir. 2013).

Lastly, PO mistakenly relies on case law on the meaning of the indefinite article “a.” *SonicWall* held that “‘a computer’ may mean ‘one or more computers’” if “the same ‘one or more computers’” can satisfy subsequent limitations. *Finjan LLC v. SonicWall, Inc.*, 84 F.4th 963, 974 (Fed. Cir. 2023) (citing *Salazar v. AT&T*

Mobility LLC, 64 F.4th 1311, 1317 (Fed. Cir. 2023)). Here, per the '957 specification, the top/bottom bias voltage may change, *i.e.*, it is not limited to a single, constant voltage level. Thus, all that the claims require is that this changing bias voltage be applied in both stages.

III. GROUND 1

A. Voltage Applied on a Word-Line Layer Is Applied “on a Gate Terminal”

PO attempts to distinguish Hongtao by arguing that it shows voltages on word lines rather than on gates. POR 32–44. PO argues gate voltages need time to develop from “target voltages applied to word lines,” and thus gate-voltage waveforms would appear “curved” due to a significant RC (resistance-capacitance) delay “associated with a given word line.” *Id.*, 32, 37–38. In contrast, Hongtao shows straight-line waveforms, allegedly representing target word-line voltages. *Id.*, 38. PO’s position should be rejected, both because it ignores Hongtao’s disclosure of gate voltages and because it is inconsistent with the '957 patent and prior-art references. Liu2 ¶ 15.

1. Hongtao Discloses Applying Voltages on Gate Terminals

PO does not dispute that Hongtao shows first bias and lower second bias voltages. Liu2 ¶ 16. PO merely asserts that Hongtao discloses word-line voltages rather than gate voltages. PO is wrong. As the Board correctly recognized, Hongtao discloses that “[t]he *gates* of the unselected memory cells on the selected string *are*

applied with a conduction voltage through the unselected word lines.” Ex. 1005, [0025] (cited in ID, 13). PO, in effect, simply ignores this sentence and makes its same flawed “voltage-on-the-gate-terminal” arguments. POR, 36–40. This demonstrates that PO’s “voltage-on-the-gate-terminal” arguments cannot be correct, because they contradict express prior-art statements. Further, a POSITA would have understood that Hongtao discloses applying the conduction voltage on the gates by disclosing the effect of that voltage on channel coupling and read interference. Liu2 ¶¶ 17–18. Finally, because Hongtao’s Figure 2 “gate[]” voltage is shown to peak and then plateau for a period of time, it cannot be reasonably said, as PO urges, that this gate voltage actually never reaches this plateaued peak value. *Id.* ¶ 19.

PO’s argument that Hongtao’s paragraph [0026] does not explain why Hongtao lowers the bias voltage during the read phase also fails. POR, 41–43. Paragraph [0026] states a general principle affecting read interference, namely, the greater the interference-inducing voltage, the greater the interference. A POSITA would have understood that reducing conduction voltage reduces “conduction voltage - driving voltage,” the interference-inducing voltage. Hongtao’s Figure 2 shows exactly that. Figure 3, which “*further* reduce[s] the read interference,” does not negate Figure 2. Ex. 1005, [0026]; Liu2 ¶ 20. Hongtao does not teach away from Figure 2. *In re Peterson*, 315 F.3d 1325, 1331–32 (Fed. Cir. 2003).

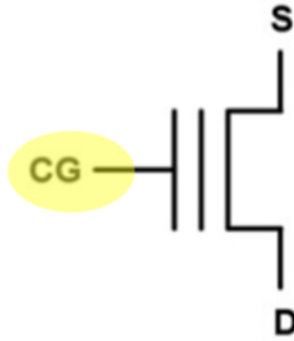
2. PO's Manufactured Word-Line-Voltage Dispute Fails

Even if the Board were to find that Hongtao does not disclose “gate” voltage (it does), PO's arguments still fail, because word-line voltages are gate voltages. PO's alleged distinction is simply made up: (a) the '957 patent and prior-art references use “gates” and “word lines” and their voltages interchangeably; (b) PO's curved-waveform argument is full of contradictions and would leave the '957 patent without a single claimed embodiment; (c) PO's alleged RC delays across a word line would create untold complications for real-world devices and §112 problems for the '957 patent because every memory cell experiences a different delay. Put simply, the word-line voltages shown in figures in the '957 patent and prior-art references are gate voltages—regardless of nomenclature—because applying voltages to effectuate memory-cell operations is the focus of this art, not some voltage that would be delayed and deformed before serving its function. Liu2 ¶ 21.

a. The Art Use Gate Terminals and Word Lines Interchangeably

Neither the '957 patent nor the prior art distinguishes word lines from gates. In fact, PO agrees that word lines function as gates. In a related IPR, PO states: “the wordlines serve as the gates of the transistors....” Ex. 1029, 11. That is so because word-line voltages are gate voltages that effectuate memory-cell operations. Liu2 ¶ 22; *infra* §III.A.2.c.

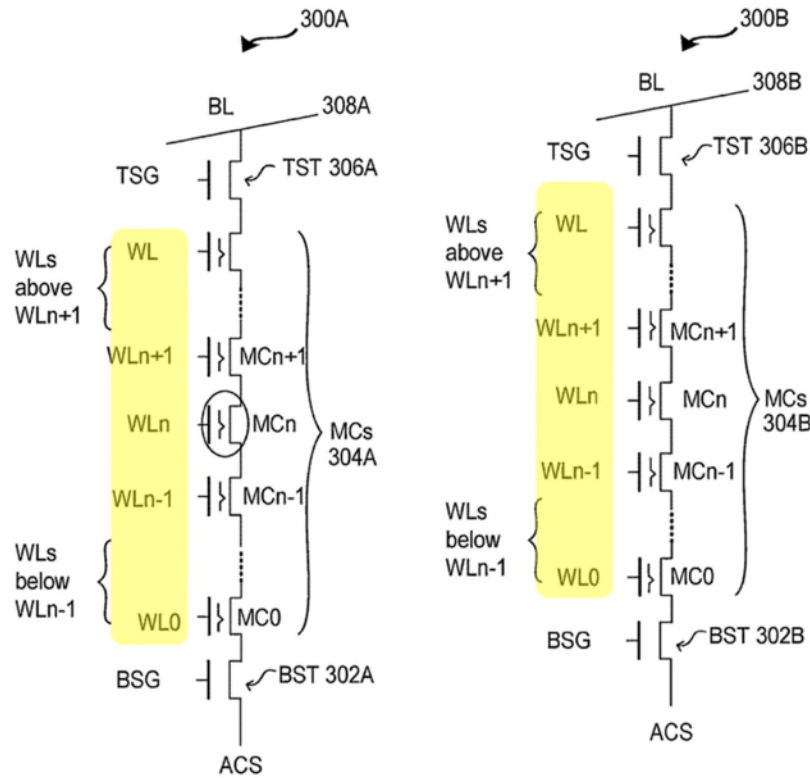
Preliminarily, a gate (terminal) is also called a control gate (“CG”), as shown in this well-known symbol of a memory-cell transistor:



Ex. 1018, 81; Liu2 ¶ 23.

The '957 patent uses “gate” and “word line” interchangeably.

First, the '957 patent equates “gate layers” with “word line layers.” Ex. 1001, 8:4. It also labels the memory-cell-transistor control gates as “WL” (*i.e.*, word line):



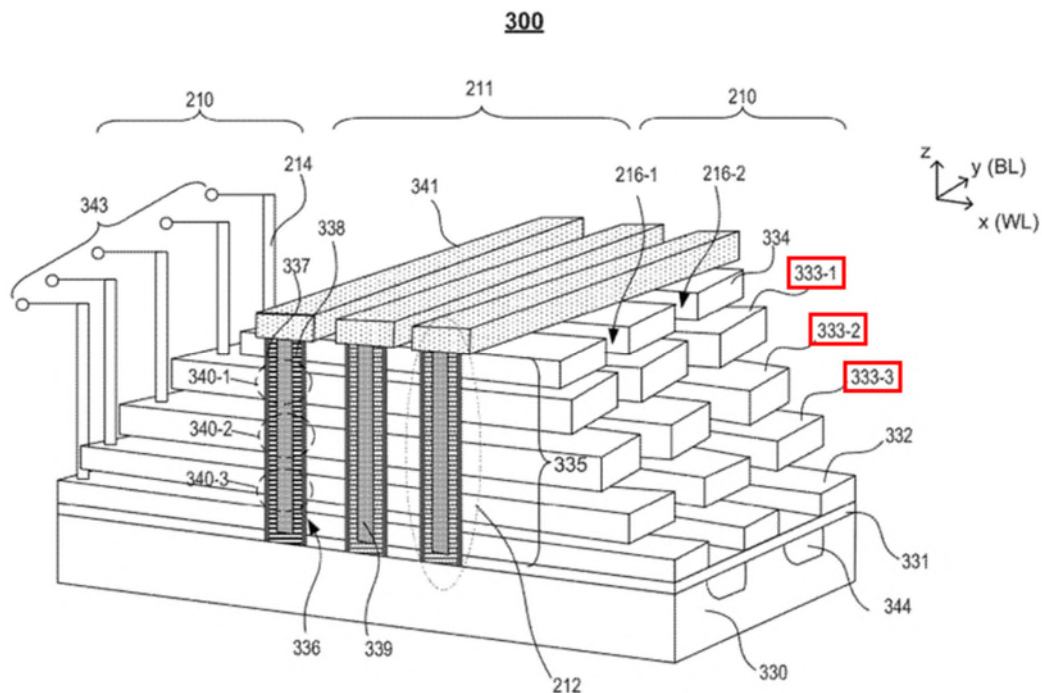
Id., Fig. 3. Thus, Figure 3 demonstrates that the waveforms in Figures 4–9 labeled with “WL” and described as word-line voltages are gate voltages. Liu2 ¶¶ 24–25.

Second, the ’957 patent repeatedly describes memory-cell operations based on word-line voltages, impliedly equating word-line voltages with gate voltages. Liu2 ¶ 26. In a narrow technical sense (not used by the ’957 patent), memory-cell operations depend on gate voltages, not word-line voltages, because transistors have gates, not word lines. Ex. 1018, 81 (the transistor symbol). Thus, the ’957 patent only makes sense if it does not distinguish word-line voltages from gate voltages. For example, the patent discloses “[t]he verify/read operation can be configured ... *by applying appropriate bias voltages on the word line layers* of the memory

cells....” Ex. 1001, 9:62–67. Appropriate bias voltages on word-line layers can be used to configure verify/read operations because they **are** appropriate bias voltages on the gates.

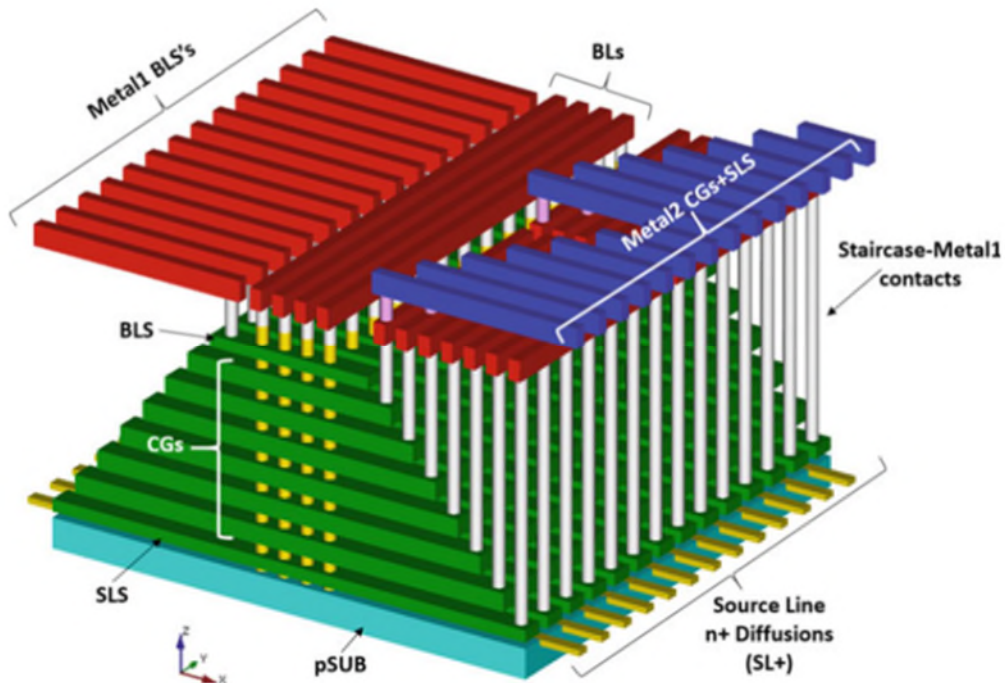
Turning to prior-art references, they corroborate that control gate and word line are used interchangeably.

First, the prior art equates the two terms. For example, another patent assigned to PO states that “control gates 333 [are] also referred to as ‘word lines (WLs).’” Ex. 1025, 6:41–42:



Id., Fig. 3; Liu2 ¶ 27.

Other references treat control gates and word lines as synonyms:



Ex. 1018, 131 (showing word-line layers as “CGs”).

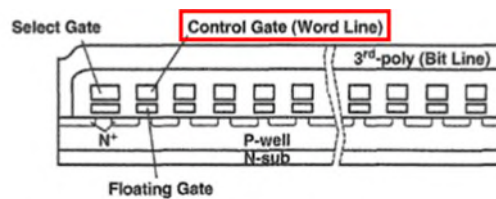
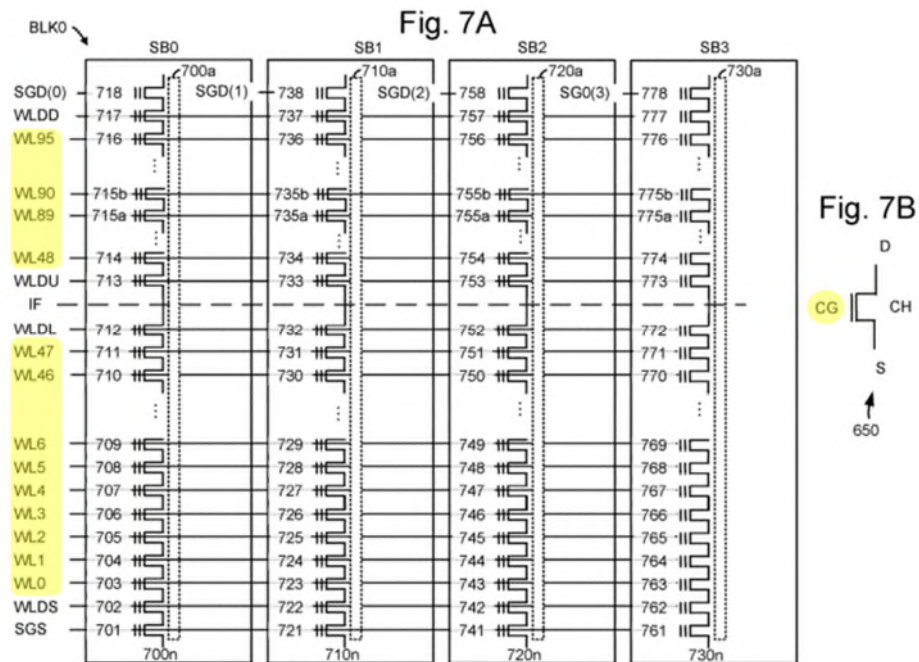


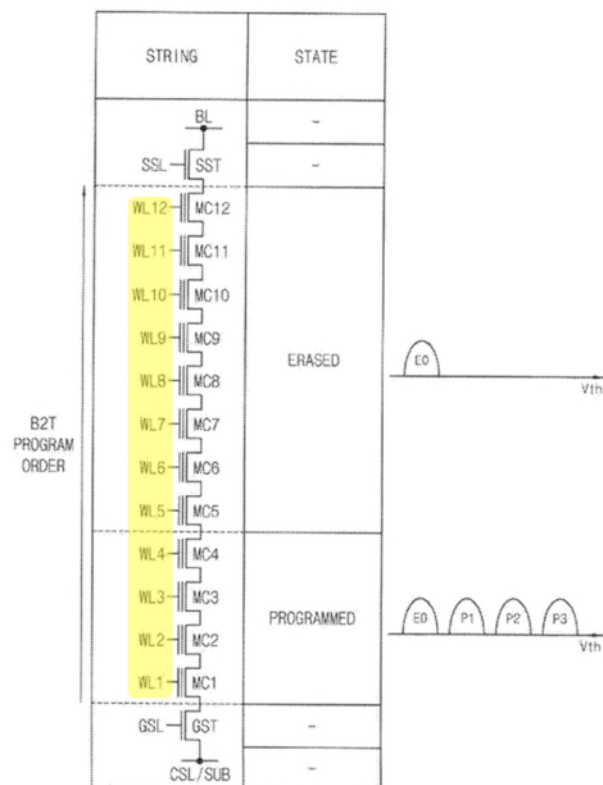
FIGURE 3.4 Cross-sectional view of a 0.4-μm-rule NAND-structure cell. Copyright 1994, The Japan Society of Applied Physics.

Ex. 1014, 62; *id.*, 205 (“CGs (word lines: WLs)”); Liu2 ¶¶ 28–30. Patent literature, including a reference cited by the ’957 patent, also uses the two terms synonymously. Liu2 ¶ 31.

Further, like the ’957 patent, prior-art references label gates of memory-cell transistors as “WL”:

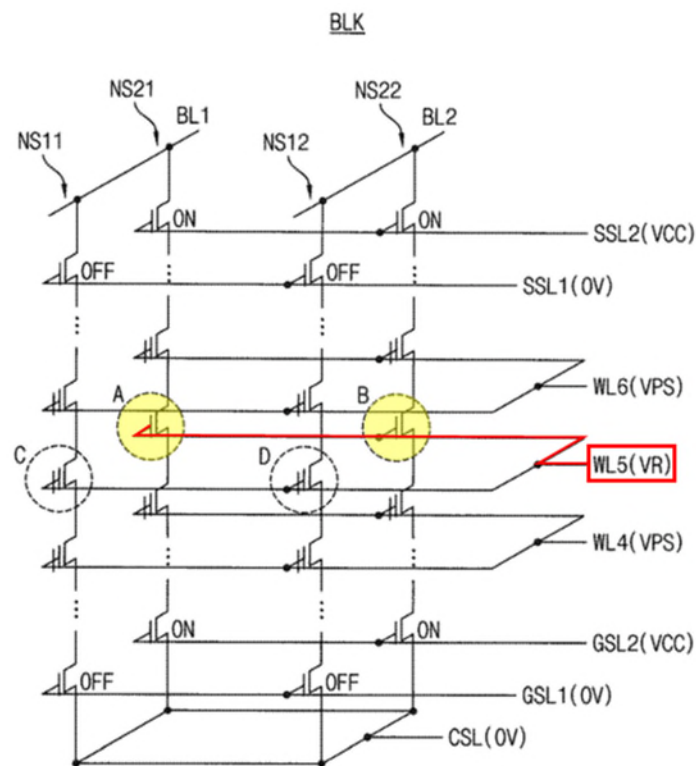


Ex. 1030, Figs. 7A–7B.



Ex. 1006, Fig. 11; Liu2 ¶ 32.

Second, prior-art references disclose applying gate voltages on word lines or, conversely, applying word-line voltages on gates. For example, the aforementioned '957-cited reference discloses “**applying a control gate voltage ... to the selected word line**” for a verify operation. Ex. 1030, 3:38–42; Liu2 ¶ 33. As a reciprocal example, Costa’s Figure 10 shows “WL” voltages, which Costa describes as “a signal **applied to the control gates....**” Ex. 1008, [0085]; Liu2 ¶ 34. As a further example, Ko describes that the “read voltage VR is **applied to [the] gates** of the selected memory cells A and B.” Ex. 1021, [0102]. VR is a word-line voltage:



Id., Fig. 13, [0102]; Liu2 ¶¶ 35–36.

Additionally, like the '957 patent, other references disclose applying word-line voltages to effectuate memory-cell operations. For example, references routinely describe applying word-line voltages to turn on memory cells. In doing so, the art is describing applying voltages on gates because gate voltages (in PO's narrow sense) determine memory-cell operations. Liu2 ¶¶ 37–39.

Third, Suzuki contradicts PO's position. PO affirms that Suzuki shows gate voltages including VCGM because of its curved waveforms. POR, 53; Ex. 1031, 216:1–7; Liu2 ¶ 40. Describing Figure 11, Suzuki states, contrary to PO's position: "VCGM is *applied to the word lines....*" Ex. 1007, [0138].

b. Patent Owner Distorts the Import of Curved Waveforms

PO argues that Hongtao does not disclose gate voltages because Hongtao shows piecewise-linear waveforms rather than curved waveforms. POR, 38–40, Ex. 1031, 168:13–169:7. PO alleges that gate voltages need time to develop from target word-line voltages, resulting in curved waveforms. POR, 36–38. PO's curved-waveform argument distorts the '957 patent.

As an initial matter, Figure 5, the conventional scheme PO extensively relies on to support this purported distinction, does not support PO's argument.³ It is the only embodiment among Figures 4–9 that cannot prevent HCI and ESUM loss, the invention's alleged benefit. For reasons explained in the next section, that deficiency stems from the delay between the voltage-generating circuits and the word-line layers. That delay does not allow word-line/gate voltages in the conventional scheme to develop to the target level within a short pre-pulse time of less than 1 nanosecond. On the other hand, the claimed embodiments Figures 6–9, whether given a short or long pre-pulse period, allegedly do not have this deficiency. Thus, a POSITA would understand that the curves of Figure 5 illustrate this insufficient voltage development, rather than distinguishing gate voltages (curved) from word-line voltages (linear) as PO argues. Liu2 ¶ 46 (citing, *e.g.*, Ex. 1001, 15:18–30, 11:57–12:27). Accordingly, the '957 patent consistently refers to word-line

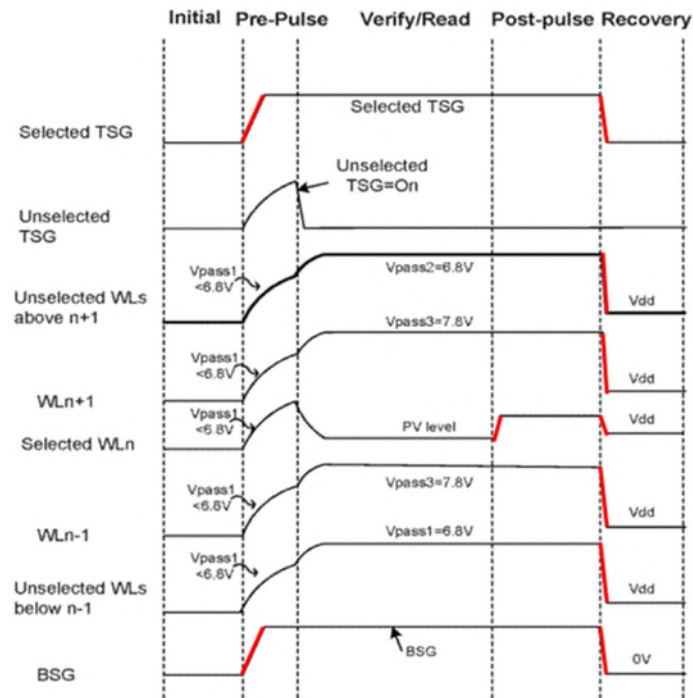
³ Figures 4–5 of the '957 patent illustrate conventional schemes, called “related example[s].” Ex. 1001, 5:50–55. Figures 6–9 illustrate claimed embodiments. Liu2 ¶¶ 41–44. In deposition, PO's expert was unable to identify if any of these figures is a claimed embodiment and admitted that “embodiment(s)” in his declaration does not mean “claimed embodiments.” Ex. 1031, 123:10–124:20, 139:13–140:1; Liu2 ¶ 45.

voltages—not gate voltages—being “developed.” Liu2 ¶ 47. And disclosures of voltages that are not fully developed are directed to conventional schemes with short pre-pulse time, *e.g.*, Figure 5. Ex. 1001, 6:66–7:12, 12:15–18.

Moreover, PO’s curved-waveform argument is full of contradictions.

First, PO’s argument would lead to the absurd result that not a single embodiment satisfies the claims of the ’957 patent. *See* Ex. 1031, 221:15–223:19 (PO’s expert opining that Figures 6–7 do not show gate voltages). Only Figure 5 shows curves. But Figure 5 does not embody any claim. Liu2 ¶ 48. Especially in view of the resulting complex technical issues, PO’s argument would invalidate the patent for lack of written description and enablement for handling PO’s alleged RC delays between word-line and gate voltage. *Infra* §III.A.2.c. That cannot be the right result. *Wang Lab’ys, Inc. v. Am. Online, Inc.*, 197 F.3d 1377, 1383 (Fed. Cir. 1999).

Second, under PO’s theory, Figure 5 is internally inconsistent because it only shows curves for some rising voltages. The falling voltages on the same waveforms should also be—but are not—curved because RC delays apply to both. Ex. 1031, 214:8–215:4. Nor is the rising edge of Selected WLn curved during the post-pulse period:

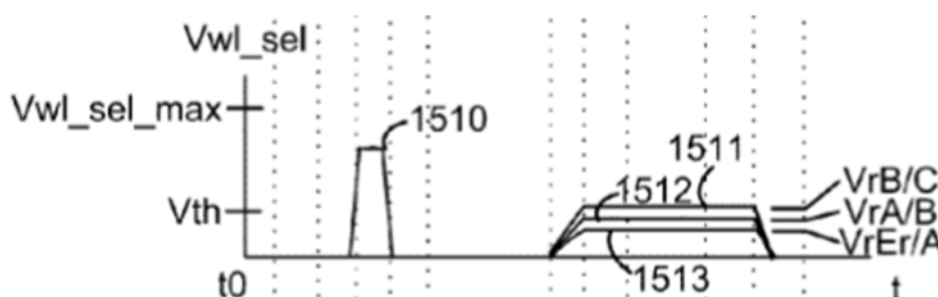


Ex. 1001, Fig. 5. Further, Selected TSG and BSG waveforms have no curves. But those are also word lines. Ex. 1031, 53:3–54:5. On the other hand, Petitioner’s position that the curves illustrate insufficient time for word-line voltages to fully develop before their levels change after a short pre-pulse period resolves such inconsistencies. Liu2 ¶ 49.

Further, in contrast, prior-art curved waveforms are internally consistent. Ex. 1007, Fig. 11; Ex. 2007, Fig. 8B; Ex. 1030, Fig. 10A. Figure 5’s inconsistencies under PO’s theory make it an unreliable source for interpreting the ’957 patent. Liu2 ¶ 50; *Trs. of Columbia Univ. in City of New York v. Symantec Corp.*, 811 F.3d 1359, 1366 (Fed. Cir. 2016) (opining that the patentee cannot rely on inconsistencies in its

own specification to support a claim construction). Indeed, the apparent inconsistencies show PO to be wrong.

Third, prior-art references contradict PO’s distinction of voltages by the waveform shapes. They simply do not distinguish the two voltages as PO does. For example, the figure below shows piecewise-linear V_{wl_sel} waveforms at three levels $V_{rB/C}$ – $V_{rEr/A}$:



Ex. 1019, Fig. 15B. But the reference states “ V_{wl_sel} can be provided at one of three **control gate** read levels.” *Id.*, 25:2–3. And Suzuki discloses a reciprocal scenario: applying curved-waveform voltages to word lines. Ex. 1007, [0134]. Similarly, the aforementioned ’957-cited reference discloses a curved waveform as “a voltage **applied to a word line**....” Ex. 1030, Fig. 10A, 19:60–61; Liu2 ¶ 51.

c. Patent Owner Errs on the Dominant Source of RC Delays and Creates an Unworkably Complicated Device

PO argues that significant RC delays exist across a word-line layer in 3D NAND devices such that a word-line voltage and its corresponding gate voltage are

different. POR, 36–38.⁴ PO is mistaken about the dominant source of RC delays. If PO’s theory were correct, memory devices would be unworkably complicated and the ’957 patent and reference would fail to enable a POSITA to practice their disclosures.

In 3D NAND flash, applied voltages from voltage-generating circuits experience RC delays before reaching word-line layers because of resistance in intervening components. Liu2 ¶ 52. Due to these RC delays, the word-line voltages lag in time relative to the voltage-generating-circuit outputs. This was Dr. Liu’s testimony in a related IPR: “***signal takes time to go from the voltage generation circuit and be reinserted to the word line....***” POR, 37 (emphasis added in POR). In comparison, the word-line layers have negligible resistances. And word-line voltages and gate voltages are the same because word lines are gates. Liu2 ¶¶ 53–55.

⁴ In deposition, PO’s expert shifted his theory to include resistance of word line drivers (analogous to voltage-generating circuits) and other unspecified components. Ex. 1031, 92:4-10, 162:9-15, 164:19-165:11, 171:12-172:8. His shifting theory corroborates Petitioner’s position that other components contribute to the RC delays. PO is wrong, however, to assert that the word-line layers by themselves significantly contribute to the resistance.

If that were not the case (as PO argues), serious operational issues would arise that neither the '957 patent nor prior art discusses. Under PO's theory, because a significant part of RC delays occurs on the word-line layers, each memory cell would experience different RC delays. Ex. 1031, 209:19–210:13. This would complicate memory operation or create more operational errors. PO's theory involves RC delays that are "complicated aggregation" of resistance and capacitance "depend[ing] on the actual physical layout of a specific 3D-NAND Flash design." *Id.*, 204:19–205:8, 164:19–165:11. Making matters worse, each word-line layer would have **multiple** RC time constants, and the RC time constants would depend on "[e]very physical aspect of the integrated circuit and the layers therein," "determined by a myriad [of] factors," resulting in "no simple algebraic representation of the waveform." *Id.*, 209:19–210:17, 207:18–208:17, 169:12–170:14. These are not issues that the '957 patent or prior art contemplates. Liu2 ¶¶ 56–57. Indeed, their interchangeable references to gate voltages and word-line voltages proves PO wrong. See *Ecolab, Inc. v. FMC Corp.*, 569 F.3d 1335, 1345 (Fed. Cir. 2009) (finding, where claim language permits an operable construction, the inoperable construction is wrong); *Wang Lab'ys, Inc.*, 197 F.3d at 1383; Liu2 ¶¶ 58–59.

In view of such complexity in determining RC time constants, PO's bare assertion that Hongtao's elevated pre-conduction voltage is a time-minimization

technique is a sleight of hand. *See* Ex. 2003 ¶¶ 97–99 (providing no basis from Hongtao). PO’s argument rests on a curved waveform added to Hongtao’s first and second bias voltages. POR, 40. But this waveform, like the other curved waveform PO’s expert created, has “no specific RC time[]constant.” Ex. 1031, 208:18–209:18. The waveform simply and magically reaches the target level at exactly the right time required to support PO’s time-minimization argument. POR, 39–40. A waveform that overshoots or undershoots the target voltage is much more likely without considering a myriad of factors. Liu2 ¶¶ 60–61. Yet Hongtao, a presumptively enabling patent application from PO itself, is completely silent on these considerations. *See Apple Inc. v. Corephotonics, Ltd.*, 861 F. App’x 443, 449 (Fed. Cir. 2021) (stating the “well-established” rule that foreign patent applications “are presumed enabling”).

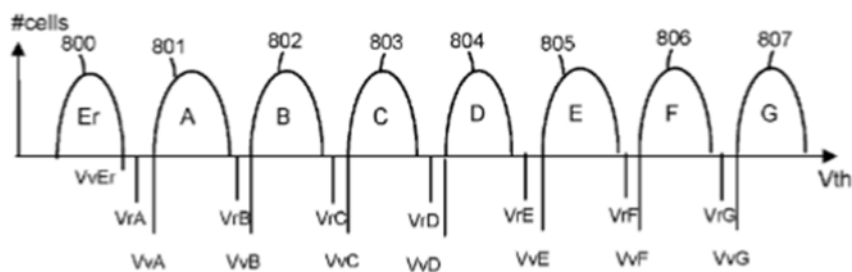
* * *

For these reasons, PO’s “voltage-on-the-gate-terminal” argument fails. *See also* Liu2 ¶¶ 62–65 (identifying additional inconsistencies and mischaracterizations in PO’s arguments).

B. Read Operations At Least Render Obvious Verify Operations

Even though verify and read operations are “virtually identical” (Pet., 72), PO argues that verify operations would not have been obvious or understood from Hongtao’s read operations. POR, 27–32. Verify operations are merely read

operations executed after, and to verify, program operations. *Id.*, 73. Indeed, PO’s expert uncritically and voluntarily refers to “read verify operations” when explaining read operations. Ex. 1031, 81:2–82:4. Well known and routine, the read voltage (*e.g.*, V_{rA} – V_{rG} below) is slightly lower than the corresponding verify voltage (V_{vA} – V_{vG}). Ex. 1003 ¶ 193; Liu2 ¶¶ 66–67:



Ex. 1017, Fig. 8A; 15:15–21.

The ’957 patent and the prior art reject any notion that a POSITA would not have looked at these operations as, in effect, one and the same.

The ’957 patent claims “[a]n apparatus for **reading** a memory device...” comprising pre-**verify** and **verify** stages. Ex. 1001, claim 1; *id.*, Fig. 10, 15:31–33 (language virtually verbatim to claim 1 “of a method 1000 for **reading** a memory device.”). The inventors could have—indeed **should** have if the two operations are distinct—claimed “[a]n apparatus for **verifying** a memory device.” But they didn’t. Further, the ’957 specification consistently describes, as an “aspect of the disclosure, a method [or an apparatus] for **reading** a memory device” that comprises **pre-verify** and **verify** stages. Liu2 ¶ 68. The inventors plainly considered reading and verifying

to be interchangeable. In fact, the same sentence equating gate terminal with gate also equates read with verify. Ex. 1001, 9:41–44 (“In addition, a **read (or verify)** voltage can be applied on the **gate terminal (or gate)**....”).

Prior-art references also refute PO’s argument. Pet., 72–74. Both read/verify involve a sensing operation to detect the selected cell’s threshold voltage. Liu2 ¶¶ 69–70. Both involve the same processing flow. *Id.* ¶ 70. The same voltage generators generate voltages to control both. *Id.* ¶¶ 71–72; Ex. 1031, 101:13–22, 102:18–104:4. Given these similarities, read operations would have rendered verify operations obvious, and combining the two also would have been obvious, involving merely routine and simple changes well within a POSITA’s skill. Liu2 ¶ 73.

PO’s argument that verify operations can use lower bias voltages on unprogrammed cell is irrelevant. POR, 31. As PO concedes, this is an optional “capab[ility].” *Id.* Suzuki’s verify operation, for example, does not involve this capability. Ex. 1007, Fig. 11 (showing WL_{usel} for all unselected gates). Further, the claims do not require applying a voltage on the unprogrammed cells lower than that on the programmed cells during either the pre-verify or verify stage. Liu2 ¶ 73.

PO’s citations do not compensate for its flawed argument. In fact, its cited references are consistent with Petitioner’s position. *Id.* ¶ 74.

C. Hongtao's Two Phases Correspond to the Pre-Verify and Verify Stages

Misapplying the Board's statement regarding Ground 3, PO argues that Hongtao's pre-conduction and read phases do not respectively correspond to the pre-verify and verify stages. POR, 31–32. PO's argument is conclusory. Ex. 2003 ¶ 84; Liu2 ¶ 75. As Dr. Liu has explained, Hongtao's pre-conduction phase prepares for the sensing operation occurring in the read phase (*i.e.*, verify phase) by pre-conditioning the channels to reduce HCI. Ex. 1003 ¶¶ 71–72, 75. Additionally, Hongtao's pre-conduction voltage serves the same function as the first verify voltage. *Id.* ¶ 105. PO did not rebut these explanations. Liu2 ¶ 76.

D. Hongtao Renders Obvious Claims 5–6

PO's argument against claims 5–6 rests on its flawed claim construction. Under the correct construction, Hongtao in view of Yu satisfies claims 5–6. Liu2 ¶¶ 77–78.

IV. GROUND 2

A. Suzuki Discloses a First Bias Voltage in a Pre-Verify Stage

PO incorrectly contends that the beginning of Suzuki's recovery phase cannot be part of "pre-verify stage," and hence Suzuki does not disclose the first bias voltage. POR, 50–54.

To start, there can be no reasonable debate that programming terminates after the WLsel voltage decreases below VPGM (the very beginning of t3). Ex. 1007,

[0137]. Next, applying VPASS on unselected memory cells during t3–t4 self-boosts the channel voltage to prepare for a voltage transition,⁵ avoiding a disturb phenomenon, and is therefore part of the process that “pull[s] out” the electrons for more accurate sensing. Ex. 1007, [0134]–[0135], [0140]. In short, the recovery operation in t3–t6 effectuates the removal of the electrons for a more accurate, and thus prepares for, the verify step. Thus, recovery is “pre-verify.” And VPASS is integral to the recovery operation. Thus, VPASS is a first verify voltage. Liu2 ¶¶ 81–82.

B. Suzuki Discloses Claims 5–6

PO’s argument regarding Claims 5–6 relies on its erroneous claim construction. POR, 58. Thus, Suzuki discloses claims 5–6. *Supra* §§II, III.D; Liu2 ¶ 83.

V. GROUND 3

PO employs straw-man arguments against Costa and Seo individually. Ground 3 posits that Costa and Seo together, not individually, render the Challenged Claims obvious. Liu2 ¶ 84.

⁵ t1–t2 prepares for a voltage transition as part of programming, just like t3–t4 prepares for a voltage transition as part of pre-verify. Ex. 1007, [0134]–[0135].

A. Costa and Seo Render Obvious Applying Voltages on Gate Terminals

PO attacks Ground 3 using the same “voltage-on-the-gate-terminal” argument. POR, 67–68. This argument fails for the same reasons explained in Ground 1. The idea that these references—dealing with operations that gate voltages control—instead disclose voltages on the edge of word lines and take an unknown time to travel to the gates strains credibility. Liu2 ¶ 85; *supra* §III.A.2.

B. A POSITA Would Have Been Motivated to Combine Costa and Seo with a Reasonable Expectation of Success

1. Combining Costa’s Verify Operation and Seo’s Read Operation Would Have Been Obvious

To the extent that PO’s vague assertion of a lack of motivation to combine Costa’s verify with Seo’s read is based on an alleged distinction between the two operations, PO is wrong. POR, 60; *supra* §III.B; Liu2 ¶ 86.

2. Seo’s Two Time Periods Correspond to the Two Stages, and Costa’s Sensing Phase Corresponds to the Verify Stage

Based on the pre-institution record, the Board found it unclear how Seo’s time periods and Costa’s sensing phase correspond to the ’957 patent’s two stages. ID, 26–27. With the correct understanding that read and verify operations are virtually identical, the correspondence between Seo’s two time periods to the claimed pre-verify and verify stages would have been obvious. Verification takes place during period t2 when Vread is applied to Sel WL and Vpass is applied to Unsel WLs. Thus, period t2 corresponds to the verify stage. Voltages applied in period t1

condition the channel to reduce HCI before reading. Thus, period t1 corresponds to the pre-verify stage. Liu2 ¶¶ 87–88.

Costa’s “sensing phase” corresponds to Seo’s time period t2 and the claimed verify stage. Programming is verified by setting up appropriate voltages on the memory cells during the sensing phase. *Id.* ¶ 89. Indeed, Costa expressly identifies the voltage setup as a verify operation. Ex. 1008, [0138], [0023].

3. Lowering Seo’s Vpass During the Verify Stage Would Have Been Obvious Based on Costa

The Board also found it unclear that “[Costa’s] VreadL is a second bias voltage that is smaller than the first bias voltage (Seo’s VPASS).” ID, 27. The Petition explained that it would have been obvious to lower Seo’s voltage applied on the unselected word lines during the verify stage. Pet., 128.

Costa’s pass voltage Vread and Seo’s pass voltage Vpass both turn on all unselected memory cells to verify the selected cell. Thus, both pass voltages must be high enough to ensure all unselected cells act as pass gates. Liu2 ¶¶ 90–91. A POSITA would have at least found it obvious to use the same voltage level for both because they perform the same function. *Id.* ¶ 92. Costa recognizes this voltage level is “an overdrive voltage” but that it should “generally be set as low as possible” “[t]o limit read disturb....” Ex. 1008, [0096]. This teaching on Vread also applies to Seo’s Vpass in the combination because both are pass voltages applied on unselected word lines and because limiting read disturb is generally desirable for

flash devices. Liu2 ¶ 93. Thus, as Costa reduces its voltage to V_{readL} , a POSITA would have found it obvious to also lower the second bias voltage in the combination.

It would have been obvious to lower Seo's V_{pass} only during the verify stage. Ex. 1003 ¶ 308. Seo turns off the selected memory cell during the pre-verify stage. Ex. 1009, Fig. 8 (showing a low voltage on "Sel WL" during t_1). Without a conductive path across the selected memory cell, the source terminals of the cells above the selected cell are left floating and their voltages increase. But since (gate voltage - source voltage) relative to the threshold voltage determines cell operations, keeping the gate voltage high when the source voltage increases ensures the memory-cell transistors would turn on, whether the cell is programmed or unprogrammed. Doing so does not significantly increase HCI because the t_1 period is short. It reduces the risk of not turning on unselected cells, which, contrary to Seo's objective, would increase HCI-induced read disturb on unselected memory strings. Liu2 ¶ 94.

Unlike Dr. Liu's explanations, PO's arguments that the Petition "contradicts the basic operating principles of NAND memory strings" (POR, 62) and that Costa's teaching to lower the read voltage "is equally applicable in both time periods" (*id.*, 66) are conclusory. *Id.* ¶ 95.

In any event, only two realistic options exist for the Vread level during the pre-verify stage: keeping it at the normal level or lowering it as in Costa’s verify stage. A POSITA would have at least found it obvious to try both options and would have found the claims obvious. *See Google LLC v. Koninklijke Philips N.V.*, 795 F. App’x 840, 846 (Fed. Cir. 2020); Liu2 ¶ 96.

VI. PO’S EXPERT TESTIMONY IS ENTITLED TO LITTLE WEIGHT

Dr. Przybylski’s declaration and deposition testimony are entitled to little weight.

First, Dr. Przybylski’s declaration merely parrots PO’s Response through conclusory remarks, including words copied from the Response and then altered. This is most evident where the declaration altered quotations from references for no apparent reason—and without any acknowledgement. For example, his declaration frequently replaces “apply [a voltage]” from the Response with “administer [a voltage].” Such replacements found their way into Hongtao, Suzuki, and Seo quotations. *Compare* POR, 18, 23, 64 *with* Ex. 2003 ¶¶ 57, 63, 157 (both “quoting” Hongtao, [0023], Suzuki, [0114], and Seo, [0089]). The most reasonable explanation for such alterations is an oversight in a copy-and-modify process.

Second, the record plainly contradicts his opinions. Even PO’s own patent contradicts his opinions. *Compare* Ex. 1025, 6:41–42 (“control gates 333 [are] also referred to as ‘word lines (WLs).’”) *with* Ex. 1031, 57:21–58:1 (“Q. Are control

gates also referred to as word lines? A. No.”). Dr. Przybylski’s opinions are entitled to no weight. *Xerox Corp. v. Bytemark, Inc.*, IPR2022-00624, Paper 9 at 15–16 (Aug. 24, 2022) (precedential).

Third, his testimony is disingenuous. For example, despite the centrality of waveform shapes to his arguments, he alleges that an analysis of whether Figures 5–7 show gate voltages is “completely tangential” to his task. Ex. 1031, 226:6–227:20, 230:18–234:9; *see also* Liu2 ¶ 45 (commenting on Dr. Przybylski’s inability to identify claimed embodiments). Dr. Przybylski’s testimony should be disregarded.

VII. CONCLUSION

Petitioner respectfully requests a final written decision finding the Challenged Claims unpatentable.

Dated: April 25, 2025

Respectfully submitted,

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CERTIFICATE OF WORD COUNT

The undersigned certifies that the foregoing Petitioner's Reply Brief with the word count limits set forth in 37 C.F.R. §42.24(a)(1)(i). Excluding the parts of the Petition exempted by 37 C.F.R. §42.24(a)(1), this Reply contains 5,582 words as determined using the word count feature in Microsoft Word, which was used to prepare this Reply.

Dated: April 25, 2025

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CERTIFICATE OF SERVICE

The undersigned hereby confirms that the foregoing paper was caused to be served on April 25, 2025 via electronic mail, upon the following attorneys of record for the PO:

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