

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,

Petitioner,

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,

Patent Owner.

Case IPR2024-00795
Patent 11,501,822

**DECLARATION OF STEVEN PRZYBYLSKI, PH.D. IN SUPPORT OF
PATENT OWNER'S RESPONSE**

Executed this 3rd day of January, 2025 in Ann Arbor, Michigan.



Steven A. Przybylski, Ph.D.

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LIST OF ABBREVIATIONS

Abbreviation	Term
'822 or '822 Patent	U.S. Pat. No. 11,501,822 (Ex. 1001)
Aritome	Aritome, “NAND Flash Memory Technologies” (2016) (Ex. 1006)
Brown	Brown et al., “Nonvolatile Semiconductor Memory Technology” (1998) (Ex. 1007)
Cappalleti	Cappelletti, et al., “Flash Memories” (1999) (Ex. 1008)
Challenged Claims	'822, Claims 1-9 and 11-19
Chen	U.S. Pat. No. 10,770,157 (Ex. 2004)
Hambley	Hambley, “Electrical Engineering Principles and Applications, Fourth Edition” (2008) (ex. 2008)
Kim	U.S. Pub. No. 2011/0194351 (Ex. 2005)
Liu	Declaration of Dr. David Kuan-Yu Liu (Ex. 1003)
Lee	U.S. Pat. No. 10,121,529 (Ex. 1004)
Office	U.S. Patent and Trademark Office
Petition or Pet.	Petition for <i>Inter Partes</i> Review of U.S. Patent No. 11,501,822 (IPR2024-00795, Paper 1)
Parallel District Court Litigation	<i>Yangtze Memory Technologies Company, Ltd. V. Micron Technology, Inc.</i> , NDCA-3-23-cv-05792 (N.D. Cal.)
Patent Owner	Yangtze Memory Technologies Co. Ltd.
Petitioner	Micron Technology, Inc.

POSITA	Person of ordinary skill in the art
Yang	U.S. Pat. No. 10,726,920 (Ex. 1010)
Zhao	U.S. Pat. No. 10,643,718 (Ex. 1005)

I, Steven Przybylski, Ph.D., hereby declare as follows:

I. INTRODUCTION

1. I have been retained by counsel for Yangtze Memory Technologies Company, LTD (“YMTC”) in the above captioned *inter partes* review of U.S. Patent No. 11,501,822 (Ex. 1001, “’822 Patent”). I have been asked to consider the scope and content of the prior art, and respond to certain allegations regarding the prior art, presented by Micron Technology, Inc., (“Petitioner”) in its petition for *inter partes* review of the ’822 Patent (“Petition”) and the April 9, 2024 Declaration of Dr. David Kuan-Yu Liu (Ex. 1003, “Liu”). The arguments raised in Dr. Liu’s declaration are similar to those raised in the Petition. Unless otherwise noted, my opinions with respect to the Petition also apply to the corresponding section of Dr. Liu’s declaration, and vice-versa. As explained in Sections X-XIII (discussing the Grounds raised in the Petition) the invalidity arguments raised in the Petition fail to anticipate or render obvious any of the Challenged Claims, and the arguments raised in Dr. Liu’s declaration fail for similar reasons.

2. I am being compensated for my time at my usual consulting rate of \$575 per hour, plus reimbursement for any actual expenses. No part of my compensation depends on the content of the opinions that I herein render or on the outcome of this review proceeding. I have no expectation or promise of additional business with

Patent Owner in exchange for the positions explained herein. I do not have any direct financial interest in any of the parties.

3. Unless otherwise noted, the statements made herein are based on my personal knowledge, and if called to testify about this declaration, I could and would do so competently and truthfully.

II. QUALIFICATIONS

4. My qualifications including cases in which I was an expert are stated more fully in my curriculum vitae which has been provided as Appendix A. Here, I provide a brief summary of my qualifications.

5. I earned a Bachelor of Applied Science from the University of Toronto in 1980. I was enrolled in the Engineering Science program, completing a course of study combining the Electrical Engineer and Computer Science options.

6. I earned a Master of Science in Electrical Engineering degree and a Ph.D. in Electrical Engineering in 1982 and 1988 respectively, both from Stanford University.

7. I also earned a Masters of Business Administration from the Haas School of Business at the University of California at Berkeley in 2000.

8. I have extensive experience with memory semiconductor integrated circuits and the memory systems constructed of them. At Stanford, my dissertation was on the optimization of single- and multi-level cache hierarchies to maximize

system-level performance. Also at Stanford, I was a member of the core team that architected, designed, built, and tested the seminal MIPS processor. I was responsible for the design of the instruction decode and control units as well as architecting the virtual memory support. I assembled and debugged the entire microprocessor design and oversaw its fabrication and testing. In 1984 and 1985, I took a leave of absence from Stanford to become a member of the founding team of MIPS Computer Systems, a startup in California that designed, built, and sold processors and computer systems. In 1989, after finishing my doctorate and brief post-doctorate at Stanford, I returned to MIPS Computer Systems. Throughout my two periods of employment at MIPS Computer Systems, I had a number of titles and worked on a variety of projects. Noteworthy were stints as processor architect, systems architect, hardware-software team liaison, and Chief Scientist of the High-End Systems group. During the second period, I also served as a Consulting Assistant Professor in the Department of Electrical Engineering at Stanford. I designed and taught an advanced graduate level course on cache and memory system design.

9. In 1991, I left MIPS to become an independent consultant. In that capacity I have provided technical, strategic, marketing, and intellectual property services to a large number of clients both domestically and internationally.

10. The technical consulting I performed was principally related to advancements in semiconductor memories and their application in systems. Specifically with respect to non-volatile memories and Flash memories in particular, I advised companies on a variety of memory types and on trends in NAND and NOR Flash memories and the processes used in their manufacture. In the 2000's, I helped develop a new NAND Flash architecture and separately a universal memory interface that was optimized for use in heterogeneous memory systems and that was equally applicable to DRAMs and to NAND Flash devices.

11. I am a member of both the Institute of Electrical and Electronics Engineers (IEEE) and the Association of Computing Machinery (ACM). In addition, in 1997 I became a registered patent agent. I am listed as the inventor on 11 domestic patents and their foreign counterparts. The subject matters include memory devices, memory subsystems, networks, error detection and correction codes, processors and cache memories. Between 1994 and approximately 2000, I was a leading independent analyst following, writing, and teaching about both the technical and business aspects of the DRAM industry. Overall, I have written three books and over 25 articles in the areas of memory, processors, and computer systems. In particular, I wrote and revised an 850-page book entitled "New DRAM Technologies: A Comprehensive Analysis of the New Architectures." I have presented many lectures, classes and seminars on semiconductor memories and their memory systems,

processors and computer systems. I have presented full and half-day seminars on discrete and embedded DRAMs to over 2,500 engineers, marketers, managers, and financial analysts.

III. MY ASSIGNMENT AND BASES OF OPINIONS

12. I have been asked to provide my opinions as to the scope and content of the prior art presented by Petitioner and Dr. Liu in the Petition. Specifically, I have been asked to provide my opinions concerning the scope and content of the Lee (Ex. 1004), Zhao (Ex. 1005), and Yang (Ex. 1010) references as would have been understood by a person of ordinary skill in the art, and to respond to certain assertions by Petitioner and Dr. Liu regarding the four Grounds presented in the Petition.

13. In the course of conducting my analysis and forming my opinions, I have reviewed the references and materials cited in the Petition and herein including those listed below:

Exhibit Number	Description
N/A	Petition for <i>Inter Partes</i> Review of U.S. Patent No. 11,501,822 (IPR2024-00795, Paper 1)
Ex. 1001	U.S. Patent No. 11,501,822 B2 to Jia et al.
Ex. 1002	File History of U.S. Patent No. 11,501,822 B2 to Jia et al.
Ex. 1003	Declaration of David Kuan-Yu Liu, Ph.D. (“Liu”)
Ex. 1004	U.S. Patent No. 10,121,529 B2 to Lee (“Lee”)
Ex. 1005	U.S. Patent No. 10,643,718 B2 to Zhao et al. (“Zhao”)
Ex. 1006	Aritome, “NAND Flash Memory Technologies” (2016)
Ex. 1007	Brown et al., “Nonvolatile Semiconductor Memory Technology” (1998)

Ex. 1008	Cappelletti, et al., “Flash Memories” (1999)
Ex. 1009	U.S. Patent No. 9,589,978 to Yip
Ex. 1010	U.S. Patent No. 10,726,920 B2 to Yang
Ex. 1011	Silvagni, “3D NAND Flash Based on Planar Cells,” Computers 2017
Ex. 1012	Micheloni et al., “Inside Solid State Drives (SSDs)” (2 nd Ed. 2018)
Ex. 1015	File History of U.S. Patent No. 11,081,164 (Appl 16-709,944) to Jia et al.
Ex. 1016	File History of U.S. Patent No. 11,862,230 (Appl 17-965,527) to Jia et al.
Ex. 1017	<i>Curriculum Vitae</i> of David Kuan-Yu Liu, Ph.D.
Ex. 2002	U.S. Pat. No. 11,081,164 (“the ’164 patent”)
Ex. 2003	File History of U.S. Pat. No. 11,081,164 (“’164FH”)
Ex. 2004	U.S. Pat. No. 10,700,157 (“Chen”)
Ex. 2005	U.S. Pub. 2011/0194351 (“Kim”)
Ex. 2012	Pulse, Wiley Electrical and Electronics Engineering Dictionary (2004)
Ex. 2013	Pulse, IEEE Standard Dictionary (1996)
Ex. 2014	Pulse, Webster's II New College Dictionary (2001)
Ex. 2015	Micron’s Preliminary Claim Constructions and Extrinsic Evidence Pursuant to Patent Local Rule 4-2, <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc.</i> , N.D. Cal. 3:23-cv-05792-RFL (Aug. 5, 2024) (“Micron’s Preliminary Claim Constructions”)
Ex. 2016	Dispose, Merriam-Webster’s Dictionary and Thesaurus (2014)
Ex. 2017	Dispose, Merriam-Webster’s Collegiate Dictionary (2012)
Ex. 2018	Dispose, American Heritage Dictionary of the English Language (2011)
Ex. 2019	Dispose, New Oxford American Dictionary (2010)
Ex. 2020	Series of Images, Stamped as Ex. 2020 in the December 17, 2024, Deposition of Dr. David Kuan-Yu Liu
Ex. 2021	Transcript of the December 17, 2024, Deposition of Dr. David Kuan-Yu Liu (“Liu Tr.”)
Ex. 2022	Hambley, “Electrical Engineering Principles and Applications, Fourth Edition” (2008) (“Hambley”)

14. My opinions in this declaration are based on my review of these documents, as well as upon my education, training, research, knowledge, and experience.

15. All emphases (such as bolding, underlying, or italics) appearing in quotations and citations cited herein have been added by me, unless otherwise stated.

IV. SUMMARY OF MY OPINIONS

16. It is my opinion that:

- Lee does not disclose or render obvious the use of “word line pre-pulse signal[s],” as required by the independent claims of the ’822 Patent. *See* ’822 Patent at 7:54-8:13, 8:53-9:13.
- Lee does not disclose or render obvious that groups of word lines are “disposed in an order of distance from the selected word line,” as required by dependent claims 2 and 12 of the ’822 Patent.
- Lee does not disclose or render obvious a “first group of the plurality of word lines are disposed adjacent to the selected word line,” as required by dependent claims 3 and 13 of the ’822 Patent.
- Zhao does not disclose or render obvious applying a “first word line pre-pulse signal ... during a pre-charge period,” as required by the independent claims of the ’822 Patent.

- A person of ordinary skill in the art would not have been motivated have been motivated to apply Lee’s purported teachings to Zhao’s system in the manner described in the Petition.
- Yang does not disclose or render obvious that “a voltage level of the second word line pre-pulse signal is greater than that of the first word line pre-pulse signal, and a voltage level of the third word line pre-pulse signal is greater than that of the second word line pre-pulse signal,” as required by the independent claims of the ’822 Patent.
- Yang does not disclose or render obvious that groups of word lines are “disposed in an order of distance from the selected word line,” as required by dependent claims 2 and 12 of the ’822 Patent.
- Yang does not disclose or render obvious a “first group of the plurality of word lines are disposed adjacent to the selected word line,” as required by dependent claims 3 and 13 of the ’822 Patent.

V. APPLICABLE LEGAL STANDARDS

17. I am not a legal expert and offer no opinions on the law. However, I have been informed by counsel of the various legal standards that apply, and I have applied those standards in arriving at my conclusions.

A. Claim Construction

18. I was informed, unless otherwise noted, I should give claim terms their ordinary and customary meaning as understood by a person of skill in the art at the time of the invention. I was informed and I understand that the words of the patent's claims and the context in which the term is used in the claims can be highly instructive in ascertaining the term's meaning. I further understand that the terms of a claim are to be interpreted in the context of the entire patent, including the patent's other claims, its specification and its figures.

19. I have been further instructed that a patent's "prosecution history" may often provide helpful evidence about how the Patent Office and the applicant understood the patent and its claims. Therefore, I have been instructed that claim terms should also be interpreted in light of the patent's prosecution history. In addition to the claims, the specification, the figures, and the prosecution history, I have been instructed that certain "extrinsic evidence" such as scientific or technical references may also help inform the way in which the person of ordinary skill in the art might understand the claim term. I have been instructed that extrinsic evidence must always be considered in the context of the intrinsic evidence.

B. Anticipation

20. I have been informed by counsel that a patent claim is invalid as anticipated if each element of that claim is present either explicitly or inherently in

a single prior art reference. I have also been informed that, to be an inherent disclosure, the prior art reference must necessarily disclose the limitation, and the fact that the reference might possibly practice or possibly contain a claimed limitation is insufficient to establish that the reference inherently teaches the limitation.

C. Obviousness

21. I understand that a claim is unpatentable if it would have been obvious to a person of ordinary skill in the art at the time the invention was made. I understand that a claim could have been obvious from a single prior art reference or from a combination of two or more prior art references. I understand that an obviousness analysis requires an understanding of the scope and content of the prior art, any differences between the invention and the prior art, and the level of ordinary skill in evaluating the pertinent art.

22. I further understand that a claim would have been obvious if it unites old elements with no change to their respective functions or alters prior art by mere substitution of one element for another known in the field, and that combination yields predictable results. Also, I understand that obviousness does not require physical combination or bodily incorporation, but rather consideration of what the combined teachings would have suggested to persons of ordinary skill in the art at the time of the invention.

23. While it may be helpful to identify a reason for this combination, I understand that there is no rigid requirement of finding an express teaching, suggestion, or motivation to combine within the references. When a product is available, design incentives and other market forces can prompt variations of it, either in the same field or a different one. If a person of ordinary skill in the art can implement a predictable variation, obviousness likely bars its patentability. For the same reason, if a technique has been used to improve one device and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique would have been obvious. I understand that a claim would have been obvious if a person of ordinary skill in the art would have had reason to combine multiple prior art references or add missing features to reproduce the invention recited in the claims.

24. I further understand that certain factors may support or rebut the obviousness of a claim. I understand that such secondary considerations include, among other things, commercial success of the patented invention, skepticism of those having ordinary skill in the art at the time of invention, unexpected results of the invention, any long-felt but unsolved need in the art that was satisfied by the invention, the failure of others to make the invention, praise of the invention by those having ordinary skill in the art, and copying of the invention by others in the field. I

understand that there must be a nexus, that is, a connection, between any such secondary considerations and the invention.

25. I understand that in considering obviousness, it is important not to determine obviousness using the benefit of hindsight derived from the patent being considered.

D. Claim Dependency

26. I understand that a patent may include two types of claims, independent claims and dependent claims. An independent claim stands alone and includes only the limitations it recites. A dependent claim can depend from an independent claim or another dependent claim. I understand that a dependent claim includes all the limitations that it recites in addition to all of the limitations recited in the claim from which it depends.

VI. THE '822 PATENT

A. Overview of the '822 Patent

27. The '822 Patent discusses a novel pre-charging process for applying signals to word lines of a three-dimensional non-volatile flash memory device to mitigate the effects of “programming disturb.” '822 Patent, 1:52-55. In general, “programming disturb” (or “program disturb”) occurs when performing a program operation on a selected memory cell inadvertently changes the programmed state of adjacent memory cells that share the same word line or the same bit line as the

selected memory cell. *See, e.g.*, Ex. 1006 (“Aritome”) at 52 (explaining that “[p]rogram disturb is a phenomenon in which the threshold voltage (V_t) of unselected cell is increased during program operation”); Ex. 1007 (“Brown”) at 239 (describing “[p]rogram-[d]isturb [m]echanisms” that alter the programmed state of “unprogrammed or erased cells that are connected to the same wordline as the cell being programmed” or “programmed cells that are on the same bitline as the cell being programmed”); Ex. 1008 (“Cappelletti”) at 32-33 (“Program disturbs affect cells sharing either the word line or the bit line of a cell addressed for programming ... and must be minimized with a tailored choice of the programming voltages and an optimized circuit design”).

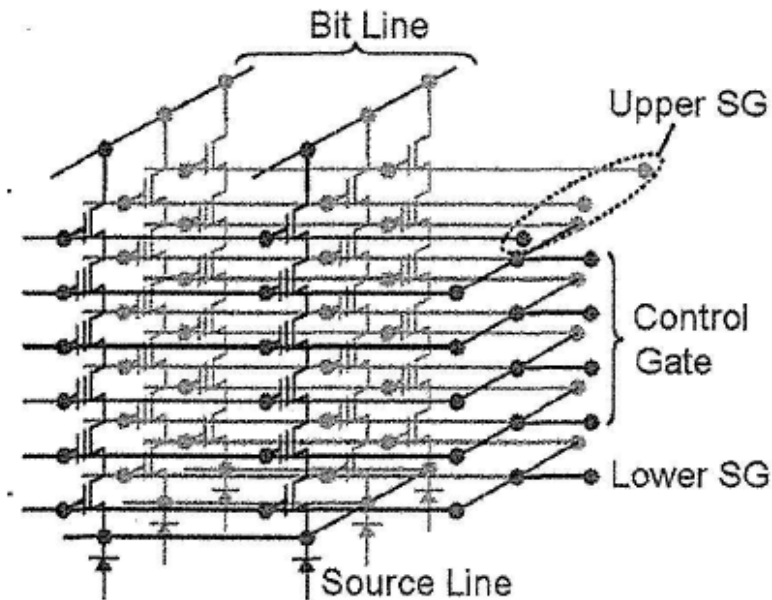
28. As explained by the ’822 Patent, the prior art at the time of the ’822 Patent sought to address programming disturb by employing a pre-charging process that would “remove boosting charges (electrons) of the unselected memory string.” ’822 1:32-39. However, the methods at the time had difficulty removing electrons in the “bottom of the channel,” and the typical approaches for addressing this issue—such as increasing the pre-pulse time or using a larger voltage level—had drawbacks on memory device programming speed and increased the risk of transistor breakdown. ’822 Patent, 1:38-48.

29. To address these problems, the ’822 Patent described a novel approach to pre-charging that improved on traditional methods by reducing the effects of

programming disturb without compromising device-level performance. '822 Patent, 1:53-55. The claimed pre-charging process introduced by the '822 Patent has several features that were not previously disclosed or rendered obvious by the art at the time. This includes, for example, applying three different pre-pulse signals of incrementally increasing voltages levels to three different groups of word lines during a pre-charge period. See '822 Patent, 1:56-2:27, claims 1, 11. As explained by the '822 Patent, by applying these incrementally increasing pulse signals to different groups of word lines, the overall duration of the pre-charging process is kept short and the voltage levels may be reduced, thus reducing the negative effects on programming speed and device longevity that came from traditional methods of pre-charging that would resort to longer pre-charging times or high voltage levels in an attempt to mitigate program disturb. '822 Patent, 1:41-48. As a result, the techniques described by the '822 Patent were able to overcome the drawbacks of the pre-charging methods previously disclosed in the art. See, e.g., '822 Patent, 1:20-48.

30. 3D NAND flash memory technology architecture has been developed to vertically stack memory cells across multiple layers to increase bit density and storage capacity as compared to traditional NAND memory. '822 Patent, 1:29-32. In general, 3D NAND flash memory organizes memory cells into vertically stacked “strings” of memory, which intersect with horizontally arranged “word lines” that

can be used to apply voltages onto the gate terminals of each of the individual memory cells. See '822 Patent, 2:43-3:2. These vertically stacked “memory strings” are then placed together to form a full three-dimensional array.



Ex. 1006 (“Aritome”), 296. Each memory cell in the string is formed as a transistor with a variable “threshold voltage” (i.e., the voltage that, when applied to the gate terminal of the memory cell, will cause the transistor to turn on and begin conducting current between the source and drain) that corresponds to the stored state of the memory cell. See, e.g., Ex. 1007 (“Brown”) at 30-32 (describing the basic operating principles of a transistor); Ex. 1008 (“Cappelletti”) at 14-17 (same). Voltages can be applied to the gate terminals of each memory cell through the corresponding “word lines,” and different voltages can be applied to the memory string channel (i.e., the channel that runs between the source and drain terminals of each memory cell within

the memory string) using the bit lines and source lines that are connected on either end of the memory string. *See* Ex. 1006 (“Aritome”), 42-49. At the top and the bottom of each memory string are also “select gate” transistors that are turned on in order to connect the corresponding memory string to the bit line and the source line, and which are typically used to selectively control which of the memory strings is connected to the bit line and source line at any given time. *Id.* 295-296.

31. During a programming operation, a high programming voltage (V_{pgm}) is typically applied to the word line connected to the memory cell that is being programmed—also known as the “selected” word line—while a low voltage (e.g., 0V) is applied to the bit line of the memory string containing the memory cell being programmed. Ex. 1006 (“Aritome”), 42-46. This creates a large voltage difference between the “gate” terminal of the memory cell (which is connected to the word line), and the channel of the memory cell (which is connected indirectly to the bit line). *See id.* This large voltage difference causes electrons to be injected into the storage layer of the memory cell, thus changing the threshold voltage of that memory cell which, in turn, can be detected using a subsequent “read” operation in order to determine the programmed value of the memory cell. *Id.*, 45-46.

32. To ensure that the voltage being applied to the bit line actually reaches the memory cell that is being programmed, a “ V_{pass} ” voltage—which is large enough to turn on the memory cells, but not large enough to cause electrons to be

injected into the storage layer—is applied to all of the unselected word lines during the programming operation. *Id.*, 44-46. Additionally, because the selected word line that receives the high programming voltage (V_{pgm}) also intersects many other memory strings, an “inhibit” voltage is traditionally applied to the bit lines for those other unselected memory strings. *Id.*, 46. Applying an “inhibit” voltage to bit lines of the unselected memory string (as opposed to the 0V value used on the selected memory string that contains the cell being programmed) results in a smaller voltage difference between the gate terminal and channel of each memory cell, which helps prevent the memory cells on the unselected memory strings from being inadvertently programmed during the programming operation. *Id.*

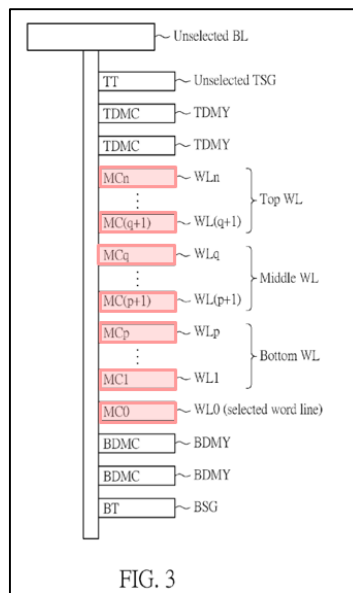
33. But as explained by the ’822 Patent, the effects of programming disturb can be exacerbated as the number of vertical layers in the device, and the overall bit density of the device, increases. ’822 Patent, 1:32-33. As was understood in the art, programming disturb (or program disturb) is an undesirable phenomenon that occurs when a program operation on a selected memory cell inadvertently changes the programmed state of adjacent memory cells that share the same word line or the same bit line as the selected memory cell—thus causing data corruption and reducing the overall reliability and integrity of the data stored with the device. *See, e.g.*, Ex. 1006 (“Aritome”) at 52 (generally describing program disturb); Ex. 1007 (“Brown”) at 239 (same); Ex. 1008 (“Cappelletti”) at 32-33 (same).

34. As explained by the '822 Patent, unwanted programming disturb can be mitigated by employing a pre-charging process to “remove boosting charges (electrons) of the unselected memory string.” '822 Patent, 1:32-38. But the methods at the time had difficulty removing electrons in the “bottom of the channel,” particularly as the number of layers in the device was increased. '822 Patent, 1:38-41. Moreover, the typical approaches for addressing this issue—such as using larger voltage levels or extending the pre-pulse time—would result in longer overall programming times (e.g., as a result of extended pre-pulse times) or increased the risk of transistor breakdown (e.g., as a result of using larger voltages than otherwise necessary). '822 Patent, 1:38-48. By comparison, the inventors of the '822 Patent were able to avoid the drawbacks of earlier methods by developing an improved type of pre-charging operation that was able to mitigate the effects of programming disturb in memory devices without resorting to extending charging times or large voltages used in earlier approaches. '822 Patent, 1:48-55.

35. Specifically, the new approach described in the '822 Patent mitigates program disturb in non-volatile memory devices by applying multiple pre-pulse signals with increasingly large voltage levels to successive groups of memory device word lines. This is done by grouping the word lines within the memory string, and then applying increasingly larger pre-charging voltages to each of those different groups. For example, as shown in Figure 3 below, a non-volatile memory device

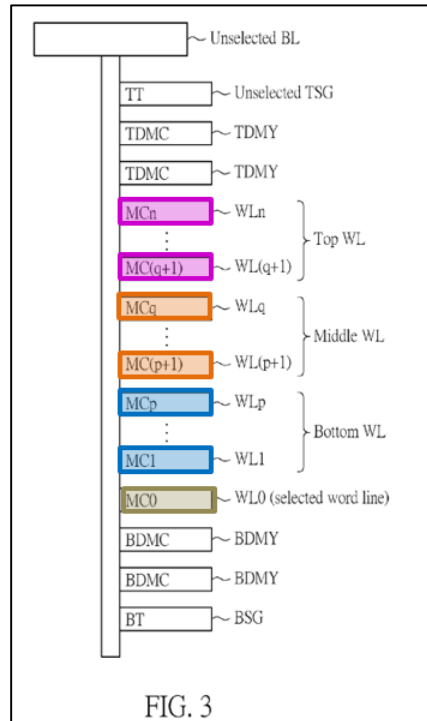
may be formed by a plurality of memory strings with each memory string including: a top select gate transistor (“TSG”) that can be turned on-and-off to control when the memory string is connected to the bit line (“BL”), at least one top dummy memory cell (“TDMY”) and one bottom dummy memory cell (“BDMY”) that are not configured to store data but are instead used to electrically isolate portions of the memory string from the rest of the memory device, a plurality of memory cells arranged in series that are “configured to store data,” and a bottom select transistor (“BSG”) that can be turned on-and-off to control when the memory string is connected to a source line. ’822 Patent, 3:6-9, 3:18-19. In general, the memory cells that form the memory string are arranged in series “between the top dummy memory cell and the bottom dummy memory cell.” ’822 Patent, 3:23-26. The gate terminal of each memory cell is then connected to a **word line (“WL”)** that can be used to control the voltage applied to the gate terminal of each of the corresponding memory cells within the string. ’822 Patent, 3:20-23, 3:26-29.¹

¹ All emphasis and annotations have been added, unless otherwise noted.



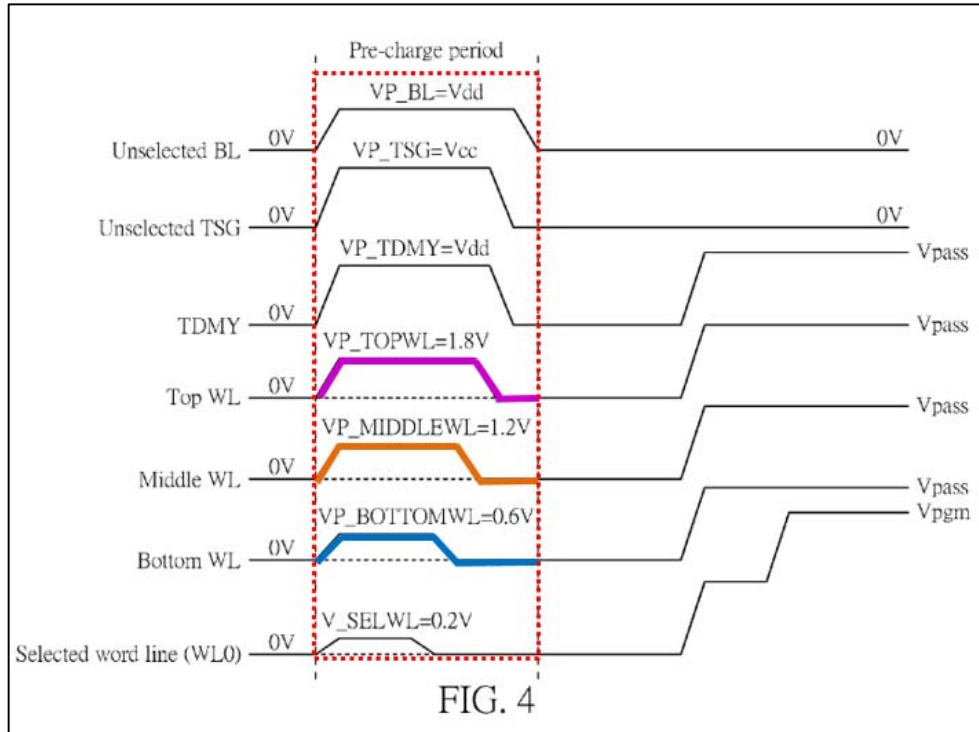
36. To control the voltages applied “during a pre-charge period” that occurs “before programming,” the ’822 Patent teaches using a “control circuit” to apply “word line pre-pulse signals” to the word lines “disposed between the selected word line and the top dummy word line TDMY (or the top select gate TSG).” ’822 Patent, 3:43-46, 3:55-59. That is, in the particular arrangement illustrated in Figure 3, the ’822 Patent teaches applying the pre-charging operation to word lines on the drain side of the selected memory cell (i.e., the portion of the memory string illustrated **above** the selected word line) closer to the TDMY or TSG where the memory string connects to the bit line. In some embodiments, the control circuitry can also be configured to apply a “dummy word line pre-pulse signal” to “top dummy word lines TDMY” and “bottom dummy word lines BDMY” during the pre-charging period. ’822 Patent, 3:59-65. For example, as shown in Fig. 3 below, once a word line has been selected for programming, the various word lines disposed between the

selected word line and TDMY (or the TSG) may be “divided into multiple groups of ... word lines”: a “**first group of word lines**” including word line WL1 through word line WL_p, a “**second group of word lines**” including word line WL(_p+1) through word line WL_q, and a “**third group of word lines**” including word line WL(_q+1) through word line WL_n. ’822 Patent, 4:66-5:2, 5:18-34.



37. During the “pre-charge period,” three different word line pre-pulse signals with incrementally increasing voltage levels are then applied to the three different groups of word lines. For example, in the embodiment illustrated in Fig. 4, a **first word line pre-pulse signal** VP_BOTTOMWL is applied to the first group of word lines (“Bottom WL”), a **second word line pre-pulse signal** VP_MIDDLEWL is applied to the second group of word lines (“Middle WL”), and

a third word line pre-pulse signal VP_TOPWL is applied to the third group of word lines (“Top WL”) during the **pre-charge period** that occurs prior to a programming step. ’822 Patent, 5:50-55.



38. As shown in Fig. 4, the word line pre-pulse signals applied to the different groups have incrementally increasing voltage levels, with the VP_BOTTOMWL signal having the lowest voltage level (rising to 0.6 volts before falling back down to 0 volts), VP_MIDDLEWL having an intermediary voltage level (rising to 1.2 volts before falling back down to 0 volts), and VP_TOPWL having the highest voltage level (rising to 1.8 volts before falling back down to 0 volts). ’822 Patent, 5:65-6:4. In the embodiment illustrated in Fig. 4, a top dummy word line pre-pulse signal, VP_TDMY, that is applied to the dummy word lines has

a separate voltage level (Vdd) that is greater than the voltage levels for VP_TOPWL (0.6 volts), VP_MIDDLEWL (1.2 volts) and VP_BOTTOMWL (1.8 volts). '822 Patent, 6:4-8. Similarly, as illustrated in Fig. 4, the pre-pulse signal for the selected word line, V_SELWL, has a voltage level (0.2 volts) that is lower than the voltage levels for VP_TOPWL (0.6 volts), VP_MIDDLEWL (1.2 volts) and VP_BOTTOMWL (1.8 volts). '822 Patent, Fig. 4, 5:62-64.

39. As explained by the '822 Patent, by supplying different pre-pulse voltages with incrementally increasing voltage levels to the word lines disposed between the selected word line and the top select gate, the channel potential gradient is enhanced, which improves the overall distribution and movement of channel-trapped electrons, and thus prevents unwanted electrons from accelerating into unselected memory cells and causing programming disturb during a programming operation. See '822 Patent, 7:37-47. Additionally, by using multiple pre-pulse signals to create a channel potential gradient and thus mitigate programming disturb, the '822 Patent achieves faster programming time and less risk of transistor breakdown phenomenon as compared to conventional systems by reducing the overall duration of the pre-charge period and enabling smaller overall voltage levels to be used for the pre-charging process. See '822 Patent, 1:41-48. Accordingly, the claimed pre-charging process described in the '822 Patent provides significant advantages over previous types of pre-charging methods that, for example, resorted

to larger voltages or longer pre-charging times in order to remove electrons stuck at the bottom of the channel. See '822 Patent, 1:38-48.

B. Listing of the Challenged Claims

40. For reference, claims 1-9 and 11-19 of the '822 Patent are reproduced below:

[1.pre] A memory device, comprising:

[1.a] a plurality of memory strings;

[1.b] a bit line connected to a first memory string of the plurality of memory strings;

[1.c] a select gate line connected to the first memory string of the plurality of memory strings;

[1.d] a selected word line of a plurality of word lines, wherein the plurality of word lines is connected to the first memory string; and

[1.e] a control circuit configured to:

[1.e.1] apply a first word line pre-pulse signal of a plurality of word line pre-pulse signals to a first group of the plurality of word lines during a pre-charge period;

[1.e.2] apply a second word line pre-pulse signal of the plurality of word line pre-pulse signals to a second group of the plurality of word lines during the pre-charge period; and

[1.e.3] apply a third word line pre-pulse signal of the plurality of word lines pre-pulse signals to a third group of the plurality of word lines during the pre-charge period,

[1.e.4] wherein a voltage level of the second word line pre-pulse signal is greater than that of the first word line pre-

pulse signal, and a voltage level of the third word line pre-pulse signal is greater than that of the second word line pre-pulse signal.

2. The memory device of claim 1, wherein the first group of the plurality of word lines, the second group of the plurality of word lines, and the third group of the plurality of word lines are disposed in an order of distance from the selected word line of the plurality of word lines.
3. The memory device of claim 1, wherein the first group of the plurality of word lines are disposed adjacent to the selected word line, the second group of the plurality of word lines are disposed between the first group of the plurality of word lines and the select gate line, and the third group of the plurality of word lines are disposed between the second group of the plurality of word lines and the select gate line.
4. The memory device of claim 1, wherein the control circuit is configured to apply a bit line pre-pulse signal to the bit line during the pre-charge period.
5. The memory device of claim 4, wherein the first memory string is an unselected memory string, and the bit line is an unselected bit line.
6. The memory device of claim 1, wherein the control circuit is configured to apply a word line signal to the selected word line of the plurality of word lines.
7. The memory device of claim 1, wherein the control circuit is configured to apply a top dummy word line pre-pulse signal to a top dummy word line of the plurality of word lines during the pre-charge period.
8. The memory device of claim 7, wherein a voltage level of the top dummy word line pre-pulse signal is greater than that of the third word line pre-pulse signal.
9. The memory device of claim 1, wherein the voltage levels of the first word line pre-pulse signal, the second word line pre-pulse signal, and the third word line pre-pulse signal are positive.

[11.pre] A method of controlling a memory device, the memory device comprising a plurality of memory strings, a bit line connected to a first memory string of the plurality of memory strings, a select gate line connected the first memory string of the plurality of memory strings, a selected word line of a plurality of word lines, wherein the plurality of word lines is connected to the first memory string, the method comprising:

[11.a] applying a word line signal to the selected word line of the plurality of word lines connected to the first memory string of the plurality of memory strings during a pre-charge period;

[11.b] applying a first word line pre-pulse signal of a plurality of word line pre-pulse signals to a first group of the plurality of word lines during the pre-charge period;

[11.c] applying a second word line pre-pulse signal of the plurality of word line pre-pulse signals to a second group of the plurality of word lines during the pre-charge period; and

[11.d] applying a third word line pre-pulse signal of the plurality of word line pre-pulse signals to a third group of the plurality of word lines during the pre-charge period;

[11.e] wherein a voltage level of the second word line pre-pulse signal is greater than that of the first word line pre-pulse signal, and a voltage level of the third word line pre-pulse signal is greater than that of the second word line pre-pulse signal.

12. The method of claim 11, wherein the first group of the plurality of word lines, the second group of the plurality of word lines, and the third group of the plurality of word lines are disposed in an order of distance from the selected word line of the plurality of word lines.

13. The method of claim 11, wherein the first group of the plurality of word lines are disposed adjacent to the selected word line, the second group of the plurality of word lines are disposed between the first group of the plurality of word lines and the select gate line, and the third group of the plurality of word lines are disposed between the second group of the plurality of word lines and the select gate line.

14. The method of claim 11, further comprising applying a bit line pre-pulse signal to the bit line during the pre-charge period.

15. The method of claim 14, wherein the first memory string is an unselected memory string, and the bit line is an unselected bit line.

16. The method of claim 11, further comprising apply a top dummy word line pre-pulse signal to a top dummy word line of the plurality of word lines during the pre-charge period.

17. The method of claim 16, wherein a voltage level of the top dummy word line pre-pulse signal is greater than that of the third word line pre-pulse signal.

18. The method of claim 16, wherein the top dummy word line is disposed between the third group of the plurality of word lines and the select gate line.

19. The method of claim 11, wherein the voltage levels of the first word line pre-pulse signal, the second word line pre-pulse signal, and the third word line pre-pulse signal are positive.

VII. LEVEL OF ORDINARY SKILL IN THE ART

41. My opinions in this declaration are based on the understandings of a person of ordinary skill in the art, which I understand is sometimes referred to as an “ordinary artisan” or by the acronyms “POSITA” (person of ordinary skill in the art) or “POSA,” as of the time of the invention.

42. I have been asked to consider the level of ordinary skill that someone in the field of technology of the '822 Patent would have had at the time the claimed invention disclosed in the '822 Patent was made. In determining the level of ordinary skill in the art, I considered the following: (1) the levels of education and

experience of persons working in the field; (2) the types of problems encountered in the field; and (3) the sophistication of the technology.

43. In my opinion, a person of ordinary skill in the art capable of reading and understanding the claims of the '822 Patent at the time of the invention would have had at least a bachelor's degree in electrical engineering, computer engineering, or a similar discipline, along with at least 2 years of professional experience with semiconductor memory devices, or an equivalent level of knowledge and experience. For example, an advanced degree may replace some of the professional experience, or extensive experience may replace some of the educational requirements.

44. In this case, Dr. Liu has asserted in his declaration that a person of ordinary skill in the art at the time of the invention described in the '822 Patent would have a:

bachelor's degree in electrical engineering or a similar discipline, along with 2-3 years of professional experience working with (e.g., researching, designing, or teaching) NAND flash memory devices (including issues relating to the operation, e.g., programming, of said devices), or an equivalent level of skill, knowledge, and experience (e.g., an advanced degree may replace some of the professional experience).

Liu ¶37.

45. In view of my educational background and years of experience, including my many years of experience developing NAND Flash architecture, I both

met and exceeded the qualifications of a person of ordinary skill in the art as of the earliest possible priority date of the '822 Patent in October 2019. That is true under both my own definition of a POSITA, as well as under Dr. Liu's definition, and my opinions as set forth herein are the same regardless of which definition of a person of ordinary skill in the art is applied.

VIII. CLAIM INTERPRETATION FOR THE '822 PATENT

46. As discussed below, I understand that Patent Owner has proposed the terms: (1) "word line pre-pulse signal," and (2) "disposed in an order of distance from the selected word line" / "disposed adjacent to the selected word line" for construction. I also understand that Petitioner did not identify any proposed claim constructions in the Petition, but has proposed certain terms for construction in the parallel district court proceeding. I have applied Patent Owner's constructions in rendering my opinions, but my opinions would not change if the claims were instead interpreted in accordance with their ordinary and customary meaning as understood by a person of skill in the art at the time of the invention.

A. "Word Line Pre-Pulse Signal" (All Claims)

47. I have been informed that Patent Owner construes the term "word line pre-pulse signal" as a "pulse signal to prepare word lines for a programming step" wherein a "pulse" is a "signal that must increase in value and then decrease in value (or vice versa)." That construction is consistent with the way the term is used in the

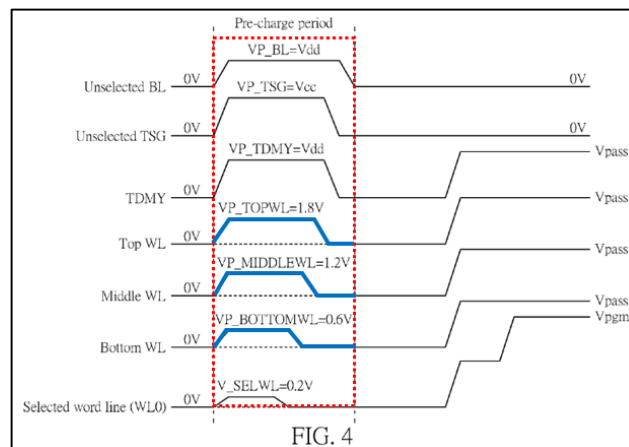
'822 Patent specification, and the customary and ordinary meaning of the term “pulse.” I have applied that construction in rendering my opinions, but my opinions would not change if I instead applied the ordinary and customary meaning.

48. Various portions of the '822 Patent support Patent Owner's proposed construction of the term “word line pre-pulse signal,” and confirm that the term refers to pulse signals that are used for preparing word lines for a programming step. At the outset, the claim 1 recites applying a “word line pre-pulse signal ... during a pre-charge period.” '822 Patent, 3:43. As explained by the '822 Patent, the pre-charge period occurs “before programming” and is used to prepare for the subsequent programming step. '822 Patent, 3:43. Additionally, the '822 Patent explains that each “word line pre-pulse signal” is a pulse with a “pulse duration,” which is further confirmed by dependent claim 20 reciting a “**pulse duration** of the second word line pre-pulse signal is greater than that of the first word line pre-pulse signal.” See '822 Patent, 7:19-36, claim 20.

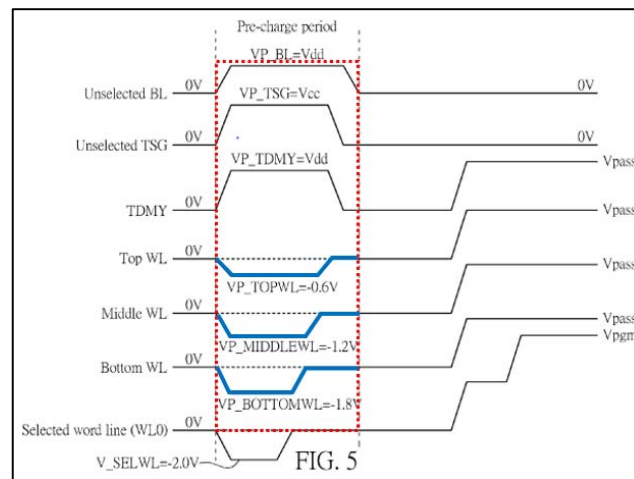
49. All of the embodiments in the '822 Patent also support Patent Owner's proposed construction. Indeed, the specification states that the “word line pre-pulse signals” illustrated in Fig. 4 are all “positive pulse signals,” and that the signals illustrated in Fig. 5 are all “negative pulse signals.” See '822 Patent, 6:11-19, 6:61-66, Figs. 4-5 (depicting each of the word line pre-pulse signals as pulses during the pre-charging period). Each of those signals are also described as having a “pulse

duration” within the pre-charge period, and has the effect of reducing programming disturb. *See* ’822 Patent, 7:19-36 (describing pulse duration); *see also* ’822 Patent 1:15-19 (“applying word line pre-pulse signals” is for “reducing programming disturb”), 3:43-46 (the “pre-charge period” is “before programming”).

50. In addition to confirming that each of the word line pre-pulse signals is a type of pulse, the specification also confirms that—at minimum—each pulse must increase in value and then decrease in value (or vice-versa). For example, as shown in Fig. 4, each of the illustrated “word line pre-pulse signals” is depicted as a “positive pulse” that first increases in value to a fixed level before then decreasing in value during the pre-charge period.



’822 Patent, 6:61-7:6, Fig. 4. Similarly, as shown in Fig. 5, each of the illustrated “word line pre-pulse signals” is depicted as a “negative pulse” that first decreases in value to a fixed level before increasing in value during the pre-charge period.



'822 Patent, 7:6-18, Fig. 5. Each of the “word line pre-pulse signals” shown in Fig. 4 and Fig. 5 are thus “pulses” that increase in value and then decrease in value (or vice-versa) during the pre-charge period, and each one is also described as having a corresponding “pulse duration,” to describe the time between the beginning and the end of the corresponding pulse. See '822 Patent, 7:19-36, Figs. 4-5.

51. The fact that a “pulse” must increase in value and then decrease in value (or vice versa) is also consistent with the plain and ordinary meaning of the term, as confirmed by dictionary definitions of the term “pulse.” I have been informed that the dictionary definitions for the term pulse found in Exs. 2012-2014 were cited by Micron in support of its proposed claim construction of the term “word line pre-pulse signal” in the parallel district court proceeding. Each of those definitions confirms that a “pulse” must, at minimum, include some type of rise and fall in order to qualify as a “pulse.” See *e.g.*, Ex. 2012 (Pulse, Wiley Electrical and Electronics Engineering Dictionary (2004)) (“a well defined variation which increases from a

steady value to a maximum, ***then back to or near the original value***, all in a comparatively short time); Ex. 2013 (Pulse, IEEE Standard Dictionary 1996) (“[a] wave that departs from an initial level for a limited duration of time ***and ultimately returns*** to the original level”); Ex. 2014 (Pulse, Webster's II New College Dictionary – 2001) (“A transient amplification or intensification of a characterization ... of a wave characteristic, ***followed by return*** to equilibrium or steady state”); *see also* Ex. 2015 (Micron’s Preliminary Claim Constructions) at 4-5 (listing materials cited by Micron regarding its proposed construction of “word line pre-pulse signal”).

52. In the Decision to Institute (DI), the Board has observed that the Petitioner “applies its teaching with the same understanding of pre-pulse signal as the Patent Owner,” and that both parties recognized that the term “word line pre-pulse signal” required a pulse signal used to prepare word lines for a programming step. *See* DI at 7. I have been informed that in the parallel district court proceeding, the Petitioner proposed that the term “word line pre-pulse signal” should be construed as a “signal that increases in value and then decreases in value (or vice versa) before a programming step.” *See* Ex. 2015 at 4. That construction further confirms that Petitioner believes that: (1) the claimed “word line pre-pulse signal” is a form of pulse; and (2) at minimum a pulse signal needs to increase in value and then decrease in value (or vice-versa).

53. It also appears that, during his deposition, Petitioner’s expert Dr. Liu said he didn’t know how to define the term “pulse.” For example, in response to the question “What is a pulse?” Dr. Liu responded that “I don’t know. I’m not here to define the pulse....” Ex. 2021 (“Liu Tr”) at 25:19-25. Similarly, Dr. Liu refused to comment on whether the example waveforms shown in Ex. 2020 (charting voltage versus time for various sample waveforms) could qualify as a pulse. *See generally* Liu Tr. 29:14-62:3 (refusing to answer questions concerning the waveforms shown in Ex. 2020); *see also id.* 39:7-25 (refusing to comment on whether example waveforms in Ex. 2020 constitute a pulse), 41:3-44:25, 44:7-25 (refusing to answer any questions concerning Ex. 2020; “...are you willing to answer any of my questions about this document? No”), 45:1-46:2 (refusing to answer outside the context of the ’822), 57:23-62:3 (refusing to answer whether a waveform would constitute a pulse if the waveform appeared as part of Figure 4 of the ’822).

54. I have not been asked to render an opinion on the precise scope of the term pulse, beyond the fact that a pulse signal “must increase in value and then decrease in value (or vice versa).” As I discuss in greater detail in Sections X-XIII, under that construction Petitioner’s Grounds based on Lee, Zhao, and Yang fail to disclose or render obvious any of the Challenged Claims. However, my opinions as to the Grounds raised in the Petition do not depend on this particular construction,

and would be the same even if the claims were construed in accordance with their ordinary and customary meaning in view of the patent specification.

**B. “Disposed in an Order of Distance from the Selected Word Line”
(Claims 2, 12) / “Disposed Adjacent to the Selected Word Line”
(Claims 3, 13)**

55. Petitioner’s Grounds based on Lee, Zhao, and Yang fail to disclose or render obvious the limitations of independent claims 1 and 11, and thus fail to disclose or render obvious any of the Challenged Claims. I have been informed that, to the extent it is necessary for the Board to determine if the added limitations of dependent claims 2 and 12 are disclosed or rendered obvious, Patent Owner argues that the plain and ordinary meaning of the term “disposed in an order of distance from the selected word line” to require that the word line groups be disposed in order based on the location of the selected word line. Similarly, as used in claims 3 and 13, Patent Owner argues that the plain and ordinary meaning of the term “the first group of the plurality of word lines are disposed adjacent to the selected word line” to require that group to be disposed adjacent to the location of the selected word line. Under those constructions, it is my opinion that claims 2-3 and 12-13 are not satisfied by Lee or Yang, each of which disclose the use of predetermined groups that remain the same regardless of where the selected word line is located. Specifically, the claims are not satisfied by predetermined word line “groups” that do not change with the location of the selected word line. Such an interpretation, which is implicit in

Petitioner's mappings for at least Grounds 1 and 4, ignores the ordinary and customary meaning of the word "disposed."

56. Various portions of the '822 Patent specification support Patent Owner's proposed construction. For example, as described by the '822 Patent, once a word line (e.g., WL0) is chosen as the selected word line, "the word lines WL1 to WLn are divided into a first group of word lines (Bottom WL), a second group of word lines (Middle WL) and a third group of word lines (Top WL)." '822 Patent, 5:18-22. *See also* '822 Patent, 5:24-34 ("The first group of word lines (Bottom WL) is between the selected word line (word line WL0) and the second group of word lines (Middle WL)").

57. Patent Owner's proposed construction is also consistent with the ordinary and customary meaning of the term "disposed." For example, dictionary definitions of the term "disposed" require items to be "arrange[d] in a particular position" or to be "put in place." *See e.g.*, Ex. 2016 (Merriam Webster's Dictionary and Thesaurus 2014) ("put in place"); Ex. 2017 (Merriam Webster's Collegiate Dictionary 2012) (same); Ex. 2018 (American Heritage 2011) ("To place or set in a particular order; arrange"); Ex. 2019 (New Oxford American 2010) ("arrange in a particular position"). Accordingly, the ordinary and customary meaning of the term "disposed" further confirms that groups "***disposed in an order of distance from the selected word line***" must be arranged into position based on the location of that word

line. Similarly, a group that is “*disposed adjacent to the selected word line*” must be arranged into its position based on the location of that word line.

58. The fact that claims 2-3 and 12-13 require word line groups to be based on the location of the selected word line is also confirmed by Petitioner’s characterization of the claims in the Petition. Specifically, when summarizing the subject matter of the Challenged Claims, Petitioner stated that in “dependent claims 2-3 and 12-13” the claimed “groups” will be chosen based on the location of the “currently selected” word line that has been chosen for programming. Pet. 2.

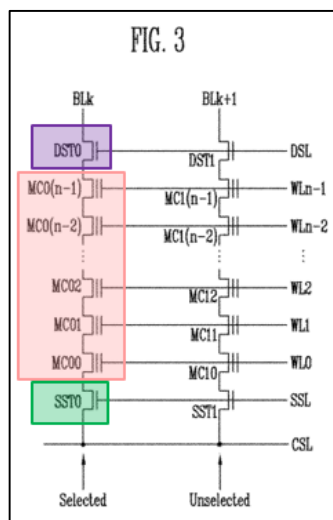
59. Accordingly, it is my opinion that Patent Owner’s proposed construction is consistent with the ’822 Patent specification, as well as the ordinary and customary meaning of the claim language. Specifically, as confirmed by plain meaning of the claims and the specification, the added limitations of dependent claims 2-3 and 12-13 require that the word line groups be disposed in order based on the location of the selected word line. Moreover, as I discuss in greater detail in Sections X.B, X.C, XIII.B, and XIII.C (discussing Ground 1 and 4), under those constructions Petitioner’s Grounds based on Lee and Yang fail to disclose or render obvious the added limitations of dependent claims 2-3 and 12-13.

IX. THE ASSERTED PRIOR ART

A. U.S. Patent No. 10,121,529 (“Lee”) (Exhibit 1004)

60. Lee was issued on November 6, 2018. For the purposes of my present analysis, I have been asked to assume that Lee is prior art to the ’822 Patent. I understand that the Petition argues that Lee renders obvious various claims of the ’822 Patent, but that the Petition does not argue that Lee actually anticipates any of the Challenged Claims. *See* Pet., 6, 26-41.

61. Lee’s summary section states that it is directed to “a semiconductor memory device configured to mitigate a program disturb phenomenon, and a method of operating the semiconductor memory device.” Lee, 1:53-56. For example, as shown in Fig. 3, Lee describes a typical memory device where memory cell strings include “a **source select transistor SST0**, **memory cells MC00 to MC0(n-1)**, and **a drain select transistor DST0**” arranged in a series.



Lee, 7:37-58, Fig. 3. Although Lee purports to mitigate program disturb, it does so in a very different manner than the '822 Patent. The '822 Patent mitigates program disturb resulting from “boosting charges” by using pre-pulse signals to create a “**channel potential gradient**” during a pre-charge period, thus removing unwanted charge. See '822 Patent, 1:20-48. By comparison, Lee states that it seeks to create a more “**uniformly formed precharge level** in the entirety of the cell string.” Lee, 7:58-62. According to Lee, the uniformly formed precharge is advantageous because a “typical” pre-charge operation will cause “a threshold voltage of a memory cell [to be] increased by a **resistance component** between the source select transistor and the drain select transistor,” which can reduce the pre-charge level in the memory cell. Lee, 8:25-52.

62. As explained by Lee, because “a threshold voltage of a memory cell is increased by a **resistance component** between the source select transistor and the drain select transistor” this means that the resulting “**precharge level** in a source select side channel is reduced.” Lee, 8:25-32. In other words, Lee is concerned with the voltage level at the “source select side” of the memory string channel being indirectly “reduced” as a result of a “resistance component” between the source select transistor and drain select transistor located at either end of each memory string. This reduction in voltage is a consequence of Ohm’s law (i.e., $V=I \cdot R$, voltage equals resistance-times-current), and will manifest whenever current is

running along the length of the memory string. Specifically, whenever there is current running from the drain select transistor to the source select transistor along the length of the memory string (e.g., as a result all of the transistors within the memory string being turned on), resistance along the length of the memory string will create a voltage drop across each of the memory cell transistors. This, in turn, can limit the degree to which the transistors are on during precharge, preventing the full “precharge level” being reached on the “source select side” of the channel (i.e. the portion closest to the source select transistor) and limiting the channel boosting in that portion of the channel. See Lee, 8:25-32. To address this issue and create a more uniform level of charge, Lee states that it will apply “different pre-bias voltages to the respective word line groups” along the entire length of the memory string based on the relative positions of the word lines. Lee, 2:63-3:7. For example, in a “memory block” that includes “thirty-two word lines WL0 to WL31,” Lee states that the system will determine “pre-bias voltages to be applied to the respective word lines WL0 to WL31 depending on a position of a word line coupled to the target memory cell to be programmed.” Lee, 8:3-17. Following that determination step, Lee states that “during a precharge process, the closer a word line group to which a word line belongs is to the drain select transistor, the higher a pre-bias voltage to be applied to the word line may be.” Lee, 8:18-52. As a consequence of applying pre-bias voltages to each of the word lines, Lee’s approach ensures that all of the

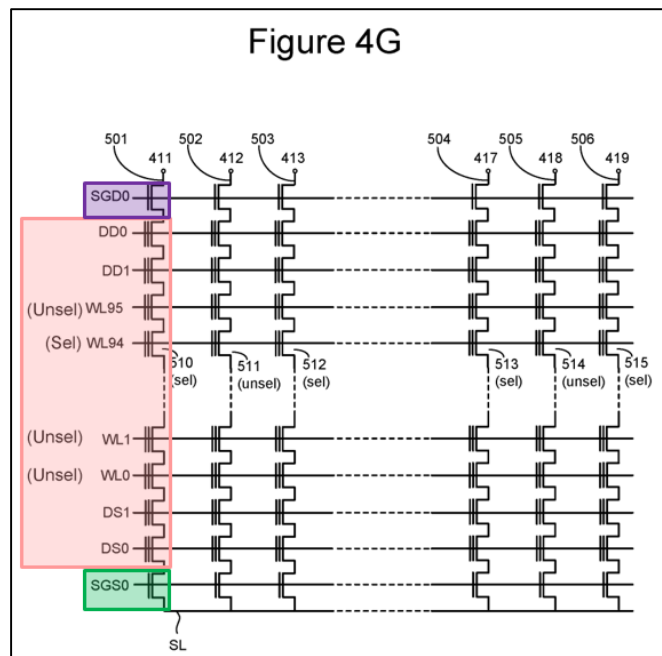
channels of the memory cells in the unselected NAND strings are fully turned on and development of the precharge is not inhibited. Lee, 8:18-52.

63. Lee does not include any signal diagrams, or provide any further details regarding the shape and timing of the specific “pre-bias” voltages that are used during the pre-charging process. At most, Lee states that “different” voltages are used for certain pre-bias voltages, with some of the voltages being applied to certain word lines being “higher” than others based on where they are positioned within the memory string relative to the selected word line. *See* Lee, 7:58-62, 8:65-9:6. As I explain further in relation to Petitioner’s proposed Grounds, there is nothing in Lee to suggest or otherwise render obvious that the “pre-bias” voltages are applied as “pulses” in particular, or that they would qualify as “word line pre-pulse signals” as required by the independent claims of the ’822 Patent. *See* Section X.A (discussing Petitioner’s Ground 1 arguments).

B. U.S. Patent No. 10,643,718 (“Zhao”) (Exhibit 1005)

64. Zhao was issued on May 5, 2020. For the purposes of my present analysis, I have been asked to assume that Zhao is prior art to the ’822 Patent. I understand that the Petition argues that Zhao (or Zhao in view of Lee) renders obvious various claims of the ’822 Patent, but that the Petition does not argue that Zhao actually anticipates any of the Challenged Claims. *See* Pet., 44-71.

65. As illustrated in Figure 4G, the structure of Zhao's memory device is based on "vertical NAND strings with charge-trapping material" that "includes **memory cells** connected by a channel." Zhao, 6:34-46. Each "NAND string" is made up of multiple **memory cells** connected in series between a drain side select transistor controlled by a "[d]rain side selection line" and a source side select transistor controlled by "[s]ource side selection line." These selection lines are used to select which blocks of the NAND strings to interact with for memory operations. Zhao, 9:10-18, 11:53-12:13. Each NAND string is connected to a bit line through its drain side selection transistor and to a source line (SL) through its source side selection transistor. Each **memory cell** in a NAND string is connected to a word line, and during a memory operation (e.g., a programming or reading operation) there will be a "selected memory cell" on a "selected NAND string" that is being operated on, "unselected memory cells" on the selected NAND string, as well as unselected NAND strings. Zhao, 12:14-41, 27:30-48.



66. Zhao addresses the phenomenon of “program disturb” in memory systems, which it characterizes as “the unintended programming of one or more locations in a memory while performing a programming process for other locations in the memory.” Zhao, 2:10-14. Specifically, Zhao discusses one potential source of program disturb that “can result from electrons trapped in the channel being accelerated from one side of a selected word line to another side of the selected word line and redirected into the selected word line.” Zhao, 2:14-18. To address this source of program disturb, Zhao states that “countermeasures are proposed to open the channel from one side of a selected word line to the other side of the selected word line.” Zhao, 2:10-26. In other words, Zhao’s techniques are intended to create an even distribution of charges in the area surrounding the selected word line by

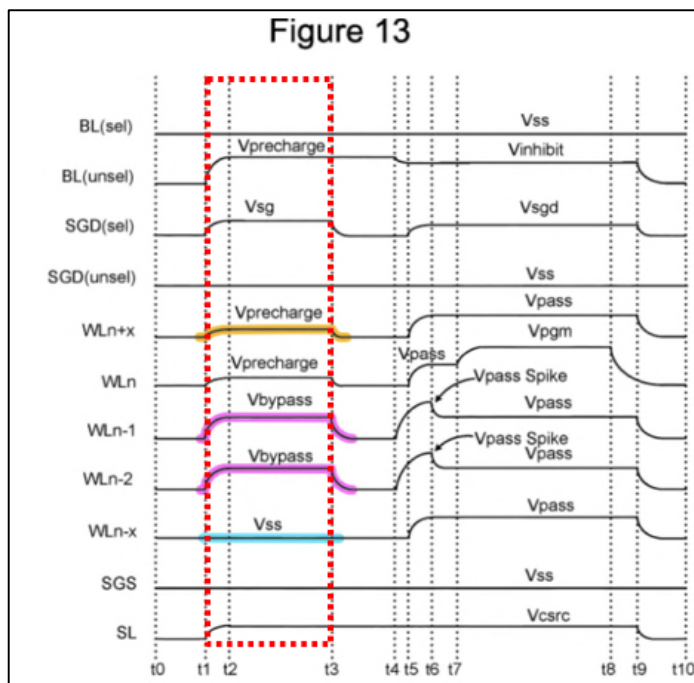
turning on the memory cell transistors driven by the selected word line prior to the program operation.

67. To combat program disturb, Zhao describes three categories of possible countermeasures that take place at different points in the programming cycle. First, Zhao states that “[o]ne proposed countermeasure includes purging (cleaning/clearing the electrons from) the already programmed side of the channel during a pre-charge operation performed as part of the programming process.” Zhao, 2:27-49. Second, Zhao states that “[a]nother proposed countermeasure includes applying a voltage spike on one or more already programmed unselected word lines adjacent the selected word line during boosting of the not yet programmed side of the channel.” Zhao, 2:50-3:4. Finally, Zhao states that “[a]nother proposed countermeasure include delaying the ramping down of voltages of one or more already programmed unselected word lines adjacent the selected word line at the conclusion of a program verify process.” Zhao, 3:5:24. Of these techniques, only the first is performed during a precharge operation.

68. Figure 13 is a signal or timing diagram illustrating the different program disturb countermeasures disclosed by Zhao starting from time t_0 when “all the

depicted signals are at ... **0 volts (Vss)**.” Zhao, 22:34-41. As is relevant for the ’822

Patent, Zhao states the time period “from **t1-t3 corresponds to pre-charging.**” *Id.*²



69. As depicted in Figure 13, the **Vss**, **Vprecharge**, and **Vbypass** waveforms are applied to different sets of unselected word lines, which the Petitioner incorrectly attempts to characterize as “word line pre-pulse signals” applied during a “pre-charge period.” See Pet. 49-52. Specifically, a “**pre-charge voltage Vprecharge**” is applied to “the drain side unselected word lines WLn+x” (Zhao, 22:39-50) while “already programmed source side unselected word lines WLn-1 and WLn-2 are raised to a **bypass voltage Vbypass**” (Zhao, 22:50-60) and “[t]he

² I have reproduced the same annotations used by Petition and Dr. Liu for **Vprecharge**, **Vbypass**, and **Vss** (e.g., 0 v).

remaining source side unselected word lines WLn-x remain at **Vss (e.g., 0 v)**” (Zhao, 23:7-9). As the Board recognized in the Decision to Institute, this flat **Vss** voltage is not a “word line pre-pulse signal” under any reasonable interpretation, and would not satisfy either Petitioner’s or Patent Owner’s proposed claim constructions as discussed in Section VIII.A because it does not “increase[] in value and then decrease[] in value (or vice versa)” at any point. *See* DI at 19.

70. As explained by Zhao, this flat **Vss** voltage applied to the unselected source side word lines may be “0 volts” or another voltage level “too low to pre-charge and/or too low to turn on the memory cells in a highest data state.” Zhao, 19:22-26. But regardless of the precise value used, Zhao teaches that the word lines “remain” at that value throughout the t1-t3 period that corresponds to pre-charging. *See* Zhao, 22:34-43, 23:7-10. Contrary to what Petitioner seems to suggest, Zhao does not disclose or otherwise suggest that some other “low” voltage takes the place of **Vss** during the relevant t1-t3 time period. *See* Pet. 51. Moreover, there would be seemingly no purpose in replacing **Vss** with *another* low voltage “too low to pre-charge and/or too low to turn on the memory cells” because **Vss** is *already* low enough to keep the memory cells WLn-x turned off and prevent pre-charging. *See* Zhao, 19:22-26. Accordingly, Zhao fails to disclose or otherwise render obvious using three separate “word line pre-pulse signals” as required by the independent claims of the ’822 Patent.

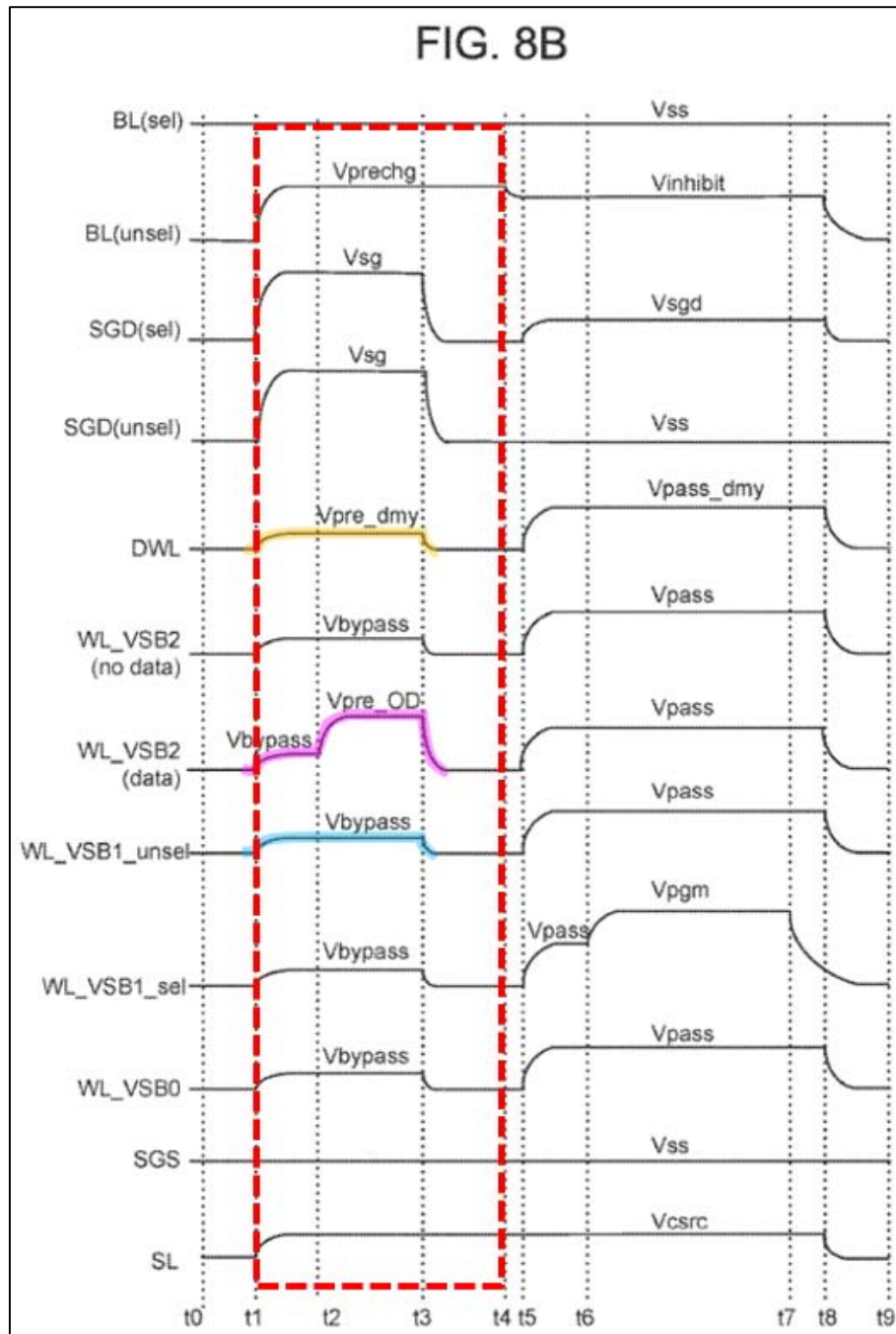
C. U.S. Patent No. 10,726,920 (“Yang”) (Exhibit 1010)

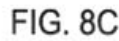
71. Yang was issued on July 28, 2020. For the purposes of my present analysis, I have been asked to assume that Yang is prior art to the ’822 Patent. I understand that the Petition argues that Yang renders obvious various claims of the ’822 Patent, but that the Petition does not argue that Yang actually anticipates any of the Challenged Claims. *See* Pet., 6, 71-89.

72. Yang states that it is able to prevent or reduce the effects of “program disturb,” which it describes as “the unintended programming of an unselected memory cell while performing a programming process for selected memory cells.” Yang, Abstract, 2:35-41. As explained by Yang, to prevent programming disturb, “boosting voltages” are applied to the channel of an unselected NAND string to “at least reduce program disturb of one or more memory cells coupled to the unselected NAND string.” Yang 2:42-62. As is typical for NAND memory devices, raising the voltage of the channel helps prevent unwanted programming because “the differential between the channel voltage (of the unselected memory cell) and the ... control gate of [the] unselected memory cell[] will be too small to allow for programming of the unselected memory cell.” Yang 25:65-26:3. However, if the channel is not “adequately pre-charged” prior to programming, the channel “may fail to boost to a sufficient voltage during the programming phase to adequately prevent program disturb.” Yang 2:42-62.

73. To address this purported problem, Yang describes a type of “pre-charge” operation that makes use of two different bias voltages on the unselected memory cells. Specifically, Yang states that “during a pre-charge phase of a programming operation, an overdrive voltage is applied to some memory cells and a bypass voltage is applied to other memory cells.” Yang 3:28-31. An example of these two different voltages being used is illustrated Figures 8B and 8C below. In general, Yang states that “times t1-t4” correspond to the “**pre-charge phase**.” 23:19-25. For “data word lines ... that are not programmed,” a “**bypass voltage**” (“**Vbypass**”) is applied, and by comparison, for “programmed word lines” a separate “**overdrive voltage**” (“**Vpre_OD**”) is applied from t2-t3. Yang 24:1-17, 24:28-46, 25:9-28. Yang also discloses “dummy” memory cell used to “electrically isolate” different sets of memory cells within the string receive a “**dummy pre-charge voltage**” (“**Vpre_dmy**”) during the pre-charge period. Yang, 12:35-43, 24:18-27.³

³ Petitioner’s annotations for **Vbypass**, **Vpre_dmy**, and **Vpre_OD** have been reproduced.





74. The Petition asserts WL8-WL11 receiving **Vbypass** is equivalent to the

argument is flawed. As recognized in the Decision to Institute, Yang does not disclose or otherwise render obvious that these are three distinct “word-line pre-pulse signals,” and the mapping presented in the Petition does not establish that “a voltage level of the second word line pre-pulse signal is greater than that of the first word line pre-pulse signal” (i.e., that **Vpre_dmy** is somehow greater than **Vbypass**) as required by the Challenged Claims. See DI 25. Rather, **Vbypass** and **Vpre_dmy** serve a similar purpose and are depicted in Yang as having *identical* values. There is nothing to suggest that different values would be used for **Vbypass** and **Vpre_dmy**, much less that **Vpre_dmy** in particular would be the larger of the two.

X. PETITIONER’S GROUND 1: LEE DOES NOT DISCLOSE OR RENDER OBVIOUS CLAIMS 1-3, 6, AND 11-13

75. Ground 1 of the Petition alleges that Lee renders obvious claims 1-3, 6, and 11-13.

76. As explained below in Section X.A, Lee does not disclose or render obvious the use of “word line pre-pulse signals” as required by limitations [1.e.1]-[1.e.3] of independent claim 1, or corresponding limitations [11.b]-[11.d] of independent claim 11. To the extent Lee discloses that different “pre-bias” voltages are applied to different groups of word lines, Lee does not disclose or render obvious that these voltages are applied in the form of “pulses,” nor would it have been obvious to modify Lee to apply the “pre-bias” voltages as pulses.

77. Additionally, as explained below in Sections X.B and X.C, Lee does not disclose or render obvious the added limitations of dependent claims 2-3 and 12-13 which require, among other things, that groups of word lines are “disposed” based on the location of the word line that has been selected for programming.

A. Independent Claims: Lee Does Not Disclose or Render Obvious a “[First/ Second/ Third] Word Line Pre-Pulse Signal” Applied “During a Pre-Charge Period” (Limitations [1.e.1]-[1.e.3] and [11.b]-[11.d])

78. Lee does not disclose or otherwise render obvious applying “word line pre-pulse signals” to different groups of word lines, as recited by limitations [1.e.1]-[1.e.3] and [11.b]-[11.d] of independent claims 1 and 11.

79. The term “word line pre-pulse signal” means a “pulse signal to prepare word lines for a programming step” wherein a “pulse” is a “signal that must increase in value and then decrease in value (or vice versa).” See Section VIII.A (claim construction of “word line pre-pulse signal”). The Petition attempts to characterize Lee’s pre-bias voltages as equivalent to the claimed “word line pre-pulse signals.” See Pet, 26-44. But Lee’s pre-bias voltages do not qualify as “word line pre-pulse signal[s]” because they are not formed as pulses, and they do not “increase in value and then decrease in value (or vice-versa)” during the relevant time period. Similarly, the Petition has failed to show that it would have been obvious to apply pulses instead of Lee’s pre-bias voltages, and Petitioner’s arguments to the contrary improperly try to conflate the claimed *pre-pulse* (or *pre-charge*) signals applied

during a pre-charge period with the subsequent **programming** voltages that are used when setting the value of a selected memory cell. Moreover, Lee's states that the intended purposes of the pre-bias voltages it to create a "uniform" pre-charge level throughout the channel of the memory string, which is consistent with the use of flat bias voltages that enable the voltage level in the memory string reach a single steady state value before being followed immediately by programming voltages. Lee, 7:58-62, 9:7-13, Fig. 7. By comparison, using a "pulse" in the context of Lee's system would, at best, needlessly extend the overall programming time, by necessarily including a falling edge of the "pulse" and a quiescent time between the precharge "pulse" and the start of the programming pulse.

80. Each of the Challenged Claims requires applying three different "word line pre-pulse signal[s]" to different groups of word lines. Specifically, independent claim 1 recites a control circuit configured to **"apply a first word line pre-pulse signal of a plurality of word line pre-pulse signals to a first group of the plurality of word lines** during a pre-charge period" (Element [1.e.1]); **"apply a second word line pre-pulse signal of the plurality of word line pre-pulse signals to a second group of the plurality of word lines** during the pre-charge period" (Element [1.e.2]); and **"apply a third word line pre-pulse signal of the plurality of word lines pre-pulse signals to a third group of the plurality of word lines** during the pre-charge period" (Element [1.e.3]). Similar limitations are also found in Elements

[11.b]-[11.d] of independent claim 11, and are also required by each of the '822 Patent dependent claims by virtue of their dependency on claims 1 and 11.

81. As I discussed above in Section VI, the '822 Patent mitigates programming disturb by applying multiple “word line pre-pulse signals” such that the “**channel potential gradient is therefore enhanced** ... thus enhancing the pre-charge effect of the unselected bit line and reducing programming disturb.” '822 Patent, 4:39-59; *see also id.* 7:37-47 (the disclosed use of word line pre-pulse signals will “**enhance potential gradient** ... thus enhancing the pre-charge effect”). As described by the '822 Patent, this can help mitigate programming disturb without using resorting to increased voltage levels or longer programming times. *See* '822 Patent 1:41-44. By comparison, Lee seeks to accomplish the opposite. Rather than creating a potential gradient, Lee seeks to have a “**uniformly formed**” level of charge throughout the channel of the memory string, and does so by compensating for a “resistance component between the source select transistor and the drain select transistor.” Lee, 7:58-62, 8:25-52.

82. To create this uniform level of charge, Lee discloses the use of “pre-bias” voltages, which Petitioner incorrectly tries to equate with the “pre-pulse signals ... during a pre-charge period” recited by independent claims 1 and 11 of the '822 Patent. As discussed in Section VIII.A, the term “word line pre-pulse signal” means a “pulse signal to prepare word lines for a programming step” wherein a “pulse” is

a “signal that must increase in value and then decrease in value (or vice versa).” But Lee does not disclose or render obvious that “pre-bias” voltages are formed as “pulses,” or would otherwise “increase in value and then decrease in value (or vice-versa).” In fact, Lee does not disclose any type of waveform or timing characteristics for the various “pre-bias” voltages. At most, Lee states that these voltages are used to create a “uniform precharge level,” which would suggest the bias voltages are applied as flat signals that enable the precharge level to reach a single steady-state value along the full length of the memory string before being followed immediately by programming voltages. *See* Lee 7:58-62, 9:7-13, Fig. 7.

83. The Petition presents two incorrect arguments for why a POSITA would have found it obvious to implement Lee’s “pre-bias voltages” in the form of “word line pre-pulse signals.” First, the Petition states that Lee’s voltages must be applied as pulses (or that it would have been obvious for them to be pulses) based on the combination of: (1) Lee supplying “pre-bias voltages in a separate and distinct-in-time step;” and (2) Lee’s pre-bias voltages will “differ from the later V_{pgm} and V_{pass} voltages” that are used in the subsequent programming step. Pet., 38-39. Second, the Petition argues that it would have been obvious to replace Lee’s bias voltages with pulses because pulses were commonly used in programming operations. Both arguments are incorrect.

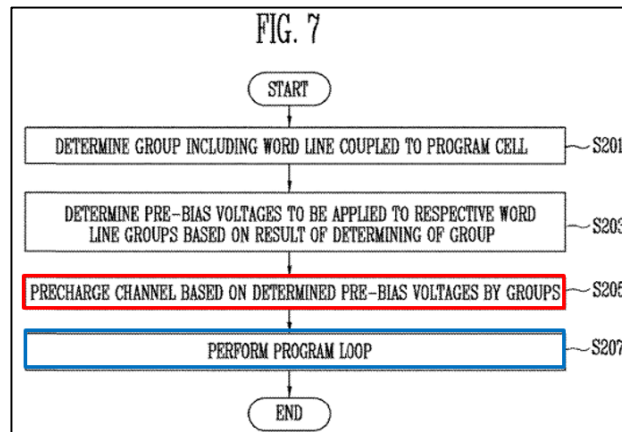
84. **Petitioner's First Argument:** Taking Petitioner's first argument, the facts being highlighted in the Petition do not require (or otherwise suggest) that voltages are being applied in the form of pulses. Lee does not disclose the waveform or timing characteristics of the "pre-bias" voltages, and there is nothing in Lee to suggest that those voltages would be supplied in the form of "pulses." In fact, the criteria set out on the Petition (i.e., that the signal occurs in a distinct time step, and that it has a value that differs from some later voltages), could be satisfied by any number of signals (e.g., a flat signal followed by a ramping voltage, a non-linear function shaped like a charging capacitor, a monotonically-increasing staircase function, etc.), and there is nothing to suggest that it requires the use of a "pulse" in particular. Moreover, given Lee's stated goal of creating a "uniform precharge level," it would be advantageous to apply bias voltages as flat signals that remain constant throughout the entire pre-charge period—thus encouraging the precharge level to reach a "uniform" steady-state value—before being followed immediately by programming voltages. See Lee 7:58-62, 9:7-13, Fig. 7. In the context of Lee's system and stated goals, the temporal gap between a precharge pulse and the start of the programming phase extends the time needed to complete the programming operation, which disadvantageously reduces device throughput and slows the overall device operation.

85. Dr. Liu incorrectly interprets Lee as somehow disclosing that the pre-bias voltages are cycled on-and-off prior to programming, but Lee says no such thing. See Liu ¶203. Specifically, in the Decision to Institute, the Board credited Dr. Liu’s mischaracterization of Lee as disclosing “on-off pre-bias voltages” that are cycled on and off. See DI 10-11, citing Liu ¶203. In relevant part, Dr. Liu’s declaration asserts—without any citation to Lee itself—that Lee’s pre-bias voltages are “**removed prior to commencing the program loop,**” and are thus “on-off” voltages that form the shape of a pulse. See Liu ¶203. That characterization has no support in Lee itself, and Lee makes no mention of cycling off the pre-bias voltages prior to programming. Indeed, neither Lee nor Dr. Liu articulate any advantage to applying the precharge voltages as a pulse, given Lee’s stated goals of creating a “**uniform pre-charge level in the entirety of the cell string**” prior to programming, and would extend the time required to perform the overall programming operation. See Lee 7:58-62, 9:7-13, Fig. 7. Instead, Lee teaches that the pre-charge voltages are followed immediately by programming voltages (i.e., there is no intermediary period where the pre-charge voltages get removed or replaced prior to programming). Specifically, Lee states:

After the pre-bias voltage is applied to the respective word lines and the precharge operation is completed, ***a program voltage may be applied to the selected word line WL10, and a pass voltage may be applied to unselected word lines WL0 to WL9 and WL11 to WL31.*** The above-

mentioned operation is a program loop for memory cells,
and the program loop may be repeatedly performed.

Lee, 9:7-13. This can also be seen in Figure 7 of Lee, which show that the
“**Precharge Channel**” step is followed immediately by the start of the “**Program
Loop**,” with no intermediary period between them.



Lee, Fig. 7.

86. At no point does Lee describe or otherwise render obvious that the pre-bias voltages are cycled on-and-off in the form of precharge pulses, nor would cycling those bias voltages on-and-off serve to create a more “uniform pre-charge level.” Nor does Lee disclose or render obvious any other voltages used during the precharge operation that “increase in value and then decrease in value (or vice versa)” as required by the claimed “word line pre-pulse signal.” See Section VIII.A (Claim Construction).

87. **Petitioner’s Second Argument:** Petitioner’s second argument incorrectly asserts that it would have nonetheless been obvious to implement Lee’s pre-bias voltages as pulses. Specifically, Petitioner and Dr. Liu argue that “when the ’822 Patent was filed, programming voltages were conventionally provided in the form of a ‘pulse,’” and as a result, they incorrectly infer that Lee’s “pre-bias voltages ... obviously would be supplied as pulses” as well. See Pet., 39; see also Liu Dec. ¶¶ 204-205. That argument is misguided, and improperly conflates **programming voltages** with the preparatory **pre-pulse** (or **pre-charge**) signals that would be applied during a pre-charge period. The ’822 Patent discloses that a pre-charge period is used to remove boosting charges **before** a subsequent programming operation. See ’822 Patent, 1:34-41, 3:43-46 (signals are applied in “**a pre-charge period (before programming)**”) (emphasis added); see also *id.* 3:50-65 (describing the various signals applied in a pre-charging period). The Petition identifies examples of various programming pulses supposedly known in the art, but those identified voltages have no relationship to the waveforms that would be used in a “pre-charging” operation, and serve a different purpose entirely. See Pet., 39; Liu Dec. ¶¶ 204-205 (citing Aitome (Ex. 1006) at 44, 116-117, 142-143 (discussing “applying high-voltage, V_{pgm} ” for “programming pulses”); Cappelletti (Ex. 1008) at 354 (a “[p]rogram [p]ulse” is provided to program a “selected cell”)). In every case, the voltages being identified are part of a programming step to set the value of a

memory cell, which has no relation to the voltages that might be used during a “pre-charging” operation. See Aitome (Ex. 1006) at 44, 116-117, 142-143; Cappelletti (Ex. 1008) at 354. Indeed, none of the cited portions of the Aritome or Cappelletti background references discloses “pulses” being used during a pre-charging period, nor has Dr. Liu provided a reason why using pulses in a programming step would necessitate (or otherwise render obvious) modifying Lee to use similarly shaped pulses during a pre-charging step. Indeed, Lee teaches creating a “uniform precharge level” using a pre-charge operation which is followed immediately by applying programming voltages. See Lee 7:58-62, 9:7-13, Fig. 7. The most efficient approach is applying flat signals that remain constant throughout the entire pre-charge period, followed directly by programming pulses. Using transient pulses does not create a more “uniform precharge level” in the context of Lees system, and would, at best, introduce time inefficiencies by requiring a longer total time to perform the programming operation. Accordingly, even assuming that “pulses” were commonly used for subsequent programming operations (e.g., to set the value of a selected memory cell), a POSITA would not have been motivated to modify Lee to use similarly shaped “pulses” for the bias voltages used during a recharging operation.

88. For at least the reasons above, Lee does not disclose or render obvious the use of “word line pre-pulse signals” as required by independent claims 1 and 11.

For at least the same reasons, Lee does not disclose or render obvious the limitations of dependent claims 2-3, 6, and 12-13.

B. Claims 2 and 12: Lee Does Not Disclose or Render Obvious Groups “Disposed in an Order of Distance from the Selected Word Line”

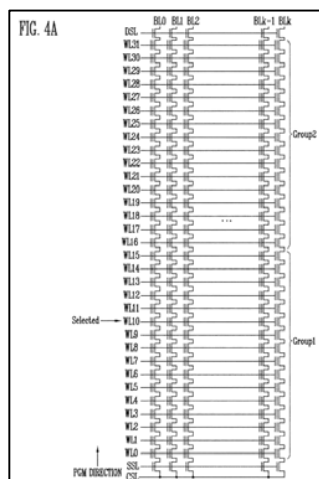
89. Lee does not disclose or otherwise render obvious groups of word lines “disposed in an order of distance from the selected word line” as recited by dependent claims 2 and 12. Instead, Lee discloses that groups of word lines are set in predetermined locations that do not change based on the location of the selected word line.

90. Dependent claim 2 recites: “The memory device of claim 1, wherein the first group of the plurality of word lines, the second group of the plurality of word lines, and the third group of the plurality of word lines ***are disposed in an order of distance from the selected word line*** of the plurality of word lines.” Similar limitations are also found in dependent claim 12.

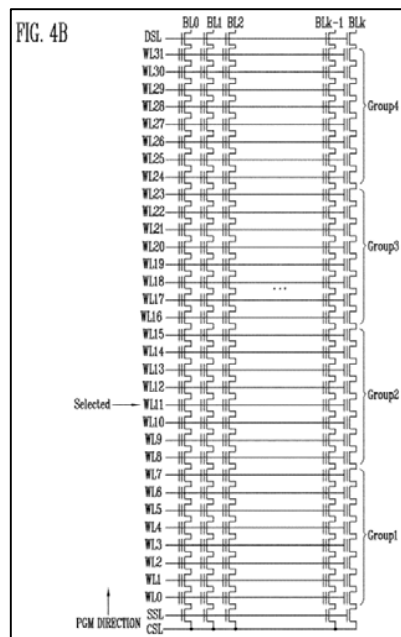
91. The term “disposed in an order of distance from the selected word line” requires that the word line groups be disposed in order based on the location of the selected word line. See Section VIII.B (Claim Construction). That interpretation is consistent with the plain and ordinary meaning of the term “disposed,” and is supported by both the intrinsic record and the extrinsic record. *Id.* Under that interpretation, Lee does not disclose or render obvious groups of words lines

“disposed in an order of distance from the selected word line.” Instead, Lee discloses that word lines are placed into fixed groups that are determined ahead of time, and the location of the selected word line has no influence on how the remaining word lines are grouped together for pre-charging.

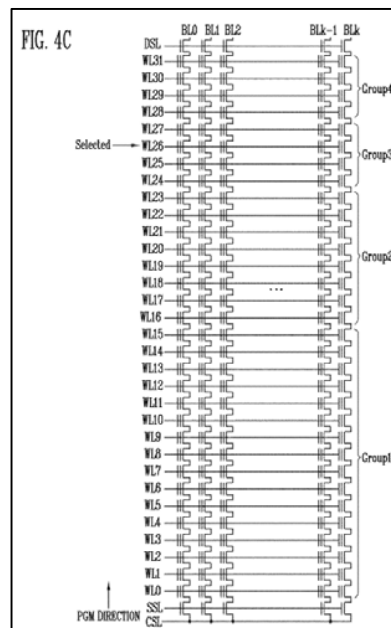
92. Lee discloses several different ways to form groups of word lines, but none of them depends on the location of the selected word line. For example, as shown in Fig. 4A, Lee might create “two word line groups” of “sixteen word lines.”



Lee, 8:4-10. Similarly, as shown in Fig. 4B, Lee might instead create “four word line groups” of “eight word lines” each.

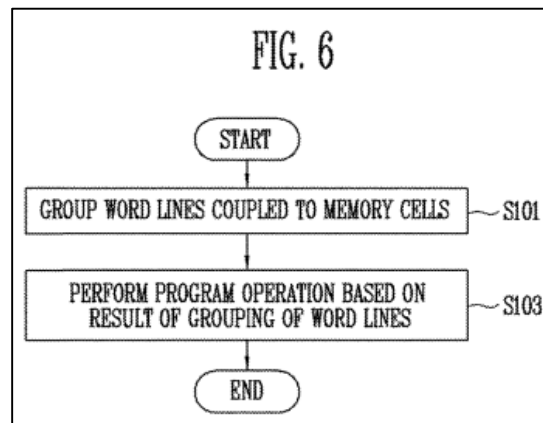


As shown in Fig. 4C, Lee may also create groups where the “closer a word line group is to the drain select transistor, the fewer the number of word lines included.”



Lee 9:36-40, 10:4-12. But in each of these scenarios, the way that word lines are divided into groups has no relationship to the location of the selected word line.

Indeed, at no point does Lee disclose or otherwise render obvious that groups are disposed based on distance to a selected word line. Rather, in each of the described embodiment, the groups are set without any regard being given to the location of the selected word line. Indeed, Lee itself teaches that the groupings are fixed *before* a word line is selected. As explained by Lee, and as shown in Fig. 6, “step S101 of grouping word lines” occurs before the word line to be programmed is even selected, and at step S103 the “pre-bias voltages to be applied” are “determined depending on which word line group is the group to which the selected word line belongs.” Lee 10:63-11:9.



Lee Fig. 6. At no point does Lee suggest that the groups depend on the location of the selected word line, and Petitioner and Dr. Liu have failed to provide any arguments suggesting that Lee could be modified in order to make the groupings dependent on the location of the selected word line.

93. During his deposition, Dr. Liu also confirmed that Lee's groups are not disposed in an order of distance from the selected word line. Dr. Liu was asked direct questions about the embodiment illustrated in Figure 4B. *See* Liu Tr. 23:3-18. When questioned directly if the groups were "disposed in an order of distance from the selected word line 11," Dr. Liu did not agree, and instead stated that they were "disposed in order either from the ... bi[t] line or from the source line," rather than the selected word line. Liu Tr. 25:2-15.

94. For at least the reasons provided above, Lee fails to teach or render obvious word line groups that are "disposed in an order of distance from the selected word line of the plurality of word lines" as required by claims 2 and 12. Rather, as disclosed by Lee and as further confirmed by Dr. Liu, Lee discloses fixed groups that are disposed based on their relative positions to the bit line (or source line). At no point does Lee disclose or otherwise render obvious that word line groups depend on the location of the selected word line.

C. Claims 3 and 13: Lee Does Not Disclose or Render the "First Group of the Plurality of Word Lines Are Disposed Adjacent to the Selected Word Line"

95. Lee does not disclose or otherwise render obvious "the first group of the plurality of word lines are disposed adjacent to the selected word line." Instead, as I discussed in relation to claims 2 and 12 in Section X.B, Lee teaches that groups

of word lines are set in predetermined locations that do not change based on the location of the selected word line.

96. Dependent claim 3 recites: “The memory device of claim 1, ***wherein the first group of the plurality of word lines are disposed adjacent to the selected word line***, the second group of the plurality of word lines are disposed between the first group of the plurality of word lines and the select gate line, and the third group of the plurality of word lines are disposed between the second group of the plurality of word lines and the select gate line.” Similar limitations are also found in dependent claim 13.

97. The term “the first group of the plurality of word lines are disposed adjacent to the selected word line” requires that group to be disposed adjacent to the location of the selected word line. See Section VIII.B (Claim Construction). That interpretation is consistent with the plain and ordinary meaning of the term “disposed,” and is supported by both the intrinsic record and the extrinsic record. *Id.* Under that interpretation, Lee does not disclose or render obvious a groups of words lines “disposed adjacent to the selected word line.” Rather, Lee’s groups are formed without any regard to the location of the selected word line. See Lee 8:4-10, 9:36-40, 10:4-12. Instead, the groups of word lines are determined ahead of time, well before the word line selected for programming has even been chosen. At no point does Lee disclose or otherwise render obvious that a first group “is disposed adjacent

to a selected word line,” nor has Petitioner and Dr. Liu provided any argument to suggest that Lee’s groups could be modified to depend on the location of the selected word line.

98. For at least the reasons provided above, Lee fails to teach or render obvious that “the first group of the plurality of word lines are disposed adjacent to the selected word line” as required by dependent claims 3 and 13. Rather, Lee discloses groups that are set in predetermined locations that do not change based on the location of the selected word line. The groups are the same regardless of which word line is selected for programming.

XI. PETITIONER’S GROUND 2: ZHAO DOES NOT DISCLOSE OR RENDER OBVIOUS CLAIMS 1, 4-7, 9, 11, 14-16, AND 18-19

99. Ground 2 of the Petition alleges that Zhao renders obvious claims 1, 4-7, 9, 11, 14-16, and 18-19.

100. As explained below in Section XI.A, Zhao does not disclose or render obvious a “first word line pre-pulse signal” as required by limitations [1.e.1] and [11.b]. Specifically, Zhao’s disclosure of a flat V_{ss} voltage being applied to word lines (i.e., the purported “first word line pre-pulse signal” identified in the Petition) is not formed as a “pulse,” nor would it have been obvious to modify Zhao to replace V_{ss} with a pulse during the purported pre-charge period.

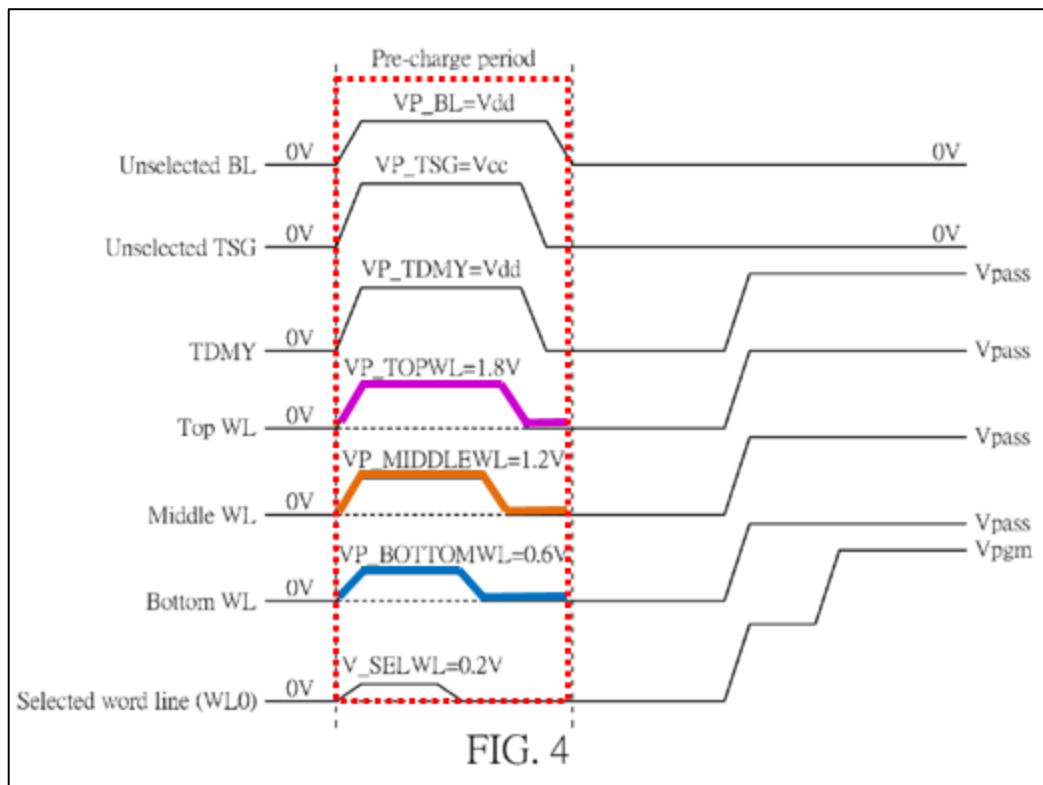
A. Independent Claims: Zhao Does Not Disclose or Render Obvious Applying a “First Word Line Pre-Pulse Signal ... During a Pre-Charge Period” (Limitations [1.e.1] and [11.b])

101. Zhao does not disclose or otherwise render obvious applying a “first word line pre-pulse signal ... during a pre-charge period,” as recited by limitations [1.e.1] and [11.b].

102. The term “word line pre-pulse signal” means a “pulse signal to prepare word lines for a programming step” wherein a “pulse” is a “signal that must increase in value and then decrease in value (or vice versa).” See Section VIII.A (claim construction of “word line pre-pulse signal”). The Petition attempts to argue that Zhao’s application of a flat Vss signal is equivalent to the claimed “word line pre-pulse signals.” See Pet., 44-59. But Zhao’s flat Vss signal does not qualify as a “word line pre-pulse signal[s]” because it is not formed as a pulse, and does not “increase in value and then decrease in value (or vice-versa)” during the relevant time period. Similarly, the Petition has failed to show that it would have been obvious to modify Zhao to replace Vss with some kind of pulsed signal during the relevant time period. The Petition attempts to argue that Vss might be replaced with some other low voltage during the pre-charge period, but that argument mischaracterizes Zhao’s teachings, and would not make sense in the context of Zhao’s system. See Pet. 44-59.

103. Each of the Challenged Claims requires applying a “first word line pre-pulse signal” during the pre-charge period. Specifically, independent claim 1 recites a control circuit configured to “**apply a first word line pre-pulse signal of a plurality of word line pre-pulse signals to a first group of the plurality of word lines** during a pre-charge period” (Element [1.e.1]). Similar limitations are also found in Element [11.b] of independent claim 11, and are also required by each of the ’822 Patent dependent claims by virtue of their dependency on claims 1 and 11.

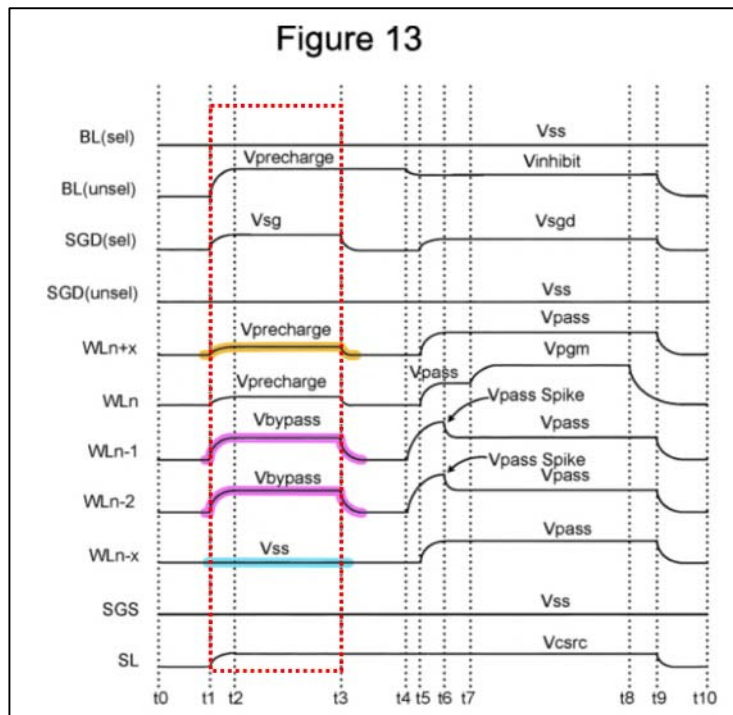
104. As I discussed above in Section VI, the ’822 Patent mitigates programming disturb by applying multiple “word line pre-pulse signals” such that the “channel potential gradient is therefore enhanced ... thus enhancing the pre-charge effect of the unselected bit line and reducing programming disturb.” ’822 Patent, 4:39-59. For example, as show in Fig. 4, the ’822 Patent discloses a first group of word lines applied with a **first word line pre-pulse signal**, a second group of word lines applied with a **second word line pre-pulse signal**, and a third group of word lines applied with **a third word line pre-pulse signal** during **the pre-charge period**:



By comparison, Zhao fails to disclose or render obvious three different “word line pre-pulse signals” being applied during a pre-charge period.

105. The example waveforms disclosed by Zhao for mitigating program disturb are shown in Figure 13 below. Zhao’s states that all of the waveforms start at “0 volts (V_{ss})” at time t_0 , and the time period “from **t1-t3 corresponds to pre-charging.**” Zhao, 22:34-41. But Zhao fails to disclose or render obvious the use of three distinct “word line pre-pulse signals” being applied to distinct groups of word lines during the t_1 - t_3 pre-charging period. The Petition improperly tries to map the claimed voltage onto V_{ss} , $V_{precharge}$, and V_{bypass} , and incorrectly tries to equate

Vss with a “first word line pre-pulse signal ... during a pre-charge period” as recited by independent claims 1 and 11.⁴ See Pet., 22-23, 52.



As explained in Section VIII.A (Claim Construction), the term “word line pre-pulse signal” means a “pulse signal to prepare word lines for a programming step” wherein a “pulse” is a “signal that must increase in value and then decrease in value (or vice versa).” Accordingly, the flat “**0 volt (Vss)**” identified in the Petition cannot be a “word line pre-pulse signal” because it is not a “pulse,” and it does not “increase[] in value and then decrease[] in value (or vice versa)” during the relevant time period.

⁴ The annotations from the Petition for **Vss**, **Vprecharge**, and **Vbypass** are reproduced below.

Moreover, there is nothing in Zhao to suggest that **Vss** could be replaced by a pulse. Instead, Zhao explicitly teaches that “word lines WLn-x **remain at Vss** (e.g., 0 v)” throughout the relevant time period. Zhao, 23:5-12.

106. The Petition attempts to address this deficiency by incorrectly arguing that the displayed **Vss** voltage could be replaced by some other voltage during the time period t1-t3. See Pet., 51-52. Specifically, the Petition points to Zhao’s statement that: “To prevent the source side of the channels from being pre-charged, **unselected source side word lines receive 0 volts or one or more voltages that are too low to pre-charge** and/or too low to turn on memory cells in a highest data state.” Zhao, 19:22-24. But contrary to what the Petition suggests, this statement is not saying that some other signal will take the place of Vss during the pre-charge period (e.g., by having some other voltage applied to word lines WLn-x from the time period t1-t3). Instead, this statement from Zhao is clarifying that the flat **Vss** signal depicted in Fig. 13 may be fixed at “0 volts,” or another fixed voltage “too low to pre-charge and/or too low to turn on memory cells.” Zhao, 19:22-26. But regardless of the exact voltage level chosen, Zhao does not disclose or render obvious a “pulse” being applied to word lines WLn-x from time period t1-t3. At most, the disclosure identified in the Petition is indicating that the flat **Vss** voltage depicted in Figure 13 may be some other low voltage level other than 0 volts.

107. Accordingly, Petitioner and Dr. Liu have failed to show a “first word line pre-pulse signal” being applied to the first group of word lines during a pre-charge period, as required by independent claims 1 and 11. Rather, the identified **Vss** voltage applied to word lines WLn-x (*i.e.*, the purported “first group of word lines”) fails to qualify as a “first word line pre-pulse signal” because it is not formed as a pulse and does not increase and then decrease in value (or vice versa). *See* Section VIII.A (Claim Construction). Moreover, Petitioner and Dr. Liu have failed to provide a rationale for why a POSITA might replace the flat **Vss** signal with some type of pulse, nor would it make sense to do so. Indeed, Zhao explicitly teaches that the word lines will receive a voltage “too low to pre-charge,” and will “**remain at Vss** (e.g., 0 v)” during the relevant time period. Zhao, 19:22-24, 23:5-12. Given that the word lines should be prevented from pre-charging, there is no reason to replace **Vss** with some other value. **Vss** already prevents pre-charging, hence why Zhao explicitly teaches that the word lines should **remain at Vss**.

108. For at least the reasons above, Zhao does not disclose or otherwise render obvious applying a “first word line pre-pulse signal ... during a pre-charge period,” as recited by limitations [1.e.1] and [11.b]. For at least the same reasons, Zhao does not disclose or render obvious the limitations of dependent claims 4-7, 9, 14-16, and 18-19.

**XII. PETITIONER’S GROUND 3: ZHAO IN VIEW OF LEE DOES NOT
DISCLOSE OR RENDER OBVIOUS CLAIMS 1-9 AND 11-19**

109. Ground 3 of the Petition alleges that Zhao in view of Lee renders obvious claim 1-9 and 11-19.

110. As explained below in Section XII.A, a POSITA would not have been motivated to combine Zhao and Lee in the manner proposed in the Petition to render obvious the subject matter of limitations [1.e.1]-[1.e.3] of independent claim 1 and the corresponding limitations [11.b]-[11.d] of independent claim 11. The purported problems being addressed by Lee regarding “resistance components” are not present in Zhao, and the combination presented in the Petition misapplies Lee and would not work as intended even if “resistance components” were somehow assumed to be present in Zhao’s system.

**A. Independent Claims: A POSITA Would Not Have Been
Motivated to Combine Zhao and Lee in the Manner Proposed in
the Petition**

111. As I discussed in Sections X.A (discussing Ground 1) and XI.A (discussing Ground 2), Zhao and Lee taken individually each fails to disclose or render obvious a “first word line pre-pulse signal,” “second word line pre-pulse signal,” and “third word line pre-pulse signal,” during “a pre-charge period” as recited by independent claims 1 and 11. To address the deficiencies in Lee and Zhao, the Petition suggests that the two references could be combined together to create three distinct “word line pre-pulse signals.” See Pet. 62. Specifically, the Petition

suggests applying Lee's teachings to replace Zhao's pre-charging voltages with multiple increasingly large pre-bias voltages in order to offset "effects caused by the resistance component between the source select transistor and the drain select transistor." Pet., 62; *see also* Lee 8:25-52 (explaining that "a threshold voltage of a memory cell is increased by a resistance component between the source select transistor and the drain select transistor"). But this proposed combination would not work as suggested in the Petition, and a POSITA would not have been motivated to apply Lee's teachings to Zhao in the manner proposed in the Petition.

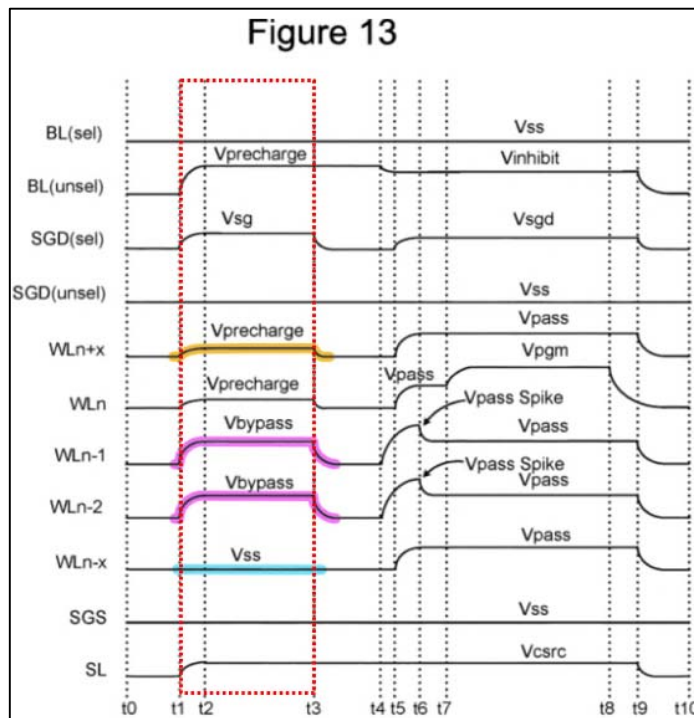
112. There are several reasons why a POSITA would not have been motivated to apply Lee's teachings in the manner suggested in the Petition. **First**, the Petition fails to account for the fact that the two references do not charge the memory string channel in the same direction—Lee's teachings are motivated by problems arising from charging operations performed via the **common source line**, but Zhao performs charging from the **bit line**. Specifically, Lee identified problems in "typical programming operations" wherein "**the precharge level in a source select side channel is reduced** and thus channel boosting is not effectively generated." Lee, 8:25-37. **Second**, Lee's pre-charging operation is concerned with offsetting the effects of a "resistance component between the source select transistor and the drain select transistor," (Lee 8:47-52), but those resistive effects are not present to modify memory cell threshold voltages in Zhao's system. **Third**, even if there were assumed

to be a “resistance” component between the source and drain present in Zhao’s system, the proposed modification described in the Petition would not compensate for the effect, and has failed to account for Zhao’s pre-charging voltages being applied through the bit line rather than the source line. **Fourth**, Zhao and Lee use fundamentally different approaches for mitigating program disturb—hence the absence of a “resistance” component in Zhao—and as a result a POSITA would not achieve any of Lee’s intended benefits by applying Lee’s teachings to Zhao in the manner proposed by the Petition. As a result, Petitioner’s proposed combination would not provide the benefits that Lee’s teachings purport to provide, and which the Petition relies on as a purported motivation to combine. Taken as a whole, there is no reason why a POSITA would combine the references in the manner suggested in the Petition.

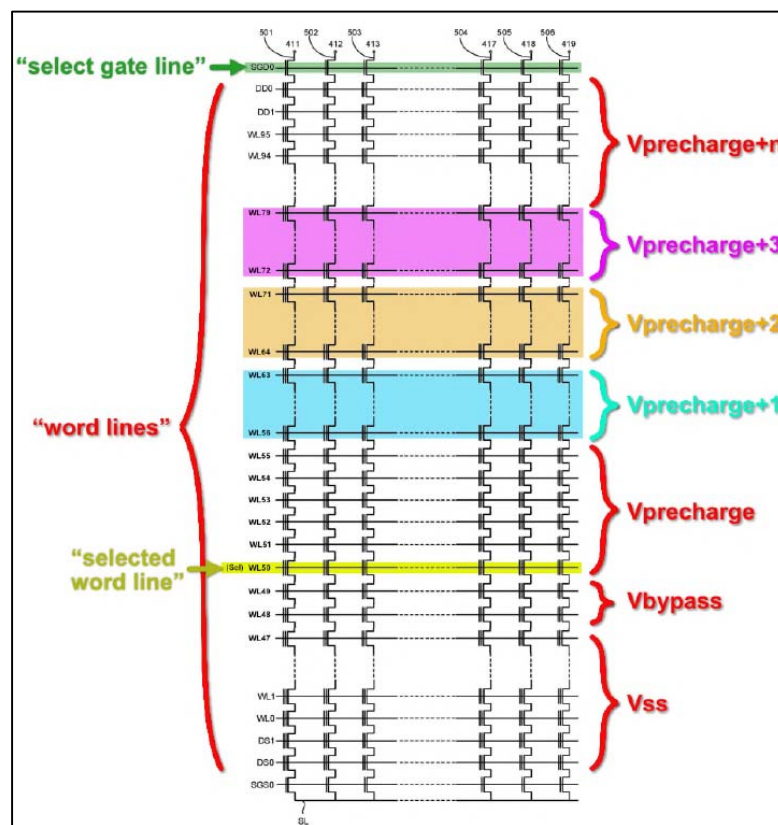
113. As discussed in Sections X.A (discussing Ground 1) and XI.A (discussing Ground 2), each of the challenged claims requires applying three different “word line pre-pulse signal[s]” to different groups of word lines. Specifically, independent claim 1 recites a control circuit configured to “**apply a first word line pre-pulse signal of a plurality of word line pre-pulse signals to a first group of the plurality of word lines** during a pre-charge period” (Element [1.e.1]); “**apply a second word line pre-pulse signal of the plurality of word line pre-pulse signals to a second group of the plurality of word lines** during the pre-

charge period” (Element [1.e.2]); and “**apply a third word line pre-pulse signal of the plurality of word lines pre-pulse signals to a third group of the plurality of word lines** during the pre-charge period” (Element [1.e.3]). Similar limitations are also found in Elements [11.b]-[11.d] of independent claim 11, and are also required by each of the ’822 Patent dependent claims by virtue of their dependency on claims 1 and 11.

114. As I discussed in Section IX.B (summarizing Zhao), Zhao describes a “**Vprecharge**” signal being applied to the selected word line (WLn) as well as all of the word lines WLn+x, which are located on the drain-side of the currently selected word line (e.g., between the selected word line and the drain select transistor (SGD) that connects the memory string to the bit line).



Zhao, Fig. 13. Petitioner and Dr. Liu argue that it would have been obvious to subdivide word lines $WLn+x$ into multiple groups of word lines, and replace Zhao's **Vprecharge** signal with multiple different signals that are applied to each of the different sub-groups. See Pet. 60-67. The Petition then proposes that the modified **Vprecharge** signals would then have increasingly large voltage levels when applied to sub-groups closer to the drain select transistor. *Id.* According to Petitioner, Lee purportedly teaches that this scheme will “compensate” for “effects caused by the resistance component between the source select transistor and the drain select transistor,” and that the combined system would operate as illustrated below. See Pet., 60-67.



Pet., 65 (annotations reproduced from Petition). Specifically, the Petition argues that by following Lee's purported teachings:

[G]roups of unselected drain-side word lines are now treated differently during the pre-charge period. WL56-WL63 would now receive a higher pre-charge voltage like $V_{precharge+1}$, WL64-WL71 would receive a still higher pre-charge voltage like $V_{precharge+2}$, WL72-WL79 would receive an even higher pre-charge voltage like $V_{precharge+3}$, and so on until the last group of drain-side word lines, which would receive $V_{precharge+n}$.

Pet., 64. But Petitioner's proposed combination would not work as presented. It is inconsistent with Lee's own teachings about why a POSITA might want to use multiple different pre-bias voltages, and the combination as presented ignores the actual structure and basic operating principles of NAND memory strings.

115. **First, the Petition Ignores Differences in Charging Direction:** At the outset, the proposed combination described in the Petition ignores the fact that the cited embodiments of Lee and Zhao do not performing charging the same way. Lee's states that its teachings address problems arising from pre-charging operations performed via the common source line (or, more specifically, pre-charging operations that apply pre-charging voltages via the source-line while current runs through the memory string), while Zhao instead charges the memory string from the bit line located on the opposite end of the memory string. Indeed, Lee states that its teachings address problems in "typical programming operations" where memory cell threshold voltages are "increased by a resistance component between the source

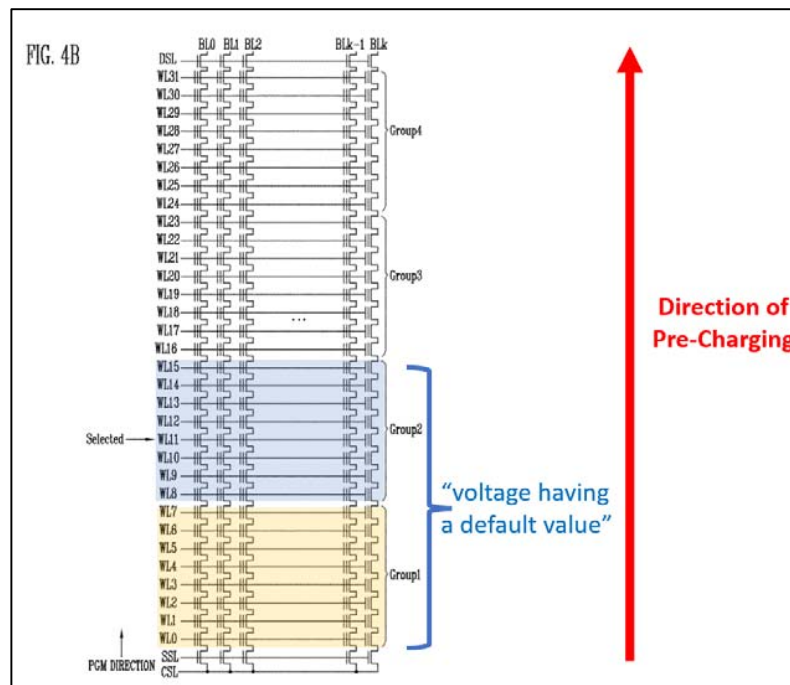
select transistor and the drain select transistor,” with the result that “**the precharge level in a source select side channel is reduced** and thus channel boosting is not effectively generated.” Lee, 8:25-37. Lee also explicitly describes its system charging the memory string through the source, stating that “precharge voltage [is] applied **to the common source line** during a precharge operation.” Lee, 8:25-37, 8:65-9:6. By comparison, in the embodiment of Figure 13 of Zhao on which Petitioner relies, the pre-charge voltages are applied through the **bit line** rather than the **source line** (i.e., the voltages being used to pre-charge the channel of the memory string are coming from the **bit line** located on the opposite side of the device). See, e.g., Zhao 22:39-47 (“[a]t time t1 ... **the unselected bit lines are raised to a pre-charge voltage** $V_{precharge}$ ”). Petitioner and Dr. Liu have completely overlooked the distinction between applying charging voltages through the **bit line** as opposed to the **source**, and incorrectly assume that Lee’s teachings (e.g., about using increasingly large voltages on the drain-side of the device closer to the bit line) would be directly applicable to Zhao without further modification. But the schemes used when charging from the bit line as opposed to the common source can differ substantially, and cannot be ported from one situation to the other without accounting for the effects of applying the pre-charge voltage through a different location and the placement of the memory cells being pre-charged. See, e.g., Yang 1:59-2:19 (distinguishing Fig. 8A-8C embodiments where “pre-charge is from a bit

line,” Fig. 9A-9C embodiments where “pre-charge is from a source line,” and Fig. 10A-10C embodiments where “pre-charge is from both a bit line and a source line”).

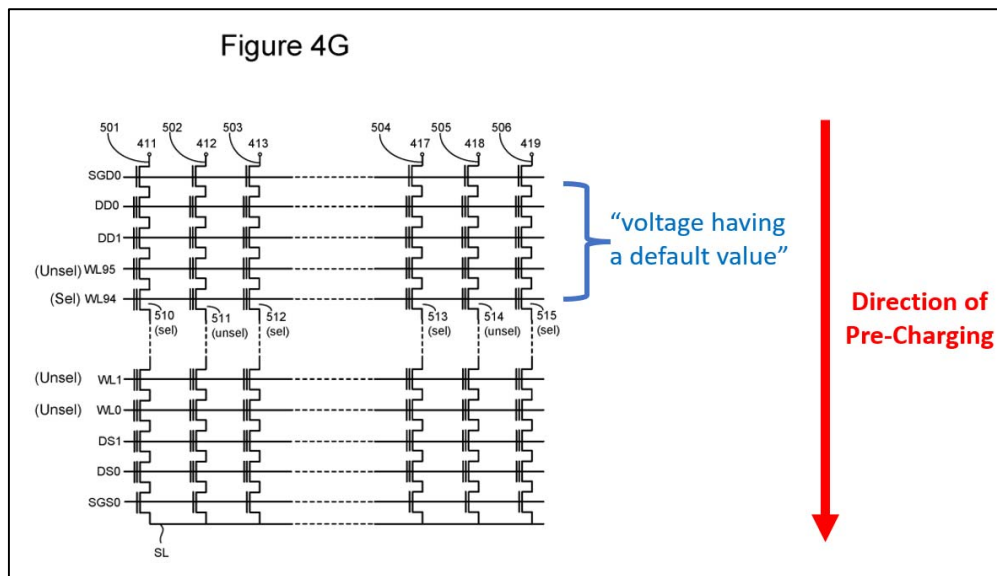
116. Petitioner and Dr. Liu have ignored the differences that arise when performing pre-charging operations from the bit line, as opposed to the source line (or pre-charging operations that apply precharge voltages through both the bit line and the source line), and have failed to account for those distinctions in the proposed combination. Indeed, the Petition has failed to explain how—if at all—Lee’s teaching would need to be adapted to compensate for that change. For example, Lee teaches that a “**precharge voltage [is] applied to the common source line during a precharge operation.**” Lee, 8:25-37, 8:65-9:6. When doing so, Lee applies a single “**default value**” to all the groups between the common source and the group with the selected word line. Lee, 9:41-59. In other words, Lee teaches that all of the memory cells on the side of the string where the precharge voltage comes from get a single default value. For example, as illustrated in Figure 4B below, Lee teaches when the selected word line is in Group2, both that group and the other groups closer to where the pre-charging voltage is applied from receive the same default value:

A pre-bias voltage having a default value is applied to the word lines WL8 to WL15 included in the second group Group2, including a word line WL11 that is coupled to a selected transistor. In addition, the pre-bias voltage having the default value also is applied to word lines WL0 to WL7 included in a first group, Group1, that is closer to the source select transistor than is the second group.

Lee, 9:41-59.



Lee, Fig. 4 (annotations added to show direction of pre-charging—the precharge voltage is applied to the string of memory cells from the source line at the bottom of the memory string, and propagates upwards). Applying this teaching to Zhao would not, as the Petition has suggested, result in groups of “drain side word lines” being “treated differently during the pre-charge period.” See Pet. 64. Zhao performs charging in the opposite direction, from the bit line. See Zhao 22:39-50 (“[a]t time t_1 ... **the unselected bit lines are raised to a pre-charge voltage** $V_{precharge}$ ”). If anything, Lee’s teachings would suggest that a **single default value** should be applied to those drain side word lines (similar to Zhao’s unmodified system where “the drain side unselected word lines $WLn+x$ are raised to the precharge voltage”). Zhao 22:39-50.



Zhao, Fig. 4G (annotations added to show direction of pre-charging—the precharge voltage is applied to the string of memory cells from the bit line at the top of the string, and propagates downwards). Accordingly, not only would a POSITA not apply Lee’s teachings in the manner suggested in the Petition, but Lee’s teachings actually suggest that Zhao should ***avoid*** being modified to have multiple different word line pre-pulse signals.

117. **Second, Lee’s Teachings About Resistance Components are Inapplicable in Zhao:** The Petition states that the proposed combination would be motivated by Lee’s teaching that multiple pre-bias voltages are needed to offset a “resistance component between the source select transistor and the drain select transistor,” but that rationale is simply inapplicable in Zhao. Pet., 60 (citing Lee 8:25-29). There is no “resistance component” in Zhao’s system that needs to be

offset, and contrary to what Petitioner suggests, replacing Zhao's **Vprecharge** with multiple pre-charge signals in the manner illustrated in the Petition would not result in a more uniform charge distribution. A "resistance component between the source select transistor and the drain select transistor" will alter the pre-charge level in the memory string only when there is a current running through the string. But Zhao's system has several transistors cut off (e.g., the transistors applied with **Vss** are turned off and act like open circuits), thus precluding any current from flowing in the memory string. As a result, the voltage level along the conducting portion of the channel (i.e., the portion of the string formed by the memory cells near the drain select transistor that receive Vprecharge through WLn+x) does not vary with a "resistance component" that needs to be offset.

118. According to Lee, "a threshold voltage of a memory cell is increased by a **resistance component** between the source select transistor and the drain select transistor" such that "*the precharge level in a source select side channel is reduced.*" Lee, 8:25-32. This relationship between resistance and voltage is governed by Ohm's law: changes in voltage are proportional to current times resistance ($V=R*I$). See, e.g., Ex. 2022 (Hambley, Electrical Engineering Principles and Applications, Fourth Edition (2008) ("Hambley")) at 29. The "resistance component between the source select transistor and the drain select transistor" (R_{channel}) will create voltage drops between the drain and source of a given transistor (ΔV_{DS}) when

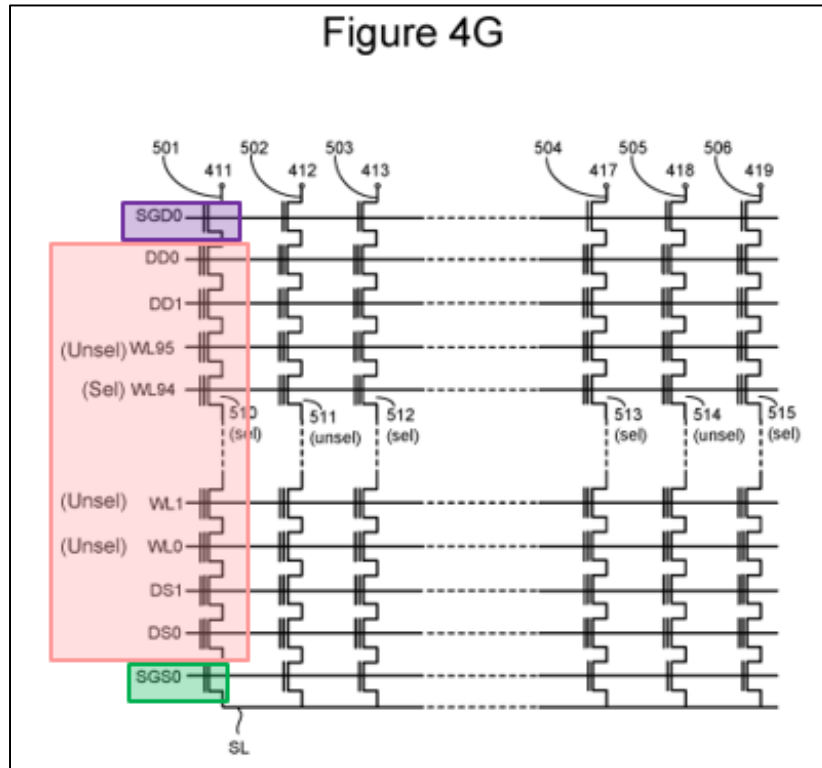
there is a current running along the length of the memory string (e.g., a current I_{DS} that runs from the source select transistor and to the drain select transistor along the length of the memory string) according to the formula $\Delta V_{DS} = R_{channel} \times I_{DS}$. See Lee, 8:25-32. In turn, this will result in a “precharge level” being reduced on the “source select side” of the memory string in traditional systems. See Lee, 8:25-32. Accordingly, Lee describes applying “different pre-bias voltages to the respective word line groups” along the entire length of the memory string based on their relative positions within the string in order to compensate for the resistance component and create a more uniform level of charge. See Lee, 2:63-3:7, 8:3-17. But this “resistance component” referenced by Lee is irrelevant in a system like Zhao’s that is designed to have ***no steady state current*** running “between the source select transistor and the drain select transistor” in the memory string. See Lee, 8:25-32.

119. I understand that during his deposition, Dr. Liu introduced a new argument that what Lee describes as a “resistance component between the source select transistor and the drain select transistor” is actually referencing a “body effect” or “source voltage effect” that causes memory cell threshold voltages to change as “a function of how many transistors [are] connected in series with it.” Liu Tr. 82:12-25. I disagree. Lee makes no mention of “body effects” or “source voltage effects.” Rather, Lee states that “a resistance component between the source select transistor and the drain select transistor” causes a “precharge level in a source select side

channel” to be “reduced.” Lee 8:25-31. In general, the “body effect” refers to the effective voltage of a transistor being modified based on a voltage difference between the source and the substrate (i.e., body) of a transistor. But in the case of Zhao, a POSITA would understand from Fig. 4E that each of the memory cells is formed in the same polysilicon layer 471, and so nominally the body/substrate voltages will be identical (i.e., grounded) for all transistors. *See* Zhao 11:1-15. As a result, any differences in memory cell threshold voltages resulting from the “body effect” would have to be a result of differences in the source voltage between memory cells within the string (i.e., voltage drops along the string itself). As before, Ohm’s law controls ($\Delta V_{DS} = R_{\text{channel}} \times I_{DS}$), and any such differences would require a current running through the memory string to be present. Whether the changes in threshold voltage are conceptualized in terms of “resistances” (as described by Lee) or the “body effect” (as Dr. Liu referenced in deposition), the physical phenomenon that Lee’s teachings are attempting to compensate for are simply not present in a system like Zhao’s where a subset of the word lines and the source select line receive low V_{ss} voltages. Doing so turns off transistors, prevents current from running through the memory string, and prevents changes in pre-charge voltage (or altered threshold voltages due to a body effect) from being present in the device.

120. The fact that Zhao has ***no current*** is a direct result of how memory strings are structured, coupled with Zhao applying a low voltage (e.g., V_{ss}) on

multiple words lines throughout the pre-charging operation. As illustrated below, Lee and Zhao both describe a traditional type of memory string formed from a “vertical column” of **memory cells** arranged in series between a **source side** select transistor and a **drain side** select transistor.



Zhao, Fig. 4G, 10:6-24; *see also* Lee, Fig. 3, 7:37-57 (describing the structure of the memory cell string). As shown in the figure, the **memory cells** that form the string are connected end-to-end in series, with the source of one memory cell being connected to the drain of the next. This means that **all** of the **memory cells** must be turned on before current can flow between the **source side** select transistor and the **drain side** select transistor (*i.e.*, all the memory cells must be turned on to form a

conductive channel through the memory cell string). If any of the **memory cells** in the string are turned off (e.g., as a result of a low voltage being applied on the corresponding word line), there will be no conductive channel formed through the string. As a result, no current can flow down the memory string between the **source side** select transistor and the **drain side** select transistor (i.e., $I_{DS} = 0$). From Ohm's law ($\Delta V_{DS} = R_{\text{channel}} \times I_{DS}$), there will also be no voltage drops between the source and drain of any memory cell that remains turned on (i.e., when $I_{DS} = 0$ it implies $\Delta V_{DS} = 0$). In such a situation, any portion of the channel still connected together will have the same uniform voltage level, and there are no variations in threshold voltage or other "resistance components" that need to be compensated for.

121. The Petition does not address these basic characteristics of Zhao, and fails to recognize that in Zhao (as well as the proposed combination illustrated in the Petition) several of the memory cells are **explicitly** turned off. Indeed, Zhao states that multiple word lines are applied with **V_{ss}** (or a similar voltage "**too low to pre-charge** and/or too low to turn on memory cells in a highest data state"), thus turning off the memory cells connected to those word lines. This precludes any current flowing between the **source side** select transistor and the **drain side** select transistor as well as between the bit line at the top of the NAND string and sources line at the bottom of the NAND string. In turn, this prevents any supposed "resistance components" from creating changes in voltage along the portion of the memory

string being pre-charged that would need to be compensated for (i.e., for the pre-charging portion of the channel, $\Delta V_{DS} = 0$ when $I_{DS} = 0$, and the value of the “resistance component” becomes irrelevant). See Zhao, 19:22-26. Accordingly, a POSITA would not apply Lee’s teachings in the manner suggested in the Petition, and Lee’s teachings would serve no purpose in the context of Zhao’s system.

122. **Third, Lee’s Teachings Would Not Work in Zhao’s System:** There is no “resistance component between the source select transistor and the drain select transistor” present in Zhao’s that needs to be compensated for by Lee’s teachings. But even assuming that such a “resistance component” were somehow relevant to Zhao, the proposed combination as illustrated in the Petition would not “offset” that resistance component. Indeed, the fact that Zhao charges from the bit line (rather than the source) would preclude Petitioner’s proposed combination from working as intended.

123. As part of the proposed combination, Petitioner proposes modifying Zhao such that “unselected drain-side word lines” are divided into groups and applied with different voltage levels, with word lines receiving higher voltages the closer they are to the bit line (e.g., such that $V_{\text{precharge}+3} > V_{\text{precharge}+2} > V_{\text{precharge}+1}$). Petition at 64-65. But unlike in Lee, Zhao applies the precharge voltage through the **bit line** rather than the **common source**. Indeed, Lee states that a “precharge voltage [is] applied to the common source line during a precharge

operation.” Lee, 8:65-9:6. By comparison, in Zhao it is “unselected bit lines” that are “raised to a pre-charge voltage.” Zhao 22:39-47. If it were assumed that a “resistance component between the source select transistor and the drain select transistor” needed to be offset in Zhao’s system, it would be the word lines *furthest from the bit line* that were being impacted. See Lee 8:47-51.

124. Under these conditions, increasing the bias voltages for “drain-side word lines” near the bit line, as Petitioner suggests in the proposed combination, would not be effective at offsetting the “resistance component between the source select transistor and the drain select transistor.” See Pet. 64-65. The bias voltages in the proposed combination are in the wrong location, and increase in value closer to the bit line where the charging voltage is being applied. Specifically, in the proposed combination illustrated on page 65 of the Petition (reproduced above), all the word lines between WL47 and WL0 are held at V_{ss} during precharge: the transistors controlled by these word lines are turned off during precharge, and as taught by Zhao, are deliberately prevented from precharging. See Zhao, 19:22-26. As such they have no resistance component to be offset whatsoever, and even if there was assumed to be some change in the threshold voltages due to a resistance component, there would be no need to “offset” that change because the transistors controlled by the word lines between WL47 and WL0 are not supposed to be turned on and precharged in the first instance. As for the remaining word lines WL56 through DD0

between the selected word line and the bit line where the charging voltage is being applied, applying larger voltages than the normal default $V_{precharge}$ value (e.g., $V_{precharge}+1$, $V_{precharge}+2$, $V_{precharge}+3$, etc.) is unnecessary, and will only contribute to increased device complexity and increased risk of transistor breakdown over time. Once again, a POSITA would not have been motivated to apply Lee's teachings in the manner suggested in the Petition, and modifying Zhao as the Petitioner has suggested would only serve to exacerbate the problems identified by Lee.

125. **Fourth, Lee and Zhao Use Incompatible Approaches:** Lee and Zhao use two disparate approaches for mitigating program disturb, which are not compatible with one another.

126. Zhao states that the described pre-charging operation is directed to “purging (cleaning/clearing the electrons from) the already programmed side of the channel” prior to the boosting and programming steps, in the region near the selected word line. See Zhao, 2:27-35; see also *id.* 18:63-19:8 (describing a method for “purging the already programmed side of the channel during a pre-charge operation”). As explained by Zhao, the act of purging mitigates “source side hot electron injection,” which describes a type of program disturb that can occur when excess charges are built up on the source side of the selected memory cell (e.g., as a result of previous programming and verification operations performed on those

cells). See Zhao 18:36-51. A boosting operation can then accelerate those excess charges from the source side of the selected memory cell to the drain side of the selected memory cell, which can then be inadvertently redirected into the storage layer of any memory cell connected to the selected word line. Zhao, 18:36-51. To address this problem, Zhao teaches that excess charges can be purged by applying “a bypass voltage to multiple already programmed side unselected word lines while pre-charging ... the channels of unselected NAND strings.” Zhao, 19:29-34; see also Zhao, 22:50-56. Doing so “opens up the channel (e.g. electrically couples the two ends of the channel) ***so that electrons can migrate (electrical communication) from the source side of the channel to the drain side of the channel***” which then “reduces or eliminates the voltage differential between the source side of the channel and the drain side of the channel that may later cause program disturb.” Zhao 22:65-23:5. In other words, Zhao is concerned with coupling the two sides of the channel together in the immediate vicinity of the selected word line so that electrons can migrate freely between the two sides.

127. Lee describes a very different approach for addressing program disturb, which operates by turning on memory cells across the full length of the string. As described above, Zhao uses a bypass voltage in the immediate vicinity of the selected word line that “electrically couples the two ends of the channel” and allows charges to be equalized. See Zhao, 22:65-23:5. But Zhao’s purging operation is only

concerned with pre-charging the memory cells near the selected word line, which minimizes the number of word lines being pre-charging and avoids establishing a channel along the full length of the string that could conduct current between the source select transistor and the drain select transistor. *See Id.* As a result, there is no need to compensate for any “resistance component” between the source and drain that would otherwise create voltage differences along the length of the channel. *See Id.* By comparison, Lee’s system operates by applying a pre-charge voltage to every memory cell in the string. *See, e.g., Lee*, 8:3-18 (a “memory block includes thirty-two word lines WL0 to WL31” and pre-bias voltages are “applied to the respective word lines WL0 to WL31 in a precharging step during a program operation”). Because Lee turns on every memory cell in the string, thus allowing current to flow, Lee must compensate for the fact that the “pre-charge level in a source side channel is reduced and thus charge boosting is not effectively generated” because “a threshold voltage of a memory cell is increased by a resistance component between the source select transistor and the drain select transistor.” *Lee*, 8:25-31, 8:47-52. This phenomenon is simply not present in Zhao.

128. In view of these differences, a POSITA would not have been motivated to apply Lee’s teachings to Zhao. Contrary to what the Petitioner has suggested, Lee and Zhao are not describing complementary techniques that can be combined together to further reducing program disturb. *See Pet.*, 66-68. Instead, the references

are describing fundamentally different approaches. Specifically, Lee's use of preset bias levels for each and every word-line (which would include those adjacent to the selected word line) operates on a fundamentally different principle than Zhao's system. As a result of operating on all word lines simultaneously, Lee needs to compensate for a "resistance component" that creates differences in pre-charge level along the length memory string (*i.e.*, at different locations between the source select transistor and the drain select transistor). But Zhao operates using only localized pre-charging voltages, and does not experience the same type of impacts from a "resistance component" as Lee does. As a result, Lee's teachings are largely inapplicable to Zhao, and attempting to apply Lee's teachings to Zhao would not bring any benefits in the context of Petitioner's proposed combination.

129. Taken as a whole, a POSITA would not have been motivated to modify Zhao in view of Lee in the manner illustrated in the Petition, nor would they have had a reasonable expectation of success in doing so. The Petition has failed to properly account for the differences in how Zhao and Lee charge memory strings (*e.g.*, through the bit line rather than the source line) or the fact that Zhao's system includes several memory cells that are cut off. As presented, the proposed combination is likely to exacerbate the sources of program disturb that Lee purports to avoid. Moreover, when accounting for the different charging directions between Lee and Zhao and the underlying device physics, a POSITA considering Lee's

teachings would have been motivated to leave Zhao unmodified (e.g., by using a single default value for Vprecharge) rather than combining the references in the manner suggested in the Petition.

130. For at least the reasons above, Zhao in view of Lee does not disclose or render obvious the use of three separate “word line pre-pulse signals” as required by independent claims 1 and 11. For at least the same reasons, the proposed combination of Zhao in view of Lee does not disclose or render obvious the limitations of dependent claims 2-9 and 12-19.

**XIII. PETITIONER’S GROUND 4: YANG DOES NOT DISCLOSE OR
RENDER OBVIOUS CLAIMS 1-7, 9, 11-16, AND 18-19**

131. Ground 4 of the Petition alleges that Yang renders obvious claim 1-7, 9, 11-16, and 18-19.

132. As explained below in Section XIII.A, Yang does not disclose or render obvious the use of three word line pre-pulse signals with incrementally increasing voltage levels being applied to different groups of word lines, as required by limitations [1.e.1]-[1.e.4] of independent claim 1 or the corresponding limitations [11.b]-[11.e] of independent claim 11.

133. Additionally, as explained below in Sections XIII.B and XIII.C, Yang does not disclose or render obvious the added limitations of dependent claims 2-3 and 12-13 which require, among other things, that groups of word lines are

“disposed” based on the location of the word line that has been selected for programming.

134. Yang does not disclose or render obvious any of the Challenged Claims.

A. Independent Claims: Yang Does Not Disclose or Render Obvious Word Line Pre-Pulse Signals with Incrementally Increasing Voltage Levels

135. Yang does not disclose or otherwise render obvious applying three “word line pre-pulse signals” to three groups of word lines that have incrementally increasing voltage levels, as required by limitations [1.e.1]-[1.e.4] and [11.b]-[11.e] of independent claims 1 and 11.

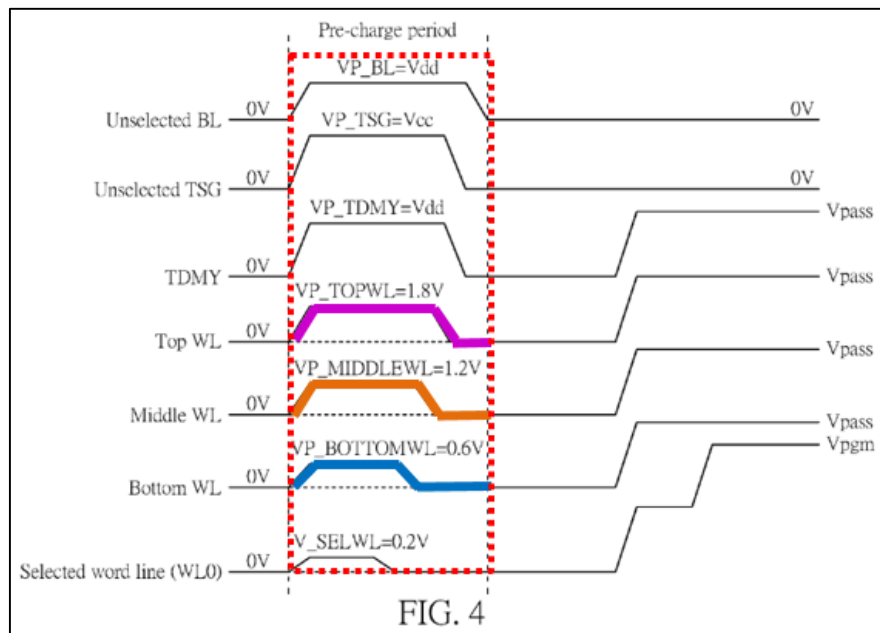
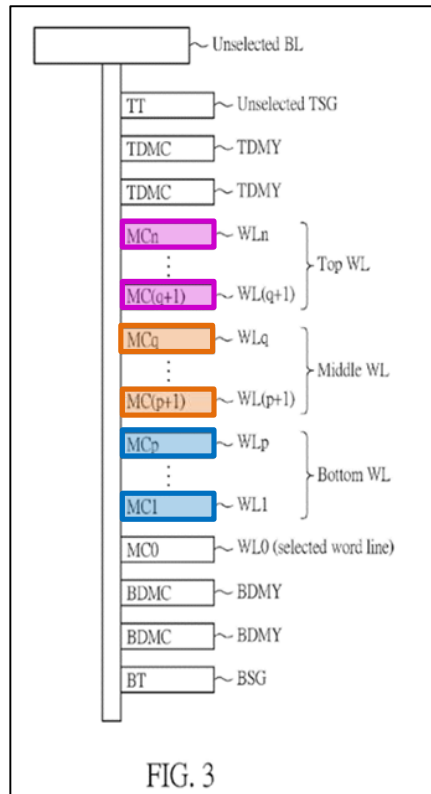
136. The Petition argues that Yang’s use of “Vbypass,” “Vpre_OD,” and “Vpre_dmy” voltages is equivalent to the claimed “word line pre-pulse signals,” but Yang does not disclose or render obvious that these voltages have incrementally increasing voltage levels (i.e., Yang fails to disclose or render obvious that Vpre_OD is greater than Vpre_dmy which is greater than Vbypass). Petitioner’s further assertion that “a POSITA would nonetheless have understood Yang to render what this limitation requires obvious” is also incorrect, and unsupported by the record. See Pet., 76-82.

137. Each of the Challenged Claims requires applying three different “word line pre-pulse signal[s]” with incrementally increasing voltage levels. Specifically, independent claim 1 recites a control circuit configured to “**apply a first word line**

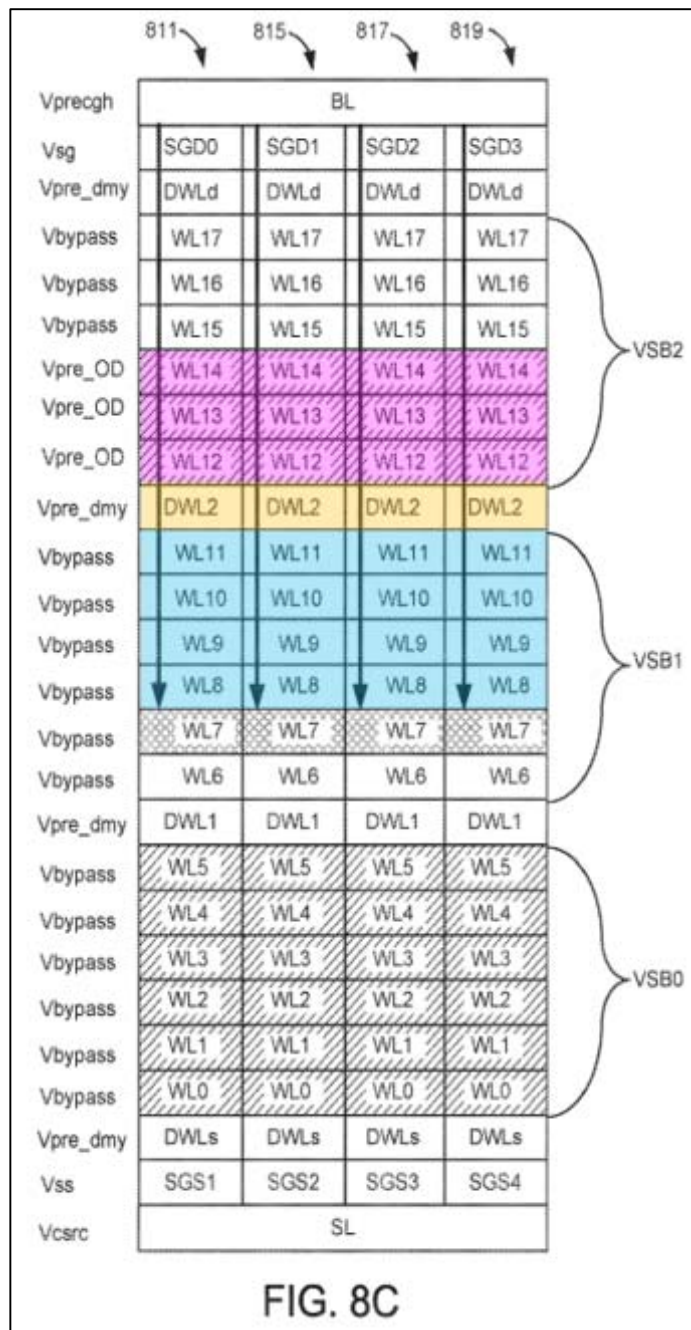
pre-pulse signal of a plurality of word line pre-pulse signals to a first group of the plurality of word lines during a pre-charge period” (Element [1.e.1]); “**apply a second word line pre-pulse signal of the plurality of word line pre-pulse signals to a second group of the plurality of word lines** during the pre-charge period” (Element [1.e.2]); and “**apply a third word line pre-pulse signal of the plurality of word lines pre-pulse signals to a third group of the plurality of word lines** during the pre-charge period” (Element [1.e.3]) wherein “*a voltage level of the second word line pre-pulse signal is greater than that of the first word line pre-pulse signal, and a voltage level of the third word line pre-pulse signal is greater than that of the second word line pre-pulse signal.*” (Element [1.e.4]). Similar limitations are also found in Elements [11.b]-[11.e] of independent claim 11, and are also required by each of the ’822 Patent dependent claims by virtue of their dependency on claims 1 and 11.

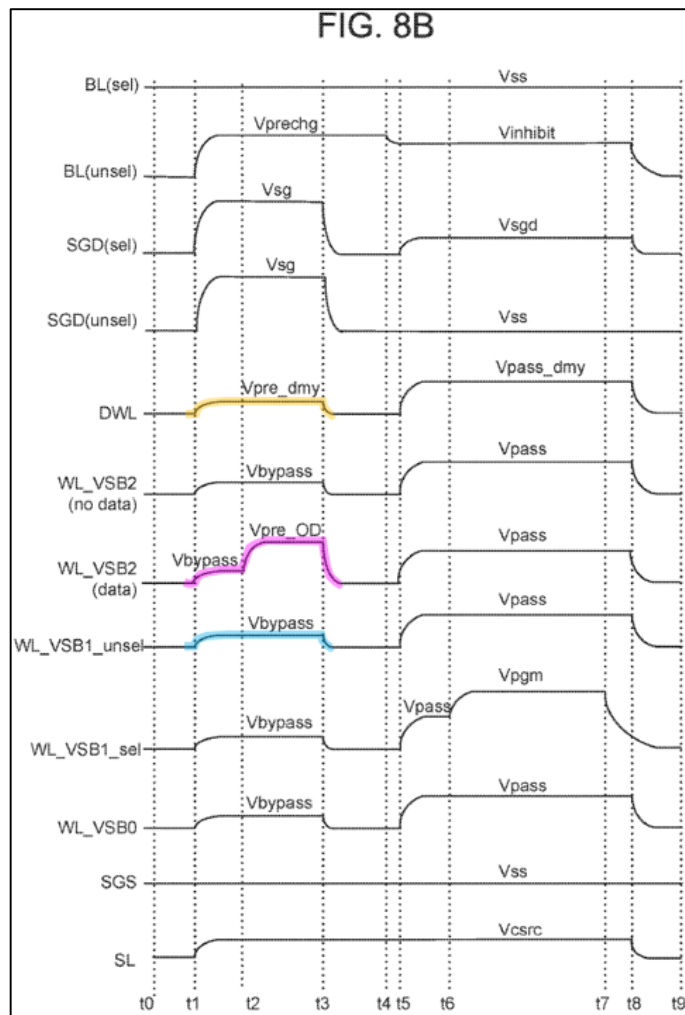
138. As I discussed above in Section VI, the system described by the ’822 Patent may be “configured to apply a plurality of word line pre-pulse signals to word lines which are disposed between the selected word line and the top dummy word line TDMY,” with “incremental” voltage levels. ’822 Patent, 3:55-59; 4:2-10. For example, as illustrated in Figs. 3-4, the **first word line pre-pulse signal** (VP_BOTTOMWL) has a voltage level of 0.6V, the **second word line pre-pulse signal** (VP_MIDDLEWL) has a greater voltage level of 1.2V voltage level, and the

third word line pre-pulse signal (VP_TOPWL) has an even greater voltage level of 1.8V. See '822 Patent, 5:50-55, 5:65-6:8, Figs. 3-4.



139. By comparison, Yang fails to disclose or render obvious three distinct “word line pre-pulse signals” being applied to groups of word lines that have incrementally increasing voltage levels. For example, as shown below in Figures 8B-8C of Yang, the Petition attempts to improperly equate the claimed “**first word line pre-pulse signal**” “**second word line pre-pulse signal**” and “**third word line pre-pulse signal**” to Yang’s disclosure of: (1) a “**bypass voltage**” (“**Vbypass**”) applied to “word lines in VSB2 that are not programmed”, (2) a “**dummy pre-charge voltage**” (“**Vpre_dmy**”) applied to “all dummy word lines,” and (3) an “**overdrive voltage**” (“**Vpre_OD**”) applied to “programmed data word lines” in the “upper vertical sub-block VB2 of the data structure.” Pet., 73-81.





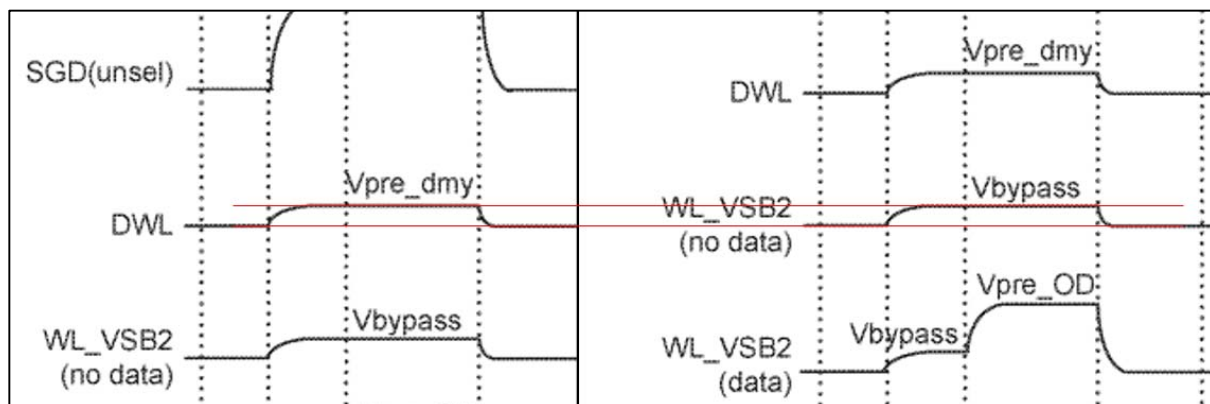
Yang, Figs. 8B-8C.⁵ But Yang does not disclose or otherwise render obvious that the identified voltages are first/second/third “word line pre-pulse signals” with the type of incrementally increasing voltage levels that are required by the claims (i.e., that **Vpre_OD** is greater than **Vpre_dmy**, which is greater than **Vbypass**).

⁵ Petitioner’s annotations for **Vbypass**, **Vpre_dmy**, and **Vpre_OD** have been reproduced.

140. Yang discloses that “[m]ore or less ... layers” may be used, which the Petition misinterprets as Yang disclosing or otherwise rendering obvious that multiple dummy layers may be used in place of the one dummy layer depicted in figure 8C. *See* Pet., 79; Yang 8:54-9:5. Yang’s dummy memory cells are placed between different “vertical sub-block[s]” of memory cells to “electrically isolate a first set of memory cell transistors within the memory string.” Yang 12:35-43. To the extent Yang discloses more layers being incorporated into the device (e.g., by increasing the size of sub-blocks or including new sub-blocks into the stack), this does not imply that multiple dummy layers would stacked up in a single location. If anything, Yang suggests that only a single layer of dummy memory cells is needed to isolate any given set of memory cells, and adding extras would serve no purpose and would only render ineffective available layers that could be used to store data.

141. As recognized in the Decision to Institute, Petitioner has failed to show that Yang discloses or otherwise render obvious that these are three distinct “word-line pre-pulse signals” with the types of incrementally increasing voltage levels required by the Challenged Claims. *See* DI 24-25. The Petition itself notes that “Yang does not provide numerical examples” for the relevant voltage levels, and fails to clearly state the exact values for each of the identified voltages. *See* Pet. 81-82. Instead, the Petition argues that a POSITA would have “nonetheless understood Yang to render what this limitation requires obvious.” Pet., 81-82. I disagree, and

Petitioner's assertions that it would be obvious for **Vpre_dmy** to have an "intermediate" in between **Vbypass** and **Vpre_OD** is unsupported by the record. See Pet. 81-82. In particular, the Petition has failed to identify anything in Yang to indicate that **Vpre_dmy** is somehow greater than **Vbypass**, or that it would have been obvious to use a value for **Vpre_dmy** that is any different than **Vbypass**. To the contrary, these voltages serve a similar purpose and are depicted in Yang as having *identical* values. The fact that they have identical values can be seen clearly by placing copies of the **Vbypass** and **Vpre_dmy** waveforms side-by-side, as shown in Fig. 8 below:



Yang. Fig. 8B (color annotations added). Moreover, it makes sense in the context of Yang's system to use identical values for **Vpre_dmy** and **Vbypass**. Doing so reduces costs and advantageously simplifies the design of a memory device by requiring only a single voltage generator to generate the signals, rather than being required to use two separate voltage generators. By comparison, there is nothing in Yang to suggest that different values would be used for **Vbypass** and **Vpre_dmy**,

much less that **Vpre_dmy** in particular would be implemented as the larger of the two.

142. For at least the reasons above, Yang does not disclose or render obvious applying three “word line pre-pulse signals” to three groups of word lines that have incrementally increasing voltage levels, as required by limitations [1.e.1]-[1.e.4] and [11.b]-[11.e] of independent claims 1 and 11. For at least the same reasons, Yang also does not disclose or render obvious dependent claims 2-7, 9, 12-16, and 18-19.

B. Claims 2 and 12: Yang Does Not Disclose or Render Obvious Groups “Disposed in an Order of Distance from the Selected Word Line”

143. Yang does not disclose or otherwise render obvious groups of word lines “disposed in an order of distance from the selected word line” as recited by dependent claims 2 and 12. Instead, Yang discloses that groups of word lines do not change based on the location of the selected word line.

144. Dependent claim 2 recites: “The memory device of claim 1, wherein the first group of the plurality of word lines, the second group of the plurality of word lines, and the third group of the plurality of word lines ***are disposed in an order of distance from the selected word line*** of the plurality of word lines.” Similar limitations are also found in dependent claim 12.

145. The term “disposed in an order of distance from the selected word line” requires that the word line groups be disposed in order based on the location of the

selected word line. *See* Section VIII.B (Claim Construction). That interpretation is consistent with the plain and ordinary meaning of the term “disposed,” and is supported by both the intrinsic record and the extrinsic record. *Id.* Under that interpretation, Yang does not disclose or render obvious groups of words lines “disposed in an order of distance from the selected word line.” Instead, Yang discloses that location of the selected word line has no influence on how word lines are grouped together for pre-charging. Yang Figure 8C, 25:9-33.

146. Yang discloses that word lines are divided into three groups for the purposes of pre-charging, none of which depends on the location of the selected word line. The first group is “data word line ... that are not programmed. Yang, 24:1-17. The second group is data word lines that are “programmed.” Yang, 24:28-31. Finally, the third group is “dummy word lines.” Yang, 24:18-27. None of these groups is determined based on the location of the selected word line. With respect to “dummy” word lines, these are determined by the layout of the device and where dummy memory cell transistors are placed during manufacturing. As for the “data” word lines, they are placed into two groups based on whether the corresponding memory cells are programmed or unprogrammed. Yang does not disclose or render obvious that these groups of word lines—or any other groups of word lines—are disposed based on a distance to a selected word line. The Petition has also failed to

present any arguments that Yang’s groups of word lines could be modified to depend on a distance from the selected word line.

147. For at least the reasons provided above, Yang fails to teach or render obvious word line groups are “disposed in an order of distance from the selected word line of the plurality of word lines” as required by claims 2 and 12. Rather, as disclosed by Yang, the groups are formed to separate “dummy” word lines, “programmed” data word lines, and “not programmed” data word lines. The groups will be the same regardless of which word line is selected for programming.

C. Claims 3 and 13: Yang Does Not Disclose or Render the “First Group of the Plurality of Word Lines Are Disposed Adjacent to the Selected Word Line”

148. Yang does not disclose or otherwise render obvious “the first group of the plurality of word lines are disposed adjacent to the selected word line.” Instead, as I discussed in relation to claims 2 and 12 in Section XIII.B, Yang teaches that groups of word lines do not change based on the location of the selected word line.

149. Dependent claim 3 recites: “The memory device of claim 1, ***wherein the first group of the plurality of word lines are disposed adjacent to the selected word line***, the second group of the plurality of word lines are disposed between the first group of the plurality of word lines and the select gate line, and the third group of the plurality of word lines are disposed between the second group of the plurality

of word lines and the select gate line.” Similar limitations are also found in dependent claim 13.

150. The term “the first group of the plurality of word lines are disposed adjacent to the selected word line” requires that group to be disposed adjacent to the location of the selected word line. See Section VIII.B (Claim Construction). That interpretation is consistent with the plain and ordinary meaning of the term “disposed,” and is supported by both the intrinsic record and the extrinsic record. *Id.* Under that interpretation, Yang does not disclose or render obvious a groups of words lines “disposed adjacent to the selected word line.” Rather, Yang’s groups are formed without regard to the location of the selected word line. See Yang 24:1-17, 24:18-27, 24:28-31. Instead, the groups of word lines are determined based on whether the word lines are “dummy” word lines, “programmed” data word lines, or “not programmed” data word lines. *Id.* At no point does Yang disclose or otherwise render obvious that a first group “is disposed adjacent to a selected word line,” nor has Petitioner and Dr. Liu provided any argument to suggest that Yang’s groups could be modified to depend on the location of the selected word line.

151. For at least the reasons provided above, Yang fails to teach or render obvious that “the first group of the plurality of word lines are disposed adjacent to the selected word line” as required by dependent claims 3 and 13. Rather, as

disclosed by Yang, the groups are formed to separate “dummy” word lines, “programmed” data word lines, and “not programmed” data word lines.

XIV. CONCLUSION

152. For at least the reasons discussed above, the Challenged Claims of the ’822 Patent are not anticipated or obvious.

153. Furthermore, as discussed in Section III above, I have used my background and experience in forming my opinions that the Challenged Claims are not anticipated or obvious over the asserted prior art.

154. This declaration represents my opinions that I have formed to date on the specific issues for which I have been asked to opine and based on the material currently available to me. I understand that the declaration will be filed as evidence in an *inter partes* review proceeding before the Board. I acknowledge that I may be subject to cross examination in the case and that cross examination will take place within the United States. If cross examination is required of me, I will appear for cross examination within the United States during the time allotted for cross examination. I reserve the right to supplement this declaration to address any new information offered by Petitioner or provided by the Board. Also, I reserve the right to supplement this declaration insofar as Petitioner is permitted to supplement the record with any additional opinions or arguments.

155. I hereby declare that all statements made herein of my own knowledge are true and all statements made herein on information and belief were and are believed by me to be true, and that all statements herein were and are made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code and that any such willful false statements may jeopardize the results of these proceedings.

APPENDIX A

Steven A. Przybylski

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Professional Experience

2003 - Present **President, Verdande Group, Inc**

An inventor, registered patent agent, strong communicator and seasoned technical expert, I provide intellectual property services to a diverse set of clients across the digital electronics spectrum. I provide patent, trade secret, and contract dispute litigation support services, and have extensive experience as a testifying and non-testifying expert in matters before district courts, the PTAB, the ITC, and foreign jurisdictions. I have testified by expert report, deposition, and live testimony on matters of claim construction, infringement, and invalidity, and have assisted in evaluations of potential damages and monetization strategies. With strong written and verbal skills, I provide tutorials to those of both technical and non-technical backgrounds, including judges and attorneys. In addition, I offer pre- and post-transaction portfolio evaluations and due diligence analyses.

I have been retained for these services with regard to:

Computer Systems

Processor design
Processor architecture
Multiprocessing
Graphics systems
Graphics/CUDA processors
Cache memories
Memory systems
Memory modules
Floating point computation
Operating systems
I/O systems
System boot issues

Consumer Electronics

Infotainment systems
Video encoding and decoding
Medical equipment
Embedded systems
Portable electronic systems
User interface design
Wired and wireless networking
Power/energy management
Standards development
Display interconnects
Integrated memories
Digital signal processing
Cloud-based content navigation
and serving

Semiconductors

DRAMs
Flash
SRAMs
Other non-volatile memories
Memory controllers
High-speed interconnects
Signal integrity
2D, 2.5D and 3D packaging
Error detection and correction
Clock distribution techniques
Semiconductor processing
IC and system testing
Computer aided design
FPGAs

2000 – 2003 **Manager, SSM Technologies, LLC.**

I managed, developed and sold a significant patent portfolio relating to DRAMs. Recognizing the intrinsic value of a long-neglected portfolio, I negotiated control of the portfolio and developed a new patent prosecution strategy. I oversaw and participated in the implementation of this strategy, culminating in the issue of a new set of broad method and apparatus claims. I then worked to monetize the portfolio and to maximize return to the inventors and SSM's investors by analyzing the sell/license decision and guiding the stakeholders through the decision-making process. I gathered relevant documentation and analyses, approached likely purchasers, presented interested parties with the collected materials, actively sold the offensive and defensive utility of the portfolio, and orchestrated an auction-style final sales process.

1991 – 2000 **President and Principal Consultant, Verdande Group, Inc**

I have consulted on product strategy, comparative technical analysis, and system-level design in the areas of DRAMs, Flash, SRAMs and other semiconductor memories, computer systems and CPU architecture, and uni- and multi-processor memory hierarchy design. Technical engagements have included serving as memory system architect for Flash and DRAM memory devices and systems. In addition, I offered: general business planning and analysis services to computer and semiconductor companies; intellectual property management, including portfolio evaluation, development and brokering, and litigation support services to IP holders and legal firms; and due-diligence analyses to venture capitalists and securities firms.

My writing and analysis encompasses an extensive range of topics for trade magazines, conferences, and academic journals. As one of the leading independent analysts of the semiconductor memory industry, I wrote (1994) and substantially revised (1996) an 850-page research report entitled *New DRAM Technologies: A Comprehensive Analysis of the New Architectures*, available from the publishers of *The Microprocessor Report*. I have also taught and presented tutorials to both technical and non-technical audiences on subjects including semiconductor memory architecture, memory hierarchy design, and computer systems and CPU architecture. In particular, I have presented over 50 full- and partial-day seminars on these topics to over 2,500 managers, engineers, marketers, and analysts. I have also served on the advisory boards of high-technology start-ups, advising on processor, DRAM and Flash memory trends and general business opportunities.

- 1989 - 1991 **Chief Scientist and Systems Architect, MIPS Computer Systems.**
I played a variety of roles within MIPS, including assistant to the Senior Vice President of Engineering, technical lead for a group of designers that investigated the technical and economic feasibility of developing a companion chip to the R3000 CPU and R3010 FPU, troubleshooter within the High-End Systems Group responsible for taking on any short or long term task that was in need of additional manpower, chief scientist for the group in charge of planning and investigating options for future high-end systems, systems architect for both a new R4000 based symmetrical multi-processor and a low-cost desk-top machine.
- 1990 - 1991 **Consulting Assistant Professor, Dept. of Elect. Eng., Stanford University.**
I designed and taught an advanced graduate level course on cache and memory hierarchy design and supervised the students' research activities. Two groups of students continued their research and ultimately published their efforts under my direction.
- 1989 - 1989 **Postdoctoral Scholar, Department of Electrical Engineering, Stanford University.**
As a postdoctoral scholar, I continued my dissertation research into the analysis of cache behaviour and performance-optimal memory hierarchy design.
- 1984 - 1985 **Computer Architect and Systems Designer, MIPS Computer Systems.**
My main contribution during MIPS' first year was the specification of the architecture and micro-organization of the R2000 VLSI RISC CPU, including the CPU interface and the cache sub-system. I was integrally involved in the implementation of both the CPU and system-level design. My most important role was that of liaison between the VLSI, board-level hardware, compiler and operating system teams.
- 1981 - 1988 **Research Assistant, Department of Electrical Engineering, Stanford University.**
I was a key participant in the MIPS VLSI CPU design team, involved in the design, debugging and testing of the IC design. I also oversaw the development of a prototype CPU board, and subsequently aided in the architectural specification of the MIPS-X VLSI CPU. My dissertation research used analytical and empirical techniques to examine memory hierarchy design from the perspective of optimizing system level performance.

Education

Haas School of Business, University of California at Berkeley, M.B.A. (2000).

Coursework and final project included a combined emphasis on business strategy and financial analysis.

Stanford University, M.S.E.E. (1982), Ph.D. (1988).

Research areas: Computer systems design and VLSI integrated circuit design. Concentrated areas of study spanned the breadth of both electrical engineering and software systems. Topics of extensive coursework included digital systems design, computer architecture, semiconductor devices, error correction codes, control theory, and system software — including user interface design, operating systems, compilers, and I/O systems. Doctoral dissertation title: Performance-Directed Memory Hierarchy Design.

University of Toronto, B.A.Sc. with Honours (1980).

My unique, specially approved course of study within the Engineering Science Programme combined the computer science and electrical engineering degree programs. This provided a broad and deep background in both areas. Coursework and undergraduate thesis covered digital systems design, computer systems, control theory, network analysis, analog circuit design, semiconductor physics, human-computer interfaces, operating systems, compilers, database design, and AI.

Honors and Publications

Awards

Most Influential Paper Award, ACM/IEEE International Symposium on Computer Architecture, 1989, with Mark Horowitz and John Hennessy.

Micro Test-of-Time Award, for one of the ten most influential papers of the first 25 years of the IEEE Micro Symposium, with John Hennessy, Norman Jouppi, Christopher Rowen, Thomas Gross, Forest Baskett, and John Gill. 1994.

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Additional Information

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