

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Case No. IPR2024-00792

U.S. Patent No. 11,468,957

MICRON TECHNOLOGY, INC.,

Petitioner,

-v-

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,

Patent Owner.

REMOTE TESTIMONY OF STEVEN PRZYBYLSKI, PhD

APRIL 17, 2025 - 11:00 A.M. ET

JOB NO. 2025-979889

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APRIL 17, 2025

11:00 A.M. ET

DEPOSITION of STEVEN PRZYBYLSKI, PhD,
before S. Arielle Santos, Certified Court
Reporter, Certified LiveNote Reporter and Notary
Public.

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1 STEVEN PRZYBYLSKI, PhD, Affirmed, Testifies
2 as Follows:

3 THE WITNESS: I do.

4
5 EXAMINATION

6 BY JOHANNES HSU:

7 Q Doctor, good morning. This is
8 Johannes Hsu for -- with Orrick,
9 Herrington & Sutcliffe for Petitioner
10 Micron Technologies.

11 A Hello.

12 Q Good morning. Thank you for
13 being here today.

14 A My pleasure.

15 Q Could you state and spell your
16 name for the record, please?

17 A Steven Alan Przybylski;
18 S-T-E-V-E-N, P-R-Z-Y-B-Y-L-S-K-I.

19 Q Doctor, you have been deposed
20 many times before, correct?

21 A A good number.

22 Q So you are familiar with how

1 this thing will proceed, right?

2 A Generally so, yes.

3 Q Okay.

4 So I am going to skip all that
5 formality since you're well familiar with
6 it, but I just have one request.

7 If someone discusses or tries to
8 discuss this deposition with you before
9 the end of the deposition, such that the
10 court reporter is not aware of it, could
11 you please let us know?

12 A Of course.

13 Q Thank you.

14 Now, is there any reason that
15 will prevent you from testifying
16 competently today?

17 A No.

18 Q Okay.

19 And we are here -- you are here
20 to give testimony regarding the
21 declaration you submitted in the IPR
22 proceeding relating to US Patent No.

1 11,468,957, correct?

2 A That's correct.

3 Q If I refer to that patent by the
4 '957 patent, you understand what I am
5 talking about, right?

6 A Yes, I will.

7 Q Okay.

8 And like we said, you submitted
9 a declaration, and that's Exhibit 2003,
10 that was attached to YMTC's patent owner
11 response, correct?

12 A Yes, I believe so.

13 Q Okay.

14 Do you have -- let's see -- let
15 me -- let's do this.

16 I will put that declaration into
17 the chat so you can have -- I am sure you
18 have a copy of it already, but let me
19 just do this.

20 A Just so we are clear, my files
21 for this case are on a flash drive and
22 that flash drive is not connected to my

1 computer, it's not installed, and I don't
2 have any hard copies of the documents in
3 front of me.

4 Q Okay.

5 A So I will rely on stuff being
6 put in chat, if you don't mind.

7 Q Of course not.

8 So I am putting your declaration
9 into the chat box. Let me know if you
10 receive it.

11 A I have seen it, I am downloading
12 it now.

13 Q Okay.

14 A I have that up.

15 Q Okay.

16 So if you don't mind, let's turn
17 to paragraph 13. I am starting on page
18 5.

19 A Page 5, paragraph 13. I am
20 there.

21 Q Okay.

22 That paragraph contains a table

1 of materials that you reviewed in the
2 preparation of your declaration, correct?

3 A Yes, I reviewed these documents.

4 Q Okay.

5 Now let's go to page 113 of the
6 declaration.

7 A My CV?

8 Q That's right.

9 So I would like to talk about
10 your experience a little bit. It looks
11 like you have worked as a technical
12 consultant since 1991 till the present
13 time, except for roughly three-year break
14 in the early 2000s when you were working
15 at SSM Technologies?

16 Is that a fair statement?

17 ABED BALBAKY: Objection to
18 form.

19 THE WITNESS: My involvement
20 as a technical consultant was in
21 parallel with my role as manager
22 of SSM. It did not stop. Just

1 so -- there -- principally during
2 that time period, I was working
3 for SSM, but I also continued to
4 have some additional consulting
5 work on the side.

6 BY JOHANNES HSU:

7 Q Okay.

8 So you were still working as a
9 consultant as part of the Verdande Group
10 in the years 2000 to 2003; is that
11 correct?

12 A Yes, but at a reduced level,
13 because my principal role there was as
14 SSM Technologies' manager.

15 Q Okay.

16 And your primary role with the
17 Verdande Group is serving as a technical
18 consultant; is that correct?

19 A Yes. The technical and
20 litigation support, intellectual property
21 consultant generally.

22 Q Is the Verdande Group your own

1 consulting company?

2 A My wife and I own the
3 corporation.

4 Q Okay.

5 Does it have any other technical
6 employees?

7 A No.

8 ABED BALBAKY: Objection,
9 relevance.

10 BY JOHANNES HSU:

11 Q Now, during -- go ahead.

12 Was somebody trying to speak?

13 A Not I.

14 Q Now, during your first stint as
15 the president and principal consultant of
16 the Verdande Group, you consulted on
17 product strategy, comparative technical
18 analysis, and system level design; is
19 that correct?

20 A That's how I described it there
21 in my CV, yes.

22 Q Can you briefly describe what

1 product strategy involved?

2 A Product strategy is a broad
3 term, a category of consulting
4 practice in which for me I helped my
5 clients evaluate and navigate a
6 relatively difficult memory marketplace
7 where there's a lot of change going on so
8 I was helping them understand how the
9 memory marketplace was going to impact
10 their products and help them refine or
11 adapt their overall product strategy in
12 -- as a result.

13 (Zoom Interruption and
14 Reporter Clarification.)

15 THE WITNESS: For me, the
16 consulting on product strategy
17 involved helping my clients
18 navigate a difficult and
19 tumultuous memory device and
20 memory module marketplace during
21 that period, helping them
22 understand how those changes in

1 the memory device sphere was going
2 to impact their own products and
3 to adapt or adjust those -- their
4 strategies correspondingly.

5 BY JOHANNES HSU:

6 Q How was the marketplace
7 difficult and tumultuous?

8 A In the DRAM world, there were
9 about a dozen new architectures that were
10 proposed by corporations and consortia
11 and JEDEC body, standardization body;
12 they were all trying to negotiate a
13 dramatic change in performance without
14 significantly increasing cost.

15 So there was these broad
16 selection of new architectures, it was
17 very unclear which were going to survive,
18 became dominant, and, thereby, be the
19 ones that were preferred from a
20 customer's perspective.

21 Q So were you assisting DRAM
22 manufacturers or DRAM users with product

1 strategy?

2 ABED BALBAKY: Objection.

3 Form.

4 THE WITNESS: Both. I was
5 uniquely positioned to straddle
6 the systems and semiconductor
7 worlds so that I can communicate
8 effectively to both the users of
9 semiconductor memories, i.e.,
10 systems companies, as well as the
11 DRAM and semiconductor vendors to
12 make sure that their products were
13 what the systems companies could
14 effectively make use of.

15 BY JOHANNES HSU:

16 Q Okay.

17 But is it fair to say that your
18 role was primarily coming from the
19 systems company and then assisting them,
20 and in that process, also had the
21 collateral benefit to the DRAM
22 manufacturers to make sure that their

1 products meet the systems requirements?

2 A I don't remember specifically,
3 but the mix of clients was fairly equal
4 between the semiconductor vendors and
5 systems companies that would use those
6 devices.

7 So I really had a role in both
8 worlds. And as I said, I was able to
9 effectively straddle that boundary and
10 help companies on both sides of it.

11 Q Can you briefly describe what
12 comparative technical analysis involved?

13 A So comparative technical
14 analysis means to compare things on a
15 technical level so in particular for this
16 time period where I was on top of these
17 dramatic changes in the semiconductor
18 memory marketplace I developed speaking
19 engagements and written documents that
20 contrasted these different architectures
21 that were coming into the marketplace and
22 highlighted their technical and business

1 strengths and weaknesses.

2 (Discussion off the record.)

3 BY JOHANNES HSU:

4 Q Doctor, thank you for bearing
5 with that disruption.

6 Now, could you briefly describe
7 system level design.

8 A System level design is the art
9 of aggregating integrated circuits into a
10 system.

11 Q And could you briefly describe
12 the system level design that you
13 performed during 1991 through 2000, when
14 you were working as a principal
15 consultant with the Verdande Group?

16 A So my expertise was -- is
17 focused on semiconductor memories and
18 processors, and those are among the
19 principal components of any system that's
20 processor based.

21 So my role as a consultant in
22 this space, was to help my clients

1 architect their systems using drawing on
2 the available processors and the
3 available memory types, both at the
4 device and module level, in order to
5 develop systems that were going to be
6 functional and cost and performance
7 effective.

8 Q Now, the description on your CV
9 states that, "Technical engagement have
10 included serving as a memory system
11 architect for Flash and DRAM memory
12 devices and systems."

13 Do you see that?

14 A Yes, I see that.

15 Q Is the system level design work
16 that we just discussed done in your role
17 as this memory system architect?

18 A System design can encompass
19 memory system design, if that's how the
20 overall task is being partitioned.

21 Alternatively, if, for example,
22 a client was a semiconductor vendor, then

1 the memory system design function would
2 be in the abstract and not associated
3 with a particular system.

4 Q So you have done work -- a
5 system level design work for both
6 semiconductor vendors, as well as system
7 suppliers; is that correct?

8 A I think the way I described it
9 is that system level work was principally
10 done for -- to aid the system companies
11 that were my clients, and memory system
12 design and memory device architecture
13 were done principally for the
14 semiconductor vendors that I was engaged
15 by.

16 So there's just a slight shift
17 in terms of how my expertise was best
18 useful to those clients, based on what
19 their business was.

20 Q Now, what type of flash devices
21 were you working with at the time?

22 ABED BALBAKY: Objection.

1 Form.

2 THE WITNESS: That was a long
3 time ago. I don't remember
4 specifically. That was very early
5 in the development of Flash as it
6 evolved from EPROM and EEPROM. So
7 I don't have any specific
8 recollection for that particular
9 timeframe.

10 For the most recent
11 timeframes, I might have a better
12 recollection.

13 BY JOHANNES HSU:

14 Q That timeframe was before the
15 advent of 3D NAND Flash, correct?

16 A I believe so. I think 3D -- 3D
17 Flash was invented a long time ago, the
18 concept of stacking memory cells
19 vertically, but as a commercial Flash
20 product, it's more recent.

21 Again, I don't have the specific
22 dates in front -- in my memory to help me

1 be more specific than that.

2 Q Is it fair to say that in your
3 role as a technical consultant, you are
4 working with products to be
5 commercialized, and so 3D Flash didn't --
6 wasn't relevant at the time because it
7 wasn't yet a commercial product?

8 ABED BALBAKY: Objection.

9 Form.

10 THE WITNESS: Again, I don't
11 remember specifically when 3D NAND
12 Flash became a commercial product
13 so I hesitate to be definitive
14 with regard to the 1991 to 2000
15 timeframe, but generally speaking,
16 that sounds accurate.

17 BY JOHANNES HSU:

18 Q Now, let's move on to your
19 second stint as -- with the Verdande
20 Group starting 2003.

21 The description of this
22 particular time period refers to

1 intellectual property services.

2 What does that refer to?

3 A It refers to patents and trade
4 secrets relating to semiconductor
5 memories, processors, systems, a wide
6 variety of subject matters that I have
7 listed there in my CV.

8 So -- I have helped curate
9 portfolios. I have helped evaluate
10 portfolios before and after transactions.
11 I have helped with cases before the PTAB,
12 as well as the ITC, in various testifying
13 and non-testifying roles.

14 Q So in the part where you would,
15 for example, help with cases before the
16 PTAB and before the ITC, does that
17 overlap with litigation support services?

18 Is that the description on your
19 CV?

20 ABED BALBAKY: Objection.

21 Form.

22 THE WITNESS: Overlap is

1 accurate. It -- I consider the
2 PTAB cases and the ITC to be
3 litigation and so they fall under
4 that rubric, but obviously
5 District Court cases are also
6 litigation.

7 BY JOHANNES HSU:

8 Q And would it also be fair to say
9 that your description of intellectual
10 services encompasses what your CV refers
11 to as pre- and post-transaction portfolio
12 evaluation and due diligence analysis?

13 A Yeah, that's what I described in
14 that paragraph; that among the
15 intellectual property services, I do due
16 diligence and portfolio evaluation
17 services.

18 Q Do these services that you have
19 described generally involve analyses of
20 documents, such as patents, technical
21 documents, publications, et cetera?

22 A What was the last word you said?

1 I couldn't understand it.

2 Q Let me repeat the question.

3 Do these services that you have
4 described generally involve analyses of
5 documents, such as patents, technical
6 documents, or publications?

7 A Yes. I mean, we deal with
8 documents of all varieties every day. So
9 reviewing documents is an essential part
10 of what I do.

11 Q Can you put a percentage on what
12 part of your day involves reviewing
13 documents?

14 ABED BALBAKY: Objection.
15 Relevance.

16 THE WITNESS: That varies
17 widely from zero to 100 percent,
18 depending on what I am doing on
19 that particular day.

20 BY JOHANNES HSU:

21 Q How about on average, in the,
22 say, past 10 years, can you put a rough

1 percentage on that?

2 A No. I hesitate to put a rough
3 percentage on it -- on a day-by-day and
4 client-by-client and
5 activity-by-activity. So it's obviously
6 dealing with documents of all forms is a
7 very high fraction of what I do, but a
8 concrete number, no, I hesitate to put
9 that.

10 Q Have you worked with actual NAND
11 Flash devices as part of your
12 intellectual property services?

13 A Yes.

14 ABED BALBAKY: Objection.
15 Form.

16 BY JOHANNES HSU:

17 Q And is that associated with a
18 particular litigation matter?

19 ABED BALBAKY: Objection,
20 foundation.

21 THE WITNESS: There have been
22 numerous clients in the last

1 two decades where I have done work
2 on NAND Flash in conjunction with
3 my retention.

4 BY JOHANNES HSU:

5 Q And by "NAND Flash," you are
6 referring to an actual product, correct?

7 ABED BALBAKY: Objection.
8 Form.

9 THE WITNESS: I was referring
10 to actual products, as well as
11 documents describing inventions
12 and potential products, as well as
13 actual documents -- actual
14 products.

15 So it transcends both the --
16 the entire spectrum of designs
17 from the hypothetical to the
18 commercial.

19 BY JOHANNES HSU:

20 Q You developed a new NAND Flash
21 architecture in the 2000s, correct?

22 A I contributed to that. That

1 was -- I was a principal architect on the
2 high-level architecture, but then I was
3 involved in the development of that
4 architecture into a particular design.
5 So it was both in the abstract sense of
6 developing an architecture, as well as
7 the development of potential products.

8 Q Could you describe that in a
9 little more detail.

10 Let's start with the high-level
11 architecture work. What did that
12 involve?

13 A So a memory device architecture
14 specifies a variety of different aspects
15 of a semiconductor memory device. That
16 specification is essentially the contract
17 between the producers of the device and
18 the users of the device so that the users
19 can design the part into their systems
20 and it will work.

21 So the specifications define
22 everything from the physical nature of

1 the device, what package it's in, which
2 pins carry which signals. It also
3 includes the logical definition of the
4 device; what commands does it do, how do
5 you get it to do those demand --
6 commands, what is the addressing scheme
7 for volatile versus non-volatile
8 memories, how does that impact the
9 operation of the device.

10 It also specifies the temporal
11 characteristics of the device; how do you
12 at a very granular level control the
13 device to make it do what it -- what you
14 want it to do, and what timeframe does it
15 do that. So the physical, logical,
16 temporal, also -- test is also frequently
17 a part of that architecture as well.

18 So all of these aspects together
19 -- come under the overarching rubric of
20 memory device architecture.

21 Q So basically, how the outside
22 world interfaces or interacts with the

1 memory device.

2 Is that a fair characterization
3 of that work?

4 A Yes. In the broad sense of
5 interfaces, yes. I mean, you could --
6 your question could be interpreted more
7 narrowly, where interface is purely an
8 electrical or signaling characteristic.
9 But the way I have been using the term
10 "architecture" here today it's much
11 broader than that.

12 To use the metaphor again that I
13 used previously, the specification of the
14 architecture allows the semiconductor
15 vendor to design a part that can be
16 purchased by a systems company that will
17 work and the specification is the
18 document that describes what to build for
19 the semiconductor vendors and how to use
20 it for the systems vendors.

21 Q Now, the other part of this
22 architecture work you mentioned was the

1 development of potential products.

2 Could you elaborate on that
3 briefly?

4 ABED BALBAKY: Objection to
5 form.

6 THE WITNESS: So to the
7 extent that my clients were
8 involved in designing specific
9 products, I helped them with that
10 by -- everything from very
11 high-level recommendations to
12 actual low-level design work, all
13 the way down to internal memory
14 device block diagrams and doing
15 analyses of signal integrity on
16 the interfaces and so forth.

17 So again, it's -- my
18 expertise in this field is broad
19 and extends across several
20 different levels of abstraction.

21 BY JOHANNES HSU:

22 Q Now, you also developed a

1 universal memory interface that was
2 optimized for use in heterogeneous memory
3 systems, right?

4 A Are you reading from the CV?

5 Q I am reading, I think, from
6 paragraph 10 of your declaration.

7 A Okay. Let me go there then.

8 Q Page 4.

9 A Thank you.

10 Would you repeat the question,
11 please.

12 Q Certainly.

13 You also developed a universal
14 memory interface that was optimized for
15 use in heterogeneous memory systems,
16 correct?

17 A Yes. That's what I described in
18 my paragraph 10.

19 Q Could you briefly describe that
20 interface.

21 A Traditionally, and to this day,
22 NAND Flash devices and DRAMs have

1 dramatically different interfaces at
2 practically every level of abstraction.
3 What that -- what I did for that client
4 was to abstract a single memory
5 architecture and interface design that
6 would be efficient and effective for
7 connecting both DRAMs and Flash devices
8 to a singular memory controller.

9 Q So would it be fair to say that,
10 again, this is a task that is more
11 dealing with how the external world
12 interfaces or interacts with these memory
13 devices DRAM and Flash?

14 ABED BALBAKY: Objection,
15 form. Objection, foundation.

16 THE WITNESS: The
17 specification and the definition
18 of the architecture includes that.
19 But in order to be an effective
20 architecture, it is developed in
21 response to what is practical on
22 the internals of the memory

1 devices.

2 So although the universal
3 architecture included facilities
4 for high-speed communication with
5 both DRAMs and -- on their time
6 scale, and Flash devices on their
7 time scale, in order to do that
8 effectively, it drew very heavily
9 on the internal natures of those
10 two types of devices.

11 BY JOHANNES HSU:

12 Q Which year in the 2000s did you
13 work on this?

14 A That was in the latter half of
15 the aughts.

16 (Reporter Clarification.)

17 THE WITNESS: Aughts -- the
18 2000s.

19 BY JOHANNES HSU:

20 Q So somewhere around 2006 through
21 2009 timeframe?

22 A I don't have my records in front

1 of me to know exactly when I was engaged
2 in that project. It's been almost
3 two decades. So it's somewhere in that
4 timeframe, but I hesitate to be more
5 precise than the second half of the
6 2000s.

7 Q We can set aside your
8 declaration for now.

9 A Okay.

10 Q And I am going to drop in what
11 has been already marked as Exhibit 1001.
12 Let me know if you get it.

13 A I see it there. I am
14 downloading it now.

15 Q Okay.

16 A Okay. I am looking at
17 Exhibit 1001 front page.

18 Q And that is the '957 patent that
19 is the subject matter of this IPR
20 proceeding, correct?

21 A That is correct.

22 Q Let's turn to Figure 2 of the

1 patent.

2 A Yes, I am looking at Figure 2.

3 Q What does Figure 2 show?

4 A Figure 2 is described in Column
5 5 as a cross-section view of a 3D NAND
6 memory device, in accordance with
7 exemplary embodiments of the disclosure.

8 Q Does this cross-sectional view
9 show a staircase structure --

10 (Simultaneous Crosstalk.)

11 ABED BALBAKY: Objection --

12 I'm sorry, can you repeat the
13 question. I interrupted you
14 there.

15 JOHANNES HSU: Sure.

16 BY JOHANNES HSU:

17 Q Does this cross-sectional view
18 show a staircase structure as is it
19 commonly known?

20 ABED BALBAKY: Objection,
21 relevance. Objection, scope.

22 THE WITNESS: So Column 8 of

1 the '957, starting at line 50,
2 says, "Still referring to Figure
3 2, word line layers 12a to 12p can
4 be formed in a stair-cased
5 configuration in the staircase
6 regions, 200A to 200B, and so
7 forth.

8 BY JOHANNES HSU:

9 Q So is your answer to my previous
10 question a yes?

11 A I think that as described in
12 Column 8, it uses the word staircase
13 configuration in a staircase region, so
14 it seems so to me, but I am just reading
15 the patent.

16 Q Okay.

17 Would you have an objection if I
18 refer to what the patent refers to as a
19 staircase configuration as a staircase
20 structure?

21 ABED BALBAKY: Objection.

22 Form.

1 THE WITNESS: I don't see an
2 advantage to calling it a
3 staircase structure instead of a
4 staircase configuration, but I
5 will understand what you mean if
6 you refer to it that way.

7 BY JOHANNES HSU:

8 Q That sounds good. And I will
9 try to remember to refer to it as a
10 staircase configuration, but if I refer
11 to it as a "staircase structure," to me,
12 they are the same thing.

13 A And I will follow your lead.

14 Q Now, what is a memory stream?

15 A So in the context of the '957
16 and NAND Flash devices, the concept of a
17 memory string or memory cell string is
18 introduced in Column 7. It is the
19 structure that is illustrated in Figure
20 3, where you have a collection of
21 serially connected memory cells in a
22 string configuration.

1 Q And Figure 3 shows a circuit
2 diagram, correct?

3 A An annotated circuit diagram, I
4 would say, but, yes. I think schematic
5 would be the best way to describe what
6 that is.

7 Q Does the memory string that's
8 shown in a schematic in Figure 3, has a
9 physical correspondence in Figure 2?

10 A I am having trouble finding
11 exactly -- oh, there it is. Figure 3 is
12 described in Column 9, top of Column 9,
13 and it refers to the strings 300A, 300B,
14 and describes its -- the transistors that
15 are formed within the strings --
16 (Reviewing) -- not seeing a specific
17 reference linking Figures 2 and 3
18 together.

19 I think a POSITA looking at them
20 and reading the '957 would understand
21 that the strings are formed vertically
22 within the staircase structure, as you

1 use.

2 Q Where in the staircase structure
3 are the memory strings located?

4 ABED BALBAKY: Objection,
5 form. Objection, foundation.

6 THE WITNESS: So reading from
7 Column 8 of the '957, beginning
8 Line 27, The array Region 200
9 [sic] can include a plurality of
10 channel structures 18.

11 Then it goes on to say that
12 each of the channel structures 18
13 can extend through the stack and
14 be coupled to word line layers to
15 form respective vertical NAND
16 memory cell strings.

17 So the -- in Figure 2, item
18 18 is an example of where a memory
19 cell string would be found.

20 BY JOHANNES HSU:

21 Q In Figure 2, there is one
22 vertical structure that resides within a

1 box 18.

2 Do you see that?

3 A Yes. Box 18 is a hashed box and
4 there is a structure shown within it.

5 Q Now, there are four additional
6 vertical structures that appear identical
7 to what is enclosed within box 18,
8 although they are not annotated as such.

9 Do you agree with that?

10 A (Reviewing.) Again, reading
11 from that same portion of Column 8, "The
12 array region 200A can include a plurality
13 of channel structures 18."

14 So although it shows four, which
15 is a plurality, in any real device there
16 would be a great many more than four.

17 Q So each of those five represents
18 a memory stream, correct?

19 A It doesn't actually show the
20 memory string details within Figure 2,
21 it's much too abstract. But that is
22 where they would be found within those

1 channel structures as articulated in
2 Column 8.

3 Q And as shown in Figure 3, each
4 of these memory strings comprise --
5 comprises a number of transistors,
6 correct?

7 A (Reviewing.) Yes. The memory
8 cells made from charge trapping Flash
9 memory cells are shown in Figure 3 and
10 annotated as MC with a subscript.

11 Q And so the channel structures --
12 strike that.

13 So the memory strings shown in
14 Figure 2 would comprise these transistors
15 that are denoted as memory cells,
16 correct?

17 ABED BALBAKY: Objection.

18 Form.

19 THE WITNESS: Yeah. Again,
20 referring back to figure -- Column
21 5, it says that Figure 3 is a
22 schematic diagram of NAND memory

1 cell strings.

2 So that's -- those are the
3 transistors and connections that
4 make up a memory cell string in
5 each of the two shown there in
6 Figure 3.

7 BY JOHANNES HSU:

8 Q Right, but I would like to bring
9 your attention back to Figure 2.

10 We discussed the fact that
11 Figure 2 illustrates five memory strings,
12 right?

13 A (Reviewing.) What it formally
14 says is that it shows five channel
15 structures. Figure 2 doesn't have the
16 detail to show the actual strings, but it
17 indicates that the channel structures
18 are -- that the -- within the channel
19 structures are formed, the memory cell
20 strings.

21 Q So I just want to make sure we
22 are on the same page and I am not trying

1 to draw distinction between channel
2 structure, well -- strike that.

3 So you stated that the channel
4 structures are formed within the cell
5 strings, correct?

6 ABED BALBAKY: Objection.
7 Form.

8 THE WITNESS: That's not what
9 I said, no.

10 BY JOHANNES HSU:

11 Q Okay.

12 You stated the channel
13 structures are within the -- are formed
14 -- strike that.

15 If I am understanding you
16 correctly, you said that memory
17 cell strings are formed within the
18 channel structures; is that
19 correct?

20 A Yes. I think that's how a
21 POSITA would understand the disclosure of
22 Column 8, lines 27 through 43.

1 Q So is it the case that within or
2 at these channel structures, are the
3 transistors that form the memory cells?

4 A Again, reading from Column 8, it
5 says, beginning at line 33, "The vertical
6 NAND memory cell string can include one
7 or more top select transistors, a
8 plurality of memory cells (MCs), and one
9 or more top select transistors..." and so
10 forth.

11 So the answer is that this
12 paragraph clearly indicates that the
13 memory cells which comprise memory cell
14 transistors, are formed within the
15 string.

16 Q Now, where is a memory cell
17 located within this staircase
18 configuration?

19 A (Reviewing.) Again, the
20 disclosure of Column 7 and 8 of the '957
21 talking about Figures 2 and 3 indicate
22 that the memory cells are formed serially

1 within the string and they connect to
2 word line layers.

3 So they are, generally speaking,
4 formed at or near the intersections of
5 word line layers and a channel structure.

6 Q So for example -- strike that.

7 Do you understand the
8 annotations -- or the designators 12a, b,
9 c, et cetera, to denote a word line layer
10 in Figure 2?

11 A Yes. That's exactly what it
12 says at the top of Column 8, that the
13 memory array region is arranged between
14 the staircase regions and is formed in a
15 stack of alternating word line layers,
16 12a to 12p...

17 So the 12a to p are word line
18 layers.

19 Q Okay.

20 So to translate your previous
21 answer into a couple concrete examples,
22 there is a memory cell transistor located

1 at the intersection of word line layer

2 12b and memory string 18, correct?

3 A (Reviewing.) Repeat the
4 question, please.

5 Q Sure.

6 To translate your previous
7 answer into a couple concrete examples,
8 would you agree that there is a memory
9 cell transistor located at an
10 intersection of word line layer 12b in
11 the memory string that is within the
12 annotated box 18?

13 A (Reviewing.) It's not clear
14 immediately whether 12b, the word line
15 12b, connects to a select transistor or a
16 memory transistor.

17 Certainly 12a is a select line,
18 not a memory word line. So it's
19 connected as would be shown in Figure 3
20 to the BSG -- BST 302, not one of the MC
21 memory cells.

22 But aside from that lack of

1 precision, it's -- generally speaking,
2 that there are transistors at those
3 locations, whether they are a memory cell
4 transistor or some other dummy transistor
5 or select transistor is not clear for
6 word line 12b, in particular.

7 Q Just to wrap up the concrete
8 example questions, would you agree that
9 there is also a transistor at the
10 intersection of word line layer 12p, in
11 the memory string that resides within
12 the dashed rectangle box annotated 18?

13 A (Reviewing.) Again, a similar
14 situation happens with 12p as in with
15 12b, as we were just talking, although
16 it's clearer here.

17 Column 8, line 8, it says that,
18 word line layer 12p can be a TSG layer in
19 the device 100. As illustrated in Figure
20 2, 12p is the topmost word line, and
21 looking at Figure 3, the topmost
22 transistor in the string is -- and by

1 topmost, I mean closest to the bit line,
2 that is -- that is a select transistor,
3 not a memory cell transistor.

4 Q In your opinion, is there a
5 difference between a word line layer
6 that's connected to a memory cell versus
7 a select line that's connected to a top
8 select gate?

9 A There can be, certainly. It
10 depends on the overall organization of
11 the memory device and its partition into
12 plains, blocks, and pages. The select
13 transistor word line may be connected to
14 a different number of select transistors
15 than a regular word line would be
16 connected to memory cells.

17 Q Could you clarify what you meant
18 by the "transistor word line may be
19 connected to a different number of select
20 transistors"?

21 A So in a NAND Flash, 3 NAND Flash
22 memory device, the word lines connect to

1 a large number of memory cells in a
2 plurality of strings.

3 So the number of memory cells at
4 a particular word line controls is a
5 large number. The number of select
6 transistors that are controlled by a
7 common select control line, TSG, for
8 example, in Figure 3, may be different in
9 some implementations.

10 THE WITNESS: We have been
11 going about an hour, are we done
12 with this section or do you --

13 (Simultaneous Crosstalk.)

14 JOHANNES HSU: Just a few
15 more minutes if you don't mind.

16 THE WITNESS: Just a few.

17 JOHANNES HSU: Yes.

18 BY JOHANNES HSU:

19 Q So looking back at Figure 2.

20 Do you see on the bottom left
21 there is an axis legend X, Y, and Z?

22 A I see that.

1 Q So you understand it's showing
2 the Y axis is going across the page and Z
3 axis is pointing up, correct?

4 A Yes, that's what the axis shows.

5 Q And the X axis would be going in
6 and out of the page if it were 3D?

7 A And that is consistent with what
8 the text describes this as a
9 cross-section.

10 Q Now, you just mentioned that a
11 word line can be coupled to a large
12 number of memory cells, correct?

13 A Generally that is the case, yes.

14 Q And looking at what is
15 illustrated in Figure 2, just so we have
16 something to look at, is it the case that
17 these memory cells would be located on --
18 at different locations of that word line?

19 For example, here it shows five
20 across the Y axis?

21 ABED BALBAKY: Objection.

22 Form.

1 THE WITNESS: I think the
2 point you are trying to make is
3 better made in Figure 3, not in
4 Figure 2, because it shows that
5 each word line is connected to one
6 memory cell in each string that
7 that word line is connected to.

8 I think you are trying to get
9 at whether a word line can control
10 two memory cells in one string.
11 But if I am wrong, please repeat
12 the question.

13 BY JOHANNES HSU:

14 Q Sure.

15 But would you agree that these
16 two word lines, for example, they don't
17 occupy the same space. They are
18 separated physically on the word line,
19 correct?

20 ABED BALBAKY: Objection.
21 Form.

22 THE WITNESS: You misspoke.

1 Please repeat the question.

2 BY JOHANNES HSU:

3 Q Sure.

4 You said that, as an example,
5 Figure 2 -- Figure 3 shows the same word
6 line controlling two memory strings.

7 Now, my question is, would you
8 agree that these two memory strings that
9 are controlled by the same word line are
10 located at different locations of the
11 word line?

12 A First, let me clarify that the
13 word lines control specific memory cells
14 in the strings. So if you want to
15 extrapolate that to say the word lines
16 controls the entire memory string, that's
17 a stretch. But I will understand what
18 you mean.

19 It is obvious that separate
20 strings are not physically coincident.
21 Otherwise, they would be one string and
22 not two; and, therefore, they must be at

1 different locations, and that the memory
2 cells controlled by a common word line in
3 different strings must necessarily be in
4 different locations.

5 JOHANNES HSU: Let's go ahead
6 and take a break, please.

7 THE WITNESS: Ten minutes,
8 please.

9 JOHANNES HSU: Of course.
10 Thank you.

11 (Whereupon a Recess Commenced
12 at 12:14 p.m. and Testimony
13 Recommenced at 12:26 p.m. EDT.)

14 BY JOHANNES HSU:

15 Q We are back on.

16 Doctor, just before the break,
17 you discuss select transistor versus
18 memory transistor.

19 Do you recall that?

20 A I recall using those terms, yes.

21 Q And also you used the terms
22 select line and memory word line,

1 correct?

2 A I used those terms, yes.

3 Q Just so that we are on the same
4 page, is an example of what you refer to
5 as a select transistor what the patent
6 refers to as top-select-gate or
7 bottom-select-gate?

8 A (Reviewing.) So the select
9 transistors have gate connections, which
10 is how they are controlled, it's their
11 control point. So a select gate is a
12 layer that is comparable to a memory cell
13 gate layer or word line layer, those two
14 are synonymous. But they are conveying
15 different things into the memory array.

16 Q What did you mean that a select
17 gate layer is comparable to a gate layer
18 or word line layer?

19 A So again, referring to Column 8,
20 and to use the terminology of the '957,
21 there are word line layers are conducting
22 and they connect generally to gates of

1 transistors in the memory strings, and if
2 -- the patent uses the same item numbers
3 for these word line layers, regardless of
4 whether they are connected to a memory
5 cell gate or a select transistor gate.

6 Q Do you understand from the
7 patent that since it uses the same
8 reference designator number for both the
9 top-select-gate lines, bottom-select-gate
10 lines, as well as word line layers, that
11 the patent is not distinguishing them for
12 purposes of controlling the respective
13 transistors?

14 ABED BALBAKY: Objection.

15 Form.

16 THE WITNESS: I'm sorry, that
17 question is nonsensical to me.
18 The patent says what it says. It
19 uses these unit numbers,
20 consistently has different names
21 for different unit numbers. It
22 speaks for itself.

1 BY JOHANNES HSU:

2 Q Let me clarify by ways of an
3 example.

4 Looking again at Figure 2,
5 reference designator 22 denotes a word
6 line contact, correct?

7 A Word line contacts 22 are shown
8 in Figure 2, yes.

9 Q Okay.

10 And as we previously discussed,
11 reference designator 12 followed by a
12 letter, denotes a word line layer,
13 correct?

14 A Yes. Again, reading from Column
15 12, 12a through 12p are called word line
16 layers, even though they don't all
17 connect to memory cells.

18 Q So the word line contacts and
19 word line layers are represented by
20 different reference designators,
21 indicating that they are different
22 components, correct?

1 A The use of designators in a
2 patent figure is for purposes of
3 clarifying what the text is referring to.
4 In this case, the drawer of the Figure 2
5 has used different item numbers for the
6 word line contacts, down into the
7 staircase structures, as well as the
8 horizontal word lines -- word line
9 layers, sorry, 12a through 12p.

10 Q Now, you mention a little while
11 ago that the select gate lines are used
12 to control the gates of the corresponding
13 select gate transistors; is that correct?

14 A I think you misspoke a little
15 bit. Select gate line -- we have word
16 line layers, we have select gates on
17 select transistors.

18 Maybe just repeat the question,
19 please.

20 Q Let me rephrase the question.

21 A Please.

22 Q You stated earlier that the

1 select transistors have gate connections
2 which is how they are controlled.

3 Do you recall that?

4 A Yes. That's true of almost all
5 types of transistors, that they have a
6 gate connection for controlling the flow
7 of current through their channel.

8 Q So that would also be true of
9 memory cell transistors, correct?

10 A Generally speaking, yes.

11 Q And is that the reason why
12 literature in the field commonly refers
13 to the gate as the control gate?

14 ABED BALBAKY: Objection.

15 Form.

16 THE WITNESS: Yes. A POSITA
17 would understand both terms to be
18 referring to the gate of a MOS
19 transistor.

20 BY JOHANNES HSU:

21 Q Are control gates also referred
22 to as word lines?

1 A No.

2 Q What does gate voltage refer to?

3 A Gate voltage refers to a voltage
4 on a gate transistor.

5 Q Would that be the same as a
6 voltage applied on a gate terminal of the
7 transistor?

8 A Yes. A POSITA would generally
9 recognize those two terms as being
10 synonymous, that the voltage applied to
11 the gate of a transistor can be called
12 the gate voltage.

13 Q Now, the control gates of these
14 memory cell transistors are coupled to
15 word line layers, right?

16 A Yes, that's fair.

17 Q And what is a POSITA's
18 understanding of where the gate of a -- a
19 memory cell transistor is located?

20 ABED BALBAKY: Objection to
21 form.

22 THE WITNESS: Well, it's part

1 of the transistor, but exactly
2 where in the transistor depends on
3 the physicality of that
4 transistor, how it's fabricated.
5 So there's no one answer for all
6 types of transistors or even all
7 types of memory cell transistors.

8 BY JOHANNES HSU:

9 Q But regardless of the type of
10 transistors, your previous answer that
11 the gates is coupled to a word line layer
12 in a Flash memory holds true, correct?

13 A That is true. It would be even
14 more precise if you stuck the word NAND
15 in there, and that we are talking
16 specifically not just about Flash but
17 NAND Flash specifically, because there
18 are other varieties of Flash.

19 Q Now, do the word lines serve as
20 a gate of the memory cell transistors?

21 ABED BALBAKY: Objection.
22 Form.

1 THE WITNESS: It depends on
2 the memory type and the physical
3 structure of the memory cell
4 transistors.

5 BY JOHANNES HSU:

6 Q Based on the memory type and the
7 physical structure of the memory cell
8 transistors, as disclosed in the '957
9 patent, do the word lines serve as the
10 gates of the memory cell transistors?

11 A (Reviewing.) I am not finding a
12 specific citation within the '957 that
13 would corroborate that statement. It's
14 certainly true of some 3D NAND Flash
15 commercial devices. But the '957, to my
16 understanding right now, doesn't actually
17 require that, unless there's a citation
18 within the '957 you want to point me to
19 that would expand my knowledge.

20 Q Can you identify the type of 3D
21 NAND Flash for which the previous
22 statement is true as you indicated in

1 your previous answer?

2 A I'm sorry, I missed the question
3 part of that. Can you just repeat it for
4 me, please.

5 Q Sure.

6 Previously -- I am going to
7 rephrase it.

8 Previously, I asked based on the
9 memory type and the physical structure of
10 the memory cell transistors as disclosed
11 in the '957 patent, do the word lines
12 serve as the gates of the memory cell
13 transistors?

14 Do you recall that?

15 A Yes, generally.

16 Q Okay.

17 And then you responded, in part,
18 it is certainly true of some 3D NAND
19 Flash commercial devices, right?

20 A Hm-hm.

21 Q Can you identify some of these
22 3D NAND Flash commercial devices?

1 A No, not off the top of my head.
2 I mean, I know that's generally true of
3 commercially available 3D NAND Flashes,
4 or at least some of them. But can I
5 identify particular part numbers? No.
6 I'm not privy to internal documents,
7 generally speaking.

8 Q So is your testimony that it is
9 generally true of commercially available
10 3D NAND Flash that serve as a gates of
11 the memory cell transistors?

12 ABED BALBAKY: Objection to
13 form. Objection, mischaracterizes
14 his testimony.

15 THE WITNESS: I think I would
16 rephrase it a little bit
17 differently, in that a portion of
18 the word line that is physically
19 adjacent to the gate dielectric or
20 gate oxide, if you prefer, of a
21 memory cell forms the gate of that
22 memory cell at that junction,

1 right at the gate. It's formed by
2 the same material that is making
3 up the word line layer.

4 BY JOHANNES HSU:

5 Q How far does that portion
6 extend?

7 A That portion of the material
8 that is making up the gate that is
9 relevant to the operation of the
10 transistor, is exactly at the boundary.
11 That's where the electric fields are
12 generated that cause the operation of the
13 memory cell transistor.

14 Q What boundary are you referring
15 to?

16 A I am talking about the boundary
17 between the material that makes up the
18 word line layers, as to use the 597 [sic]
19 terminology, and the gate dielectric or
20 gate oxide that separates that from the
21 charge-trapping layer or the channel
22 itself.

1 Q So let me just make sure I am
2 understanding your testimony.

3 You are saying that the word
4 line portion exactly at a boundary
5 between the word line and the gate
6 dielectric, serves as the gate terminal
7 of the transistor; is that correct?

8 A It would be more precise to say
9 that the portion of the word line layer,
10 because that's referring to the material
11 that is a conductor, that is physically
12 adjacent to the gate dielectric -- it's
13 that boundary that the fields that
14 control the operation of the transistor
15 are generated based on the voltage of
16 that conductor at that point, at the
17 dielectric.

18 And so that portion of the
19 conductor is the gate, and it has a
20 voltage and that is the gate voltage of
21 the transistor.

22 Q So where would a POSITA draw

1 that boundary between what you considered
2 the gates of the memory cell transistor
3 and the word line?

4 ABED BALBAKY: Objection.
5 Form.

6 THE WITNESS: I'm sorry, that
7 wasn't clear to me at all. Could
8 you repeat the question, please.

9 BY JOHANNES HSU:

10 Q I am going to try to hopefully
11 make it more clear.

12 You testified that there's a
13 boundary between the word line layer and
14 the gate.

15 A No.

16 Q Okay.

17 So could you help me understand?

18 A So there is a word line layer in
19 the '957 patent, many of them, and they
20 are conductive and they are in
21 commercially-available devices, not shown
22 in the '957, that the word line layer is

1 in contact with the gate dielectric of
2 the memory cell transistors.

3 The conductive layer at that
4 boundary between the word line layer and
5 the dielectric, is the gate. And its
6 voltage is the gate voltage.

7 Q How -- strike that.

8 Does that conductive layer
9 add a boundary between the word
10 line layer and the gate dielectric
11 have some sort of width?

12 A Well, the width of the word line
13 layer is the entire width of the layer as
14 shown in Figure 2 from one extreme of the
15 staircase structure to the opposite
16 staircase structure. So the width of the
17 word line layer extends the entire width
18 of the integrated circuit in the
19 implementation shown in Figure 2.

20 BY JOHANNES HSU:

21 Q But do you consider that to be
22 -- that entire width to be the gate of

1 the memory cell transistor?

2 A No.

3 Q So can the gate of the memory
4 cell transistor be categorized to have
5 some width?

6 A Well, first of all, when we are
7 talking about transistors, length and
8 width have to do with the channel, not
9 with the gate. So you should adjust your
10 terminology correspondingly and re-ask
11 the question.

12 Q I was using the word "width" to
13 be consistent with what is shown in
14 Figure 2, where, for example, you also
15 agree that the word line layer has a
16 width running horizontally.

17 A So in the wide direction.

18 Q In the wide direction, correct.

19 A So in this structure, where a
20 large conductive layer, being a word line
21 layer, connects to many gate -- forms
22 many gates on many transistors at

1 different locations around it. The
2 actual gate of each transistor, as I have
3 indicated previously, is just that layer
4 at the boundary without any thickness of
5 note.

6 That differentiates this
7 structure from how transistors are made
8 in many other types of devices where
9 there is a physical layer that has a
10 height that -- and that whole height is
11 considered the gate because that whole
12 area is built together at one time.

13 For these structures, for the 3D
14 NAND Flash structures, that is not -- an
15 accurate way to describe the relationship
16 of the memory cell to their gates to the
17 word line layers and the word lines that
18 control the transistor.

19 Q What did you mean by the phrase
20 "at the boundary without any thickness of
21 note"?

22 A As I have said several times

1 already, in this structure, the gate is
2 the portion of the word line layer that
3 is physically in contact with the gate
4 dielectric because that's where the
5 electric fields originate.

6 Q But is it your testimony that
7 this portion has no finite thickness?

8 A The word line layer is very big.
9 The portion of the word line layers that
10 constitute the gate with a gate voltage,
11 is the immediate portion that is adjacent
12 to and touching the word -- the gate
13 dielectric.

14 Q So I am still trying to
15 understand because you used the word
16 "portion." You also used the word
17 "boundary."

18 I am trying to understand
19 exactly what part of the word line layer
20 you are referring to as the gate.

21 A As I have said repeatedly
22 already, it is the portion of the word

1 line layer that is physically in contact
2 and adjacent to the gate dielectric.

3 Q Does this portion has a width in
4 the wide direction of Figure 2 -- strike
5 that.

6 Does this portion has a non-zero
7 width in the Y direction of Figure 2?

8 A Conceptually, no. Conceptually,
9 the gate is formed by the portion of the
10 word line layer that is touching the gate
11 dielectric. It is only the material
12 that's touching the dielectric that is
13 presenting a voltage at corresponding
14 electric fields into the substance, the
15 body of the transistor.

16 So whether -- the fact that that
17 material extends beyond the boundary for
18 great distances across the entire
19 integrated circuit, is irrelevant to the
20 operation of the memory cell. And so we
21 don't consider the entire extent of the
22 word line layer to be the gate. It's

1 just the portion that's talk touching the
2 gate dielectric that is the gate.

3 Q Now, going back to the select
4 line versus memory word line. If I may
5 direct your attention to Column 8,
6 line -- starting at line 2.

7 It says, [As Read:] The word
8 line layers, 12a through 12p can include
9 one or more bottom slight gate (BSG)
10 layers, gate layers (layers) and one or
11 more top-select-gate (TSG) layers that
12 are arranged sequentially over the
13 substrate 10.

14 Did I read that correctly?

15 A Yes, you did.

16 Q Do you understand this sentence
17 to imply that the BSG layers, the gate
18 layers or word line layers, and the top
19 select gate or TSG layers, are made from
20 the same material?

21 A (Reviewing.) I am not aware of
22 any disclosure within the '957 that all

1 of the word line layers 12a to 12p, are
2 constructed identically. If you know of
3 a passage that speaks to this, I would
4 appreciate a pointer.

5 Q Based on the knowledge of a
6 POSITA, are these different layers
7 typically constructed from the same
8 materials?

9 A I think a POSITA would
10 understand that they could be but they
11 would not necessarily have to be and that
12 it would vary potentially from vendor to
13 vendor, from family to family, from
14 design to design.

15 Q Now, a memory cell, as you
16 mentioned earlier, includes a transistor,
17 right?

18 A Not all memory cells include
19 transistors. All NAND Flash memory cells
20 include a transistor.

21 Q I appreciate that clarification.
22 And just in case I forget it again, when

1 I am referring to NAND Flash in the
2 context of this deposition, I do have in
3 mind NAND Flash memory -- memory devices.

4 A You mean 3D NAND Flash memory
5 devices or all NAND Flash memory devices?

6 Q 3D. Thank you for that
7 clarification.

8 A Okay. I will try to remember
9 that, but I will reserve the right to
10 insert those qualifiers, if you skip
11 them.

12 Q So these transistors of NAND
13 Flash memory cells, they have a gate, a
14 source, and a drain, right?

15 A They also have a substrate, but
16 we generally talk primarily about the
17 gate drain and source as the connection
18 points to the transistor.

19 Q Does your answer also apply to
20 the transistor at the top select gate?

21 A Well, that's obviously a
22 different type of transistor. It's not a

1 charge-trapping transistor, as shown in
2 Figure 3. But it too has a source, a
3 drain, and a gate.

4 Q Does it also have a substrate?

5 A Presumably. It's shown as a MOS
6 transistor. So it has some material that
7 the channel is formed in and that's -- if
8 not -- not -- may or may not want to call
9 it a substrate, as opposed to just the
10 body of the transistor because these are
11 not made in a substrate. They are made
12 in a vertical column.

13 So perhaps I was a little bit
14 generous when I used the word substrate
15 instead of body earlier.

16 Q So setting aside for the moment
17 the question about body versus substrate,
18 would you agree that TSG cells, memory
19 cells, and BSG cells all have source
20 terminals, gate terminals, and drain
21 terminals?

22 A Yes. Figure 3 illustrates those

1 transistors and their connection points.

2 Q And all of these transistors are
3 controlled via the gate's voltage,
4 correct?

5 ABED BALBAKY: Objection.

6 Form.

7 THE WITNESS: Each transistor
8 is controlled by, in part, the
9 gate voltage, as well as the
10 voltages on the source, drain, and
11 substrate. But for a lot of these
12 discussions, it's the gate voltage
13 that is principally at issue.

14 BY JOHANNES HSU:

15 Q Now, you mentioned earlier that
16 the patent discloses word line layer 12p
17 can be a top-select-gate layer, correct?

18 A I believe my testimony earlier
19 was towards -- relating Figures 2 and 3
20 to each other, where 12p is the topmost
21 word line layer in Figure 2, and in
22 Figure 3, the first or topmost transistor

1 in the string is the TSG transistor --
2 I'm sorry, TST transistor, 306A. And so
3 if these two are corresponding to the
4 same embodiment, the 12p would be
5 connecting the TSG signal.

6 Q I will just direct your
7 attention back to Column 8 again, lines 6
8 through 8.

9 "...the word line layer 12a can
10 be a BSG layer, and the word line layer
11 12p can be a TSG layer in the device
12 100."

13 Did I read that correctly?

14 A Yes, you did.

15 Q So would you agree that the BS
16 -- strike that.

17 Would you agree that the BSG
18 layer and the TSG layer are both
19 part of the staircase
20 configuration that's shown in
21 Figure 2?

22 A Yes. That paragraph in Column 8

1 explicitly calls all of the 12a through p
2 word line layers, and then further
3 itemizes 12a as a BSG layer. It's also a
4 word line layer. And 12p is a word line
5 layer and it's also a TSG layer.

6 BY JOHANNES HSU:

7 Q Now, what are the layers in
8 between, let's say, the word line layers?

9 A So in between the layers 12a
10 through 12p, the paragraph at the top of
11 Column 8 further discloses that there are
12 insulating layers 14a through 14q over
13 the substrate 10.

14 Q And these are also known as
15 dielectric layers, do you agree?

16 A Dielectrics are insulating, yes.
17 So the two terms are not strictly the
18 same, but they are often interchangeable.

19 Q Would a POSITA understand the
20 insulating layers or dielectric layers
21 14a through 14q to be made from the same
22 dielectric material?

1 A Not necessarily at all. There
2 are -- these dielectrics layers are
3 probably complex stacks made up of
4 multiple thinner layers, even at the time
5 of the filing of the '957. And so it
6 would -- it would be a leap for a POSITA
7 to assume that all of the dielectric
8 layers 14a through 14q were fabricated
9 identically. They might be, but there's
10 no reason in the disclosure to suggest
11 that it is a requirement or an aspect of
12 the disclosure of the '957.

13 Q Now, earlier, we talked about
14 the width of the word line there.

15 Do you recall that?

16 A Yes. We talked about the X, Y,
17 and Z directions of Figure 2.

18 Q Right.

19 Would you agree that these
20 different word line layers have different
21 widths in the Y direction?

22 A It certainly looks that way from

1 Figure 2. I don't recall any specific
2 language in the text to corroborate that.
3 Again, if there is something that I have
4 forgotten, please point me at it.

5 Q But that would be a POSITA's
6 understanding of how these staircase
7 configurations are structures, right? --
8 which is why they are called staircase
9 configurations.

10 Would you agree?

11 ABED BALBAKY: Objection.
12 Form.

13 THE WITNESS: That's what
14 Figure 2 shows. It shows a
15 staircase -- a structure that
16 looks like a staircase to a POSITA
17 on both the left and the right
18 sides of the integrated circuit.

19 BY JOHANNES HSU:

20 Q And each -- strike that.

21 And would you agree that the
22 terminology staircase configuration

1 conveys the fact that the structure or
2 configuration has multiple steps of
3 different widths in a Y direction?

4 ABED BALBAKY: Objection,
5 relevance.

6 THE WITNESS: That's a fair
7 statement.

8 BY JOHANNES HSU:

9 Q Okay.

10 Now, let's turn to the operation
11 of 3D NAND Flash at the time of the 5 --
12 '957 patent.

13 What are the main operations
14 supported by a 3D NAND Flash?

15 ABED BALBAKY: Objection.
16 Form.

17 THE WITNESS: Generally
18 speaking, the principal operations
19 are erasing programming and
20 reading. There are others, but,
21 again, those are the principal
22 ones.

1 BY JOHANNES HSU:

2 Q How do read operations work?

3 A (Reviewing.)

4 Q Just to clarify, I'm asking this
5 question just for NAND Flash memory --

6 A Yeah.

7 Q -- that existed at the time of
8 the patent, not necessarily how the
9 patent itself disclose or not disclose
10 it. Is that fair?

11 A Okay. Because I don't think it
12 actually discloses NAND -- let's see, it
13 has read verify operations. In the most
14 abstract, a read operation in a 3D NAND
15 Flash memory device isolates one
16 particular memory cell per string by
17 putting all of the other transistors in
18 the string into a conductive state, and
19 then once you are in that state, you can
20 determine whether the threshold voltage
21 on a particular memory cell is lower or
22 higher than the applied word line for

1 that memory cell, and that's how you can
2 determine the information that is stored
3 in the charge-trapping layer of that
4 memory cell.

5 Q So just to clarify your
6 statement.

7 You said that "you can determine
8 whether the threshold voltage on a
9 particular memory cell is lower or higher
10 than the applied word line voltage for
11 that memory cell"; is that correct?

12 A Yeah. It would have been a
13 little bit more precise if I had used
14 gate voltage instead of word line
15 voltage. Because the -- it is the
16 voltage at the memory cell on the word
17 line layer that is determining whether
18 the selected memory cell is going to be
19 turned on or not.

20 Q How are the other transistors in
21 the industry put into a conductive state?

22 A By raising their word line --

1 I'm sorry, by raising their gate voltages
2 to the point where a channel is formed
3 between the source and the drain of the
4 corresponding transistors.

5 Q Is that voltage commonly known
6 as the pass voltage?

7 A Yeah. The '957 does refer to
8 pass voltages that can be applied to the
9 gates of select and memory cell
10 transistors in order to cause them to
11 become conductive.

12 Q Are you familiar with the term
13 "pass gate"?

14 A Yes.

15 Q What is that?

16 A A pass gate -- there's a couple
17 of different varieties of pass gates in
18 the art. It is generally a transistor or
19 collection of transistors that are
20 configured to be either allowing a signal
21 to pass from -- through it or not,
22 depending on the state of a control

1 gate -- control node would be better.

2 Q What is the -- strike that.

3 What is a pass gate in the
4 context of a 3D NAND Flash?

5 ABED BALBAKY: Objection to
6 form.

7 THE WITNESS: My description
8 of what a pass gate is, is across
9 all usages of the term. So that
10 definition, if you will, applies
11 the same for -- in the context of
12 a 3D NAND Flash device or anything
13 else, a processor, what have you.

14 BY JOHANNES HSU:

15 Q These other transistors that you
16 mentioned earlier that are have put into
17 a conductive state, can those be called
18 pass gates?

19 A I think you are referring to the
20 memory cells in a string. Is that -- can
21 you rephrase to include that?

22 Q Sure.

1 You mentioned earlier that other
2 memory cell transistors are put into a
3 conductive state in a read operation.

4 Can those memory cell
5 transistors be called pass gates?

6 A Not properly. The transistors
7 within a string have unique names that
8 are evocative of their function. So they
9 are select gates -- I'm sorry, select
10 transistors, memory cells or, not shown
11 here, dummy cells, or other types of
12 transistors within the strings.

13 If they -- any one of those is
14 put into a conductive state by applying
15 an appropriate voltage on its gate, then
16 it operates as a pass gate. But it's not
17 a pass gate. If you can understand the
18 distinction.

19 Q And that appropriate voltage
20 which enables the transistor to operate
21 as a pass gate is a gate voltage that is
22 higher than the threshold voltage of the

1 transistor; is that correct?

2 A In the simplest
3 conceptualization, yes, there are other
4 factors that can determine whether or not
5 a transistor is put into a conductive
6 state, in addition to or in cooperation
7 with the gate voltage.

8 Q Can you identify these other
9 factors?

10 A A body effect is an example or
11 source voltage relative to the gate, can
12 all impact what mode the transistor is
13 operating in, or VGS is another example,
14 it will determine the on resistance of
15 the transistor.

16 So, you know, the full model of
17 a MOS transistor is quite complicated.
18 We, wherever possible, can simplify it
19 conceptually and think principally of the
20 gate voltage as determining whether the
21 transistor is on or off because that
22 works most of the time.

1 Q What did you mean by "VGS"?

2 A It's the voltage between the
3 gate and the source.

4 Q By "between," do you mean the
5 gate voltage minus the source voltage?

6 A Yes. It's the difference
7 between the voltage of the gate and the
8 voltage of the source.

9 Q In fact, the threshold voltage
10 is properly defined relative to that
11 difference, correct?

12 ABED BALBAKY: Objection.
13 Form.

14 THE WITNESS: I believe
15 that's accurate, at least in part.
16 The full calculation of what the
17 threshold voltage is in practice
18 is complicated, and I don't have
19 it memorized.

20 BY JOHANNES HSU:

21 Q Now, can the voltage applied on
22 the word line coupled to a transistor

1 operating as a pass gate be called a pass
2 voltage?

3 A You know, we can call whatever
4 we want a pass voltage. What happens in
5 the '957 is that, for example, in Column
6 9, it talks about bias voltages (or pass
7 voltages) can be applied to gate
8 terminals (or gate), et cetera.

9 So the '957 uses the word pass
10 voltages to refer to bias voltages on
11 select transistors at a minimum, if not
12 memory cells as well.

13 Q How does -- excuse me.

14 How does the threshold voltage
15 of a memory cell transistor get changed
16 to a desired level?

17 A For what kind -- what kind of
18 memory device case?

19 Q Again, 3D NAND Flash.

20 A Charge-trapping 3D NAND Flash or
21 floating gate 3D NAND Flash?

22 Q Let's start with charge

1 trapping.

2 A By injecting electrons into the
3 charge-trapping layer through tunneling,
4 we are essentially putting charge on or
5 very close to the gate of the memory cell
6 and that changes its threshold voltage.

7 Q Is that done by applying some
8 sort of voltage to the memory cell?

9 A Yes, very specific voltages in
10 order to get the tunneling to occur.

11 Q And does that very specific
12 voltages apply at the gate of the memory
13 cell?

14 A At least in part, yes.

15 Q What is a typical level of that
16 specific voltage?

17 A Well, in -- (Reviewing) -- well,
18 it varies, obviously, a great deal from
19 device to device in the real world. In
20 the '957, I don't think it gives an
21 example of a program voltage. Some of
22 the other references that we have in this

1 matter do give example program voltages.
2 But they are -- it's safe to say that the
3 program voltages is going to be elevated
4 relative to the other voltages within the
5 memory string and other word line layers.

6 Q Is the program voltage also
7 elevated relative to the voltage that is
8 used to read the memory cell?

9 ABED BALBAKY: Objection,
10 relevance.

11 THE WITNESS: Again, I don't
12 think we have an example here
13 within the '957 of a program
14 voltage. So we can't say whether
15 their device operates at a
16 particular level for the program
17 voltage.

18 I think at least for some of
19 the other references here and --
20 the program voltage would be
21 higher than any of the read
22 voltages. I am not sure that's a

1 necessary requirement, though.

2 BY JOHANNES HSU:

3 Q Now, you used the term voltage
4 generator or voltage generation circuit,
5 right?

6 A Can you point me to a particular
7 paragraph.

8 Q Sure. This will be in your
9 declaration paragraph 79.

10 A (Reviewing.)

11 Q So paragraph 79 mentions voltage
12 generator and you can also look at
13 paragraph 94.

14 A Yeah, I will stick to one other
15 time is referring to the disclosure of Yu
16 and refers to voltage generator for 60 of
17 that disclosure.

18 Q Is it your understanding that
19 voltage generator in Yu is what you refer
20 to as a voltage generation circuits in
21 paragraph 94?

22 A (Reviewing.) Most likely, but

1 we would have to look at Yu to confirm
2 it, probably.

3 Q Okay.

4 In paragraph 94, the fourth line
5 on page 62, you said, "Word line drivers,
6 or analogous voltage generation circuits,
7 operate as voltage sources..." I will
8 stop there.

9 Did I read that part correctly?

10 A Yes, you did.

11 THE WITNESS: We have been
12 going another hour and 10,
13 actually. Are we close to a break
14 point?

15 JOHANNES HSU: That's -- we
16 can do that for sure, but that's
17 -- for now answer the question --
18 oh, sorry, let's finish this part
19 of the questioning.

20 BY JOHANNES HSU:

21 Q Is there a difference between
22 word line drivers and voltage generation

1 circuits?

2 A Generally, yes.

3 Q What are the differences?

4 A Word line driver is a generic
5 term for the circuitry that directly
6 connects to word lines in all types of
7 semiconductor memory devices.
8 Voltage-generating circuits are found in
9 all manner of integrated circuits, except
10 for the simplest ones, and they generate
11 a specific voltage according to their
12 control inputs. So they can either
13 generate one specific voltage reliably or
14 controllably to generate a plurality of
15 different voltages.

16 Q And is your answer the same for
17 3D NAND Flash devices?

18 A Yes. My answer was not specific
19 to 3D NAND Flash, but encompasses all
20 varieties of memory integrated circuits.

21 Q So in what ways are they
22 analogous, as you phrased it in paragraph

1 94?

2 A They are analogous in that
3 sometimes word line drivers are drawn to
4 include voltage generated circuits and
5 sometimes they are drawn separately.

6 So I use the word "analogous"
7 there to indicate the relationship at
8 times between word line drivers and
9 voltage generating circuits. The word
10 line drivers being responsible for taking
11 the generated voltages and driving them
12 onto the corresponding word lines.

13 Q Where are these components
14 located in a 3D NAND Flash device?

15 A That varies significantly from
16 vendor to vendor, from generation to
17 generation. Typically, they are at the
18 bottom of the stack, but not exclusively
19 so.

20 Q And by "stack," you are
21 referring to, for example, what is
22 illustrated in Figure 2 of the '957

1 patent?

2 A Yes.

3 JOHANNES HSU: Okay. I think
4 we can break there.

5 THE REPORTER: Off the
6 record.

7 (Whereupon a Recess Commenced
8 at 1:36 p.m. and Testimony
9 Recommenced at 2:09 p.m. EDT.)

10 BY JOHANNES HSU:

11 Q All right. Doctor, welcome
12 back.

13 A Thank you.

14 Q Recall earlier we had discussion
15 about pass gates?

16 A Yes.

17 Q And you testified that the
18 memory cells -- strike that.

19 You testified that memory cell
20 transistors, other than the one that is
21 to be read in a read operation, can be
22 put into a conductive state by applying

1 an appropriate voltage on its gate, then
2 the transistor would operate as a pass
3 gate; is that correct?

4 A It's a reasonable paraphrasing
5 of my testimony.

6 Q Okay.

7 If I may direct your attention
8 to the '957 patent Column 9, lines 34
9 through 41.

10 A 9; 34 to 41. Okay.

11 Q Is it fair -- strike that.

12 This particular passage talks
13 about pass voltages, right?

14 A (Reviewing.) Yes.

15 Q And it appears to treat the pass
16 voltage synonymously with bias voltages,
17 right?

18 A (Reviewing.) I don't interpret
19 the parenthetical on Column 9, line 35
20 where "or pass voltages" is
21 parenthetically modifying bias voltages
22 to indicate that those two terms are

1 synonymous.

2 There are certainly other
3 circumstances, perhaps not in this
4 patent, but elsewhere, where not all bias
5 voltages just, i.e., a voltage on a node
6 to create a particular bias condition are
7 necessarily pass voltages.

8 Q Here, I would like you to focus
9 just on the '957, independent of what
10 other literature might use the term.

11 So in that sentence, it has the
12 same structure, "gate terminals (or
13 gates)."

14 And you earlier testified that
15 gate terminals and then gates are
16 synonymous, correct?

17 ABED BALBAKY: Objection to
18 form.

19 THE WITNESS: For the
20 particular context that you asked
21 me about previously, yes. But
22 that does not necessarily speak to

1 the "or pass voltages"

2 parenthetically.

3 And you know, we have to look
4 at the entirety of the disclosure
5 of the '957 through the eyes of a
6 POSITA to understand whether bias
7 voltages and pass voltages are
8 being treated synonymously in the
9 '957. I have not done that. I
10 cannot say.

11 BY JOHANNES HSU:

12 Q So going back to your earlier
13 testimony, you said that the memory cells
14 can be put into a conductive state by
15 applying an appropriate voltage and then
16 the transistor will offer it as a pass
17 gate.

18 And I think you said that's a
19 fair characterization of what you
20 testified earlier; is that right?

21 A Yeah, I believe so. But again,
22 we would have to review my exact

1 testimony to be sure.

2 Q Do you understand there's
3 sufficient bias voltages such as 6.8 volt
4 on lines 38 and 39, to be an example of
5 the appropriate voltage that you referred
6 to earlier to enable a transistor to
7 operate as a pass gate?

8 ABED BALBAKY: Objection to
9 form.

10 THE WITNESS: Yes. So in the
11 6.8 volts in Column 9 at line 39,
12 is reasonably interpreted as an
13 example and not a sole value that
14 would work in all circumstances.

15 BY JOHANNES HSU:

16 Q So based on this disclosure
17 that's described in Column 9, lines 34
18 through 41, is it correct to say that the
19 TSG transistor is operating as a pass
20 gate?

21 A When in Column 9, the '957 says,
22 "The bias voltages can be sufficient,

1 such as 6.8 volts, to turn on the TSG
2 transistor," to a POSITA, that would
3 indicate that the TSG transistor is on
4 and is operating as a single-ended pass
5 gate in that mode.

6 Q Is that also true of the BSG
7 transistor?

8 A (Reviewing.) Yes.

9 Q Is that also true of the
10 unselected memory cells?

11 A (Reviewing.) So with regard to
12 the unselected memory cells, there are
13 embodiments where it looks like the
14 appropriate voltage to turn on the
15 unselected memory cells might be more
16 than 6.8 volts.

17 But in general, the idea is
18 comparable that at a certain applied
19 voltage, the unselected memory cells will
20 be put into a conductive state, as they
21 would be in a -- they were operating as a
22 pass gate, single-ended pass gate.

1 Q Right before the break, you
2 testified that the voltage-generating
3 circuits typically are at the bottom of
4 the stack.

5 Remember that testimony?

6 A They can be. I don't know if
7 typical is necessarily the case, but
8 there is a -- that is one place where
9 they can go. They can go on the top or
10 they can go on the sides. There have
11 been implementations of all of those that
12 -- in the past.

13 Q And these are the circuits from
14 which the voltage that eventually becomes
15 the gate voltage originate, correct?

16 A There are a lot of peripheral
17 circuits for a typical 3D NAND Flash.
18 That is one of the functions of the
19 peripheral circuits, to generate voltages
20 of all different flavors for use in the
21 different operations at the different
22 stages of the different operations.

1 So -- I'm sorry, I lost my train
2 of thought. Did that answer the
3 question?

4 Q Yes. Let's unpack that answer a
5 bit.

6 So is the voltage-generating
7 circuit part of the peripheral circuits
8 of a 3D NAND Flash?

9 A Generally speaking, yes.
10 Whether a particular engineer would
11 consider one circuitry to be part of the
12 peripheral circuitry or another, is
13 personal and based on design styles
14 within a particular company.

15 But in general, the peripheral
16 circuits are viewed as everything outside
17 of the memory arrays, per se.

18 Q And you mention that the
19 voltage-generating circuit is used to
20 generate voltages of all different
21 flavors for use in the different
22 operations, correct?

1 A That's paraphrasing what I said,
2 but basically, yes.

3 Q So for example, the
4 voltage-generating circuits generates the
5 pass voltage in a read operation,
6 correct?

7 A In a read operation, you have a
8 variety of different voltages that are
9 going to be needed, not just for the
10 select transistors and the unselected
11 memory cells, but also the selected
12 memory cell is going to have to have a
13 variety of different voltages applied to
14 it.

15 Voltage generators, plural, will
16 be responsible for creating all of those
17 as required.

18 Q And would the answer be the same
19 for a program operation, except that the
20 voltage levels will be different?

21 A In general, yes, the voltage
22 generators and the peripheral circuitry,

1 generally, is responsible for creating
2 all of the voltages that are needed for
3 all of the operations, including a
4 program operation.

5 Q How does the voltages go from
6 the voltage generators to the gates of
7 memory cells?

8 A On wires and through other
9 circuitry.

10 Q What other circuitries do these
11 voltages go through?

12 A Again, it's subject to the
13 design styles and the particulars of a
14 specific device. But in general, the
15 word line drivers accept voltages from
16 the voltage generators and forward them
17 to the appropriate word line layers, in
18 order to affect the operation being
19 performed.

20 Q Do the voltages go through word
21 line decoders?

22 A Whether the word line decoders

1 are distinct or integral to the word line
2 drivers is highly variable and, you know,
3 what's called driver, what's called the
4 decoder is subject to personal whim.

5 Sometimes there's a pre-decoder
6 and a post-decoder and the post-decoder
7 is part of the word lines. It's all
8 highly subjective and I don't think the
9 597 [sic] speaks to a particular
10 terminology that we can rely on.

11 Again, if I am wrong on that,
12 please point me to a passage in the '957.

13 Q I will point you to Column 7,
14 the paragraph starting on line 48 --
15 actually, it's going to run through
16 Column 8 -- strike that.

17 So if I may direct your
18 attention to Column 7, around line --
19 starting from line 57. There, it refers
20 to "decoder structures, driver
21 structures, charge structures, and other
22 structures."

1 Do you see that?

2 A I do.

3 Q Does that disclosure change your
4 previous answer?

5 A No, I don't think so. This
6 disclosure is just saying that the
7 authors of the '957 consider all of those
8 different things, regardless of how they
9 are grouped or implemented; that all of
10 them are part of the peripheral circuits,
11 or as they call them, periphery circuits.

12 Q Is it correct that whether the
13 decoders and the word line drivers are
14 considered to be one component or
15 separate components, the voltages from
16 the voltage-generating circuit would go
17 through whatever they are called, decoder
18 and/or driver, to reach the memory cell
19 gates?

20 A Yeah, that's a fair statement.
21 But, you know, for example, Figure 11 of
22 the '957 doesn't enumerate these

1 individual peripheral circuits except in
2 the coarsest terms.

3 So the -- I think that is fair
4 to say that in the '957, all of those
5 structures are related to getting the
6 appropriate voltages to the gates of the
7 memory cells and the gates of the select
8 transistors and onto the word line --
9 onto the bit lines, as appropriate.

10 Exactly how an engineer has
11 divided them up and named them, is
12 irrelevant.

13 Q Figure 11 does show a column
14 decode 1010 in row presumably that also
15 mean decode -- just spelled as DEC --
16 1008, correct?

17 A Yes, those blocks are part of
18 Figure 11.

19 Q Do you understand those to be
20 the decoders that we have been -- strike
21 that.

22 Do you understand those to be

1 instances of the decoders that we have
2 been discussing?

3 A Generally speaking, yes. But
4 again, Figure 11 is at a sufficiently
5 high level that there is a lot of
6 circuitry that's not shown here and there
7 are sub-blocks within each of these
8 blocks that would have names and
9 functionality as well.

10 So the answer is yes, with
11 caveats.

12 Q And is it correct that Figure 11
13 is a block diagram and doesn't denote any
14 physical structure of the memory device?

15 A Yes, it's a logical block
16 diagram.

17 Q As the voltage is going through
18 these, as you put it, blocks and
19 sub-blocks to reach the gate terminal, is
20 there a delay associated with that?

21 A Inevitably, yes. Nothing is
22 instantaneous in circuits.

1 Q Earlier, we talked about the
2 fact that the voltage generator generates
3 a lot of different voltages for different
4 operations.

5 Do you recall that?

6 A Yes.

7 Q And is it fair to say that the
8 voltages that are -- that are outputs by
9 a voltage-generating circuit, that is
10 routed to a particular memory cell, would
11 basically travel through the same routes,
12 whether it's for a read operation or
13 another operation like a program
14 operation?

15 ABED BALBAKY: Objection.

16 THE WITNESS: Not
17 necessarily. We don't know
18 anything, as you said, about the
19 details of how these blocks are
20 being conceptualized by the
21 authors of the '957.

22 The voltage generator or

1 generators, plural, are not shown
2 in Figure 11. How those generated
3 voltages are routed to the gates
4 of specific memory cells is not
5 discussed, that I am aware of, in
6 the specification of the '957.

7 BY JOHANNES HSU:

8 Q But would a POSITA understand
9 that in any event, the voltage will have
10 to travel through certain blocks or
11 sub-blocks?

12 A That's an extremely generous --
13 general statement that is true.

14 Q You testified earlier that
15 delays would be associated with that
16 traveling through the blocks and
17 sub-blocks, correct?

18 A Delays of one form or another,
19 yes.

20 Q And in the course of these
21 operations, is it correct that sometimes
22 the voltages would be increasing, while

1 at other times, the voltages will be
2 decreasing?

3 ABED BALBAKY: Objection.

4 THE WITNESS: What voltages
5 are you referring to here? That's
6 too vague.

7 BY JOHANNES HSU:

8 Q I was referring to the voltages
9 output by the voltage-generating circuit
10 to be applied to the gates of a memory
11 block.

12 A So you are saying -- you are
13 asking about the outputs of the voltage
14 generator or where?

15 Q So let me rephrase the question.
16 The gate voltages are generated
17 by the voltage-generating circuits,
18 right?

19 A At their source, yes.

20 Q And sometimes these gate
21 voltages, during the course of a memory
22 device operation, will be increasing,

1 correct?

2 A Well, that's certainly shown in
3 the figures of the '957, that the
4 voltages shown increase and decrease at
5 different points of time. So that's hard
6 to dispute.

7 Q And correspondingly, what is
8 generated at the voltage source generate
9 -- strike that.

10 Correspondingly, what -- the
11 voltages that's output by the
12 voltage-generating circuits, are
13 also increasing or decreasing,
14 correct?

15 ABED BALBAKY: Objection.
16 Form.

17 THE WITNESS: No, we don't
18 know that. We don't know anything
19 about how the voltage that --
20 voltages that are disclosed within
21 the '957 are generated or selected
22 and routed to their destinations.

1 BY JOHANNES HSU:

2 Q But did you not testify earlier
3 that the voltages are generated by a
4 voltage generation circuit?

5 A Each voltage will be generated
6 by a voltage generator circuit. A
7 voltage generation circuit may be fixed
8 or it can be programmable. And there is
9 no discussion in the '957 about whether
10 the inventors had any particular concept
11 of that in mind as they prepared their
12 patent.

13 Q I wasn't thinking about that
14 level of detail.

15 But you agree that the gate
16 voltages are generated by these
17 voltage-generating circuits, right?

18 ABED BALBAKY: Objection.
19 Form.

20 THE WITNESS: So the specific
21 voltages that ultimately end up on
22 the gates of memory cells and

1 select transistors, derive lineage
2 back to voltage generators of some
3 form or another, yes.

4 But everything that's in
5 between is not discussed or
6 restricted in any way that I am
7 aware of in the '957.

8 BY JOHANNES HSU:

9 Q So I am discussing NAND Flash
10 devices generally, not specifically what
11 is disclosed or not disclosed by the '957
12 patent. Okay?

13 A Okay.

14 Q So given a gate voltage that is
15 increasing, for example, would a POSITA
16 understand that that increasing gate
17 voltage has a corresponding increasing
18 gate voltage at the output of
19 voltage-generating circuits, or if you
20 prefer, the word line drivers?

21 A No to the former and yes to the
22 latter.

1 Q What is the distinction?

2 A We don't know anything about the
3 structure of the voltage-generating
4 circuits and since you broadened it to be
5 all forms of 3D NAND devices, there are a
6 myriad of design alternatives for the
7 voltage generators, plural.

8 It's the physical structure of
9 the NAND -- 3D NAND, typically means
10 there's a singular word line driver per
11 word line layer, although that's not
12 necessarily true either. The way that
13 Figure 3 is drawn, you could have a
14 plurality of parallel word line drivers
15 driving the same word line layer.

16 So even in that circumstance,
17 you would presumably have a word line
18 driver voltage that's changing, although
19 you could affect that by turning off
20 one word line driver and turning on a
21 different one.

22 So, again, your question is too

1 broad, too general vis-à-vis its scope,
2 to have a definitive answer.

3 Q Is it fair to characterize your
4 answer to indicate that the voltage
5 generation and driving has many different
6 options and is a complicated undertaking?

7 A In the commercial world, yes,
8 absolutely. There are many options at
9 every point of the design process, and 3D
10 NAND Flash devices are extremely
11 complicated, very delicate devices that
12 require a tremendous amount of
13 sophistication in the design and
14 manufacturing to ensure their
15 functionality and reliability.

16 Q Now I would like to turn your
17 attention to Column 16, lines 47 through
18 51.

19 A 47 you say?

20 Q 47.

21 A Starting "For example..."

22 Through 51?

1 Q Hm-hm. Yes.

2 A Okay. I have read that.

3 Q The '957 patent here discloses
4 that voltages apply to selected memory
5 cells are applied through the row
6 decoders and column decoders, correct?

7 A Yeah, that is what it says
8 there.

9 Q I would like to turn now to your
10 opinion of the embodiments of the '957
11 patent.

12 So let's go to Figure 4.

13 A Of the 954?

14 Q Of the '957 patent.

15 A I'm sorry, '957. Forgive me.

16 Figure 4. I am looking at
17 Figure 4.

18 Q Is Figure 4 an embodiment of any
19 of the claims of the '957 patent?

20 A (Reviewing.) That's not a
21 question I have been asked to analyze and
22 I have not gone through each of the

1 figures in each of the claims to see what
2 reads on which embodiment for all of the
3 different embodiments of the '957.

4 Q Fair to say today you don't know
5 whether Figure 4 is an embodiment of any
6 claims of the '957 patent, correct?

7 A As I just said --

8 ABED BALBAKY: Objection.

9 Form.

10 THE WITNESS: -- I have not
11 been asked to review the figures
12 and cross-reference them with each
13 of the claims. I have not done
14 that work. I don't know the
15 answer to it.

16 BY JOHANNES HSU:

17 Q Is that answer the same for
18 Figure 5?

19 A In general, yes. I have not
20 gone and been asked to look at each of
21 the figures and embodiments and see which
22 claims read on which embodiments.

1 Q Is that answer the same for
2 Figure 6?

3 A Let's see, I think Figure 6 is
4 special.

5 (Reviewing.) Let me look at my
6 declaration for a second. On page 21 of
7 my declaration, I have a copy of Figure 6
8 that is annotated with bias voltages and
9 verify voltages, which correspond to some
10 of the elements of Claim 1.

11 So at least to the extent of
12 those elements, they are represented in
13 Figure -- in the embodiment of Figure 6.

14 Q Is Figure 7 an embodiment of any
15 of the claims of the '957 patent?

16 A For that one, I --
17 (Reviewing) -- reading from my paragraph
18 53 on page 33 of my declaration, I say
19 that, As shown in the annotated version
20 of Figure 7 below, much like the other
21 figures of the '957 patent, Figure 7
22 illustrates a bottom bias voltage with a

1 fixed voltage level administered to the
2 BG -- BSG layer in both pre-pulse and the
3 subsequent verify/read stage, and
4 similarly illustrates top bias voltage
5 with a fixed voltage level being
6 administered to the TSG layer in both the
7 pre-pulse stage and subsequent
8 verify/read stage.

9 This uses claim language from
10 Claims 5 and 6. So for at least those
11 elements, there is a correspondence. But
12 beyond that, I have not analyzed this
13 figure and this embodiment vis-à-vis the
14 other elements of those claims or the
15 other claims.

16 Q So is it your opinion that
17 Figure 7 embodies Claims 5 and 6 of the
18 '957 patent?

19 ABED BALBAKY: Objection.

20 Mischaracterizes his testimony.

21 THE WITNESS: Yeah, that's
22 not what I said.

1 I said with regard to those
2 specific elements of 5 and 6,
3 those are represented and found
4 within Figure 7. Those claims are
5 dependent on other claims and they
6 have other elements that I have
7 not offered an opinion on.

8 BY JOHANNES HSU:

9 Q Okay. So let's actually circle
10 back to claim -- sorry, Figure 6, then.

11 You were pointing to, I think,
12 page 21 of your declaration?

13 A Page 22.

14 Q Page 22, the figure there,
15 right. The annotated figure on page 22?

16 A And the text that follows it.

17 Q So is it your opinion that
18 Figure 6 is an embodiment of Claim 1 of
19 the '957 patent?

20 A As I said a moment ago, I have
21 shown that the bias voltages and the
22 verify voltages that are claimed within

1 Figure 6, are -- I'm sorry, that are
2 claimed in Figure -- in Claim 1, are
3 present in Figure 6.

4 That is the extent to which this
5 present discussion on pages 21 and 22 of
6 my declaration relates to Figure 6.

7 Q Is Figure 8 an embodiment of any
8 of the claims of the '957 patent?

9 A Again, I've not been asked to
10 analyze Figure 8 or many of the other
11 figures and their embodiments vis-à-vis
12 which elements of which claims are found
13 within those embodiments. So I do not
14 know. I have not been asked to do that
15 and I have not.

16 Q Is your answer the same for
17 Figure 9?

18 A Yes.

19 Q Is Figure 10 an embodiment of
20 any of the claims of the '957 patent?

21 A Same answer; I have not been
22 asked to analyze Figure 10 specifically

1 to see whether it alone, with its
2 associated discussion in the
3 specification, performs all of the steps
4 of any particular claim -- let me
5 rephrase that. I will start again.

6 I have not been asked to analyze
7 Figure 10 to see whether it embodies all
8 of the elements of any particular claim
9 of the '957.

10 Q Based on your testimony, then,
11 to summarize, sitting here today, you
12 have no opinion whether any of Figures 4
13 through 10 embodies any of the claims of
14 the '957 patent; is that correct?

15 A Well to be clear, my role here
16 has been to critique the arguments in the
17 petition in Dr. Liu's declaration. It is
18 not required of me to analyze the
19 embodiments of the '957, relative to the
20 claims of the '957, to see whether they
21 are enabled or not in order to perform my
22 designated function of critiquing of the

1 petition.

2 I was not asked to do that. I
3 did not do that. I have no opinion
4 sitting here today about those questions.

5 Q You have no opinion sitting here
6 today about whether any of Figures 4
7 through 10 embodies any of the claims of
8 the '957 patent, correct?

9 ABED BALBAKY: Objection.

10 Asked and answered.

11 THE WITNESS: I will just
12 refer you to my previous answer.
13 I was not asked to do that. It
14 was not required of me to complete
15 my task of critiquing the
16 arguments of the petition and
17 Liu's declaration. And so I did
18 not do what I was not asked to do.
19 So I have no opinion, sitting here
20 today.

21 BY JOHANNES HSU:

22 Q Figure 4 illustrates a long

1 pre-pulse time, correct?

2 A (Reviewing.) Let me see where
3 it says that.

4 (Reviewing.) So that's towards
5 the bottom of Column 11 of '957, where it
6 says that it should be noted that in
7 Figure 4, a long pre-pulse time in a
8 range from 1 nanoseconds to
9 10 microseconds is applied in the
10 pre-pulse stage.

11 So yes, it refers to that as a
12 long pre-pulse time.

13 THE WITNESS: Could we take a
14 break, please?

15 I'm sorry, I got that in
16 before you asked the question.

17 JOHANNES HSU: Of course.

18 THE WITNESS: Five-minute
19 break, please.

20 JOHANNES HSU: Of course.

21 THE REPORTER: Off the
22 record.

1 (Whereupon a Recess Commenced
2 at 2:59 p.m. and Testimony
3 Recommended at 3:06 p.m. EDT.)

4 BY JOHANNES HSU:

5 Q Doctor, welcome back.

6 A Thank you.

7 Q Does Figure 5 illustrate a short
8 pre-pulse time?

9 A Yes, that's described in Column
10 12 of the '957, beginning at line 10, and
11 it goes on to say that, "The
12 verify/reading operation can have a
13 pre-pulse stage with a short pre-pulse
14 time. The short pre-pulse time may be
15 insufficient for the bias voltages
16 applied to the word lines ($>N+1$), $WLn+1$,
17 WLn , $WLn-1$, and $WLs (<n-1)$ to be fully
18 developed in the pre-pulse stage."

19 Q Does Figure 6 illustrate a long
20 pre-pulse time?

21 A Yes, and that's disclosed again
22 in Column 12, starting at line 31. "As

1 shown in Figure 6, the memory cells can
2 be programmed in the forward order, and
3 the verify/read operation can include a
4 long pre-pulse time in the pre-pulse
5 stage."

6 Q Does Figure 7 illustrate a short
7 pre-pulse time?

8 A (Reviewing.) Do you have a
9 particular line number you can point me
10 to? I am having trouble --

11 Q Sure.

12 Column 13, starting from --
13 (Simultaneous Crosstalk.)

14 A There it is. I missed it the
15 first -- yes.

16 So in column -- line 13,
17 starting at Column 8 it discloses that
18 Figure 7 includes a short pre-pulse time.

19 Q And does Figure 8 illustrate a
20 long pre-pulse time, like Figure 6?

21 And I will point you to Column
22 12, lines 38 through 42.

1 A (Reviewing.) Did you say Column
2 12 or 14?

3 Q 12.

4 A 12. Line 38.

5 38 is -- 39 is the start of the
6 paragraph.

7 Okay. Yes. So Figure 6 is a
8 long pre-pulse and then you were asking
9 me to compare that to Figure 8; is that
10 right?

11 Q No. I was asking whether you
12 agree that both Figure 6 and Figure 8
13 illustrate a long pre-pulse time?

14 A Okay. So we have identified
15 that Figure 6 is disclosed as long
16 pre-pulse. So now we need to confirm
17 Figure 8; is that correct?

18 Q Sure.

19 A And do you have a line number
20 for me there?

21 Q That was the Column 12 starting
22 from line 38.

1 A That's not about Figure 8.

2 ABED BALBAKY: Counsel, I
3 believe your citation was intended
4 to be at Column 14. You may have
5 it written down incorrectly.

6 THE WITNESS: Yes. In Column
7 14, it does disclose column --
8 Figure 8 as showing a long
9 pre-pulse time, as counsel has
10 indicated.

11 JOHANNES HSU: Thank you,
12 counsel. It is indeed Column 14.

13 BY JOHANNES HSU:

14 Q Now, moving on to Figure 9.

15 As far as I can tell, the '957
16 patent doesn't directly say that it is a
17 short -- it involves a short pre-pulse
18 time, but it compares it with Figure 7 on
19 the bottom of Column 14.

20 So do you agree that Figure 9
21 illustrates a short pre-pulse time like
22 Figure 7?

1 A Well, it certainly seems that
2 way, but in the absence of a concrete
3 disclosure to that effect, we will have
4 to leave it with some uncertainty.

5 Q My next few questions is in the
6 context of your testimony that you have
7 not been asked to analyze whether any of
8 these Figures 4 through 10 embodies any
9 of the claims of the '957 patent.

10 Are you with me?

11 A Yes.

12 Q Okay.

13 So let's go to your declaration.
14 Let's start with paragraph 36.

15 Actually could have gone
16 straight here earlier to save us a little
17 time. My apologies.

18 A I am looking at 36, yes.

19 Q Okay.

20 The citation at the end of that
21 paragraph, that refers to Figures 4, 6,
22 and 8 and then Figures 5, 7, and 9.

1 Do you see that?

2 A Yes, I see that.

3 Q Okay.

4 So first of all, here in the
5 parenthetical you said "4, 6, 8
6 (describing embodiments with a lengthy
7 pre-pulse duration)." Correct?

8 A Yes.

9 Q So that's consistent with what
10 we have had just discussed; that they --
11 Figures 4, 6, and 8 illustrate a long
12 pre-pulse time, correct?

13 A Yes, that's duplicitous of what
14 we just went through.

15 Q And then at the end, when it
16 explains Figures 5, 7, and 9, it says
17 "describing embodiments with a brief
18 pre-pulse duration." Correct?

19 A Yes, that's what I wrote there.

20 Q So does that refresh your memory
21 that Figure 9, like Figures 5 and 7,
22 illustrate a short pre-pulse time?

1 A Yes. So this is based on the
2 comparison of Figures 7 and 9 and not the
3 specific recitation that exists for all
4 of the other ones except 9, about this --
5 the duration of the pre-pulse period.
6 But in this case, I did indicate that
7 Figure 9 does disclose a brief pre-pulse
8 duration.

9 Q So with apologies to that
10 detour, now I am going to get back the
11 questions I had intended to ask in the
12 context of your testimony that you were
13 not asked to analyze whether any of these
14 Figures 4 through 10 embodies any other
15 claims of the '957 patent. Okay?

16 A Okay.

17 Q All right. So as we just
18 discussed in these two parentheticals,
19 you used the words describing embodiments
20 with a lengthy or a brief pre-pulse
21 duration, correct?

22 A Yes, that's how I describe it

1 there.

2 Q So by "embodiments," you don't
3 mean that they are embodiments of any of
4 the claims, correct?

5 A No. I think the way that the
6 '957 describes its figures as exemplary
7 embodiments. That is the same way that I
8 have used it in that paragraph in my
9 declaration; that they are embodiments,
10 they are not necessarily claimed
11 embodiments.

12 Q So to make sure we are on the
13 same page, here you are saying these six
14 figures, 4 through 9, are exemplary
15 embodiments but not necessarily claim
16 embodiments, correct?

17 A As I testified previously, I
18 have not been asked to verify whether any
19 of these embodiments disclose all of the
20 elements of any particular claim.

21 So that is -- in that paragraph
22 in my declaration, I am referring to

1 embodiments and not claimed embodiments.

2 Q Okay.

3 Let's turn to paragraph 50, top
4 of page 32.

5 A Just the tail end of 50?

6 Q Correct.

7 A Okay.

8 Q Starting from the top of page
9 32, the sentence states, "Each of the
10 other embodiments of the '957 patent,
11 such as those illustrated in Figures 5
12 through 9..." and then goes on.

13 Did I read that correctly?

14 A Yes, you did.

15 Q Is your answer the same here
16 that the embodiments in this sentence
17 does not necessarily mean claimed
18 embodiments?

19 A The language speaks for itself.
20 It is the embodiments and the word
21 "claim" does not exist in that sentence.

22 Q That's just -- let's try to

1 shortcut this a little bit.

2 Is that your answer to all
3 occurrences of embodiments in your
4 declaration?

5 And I can represent to you, you
6 don't use the term "claimed embodiments."
7 And if you want to click through them,
8 you're welcome to do so.

9 A Yeah, I would have to do that in
10 order to be able to answer your question
11 truthfully.

12 Q Okay.

13 Then let's go through them one
14 at a time.

15 Paragraph 53. First sentence.

16 A 53. (Reviewing.)

17 Yes.

18 Q So not necessarily claimed
19 embodiments?

20 A I do not represent in that
21 sentence that the embodiment of Figure 7
22 is a claimed embodiment.

1 Q Okay. Paragraph -- paragraph
2 110, on page 73, fourth line from the
3 bottom.

4 The phrase "the embodiments in
5 the '957 patent specification."

6 A Let me read the whole paragraph,
7 please.

8 Q Sure.

9 A (Reviewing.) Yes. In this
10 paragraph, I say that the description of
11 -- that's previous to that in paragraph
12 110, is consistent with the plain and
13 ordinary meaning of the claim language.

14 I do not go as far as to say
15 that the embodiment of -- that's being
16 referred to here, is, in fact -- wait,
17 110. (Reviewing.)

18 Figure 4, for example -- yes, is
19 a claimed embodiment. Just that it is
20 consistent with the plain and ordinary
21 meaning of that portion of Claims 5 and
22 6.

1 Q Paragraph 113, page -- on page
2 76.

3 Here, the fifth line from the
4 bottom also refers to embodiments
5 included in the '957 patent, including
6 the embodiments of Figure 7.

7 Can you comment on what you
8 meant by embodiments or embodiment,
9 plural or singular here.

10 A Again, I am using the term
11 "embodiment" as it's used in the '957
12 vis-à-vis exemplary embodiments, not
13 necessarily commenting on whether or not
14 they are claimed.

15 Q Last one, paragraph 137 on page
16 90.

17 At the end of the paragraph the
18 clause all of the embodiments -- or the
19 phrase, "all of the embodiments in the
20 '957 patent specification."

21 A (Reviewing.) Same answer.

22 This is, again, with regard, I

1 cite to Figure 4 of the '957 in the
2 citations after that sentence. That
3 sentence does not explicitly say that the
4 embodiments of the '957 patent are
5 individually claimed or not.

6 I do say in that sentence that
7 the interpretation of the claim language
8 is consistent with the plain and ordinary
9 meaning of that and the embodiments of
10 the specification.

11 Q So to summarize, in all of these
12 paragraphs that we looked at, the
13 occurrences of the word embodiment, in
14 the singular or plural, does not
15 necessarily mean a claimed embodiment; is
16 that correct?

17 ABED BALBAKY: Objection to
18 form.

19 THE WITNESS: Let me make
20 sure we haven't skipped over any.

21 (Reviewing.)

22 Did we do 102? Paragraph

1 102? There's a word embodiment in
2 there. Do you care?

3 BY JOHANNES HSU:

4 Q Well, that was referring to
5 embodiments in the Hongtao reference. So
6 I skipped it.

7 A Good point. Thank you.

8 Q Same with paragraph number 103.

9 A Yes, I see that now. I
10 apologize.

11 Okay. Would you repeat the
12 question, please?

13 Q So to summarize, in all of these
14 paragraphs that we looked at, the
15 occurrences of the word embodiment in the
16 singular or plural form, does not
17 necessarily mean a claimed embodiment; is
18 that correct?

19 A Yes. In all of these paragraphs
20 that we went through together, the word
21 embodiment is not prefixed by claimed and
22 it means embodiment, not claimed

1 embodiment.

2 Q You mentioned earlier that you
3 are using -- strike that.

4 You mentioned earlier that the
5 '957 patent uses the phrase "exemplary
6 embodiments," correct?

7 A Yes, it does so repeatedly.

8 Q Okay.

9 So let's turn back to the
10 patent, and I would like to direct your
11 attention to Column 12, lines -- starting
12 from line 28.

13 A I am there.

14 Q There, it identifies Figure 6 as
15 a schematic diagram "in accordance with
16 exemplary embodiments of the disclosure,"
17 correct?

18 A Yes, that's fairly common patent
19 parlance.

20 Q And is that one instance of what
21 you refer to as repeated usages of the
22 phrase "exemplary embodiments" in the

1 '957 patent?

2 A (Reviewing.) Yeah, I think
3 there's over 20 different instances of
4 the phrase "exemplary embodiment,"
5 referring to most, if not all, of the
6 figures in the range that you have been
7 focusing on.

8 Q Let's turn to Column 13, lines 5
9 through 8.

10 Here, it states, "Figure 7 is a
11 second schematic diagram" -- and I will
12 skip the middle -- "in accordance with
13 exemplary embodiments of the disclosure."
14 Correct?

15 A That's what it says.

16 Q Okay.

17 And I will direct your attention
18 to Column 14, starting from line 31.

19 A Okay.

20 Q Here, it states, "Figure 8 is a
21 first schematic diagram" -- and then
22 again, I will skip the irrelevant

1 part for the purpose of discussion, and
2 it goes on to say -- "in accordance with
3 the exemplary embodiments of the
4 disclosure." Correct?

5 A Those are the words there, yes.

6 Q And I will direct further your
7 attention to Column 14, starting from
8 line 63.

9 A I am there.

10 Q There it characterizes Figure 9
11 using the same language, right?

12 In accordance with the -- with
13 exemplary embodiments at the disclosure.

14 A Yes, those are the words it
15 uses.

16 Q Can you find -- and it seems
17 like you are able to search in the
18 specification, is that correct, when you
19 identify more than 20 or about 20
20 occurrences of the phrase "exemplary
21 embodiments"?

22 A Yes, I can search the PDF.

1 Q Okay. Super.

2 Can you identify for me any
3 disclosure that Figure 4 is in accordance
4 with exemplary embodiments of the
5 disclosure?

6 A (Reviewing.) The very bottom of
7 Column 9 refers to, "In an exemplary
8 embodiment of Figure 4..."

9 Does that satisfy your
10 conditions?

11 Q What line are you on -- oh, the
12 very bottom?

13 A Yeah, 67.

14 Q Which states, "In an exemplary
15 embodiment of Figure 4..." Correct?

16 A Yes. Indicating that Figure 4
17 is an exemplary embodiment.

18 Q But it doesn't say in accordance
19 with exemplary embodiments of the present
20 disclosure, does it?

21 A That seems to be a difference
22 without a distinction, as far as what is

1 common practice in the writing of
2 specifications there. I do not see a
3 significant difference between those two
4 sets of words.

5 Q Do you recall how you had
6 mentioned that you used Figure 6 of the
7 patent to illustrate the voltages
8 required by Claim 1?

9 A Yes. I pointed to a page, I
10 think it was 22 of my declaration. We
11 can go back to that.

12 Q That's right.

13 A Yes. Page 22, Figure 6
14 annotated.

15 Q And Doctor, you recall Claim 1
16 has a requirement that wherein the second
17 bias voltage is smaller than the first
18 bias voltage, correct?

19 A That is the last element of
20 Claim 1, "wherein the second bias voltage
21 is smaller than the first bias voltage."

22 Q And here, on page 22, in the

1 middle of paragraph 37, you annotated the
2 unselected word lines above n+1 with
3 first and second bias voltages, correct?

4 A Yes, in two different shades of
5 red.

6 Q And it can be observed that the
7 second bias voltage is smaller or lower
8 voltage level than the first bias
9 voltage, correct?

10 A It's not only drawn that way,
11 but the text -- it's also annotating the
12 figure indicates that concretely.

13 Q And that satisfies that claim
14 elements that were in clause that we just
15 read, correct?

16 A To the extent that the two
17 annotated voltages do represent a valid
18 first bias voltage and a second bias
19 voltage, as I believe they do, then the
20 second one is less than or smaller than
21 the first one.

22 Q So you believe that these

1 voltages that you have annotated,
2 represents a valid first bias voltage and
3 a second bias voltage as recited in Claim
4 1; is that correct?

5 ABED BALBAKY: Objection to
6 form.

7 THE WITNESS: Claim 1
8 requires or recites a first bias
9 voltage and a second bias voltage,
10 wherein the second bias voltage is
11 smaller.

12 So the claim -- the scope of
13 Claim 1 incorporates those two
14 things in that one relationship.

15 The Figure 6 can be annotated
16 with a first and second bias
17 voltages as shown, wherein, the
18 second one is less than the first
19 one.

20 BY JOHANNES HSU:

21 Q But is it your opinion that the
22 first bias voltage and the second bias

1 voltage, as you have annotated in Figure
2 6, satisfy the requirement for those two
3 voltages in Claim 1?

4 ABED BALBAKY: Objection to
5 form.

6 THE WITNESS: So the bias
7 voltages show up in multiple
8 places within Claim 1. This
9 figure is specifically relating to
10 a first bias voltage that is
11 greater than a second bias
12 voltage, that is the essence of
13 the final wherein clause of Claim
14 1. That is what I am indicating
15 here.

16 BY JOHANNES HSU:

17 Q Let's go back to Figure 4 of the
18 '957 patent.

19 A All right.

20 Q Can you identify a first and a
21 second bias voltage that satisfy the
22 wherein clause, wherein the second bias

1 voltage is a smaller than the first bias
2 voltage?

3 A I have not done that as part of
4 my declaration.

5 Q Sitting here today, you are not
6 able to form an opinion.

7 Is that your testimony?

8 A I haven't been asked to examine
9 Figure 4 in detail, other than to
10 highlight it to illustrate the pre-pulse
11 stage and the verify/read stage, as shown
12 in page 19 of my declaration.

13 But above and beyond that, to
14 identify a specific bias voltages or
15 verify voltages in Figure 4, no, I have
16 not been asked to do that and I have not
17 done so.

18 Q If you're asked today to do that
19 analysis, is that something you would be
20 able to perform today?

21 ABED BALBAKY: Objection to
22 form.

1 THE WITNESS: I could start
2 today. I do not guarantee I could
3 finish today, but...

4 BY JOHANNES HSU:

5 Q Now, going to paragraph 113 of
6 your declaration.

7 A 113, I am there.

8 Q You testified earlier that you
9 used the embodiment of Figure 7 to
10 explain the interpretation of Claims 5
11 and 6, correct?

12 A (Reviewing.) So on pages 33 and
13 34, going into 35 of my declaration, I do
14 address an argument in the petition
15 vis-à-vis the interpretations of Claim 5
16 and 6.

17 The petition used Figure 7. So
18 I have done the same.

19 Q But you did not express a
20 criticism for using Figure 7 to explain
21 Claims 5 and 6, correct?

22 ABED BALBAKY: Objection to

1 form.

2 THE WITNESS: I believe I
3 have effectively rebutted the
4 arguments vis-à-vis Claims 5 and 6
5 throughout my declaration,
6 particularly in the latter, in the
7 sections at the end addressing the
8 specific grounds.

9 There was no -- that analysis
10 would not have been helped by
11 further critiquing the use of
12 Figure 7, other than to say that
13 "Petitioner incorrectly argues
14 based on the embodiment
15 illustrated in Figure 7 of the
16 '957, any given 'top bias voltage'
17 or 'bottom bias voltage' may have
18 different values at different
19 times."

20 So I critique the argument
21 without necessarily addressing the
22 figure that was used in that

1 analysis.

2 BY JOHANNES HSU:

3 Q Your critique is that, in your
4 opinion, the same voltage level should be
5 applied in the pre-verify stage, in the
6 verify stage for the bottom bias voltage
7 and the top bias voltage, correct?

8 A Yes. As I described in
9 paragraph 54, I say that, "I agree with
10 the patent owner's interpretation of the
11 claim language, and disagree with
12 Petitioner's proposed interpretation."

13 Going on to say that, The plain
14 and ordinary meaning of the claim
15 language and the '957 patent
16 specification confirm that the limitation
17 apply a bottom/top bias voltage on a gate
18 terminal of the [TSG/BSG] transistor of
19 the first memory cell string in a
20 pre-verify stage and verify stage as
21 recited in Claims 5 and 6 is properly
22 understood to require a single voltage

1 level be applied in both of those stages.

2 Q You do not dispute that Figure 7
3 discloses a bottom bias voltage and a top
4 bias voltage, correct?

5 A (Reviewing.) So the claim
6 language of example Claim 5, is apply a
7 bottom bias voltage on a gate terminal of
8 the BSG transistor.

9 So a voltage applied to that
10 gate terminal is a bottom bias voltage,
11 as defined within that first element of
12 Claim 5. And in Figure 7, we have a BSG
13 signal connected to the gate of the BSG
14 transistor.

15 So that green annotation there
16 does satisfy the first portion of the
17 first element of Claim 5 being apply a
18 top/bottom bias voltage to -- on a gate
19 terminal of the BSG transistor.

20 Q The top waveform that you have
21 annotated in red is the top bias voltage
22 in Claim 5, correct?

1 ABED BALBAKY: Objection to
2 form.

3 THE WITNESS: Yes.
4 Similarly, the second element of
5 Claim 5, for example, defines a
6 top bias voltage as the voltage on
7 the gate terminal of the TSG
8 transistor.

9 That top bias voltage,
10 subsequently, is recited to -- to
11 have to be applied in both of the
12 stages, but the bias voltage
13 portion of that element is the
14 gate voltage on the TSG
15 transistor, as that definition
16 corresponds to the red annotation
17 on my page 34, which is a bias
18 voltage applied to a gate terminal
19 of TSG transistor.

20 BY JOHANNES HSU:

21 Q The third claim limitation of
22 Claim 5 recites a positive voltage,

1 correct?

2 A Those are the first four words
3 of the third element of Claim 5.

4 Q Did you perform any analysis
5 with respect to that claim element?

6 A (Reviewing.) With regard to the
7 '957 patent, no, I was not looking at the
8 embodiments of the '957 to see whether
9 they have positive voltages on the gate
10 terminals of memory cells. However, it's
11 clear from superficial examination of
12 those figures, that they are all shown to
13 be positive.

14 Q Are you equating any voltages
15 with they positive voltage level with the
16 positive voltage claimed in Claim 5?

17 ABED BALBAKY: Objection to
18 form.

19 THE WITNESS: Well, Claim 5
20 recites a positive voltage on gate
21 terminals. So anything that
22 anticipates or infringes will have

1 to have a positive voltage on a
2 gate terminal.

3 With regard to the
4 embodiments of the '957, I have
5 not rendered an opinion that it
6 does have positive voltages on
7 gate terminals on any of its
8 embodiments because that's not
9 central to my role of critiquing
10 the petition and Dr. Liu's
11 declaration.

12 So to that extent, I have not
13 applied a particular definition to
14 a positive voltage, other than the
15 plain and ordinary meaning.

16 BY JOHANNES HSU:

17 Q What I was trying to clarify was
18 the limitation says apply a voltage --
19 strike that.

20 The claim limitation says,
21 "apply a positive voltage on gate
22 terminals," and then it goes on to

1 qualify what gate terminals it is
2 referring to.

3 I just wanted to clarify that
4 you are not equating this claimed
5 positive voltage with any of the
6 waveforms that's shown in Figure --
7 Figure 7, that may happen to have a
8 positive voltage level?

9 A Yes. I was not asked to
10 really -- to look at the embodiments of
11 the '957 and to conclude affirmatively or
12 otherwise that they offer a positive
13 voltage on a gate terminal or relative to
14 the subsequent phrases in that element.

15 Q So just to be clear, you have
16 not formed any opinion as to -- which
17 waveform in Figure 7 may or may not
18 satisfy that positive voltage limitation
19 in Claim 5; is that correct?

20 A As I testified at length
21 earlier, I was not asked and did not
22 perform any analysis vis-à-vis the

1 embodiments of the '957 to see which of
2 them read on any of the claims in
3 particular.

4 Q So just -- strike that.

5 Did you perform any analysis
6 with respect to Claim 4?

7 A The only analysis that I
8 performed with regard to Claim 4 is to
9 note that it depends on Claim 1, and,
10 therefore, any reference that fails to
11 anticipate Claim 1 would also fail to
12 anticipate Claim 4.

13 I don't know if I actually wrote
14 that down as far as an opinion, but it's
15 certainly with regard to the grounds
16 analysis towards the end of my
17 declaration, I think I said things to
18 that effect. But I will have to check to
19 be sure, if you wish me to do -- to be
20 definitive.

21 Q Let me ask a more specific
22 question.

1 Is it the case that you did not
2 perform an analysis with respect to any
3 of the additional limitations of Claim 4?

4 A Again, I was not asked to do so
5 and did not perform such analysis.

6 Q And if you are asked to perform
7 such an analysis in this deposition, you
8 may or may not be able to complete it
9 today; is that correct?

10 A That's a fair statement.

11 Q Now, you recall earlier we had
12 discussion about what a gate is of a
13 memory cell versus a word line?

14 Do you recall that?

15 A We had extended discussions
16 about a word line layer relative to the
17 gate of a transistor.

18 Q And is it your opinion that a
19 voltage applied on a word line layer is
20 not the same as a voltage applied on a
21 gate terminal?

22 ABED BALBAKY: Objection.

1 Form.

2 THE WITNESS: In the context
3 of 3D NAND Flash, those two things
4 are not the same.

5 BY JOHANNES HSU:

6 Q Can you explain the basis for
7 your opinion?

8 A (Reviewing.) I have about close
9 to ten pages describing what goes on
10 within a 3D NAND Flash memory device
11 vis-à-vis the target voltages for the
12 word lines and the voltages as they
13 ultimately reach the gates of memory
14 cells. We can read those entire pages
15 into the record, if you want, or if
16 there's any particular portion of that
17 you would like to discuss in particular,
18 I would be happy to.

19 Q Are you able to succinctly
20 summarize the basis for your opinion?

21 ABED BALBAKY: Objection to
22 form.

1 THE WITNESS: I think my
2 opinions speak for themselves and
3 the full support for those
4 opinions is all laid out there.

5 I think in brief, since you
6 asked me to summarize, it's that
7 the word line layers, though they
8 are conductive, are really large.
9 They have resistance. They are
10 really large and close to each
11 other, and so they have really
12 large capacitances. The word line
13 drivers have specific source
14 impedances.

15 All those things combined, to
16 me, that the word line driver can
17 start to drive a target voltage at
18 a particular instance, but that
19 the voltage at a distant memory
20 cell, will take significant time
21 to have its gate voltage rise up
22 to a value that's comparable to

1 that target voltage.

2 And this is explained in
3 detail in the '957, the difference
4 between target voltages and actual
5 gate voltages.

6 BY JOHANNES HSU:

7 Q You mentioned resistance of the
8 word line layers in your previous answer,
9 correct?

10 A I did.

11 Q Sorry you -- my connection was
12 broken a little bit.

13 A Did you want me to reiterate the
14 answer?

15 Q No, not reiterating. I'm just
16 confirming that you referred to
17 resistance of the word line layers in
18 your previous answer.

19 A Yes. In this case, since it's a
20 -- they are not wires, they are sheets.
21 So it's a sheet resistance.

22 Q And then the capacitance of --

1 strike that.

2 You also mentioned large
3 capacitances because the word line layers
4 are large and close to each other,
5 correct?

6 A Separated by a thin dielectric,
7 which is what you want to have a large
8 capacitance.

9 Q And are those resistance and
10 capacitance related to the RC
11 time-constant, as discussed in your
12 declaration?

13 A In part, yes. In addition to
14 the source resistance of the word line
15 drivers.

16 Q Can you point me to where in
17 your declaration you talked about
18 resistance of word line drivers?

19 A (Reviewing.) That's all
20 encompassed in my declaration beginning
21 in paragraph 94, going on to 95 as well.
22 It talks about the word line drivers and

1 how they operate and how the RC
2 time-constant is derived from the
3 physical and electrical characteristics
4 of the circuit as a whole, including the
5 word line drivers.

6 Q And the capacitance is a result
7 of the word line layers functioning as
8 conductive plates of a capacitor
9 separated by a dielectric layer, correct?

10 A Yes. And those conductive
11 plates have internal sheet resistance, as
12 well, which contributes to the overall AC
13 frequency response of that capacitor as
14 driven by the word line.

15 JOHANNES HSU: Okay. I think
16 we have been going about an hour.
17 So we can take a break.

18 THE WITNESS: Yes, please.

19 THE REPORTER: Off the
20 record.

21 (Whereupon a Recess Commenced
22 at 4:08 p.m. and Testimony

1 Recommenced at 4:14 p.m. EDT.)

2 BY JOHANNES HSU:

3 Q Doctor, welcome back.

4 A Thank you.

5 Q So right before the break we
6 were talking about resistance and
7 capacitance. I just want to make sure I
8 am understanding your opinion correctly.

9 I understand the capacitance is
10 from -- basically the word line layers,
11 together with the intermediate dielectric
12 layers acting as capacitors; is that
13 correct?

14 A That's certainly one component
15 of the overall capacitance as it would be
16 analyzed to determine the actual signal
17 waveforms through the 3D NAND Flash
18 device.

19 Q And there are two sources of
20 resistance; one is from the sheet
21 resistance of the word line layers, and
22 the other is from the word line drivers,

1 correct?

2 A Well, there are additional
3 resistance components, whether they are
4 dominant or inconsequential depends on
5 the actual physical layout of a specific
6 3D NAND Flash design.

7 I mean, if you look at Figure 2,
8 you could see where there are additional
9 components that would contribute to both
10 resistance and capacitance that are
11 evident within that physical structure.

12 Q What is a reason that in your
13 opinion Figure 2 of Hongtao does not
14 disclose gate voltages?

15 A (Reviewing.) At least in part,
16 in my section IX-A about Hongtao,
17 starting on page 35 of my declaration, I
18 note that, like, for example, Figure 4 of
19 the '957, Hongtao shows voltages as
20 piecewise linear.

21 In other words, they are not
22 showing actual voltages, but they are

1 showing idealized target voltages that
2 are not reliably representative of the
3 actual voltage on any particular gate of
4 a particular memory cell.

5 Q You said "at least in part."

6 Are there other reasons that
7 support your opinion that Figure 2
8 Hongtao does not disclose gate voltages?

9 A Can you put Hongtao into the
10 chat, please?

11 Q It's going to take me just a
12 little while. I will try to make it
13 fast.

14 A Yeah. I can't answer that
15 without actually looking at Hongtao. I
16 only have citations to it and the
17 figure -- a few of the figures we
18 produced in my declaration. So I need
19 the whole thing.

20 Q Sure. Actually, maybe let's try
21 a different question --

22 A Okay.

1 Q -- for the time being.

2 What is the reason that, in your
3 opinion, Costa does not disclose gate
4 voltages?

5 ABED BALBAKY: Objection to
6 form. Objection, foundation.

7 THE WITNESS: (Reviewing.)

8 Likewise, can you put Costa into
9 the chat, please?

10 BY JOHANNES HSU:

11 Q So are you not able to answer
12 those questions by just referring to your
13 declaration?

14 A I might, but there are citations
15 within my declaration that I would like
16 to look at to understand, refresh my
17 memory, in terms of what exactly I was
18 citing to.

19 So I can read to you the
20 portions of my declaration about those
21 two references. If you want anything
22 above and beyond that, I need to look at

1 the actual references.

2 Q Okay.

3 So I just put Hongtao into the
4 chat box.

5 A Okay. Thank you.

6 Q Let me know what references
7 you're looking at in your declaration,
8 please.

9 A So back to Hongtao now.

10 (Reviewing.)

11 So can you repeat the question
12 about Hongtao, since that was previous?

13 Q Besides the piecewise linear
14 form of Figure 2 in Hongtao, are there
15 other reasons that support your opinion
16 that that particular figure, Figure 2,
17 does not display -- disclose gate
18 voltages?

19 A Well, I think that that is more
20 than sufficient reason. Just -- Hongtao,
21 in paragraph 14, says that it is a timing
22 diagram for reading a 3D NAND memory

1 cell. But a POSITA looking at that would
2 say that's obviously not an actual timing
3 diagram of specific voltages, it's
4 stylized, it's abstracted, if you will,
5 and that those are not actual voltages,
6 but target voltages that are being
7 described in Figure 2.

8 Q We discussed earlier that the RC
9 time-constant associated with NAND Flash
10 memory, correct?

11 A In part, yes.

12 Q Now, what determines an RC
13 time-constant?

14 A In the simplest RC time-constant
15 circuit, you have an idealized voltage
16 source. You have a resistance and
17 capacitance and that -- in that
18 circumstance, the time-constant is very
19 simple. It's just a product of the
20 resistance of capacitance.

21 In the circumstances we are
22 talking about here, where you have a

1 distributed resistance and a distributed
2 capacitance of the plate capacitors
3 between the word line layers, plus the
4 distributed capacitance of all OF the
5 gates of the memory cells and the
6 distributed capacitances between the
7 gates of the memory cells and the sources
8 and drains and channels of those memory
9 cells, there is no simple algebraic
10 representation of the waveform, but it is
11 still characterized as an RC
12 time-constant waveform, even though it is
13 much more complex than the simple example
14 I started with.

15 Q You mentioned in your
16 declaration the concept of RC delay,
17 right?

18 A Can you point me to a particular
19 paragraph?

20 Q Paragraph 94.

21 A Thank you.

22 Okay. I am there.

1 Q Here, in paragraph 94, you
2 stated, I am quoting here, "...each word
3 line has an RC time-constant that arises
4 from the large capacitances produced by
5 the layered structure of the device."

6 And then you cite Exhibit 1014,
7 with a parenthetical, (discussing the 'RC
8 (resistance-capacitance) delay' in word
9 lines..."

10 Is that correct?

11 A That's what I wrote there, yes.

12 Q What is an RC delay?

13 A As illustrated in the figure
14 that I created and added on my page 62,
15 you see that the abstracted voltage
16 applied to a word line is shown in the
17 top portion of that figure as being, you
18 know, having a high slew rate to a target
19 voltage, but that by the time you get to
20 the gate of a memory cell at the far end
21 of the integrated circuit, the rate of
22 change of the voltage at that gate will

1 be smoothed into an exponential and the
2 difference in time between when that
3 voltage at the gate reaches its effective
4 value, whatever that happens to be in
5 that circuit, and the transition of the
6 voltage applied to the word line driver,
7 that delay constitutes what would be
8 understood by a POSITA to be an RC delay.

9 Q You began paragraph 94 with a
10 statement that "each word line has an RC
11 time-constant..." Correct?

12 A Yes.

13 Q Is that RC time-constant for
14 each word line the same as other word
15 lines or different for each word line?

16 A Well, it's not just different
17 for each word line, but it's different
18 for each memory cell on the word line.
19 Because, as we have noted previously, the
20 resistance and the capacitances are
21 distributed, and so the amount of delay
22 at one end of the device might be

1 different than at the other end of the
2 device.

3 So the -- when we talk about the
4 RC delay or RC time-constant in such a
5 complex environment, it's not just the
6 simple product of the resistances
7 capacitance, but it is, in fact, a
8 complex simulation to determine how much
9 delay is present at any particular memory
10 cell.

11 Q So where does the delay occur
12 between its source -- strike that.

13 I understand -- there's a delay
14 at the gate, correct?

15 A There is a delay relative --
16 between the word line driver's input, be
17 it, enables as well as voltages, and when
18 an effective voltage is observable at a
19 particular memory cell, somewhere within
20 the memory array.

21 You asked me a couple of
22 questions ago about whether they were all

1 the same or did you withdraw that
2 question? All the word lines RC delays?

3 BY JOHANNES HSU:

4 Q I understood you to have
5 answered the question that they each have
6 different --

7 A Yeah, okay. Very good.
8 They are all different because
9 of the staircase -- at least in part
10 because of the staircase structure. The
11 area of each word line layer is
12 different. So the capacitances that
13 contribute to this RC delay are different
14 for each memory word line layer. So
15 that's one aspect of why they are all
16 different.

17 Q Would it be more precise to
18 characterize the delay experienced by a
19 particular voltage not by just an area of
20 the word line layer it travels on, but
21 rather the path it takes from the word
22 line contact to the gate terminal?

1 A Well, all of these things
2 contribute to the overall delay. And
3 that's why I am saying it's not a simple
4 product of a resistance and capacitance,
5 but there's the word line source
6 resistance.

7 If you look at Figure 2, there's
8 the resistance of the vias down to the
9 appropriate word line level, and then it
10 is the distributed RC characteristics of
11 the word line layers, which are areas, as
12 we discussed.

13 Plus we have the capacitances
14 associated with the myriad memory cells
15 that are coupled to each individual word
16 line layer.

17 So all of these things
18 contribute to the delay, and it's -- some
19 are much larger than others, some memory
20 cells are closer to the word lines than
21 others so they might have a less delay,
22 some might be lower down in the stack so

1 their capacitance are bigger. They might
2 have greater delay. It all varies.

3 Q Now, looking at Figure 2 of
4 Hongtao.

5 Do you understand the waveforms
6 -- voltage waveforms that's illustrated
7 in Figure 2 as applied to the labels and
8 selected word lines and selected word
9 lines to be the voltage's presence on the
10 word line layer?

11 A (Reviewing.) In light of the
12 entire specification, and Figure 2 in
13 particular -- as I say on my page 38,
14 towards the bottom, Figure 2 of Hongtao
15 depicts target voltages that are being
16 administered to the word lines, and not
17 reflect the actual bias voltages present
18 at any specific time at the gates of the
19 memory cells.

20 So whether they are the target
21 voltages being applied to as one of the
22 inputs to the word line drivers or

1 whether they are at the top of the via
2 going down to the memory -- to the word
3 line layers, is not something I needed to
4 opine on to come to the conclusion about
5 Hongtao and the arguments about it in the
6 petition and declaration.

7 Q You see Figure 2, Hongtao, there
8 is a waveform that's labeled Top Select
9 Transistor of the Selected Stream.
10 Correct?

11 A Top select transistor of the
12 selected string. Yes. That's the second
13 one from the top. That one?

14 Q And the third one from the top
15 -- strike that.

16 And the second one from the
17 bottom is Bottom Select Transistor of the
18 Selected String. Correct?

19 ABED BALBAKY: Objection to
20 form.

21 THE WITNESS: That's how it's
22 labeled in Figure 2, yes.

1 BY JOHANNES HSU:

2 Q And both of these waveforms are
3 given the conduction voltage during the
4 red read phase of the diagram, correct?

5 A Yes. The conduction voltage is
6 applied -- is shown there in the read
7 phase for those two signals, as well as
8 the unselected word lines.

9 Q These waveforms are specifically
10 identified as the waveform for the top or
11 bottom select transistors, correct?

12 A Are you reading specifically
13 from Hongtao?

14 Q Correct.

15 A What paragraph?

16 Q I am just looking at the figure.

17 A Oh. (Reviewing.)

18 I think a POSITA, in looking at
19 the entirety of Figure 2, would
20 understand that just like the unselected
21 and selected word lines are showing
22 target voltages on their way to the

1 corresponding memory cells, the top
2 select and bottom select waveforms are
3 also depicting target voltages that will
4 be sent towards those top select and
5 bottom select transistors; that all of
6 these are comparable.

7 Q Would a POSITA looking at Figure
8 2 understand where on the way to the
9 corresponding memory cells these
10 waveforms capture that?

11 ABED BALBAKY: Objection to
12 form.

13 THE WITNESS: I don't think
14 the term "captured" is appropriate
15 here. This is trying to teach
16 what -- teach the operation of the
17 memory's device in Hongtao and
18 these waveforms have been
19 abstracted or stylized in order to
20 clarify what is going on.

21 In the process of doing so,
22 showing target voltages, not

1 actual voltages on specific nodes
2 at memory cells, and that applies
3 to the select transistors, as well
4 as it does to the memory cells.

5 BY JOHANNES HSU:

6 Q But you testified that these
7 waveforms are showing target voltages on
8 their way to the corresponding memory
9 cells, correct?

10 A Well, they are the target
11 waveforms at the drivers and the drivers
12 are sending these signals on to the word
13 line layers, which communicate them,
14 albeit in a modified form, towards the
15 memory cells and the select transistors
16 throughout the memory array.

17 Q So is it -- strike that.

18 So if I understand you
19 correctly, your testimony is that these
20 waveforms are waveforms at the outputs of
21 the word line drivers; is that correct?

22 A They could be at the output of

1 the word line drivers or input to the
2 word line drivers. It doesn't matter.
3 I did not need to form an opinion on that
4 distinction to understand what Hongtao is
5 teaching vis-à-vis Figure 2, and the
6 actual voltages that a POSITA would
7 understand are on the gates of the memory
8 styles.

9 Q Ignore the distinction about
10 input versus output for this question.

11 Is it your opinion that Figure 2
12 of Hongtao illustrates waveforms at the
13 word line drivers?

14 ABED BALBAKY: Objection to
15 form.

16 THE WITNESS: Yes. As I have
17 said on page 38, and as I have
18 already highlighted to you, I say
19 that, Figure 2 of Hongtao depicts
20 the target voltages that are being
21 administered to the word lines,
22 and do not reflect the actual bias

1 voltages present at any specific
2 time at the gates of the terminals
3 of the memory cells.

4 So either they are at the
5 word line, as you suggest -- I'm
6 sorry, at the word line driver.

7 BY JOHANNES HSU:

8 Q The word line driver voltages,
9 according to paragraph 58, are applied or
10 administered to the word line layers; is
11 that correct?

12 A Yes. Because the way that the
13 word line drivers communicate, word line
14 voltages to memory cells and select
15 transistors is via the word line layers.

16 Q Would the voltage waveforms --
17 strike that.

18 How would the voltage waveforms
19 look at the intersection of a word line
20 contact in a corresponding word line
21 layer?

22 A Can you describe what you mean

1 by "word line contact"?

2 Q Word line contact is, as we
3 discussed earlier, as an example, the
4 vertical structure numbered 22 in Figure
5 2 of the '957 patent.

6 A Right. Okay.

7 So we don't know very much from
8 Hongtao about how the word lines are
9 driven, where the word line drivers are,
10 or how they are connected to the word
11 line layers.

12 That's, again, something that's
13 very device specific. And Figure 2 of
14 the '957 shows us one possible
15 implementation. We don't know whether
16 Hongtao is contemplating a comparable or
17 identical structure or something somewhat
18 different.

19 That said, the smooth and
20 delayed waveforms at the gates of the
21 memory cells are depicted on page 40, in
22 the figure I have drawn there.

1 I think that answers your
2 question, but correct me if I am wrong.

3 Q So looking at the figure on page
4 40 of your declaration, your testimony is
5 that the original waveform showing
6 Hongtao, the waveform that's in black, is
7 the waveform at the word line driver --
8 let me pause there.

9 Do you agree so far?

10 A Yes.

11 Q And the waveform that you have
12 added in red is the waveform of the gate
13 voltage; is that correct?

14 A Yes, and that's what I describe
15 in the paragraph immediately preceding
16 that figure.

17 Q And your testimony is also that
18 it cannot be determined what the waveform
19 looks like at the intersection of a
20 waveform -- of a word line contact and
21 word line layer; is that correct?

22 ABED BALBAKY: Objection to

1 form.

2 THE WITNESS: Because the
3 actual waveform in terms of
4 voltages and nanoseconds, is
5 highly dependent on the specifics
6 of the implementation, we can't
7 put numbers onto the red line.

8 But we can deduce that the red
9 line exists different from the
10 black line, and that it would have
11 approximately that shape.

12 BY JOHANNES HSU:

13 Q Where did you get the idea that
14 this waveform illustrates something on
15 the order of nanoseconds?

16 A Well, we have, in the '957, the
17 distinction between short and long
18 pre-charge periods. And at one extreme,
19 it's in nanoseconds and for the other
20 extreme, for very long pre-pulse periods,
21 it's in microseconds.

22 So this -- in the timeframe of

1 the filing of the '957, we typically are
2 dealing in nanoseconds as a relevant time
3 unit.

4 Q Is it your opinion that the
5 claims of the '957 patent only applies to
6 embodiments with a pre-verify stage on
7 the order of nanoseconds?

8 A No. The claims don't mention
9 nanoseconds at all. That's not -- the
10 claims -- the claims, they speak for
11 themselves.

12 The -- what I am doing here is I
13 am critiquing the specific implementation
14 of Hongtao and how its figure was
15 misinterpreted in the petition and
16 declaration of Dr. Liu.

17 Q Since the claims are not
18 restricted to a pre-verify stage on the
19 order of nanoseconds, can Hongtao Figure
20 2 disclose a pre-verify stage that's on
21 the order of, for example, up to
22 10 microseconds, as stated in the '957

1 specification?

2 ABED BALBAKY: Objection to
3 form.

4 THE WITNESS: In the '957
5 specification, there are two
6 domains that are discussed, short
7 and long. In Hongtao we can
8 assume that we are dealing with
9 short pre-verify -- not the right
10 word -- short pre-conduction
11 phases. Because if they were
12 long, they would be -- they would
13 be wasting significant amount of
14 time and they would be drawn
15 differently.

16 So the presumption that a
17 POSITA would have, looking at
18 Figure 2 and the specification of
19 Hongtao not indicating that the
20 pre-conduction phase is
21 specifically longer than
22 necessary, a POSITA would

1 recognize that the pre-conduction
2 phase here is short and that the
3 figure on page 40 is appropriate.

4 BY JOHANNES HSU:

5 Q It is your opinion that the
6 claims of the '957 patent is not limited
7 to a short pre-verify stage, correct?

8 A As I have said, the claims don't
9 talk about long or short. I have not
10 been asked to opine on the scope of those
11 claims -- those elements in whether they
12 would apply only to long or short. I
13 have not had to do that in order to
14 effectively critique the arguments in the
15 petition and Dr. Liu's declaration.

16 Q So sitting here today, you have
17 no opinion as to whether the claims of
18 the '957 patent are limited to a short
19 pre-verify stage, correct?

20 ABED BALBAKY: Objection to
21 form.

22 THE WITNESS: I was not asked

1 to form an opinion on that aspect
2 of the claims and I did not do so.

3 BY JOHANNES HSU:

4 Q And what disclosure from Hongtao
5 did you rely on to opine that its
6 pre-conduction phase has a short duration
7 on the order of nanoseconds?

8 ABED BALBAKY: Objection to
9 form.

10 THE WITNESS: Well, certainly
11 the application date for Hongtao
12 being 2018 would indicate that the
13 context for Hongtao's discussion
14 of memory circuits would be in the
15 context of the processes that are
16 in place at that time when which
17 signal transitions happen in
18 nanoseconds, not microseconds.

19 That's being the principal
20 reason why I answered the way I
21 did previously.

22 BY JOHANNES HSU:

1 Q The '957 was filed after
2 Hongtao, correct?

3 A The '957 drives priority to
4 December 15, 2020.

5 Q And that's after Hongtao's
6 priority, correct?

7 A I have been asked to assume that
8 it's prior art. I did not actually see
9 whether it's -- is, in fact, that way.
10 It does list on its front page that it's
11 application publication date is 2018,
12 which is before 2020.

13 But again, that's not a formal
14 opinion of mine that it is prior art.

15 Q And presumably, the technology
16 in 2020 is more advanced than the
17 technology in 2018, correct?

18 A Possibly. We would have to look
19 at the introduction dates of specific
20 technology nodes to see if that's true or
21 not. I have not done that. I do not
22 have that information off the top of my

1 head.

2 Q Right.

3 But you have no reason to think
4 that the technology actually regressed
5 within those two years, correct?

6 A COVID did a lot of things, but I
7 don't think it did that.

8 Q Okay.

9 So when '957 discloses long
10 pre-verify stages and not limit its
11 claims to only a short pre-verify stage,
12 is the '957 wasting significant amount of
13 time in its operations?

14 ABED BALBAKY: Objection to
15 form. Objection to foundation.

16 THE WITNESS: (Reviewing.)
17 Again, I have not been asked to
18 analyze the embodiments of the
19 '957 in detail to see whether
20 they -- the embodiments with
21 specified long pre-pulse periods
22 are wasting time, to use your

1 words.

2 But -- so I don't have an
3 opinion on that. I haven't been
4 asked to do so.

5 BY JOHANNES HSU:

6 Q And just for clarity, the phrase
7 "wasting significant amount of time" was
8 your words. I was just borrowing it.

9 A You were borrowing it.

10 Q Now, can you point me to
11 anything within the four corners of
12 Hongtao that discloses the pre-conduction
13 phase to be a short duration on the order
14 of nanoseconds?

15 ABED BALBAKY: Objection to
16 form.

17 THE WITNESS: (Reviewing.)
18 Certainly. If you look at Figure
19 2, we have a number of clues that
20 points us towards that conclusion.

21 First of all, is the
22 particular shape for the top

1 select, unselected, and bottom
2 select -- bottom select transistor
3 selected string for top and
4 bottom, as well as the shape
5 depicted for the selected word
6 lines, that all indicate that
7 these transitions of voltage and
8 the specified periods of time are
9 not excessively long. They are
10 sufficient to perform a specific
11 operation, and that's all, and not
12 substantially longer than
13 necessary.

14 This comes from the drawn
15 length of the pre-conduction phase
16 and the drawn length of the
17 individual read voltage periods.

18 Now, granted, these are not
19 drawn to scale, but they are an
20 indication to a POSITA that we are
21 in a -- to use the '957's
22 terminology -- a short pre-pulse

1 period domain.

2 BY JOHANNES HSU:

3 Q But you can't point me to
4 anything in the Hongtao specification
5 that discloses this; is that correct?

6 A To reiterate, I was critiquing
7 the petition and the declaration of Dr.
8 Liu. In neither of those documents is
9 there any suggestion that the
10 pre-conduction phase is longer than
11 necessary in Hongtao. That the whole
12 topic was not addressed.

13 So the presumption, then, is
14 what a POSITA would look at and would
15 come to conclusion that these are short
16 pre-conduction periods relative to the
17 overall operation time and that makes
18 sense and it's entirely internally
19 consistent that that's the case. Figure
20 2 by itself teaches that.

21 Q And Figure 2 by itself teaches
22 that because, as you testified earlier,

1 the waveforms have a particular shape; is
2 that correct?

3 A That is the principal aspect of
4 Figure 2, that's suggesting to a POSITA
5 that that's the case. There's been no
6 suggestion within the petition or
7 declaration that that's not the case. So
8 there was no need to rebut an argument
9 that was not made.

10 Q What about the shape suggests
11 that the duration is short on the order
12 of nanoseconds?

13 ABED BALBAKY: Objection to
14 form.

15 THE WITNESS: Again, not
16 necessarily nanoseconds, but
17 short.

18 In other words, as the term
19 is used in the '957, that the
20 actual voltages have not
21 completely gotten to their target
22 levels by the end of the

1 pre-conduction phase. That's a
2 transliteration of 957's
3 discussion of long versus short
4 into the terminology of Hongtao.

5 But the fact that, for
6 example, the unselected word lines
7 go higher than the conduction
8 voltage for a short period time
9 during the pre-conduction period
10 in order to accelerate the
11 transition from the quiescence
12 state to the conduction voltage
13 state, prior to entering the read
14 portion of the operation, is what
15 is indicative to a POSITA that we
16 are dealing in a short domain.

17 It's been another hour.

18 JOHANNES HSU: Thank you for
19 that reminder. Let's take another
20 break.

21 THE WITNESS: Okay. Another
22 five, please.

1 JOHANNES HSU: Thank you.

2 THE REPORTER: Off the
3 record.

4 (Whereupon a Recess Commenced
5 at 5:05 p.m. and Testimony
6 Recommenced at 5:12 p.m. EDT.)

7 BY JOHANNES HSU:

8 Q Doctor, welcome back.

9 A Thank you.

10 Q Can you identify for me where in
11 Hongtao the disclosure mentions word line
12 drivers?

13 A (Reviewing.) Well, a POSITA
14 looking at Figure 1 would see the word
15 lines connected to memory cells and
16 recognize that in that figure, there is
17 nothing shown driving those word lines
18 but there must be. So it is implied in
19 Figure 1 that there are word line drivers
20 connected to those drawn word lines.

21 Q But are you able to find that
22 disclosure in the -- within the four

1 corners of Hongtao?

2 A I believe a POSITA would find it
3 inherent in Figure 1.

4 Q Is it your testimony that a
5 POSITA would infer a driver from Figure 1
6 and import the word driver into Figure 2?

7 ABED BALBAKY: Object to
8 form.

9 THE WITNESS: I think Figure
10 2 speaks for itself. And as we
11 said, we acknowledge that these
12 control signals are driven into
13 the memory array, that that's
14 inherent in the concept of a 3D
15 NAND Flash memory device, and
16 there's no need to explicitly
17 import the word "driver" into
18 Figure 2, even though we found
19 that a POSITA would find the
20 concept of a word line driver,
21 driving the shown word lines as
22 being necessary in Figure 1.

1 BY JOHANNES HSU:

2 Q Let's go back to your
3 declaration. Page 62, paragraph 94.

4 (Reporter Clarification.)

5 BY JOHANNES HSU:

6 Q Page 62.

7 A Okay. I am there.

8 Q We discussed this figure
9 earlier, right, that you prepared?

10 A Yes, we did.

11 Q I just want to get a better
12 understanding of this figure.

13 So the vertical axis, if one
14 were present, represents voltage level,
15 correct?

16 A Yes. That's implied by the name
17 of each of the traces as being voltage
18 applied or voltage at.

19 Q An increasing or higher voltage
20 level in the upward direction, correct?

21 A Yes, that's standard.

22 Q And the horizontal represents --

1 horizontal axis represents time, correct?

2 A Yes.

3 Q And later in time in the
4 rightward direction?

5 A Yes, in the abstract. So no
6 specific units attached to the figure.

7 Q Even though no specific units
8 are attached to the figure, would it be
9 fair to say that they are intended to
10 represent the same time scale?

11 A Yes. That's common with regard
12 to timing diagrams, or as the '957 calls
13 them, schematics, where the multiple
14 traces shown together, they are assumed
15 to be at the same time scale.

16 Q How about the vertical scale?
17 Did you also intend that the
18 voltage are represented by the same
19 scale?

20 A Roughly speaking, yes. But
21 it's, again, since there are no
22 specifics, it's indicative of an RC

1 time-constant and an RC delay.

2 So a POSITA with the basic
3 understanding of RC circuits would
4 understand that the voltage at the gate
5 of a cell was going to rise according to
6 an exponential, and yet, asymptotically
7 close to the target voltage as applied to
8 the word line driver.

9 Q Are you saying that the figure
10 should not be interpreted to have the
11 same voltage scale for these two
12 waveforms?

13 A No, I don't think that was my
14 testimony at all.

15 Q So would it be acceptable to
16 interpret these two waveforms to be on
17 the same voltage scale?

18 A As I have mentioned just a
19 moment ago, yes, approximately so.

20 Q And do the top and bottom
21 waveforms start from the same initial
22 voltage?

1 A A POSITA looking at these pairs
2 of figures, recognizing that they are the
3 same signal at different points along its
4 path to its destination, and that there
5 is a quiescent period at the beginning
6 before the transition, a reasonable
7 conclusion for a POSITA to make is that
8 they are both starting at the same
9 voltage level probably VSS.

10 Q And the high horizontal level of
11 the top waveform represents a target
12 voltage level, correct?

13 A Yes.

14 Q Now, if we draw a horizontal
15 line across each of the two waveforms at
16 the same level above the initial level,
17 which you said to be the same, is it fair
18 to say that the horizontal line would
19 intersect the top waveform earlier in
20 time than the horizontal line would
21 intersect the bottom waveform?

22 A You mean for a horizontal line

1 that we are drawing across both
2 waveforms?

3 Q Two horizontal lines, one across
4 each waveform, equal distance above the
5 respective initial level.

6 A And some non-trivial amount
7 above the quiescent level.

8 Is that what you are
9 hypothesizing?

10 Q Fair enough. Non-trivial
11 amount.

12 A Then, yes, the figure is showing
13 that the target waveform transitions
14 quickly, and that by the time you get to
15 a memory cell gate, a period of time has
16 elapsed, and if you need that voltage at
17 the gate to reach a particular level in
18 order to appropriately perform a specific
19 operate, then that's going to be towards
20 the end of that rising exponential as
21 shown.

22 Q In other words, there's a delay

1 of the gate voltage relative to the
2 target voltage, correct?

3 A Yes. The voltage at the memory
4 cell, which has to reach some level in
5 order to turn that memory cell on based
6 on what its actual threshold voltage is,
7 will be significantly delayed relative to
8 the transition in the target voltage
9 indicated in the top line.

10 Q Is there a delay at any
11 particular voltage level above the
12 initial level?

13 And let's assume that difference
14 is non-trivial, as we discussed earlier,
15 difference in voltage level.

16 A Yes. The higher the voltage you
17 need at the gate of the memory cell, the
18 longer the delay will be.

19 Q And that is the RC delay
20 associated with the RC time-constant,
21 correct?

22 A Yes. As we discussed at length

1 earlier, for this particular circuit for
2 a 3D NAND Flash, the RC delay is a
3 complicated aggregation of distributed
4 volt resistances and capacitances and a
5 non-zero source resistance for the driver
6 and a host of other factors which make it
7 look essentially like exponential, a
8 rising exponential.

9 Q Now, in the last sentence right
10 above the figure, you stated, the RC
11 time-constants associated with a given
12 word line layer, correct?

13 A Yes. And again, as we discussed
14 previously, each word line layer is going
15 to have a unique set of resistance and
16 capacitance factors that determine the
17 rise time of the voltage at a particular
18 memory cell.

19 Q What are these unique set of
20 resistance capacitance factors that
21 determines the rise time of the voltage?

22 A Well, we went through them all

1 earlier. There's the distributed
2 resistance of the sheet of conductor that
3 represents each word line layer. There
4 is the distributed capacitance of the
5 word line layer to each of its adjacent
6 neighbors. And in cases like this, you
7 actually have to look not just at the
8 neighbors, but the one beyond the
9 neighbors to get capacitive couplings
10 fully nailed down.

11 And then we also have the
12 distributed capacitance of all of the
13 memory cells attached to -- coupled to a
14 particular word line layer.

15 Plus, we have the source
16 resistance of the driver and any
17 resistance of any wires between the
18 driver and the corresponding word line
19 layer.

20 There are probably others, too,
21 that I have neglected to mention that may
22 or may not be significant in the overall

1 calculation.

2 Q Now, in that last sentence above
3 the figure, RC time-constants is in the
4 plural. And as stated, that RC
5 time-constants, plural, associated with a
6 given word line layer.

7 Did you intend to say a given
8 word line layer has multiple RC
9 time-constants?

10 A Well, the overall aggregate RC
11 time-constant is derived from a
12 distributed collection of small RC
13 time-constants. So technically, that is
14 accurate.

15 It may have been clear if I had
16 left off the "S" from constants in that
17 sentence, but it's valid either way.

18 Q And then these distributed
19 resistance and capacitance, they would be
20 determined in part by, for example, the
21 dimensions at the word line layer?

22 A Every physical aspect of the

1 integrated circuit and the layers
2 therein, contribute one way or another to
3 the resistances, capacitances,
4 inductances of the circuits.

5 So there's a very tight coupling
6 between the physicality of the device and
7 the time constants that will be observed.

8 Q And to the extent that these
9 factors determine the resistance or the
10 capacitance, they consequently impact the
11 value of the RC time-constant, correct?

12 A Yes, that's a fair assessment;
13 that a POSITA would understand that the
14 overall shape of the voltage at the gate
15 of the memory cells is determined by a
16 myriad factors, both physical and
17 electrical, and material too.

18 Q What is the time-constant you
19 used to draw this figure on page 62 in
20 paragraph 94?

21 A As I mentioned before, it's a
22 pedagogical tool to illustrate the

1 distinction between target word line
2 drivers, target word line voltages, and
3 voltages at memory cells.

4 There's no axis, there's no
5 labels, there's no indication of scale.
6 It's -- and so there was no specific RC
7 time-constant that was used in
8 determining it.

9 Q What is the time-constant you
10 used to draw the figure on page 66 in
11 paragraph 98?

12 A The same answer applies. This
13 is showing that in the context of a short
14 pre-pulse period, as defined in the '957,
15 that the voltage at the gate of a memory
16 cell will transition more slowly than at
17 the word line driver inputs, and that is
18 what I am showing there.

19 Q And when you say there is one or
20 more RC time-constants associated with a
21 given word line layer, is that statement
22 true of the top-select-gate layer?

1 A It's true all of these layers
2 because the time-constant between the
3 driver and each memory cell is going to
4 be slightly different. And as we
5 discussed earlier, memory cells that are
6 closer to the word line driver will see
7 different a time-constant than ones
8 further away.

9 So there is -- in that sense,
10 each word line layer demonstrates or a
11 different RC delay based on where the
12 destination is. Each memory cell is in a
13 different physical location.

14 Q And just to be clear, it is also
15 true of the bottom-select-gate layer,
16 correct?

17 A Yes. Although we have discussed
18 this morning about the number of
19 transistors attached to the bottom select
20 layer or the top select layer may be
21 different than the number of memory cells
22 coupled to each of the word lines.

1 So again, there may be
2 differences between top and bottom and
3 word lines that are not evident within
4 these figures of Hongtao.

5 Q Is it correct that different RC
6 time-constants would result in a
7 different curvature and delay of the
8 resulting waveform relative to the target
9 waveform?

10 A Yes, that is the consequence of
11 different RC time-constants, and as a
12 designer of such a device, you got to
13 make sure that the worst case is within
14 spec.

15 Q So both figures you prepared --
16 strike that.

17 So the curved waveforms in both
18 figures you prepared in paragraph 94 and
19 paragraph 98, would look different if a
20 different time-constant is effective,
21 correct?

22 ABED BALBAKY: Objection to

1 form.

2 THE WITNESS: Yes. And they
3 are going to be somewhat
4 different, depending on a specific
5 device, how much the delay would
6 be different from one corner of
7 the device to another based on the
8 location of the word line driver,
9 and the interconnection
10 technologies.

11 But yes, there would be some
12 differences between them.

13 BY JOHANNES HSU:

14 Q Okay.

15 I am going to put in chat -- in
16 the chat box another reference -- well,
17 actually, my apologies, let's just use
18 your declaration.

19 So let's turn to page 82 of your
20 declaration.

21 A Okay.

22 Q That is Figure 11 from the

1 reference Suzuki, correct?

2 A Annotated, yes.

3 Q Thank you for that additional
4 detail.

5 It is your opinion that this
6 particular figure discloses gate voltages
7 as opposed to target voltages, correct?

8 A (Reviewing.) I am not finding
9 anywhere in my declaration where I
10 specifically say that.

11 Do you have a citation for me to
12 look at or not?

13 Q Let me confirm. I think I do.

14 Yes. Paragraph 127, for
15 example, page 84. Bottom of the page,
16 "As compared to references like Hongtao
17 and Seo..."

18 A You found it, yes, I knew it was
19 there somewhere. Thank you. I
20 appreciate that.

21 As compared -- reading from page
22 84, paragraph 127, "As compared to

1 references like Hongtao and Seo, which
2 illustrate only target voltages for
3 different word lines, Figure 11 of Suzuki
4 has the type of curved lines that are
5 indicative of actual bias voltages that
6 would develop over time at the gate
7 terminals of various transistors..."

8 Q So Suzuki Figure 11 illustrates
9 gate voltages because it shows curved
10 waveforms, right?

11 A It shows RC time-constants in,
12 generally speaking, that these are not us
13 -- stylized and abrupt piecewise linear
14 voltages, but actually smooth transitions
15 from one state to another. And that's
16 what I am using to suggest that these are
17 showing actual gate voltages and not
18 target voltages.

19 Q These transitions from one state
20 to another includes both transitions from
21 a lower voltage to a higher voltage and
22 vice-versa, correct?

1 A Yes. And that is how RC
2 time-constants work, regardless of
3 whether you are going up or down, the
4 same physics applies.

5 Q So going back to page 82,
6 paragraph 125, that annotated Figure 11
7 of Suzuki?

8 A Yes, I am there.

9 Q So you see, VCGM on two of the
10 waveforms?

11 A Yes.

12 Q Okay.

13 So in your opinion, VCGM is a
14 voltage applied to the gate terminal,
15 correct?

16 A I don't believe I characterize
17 it as such.

18 If you put the reference in the
19 chat, I could verify that for you. There
20 is one reference to VCGM in my paragraph
21 127. It doesn't answer your question,
22 no.

1 Q You have just opined -- here, as
2 well as in your declaration, that Suzuki
3 Figure 11 shows gate voltages; did you
4 not?

5 A Yes, or that is the presumption,
6 based on what a POSITA would understand
7 looking at this.

8 Q So as part of these waveforms,
9 does it not stand to reason that the
10 voltage VCGM is a gate voltage?

11 A Yes, it makes sense. But again,
12 I would like to see the reference to be
13 sure.

14 Q Is there any reason that would
15 lead you to think VCGM is not a voltage
16 applied to the gate terminal of these
17 respective memory cells?

18 A No. But again, I would like to
19 see the reference, just to confirm for
20 myself. But this would all be in the
21 context of a specific memory string
22 that's being verified -- programmed and

1 verified here.

2 Q If an entire waveform -- strike
3 that.

4 If an entire waveform
5 illustrates voltages apply on the gate
6 terminal, as you opined for Figure 11 of
7 Suzuki, is there any reason to say a
8 portion of that voltage waveform is not
9 applied on the gate terminal?

10 A No. As I just opined -- or I
11 answered your previous question, I have
12 no reason to suspect that but I prefer to
13 look at the reference to refresh my
14 memory.

15 Q I am going to put another
16 reference in the chat box. Let me know
17 when you get it.

18 A Okay. I am looking at Yang.

19 Q You've seen this document
20 before, right?

21 A I presume it's on my list of
22 documents reviewed.

1 Yes, I have.

2 Q And let's turn to Figure 8B of
3 Yang, Exhibit 2007.

4 A 8B like boy?

5 Q 8B like boy, correct?

6 A Okay. I am looking at 8B.

7 Q Figure 8B shows waveforms with
8 smooth curve lines, correct?

9 A Yes, it does.

10 Q So is it your opinion that a
11 POSITA looking at this figure, would
12 conclude these waveforms represent
13 voltages apply on gate terminals of these
14 respective transistors?

15 A (Reviewing.) I'm sorry, repeat
16 the question, please.

17 Q Is it your opinion that a POSITA
18 looking at Figure 8 of Exhibit 2007,
19 would conclude that these waveforms
20 represent voltages applied on gate
21 terminals of these respective
22 transistors?

1 A Well, certainly the bit lines
2 don't go to gates. But that aside,
3 the -- in the absence of a careful review
4 of Yang to see if the specification gives
5 some indication to the contrary, but just
6 looking at 8B in isolation, a POSITA
7 would come to that conclusion, again,
8 seeking further confirmation from the
9 specification or the other figures.

10 Q And a POSITA would come to that
11 conclusion because of the smooth and
12 curved waveforms shown in Figure 8B,
13 correct?

14 A So this reference I talk about
15 on page 63 of my declaration, and in the
16 context of testimony of Dr. Liu about
17 this figure. I don't actually make draw
18 the conclusion that it is, in fact, at
19 the gates that these -- of the memory
20 cells that these figures -- that these
21 waveforms are shown. But it is
22 referenced to highlight Dr. Liu's

1 testimony that there are parasitics and
2 there are delays.

3 So whether or not these are
4 actually at the gates of memory cells or
5 just somewhere along the line is
6 irrelevant. Dr. Liu was acknowledging
7 that there are parasitic components, RC
8 components that cause some ramping of the
9 signal waveforms, be they at the gates or
10 not quite at the gates, somewhere along
11 the line.

12 Q But would you agree that by
13 applying the same logic and reasoning
14 that you determined Suzuki Figure 11
15 could disclose gate voltages, one would
16 reach the same conclusion with respect to
17 Figure 8B of Yang because they both
18 comprise smooth and curved waveforms?

19 ABED BALBAKY: Objection to
20 form.

21 THE WITNESS: As I already
22 answered, looking at 8B in

1 isolation, a POSITA might come to
2 that conclusion, but would search
3 the rest of the disclosure and the
4 other figures to corroborate that
5 initial assessment.

6 BY JOHANNES HSU:

7 Q Let's turn back to the patent
8 '957 patent.

9 A Are we done with Yang?

10 Q Yes.

11 A Okay.

12 Q Let's turn to Figure 6 of the
13 '957 patent.

14 A I am looking at Figure 6.

15 Q Are the voltages in Figure 6
16 gate voltages or word line voltages?

17 ABED BALBAKY: Objection to
18 form.

19 THE WITNESS: (Reviewing.)

20 As we noted previously, the '957
21 discloses that Figure 6 has a long
22 pre-pulse and that although it's

1 not shown, that the voltages at
2 the memory cells will have reached
3 their target voltages by the end
4 of the pre-pulse period.

5 However, Figure 6 does not
6 show that transition between the
7 quiescent level and the target
8 level, it only shows the target
9 level. So to the extent that it
10 is not showing actual gate
11 voltages on the memory cells
12 because it's showing the piecewise
13 linear target voltages, the
14 presumption is that a POSITA would
15 not recognize these as gate
16 voltages.

17 BY JOHANNES HSU:

18 Q Let's turn to Figure 7.

19 Are the voltages in Figure 7
20 gate voltages or word line voltages?

21 ABED BALBAKY: Objection to
22 form.

1 THE WITNESS: So it discloses
2 in Column 13 that Figure 7 is in
3 the short pre-pulse time regime.
4 It does not attempt to show the
5 transitions as smooth voltage
6 lines that fail to reach their
7 quiescent or their target levels
8 within the pre-pulse period.

9 And so all together, those
10 factors would lead a POSITA to
11 believe that these are not gate
12 voltages as depicted in Figure 7.
13 But let me reiterate that my
14 analysis of all of these
15 embodiments has not taken center
16 stage in my declaration. I have
17 not opined on these, per se. And
18 they are outside the four corners
19 of my declaration.

20 BY JOHANNES HSU:

21 Q Would you agree, though, that
22 the -- your distinction between gate

1 voltages versus word line voltages is a
2 key argument in your declaration?

3 ABED BALBAKY: Objection to
4 form.

5 THE WITNESS: The distinction
6 between target voltages and actual
7 gate voltages is central to the
8 '957 patent. And to that extent,
9 it is central to the analysis of
10 the prior art and the validity of
11 this patent.

12 BY JOHANNES HSU:

13 Q Even though that distinction is
14 central to the validity of the patent,
15 you have not undertaken an analysis of
16 whether Figure 6 or Figure 7 shows gate
17 voltages or word line voltages; is that
18 correct?

19 ABED BALBAKY: Objection to
20 form. Objection, mischaracterizes
21 his testimony.

22 THE WITNESS: Again, what I

1 have said repeatedly today is that
2 these embodiments within the '957
3 are tangential, at best, to my
4 critique of the arguments in the
5 petition and Dr. Liu's
6 declaration.

7 I have not opined on what
8 these embodiments do or do not
9 show. I have used them on
10 occasion to help illustrate for
11 the board particular phenomena
12 that occur in 3D NAND Flash
13 devices and in the prior arts that
14 have been brought forward by
15 petitioners, but I have not spent
16 any significance amount of time
17 worrying about what these
18 embodiments show or not because I
19 have not been asked to. It's not
20 been relevant to my task.

21 BY JOHANNES HSU:

22 Q You recall that you testified

1 Figure 4 of the '957 patent shows
2 piecewise linear waveforms?

3 A Yes.

4 Q Do you recall that?

5 A I do.

6 Q Does Figure 6 of the '957 patent
7 show piecewise linear waveforms?

8 A Yes, it does. But again, I
9 reiterate that these embodiments of the
10 '957 are completely tangential to my task
11 here and my opinions in this matter.

12 Q Does Figure 7 of the '957 patent
13 show piecewise linear waveforms?

14 A Generally speaking, yes, it does
15 show piecewise linear waveforms.

16 But again, I will reiterate that
17 the embodiments of the '957 are
18 tangential to my analysis in this matter
19 and are not relevant to my critique of
20 the arguments in the petition or the
21 declaration of Dr. Liu.

22 Q And the piecewise linear

1 waveforms are in contrast with the smooth
2 curved waveforms of Figure 5, correct?

3 A Yes. Figure 5, per the
4 specification of the '957, is in a
5 different regime entirely and depicts the
6 waveforms differently as a result.

7 Again, these are tangential to
8 my opinions in this matter and not
9 relevant to my critique of the arguments
10 in the petition and Dr. Liu's
11 declaration.

12 Q When you say these are
13 tangential to your opinions, what exactly
14 are you referring to?

15 A Well, my opinions in this matter
16 are those that are outlined at the
17 initial pages of my declaration and which
18 are expanded in more detail throughout.
19 None of them relate specifically to any
20 of the embodiments of the '957.

21 Q Let's turn to paragraph 90 of
22 your declaration.

1 A I am at 90.

2 Q In paragraph 90 and on page 58,
3 you discuss the '957 patent
4 "differentiates between voltages applied
5 to word line layers in a pre-pulse stage,
6 and the resulting bias voltages that are
7 applied to gate terminals of the
8 corresponding memory cells, which develop
9 over time as a result."

10 Do you see that?

11 A Yes.

12 Q And then you go on to say, For
13 example, as shown in Figure 5 of the '957
14 patent, when a short pre-pulse time is
15 used, the bias voltages that are applied
16 may not have sufficient time to develop
17 fully -- and I will skip the rest of
18 it -- but then you go on to include an
19 annotated version of Figure 5 with
20 annotation on the curved portions of one
21 of waveforms, correct?

22 A Yes. And as I have noted over

1 and over again today, these differences
2 between the figures of the '957 help the
3 POSITA understand what it is teaching,
4 but -- and so I am including these
5 citations and figures to help the board
6 understand as well.

7 Q But you testified a moment ago
8 that none of your opinions relate
9 specifically to any of the embodiments at
10 the '957; did you not?

11 ABED BALBAKY: Objection to
12 form.

13 THE WITNESS: What I tried to
14 convey to you a moment ago was
15 that the -- my formal opinions in
16 this matter don't specifically
17 relate to embodiments of the '957.
18 The embodiments are used in this
19 discussion of my opinions, to help
20 clarify for the board what is
21 going on in these references in
22 contrast to what is being

1 described in the '957.

2 Those are my opinions in this
3 matter, not whether or not, you
4 know, Figure 5 or Figure 6 depicts
5 something in particular or not.

6 We have been going for an
7 hour again. Do you want to pause?

8 JOHANNES HSU: If you would
9 hang in there, I think we are
10 almost done.

11 THE WITNESS: Okay. We will
12 hang in.

13 JOHANNES HSU: Okay.
14 Appreciate it.

15 BY JOHANNES HSU:

16 Q So are you saying your opinion
17 -- strike that.

18 Are you saying that what is
19 depicted in Figure 5, is tangential to
20 your opinion as stated in your
21 declaration?

22 ABED BALBAKY: Objection to

1 form.

2 THE WITNESS: So your
3 previous question, you
4 specifically were referring to my
5 paragraph 90 and what I say in
6 that. That paragraph is an
7 explanation of my opinion, which
8 is that, Hongtao in view of Yu,
9 does not disclose or render
10 obvious the application of a first
11 voltage and a second voltage on
12 the gate terminal of a non-program
13 memory cell, et cetera.

14 I am illustrating my opinion
15 to that effect by exploring for
16 the board how it's depicted within
17 the '957, but the opinion is about
18 Hongtao in light of Yu.

19 BY JOHANNES HSU:

20 Q I will quote your earlier
21 testimony, Doctor.

22 You stated, quote, "I will

1 reiterate that the embodiments of the
2 '957 are tangential to my analysis in
3 this matter and are not relevant to my
4 critique of the arguments in the petition
5 or the declaration of Dr. Liu end quote.

6 ABED BALBAKY: Objection.

7 BY JOHANNES HSU:

8 Q Does that include -- does that
9 include the embodiments as shown in
10 Figure 5?

11 A As I just indicated, my opinion
12 with regard to paragraph 90 and the
13 surrounding discussion, is in support of
14 my opinion that Hongtao, in view of Yu,
15 does not render obvious limitations 1B
16 and 1D.

17 I include discussion of Figure 5
18 and other portions of the '957, in order
19 to help the board understand the basis
20 for my opinion. It is not my opinion,
21 per se.

22 Q You are not answering the

1 question. So let's try again.

2 Your earlier testimony was, "the
3 embodiments of the '957 are tangential to
4 my analysis in this matter, and are not
5 relevant to my critique of the arguments
6 in the petition in the declaration of Dr.
7 Liu."

8 Are you with me so far?

9 A So far.

10 Q Okay.

11 The question is, is the
12 embodiment of Figure 5 tangential to your
13 analysis in this matter and is not
14 relevant to your critique of the
15 arguments in the petition or the
16 declaration of Dr. Liu?

17 A I believe that my analysis of
18 Hongtao, in view of Yu, is essentially
19 about the disclosure in those references
20 that I have shown Figure 5 annotated, or
21 described portions of the '957 patent, is
22 tangential to my critique of Hongtao in

1 view of Yu and is presented here in the
2 same section to help the board understand
3 my reasoning with regard to Hongtao in
4 view of Yu.

5 That is --

6 (Simultaneous Crosstalk.)

7 Q Let's --

8 A That is what I mean by
9 tangential.

10 Q Let's turn to Hongtao Figure 2.

11 You have Figure 2 in front of
12 you?

13 A I am scrolling to it. Wait.
14 That's Hongtao. Where is 2?

15 Q Page 10 in the copy I am looking
16 at.

17 A Sorry, yes. It was stuck in the
18 provisional and untranslated copy of it.

19 Here. I am at 2.

20 Q Does Figure 2 of Hongtao show
21 piecewise linear waveform?

22 A Yes, a POSITA would recognize

1 these waveforms as piecewise linear.

2 Q Does Figure 2 of Hongtao show
3 curved and smooth waveforms?

4 A POSITA would not see any smooth
5 and -- waveforms in Hongtao Figure 2.

6 Q Okay.

7 JOHANNES HSU: We can break
8 for 10 minutes off the record.

9 THE WITNESS: Okay.

10 (Whereupon a Recess Commenced
11 at 6:18 p.m. and Testimony
12 Recommenced at 6:26 p.m. EDT.)

13 JOHANNES HSU: Back on the
14 record. Barring any re-cross, I
15 have no further questions.

16 ABED BALBAKY: I have a few
17 quick questions.

18

19 EXAMINATION

20 BY ABED BALBAKY:

21 Q So to start Dr. Przybylski, did
22 you render any opinions regarding the

1 level of skill that a POSITA would have?

2 JOHANNES HSU: Objection.

3 That was not part of the -- part
4 of my questioning. Out of scope.

5 BY ABED BALBAKY:

6 Q Let me rephrase then.

7 Dr. Przybylski, could you please
8 look at your CV on page 113 of your
9 declaration.

10 A I am looking at it.

11 Q Is it correct to say that you
12 spent -- working from most recently, from
13 2003 to present, you were the president
14 of Verdande Group?

15 A Yes.

16 Q And from 2000 to 2003, you were
17 manager of the SSM Technologies LLC?

18 A Yes, I was.

19 Q And from 1991 to 2000, president
20 and principal consultant of Verdande
21 Group, Incorporated?

22 A Yes.

1 Q Is it fair to say that during
2 your work in those time ranges, that you
3 had experience either researching,
4 designing, or teaching about NAND memory
5 devices, including issues relating to the
6 operations, for example, the programming
7 of those devices?

8 A Yes. I've spent significant
9 amount of time researching, teaching
10 about NAND devices, specifically in the
11 latter of those present -- those time
12 periods that you talked about. So
13 unequivocally, yes.

14 Q Could you give an approximate
15 number of years of experience that you
16 have researching, designing, and teaching
17 about NAND memory devices, including
18 their operations?

19 A Well, certainly the -- in the
20 2003 to present timeframe, where at the
21 beginning of that timeframe the
22 non-volatile memories were transitioning

1 from the predecessor technologies to NAND
2 technology -- NAND Flash technologies, I
3 was following and researching and talking
4 with people throughout that period about
5 those memory devices.

6 In particular, I went with
7 Johannes a couple of specific engagements
8 where I was significantly involved for
9 many years on a near full-time level
10 designing NAND Flash memories and their
11 memory systems.

12 Q Thank you.

13 If you could turn to pages 21
14 and 22 of your declaration.

15 Do you recall Johannes asking
16 you any questions about the annotated
17 copy of Figure 6 and the content of
18 paragraph 37?

19 A Yes.

20 Q So do you recall -- do you
21 recall providing testimony regarding
22 whether or not the waveforms illustrated

1 in Figure 6 are target voltages as
2 compared to actual gate voltages?

3 A I believe I testified that these
4 are target voltages in Figure 6, not
5 actual gate voltages.

6 Q Do you recall testifying about
7 Figure 6 using long pre-pulse periods?

8 A Yes. We spent significant
9 amount of time looking at different
10 embodiments of the '957 and
11 characterizing each, per the disclosure
12 of the '957 as having either long or
13 short pre-conduction periods.

14 Q And what is the significance of
15 using a long pre-pulse time or long
16 pre-pulse period?

17 A Well, in a long pre-pulse
18 period, the voltages at the memory cells
19 have time to reach their target voltages
20 or indistinguishably dissimilar from
21 them.

22 And so the transition to the

1 next phase of the operation is
2 straightforward because you have fully
3 covered any RC time-constant delays
4 associated with the electrical and
5 physical characteristics of the NAND
6 Flash memory device.

7 Q Absent some explanation that a
8 given device is using long pre-pulse
9 periods, would you assume by default that
10 any given device uses long pre-pulse
11 periods?

12 A I think I got the sense of that
13 backwards.

14 Can you repeat it for me,
15 please.

16 Q Sure. Let me rephrase slightly.
17 Absent some explicit description
18 that a given device is using long
19 pre-pulse periods, would you assume that
20 any device uses long pre-pulse periods?

21 A No, I would not assume that. My
22 inclination would be to assume short

1 pre-pulse periods because those are going
2 to be shorter, and that if there is no
3 disclosure or reason given for a long
4 pre-pulse period, the inclination would
5 be to figure out how to do a short
6 pre-pulse period.

7 ABED BALBAKY: Thank you
8 that's all.

9
10 FURTHER EXAMINATION

11 BY JOHANNES HSU:

12 Q Doctor, just quickly.

13 You agree that the '957 patent
14 discloses long pre-pulse periods in
15 Figures 6 and 8, correct?

16 A If I recall our discussion
17 earlier, we were relying on the 957's
18 explicit disclosure of those facts.

19 Q And you also testified that the
20 claims of the '957 patent is not limited
21 to a short pre-verify stage, correct?

22 A I believe what I testified to

1 was that the claims don't include the
2 words long or short.

3 Q As a POSITA, would you
4 understand the claims of the '957 patent
5 to be not limited to a short pre-verify
6 stage?

7 A I don't think I rendered an
8 opinion as to whether a POSITA would
9 understand that to be part of the scope
10 of the '957 claims. I don't recall
11 having testified to that in my
12 declaration one way or the other.

13 Q It is your opinion that the
14 claims of the '957 patent does not
15 mention a time scale and that the claims
16 speak for themselves, correct?

17 A I believe our testimony earlier
18 was that the claims do not include
19 specific time scales. I remember that
20 testimony.

21 JOHANNES HSU: I have no
22 further questions.

1 ABED BALBAKY: Nothing for

2 me.

3 THE WITNESS: Okay.

4 (Whereupon a Discussion is Held Off the
5 Record.)

6 (Whereupon Testimony Concluded at 6:38 p.m.
7 EDT.)

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ACKNOWLEDGEMENT

STATE OF _____

COUNTY OF _____

I, the undersigned, hereby
certify that I have read the transcript
of my testimony taken under oath in my
deposition; that the transcript is a true
and complete and correct record of my
testimony, and that the answers on the
record as given by me are true and
correct.

STEVEN PRZYBYLSKI, PhD

Signed and subscribed to before
me this _____ day of _____,
20__.

Notary Public

1 I, S. Arielle Santos, CSR, CLR, do
2 hereby certify:
3 That prior to being examined, the witness named
4 in the forgoing deposition, was by me duly
5 affirmed remotely under order SC of FL No.
6 AOSC20-23 Amendment 4 (II)(C)(2) to testify the
7 truth, the whole truth, and nothing but the
8 truth.
9 That said deposition was taken before me at the
10 time and place set forth and was taken down by
11 me in shorthand and thereafter reduced to
12 computerized transcription under my direction
13 and supervision, and I hereby certify the
14 foregoing deposition is a full, true and correct
15 transcript of my shorthand notes so taken.
16 I further certify that I am neither counsel for
17 nor related to any party to said action nor in
18 anywise interested in the outcome thereof.

19



20

21 S. Arielle Santos, CSR

22 Notary No. HH 192604 Exp 10/31/2025