

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,

Petitioner,

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,

Patent Owner.

Case IPR2024-00792
Patent 11,468,957

PATENT OWNER'S SUR-REPLY

TABLE OF CONTENTS

I. INTRODUCTION	1
II. CLAIM CONSTRUCTION	1
III. GROUND 1: PETITIONER’S NEW ARGUMENTS FAIL TO SHOW THAT HONGTAO IN VIEW OF LIU RENDERS OBVIOUS THE CHALLENGED CLAIMS	7
A. Independent Claim: Hongtao in View of Yu Still Fails to Disclose or Render Obvious a “Pre-Verify Stage”	7
B. Independent Claim: Hongtao in View of Yu Still Fails to Disclose or Render Obvious Applying “a First Bias Voltage” and “a Second Bias Voltage” on the Gate Terminal of a Not Programmed Memory Cell “Wherein the Second Bias Voltage Is Smaller than the First Bias Voltage”	11
C. Claims 5 and 6: Hongtao in View of Yu Still Fails to Disclose or Render Obvious a “Top Bias Voltage” or “Bottom Bias Voltage” Applied “In the Pre-Verify Stage and the Verify Stage”	16
IV. GROUND 2: PETITIONER’S NEW ARGUMENTS FAIL TO SHOW THAT SUZUKI DISCLOSES CLAIMS 1-6	17
A. Independent Claim: Suzuki Does Not Disclose Applying a First Verify Voltage and First Bias Voltage in a “Pre-Verify” Stage, or Applying a Second Bias Voltage in a “Verify” Stage “Wherein the Second Bias Voltage Is Smaller than the First Bias Voltage”	17
B. Claims 5 and 6: Suzuki Still Does Not Disclose a “Top Bias Voltage” or “Bottom Bias Voltage” Applied “In the Pre-Verify Stage and the Verify Stage”	20
V. GROUND 3: PETITIONER’S NEW ARGUMENTS FAIL TO SHOW THAT COSTA IN VIEW OF SEO DISCLOSES OR RENDERS OBVIOUS CLAIMS 1-6	20
A. Independent Claim: Costa in View of Seo Still Does Not Disclose or Render Obvious a “Pre-Verify Stage”	20
B. Independent Claim: Costa in View of Seo Does Not Disclose or Render Obvious Applying “a First Bias Voltage” and “a Second Bias Voltage” on the Gate Terminal of a Not Programmed Memory Cell “Wherein the Second Bias Voltage Is Smaller than the First Bias Voltage”	21

VI. Dr. Przybylski’s Tesimony Further Confirms Petitioner’s Arguments	
Fail	25
VII. CONCLUSION.....	27

TABLE OF AUTHORITIES

Cases	Page(s)
<i>Finjan LLC v SonicWall, Inc.</i> , 84 F.4th 963 (Fed. Cir. 2023)	6
<i>Henny Penny Corp. v. Frymaster LLC</i> , 938 F.3d 1324 (Fed. Cir. 2019)	1
<i>Rolls-Royce, PLC v. United Techs. Corp.</i> , 603 F.3d 1325 (Fed. Cir. 2010)	24
Other Authorities	
37 C.F.R. § 42.23(b)	1

LIST OF EXHIBITS

Exhibit	Description
Ex. 2001	Micron 4-2 Claim Construction Disclosure
Ex. 2002	YMTC 4-2 Claim Construction Disclosure
Ex. 2003	Declaration of Steven Przybylski (“Przybylski”)
Ex. 2004	U.S. 2024/0295960 (“Li”)
Ex. 2005	U.S. 2023/0343398 (“Dong”)
Ex. 2006	Transcript of December 17, 2024 Deposition of Dr. Liu for IPR2024-00795 in Connection with Patent U.S. 11,501,822 (“Liu822 Tr.”)
Ex. 2007	U.S. 10,726,920 (“Yang”)
Ex. 2008-09	Reserved
Ex. 2010	Declaration of Jonathan Bradford
Ex. 2011	Transcript of May 28, 2025 Deposition of Dr. Liu for IPR2024-00792 in Connection with Patent U.S. 11,468,957 (“Liu957 Tr.”)

LIST OF ABBREVIATIONS

Abbreviation	Term
'957	U.S. Pat. No. 11,468,957
'957FH	File History of U.S. Pat. No. 11,468,957
Challenged Claims	'957, Claims 1-6
Liu	Declaration of Dr. Liu (Ex. 1003)
LiuII	Reply Declaration of Dr. Liu (Ex. 1027)
Hongtao	Chinese Pat. App. Pub. No. 109065091 (Ex. 1005)
Yu	U.S. Pat. No. 20190198117 (Ex. 1006)
Suzuki	U.S. Pat. No. 20210082505 (Ex. 1007)
Costa	U.S. Pat. No. 20180012667 (Ex. 1008)
Seo	U.S. Pat. No. 20210027848 (Ex. 1009)
Li	U.S. 2024/0295960 (Ex. 2004)
Dong	U.S. 2023/0343398 (Ex. 2005)
Liu822 Tr.	Transcript of December 17, 2024 Deposition of Dr. Liu for IPR2024-00795 in Connection with Patent U.S. 11,501,822 (Ex. 2006)
Liu957 Tr.	Transcript of May 28, 2025 Deposition of Dr. Liu for IPR2024-00792 in Connection with Patent U.S. 11,468,957 (Ex. 2011)
Yang	U.S. 10,726,920 (Ex. 2007)
Office	U.S. Patent and Trademark Office

Petition or Pet.	Petition for <i>Inter Partes</i> Review of U.S. Patent No. 11,468,957 (IPR2024-00792, Paper 1)
Parallel district court litigation	<i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc.</i> , NDCA-3-23-cv-05792 (N.D. Cal.)
Patent Owner, PO	Yangtze Memory Technologies Co. Ltd.
Petitioner	Micron Technology, Inc.
POSITA	Person of ordinary skill in the art
Przybylski	Declaration of Steven Przybylski
Reply	Petitioner’s Reply Brief (IPR2024-00792, Paper 20)

I. INTRODUCTION

Petitioner's Reply fails to engage with the Petition's deficiencies identified in the POR and instead resorts to conflating distinct concepts (*e.g.*, reading vs. verifying; target voltages vs. actual voltages) and introducing new arguments. The Board should disregard the Reply's attempts to broaden and alter the trial grounds as Petitioner needed to make its entire case in the Petition. 37 C.F.R. § 42.23(b); *Henny Penny Corp. v. Frymaster LLC*, 938 F.3d 1324, 1330-31 (Fed. Cir. 2019). In any event, Petitioner's new arguments fail to cure the problems in the Petition. Independent claim 1 and its dependent claims 5-6 (the "Challenged Claims") should be upheld as patentable.

II. CLAIM CONSTRUCTION

With respect to the claim term "apply a [top/bottom] bias voltage on a gate terminal of the [TSG/BSG] transistor of the first memory cell string in the pre-verify stage and the verify stage," the Petitioner incorrectly contends that claims 5-6 are met even when the bias voltage changes in value between the pre-verify stage and the verify stage. Pet. 61-64, 96-98. As discussed in the POR, the intrinsic record supports exactly the opposite—the same bias voltage must be applied in each of these two stages. POR 13-17. The plain meaning of applying "a ... bias voltage ... in the pre-verify stage and the verify stage," as recited in the claims, requires that the same voltage level be applied in both the pre-verify stage and the verify stage.

In addition, in the context of Fig. 4 (below), the specification explains that “a bias voltage (or [bottom/top] gate voltage), such as 5 volts” is applied to the **BSG** and selected **TSG** layers, respectively, during the “pre-pulse stage” (i.e., during the **pre-verify stage**) and “maintained” during the “verify/read” stage (i.e., during the **verify stage**). ’957, 10:57-11:15 (describing the pre-pulse stage), 11:16-57 (describing the verify/read stage), Fig. 4; Przybylski, ¶50.¹

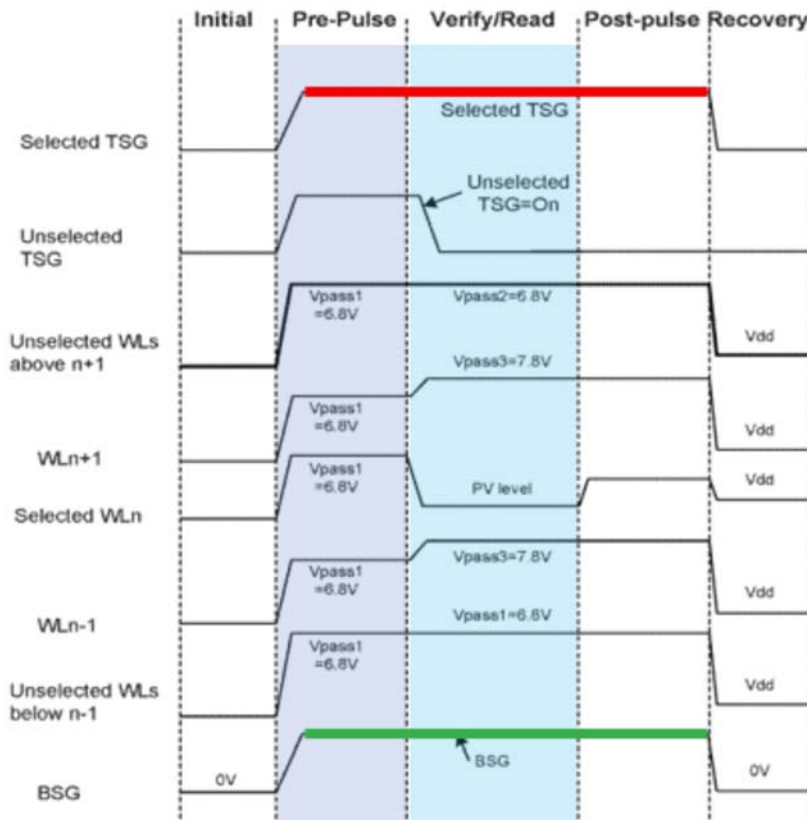


FIG. 4

¹ All emphasis and color annotations added unless otherwise noted.

The Reply does not point to any evidence, intrinsic or otherwise, that can rebut PO's claim construction position.

First, Petitioner argues that the claims refer to “a ... bias voltage” and are not limited to a “voltage level” (Reply 3), but PO's construction does not require a specific voltage level or value. Rather, the issue is whether the same voltage (whatever voltage that is) must be applied in both the pre-verify and verify stages. Moreover, PO's construction is not “rewrit[ing] the claims” (Reply 3)—the claims expressly require that “a ... bias voltage” (the same bias voltage) is applied in both stages. The claims do **not** recite, for example, a first bias voltage applied in the pre-verify stage and a second bias voltage applied in the verify stage, which would have supported Petitioner's interpretation.

Petitioner further argues that the specification supports its broader interpretation because it states that “the [top/bottom] bias voltage **can be** increased from the initial voltage to a target value (e.g., 5 volts) in the first portion of the pre-pulse stage” (Reply 3-4 (citing '957, 13:43-53)), but this statement is referring to voltage changes within a single stage,² and thus does not address whether the voltage stays the same between the two different stages. On that issue, the specification

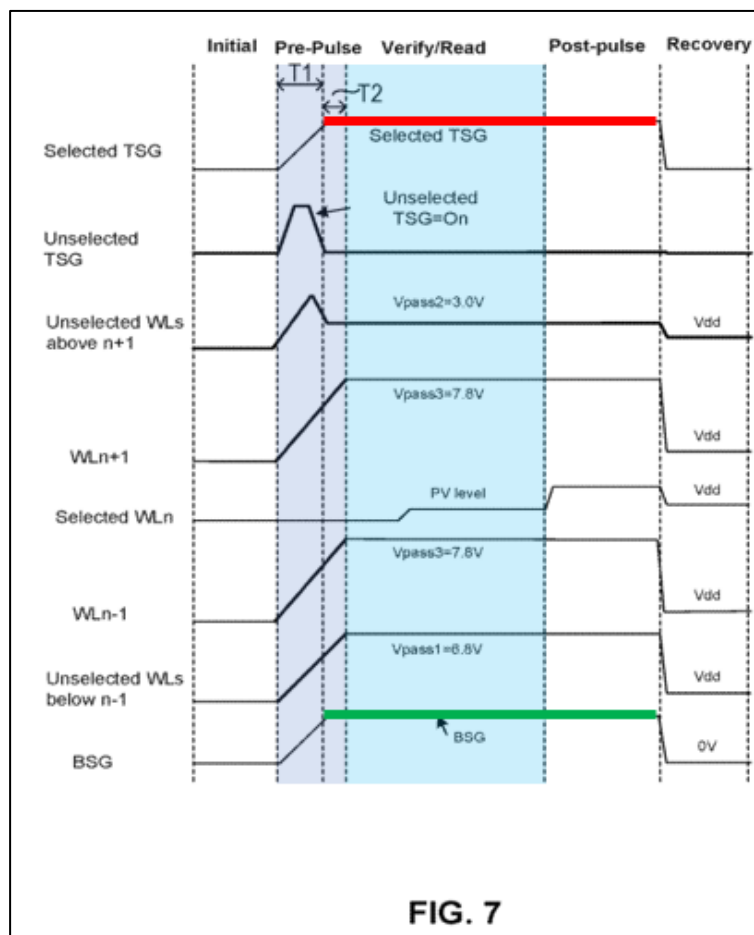
² PO's construction does not require that the claimed bias voltage be applied for the entire period within each stage.

supports PO's construction that the same voltage is applied in both stages. As explained in two sentences immediately following those relied on by Petitioner, "[t]he [top/bottom] bias voltage can be maintained through the second portion of the pre-verify stage and the verify stage." '957, 13:43-54; see also *id.* 2:56-61 ("the [bottom/top] bias voltage ... **is maintained** through the second portion of the pre-verify stage and the verify stage"), 4:4-9 (same).

Second, Petitioner argues that the claims must allow for changes in bias voltage across the two stages because the "positive voltage" recited in claim 5 does not reach a single voltage level until the verify stage in Figure 5 (Reply, 4-5), but again Petitioner ignores the specification disclosure of "maintain[ing]" the voltage in the verify and pre-verify stages. *See also* '957, 11:16-34, Fig. 6 (applying a positive voltage to BSG side transistors in the two stages), Fig. 8 (applying a positive voltage to TSG side transistors in the two stages). Moreover, while the scope of "a positive voltage" in claim 5 is a separate issue that the Board does not need to reach, the other '957 embodiments such those relating to Figures 4, 6, and 8 teach the same positive voltage applied to unselected word lines in both stages. '957, Figs. 4, 6, 8.

Third, Petitioner inexplicably refers to Fig. 7 as "PO's chosen claim-construction embodiment," and argues that because time is needed for actual gate voltages to reach an applied target value, it is impossible for the "positive voltage" purportedly illustrated in Fig. 7 to have a single value in both the pre-verify stage

and verify stages. Reply 5-6. To be clear, it was the Petition that first pointed to Fig. 7 as somehow illustrating the claimed “positive voltage” of limitation [5.C] as having multiple voltage levels. See Pet. 7, 67. The POR never took a position on the construction of the term “a positive voltage,” or whether Fig. 7 specifically illustrates claims 5 and 6. The only reason the POR cited Fig. 7 was to identify that the top/bottom bias voltages illustrated are—contrary to Petitioner’s assertion—maintained at a single voltage level in both the pre-verify and verify stages. POR 16; Przybylski, ¶52.



'957, Fig. 7. And contrary to Petitioner's position that the bias voltage cannot rise to its target level until after the pre-verify stage (Reply 5-6), the '957 explains that a "long" pre-pulse time is used such that the gate voltages fully develop to their target values, and that "the bias voltages applied in the pre-pulse stage can be full developed to (or completely reach) target values in FIG. 7." See '957, 12:28-42 (describing Fig. 6), 13:13-15 (describing Fig. 7).

Last, Petitioner abandons its previous position that "'a' can mean more than one" and thus the claimed "a ... bias voltage" can have many values. See Pet. 62. As explained in the POR, "the indefinite article a means one or more But that is a separate issue from whether the claims require the same component to perform multiple functions or satisfy multiple limitations of a claim." *Finjan LLC v SonicWall, Inc.*, 84 F.4th 963, 974-975 (Fed. Cir. 2023); POR 46-47. The Reply seemingly concedes that a single "bias voltage" must be applied in both the pre-verify and the verify stages (arguing instead that the single "voltage may change"), abandoning the Petition argument that the term "a bias voltage" standing alone would permit different voltages to be used in the pre-verify and verify stages. As explained in the POR, consistent with the plain and ordinary meaning and the intrinsic record, the term requires the same voltage be applied in both stages. POR 13-16; Przybylski ¶¶48-53.

III. GROUND 1: PETITIONER’S NEW ARGUMENTS FAIL TO SHOW THAT HONGTAO IN VIEW OF LIU RENDERS OBVIOUS THE CHALLENGED CLAIMS

A. Independent Claim: Hongtao in View of Yu Still Fails to Disclose or Render Obvious a “Pre-Verify Stage”

The Reply fails to address the deficiencies in the Petition. As explained in the POR, Hongtao and Yu fail to disclose or render obvious any type of multi-stage verification operation as required by the Claims. *See* POR 27-32. Hongtao is explicitly directed to a “reading method” for 3D NAND. Hongtao, Abstract. To the extent that the “reading method” has separate pre-conduction and reading phases, Hongtao does not teach or suggest applying those teachings to create a verification operation with distinct “pre-verify” and “verify” stages. Hongtao, [0005]-[0007]. Przybylski, ¶78. Yu also fails to disclose any type of two-stage operation in its verification operation—there is no separate pre-verify stage and verify stage. POR 29-30.

Nor did the Petition show that a POSITA would have been motivated to apply Hongtao’s teachings regarding **read** operations to Yu to create a two-stage **verification** operation. Petitioner incorrectly conflates “verifying” and “reading,” but these are distinct operations, and the art is replete with examples of those two operations using distinct voltages and biasing schemes. *See* POR 30-32 (summarizing examples). One key difference is that verification operations use distinct bias voltages for unselected word lines on programmed and unprogrammed

memory as part of a programming loop, whereas reading operations use the same voltage for all unselected word lines. *Id.* Indeed, Yu itself confirms this distinction. Specifically, for its programming loop, Yu teaches using “a first pass voltage VPASS1” for the sub-block of unselected word line with programmed memory cells, and using “a second voltage VPASS2 lower than the first pass voltage VPASS1” for the sub-block containing “memory cells ... in the erased state.” Yu, [0121]-[0122], Figs. 11-12. By comparison, Hongtao is concerned with reading operations, which involve applying the same set of voltages to all unselected word lines. *See, e.g.*, Hongtao, Fig. 2, [0025] (in the reading phase, “the unselected memory cells on the selected string are applied with a **conduction voltage** through the unselected word lines”); POR 19.

Petitioner’s Reply arguments do not cure these flaws.

First, the Reply incorrectly asserts that the operations are “virtually identical” (Reply 23-25), whereas the ’957 uses the terms “read,” “verify,” and “verify/read” at different times to refer to these distinct concepts. For example, as noted in the POR, the ’957 uses the term “verify/read” to describe the later sensing portion of the verify operation when a “program verify level” is used to determine the state of the selected memory cell. POR 30 n.3; ’957 Fig. 4, 11:35-57. Przybylski, ¶83. Thus, it is clear from context that the operation being described as a “verify/read” operation

is for verifying that a recently programmed memory cell was programmed correctly, and is separate from a reading operation. *See* Przybylski, ¶83.

The Reply effectively asks the Board to ignore the distinctions between reading and verifying operations—as exemplified by verifying operations using lower bias voltages on unprogrammed memory cells—by downplaying these unique features as “optional” capabilities. Reply, 25. But Yu’s system is restricted in this very way—using disparate bias voltages on programmed and unprogrammed memory cells during a program loop (i.e., when programming and verifying memory cells)—making it incompatible with the biasing schemes for generic “reading” operations like Hongtao that use the same voltage on all the unselected memory cells. *See*, Yu, [0121]-[0122], Figs. 11-12; Hongtao, Fig. 2, [0025]; POR 30-31.

As noted in the POR, the Petition does not address any of the differences between how “verify” and “read” operations are performed, and failed to provide any arguments or evidence beyond conclusory assertions to show why Hongtao’s disclosures could be applied to Yu’s verify operations. *See* POR 30-31. Instead of addressing these deficiencies, the Reply mistakenly argues that some verification operations (like Suzuki’s) can use a single set of voltages on unselected word lines, and that the ’957 claims do not recite different voltages for biasing programmed and unprogrammed word lines. Reply 25. But those arguments again miss the point. How Suzuki uniquely operates (or what the ’957 recites in the claims) has no bearing on

whether a POSITA would have been motivated to apply Hongtao's teachings regarding reading operations to the verification operations within Yu's programming loop.

Second, even assuming Hongtao and Yu could be combined in the manner suggested in the Petition, the Reply incorrectly argues that Hongtao's pre-conduction phase would be equivalent to a pre-verify operation. Reply 26. As recognized by the Decision to Institute ("DI") in the context of Ground 3, a read operation divided into two time periods does not equate to a "pre-verify stage" and "verify stage." DI, 26-27 (the reference "only describes time periods t1 and t2 with respect to performing a read operation ... it is not clear that time period t1 is a 'pre-verify stage' as claimed"). As noted in the POR, reading and verifying are distinct operations. POR 30-32. Even assuming Hongtao and Yu could be combined as the Petition suggests, Hongtao's disclosure of "preparing" for a reading operation does not equate to the "pre-verify" portion of a two-stage verification. Moreover, Dr. Liu's conclusory assertion that the "pre-conduction voltage" serves the same purpose as a "verify" voltage appears to be based on the fact that it "prepare[s] for the read" and "turns on the channel." See Liu ¶105. But once again, reading and verifying are distinct operations, and the similarities between Hongtao's "pre-conduction" voltage and the claimed "pre-verify" voltage are superficial at best.

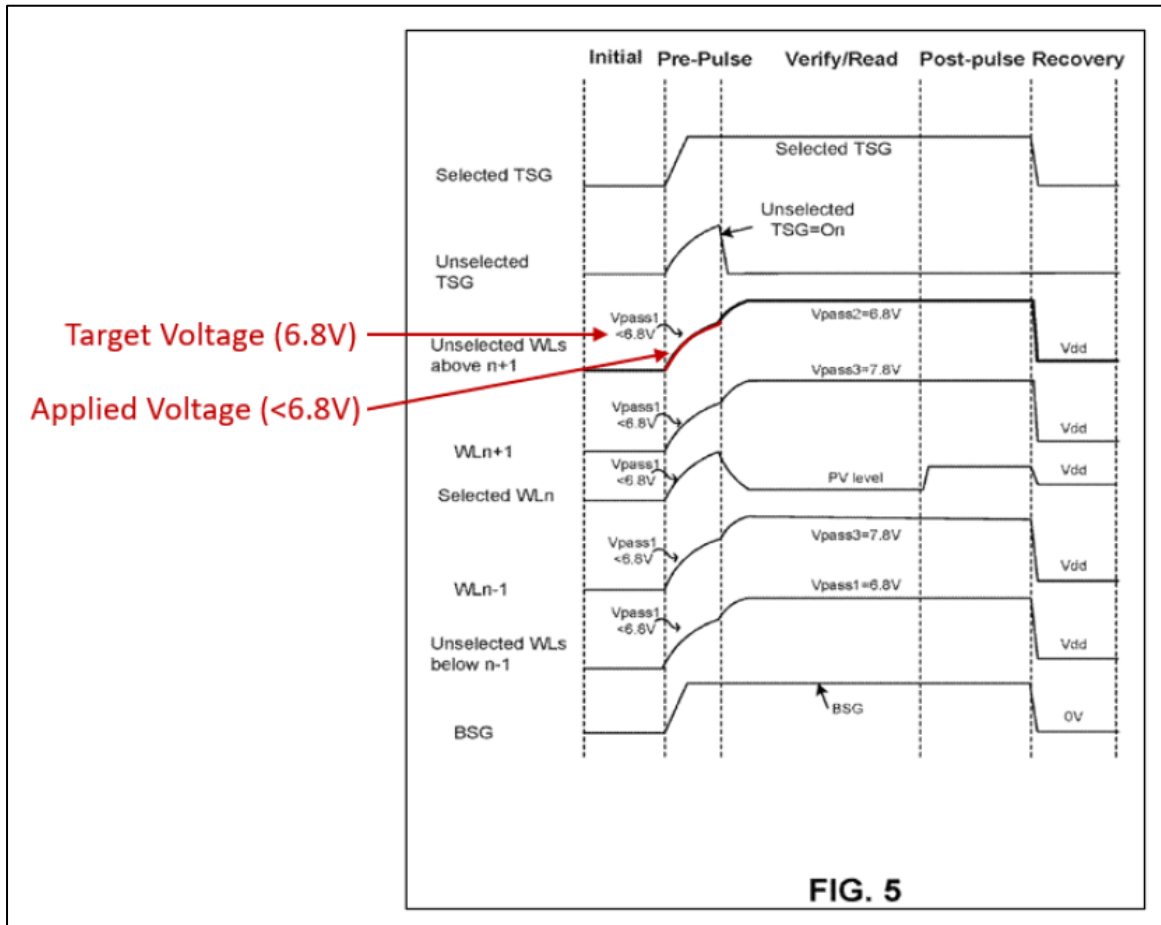
Accordingly, even in view of the new Reply arguments, Hongtao in view of Yu fails to disclose or render obvious applying bias verify voltages during a “pre-verify stage” as required by the Challenged Claims.

B. Independent Claim: Hongtao in View of Yu Still Fails to Disclose or Render Obvious Applying “a First Bias Voltage” and “a Second Bias Voltage” on the Gate Terminal of a Not Programmed Memory Cell “Wherein the Second Bias Voltage Is Smaller than the First Bias Voltage”

The Reply does not address the deficiencies in the Petition, and fails to show that Hongtao in view of Yu discloses applying bias voltages on the gate terminal of a memory cell “wherein the second bias voltage is smaller than the first bias voltage.”

As a preliminary matter, the Reply repeatedly mischaracterizes the POR as merely arguing that Hongtao shows “voltages on word lines rather than on gates,” and raises arguments to attack that constructed straw man. *See* Reply 7-8, *citing* POR 32-44. The POR arguments are not based solely on the distinction between word-lines voltages and gate voltages. Rather, as explained in the POR, Fig. 2 of Hongtao, on which the Petition relies, depicts **target** values for the word lines voltages (i.e., the piecewise linear function used to control a voltage generation circuit) rather than the **resulting** voltages that develop on the gate terminals of the memory cells. POR 34-40. The ’957 distinguishes “**target**” voltages and the actual voltages that are “**developed**” over time as a result. POR 33-34; Przybylski ¶90; ’957, 12:18-19. Fig.

5 illustrates this phenomenon during the pre-pulse period for the selected word line and unselected word lines.



The Reply mistakenly conflates the term “**target voltage**” with “**wordline voltage**,” but the two are distinct. As explained by Dr. Przybylski, “[d]rivers, or similar voltage generation circuits, **force the word lines to achieve specific target voltages over time**,” resulting in distorted voltages that are delayed relative to the target values applied to the word line drivers. See POR 36-38; Przybylski ¶¶93-95. Indeed, both the literature and Micron’s own expert recognize that there is a delay when applying voltages to word lines, and that any real voltage (e.g., as distinct from

some type of abstract target voltage) will have an RC-time constant and appear with smooth lines rather than a piecewise linear function. *See* POR 36-38 (*citing* Aritome, 350-353); *see also* Liu822 Tr. 63:22-63:3.

The Reply raises several arguments attacking a mischaracterized version of the POR arguments, but fails to address the deficiencies in Hongtao or otherwise establish that Hongtao illustrates anything other than target voltages.

First, Petitioner cites several examples to suggest that the terms “word line voltage” and “gate voltage” are used interchangeably in both the ’957 patent and the prior art (Reply 9-16), but this argument does not address the issues raised in the POR. The deficiency in Hongtao is not that it is describing “word line voltages,” but that Fig. 2 depicts **target values** for the word lines voltages (i.e., the piecewise linear function used to control a voltage generation circuit) rather than the resulting voltages that develop on the gate terminals of the memory cells.

Second, Petitioner again misses the point in discussing whether a curved waveform indicates a “gate voltage” or a “word line voltage.” *See* Reply 17-20. The importance of the curvature is not that it differentiates “word line voltages” and “gate voltages,” but that it distinguishes idealized “target” voltages from the actual voltages that develop over time. “Target” voltages are illustrated with straight lines and actual voltages are illustrated with curved lines. *See* POR 5-10, 33-34; Przybylski ¶94. As the ’957 specification explains, a “long” pre-pulse time is used

such that the gate voltages fully develop to their target values—such that the first bias voltage at the gate is actually larger than the second bias voltage as claimed. See POR 8-9; '957, 12:28-42; *see also id.* 11:48-12:9, 13:13-17 (“Compared to the verify/read operation in FIG. 5, the bias voltages applied in the pre-pulse stage can be full developed to (or completely reach) target values in FIG. 7” such that “the bias voltage ... can be fully developed in the pre-pulse stage.”). Petitioner’s assertion that, under PO’s argument, there is not a single '957 embodiment that satisfies the claims (Reply 18) ignores these disclosures.³

Third, Petitioner newly raises arguments about how big or small a delay might be (Reply 20-23), but again misses the point that the Petition never addressed what the actual voltage experienced at the gate would be in Hongtao. Petitioner does not cure this deficiency in the Reply either. Instead, it attempts to flip the burden onto PO to identify the time constant, while recognizing that the voltage might “overshoot,” “undershoot,” or “reach” the target. Reply 23. And that is the essence

³ Petitioner’s argument that the '957 figures are internally inconsistent (Reply 18-19) is similarly misplaced—the '957 depicts actual voltages when particularly relevant to a problem it is illustrating (e.g., to show when voltages in Figure 5 do not have sufficient time to develop ('957, 12:15-21)) and the specification further describes what is happening as discussed above.

of the problem—Petitioner failed to show which of these happens in Hongtao. Petitioner’s further argument that Hongtao is presumed enabling is of no moment. Hongtao is silent and not dependent on whether the actual voltage at the gate is higher in the pre-conduction phase than the voltage in the reading stage—again demonstrating that Petitioner failed to provide any evidence of how these “actual” voltages in Hongtao would develop over time.

Finally, Petitioner again incorrectly argues that Hongtao [0026] suggests that Fig. 2 uses disparate bias voltages on unselected word lines in the pre-conduction and reading phases. Reply 8. As explained in the POR, Hongtao says no such thing, and Paragraph [0026] instead describes **problems** in the embodiment of Fig. 2, which are addressed in the further embodiment of Fig. 3. POR 40-43. Moreover, as further explained in the POR, both Figs. 2 and 3 depict the exact same waveform depicting the same target voltage rather than resulting voltage, and therefore both embodiments fail to disclose the claimed voltage relationship. The Reply argues that Hongtao [0026] teaches the “general principle” of reducing “conduction voltage – driving voltage” (i.e., the difference between the voltages). Reply, 8. Even assuming, *arguendo*, that Hongtao describes a “general principle” of reducing “conduction voltage – driving voltage,” that says nothing about the relative magnitude of the voltages applied during **different time periods**. It does not teach or suggest that the pre-conduction voltage applied in a pre-conduction phase should differ from the

conduction voltage applied in the subsequent reading phase, or otherwise address the deficiencies in Hongtao.

In short, the Reply arguments fail to address the deficiencies in the Petition or the arguments raised in the POR, and the Petition grounds still fail to disclose or otherwise render obvious processing circuitry configured to apply first and second bias voltages on the gate terminal of a memory cell “wherein the second bias voltage is smaller than the first bias voltage” as required by the Challenged Claims.

C. Claims 5 and 6: Hongtao in View of Yu Still Fails to Disclose or Render Obvious a “Top Bias Voltage” or “Bottom Bias Voltage” Applied “In the Pre-Verify Stage and the Verify Stage”

Hongtao in view of Yu does not disclose or render obvious dependent claims 5 and 6. POR 44-48. Petitioner’s Reply does not present any additional arguments for claims 5 and 6, other than emphasizing their incorrect claim construction. Reply, 26. As discussed in Section 0, the intrinsic record supports PO’s position, consistent with the plain and ordinary meaning of the claims, that the recited top/bottom “bias voltage ... [applied] in the pre-verify stage and the verify stage” requires a single value be applied in both stages. By comparison, Petitioner’s argument that applying a “[bottom/top] bias voltage ... in the pre-verify stage and the verify stage” is satisfied even when wholly disparate voltages are applied in each stage is improper, and effectively reads out the claim limitations. Pet. 62-63. For at least these reasons, Petitioner fails to show claims 5-6 are unpatentable.

IV. GROUND 2: PETITIONER’S NEW ARGUMENTS FAIL TO SHOW THAT SUZUKI DISCLOSES CLAIMS 1-6

A. Independent Claim: Suzuki Does Not Disclose Applying a First Verify Voltage and First Bias Voltage in a “Pre-Verify” Stage, or Applying a Second Bias Voltage in a “Verify” Stage “Wherein the Second Bias Voltage Is Smaller than the First Bias Voltage”

Petitioner relies on Suzuki’s VPASS voltage during the recovery operation as the purported first bias voltage (Pet. 74-85), but the voltage is not applied during a “pre-verify stage” as required by the Claims. Instead, as illustrated in Fig. 11 below, VPASS is applied during t3-t4, which is an **end operation of the program operation**, and distinct from the period from t5-t6 with distinct voltages that acts as a **ready operation of the verify operation**, and a period from t4-t5, which is a **transition period** between the two. See Suzuki, [0131]. The three collectively constitute the “Recovery operation” as shown below:

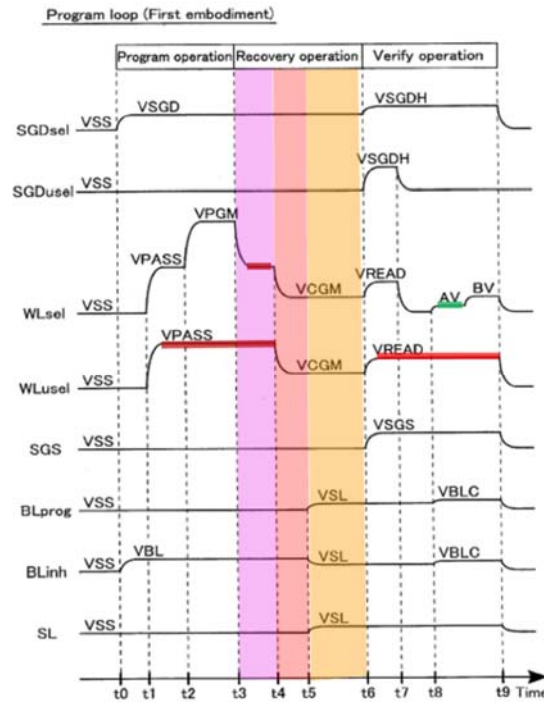


FIG. 11

The period starting at t5 (i.e., a **ready operation of the verify operation**) is when voltages are applied in anticipation of the verify operation starting at t6. Suzuki, [0139]. The Reply does not address this deficiency. Instead, the Reply presents a series of new, flawed, arguments that only further illustrate that Petitioner has not met its burden.

First, the Reply incorrectly asserts that programming “terminates” at the beginning of t3 (i.e., before the “recovery operation” begins). Reply 26. As a preliminary matter, the end of programming does not inherently demarcate the start of a “pre-verify” stage. Regardless, Petitioner’s assertion ignores Suzuki’s explicit statement that the Recovery Operation includes an “end operation of the program

operation,” which extends beyond time t_3 to include the period t_3 - t_4 as the voltages begin to ramp down. *See* POR 51; Suzuki [131].

Second, the Reply misinterprets Suzuki as disclosing that the period t_3 - t_4 is a pre-verify stage because it is purportedly used to “self-boost” the channel voltage and “pull[] out” electrons in preparation for verification. Reply 37, citing Suzuki [0134]-[0135], [0140]. Suzuki says no such thing regarding t_3 - t_4 . Rather, while Suzuki [0134]-[0135] describes applying VPASS to “self-boost,” this boost operation is described only in the discussion of the time periods from t_1 - t_3 (indisputably the **programming** stage). If anything, this further confirms that t_3 - t_4 is part of the programming operation, not a pre-verify operation, because VPASS is still applied. And while Suzuki [0140] describes a process that causes electrons to be “pulled out to the bit lines,” this is during the period t_5 - t_6 , which is a ready operation but does not have a voltage that satisfies the Claims. Suzuki [0140]; *see also id.* [0139] (also discussing t_5), Fig. 11.

Accordingly, even under Petitioner’s new argument—which equates the removal of electrons from the channel with a pre-verify stage—the time period from t_3 - t_4 (i.e., when VPASS is applied) has nothing to do with the “ready operation of the verify operation” described by Suzuki. *See* Suzuki, [0131].

B. Claims 5 and 6: Suzuki Still Does Not Disclose a “Top Bias Voltage” or “Bottom Bias Voltage” Applied “In the Pre-Verify Stage and the Verify Stage”

The Reply does not present any additional arguments for claims 5-6 and merely cross-references Petitioner’s claim construction (Reply 27), which as explained is incorrect. *See* §II.

V. GROUND 3: PETITIONER’S NEW ARGUMENTS FAIL TO SHOW THAT COSTA IN VIEW OF SEO DISCLOSES OR RENDERS OBVIOUS CLAIMS 1-6

A. Independent Claim: Costa in View of Seo Still Does Not Disclose or Render Obvious a “Pre-Verify Stage”

As explained in the POR, neither of the references, alone or in combination, describes a two-stage verification operation. POR 59-61. Indeed, Costa does not describe a verify operation that includes a distinct “pre-verify stage” and “verify stage,” and Seo does not describe verification operations at all. *See* POR 60-61. Indeed, as recognized by the Board, “Seo only describes time periods t1 and t2 with respect to performing a read operation,” and the Petition failed to explain how Seo and Costa could render obvious a multi-stage verification operation. *See* DI 26-27.

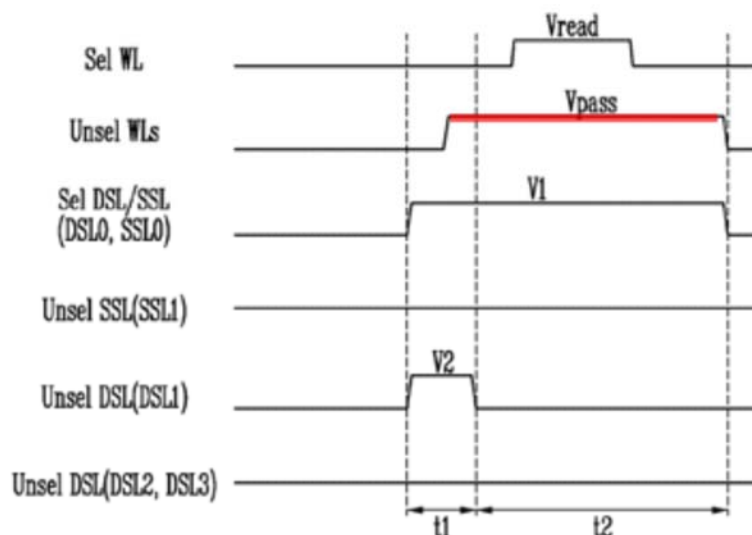
The Reply fails to address this deficiency. Instead, Petitioner falls back on its incorrect argument that “read and verification operations are virtually identical,” and makes the unsupported assertion that a “correspondence” between Seo’s time periods and “pre-verify and verify stages” would be obvious. *See* Reply 28-29. As discussed in relation to Ground 1, however, reading operations and verifying

operations are distinct. Thus, to the extent Seo describes using time period T1 to prepare for reading, that does not render obvious a verification operation with a “pre-verify” stage.

B. Independent Claim: Costa in View of Seo Does Not Disclose or Render Obvious Applying “a First Bias Voltage” and “a Second Bias Voltage” on the Gate Terminal of a Not Programmed Memory Cell “Wherein the Second Bias Voltage Is Smaller than the First Bias Voltage”

As explained in the POR, Costa and Seo do not disclose or render obvious applying distinct first and second bias voltages “on a gate terminal of at least one memory cell of the first memory cell string that is not programmed” during different stages of a verification process. See POR 61-68. Indeed, Seo teaches a constant “VPASS” voltage applied to all unselected word lines during both time periods T1 and T2 of a reading operation as shown in Fig. 8.

FIG. 8



Seo, [0087]-[0090], Fig. 8; POR 64-65.

Costa fails to address this deficiency. Rather than disclosing different voltages during different time periods, Costa discloses that a **single** bias voltage is used on each word line during the entire verify operations. Specifically, Costa teaches that a VPASSL voltage applied to **unprogrammed** word lines, and a higher VPASS voltage can be applied to **programmed** word lines, because unprogrammed word lines have a lower threshold voltage than programmed word lines. Costa [0121]-[0122], [0147]; POR 63-64. As explained by Costa, this teaching is uniquely applicable to verification operations (as compared to a reading operation), because verifications performed as part of a programming loop can leverage the fact that there is a known set of unprogrammed word lines (e.g., all words that have yet to be programmed). Costa [0121]-[0122], [0147]; POR 24, 31, 64.

Even taken together, applying Costa's teachings to Seo would—at most—result in a constant VPASSL on the unprogrammed word lines during T1 and T2, and a constant VPASS voltage applied to programmed word lines during T1 and T2. Even in a combined system, at no point does any of the unselected word lines receive a lower voltage during the second time period T2 relative to the voltage received in the first time period T1. Moreover, as explained in the POR, Petitioner's argument that it would have been obvious to apply Costa's purported teachings **only** during period T2 (thus resulting in a system where the voltage is kept at some default level

during period T1 before being reduced during time period T2) is based on conclusory remarks from Dr. Liu, misinterpretations of the references, and impermissible hindsight. *See* POR 66-68; Przybylski, ¶¶159-164.

The Reply fails to address these deficiencies. To justify applying Costa’s teachings “only during the verify stage,” Petitioner argues that during Seo’s T1 time period (i.e., during the purported pre-verify stage), applying a low voltage to the selected word line implies the “source terminals of the cells above the selected cell are left floating and their voltage increase,” thus requiring a larger gate voltage to compensate. *See* Reply 30. But that argument is not only new and improper, it has no basis in Seo, and still fails to motivate the proposed combination.

At the outset, neither the Reply nor Dr. Liu have provided any citation to Seo for the proposition that there would be a floating voltage on the source terminals of the “cells above the selected cell” that increases over time. Seo does not mention such a phenomenon, nor does Seo describe using larger bias voltages on the “cells above the selected cell” to compensate for such a phenomenon. Even assuming that Seo had some floating voltage effect that increased threshold voltages for all of the memory cells, Costa’s teachings would be applicable during time period T1 and T2 regardless of such effects.

The Reply’s only other argument is to improperly suggest that it would have been at least obvious to apply Costa’s teachings in only the “verify” stage (but not

the “verify” stage) because one of a “finite” number of options. Reply 31. But the obviousness to try doctrine applies only when the options are “finite” and “known,” and here because Costa does not even contemplate the idea of applying different bias voltages during different parts of a verify operation, the option “would not have presented itself as an option at all, let alone an option that would have been obvious to try.” *Rolls-Royce, PLC v. United Techs. Corp.*, 603 F.3d 1325, 1339 (Fed. Cir. 2010). Indeed, applying Costa’s teachings in only one of the two stages violates the very purposes of Costa’s teachings—which is to reduce the voltages applied to unprogrammed memory cells. Thus, producing the combination proposed in the Petition would require choosing an unreasonable option that has no expectation of success, and in violation of the reference’s own teachings. Moreover, the Reply’s characterization of the proposed combination as a result of “finite” possibilities is disingenuous at best. There are myriad voltages that could be applied to combinations of different word lines—far beyond the number that could be experimentally tested with reasonable effort. And contrary to Petitioner’s argument, the number of “options” does not refer to the binary choice of whether to apply a reference’s teachings (or whether to apply a reference’s teachings to certain aspects of the primary reference). Such a framing would erroneously reduce *all* proposed §103 combinations to one of only a handful of possibilities.

**VI. DR. PRZYBYLSKI'S TESTIMONY FURTHER CONFIRMS
PETITIONER'S ARGUMENTS FAIL**

Unable to rebut the testimony of PO's expert, Dr. Przybylski, the Reply inappropriately suggests that his declaration should be set aside based on a couple typos or because Petitioner disagrees with his opinions. *See* Reply 31-32. Dr. Przybylski's testimony is well supported by the record and, unlike Petitioner's and Dr. Liu's arguments, does not rely on attempts to conflate distinct concepts (e.g., verifying vs. reading; target vs. actual voltages) or rewriting claim language as discussed above. That PO relies on and restates Dr. Przybylski's reasoned opinion in the POR does not diminish the weight of his testimony.

Consistent with Dr. Przybylski's testimony, the '957 patent does not refer to "control gates" as "word lines." Ex. 1031, 57:21-58:1. While another unrelated YMTC patent states that "a plurality of tiers of control gates, also referred to as 'word lines (WLs),' are stacked within a memory array structure (Ex. 1025 (USP11,600,342), 6:41-42) as Petitioner notes, this does not mean that "control gates 333 [are] also referred to as 'word lines (WL)'" in all contexts, and certainly not in the context of the '957. Reply 31. Regardless, as Dr. Przybylski testified, the central issue here is that target voltages applied to word lines are not the same as the resulting voltages applied on gate terminals of the memory cells as discussed in Section III.B. Indeed, Petitioner questioned Dr. Przybylski on this issue for well over an hour and, as Dr. Przybylski explained time and time again, Hongtao describes

only “target” voltages—not the resulting voltages on the gate terminals. *See* Ex. 1031, 158:18-212:12.

Finally, Petitioner’s criticisms of Dr. Przybylski’s identification of claim elements in certain figures are also misplaced. As explained by Dr. Przybylski, his declaration identified certain claim elements in certain figures. *See, e.g.*, Ex. 1031, 119:7-10 (“I have a copy of Figure 6 that is annotated with bias voltages and verify voltages, which correspond to some of the elements of Claim 1”), 119:21-120:2 (“Figure 7 illustrates a bottom bias voltage with a fixed voltage level administered to the ... BSG layer in both pre-pulse and the subsequent verify/read stage”). Indeed, Dr. Przybylski carefully distinguished “elements” being embodied in the figures, as compared to “claims” being embodied in the figures. *See, e.g., id.* 120:16-121:7. Similarly, when questioned on whether certain figures showed “piecewise linear waveforms,” Dr. Przybylski answered the questions and then further noted that such questions were “tangential to [his] analysis ... and are not relevant to [his] critique of the arguments in the petition or the declaration of Dr. Liu.” *See id.* 226:5-227:20. As discussed above, unlike Hongtao, the ’957 discloses a “long” pre-pulse time and allowing gate voltages to fully “develop to” their target values. *See* ’957, 11:48-12:9, 12:28-42, 13:13-15; Przybylski ¶37. Petitioner’s attempt to fault Dr. Przybylski as somehow being disingenuous is, once again, a misrepresentation at best.

VII. CONCLUSION

Petitioner has still failed to demonstrate by a preponderance of the evidence that any of the Challenged Claims of the '957 is anticipated or obvious. Accordingly, the Board should uphold the validity of all Challenged Claims.

Dated: June 6, 2025

Respectfully submitted,

ROPES & GRAY LLP

By: /James L. Davis, Jr./

James L. Davis, Jr.

Reg. No. 57,325

ROPES & GRAY LLP

525 University Avenue, 8th Floor

Palo Alto, CA 94301

Telephone: +1-650-617-4794

James.L.Davis@ropesgray.com

Andrew T. Radsch

(*pro hac vice* forthcoming)

ROPES & GRAY LLP

525 University Avenue, 8th Floor

Palo Alto, CA 94301

Telephone: +1-650 617 4763

Andrew.Radsch@ropesgray.com

Christopher M. Bonny

Reg. No. 63,307

ROPES & GRAY LLP

525 University Avenue, 8th Floor

Palo Alto, CA 94301

Telephone: +1-650-617-4011

Christopher.Bonny@ropesgray.com

Abed R. Balbaky

Reg. No. 76,154

ROPES & GRAY LLP

1211 Avenue of the Americas

New York, NY 10036-0003

Telephone: +1-212-841-5797

Abed.Balbaky@ropesgray.com

*Attorneys for Patent Owner, Yangtze
Memory Technologies Co. Ltd.*

CERTIFICATE OF WORD COUNT

The undersigned certifies that the foregoing PATENT OWNER'S SUR-REPLY complies with the type-volume limitation in 37 C.F.R. § 42.24(c). According to the word-processing system's word count, the brief contains 5,583 words, excluding the parts of the brief exempted by 37 C.F.R. § 42.24(c).

Dated: June 6, 2025

Respectfully submitted,

By: /Christopher M. Bonny/
Christopher M. Bonny
Reg. No. 76,154
ROPES & GRAY LLP

CERTIFICATE OF SERVICE

The undersigned certifies that the foregoing PATENT OWNER'S SUR-REPLY was served in its entirety by filing through the Patent Trial and Appeal Case Tracking System (P-TACTS), as well as providing a courtesy copy via e-mail to the following attorneys of record for Petitioner listed below:

Lead Counsel	Back-up Counsel
Jeremy Jason Lang Registration No. 73,604 (jjlang@orrick.com) Postal & Hand-Delivery Address: Orrick, Herrington & Sutcliffe LLP 1000 Marsh Road Menlo Park, CA 94025 T: 650-614-7400; F: 650-614-7401 P52PTABDocket@orrick.com PTABDocketJL2@orrick.com PTABDocketJ3B3@orrick.com T61PTABDocket@orrick.com PTABDocketJ1H1@orrick.com micron-ymtc_ohs@orrick.com	K. Patrick Herman Registration No. 75,018 (pherman@orrick.com) Jared Bobrow <i>Pro Hac Vice</i> (jbobrow@orrick.com) Travis Jensen Registration No. 60,087 (tjensen@orrick.com) Johannes Hsu Registration No. 74,689 (johanneshsu@orrick.com)
<i>Counsel for Petitioner Micron Technology, Inc.</i>	

Dated: June 6, 2025

By: /Jonathan Bradford/
Name: Jonathan Bradford
ROPES & GRAY LLP