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Transcript of David Kuan-Yu Liu, PH.D.

Date: May 28, 2025

Case: Micron Technology, Inc. -v- Yangtze Memory Technologies Company, LTD.
(PTAB)

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WORLDWIDE COURT REPORTING & LITIGATION TECHNOLOGY

YMTC Ex. 2011
Micron v. YMTC
IPR2024-00792 Page 1

1 UNITED STATES PATENT AND TRADEMARK OFFICE

2
3 BEFORE THE PATENT TRIAL AND APPEAL BOARD
4

5 MICRON TECHNOLOGY, INC.,

6 Petitioner,

7 v.

8 YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,

9 Patent Owner.
10

11 Case No.: IPR2024-00792

12 U.S. Patent No. 11,468,957
13

14 VIDEOTAPED DEPOSITION OF DAVID KUAN-YU LIU, PH.D.

15 Conducted Virtually

16 Wednesday, May 28, 2025

17 11:03 a.m. EST
18
19

20 Job No.: 585607

21 Pages: 1 - 180

22 Reported by: Monique Vouthouris, CCR, RPR, CRR

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5
6 VIDEOTAPED DEPOSITION OF DAVID KUAN-YU LIU,
7 PH.D., pursuant to notice, conducted virtually via
8 Zoom Videoconference, before Monique Vouthouris,
9 Certified Court Reporter, Registered Professional
10 Reporter, Certified Realtime Reporter, and Notary
11 Public in and for the States of New Jersey and
12 New York.
13
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A P P E A R A N C E S

ON BEHALF OF PETITIONER, MICRON TECHNOLOGY,
INC., AND THE WITNESS, DAVID KUAN-YU-LIU,
PH.D.:

JOHANNES HSU, ESQ.

ORRICK, HERRINGTON & SUTCLIFFE LLP

2050 Main Street

Irvine, California 92614

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ON BEHALF OF PATENT OWNER, YANGTZE MEMORY
TECHNOLOGIES COMPANY, LTD.:

ABED BALBAKY, ESQ.

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1211 Avenue of the Americas

New York, New York 10036-8704

212.596.9090

ALSO PRESENT:

MATTHEW SIMPSON, Planet Depos Videographer

C O N T E N T S

EXAMINATION OF DAVID KUAN-YU LIU, PH.D.	PAGE
By Mr. Balbaky	6

E X H I B I T S

(Previously marked)

DEPOSITION EXHIBIT	PAGE
Exhibit 1027 Reply Declaration of David Kuan-Yu Liu.	24
Exhibit 1001 U.S. Patent No. 11,468,957, Architecture and Method for NAND Memory Operation.	35

P R O C E E D I N G S

1		
2		11:03:09
3	THE VIDEOGRAPHER: Here begins Media	11:03:09
4	Number 1 in the videotaped deposition of Dr. David	11:03:18
5	Kuan-Yu Liu in the matter of Micron Technology, Inc.	11:03:22
6	versus Yangtze Memory Technologies Company, LTD, in	11:03:26
7	the United States Patent and Trademark Office, Case	11:03:32
8	Number IPR2024-00792.	11:03:34
9	Today's date is May 28th, 2025 and the	11:03:40
10	time on the video monitor is 11:03 a.m. Eastern	11:03:43
11	Time. The remote videographer today is Matthew	11:03:47
12	Simpson representing Planet Depos. All parties of	11:03:47
13	this video deposition are attending remotely.	11:03:51
14	Would counsel please voice-identify	11:03:52
15	themselves and state whom they represent.	11:03:54
16	MR. BALBAKY: My name is Abed Balbaky from	11:03:57
17	the law firm Ropes & Gray, representing Yangtze	11:04:01
18	Memory Technology Company, who is the patent owner	11:04:05
19	in this action.	11:04:07
20	MR. HSU: This is Johannes Hsu with the	11:04:09
21	law firm of Orrick Herrington & Sutcliffe,	11:04:12
22	representing petitioner Micron Technology, Inc.	11:04:14

Transcript of David Kuan-Yu Liu, PH.D.
Conducted on May 28, 2025

6

1	THE VIDEOGRAPHER: The court reporter	11:04:20
2	today is Monique Vouthouris representing Planet	11:04:21
3	Depos.	11:04:24
4	The witness will now be sworn.	11:04:24
5	DAVID KUAN-YU LIU, PH.D.,	11:04:41
6	being first duly sworn or affirmed by the Notary,	11:04:41
7	testifies as follows:	11:05:07
8	EXAMINATION	11:05:07
9	BY MR. BALBAKY:	11:05:07
10	Q Thank you very much, Dr. Liu. I apologize	11:05:11
11	if I mispronounce your name.	11:05:15
12	A No worries, no worries, yeah.	11:05:18
13	Q So just to confirm, can you just please	11:05:20
14	re-identify yourself? What is your full name?	11:05:24
15	A My full name is David Kuan-Yu Liu, with a	11:05:26
16	hyphen between Kuan and Yu, and last name is L-i-u,	11:05:31
17	Liu.	11:05:36
18	Q And where are you located right now?	11:05:36
19	A I'm located in my residence -- or my home	11:05:37
20	office in Fremont, California.	11:05:40
21	Q Very good. What is your occupation?	11:05:42
22	A I am currently working as a consultant	11:05:45

1	individual, yeah, expert consultant advisor, yeah,	11:05:49
2	so...	11:05:54
3	Q I understand. And do you have anything in	11:05:55
4	front of you right now?	11:05:58
5	A No, I don't. I have closed all my files.	11:06:00
6	I assume the relevant document will be uploaded	11:06:04
7	through chat in this Zoom, Zoom platform.	11:06:07
8	Q That's correct. So do you understand that	11:06:10
9	you're under oath today?	11:06:15
10	A Yes, I do.	11:06:16
11	Q Okay. Just laying out some ground rules	11:06:17
12	-- well, first let me ask have you been deposed	11:06:21
13	before?	11:06:24
14	A Yes, I have been.	11:06:24
15	Q Approximately how many times have you been	11:06:25
16	deposed before?	11:06:29
17	A I would say it's in the teens, yeah, so I	11:06:30
18	can't really -- sitting right here I can't really	11:06:33
19	recall, but they are in my CV and I believe it's in	11:06:38
20	the teens, yeah.	11:06:41
21	Q But it's fair to say that you have some --	11:06:42
22	some experience with depositions?	11:06:44

1	A	I would say that's fair.	11:06:45
2	Q	Okay. Well, just going over some basic	11:06:47
3		rules, then, as a bit of refresher, so I will be	11:06:50
4		asking questions today. If I ever ask a question	11:06:54
5		that you don't understand, please ask for	11:06:57
6		clarification. If you don't ask for clarification,	11:06:59
7		I will assume that you have understood the question.	11:07:02
8		Does that make sense?	11:07:06
9	A	Yes, it does.	11:07:07
10	Q	Okay. Periodically opposing counsel may	11:07:08
11		raise objections. If it is the type of objection	11:07:14
12		that requires you not to answer, they will inform	11:07:17
13		you not to answer. Otherwise, as a general rule,	11:07:19
14		you should still answer the questions, not barring	11:07:22
15		objections. Does that make sense?	11:07:29
16	A	Yes, it does.	11:07:31
17	Q	Okay. Is there any reason why you can't	11:07:32
18		answer questions truthfully today?	11:07:34
19	A	No.	11:07:38
20	Q	So you're not on any kind of medications	11:07:39
21		that would impair your ability to answer questions	11:07:42
22		truthfully or fully?	11:07:45

1	A	No.	11:07:47
2	Q	Okay. We will periodically be taking	11:07:47
3		breaks depending on your needs and your comfort. I	11:07:52
4		will attempt to have a break every hour or so. We	11:07:55
5		may take a larger break for lunch at your	11:07:59
6		convenience, if -- if we get there.	11:08:03
7		If at any time you would like to have a	11:08:04
8		break, please let me know and we can work one in.	11:08:06
9		Only two things I want to mention. The first is we	11:08:11
10		should not take breaks in between a question and an	11:08:17
11		answer, so we want you to finish your answers before	11:08:21
12		we go on any given breaks. And the second thing is	11:08:23
13		that I would ask you not to talk with opposing	11:08:27
14		counsel during the breaks. Do you understand?	11:08:30
15	A	Yes, I do.	11:08:35
16	Q	Okay. Very good. So let me just -- so	11:08:38
17		when was the last time you were deposed?	11:08:53
18	A	Let me think. Wow, I think it's also for	11:08:56
19		this -- I'm sorry, I'm drawing a blank. I think a	11:09:05
20		few months back, yes, maybe in the last year,	11:09:17
21		beginning of this year.	11:09:21
22	Q	So do you recall being deposed in relation	11:09:22

1	to IPR number 2024-00795 for Patent Number	11:09:26
2	11,501,822?	11:09:34
3	A Yes, I do.	11:09:35
4	Q Was that the last time you were deposed?	11:09:37
5	A I believe so.	11:09:40
6	Q Okay. And what was the last time before	11:09:49
7	that that you were deposed?	11:09:52
8	MR. HSU: Objection; relevance.	11:09:55
9	A It's I think a few months preceding that.	11:09:57
10	Q Okay. That's fine. So just to lay	11:10:05
11	some -- some introduction here, today I plan to be	11:10:14
12	discussing U.S. Patent 11,468,957. I will refer to	11:10:19
13	that periodically as the '957 patent. Is that okay	11:10:25
14	with you?	11:10:29
15	A Yes, it is.	11:10:29
16	Q And you'll understand what I mean when I	11:10:30
17	refer to the '957 patent?	11:10:32
18	A Yes, I do.	11:10:36
19	Q Do you recall how many declarations you	11:10:37
20	have submitted in relation to this matter?	11:10:43
21	A I believe I submitted initial declaration,	11:10:46
22	and for that initial declaration I was not deposed.	11:10:50

1	So now I am here representing the -- and I submitted	11:10:56
2	subsequently a reply declaration and I believe I'm	11:11:00
3	here to respond to the second declaration.	11:11:03
4	Q So if I refer to your first declaration as	11:11:09
5	your initial declaration and your second declaration	11:11:11
6	as your reply declaration, will you understand what	11:11:15
7	I mean?	11:11:20
8	A I believe so.	11:11:20
9	Q Okay. So regarding your declarations, are	11:11:22
10	there any changes that you made to your declarations	11:11:31
11	or were there any changes made after you affixed	11:11:33
12	your signature?	11:11:35
13	A Not that I can recall.	11:11:41
14	Q And do those declarations reflect all of	11:11:45
15	the opinions that you have formulated in this	11:11:47
16	matter?	11:11:51
17	A I think all opinions, it's pretty	11:11:52
18	inclusive. It does include the opinions I believe	11:12:00
19	when necessary to address the response from the	11:12:04
20	patent owner. Of course, there are a lot of	11:12:09
21	detailed discussion and nuances in terms of device	11:12:13
22	physics, which for the sake of the length of the	11:12:17

1	declaration I did not include. But I don't -- I	11:12:20
2	don't want to use the word "all" to characterize	11:12:23
3	because that's very -- very inclusive.	11:12:27
4	Q But is there anything in your declarations	11:12:33
5	that you would want to correct?	11:12:35
6	A Not at the moment right now.	11:12:38
7	Q What materials did you rely on when	11:12:41
8	formulating your opinions?	11:12:45
9	A Well, beside -- in addition to the	11:12:47
10	relevant documents listed in my reply declaration, I	11:12:55
11	also relied upon my experience working in the flash	11:13:01
12	memory arena, and also based on the -- after that,	11:13:06
13	based on the knowledge of a POSITA at the time of	11:13:12
14	invention.	11:13:15
15	Q How would you characterize a POSITA for	11:13:19
16	the invention of the '957?	11:13:22
17	A I believe that's included in my initial	11:13:24
18	declaration as well as reply declaration, so we can	11:13:29
19	refer to that if you have -- if you have a copy and	11:13:35
20	I can have a copy to look at it.	11:13:38
21	Q Well, we'll get to the declaration in a	11:13:40
22	bit and we can go over that if you would like to.	11:13:44

1	But first let me ask is there any	11:13:51
2	information that you requested but were not provided	11:13:56
3	when preparing your declarations?	11:14:01
4	A I don't believe so.	11:14:09
5	Q Did you review any portion of Micron's	11:14:13
6	reply when preparing your reply declaration?	11:14:17
7	A I may have reviewed it. But sitting right	11:14:36
8	here I cannot -- I cannot recall exactly. But for	11:14:41
9	my reply declaration, of course there are some	11:14:45
10	points which I don't -- based off the declaration	11:14:48
11	from the opposing expert, which some points I	11:14:54
12	believe were erroneous and incorrect, so I took the	11:14:58
13	opportunity in my -- using my reply declaration to	11:15:03
14	address and clarify perhaps the misunderstanding or	11:15:06
15	lack of understanding.	11:15:10
16	Q So, to be clear, Dr. Liu, I didn't ask	11:15:14
17	about your opinions regarding the other expert's	11:15:19
18	declaration. I asked if you had reviewed any	11:15:22
19	portion of Micron's reply when preparing your own	11:15:26
20	reply declaration.	11:15:30
21	So to clarify and confirm, did you review	11:15:34
22	portions of Micron's reply when preparing your own	11:15:39

1	reply declaration?	11:15:43
2	A I believe so. As I answered earlier, the	11:15:45
3	purpose of reply declaration or even the reply is to	11:15:50
4	address the -- some of the details that perhaps were	11:15:56
5	-- in terms of our position perhaps that were	11:16:02
6	misunderstood or perhaps were not understood. So my	11:16:05
7	reply declaration was meant to address some of the	11:16:08
8	misunderstanding and to clarify some of the -- some	11:16:12
9	of the technical details.	11:16:19
10	Q And did you review any portion of Micron's	11:16:20
11	reply when preparing your declaration?	11:16:22
12	A I believe off and on. But I don't know if	11:16:27
13	I actually saw the final reply as we were preparing	11:16:40
14	for our reply declaration.	11:16:45
15	Q You said "off and on." What do you mean	11:16:48
16	by that?	11:16:51
17	A It's like there were points to be	11:17:06
18	discussed and then -- and then that requires support	11:17:09
19	from -- from the expert for the -- for the -- some	11:17:11
20	of the technical aspect, and that's what I meant by	11:17:18
21	off and on, just different technical points and	11:17:21
22	different issue that needs to be addressed.	11:17:24

1 Q Did you review any written portions of 11:17:28
2 Micron's reply? 11:17:35

3 A Can you clarify "written"? Because 11:17:42
4 everything nowadays is electronic. You mean like 11:17:44
5 paper or online or -- 11:17:51

6 Q I mean written as in words in a document, 11:17:53
7 electronic document is what I meant as opposed to, 11:17:57
8 for example, an oral conversation where nothing is 11:18:03
9 written down. 11:18:05

10 MR. HSU: Let me just put a word of 11:18:06
11 caution to Dr. Liu not to -- not to testify as to 11:18:09
12 any privileged conversation that you might have had 11:18:14
13 with counsel. But you can -- you may respond 11:18:16
14 otherwise. 11:18:21

15 A I think it just similar to, in general, to 11:18:21
16 drafting any reply declaration, there were some 11:18:26
17 points that need to be made and they would rely on 11:18:28
18 expert to clarify or to explain the finer details. 11:18:32
19 And so to that extent, yes, there may be some -- 11:18:38
20 some of the portion of the report in written I 11:18:43
21 looked at and some may be in -- yeah, some may be in 11:18:46
22 written form if the written form is defined as 11:18:53

1 something in a document.

11:18:56

2 Q So regarding your own reply declaration,
3 was that also something that you discussed with
4 counsel while you were drafting it?

11:19:01

11:19:08

11:19:11

5 MR. HSU: Same caution.

11:19:15

6 A For example, there was something from the
7 declaration from the expert which I do not believe
8 is correct. I do not believe the proper
9 understanding of the matter was there and I would --
10 I would clarify the technical aspect of it, and if
11 you meant that by discussion, yes, that would be the
12 discussion.

11:19:25

11:19:28

11:19:31

11:19:34

11:19:40

11:19:48

11:19:53

13 Q Did you have any assistance in drafting
14 your declaration?

11:19:54

11:19:57

15 A Can you define "assistance"?

11:20:05

16 Q For example, did anyone other than
17 yourself assist in typing up your opinions or
18 writing down things that were then incorporated into
19 your declaration?

11:20:08

11:20:15

11:20:22

11:20:25

20 A Of course, in drafting a declaration or
21 reply declaration there's always some overhead such
22 as making sure reference citation is correct and how

11:20:34

11:20:37

11:20:43

1 the citation is numbered according to the legal 11:20:46
2 document from the counsel side. And there's always 11:20:49
3 going to be a little polishing here and there in 11:20:52
4 terms of spelling, grammars and editing. 11:20:56

5 So if that falls into category of 11:20:59
6 assistance, yes, there would be assistance back and 11:21:01
7 forth between in producing this reply declaration. 11:21:06

8 Q So would it be fair to say that there is 11:21:09
9 at least some portion of your declaration that you 11:21:22
10 did not literally write yourself? 11:21:27

11 A I don't know the -- I don't know your 11:21:33
12 context of literally I did not write myself. For 11:21:37
13 example, obviously the header page, I did not write 11:21:40
14 the header page, right. 11:21:44

15 But it's fair to say that the opinion in 11:21:46
16 my reply declaration are strictly my opinions, and 11:21:48
17 so are there portion where I literally did not write 11:21:54
18 it? Yes, the header page, the reference citation 11:22:00
19 table and the reference, and those just overhead. 11:22:03
20 And, of course, there may be some minor edits here 11:22:07
21 and there for -- for due to maybe my inadequate 11:22:12
22 English writing because I'm an engineer and things 11:22:15

1 like that. So I think if that's what you meant by 11:22:19
2 literally, yes, maybe perhaps that would fall under 11:22:24
3 that category. 11:22:26

4 Q You referred to minor edits. Do you mean 11:22:26
5 minor edits in the body of the declaration? 11:22:29

6 A Well, I mean, for example, like missing -- 11:22:31
7 misspelling, missing grammatic errors or somehow 11:22:35
8 run-on sentence, things like that, so. I mean, 11:22:40
9 obviously, there would be portions based on your 11:22:43
10 definition of literally not written by me, as I 11:22:47
11 mentioned already, the header page and everything. 11:22:51
12 But my reply declaration is strictly my opinions I 11:22:54
13 stand by. 11:22:57

14 Q Who prepared the annotations to the 11:23:01
15 figures found in your declaration, your reply 11:23:04
16 declaration? 11:23:08

17 A Can you repeat the question again? I'm 11:23:09
18 sorry. 11:23:18

19 Q Let me clarify. In your reply declaration 11:23:18
20 there are several annotated figures. I'm asking who 11:23:24
21 prepared the annotations. 11:23:30

22 A You mean literally like putting markers 11:23:32

1	and everything on it? Or when you said "prepare,"	11:23:38
2	do you mean like based on -- based on my technical	11:23:42
3	content based on my suggestion and then someone	11:23:48
4	actually as per legal actually performed the	11:23:52
5	annotation? I think I'm not sure what you meant	11:23:57
6	with the word "prepare."	11:24:02
7	Q Let's do it both ways. So, first let me	11:24:05
8	ask did you place the annotations yourself? I think	11:24:10
9	you said placing markers as an example. Did you	11:24:15
10	place the markers on your figures?	11:24:20
11	A Perhaps the better way to answer is some	11:24:34
12	of the figures, in terms of the marker, they were	11:24:37
13	not done by me, but they were agreed upon and based	11:24:39
14	on my technical input and based on my technical	11:24:43
15	understanding.	11:24:46
16	Q Who was the one that decided which figures	11:24:56
17	to include in your reply declaration?	11:24:59
18	MR. HSU: Again, I caution the witness not	11:25:00
19	to divulge privileged conversation with counsel.	11:25:02
20	A I'm sorry, I actually missed your question	11:25:07
21	because I was coughing. I apologize.	11:25:11
22	Q Let me rephrase. Was it you or somebody	11:25:15

1 else that decided which figures to include in your
2 reply declaration?

3 MR. HSU: Same caution to the witness.

4 A As in any declaration or reply
5 declaration, it's -- it's -- there's a point to be
6 made, that's why you use illustration, and, of
7 course, there's also nuances of finding the proper
8 illustration to convey properly or adequately the
9 thought or the technical details. So in that
10 regard, I should -- it's fair to say that I am, to
11 say the least, agreeable or even propose the figures
12 that were to be included.

13 Q When you say --

14 A I'm sorry. I'm sorry. And if you have
15 any particular figure in mind of my reply
16 declaration, perhaps I can answer your question more
17 adequately.

18 Q When you said proposed the figures that
19 were to be included, what do you mean?

20 MR. HSU: Counsel, I've allowed this line
21 of questioning to go on for quite some time, but it
22 seems like you're invading more and more into

1	potentially privileged information, so.	11:27:36
2	MR. BALBAKY: Thank you, counsel. My	11:27:40
3	intent is not to elicit any privileged information.	11:27:42
4	I will caution you to limit your speaking	11:27:52
5	objections, but we can move on.	11:27:54
6	A Was there a question before the objection?	11:28:05
7	Q I had asked what you meant when you said	11:28:09
8	that you proposed figures to be included in your	11:28:11
9	declaration.	11:28:16
10	A I just want to state that this is the, I	11:28:21
11	think, redone declaration, reply declaration, and no	11:28:26
12	different than as I understand by the expert. So I	11:28:29
13	think, in general, the process in forming	11:28:40
14	declaration and prior declaration is pretty --	11:28:42
15	pretty set process, and I don't think I -- I just	11:28:44
16	want to say that I don't think I deviate from any --	11:28:48
17	any standard practices.	11:28:51
18	Q You said standard practices. Would it be	11:28:55
19	fair to say that standard practices means that you	11:28:59
20	had some assistance in preparing portions of your	11:29:02
21	declaration but that it reflects your opinions?	11:29:07
22	A Except I would just caution in terms of	11:29:16

1 how you define what the context of preparing 11:29:18
2 assistance and preparing. But it's no different 11:29:22
3 than drafting a declaration and with the aid and 11:29:26
4 back and forth and you just in general just -- just 11:29:28
5 the process. And again, I think I agree with your 11:29:30
6 last statement that this is my opinion and I stand 11:29:34
7 by it. 11:29:36

8 Q Thank you. And just to confirm, and we 11:29:40
9 don't have to go through quite the same rigor, but 11:29:47
10 would it be fair to say that the process you used in 11:29:50
11 drafting your initial declaration was similar to the 11:29:53
12 process used to draft your reply declaration? 11:29:57

13 A Again, I'm always getting very worried 11:30:05
14 when we use the word "similar," and by "similar" you 11:30:09
15 mean there was some citation or overhead that's done 11:30:13
16 by other people, but then I'm forming my opinion, I 11:30:17
17 expressed my opinion either through written words or 11:30:21
18 through illustration, yes, I think that would -- 11:30:24
19 that would reflect the work I put in for the 11:30:27
20 declaration or reply declaration. 11:30:33

21 Q And by "overhead" you mean things that are 11:30:48
22 not changing your opinions or the substance, but 11:30:52

1	might be addressing typos, correcting grammatical	11:30:57
2	issues and things of that nature. Is that correct?	11:31:06
3	MR. HSU: Objection; misstates prior	11:31:09
4	testimony.	11:31:12
5	A I think when I say "overhead," I think I	11:31:13
6	described it already, like the title page, obviously	11:31:16
7	I'm not in charge of the document number and the	11:31:21
8	case number and all that stuff. And then, of	11:31:26
9	course, the list of citation and how they compile	11:31:28
10	together and into the table and how -- how to	11:31:32
11	properly form the citation, yeah, I think those kind	11:31:35
12	of that's what I meant by overhead.	11:31:39
13	But, again, the declaration and reply	11:31:41
14	declaration and I'm sitting here to discuss my reply	11:31:44
15	declaration, strictly my technical opinion and I --	11:31:49
16	and I stand by it.	11:31:53
17	Q Let's change topic slightly.	11:31:57
18	Can you tell me what did you do in	11:32:02
19	preparation for today's deposition?	11:32:04
20	A Again, I would say it's no different than	11:32:06
21	how I prepare for any other deposition or how other	11:32:14
22	experts. I go through the document that's most	11:32:17

1 relevant, which in this case is my reply declaration 11:32:20
2 and in case I review them and I try to review, if 11:32:23
3 necessary, look at the citation, look at or that the 11:32:32
4 relevant material and -- and having discussion with 11:32:39
5 counsel, brief discussion with counsel and just go 11:32:49
6 over some of the logistic and everything. So that's 11:32:51
7 pretty much it. 11:32:55

8 Q Give me a second here. I would like to 11:32:57
9 share a document. I apologize, I'm not quite adept 11:33:04
10 with the remote Zoom interface. Let me know if you 11:33:10
11 were able to receive this. 11:33:25

12 A There is something in the chat box, I'm 11:33:27
13 going to try to download it. Okay. I have pulled 11:33:31
14 up my appear to be document Exhibit 1027. 11:33:36

15 Q So just to confirm for the record, would 11:33:43
16 you agree that this is the document marked Exhibit 11:33:46
17 1027 in IPR2024-00792 entitled the "Reply 11:33:50
18 Declaration of David Kuan-Yu Liu, Ph.D."? 11:33:58

19 A Yes, it appears that's at least the title 11:34:05
20 page, that's correct. 11:34:07

21 Q You can take a moment to look through the 11:34:11
22 document, but can you please confirm that this is a 11:34:17

1	copy of your reply declaration?	11:34:21
2	A Yeah, let me just take a quick look. It	11:34:23
3	appears so.	11:34:25
4	Q If you could please go down to paragraph	11:34:34
5	6, which is located on page 5.	11:34:36
6	A I'm there.	11:34:42
7	Q Can you describe this paragraph to me?	11:34:49
8	A I'll read it to you. "I have also	11:34:58
9	reviewed and considered the materials listed in my	11:35:01
10	prior declaration, the Board's institution decision,	11:35:04
11	patent owner's response, Dr." -- I don't want to	11:35:09
12	butcher the pronunciation -- "Przybylski's	11:35:13
13	declaration, and the following material to the	11:35:16
14	extent relevant to my opinion."	11:35:18
15	Q That's fine. And for the record, I	11:35:22
16	believe it's Przybylski, but --	11:35:24
17	A Przybylski, thank you.	11:35:28
18	Q As long as you do anything close to that,	11:35:30
19	I'll understand what you're referring to.	11:35:33
20	So to confirm, did you analyze the	11:35:35
21	declaration of Dr. Przybylski in preparing your	11:35:41
22	reply declaration?	11:35:46

1	A	Yes, as you can see, I have reviewed and	11:35:53
2		considered the material listed in my prior	11:35:56
3		declaration and also including doctor's declaration,	11:35:58
4		the opposing expert's declaration.	11:36:03
5	Q	So to confirm, you also considered the	11:36:06
6		materials that were cited inside of Dr. Przybylski's	11:36:09
7		declaration?	11:36:15
8	A	To the extent if I believe it's necessary,	11:36:24
9		I would review it, yes.	11:36:27
10	Q	What do you mean by to the extent	11:36:30
11		necessary? Are there portions of his declaration	11:36:34
12		that you did not review?	11:36:38
13	MR. HSU:	Objection; mischaracterizes	11:36:39
14		prior testimony.	11:36:41
15	A	I believe I have included in my reply	11:36:43
16		declaration where Dr. Przybylski cited references	11:36:49
17		when I go there and they do not match and they do	11:36:54
18		not contain the -- at least they do not confirm the	11:36:59
19		argument he was making, in such case I do not know	11:37:05
20		how you would categorize consider or included.	11:37:09
21	Q	So did you review all of the materials	11:37:15
22		cited and relied on in Dr. Przybylski's declaration?	11:37:19

1	A	Can you repeat the question again?	11:37:32
2		Because I think there may be some misconnect between	11:37:35
3		you and I.	11:37:38
4	Q	My question is, did you review the	11:37:44
5		materials that were cited and relied on by	11:37:47
6		Dr. Przybylski in his declaration?	11:37:49
7		MR. HSU: Objection; asked and answered.	11:37:54
8	A	I'm trying to understand the question.	11:38:10
9		Have I considered is your question, right, have I	11:38:12
10		considered?	11:38:15
11	Q	Yes, that is the question.	11:38:16
12	A	Obviously, to the extent if I need to	11:38:19
13		understand better Dr. Przybylski's argument, I would	11:38:23
14		go and seek a citation to understand it to that	11:38:27
15		point, to that extent if you meant consider.	11:38:32
16		But to the extent consider means if I	11:38:37
17		agree with his opinion or I believe his opinion is	11:38:39
18		correct, then I don't -- I would not agree with the	11:38:42
19		word "consider," yeah.	11:38:45
20	Q	To be clear, by "consider" I don't mean to	11:38:49
21		suggest that you agree with his opinions. I'm just	11:38:53
22		trying to confirm that you actually read and gave	11:38:56

1	thought to all of the materials that Dr. Przybylski	11:39:05
2	relied upon in preparing his declaration.	11:39:09
3	MR. HSU: Objection; asked and answered.	11:39:13
4	A Again, I considered his citation to be	11:39:19
5	used. But when you say all, for example, if -- let	11:39:25
6	me go through the paragraph 6.	11:39:30
7	I would say, again, as I answered to the	11:40:00
8	extent that I think it's necessary to understand	11:40:02
9	where it's coming from and to get a sense that the	11:40:04
10	-- perhaps the -- his argument or, yes, I do -- I	11:40:11
11	have reviewed the relevant material.	11:40:18
12	Q When you say to the extent that you think	11:40:25
13	it's necessary to understand where it's coming from,	11:40:32
14	does that mean that, at minimum, you reviewed the	11:40:36
15	portions of the materials that Dr. Przybylski	11:40:39
16	actually cited and relied upon in his declaration?	11:40:46
17	A Can you repeat the question again? It's a	11:40:53
18	long question, yeah, sorry.	11:40:56
19	Q Let me rephrase slightly. Would you agree	11:40:58
20	that Dr. Przybylski cited to various materials in	11:41:08
21	his declaration?	11:41:15
22	A Yes, I agree that citations were included	11:41:28

1 in Dr. Przybylski's declaration. The reason I do 11:41:31
2 not wish to -- the reason I'm uncomfortable in 11:41:41
3 giving the all, for example, if in his declaration 11:41:44
4 includes a book such as Aritome, I'm not going to go 11:41:48
5 through every pages. So when you say "all" I don't 11:41:53
6 believe that's fair. 11:41:56

7 And also some of the citations, as I 11:41:56
8 testified earlier, may not be relevant, but yet it's 11:41:59
9 somehow included by Dr. Przybylski in his 11:42:03
10 declaration. So those I consider -- I would say I 11:42:06
11 consider, I read it, and I don't -- I don't -- I may 11:42:10
12 not agree with it. 11:42:12

13 So I think -- I think the word "all" try 11:42:13
14 to encompassing every detail I'm not comfortable. 11:42:20
15 Obviously, I'm not going to read the whole textbook, 11:42:23
16 and that's why I believe there's a disconnect 11:42:26
17 between you and I in terms of the use of the word 11:42:28
18 "all." 11:42:32

19 Q I understand. And to confirm, I'm not 11:42:32
20 attempting to suggest or ask if you read the 11:42:36
21 entirety of the Aritome textbook. I am trying to 11:42:39
22 confirm that Dr. Przybylski in his reply -- sorry, 11:42:45

1 Dr. Przybylski in his declaration cited to certain 11:42:50
2 page ranges in that textbook. I'm trying to confirm 11:42:58
3 that you at least read the portions of the textbook 11:43:03
4 that he cited to in those page ranges. 11:43:07

5 MR. HSU: Objection; asked and answered. 11:43:11

6 A Since we're talking about, if you can give 11:43:17
7 me a precise or exact citation in the textbook you 11:43:22
8 want to talk about. 11:43:25

9 But barring that, I can give an example. 11:43:27
10 For example, Dr. Przybylski mentioned about 3D NAND 11:43:32
11 has more capacitance than 2D NAND, but that's 11:43:37
12 actually out of context. The context is that even 11:43:42
13 in 3D NAND when you try to charge from the 11:43:44
14 voltage-generating circuit to the word line, and the 11:43:47
15 word line is the control gate, the capacitance seen 11:43:52
16 by the voltage-generating circuit may be large, may 11:43:58
17 be larger between 3D and 2D, but that's irrelevant. 11:44:03
18 That's just going to show up as how long it takes 11:44:07
19 for the voltage generated by the control circuit 11:44:10
20 onto the word line and the control gate together. 11:44:13
21 So to cite that capacitance is larger as 11:44:17
22 if somehow there's going to be a disconnect between 11:44:23

1 word line and control gate, I don't -- I don't give 11:44:27
2 much credence to that, and that's the point I'm 11:44:31
3 trying to make. In terms of citation, the whole 11:44:34
4 book have to take it within the context and also 11:44:37
5 have to take it within the context of '957. 11:44:40

6 When you charge it, the compacitor place 11:44:43
7 equipotential, yes, that capacitor, just like if I 11:44:47
8 charge two capacitors, if one compacitor has higher 11:44:48
9 capacitance than the other capacitor, that doesn't 11:44:50
10 mean that these two capacitor plane are not 11:44:54
11 equipotential with respect to each other, with 11:44:58
12 respect to themselves, right. So this plane is 11:44:59
13 equipotential. This plane is equipotential. It's 11:45:01
14 just that this capacitor it may be larger than this 11:45:07
15 capacitor. 11:45:11

16 So in that citation to use that as if the 11:45:11
17 3D NAND would have disconnect -- more of a 11:45:12
18 disconnect between control gate and word line 11:45:16
19 voltage, I don't -- I don't -- you know, it's not a 11:45:22
20 good argument. 11:45:23

21 So that's what I'm trying to say that in 11:45:24
22 terms of concerning certain argument citation, 11:45:26

1 there's a -- there's a context, there's technical 11:45:31
2 merit, and I consider, and I certainly as a 11:45:35
3 responsible expert witness, I definitely would 11:45:40
4 consider his opinion, I will be objective about it 11:45:42
5 and I will read it, but then I may not agree with it 11:45:46
6 and I have to respond if I not agree with it. 11:45:50

7 So in terms of consideration, in that 11:45:54
8 context, yes. But I did not try to understand the 11:45:56
9 whole book. And, of course, you can probably find 11:45:58
10 some little point in page 597 or something. But, 11:46:02
11 no, I did not consider, I did not read through the 11:46:06
12 whole book if that's what you meant by -- by 11:46:09
13 consider. 11:46:11

14 Q I appreciate that response. But I believe 11:46:16
15 it was unresponsive and I would object to it as 11:46:20
16 such. 11:46:23

17 I wasn't asking for your opinion regarding 11:46:24
18 equipotential on capacitor gates and things of that 11:46:30
19 nature. 11:46:33

20 The only thing I was trying to confirm is 11:46:34
21 that, for example, Dr. Przybylski cited to a 11:46:36
22 particular page range in this textbook and that you 11:46:39

1	actually read those pages.	11:46:44
2	MR. HSU: Objection; asked and answered.	11:46:48
3	A The reason I can respond if the citation	11:46:51
4	the page range trying to make a point and there are	11:46:55
5	certain saving feature within that citation that	11:46:59
6	stand out as not proper or not in the context of	11:47:02
7	'957, of course I will respond to that.	11:47:07
8	But when you say the page range, the page	11:47:08
9	range could contain a lot of things. But then the	11:47:11
10	saving feature of that page range if it has	11:47:14
11	relevance, to my opinion, '957, of course I'm going	11:47:17
12	to bring that out, I'm going to consider it.	11:47:20
13	Q So you can't tell me today if you actually	11:47:22
14	read the pages of the textbook that Dr. Przybylski	11:47:25
15	cited to?	11:47:29
16	MR. HSU: Objection; misstates prior	11:47:32
17	testimony.	11:47:36
18	A I don't believe that's my testimony. I	11:47:36
19	actually earlier requested that if you have	11:47:40
20	particular page, we can go through it and I can tell	11:47:42
21	you precisely whether I review or not.	11:47:44
22	But sitting right here, when you say he	11:47:47

1 cite a certain page and his page range, he also 11:47:50
2 cited the whole Aritome book. I mean, I certainly 11:47:53
3 haven't read all the Aritome book. But if he cited 11:47:57
4 a certain page to make a point, it would be 11:48:02
5 negligent of me not to look at those pages and try 11:48:05
6 to formulate my -- my opinion and my response. 11:48:07

7 Q So to know if you had reviewed any given 11:48:10
8 range of pages in the Aritome book, you would have 11:48:14
9 to look at the Aritome book to review and see? 11:48:17

10 A Look, I'm sitting right here responding to 11:48:21
11 my reply declaration. So in the case can you point 11:48:26
12 out to me where in my reply declaration that the 11:48:29
13 page number you're referring to is relevant and I'll 11:48:32
14 be happy to go through it with you. 11:48:34

15 Q I think we can move on. I'm going to 11:48:45
16 upload a separate document. Please let me know when 11:49:14
17 you receive this. 11:49:29

18 A I haven't seen anything yet in the chat 11:49:30
19 box. Oh, here we go. 11:49:33

20 Q Just give it a second. Sorry, I think 11:49:35
21 it's a little large. 11:49:37

22 A I believe I just downloaded it. 11:49:43

1	Q	So this is the document marked Exhibit 00	11:50:00
2	--	sorry, marked 1001 in IPR2024-00792. It is a	11:50:03
3		copy of the '957 patent.	11:50:12
4		Dr. Liu, can you please confirm that this	11:50:17
5		appears to be a copy of the '957 patent?	11:50:19
6	A	Yes, I can confirm that.	11:50:28
7	Q	And to confirm, this is the patent at	11:50:30
8		issue in the case. Is that correct?	11:50:33
9	A	Yes, that's correct.	11:50:35
10	Q	And to confirm, in formulating your reply	11:50:37
11		declaration, you analyzed certain claims of the '957	11:50:46
12		patent. Is that correct?	11:50:52
13	A	To the extent that analyze means to	11:51:10
14		reaffirm or reiterate the opinion was rendered in	11:51:13
15		the initial declaration perhaps and then to perhaps	11:51:20
16		clarify or to respond to any in rebuttal against the	11:51:23
17		opinion, yes.	11:51:34
18	Q	And then in forming your opinions you also	11:51:35
19		analyzed the figures of the '957 patent. Is that	11:51:39
20		correct?	11:51:45
21	A	Yes, I believe that's fair	11:51:45
22		characterization.	11:51:48

1	Q	Okay. So to start, I would like to have	11:51:50
2		you go down to Figure 2 on page 4 of the '957	11:52:00
3		patent.	11:52:07
4	A	I'm there.	11:52:10
5	Q	Can you, in your own words, describe what	11:52:11
6		this figure is illustrating?	11:52:18
7	A	Taking into context and including the	11:52:24
8		specification and its connection to the limitation	11:52:34
9		of the claim in the language it used, we can	11:52:38
10		actually first go to the -- go to the figure to see	11:52:42
11		what it describe first, and then I will perhaps, if	11:52:47
12		necessary, I'll add some clarification.	11:52:51
13	Q	I'm sorry. I was just trying to get your	11:53:06
14		understanding of what Figure 2 is illustrating.	11:53:10
15	A	And I try to point out to you that I read	11:53:13
16		the specification and I try to use the specification	11:53:17
17		as a guideline, and it says, "Figure 4 is a first	11:53:20
18		schematic diagram of verifying/reading" --	11:53:22
19		"verifying/reading memory cells in a related	11:53:24
20		example, in accordance with exemplary embodiment of	11:53:28
21		disclosure."	11:53:28
22		And we can go to the text specification in	11:53:34

1 column 9, Figure 4 is a schematic diagram of, again, 11:53:39
2 verify/read operation to verify/read memory cell of 11:53:47
3 a 3D NAND memory device. As shown in Figure 4, the 11:53:50
4 verify/read operation include initial stage, 11:53:54
5 pre-pulse stage and verifying stage. 11:53:59

6 Q I'm sorry, Dr. Przybylski, I was asking 11:54:01
7 about Figure 2. 11:54:03

8 A Dr. Liu, yeah, sorry. 11:54:06

9 Q Sorry, apologies, Dr. Liu, I was asking 11:54:07
10 about Figure 2. 11:54:11

11 A Oh, I'm sorry. My bad. That's according 11:54:14
12 to the specification, Figure 2 is a cross-section of 11:54:31
13 view of a 3D NAND memory device, okay. 11:54:35

14 Q So in Figure 2 would you agree that 11:54:44
15 there's an array region labeled as item 200A? 11:54:51

16 A Let's refer to the description of figure, 11:55:02
17 because sitting right here I want to make sure we're 11:55:05
18 accurate. 11:55:08

19 It says column 7, the array region 200A, 11:55:17
20 yes, I would agree. 11:55:22

21 Q And then would you also agree that inside 11:55:29
22 of the array region 200A, there are what are labeled 11:55:33

1	as alternating word line layers 12a through 12p?	11:55:39
2	A Yes, a stack of alternating word line	11:55:55
3	layers 12a and 12p in column 8.	11:56:05
4	Q In your experience, is it possible to have	11:56:20
5	different voltages on different word line layers?	11:56:23
6	A Can you please clarify your question?	11:56:32
7	Q Sure. Assuming for the time being that	11:56:35
8	there is a constant voltage across the entirety of	11:56:42
9	any given word line layer, so the voltage along word	11:56:48
10	line layer 12a is constant, and the voltage across	11:56:52
11	word line layer 12b is constant and so on, can you	11:56:57
12	have different voltages on different word line	11:57:03
13	layers so that, for example, you have a first	11:57:06
14	voltage on word line layer 12a, but a different	11:57:10
15	voltage on word line layer 12b?	11:57:16
16	A I think you have to bracket your question	11:57:23
17	a little bit more because it's still very	11:57:26
18	open-ended.	11:57:29
19	Q How -- how would I need to bracket the	11:57:33
20	question further for you to be able to answer it?	11:57:36
21	A Are you -- I would like to know are you	11:57:40
22	saying that this is a word line and you're saying	11:57:46

1	that the word line -- word line are connected to the	11:57:54
2	same voltage 12a, 12b all the way through 12p are	11:58:02
3	connected to the same voltage, and are you asking me	11:58:09
4	if they can have different voltages even though they	11:58:12
5	are connected to the same voltage, is that your	11:58:14
6	question?	11:58:15
7	Q I never said anything about them being	11:58:15
8	connected to the same voltage. I'm saying that is	11:58:17
9	there ever a situation in which you can have	11:58:21
10	different voltages on different word lines?	11:58:24
11	A I'm glad I asked the clarifying question	11:58:26
12	because it sounds like that was -- can you repeat	11:58:30
13	your question again then, please? I'm sorry.	11:58:33
14	Q My question was in your experience, is it	11:58:38
15	possible to have different voltages on different	11:58:40
16	word line layers?	11:58:43
17	A Again, it depends on the operation and the	11:58:50
18	circumstances. For example, if, as we see in '957,	11:58:58
19	if a given word line layer is a selected word line	11:59:05
20	and the other one acting as either pass gate or	11:59:09
21	unselected word line to perform the respective	11:59:19
22	functioning, it is possible that they will be	11:59:27

1	connected to different voltage and bias at different	11:59:32
2	voltage, if that's what you're asking.	11:59:36
3	Q To confirm, at any given point in time,	11:59:40
4	word line layers can be biased at different voltage	11:59:47
5	levels. Would you agree with that characterization?	11:59:53
6	A Repeat your question again, please.	11:59:56
7	Q My question was, and I'm just trying to	11:59:59
8	confirm, but at any given point in time different	12:00:05
9	word line layers can be biased to different voltage	12:00:11
10	levels?	12:00:15
11	MR. HSU: Objection; incomplete	12:00:18
12	hypothetical.	12:00:20
13	A Again, as I mentioned earlier, the	12:00:30
14	question is very open-ended. So would you like to	12:00:31
15	perhaps frame in a given function or given context?	12:00:35
16	Q I'm just trying to confirm that it is	12:00:44
17	possible to have different voltages on different	12:00:47
18	word lines.	12:00:50
19	A I believe I answered that already. It	12:00:59
20	depends that if they're doing certain operation,	12:01:02
21	depending on the utilization of each memory cell in	12:01:07
22	the string, there may be cases where to serve their	12:01:12

1 respective function they would have different bias
2 voltage on it.

3 Q So to confirm, if it is necessary for the
4 function of the device, different bias voltages can
5 be applied to different word lines. Is that
6 correct?

7 A I would say that's a fair statement, yes.

8 Q How many different bias voltages can be
9 present in the device at any given time?

10 MR. HSU: Objection; incomplete
11 hypothetical.

12 A Repeat your question again.

13 Q How many different bias voltages can be
14 present in the device at any given time?

15 MR. HSU: Same objection.

16 A Which device?

17 Q So, for example, in Figure 2, it describes
18 word line layers 12a through 12p, that's
19 approximately 11-ish word lines. I haven't counted
20 the exact numbers. But could each of those 11
21 different word lines have 11 different bias voltages
22 being applied to them?

1	MR. HSU: Same objection.	12:02:55
2	A I would just say that it's hard for me to	12:02:57
3	understand the context. I have to -- I have many	12:03:04
4	years of working in flash memory experience, so I	12:03:09
5	know how the word line would be biased for a given	12:03:14
6	function and given situation. So I -- if you can	12:03:16
7	bracket into certain functions, for example, in the	12:03:22
8	context of '957 and I can -- I can -- I'll be very	12:03:26
9	happy to answer your question.	12:03:32
10	However, I also want to throw in that	12:03:33
11	regardless how you biased the word line voltage, you	12:03:37
12	can have 12a to 12b, if you want to bias a different	12:03:43
13	flavor, I don't know what -- under what circumstance	12:03:47
14	you would do that. We can -- we can discuss it, I	12:03:50
15	would be happy to discuss all the different	12:03:54
16	scenario. Regardless that in the context of '957	12:03:57
17	each of the word line will be at equipotential. It	12:04:00
18	may not -- 12a may not be same as 12b, but 12a will	12:04:04
19	be equipotential across the whole 12a and vice --	12:04:10
20	and similar for 12b, 12c, 12d. So I don't know what	12:04:14
21	voltage you want to be at, 12a, 12b, 12C. But under	12:04:19
22	what operation condition I would be happy to	12:04:24

1 entertain that different scenario, if you would 12:04:27

2 like. 12:04:29

3 Q So again, Dr. Liu, that was a bit 12:04:29

4 nonresponsive, but we'll try to make it a bit more 12:04:32

5 concrete. Let's turn to Figure 4, which you had 12:04:35

6 looked at before. 12:04:39

7 A Just so to be clear, I'm here to testify 12:04:44

8 in the context of my reply declaration in the 12:04:46

9 context of '957. That was the answer I was trying 12:04:48

10 to give and not something hypothetical with 12:04:51

11 different -- different flavor, different 12:04:54

12 combination, different permutation of voltage to see 12:04:55

13 how many we can try to -- try to hypothetically 12:05:00

14 imagine, yeah, so. 12:05:03

15 Also, counsel, is it okay if we take a 12:05:06

16 break? I think we have been going now for an hour 12:05:09

17 now or you want to ask a question first? 12:05:13

18 Q No, I think that's fine, this is a good 12:05:16

19 moment. You're right, we have been going for an 12:05:20

20 hour. Let's take a break. Would you prefer 5 12:05:24

21 minutes? 10 minutes? What would make more sense 12:05:25

22 for you? 12:05:29

1	A	At least 5 minutes would be good, but up	12:05:29
2		to you, and I appreciate the accommodation.	12:05:32
3	Q	Whatever you prefer.	12:05:36
4	A	Let's do 10 minutes then.	12:05:37
5	Q	Okay, let's do 10 minutes.	12:05:39
6	A	Thank you.	12:05:42
7	THE VIDEOGRAPHER:	We are going off the	12:05:43
8		record and the time is 12:05 p.m.	12:05:44
9		(Recess 12:05 p.m. - 12:14 p.m.)	12:05:48
10	THE VIDEOGRAPHER:	We are back on the	12:14:37
11		record and the time is 12:14 p.m.	12:14:43
12	BY MR. BALBAKY:		12:14:47
13	Q	Thank you very much.	12:14:54
14		Dr. Liu, I believe we were looking at	12:14:55
15		Figure 2. If not, can you please turn back to	12:14:59
16		Figure 2.	12:15:05
17	A	Yes, I'm at Figure 2 right now, thank you.	12:15:06
18	Q	So I was asking before if it is possible	12:15:11
19		to have different word line layers with different	12:15:18
20		voltages. And would it be fair to say that it is	12:15:26
21		possible to connect different word line layers to	12:15:31
22		different voltages?	12:15:35

1	A	Yes, under given operation there may be	12:15:51
2		different voltage on different respective word	12:15:54
3		lines.	12:15:58
4	Q	So, for example, if you had a selected	12:15:58
5		word line and then you had an adjacent unselected	12:16:00
6		word line, those might have different voltages on	12:16:05
7		them?	12:16:08
8	A	Without knowing the context, but given	12:16:16
9		that different word line or different word lines are	12:16:20
10		used to serve as control gates to facilitate the	12:16:26
11		operation of respective memory cells, there would be	12:16:31
12		cases, yes, where different voltage may be on a	12:16:35
13		selected word line and unselected word line.	12:16:39
14	Q	So in Figure 2 do you see element 22, word	12:16:49
15		line contact 22?	12:16:56
16	A	Yes, I do.	12:16:59
17	Q	Can you describe the relationship between	12:17:05
18		the word line contacts and the word lines?	12:17:08
19	A	Can you repeat your question again?	12:17:21
20	Q	Can you describe the relationship between	12:17:24
21		the word line contacts and the word lines?	12:17:29
22	A	I'm trying to see if the... give me one	12:17:35

1	second. Sorry about that. Again, the contacts you	12:18:45
2	wanted, the what?	12:18:56
3	Q I was asking if you can describe the	12:18:57
4	relationship between the word line contacts 22 and	12:19:01
5	the word line layers?	12:19:05
6	A The word line contact serves as the	12:19:18
7	electrical connection to couple the word line to the	12:19:25
8	path where the voltage would be exerted on the word	12:19:43
9	line. So the word line contact itself contacts the	12:19:51
10	word line and at the other end it will in the flash	12:19:57
11	memory architecture will mostly go to -- goes row	12:20:01
12	decoders and which will go to the control circuit	12:20:06
13	volt generating circuit.	12:20:10
14	Q Is there ever a voltage difference between	12:20:18
15	the word line contacts and the word line layers that	12:20:20
16	they connect to?	12:20:25
17	A Repeat your question again.	12:20:29
18	Q Is there ever a voltage difference between	12:20:31
19	the word line contact and the word line layer that	12:20:34
20	the contact is connected to?	12:20:41
21	MR. HSU: Objection; incomplete	12:20:44
22	hypothetical.	12:20:47

1	A	I would say in the context of '957, where	12:20:47
2		these are word line contacts, when the voltage from	12:20:58
3		the voltage-generating circuit going through the	12:21:12
4		resistance path of the X decoder and coming to the	12:21:17
5		contact and finally supplying to the word line, and	12:21:22
6		with the word line given equipotential, because word	12:21:34
7		line is a top layer capacitor, once the word line as	12:21:38
8		a plane reached the potential, there's no current	12:21:51
9		flow, so the word line and word line contact will be	12:21:58
10		at equipotential.	12:22:01
11	Q	Do you see the structure marked as channel	12:22:19
12		structure 18?	12:22:25
13	A	Yes, I do.	12:22:38
14	Q	Would you agree that there are multiple	12:22:40
15		channel structures shown in Figure 2?	12:22:47
16	A	Yes, I would agree.	12:23:13
17	Q	How many do you see?	12:23:14
18	A	Assuming each identical structure in the	12:23:17
19		cross-section are the same, I would say I would see	12:23:29
20		five.	12:23:37
21	Q	Do you see the structure marked as a top	12:23:39
22		channel contact 19?	12:23:56

1	A	Yes, I do.	12:23:58
2	Q	Do you also see the structure marked as	12:24:18
3		bottom channel contact 21?	12:24:21
4	A	Yes, I do.	12:24:34
5	Q	Would you agree that all of the channel	12:24:36
6		structures include a top channel contact and a	12:24:44
7		bottom channel contact?	12:24:47
8	A	Again, you used the word "all." At least	12:24:59
9		the five of them in the picture in the	12:25:04
10		cross-section, yes.	12:25:07
11	Q	So you would agree that all of the	12:25:07
12		illustrated channel structures include a top channel	12:25:09
13		contact and a bottom channel contact. Is that	12:25:14
14		correct?	12:25:17
15	A	Yes, I would agree, yes.	12:25:17
16	Q	In your experience, is it possible to have	12:25:24
17		different voltages at the top channel contact and	12:25:28
18		bottom channel contact of a given channel structure?	12:25:35
19	A	Can you repeat your question?	12:25:47
20	Q	Is it possible to have different voltages	12:25:49
21		at the top channel contact and bottom channel	12:25:53
22		contact of a given channel structure?	12:25:57

1 A The reason I think this -- I'm having a 12:26:37
2 hard time answering your question because I think 12:26:41
3 you need to bracket your question a little more 12:26:44
4 because it's quite broad, because when you -- is 12:26:47
5 there a -- how about this, is there a -- is there a 12:27:00
6 context to your question in terms of the operation 12:27:06
7 in terms of the '957? 12:27:09

8 Q I'm trying to confirm -- let me rephrase 12:27:13
9 this slightly then. Is it possible for the voltage 12:27:17
10 in the channel to change depending on your position 12:27:25
11 within the channel? For example, can the voltage at 12:27:34
12 the top of the channel be different than the voltage 12:27:42
13 at the bottom of the channel? 12:27:44

14 A By "channel" you don't mean channel 12:27:46
15 contact, you mean channel as being the -- as in the 12:27:50
16 context of being driven by the word line and/or the 12:27:58
17 control gate -- driven by the word line, which is 12:28:01
18 the control gate, and dictated by -- by the voltage 12:28:04
19 on the control gate or voltage on the word line, by 12:28:08
20 that do you mean that channel or do you mean channel 12:28:13
21 contact? 12:28:15

22 Q So for the purposes of this question I'm 12:28:15

1 asking about the channel which is shown as channel 12:28:18
2 structure 18, which is controlled in some way by the 12:28:24
3 voltages on the various word lines. 12:28:34

4 A Right. So, I mean, so I understand your 12:28:40
5 question, you're saying that the channel meaning 12:28:44
6 that the channel with respect to each word line, and 12:28:47
7 that word line is gating is controlling the voltage 12:28:50
8 of the channel, is that what you meant by that 12:28:54
9 channel, not the actual shaded contact layer? 12:28:56

10 Q Correct, I'm asking about -- I'm asking 12:29:00
11 about the channel, not the contact layer for the 12:29:03
12 moment. 12:29:06

13 A So for each memory cell you mean the 12:29:06
14 channel, you mean the channel that's gated by the 12:29:09
15 word line for the respective one. And the question 12:29:13
16 is can the -- what's the question again? 12:29:16

17 Q Let me -- let me change -- let's 12:29:19
18 illustrate this a little differently. One moment. 12:29:24
19 Let's go to Figure 3 temporarily. 12:29:32

20 A Okay. 12:29:37

21 Q What is Figure 3 illustrating? 12:29:37

22 A So Figure 3 is a schematic diagram of NAND 12:29:42

1 memory strings, as shown in Figure 3 I believe there 12:29:54
2 are two separate memory strings. 12:29:59

3 Q And can you describe what is a memory 12:30:04
4 string? 12:30:10

5 A In the context NAND flash memory, a string 12:30:10
6 is just a number of memory cells sandwiched by a top 12:30:24
7 select gate and a bottom select gate. 12:30:30

8 Q And these memory strings, would you agree 12:30:34
9 that they are formed by channel structures as shown 12:30:40
10 in Figure 2? 12:30:44

11 A With the caveat that the Figure 2 is 12:30:56
12 showing a 3D NAND implementation, where Figure 3 by 12:30:59
13 itself may or may not be -- does not have to be a 12:31:04
14 3D. But if we were to say that Figure 3 is taking 12:31:12
15 two of the string of Figure 2, then I would agree 12:31:15
16 that Figure 3 could be a representation of two of 12:31:19
17 the string in Figure 2. 12:31:22

18 Q And what would you describe as the channel 12:31:28
19 structure in Figure 2, where is that being shown in 12:31:31
20 Figure 3, if at all? 12:31:34

21 A As you can see from Figure 3, that just 12:31:39
22 take the string on the left-hand side, each memory 12:31:42

1 cell -- I'm just focused on memory cell. Of course,
2 the same will apply to the select gate, but let's
3 just focus on memory cell because the channel is in
4 series. So for given memory cell, the channel will
5 be the region that the current will flow and the
6 channel potential will be dictated by the word line
7 voltage, word line voltage acting as the control
8 gate to modulate the channel of each respective
9 cell.

12:31:48

12:31:57

12:32:01

12:32:04

12:32:15

12:32:19

12:32:22

12:32:26

12:32:32

10 Q And the actual potential within the
11 channel, could it be different for different memory
12 cells?

12:32:34

12:32:38

12:32:41

13 A Do you have a particular scenario?

12:32:43

14 Because it's a -- it's a very -- 3D NAND by nature
15 is very -- I would say very -- it really depends on
16 the circumstance. And most people don't understand
17 3D NAND as well, so as evidenced -- anyway, most
18 people may not, may not understand, so...

12:33:01

12:33:04

12:33:17

12:33:20

12:33:24

19 Q Assuming that you were to bias all of the
20 gates of all of the shown memory cells, memory cell
21 0 up through memory cell M plus 1 at some high
22 voltage sufficient to turn on the memory cells so as

12:33:28

12:33:39

12:33:47

12:33:52

1 to make them conduct, and then assuming you were to 12:33:55
2 also bias the bottom select gate at a high voltage 12:33:57
3 and the top select gate at some low voltage, would 12:34:02
4 you agree that under such a biasing scheme the 12:34:09
5 entire channel would be at the same voltage as 12:34:14
6 whatever voltage is being applied through the bottom 12:34:21
7 contact? 12:34:24

8 A Repeat your question. I don't think the 12:34:28
9 question you asked it's accurate, please. 12:34:30

10 Q I'm trying to understand, and maybe I can 12:34:41
11 rephrase slightly, if the channel, meaning the 12:34:44
12 channel formed by all of the memory cells, has one 12:34:54
13 voltage or if it can have multiple voltages at 12:34:59
14 different locations. 12:35:03

15 A Again, it would depend on the particular 12:35:09
16 operation, as you were saying, for example, the TSG, 12:35:12
17 the gate to the top select transistor and then you 12:35:17
18 have all these word lines WM plus one, this word 12:35:20
19 line as being the gate to each respective memory -- 12:35:24
20 memory cell, it would depend on the condition. 12:35:28

21 For example, let's hypothetically take the 12:35:30
22 one you were trying to allude to, but I don't 12:35:33

1 believe the question was adequate. Let's say that 12:35:36
2 the TSG, the gate and BSG the gate to the bottom top 12:35:39
3 and bottom select transistor are turned on as well 12:35:46
4 as all the memory cells are turned on by the word 12:35:50
5 line voltage to the gate, then presumably you have a 12:35:53
6 conductive channel going from the fill line to the 12:35:57
7 ACS. However, it would depend on, respective 12:36:02
8 channel depend on what is the bit line voltage, what 12:36:06
9 is ACS voltage. 12:36:10

10 Q Can you clarify what do you mean by "ACS"? 12:36:13

11 A ACS means array common source. ACS mean 12:36:17
12 the bottom that's connected to another node. ACS is 12:36:23
13 where you mentioned about being the -- I'm sorry, I 12:36:27
14 forgot the designation. 12:36:30

15 Q Thank you. If -- if one of the memory 12:36:34
16 cells was disconnected, had a low voltage, could you 12:36:36
17 then have different voltages on the top and bottom 12:36:43
18 of the channel? 12:36:47

19 MR. HSU: Objection; incomplete 12:36:50
20 hypothetical. 12:36:52

21 A Again, as I mentioned, it really depends 12:36:53
22 on the voltage on the bit line and voltage on the 12:36:57

1	source line.	12:37:00
2	Q Let's assume they have different voltages	12:37:02
3	and let's assume that only one of the memory cells	12:37:04
4	is turned off.	12:37:08
5	MR. HSU: Same objection.	12:37:12
6	A Do you have a particular memory cell	12:37:15
7	that's turned off? And when you say they have	12:37:17
8	different voltages, how does that work?	12:37:19
9	Q Let's say word line N is turned off and	12:37:24
10	let's say that ACS is at 0 volts and that the bit	12:37:30
11	line is at 5 volts.	12:37:36
12	A How about rest of the gate such as WLn+1	12:37:44
13	through all the way --	12:37:49
14	Q All the other gates are turned on.	12:37:51
15	A So all the WL are turned on, and then the	12:37:53
16	only thing that's turned off, the only gate that's	12:37:56
17	turned off is WLn, right.	12:37:59
18	Q Correct.	12:38:01
19	A And the bit line is a high voltage, let's	12:38:02
20	say 2 volt and ACS is ground you said?	12:38:05
21	Q Yes.	12:38:08
22	A One of the possibility in this scenario is	12:38:21

1 that the MCn, the memory cell, that's gated by WLn 12:38:24
2 source N will be brought down to ground potential 12:38:29
3 simply because there's a connecting path from -- 12:38:34
4 from ACS all the way to go up to the source of the 12:38:35
5 MCn. And then because the WLn is off, the drain 12:38:41
6 voltage, the channel will be floating, the drain 12:38:49
7 channel is volt, so then all the different WLn+1 all 12:38:53
8 the way to above WLn+1 gates and the TSG will 12:39:01
9 basically facilitate the charging of the bit line 12:39:06
10 potential on the drain side to -- to whatever 12:39:12
11 voltage minus -- minus the threshold voltage on 12:39:17
12 the -- on the drain side. 12:39:20
13 Q So the potential on the channel is it 12:39:23
14 would be different on the drain side and the source 12:39:25
15 side. Is that correct? 12:39:28
16 A On the drain side source side of what? 12:39:29
17 Because the potential will be equipotential, for 12:39:35
18 example, for the memory MC0 gated by WL0 -- 12:39:35
19 (Court Reporter clarification.) 12:39:35
20 A So the question was would there be a 12:39:51
21 potential difference, I'm trying to clarify which 12:39:53
22 memory cell is referring to, because, for example, 12:39:56

1	the memory cell designated as MC0 gated by WL0 will	12:39:59
2	be at equipotential because the ACS voltage of	12:40:07
3	ground will pass through all the way to go to the	12:40:12
4	source of the memory cell MCn gated by WLn. So that	12:40:17
5	path will be at equipotential of whatever low	12:40:24
6	voltage or 0 voltage gated by -- driven by ACS,	12:40:29
7	whereas the transistor above the MCn, they will have	12:40:34
8	different potential eventually charging up --	12:40:42
9	actually, they will eventually be equipotential, but	12:40:45
10	they will charge up at the drain side of MCn to be a	12:40:49
11	voltage that is whatever the word line voltage on	12:40:56
12	the WLn+1 is minus the threshold voltage, taking	12:41:01
13	account of the fact that MCn is floated, so there	12:41:06
14	will be a body effect and then the threshold voltage	12:41:10
15	would not be the major threshold voltage, it would	12:41:13
16	be a threshold voltage with body effect, so...	12:41:17
17	Q So to be clear, in this hypothetical we	12:41:19
18	were describing that there was some fixed voltage	12:41:22
19	being applied to the bit line. Does that change any	12:41:25
20	of your answer?	12:41:28
21	A Actually, I answered assuming there's a	12:41:32
22	fixed bit line voltage, because that was the -- that	12:41:36

1 was the boundary you set and you said there's a bit 12:41:43
2 line voltage and there's some kind of voltage and 12:41:47
3 there's ACS, there's a ground voltage on ACS, that 12:41:50
4 was the premise of your question. 12:41:53

5 Q Correct. So to confirm, then, there is a 12:41:56
6 different potential on the drain side and the source 12:42:01
7 side. I understand that you wanted to add some 12:42:07
8 details about body effects and floating and so on. 12:42:10
9 But just at its most basic, are the potentials 12:42:13
10 different? 12:42:18

11 A So I was trying to make sure I answered 12:42:19
12 your question with the proper context, and the 12:42:21
13 answer I was giving that you're saying that there's 12:42:24
14 a potential difference between drain side and source 12:42:26
15 side. Drain side of which transistor and source 12:42:30
16 side of which transistor, there's a subtlety here. 12:42:33

17 Q I was trying to propose a simple 12:42:39
18 hypothetical where only one word line is turned off, 12:42:42
19 which is word line N. And so to clarify, drain side 12:42:45
20 is relative to word line N and source side is 12:42:50
21 relative to word line N. Would you agree that 12:42:55
22 there's a potential difference between the drain 12:42:59

1	side and the source side?	12:43:01
2	A Thank you for clarification. Yes, the top	12:43:03
3	side of MCn driven by -- gated by WN would have a	12:43:06
4	voltage that's different from the bottom side of MCn	12:43:15
5	driven by ACS.	12:43:21
6	Q Let's go back to Figure 2 for a second.	12:43:25
7	In that situation we described, would there be a	12:43:30
8	different voltage on the top channel contact and the	12:43:35
9	bottom channel contact?	12:43:40
10	A Repeat your question again. I think I	12:43:50
11	know what you're asking, but I don't know if that's	12:43:53
12	what you want to ask. Please.	12:43:55
13	Q Well, I'm trying to understand what is the	12:43:57
14	voltage of the top channel contact relative to all	12:44:03
15	these other voltages that we've been describing and	12:44:08
16	the voltage of the bottom channel contact relative	12:44:10
17	to all these other voltages we've been describing.	12:44:14
18	Are they the same? Are they different? That's my	12:44:18
19	question.	12:44:23
20	MR. HSU: Objection; compound.	12:44:24
21	A I think the question is just -- I'm sorry	12:44:31
22	for taking the time to answer, but I think that the	12:44:53

1 question, it's we just went over the top channel

12:44:58

2 contact, by that you mean 18, okay, that actually

12:45:06

3 corresponds to the bit line that we just described

12:45:12

4 in the string.

12:45:15

5 Q Okay.

12:45:18

6 A Whereas the -- I don't feel like I have to

12:45:19

7 say this, but whereas 21, if you meant that by the

12:45:23

8 bottom channel contact that actually corresponds to

12:45:27

9 the ACS. So in the hypothetical case that you just

12:45:29

10 mentioned, I hope it's not a -- I'm not -- I'm not

12:45:33

11 following your true question. In the hypothetical

12:45:38

12 case one is bit line, one is ACS. And under your

12:45:40

13 definition that bit line and ACS are supplying with

12:45:45

14 different voltage and I would -- so I'm not -- is

12:45:49

15 that your question? I'm sorry, yeah, I'm sorry.

12:45:53

16 Q Yeah, to clarify, my question is, is the

12:45:56

17 top channel contact the same as the bit line and is

12:45:59

18 the bottom channel contact the same as the ACS?

12:46:07

19 MR. HSU: Objection; compound.

12:46:12

20 A I assumed that you were asking. But, you

12:46:15

21 know, having gone through many depo, I just -- I'm

12:46:19

22 very many depo, I'm -- how do you say? I'm very

12:46:25

1 scared of question like this. 12:46:28

2 But yes, to answer your question, yes, the 12:46:30

3 top channel contact is considered to be, in the 12:46:32

4 Figure 3 will be considered to be the bit line, 12:46:37

5 whereas the bottom channel contact will be 12:46:40

6 considered the ACS. 12:46:43

7 And to go back to your question whether 12:46:44

8 they can be different potential under the scenario 12:46:48

9 in the context you have described where you want to 12:46:51

10 set up one of the transistor in the middle, but you 12:46:55

11 apply different voltage to -- respective to the bit 12:46:59

12 line, which is the top channel contact, and to the 12:47:02

13 ACS, which is bottom channel contact, and under that 12:47:05

14 contacts, yes, the voltage of the two will be 12:47:11

15 different. 12:47:14

16 Q Thank you. 12:47:14

17 A I hope I answered the question, yeah. 12:47:15

18 Q That's been very helpful. I appreciate 12:47:17

19 your answer. 12:47:20

20 Let's go back to Figure 3 for a second 12:47:21

21 here. 12:47:23

22 A Okay. 12:47:25

1	Q	So Figure 3, let's focus on the left-hand	12:47:25
2		side, do you see the item labeled BSG?	12:47:28
3	A	Yes, I do.	12:47:36
4	Q	Is that a bottom select gate?	12:47:39
5	A	The symbol, yes, I believe the symbol is	12:47:46
6		to denote, just like all the different other symbols	12:47:50
7		such as WL0 to WLn+1, those are denote the gate,	12:47:56
8		which means the control terminal control layer to	12:47:59
9		drive the transistor in that case for BSG is to	12:48:04
10		modulate -- or modulate or control the transistor	12:48:09
11		so-called BST.	12:48:13
12	Q	I'm sorry. So the BST, that's the bottom	12:48:19
13		select transistor, and is that the same, is it also	12:48:25
14		referred to as bottom select gate or are those	12:48:30
15		different concepts?	12:48:32
16	A	Figure 3 is trying to illustrate on the	12:48:35
17		left-hand side all the transistor symbol those are	12:48:39
18		the you can call the control gate or gate that are	12:48:43
19		driving respective transistor. And by that we can	12:48:47
20		also consider the memory cell to be a transistor.	12:48:53
21		So on the left-hand side you have these	12:48:56
22		gate. Because gate are meant to control the	12:48:59

1 transistors, we can call them a control gate even 12:49:04
2 though they may or may not be memory cells. So you 12:49:07
3 have all these control gate that goes from BSG, WL0, 12:49:10
4 WLn-1 all the way to TSG. These are the gates that 12:49:12
5 are driving the transistor and the transistors are 12:49:17
6 designated on the left-hand side by BST, meaning 12:49:19
7 bottom select transistor, and you have MCn meaning 12:49:24
8 memory cell 0 because that's the lowest one in the 12:49:26
9 string, and you keep going up and eventually you get 12:49:31
10 to the top select transistor, TST 306A. 12:49:34

11 So the left-hand side is denoting the gate 12:49:38
12 that's controlling the transistor and the transistor 12:49:41
13 are given the name which is shown on the right-hand 12:49:44
14 side. 12:49:47

15 Q I see. So to clarify something you said, 12:49:47
16 and the control gate, is that referring to the 12:49:51
17 entire transistor, or is that referring to the 12:49:57
18 terminal -- 12:50:01

19 MR. HSU: Objection. 12:50:01

20 Q -- the gate terminal of the transistor? 12:50:02

21 MR. HSU: Objection; form. 12:50:04

22 A Can you -- I don't know how you demarcate 12:50:15

1 control gate versus control gate terminal. 12:50:19

2 Q Well, how would you define the term 12:50:22

3 "control gate"? 12:50:25

4 A It's a physical -- you can call a layer in 12:50:32

5 the 3D NAND case, physical layer in that case will 12:50:37

6 be the one we just went through 12a and 12b. These 12:50:41

7 layers that are formed on top of the channel of the 12:50:46

8 memory cell or the transistor separated by a 12:50:51

9 dielectric. That's the whole premise of MOS, you 12:50:56

10 have dielectric in between. And these gate you can 12:51:00

11 call a gate and some people -- I don't know where 12:51:04

12 the gate terminal come from, but -- in the contact, 12:51:06

13 but I don't know what you mean by the contact. Gate 12:51:10

14 terminal will just be meaning that I'm pointing to 12:51:14

15 certain thing. 12:51:16

16 But these are the gates, gates are 12:51:18

17 physical material, physical layer that are meant to 12:51:20

18 form in the contacts of 3D NAND so that they can 12:51:24

19 facilitate controlling or modulating of the channel 12:51:27

20 which we just described is the -- go back to Figure 12:51:30

21 2, is the -- is the thing that you talk about formed 12:51:34

22 by 18 going all the way down, that's modulating the 12:51:38

1 channel through modulating each of the transistor,
2 meaning that BST MC0 all the way to TST.

3 So the gate in the context that we just
4 went through in Figure 2 and Figure 3 is the word
5 line layer physical material that modulate each
6 individual transistor.

7 So when you say gate terminal, I assume
8 that you may be point to the circle of MCn, you
9 point to where the little line coming out you say,
10 okay, where the control gate material, which is the
11 word line layer, I'm using that to show that that's
12 a terminal.

13 Because when you draw a schematic of a
14 transistor you call it this is my drain terminal,
15 this is my source terminal, this is my gate
16 terminal. That is not describing a physical thing.
17 Whereas when you were describing the 18 contact,
18 those are more physical things. So we have bit line
19 contact on the top, we have source line contact ACS
20 on the bottom, those are physical material, and you
21 have the word line layer acting as the gate crossing
22 each of the -- each of the 18 channel formed by 18.

12:51:41
12:51:45
12:51:50
12:51:53
12:51:57
12:52:01
12:52:02
12:52:07
12:52:12
12:52:15
12:52:19
12:52:24
12:52:25
12:52:27
12:52:30
12:52:33
12:52:36
12:52:38
12:52:42
12:52:45
12:52:48
12:52:53

1	So that's the definition.	12:52:59
2	So gate just means that the material where	12:53:01
3	you apply the bias that will modulate the	12:53:06
4	transistor.	12:53:08
5	Q So to confirm what you just said, the gate	12:53:12
6	is material where you apply bias that will modulate	12:53:20
7	the transistor. Is that correct or is that	12:53:23
8	definition inaccurate?	12:53:27
9	A That's incorrect -- I wasn't giving a	12:53:31
10	definition. I was giving a description in the	12:53:34
11	context that you were asking. Just like we were	12:53:36
12	going through the bit line, I tried to explain that	12:53:38
13	the bit line is 18 and ACS is actually the 21 that	12:53:41
14	you were mentioning. I'm trying to describe a	12:53:46
15	physical description. I'm not trying to give a	12:53:47
16	definition, okay.	12:53:50
17	So the definition of gate, I'm not here	12:53:52
18	to -- to define gate. Suffice to say that I'm here	12:53:55
19	to describe that in the context of our discussion	12:53:59
20	with Figure 2 and Figure 3, the gate of respective	12:54:02
21	memory cells are the word line layers that	12:54:06
22	intersects with the pillar that you've just shown,	12:54:09

1 you just asked me to describe, contact by 18 and 12:54:13
2 then I believe it's 21 on the bottom, and that's the 12:54:16
3 channel where the different transistors are formed 12:54:20
4 so that gate layer, word line layer, crossing each 12:54:25
5 one will form each memory cell or the BST and TST. 12:54:29

6 I'm giving a description of the gate and 12:54:35
7 I'm also giving a description of function of the 12:54:37
8 gate, which is to modulate the channel of their 12:54:40
9 respective transistor to either conduct or not 12:54:42
10 conduct or either -- either boost it or not boost it 12:54:45
11 or such. I'm giving a description. I'm not giving 12:54:50
12 a definition. 12:54:53

13 Q Let's go to Figure 2 for a second. So you 12:54:54
14 said something and I want to clarify and confirm 12:55:08
15 that this is the case, you said that the gate of the 12:55:10
16 respective memory cells is where the word line layer 12:55:15
17 intersects with the pillar. Can you clarify what 12:55:20
18 you mean by that? 12:55:25

19 A I don't believe that's what I said. I 12:55:26
20 said the transistor is formed by -- a transistor in 12:55:29
21 the 3D NAND is formed by the intersection of the 12:55:34
22 word line layer acting as a gate with the groove or 12:55:38

1 trench, if you call it, 18 acting as a channel, a 12:55:45

2 transistor is formed through that intersection. 12:55:49

3 Q Now, you say the word line layer acts as a 12:55:56

4 gate. Can you explain what you mean by that? 12:56:01

5 A The word line layer -- I did not say word 12:56:05

6 line layer acting as a gate. I'm saying as a 12:56:06

7 description, physically the word line layer is the 12:56:10

8 gate layer that intersect the groove to form a 12:56:14

9 transistor. So the word line layer is where the 12:56:17

10 voltage of -- the voltage for the gate of that 12:56:24

11 particular transistor is not contact. Word line 12:56:33

12 layer is the gate layer that supply the voltage to 12:56:42

13 that memory transistor. 12:56:47

14 Q And when we're saying "gate," do you mean 12:56:55

15 control gate or do you mean something else? 12:56:58

16 A As I testified earlier, because in a 12:57:01

17 string you have both the select gate transistor, 12:57:07

18 whether it's top or bottom, and you also have memory 12:57:14

19 cells. These are -- although they are all 12:57:18

20 transistor, but only the memory cells serve to store 12:57:21

21 data. 12:57:26

22 Therefore, I am trying to make it more 12:57:28

1 general by saying that electrically speaking in the 12:57:32
2 electrical sense, the function of the gate is to 12:57:35
3 modulate the channel, to modulate channel by 12:57:41
4 modulate conductivity or potential of the channel to 12:57:45
5 facilitate transistor behavior. 12:57:48

6 So in that context the gate all have a 12:57:51
7 functioning of control gate just so it's easier when 12:57:55
8 I say that, otherwise because most people tend to -- 12:57:59
9 in the flash memory most people tend to associate 12:58:03
10 control gate, the electrical control gate as the 12:58:06
11 gate driving a memory transistor and they don't 12:58:09
12 necessarily associate control gate. 12:58:11

13 Because when you talk about 12:58:14
14 microprocessors in modulate arena people talk about 12:58:17
15 gate of the MOS transistor. They don't necessarily 12:58:20
16 use the control gate even though the function of the 12:58:22
17 gate is to control the conductivity or the 12:58:25
18 modulating the channel. It's just that in flash 12:58:29
19 there's also a nuance of people -- that especially 12:58:32
20 people -- not in this case not in the case of 3D 12:58:34
21 NAND, but in the case of 2D NAND sometime you have a 12:58:38
22 floating gate, the gate is not -- the gate is 12:58:42

1 actually another conductor material, so you have a 12:58:44
2 control gate and a floating gate to demarcate the 12:58:48
3 two gates in a double-gated type of structure. 12:58:49

4 So but in our case in the context '957 12:58:53
5 control gate simply means that it's a gate, 12:58:57
6 electrically serve as a gate to control the behavior 12:59:00
7 of the channel. So I lump that to include both 12:59:03
8 bottom select transistor and top select transistor. 12:59:07

9 Q I appreciate that. And does each memory 12:59:10
10 cell have its own control gate? 12:59:31

11 A So in the context of Figure 2 and Figure 12:59:36
12 3, because I'm -- we are under the context that 12:59:43
13 Figure 3 is a schematic, circuit schematic diagram 12:59:49
14 of two of the string in Figure 2. In that case, 12:59:54
15 yes, each memory cell has its own control gate as 12:59:58
16 denoted by the W_{Ln-1} , W_{Ln+1} , which I mentioned on 13:00:03
17 the left-hand side is describing the gate that's 13:00:07
18 going to be modulating the transistor and the 13:00:10
19 transistor is described denoted by the annotation on 13:00:12
20 the left-hand side, which is $BST\ 302\ MC_0\ MC_{n-1}$, to 13:00:17
21 that extent, for example, let's look at MC_n , which 13:00:23
22 you were talking about -- 13:00:23

1	(Court Reporter clarification.)	13:00:23
2	A MCn, the middle transistor, memory cell N,	13:00:31
3	N as in Nancy, and I apologize for getting -- I'm	13:00:35
4	very passionate about flash memory so I get excited,	13:00:39
5	yes.	13:00:43
6	So the MCn obviously is -- has its control	13:00:43
7	gate being the WLn as shown on left-hand side. And	13:00:50
8	I should mention that the WLn may also be the gate	13:00:55
9	for another transistor in a different string, as in	13:01:05
10	the case you see it on the right-hand side of the	13:01:09
11	string the 300B, I'm assuming that the Figure 3	13:01:13
12	designation, based on the description, is showing	13:01:18
13	another string.	13:01:22
14	So the gate layer which is the word line	13:01:23
15	layer, WLn, were actually crossing both of the	13:01:27
16	string. So, yes, each memory transistor will have a	13:01:32
17	unique gate. For example, MCn will have a unique	13:01:37
18	gate on string 300A of WLn. But WLn could be a gate	13:01:41
19	to other memory cells on the same layer but on a	13:01:50
20	different string. Does that make sense?	13:01:59
21	Q Let me try to clarify so that I	13:02:04
22	understand. So every memory cell has a control gate	13:02:09

1	which is connected to a word line layer, and all of	13:02:25
2	the control gates within that layer are connected	13:02:36
3	together. Is that right? Or did I get that wrong?	13:02:43
4	MR. HSU: Objection to form.	13:02:48
5	A Sorry. Can you repeat last sentence you	13:02:50
6	just said?	13:02:53
7	Q Sure. I said that every memory cell has a	13:02:55
8	control gate which is connected to the word line	13:03:02
9	layer and that all the gates within a given layer	13:03:05
10	are connected together.	13:03:13
11	MR. HSU: Objection; form, compound.	13:03:16
12	A I think in the context of Figure 3, it's	13:03:21
13	very clear that the string on the right-hand side,	13:03:24
14	let's use again the MCn, the string on the left-hand	13:03:31
15	side the memory cell MCn, along with the string,	13:03:35
16	s-t-r-i-n-g, a string on the left-hand side also	13:03:42
17	denoted by MCn, they share the same gate layer,	13:03:46
18	which is WLn.	13:03:52
19	Q Now, is the gate layer the same as a gate?	13:03:56
20	Are they sharing the same gate layer or are they	13:04:00
21	sharing the same gate?	13:04:03
22	A By sharing physically the same gate layer,	13:04:06

1 they electrically share the same gate. So by -- 13:04:11
2 even more specific as we see on Figure 3, by 13:04:21
3 physically sharing the same WLn layer, you 13:04:24
4 electrically share the same gate, which is also 13:04:29
5 denoted by WLn, along with other gate layers such as 13:04:36
6 BSG, bottom select gate. 13:04:42

7 So there's a physical layer and there's an 13:04:49
8 electrical function. So you're right in the sense 13:04:52
9 that the left string and right string, especially 13:04:56
10 specifically on MCn, physically they share the same 13:05:00
11 gate layer of WLn and electrically they share the 13:05:05
12 same gate, and also designated as WLn. 13:05:09

13 Q Going back to Figure 2 for a second, you 13:05:18
14 made -- 13:05:23

15 A Before that, almost another hour -- 13:05:24
16 (Simultaneous speaking.) 13:05:24

17 Q Do you want to take a break? 13:05:29

18 A We can finish your question if you want if 13:05:30
19 the question is short, I don't mind. 13:05:33

20 Q No, I think it's okay. We can take a 13:05:35
21 small break if you would like. 13:05:38

22 A Yeah, maybe this time five minutes. 13:05:40

1	Q	Five minutes sounds good, yes.	13:05:42
2	A	Thank you for the accommodation, I	13:05:44
3		appreciate it.	13:05:46
4	Q	No worries. Any time you need it.	13:05:48
5		THE VIDEOGRAPHER: We are going off the	13:05:51
6		record and the time is 1:05 p.m.	13:05:52
7		(Recess 1:05 p.m. - 1:10 p.m.)	13:05:55
8		THE VIDEOGRAPHER: We're back on the	13:10:12
9		record and the time is 1:10 p.m.	13:10:17
10		BY MR. BALBAKY:	13:10:26
11	Q	So, Dr. Liu, if you recall before we took	13:10:27
12		our break we were looking at Figure 2. So I wanted	13:10:30
13		to ask a couple questions to clarify.	13:10:34
14		So you may recall that Figure 2	13:10:40
15		illustrates word line contacts 22, which are	13:10:43
16		connected to the word line layers 12a through 12p.	13:10:49
17		Is that correct?	13:10:54
18	A	That's correct, to the extent that they	13:11:03
19		only show three contact trenches, yeah, three on	13:11:07
20		each side, yes.	13:11:12
21	Q	But presumably there would be word line	13:11:13
22		contacts, even if not illustrated, connected to each	13:11:19

1	of the word line layers?	13:11:23
2	A I think that's fair.	13:11:24
3	Q And each word line layer extends in what	13:11:28
4	is illustrated as the -- I guess it's the Y plane or	13:11:40
5	the YX plane and intersects with the channel	13:11:45
6	structures 18. Is that correct?	13:11:52
7	A I believe that that's one -- one	13:11:58
8	description, yes, that's correct.	13:12:02
9	Q And is it accurate to say that every	13:12:04
10	location where the word line layer intersects with a	13:12:14
11	channel structure it is forming a transistor?	13:12:19
12	MR. HSU: Objection; form.	13:12:25
13	A I think the -- as shown in the Figure 2,	13:12:35
14	every time the word line or the word line layer we	13:12:39
15	mentioned also is a gate layer, you will encapsulate	13:12:44
16	or intersect and encapsulate the strings. And when	13:12:54
17	they -- when such formation happens, you either form	13:13:00
18	a memory cell or you form the select transistor.	13:13:09
19	So I just want to make sure that when we	13:13:19
20	use the word "transistor," transistor in general	13:13:22
21	should also include memory cells as well as just	13:13:25
22	regular transistor that doesn't store data. Memory	13:13:29

1 cell, of course in the case of NAND, the memory cell
2 that store data, its behavior it's that of a
3 transistor but with perhaps modulated or programmed
4 threshold voltage.

5 Q And the gate terminal of a memory cell,
6 how do you understand that term?

7 MR. HSU: Objection; asked and answered.

8 A I think different people have different
9 descriptions. But if you look at a schematic of a
10 transistor, for example, as I have shown in my reply
11 declaration, and also we can look at Figure 3, and
12 for each transistor there will be we call it a
13 terminal or node just meaning just for us to have a
14 reference to point to that electrical function or
15 how the -- how the device behaves. So you have
16 drain terminal, you have gate terminal, and you have
17 source terminal.

18 Now, so when you want to say can you point
19 me or physically point me, there's no -- not
20 necessarily a specific physical point or zero
21 boundary type of concept. It's just that physically
22 there's a layer, the word line layer that act as a

1 gate layer that encapsulate a channel string. So in 13:15:26
2 that case you'll form a transistor, and in the 13:15:32
3 transistor you will have a drain node, you will have 13:15:34
4 a source node and you will have a gate node, and you 13:15:40
5 can call it gate terminal, you can call it drain 13:15:44
6 terminal, you can call it source terminal. 13:15:48

7 For example, let's take a look at what we 13:15:51
8 just gone through in Figure 3 -- 13:15:55

9 Q Well, I just want to confirm very quickly, 13:15:57
10 when we're saying that there is a drain terminal, a 13:16:03
11 source terminal or a gate terminal, is the gate 13:16:09
12 terminal the same as a control gate, or is that a 13:16:14
13 different concept? 13:16:21

14 MR. HSU: Objection; asked and answered. 13:16:22

15 A Okay. So let's just put it this way. 13:16:28
16 Maybe I'll give one description. So I would say the 13:16:31
17 way perhaps I can clarify for you is that there are 13:16:40
18 electrical designation, there's also physical 13:16:46
19 designation, and there are also a circuit 13:16:53
20 schematic-wise designation. Okay. 13:16:58

21 So for Figure 3, if we look at Figure 3, 13:17:01
22 it's a schematic circuit designation, so you can 13:17:04

1 point to certain area and say this will be gate 13:17:08
2 terminal, this will be drain terminal, this will be 13:17:12
3 source terminal. And then there will also be 13:17:15
4 electrical designation, meaning that the function of 13:17:20
5 gate terminal is acting as a gate of that 13:17:24
6 transistor, meaning that to modulate the channel and 13:17:28
7 so that the current on the drain, electrical drain 13:17:32
8 and can flow to source. So that's electrical 13:17:37
9 designation. 13:17:44

10 And you have a physical designation, which 13:17:45
11 is that the word line layer is the gate layer, 13:17:49
12 physically is a gate layer, that's how you form it, 13:17:53
13 and you can see in Figure 2. And the bit line or 13:17:56
14 the drain of that string, bit line is really acting 13:18:00
15 as if you consider all the transistor, all the 13:18:03
16 memory cell and the transistor as a string of 13:18:06
17 transistor, the bit line is the top, the physical 18 13:18:09
18 that we just mention is really the bit line of that 13:18:16
19 string, whereas the 21, I believe it's 21 that we 13:18:20
20 just mentioned is acting as the source, the ACS of 13:18:24
21 the string. 13:18:32

22 So there is the electrical definition or 13:18:34

1 electrical designation to help understand the 13:18:36
2 function, and there's also physical designation to 13:18:40
3 see -- to make it physical you can see it, because 13:18:43
4 ultimately you got to make a physical transistor, a 13:18:49
5 physical memory cell, and then there's a schematic 13:18:52
6 designation. And sometime, you know, whether people 13:18:56
7 when they see things they may not be a string chain, 13:18:59
8 they may be convoluted a little bit. 13:19:04

9 But suffice to say in the context of 13:19:08
10 Figure 3, in the context of Figure 2, in the context 13:19:08
11 of '957, word line layer is the gate layer, and word 13:19:13
12 line will act to form the gate of the transistor. 13:19:16
13 And as such, a transistor having a gate will 13:19:19
14 therefore having a gate terminal in the circuit 13:19:25
15 schematic that you can point to. 13:19:28

16 Q So in Figure 2, let's focus in on the 13:19:32
17 intersection between structure 18, the channel 13:19:37
18 structure, and the word line layer 12c. Actually, 13:19:43
19 let's do 12b. 13:19:50

20 A 12b, okay, that's the -- okay. All right. 13:19:52

21 Q So in that figure, Figure 2, where is the 13:19:57
22 gate of the memory cell formed? 13:20:13

1	A	Can you repeat your question? I'm not	13:20:30
2		sure that's even -- I'm not the question has a --	13:20:32
3		(Simultaneous speaking.)	13:20:32
4	Q	Let's approach this a little differently	13:20:38
5		because I'm trying to understand something, and, you	13:20:41
6		know, for some reason I'm not really understanding	13:20:43
7		it well.	13:20:45
8		So you agree that there is a transistor,	13:20:47
9		which could be a memory cell or a select gate, that	13:20:50
10		is formed every time a word line layer intersects	13:20:54
11		with a channel structure. Is that correct?	13:20:59
12	A	That's one characterization of it, I can	13:21:02
13		accept that, yes.	13:21:04
14	Q	And you agree that every transistor would	13:21:05
15		have a gate. Is that correct?	13:21:15
16	A	Yes, electrically it will have a gate to	13:21:23
17		modulate, to activate or to function that	13:21:25
18		transistor, yes.	13:21:30
19	Q	And that gate is also referred to as a	13:21:30
20		control gate. Is that correct?	13:21:33
21	A	In the context in my testimony I'm using	13:21:35
22		the control gate in the sense that gates functioning	13:21:40

1 is to control. So let's just use the term "control
2 gate" so that it's for the intent that we can
3 include the BST and TST in it, just so for the
4 simplicity so I don't have to each time demarcate
5 control gate from memory cell and just gate for
6 selection system, I'm using that to simplify our
7 discussion, yeah.

8 Q Now, is the control gate receiving voltage
9 through the word lines?

10 A I think we're now crossing the different
11 ground, different designation. Can you repeat your
12 question? Is a control?

13 Q Are the control gates of the memory cells
14 receiving voltage through the word line layers?

15 A In the context of '957 along with the
16 context of what '957 understood based on the
17 reference it has cited, the word line after
18 receiving the voltage supply through the X decoder
19 the word line is equipotential, word line has the
20 same potential, that word line crosses many of the
21 strings, and that word line, whatever word line
22 voltage will be the voltage of the gate with the

1 memory cell or the transistor that it intersects, in 13:23:11
2 our discussion intersects. So the word line voltage 13:23:15
3 will be the voltage of the gate of the memory cell 13:23:18
4 that it intersect, in that sense, yes. 13:23:21

5 Q Will that voltage be the same as the 13:23:28
6 voltage of the word line contact that connects to 13:23:30
7 the word line? 13:23:33

8 MR. HSU: Objection; asked and answered. 13:23:35

9 A I believe I answered this earlier. There 13:23:39
10 is -- there is voltage coming in through the 13:23:47
11 voltage-generating circuit and decoder going through 13:23:49
12 this 22, this contact through the word line. And 13:23:53
13 there may be, as we see in '957 and also in 13:23:58
14 literature, due to the resistance of the path in 13:24:04
15 delivering the voltage, which is much greater than 13:24:10
16 this 22 contact, due to that, the voltage on the 13:24:14
17 voltage-generating circuit may not reflect it right 13:24:21
18 away onto this equipotential plane of word line. 13:24:28

19 But when the equipotential the word line 13:24:33
20 is reached, there's no current flow because it's a 13:24:38
21 capacitor plane. So 22, the word line contact, word 13:24:42
22 line layer contact is same potential as the word 13:24:48

1 line, and the word line, the control gate layer or 13:24:51
2 word line layer is equipotential. 13:24:55

3 Q So when you say when the potential of the 13:24:59
4 word line is reached, what about beforehand? 13:25:01

5 A Again, it's just like charging a 13:25:09
6 capacitor, the capacitor plane is equipotential, but 13:25:13
7 it takes charges or current from the voltage 13:25:18
8 generator circuit, I believe this is in my reply 13:25:22
9 declaration, to charge that equipotential plane. 13:25:27

10 So to that extent, even then because the 13:25:30
11 resistance of the path is going to be much greater 13:25:37
12 than the resistance of the contact to the first 13:25:41
13 order, the voltage, let's just for the sake of 13:25:49
14 argument, let's pick the one you just said 12b, 13:25:55
15 correct, okay. 12b. 13:25:59

16 Q Sure. 13:26:03

17 A 12b is always equipotential, as it's being 13:26:03
18 charged up it's equipotential, okay, same potential 13:26:08
19 gate layer. And right at the top service of 22 as 13:26:12
20 it's being charged there may be some doing the 13:26:16
21 charging because the displacement of the current is 13:26:19
22 so small, it's very small. You may have a little 13:26:21

1 bit, very tiny, if any at all, voltage difference at 13:26:24
2 the top of the service of 22 versus the 13:26:31
3 equipotential plane of 12b. But that doesn't change 13:26:34
4 the fact that the 12b itself is equipotential plane. 13:26:39

5 Q You say there's some very small 13:26:44
6 displacement current and a very small voltage 13:26:48
7 difference between 22, which is the contact, and the 13:26:51
8 plate 12b. Is it possible that there's some small 13:26:58
9 voltage difference between the ends of the plate 13:27:02
10 12b? 13:27:05

11 A In the context of '957 and what '957 13:27:13
12 trying to solve, and in the context of what '957 is 13:27:18
13 referring to, the word line layer 12b is considered 13:27:22
14 to be equipotential because it's trying to solve 13:27:29
15 another problem, another issue which is much bigger 13:27:34
16 issue of the voltage going from voltage generator 13:27:38
17 generation circuit to the word line. So '957 is 13:27:44
18 very clear that in the -- in what it's teaching. 13:27:51

19 Q So how would you define a word line, the 13:28:04
20 term "word line"? 13:28:16

21 MR. HSU: Objection; form. 13:28:19

22 A Can you point me to where in my reply 13:28:21

1	declaration I'm defining "word line"?	13:28:24
2	Q Let me rephrase. Is the term "control	13:28:27
3	"gate" identical to the term "word line"?	13:28:32
4	A I believe I answered your -- your question	13:28:36
5	already. There's a physical realm, there's a	13:28:47
6	electrical realm designation, and there's a	13:28:54
7	schematic designation. Okay.	13:28:57
8	Obviously, in the context of '957, if we	13:29:01
9	looked at the figure, Figure 3 in conjunction of	13:29:04
10	looking at BSG, WL0, WLn-1 and WLn all the way to	13:29:10
11	TSG, it's very clear that the using word line, the	13:29:20
12	term "WL," word line as designation for gate. So	13:29:25
13	that's -- I mean, to the extent I can answer your	13:29:31
14	question based on Figure 3 we just discussed, we	13:29:34
15	have been discussing for a long time.	13:29:39
16	Q What about for a POSITA more generally	13:29:40
17	does the term "control gate" mean the exact same	13:29:43
18	thing as the term "word line"?	13:29:46
19	A I believe I opined on that, and I think in	13:29:48
20	the reference, at least the reference cited, and	13:29:51
21	also in the -- in the way the '957 patent is	13:29:56
22	structured between the specification and the claim.	13:30:05

1 Let me go to my -- my declaration.

13:30:10

2 Q We can go there in a second. I just want
3 your opinion because I'm trying to get a straight
4 yes or no answer, and maybe there is none, but does
5 the term "control gate" mean the same thing as the
6 term "word line"?

13:30:14

13:30:17

13:30:19

13:30:22

13:30:25

7 MR. HSU: Objection; form.

13:30:27

8 Q In your opinion as a POSITA.

13:30:31

9 A In the opinion of POSITA, and since we're
10 talking about also '957, I cannot speak for other
11 people, but in my position as a POSITA and looking
12 at the context of '957 and looking at going through
13 what we just discussed including Figure 3, word line
14 is same as gate in the context '957.

13:30:39

13:30:43

13:30:46

13:30:50

13:30:52

13:30:57

15 Q If they're the same, could you ever say
16 that the gate is receiving voltage through a word
17 line?

13:31:05

13:31:09

13:31:11

18 MR. HSU: Objection; form.

13:31:11

19 A Can you point me to where the context of
20 gate receiving voltage through a word line?

13:31:13

13:31:18

21 Q So, for example, in '957, let's go to
22 column 8 lines 50 through 55.

13:31:27

13:31:37

1	A	Okay.	13:31:53
2	Q	It says at the bottom of that section --	13:31:54
3		well, how about you read it out to me, what is the	13:32:01
4		final sentence there?	13:32:04
5	A	"Thus, gate voltage can be applied on gate	13:32:05
6		of the memory cell through the word line contacts	13:32:09
7		that are coupled to the word line layers.	13:32:14
8	Q	Would you agree that the term "gate" is	13:32:18
9		distinct from a word line contact?	13:32:20
10	A	The gate is distinct from word line	13:32:28
11		contact just like word line contact is distinct from	13:32:40
12		word line.	13:32:43
13	Q	Would you agree that the term "gate" is	13:32:43
14		distinct from word line?	13:32:45
15	A	I disagree. I think the gate is word	13:32:47
16		line. The gate layer is word line layers and a gate	13:32:52
17		is word line, so that the sentence has a physical	13:32:55
18		description, physical and also electrical.	13:33:02
19	Q	So you're saying that this is equivalent	13:33:07
20		to saying the gates of the memory cells -- let's	13:33:11
21		reset. Let me clarify.	13:33:17
22		You're saying that the gate of the memory	13:33:19

1	cell is the same as the word line?	13:33:21
2	A That's what Figure 3 is showing. I'm	13:33:29
3	simply pointing to Figure 3.	13:33:32
4	Q Is that what's being described in this	13:33:35
5	paragraph?	13:33:38
6	A I don't see any contradiction.	13:33:39
7	Q Do you agree that the paragraph recites a	13:33:48
8	gate of the memory cell and then separately recites	13:33:50
9	a word line contact and then separately recites a	13:33:54
10	word line layer?	13:33:57
11	A It's consistent because word line layers	13:34:01
12	is same as gate layers, and gate is same as word	13:34:04
13	line, and then word line contact is a separate	13:34:07
14	entity that contacts the word line or contacts the	13:34:11
15	gate.	13:34:13
16	Q Let's go to paragraph -- let's go to	13:34:20
17	column 9 lines -- let's see. Let's do 23 through	13:34:23
18	30. Can you read that out loud for me, that	13:34:35
19	section?	13:34:46
20	A You mean "During the operation"?	13:34:46
21	Q Yes, beginning there to the end of the	13:34:49
22	paragraph.	13:34:51

1	A	"During operation of device 100,	13:34:51
2		appropriate voltage could be applied to the bit	13:34:53
3		lines 308A and 308B, the gates of TST 306A and 306B	13:34:56
4		through the sub-TSG layers," and it has a whole	13:35:06
5		bunch of number 12p-1, "the gates of the memory cell	13:35:10
6		304A and 304B through the word line layers." Do you	13:35:15
7		want me to continue?	13:35:21
8	Q	Sure.	13:35:22
9	A	"The gates of the BST 302A and 302B	13:35:23
10		through the sub-BSG layers and ACS through the slit	13:35:28
11		structure. "	13:35:33
12	Q	Would you agree that in this section it is	13:35:35
13		describing the gates of the memory cells 304A as	13:35:38
14		distinct from the word line layers?	13:35:42
15	A	Repeat your question again.	13:35:47
16	Q	Would you agree that in this paragraph it	13:35:48
17		distinguishes the gates of the memory cells 304A and	13:35:53
18		304B with the word line layers?	13:35:59
19		MR. HSU: Objection; form.	13:36:04
20	A	Again, as I answered earlier, with respect	13:36:06
21		to column 8 --	13:36:08
22	Q	I'm asking about column 9.	13:36:12

1 A I know. I know. So gate layer is same as 13:36:14
2 word line layer, that's physical, so we're talking 13:36:17
3 about electrical realm and then physical realm and 13:36:20
4 circuit realm, okay. But gate is equal to word line 13:36:25
5 and the gate layers is corresponding to word line 13:36:28
6 layers and the contact on other physical structures, 13:36:31
7 so I don't see any -- yeah. 13:36:37

8 Q I'm sorry. So here it says the gates of 13:36:39
9 the memory cells are receiving voltages through the 13:36:44
10 word line layers. Do you agree? 13:36:49

11 A Again -- 13:36:57

12 MR. HSU: Objection; form. 13:36:57

13 A Sorry. Again, the gate referring to 13:36:58
14 electrical and then word line layers physical, 13:37:02
15 obviously the gate contact connect physically to the 13:37:05
16 word line layer, and that word line layer is 13:37:09
17 electrically the word line which electrically is the 13:37:15
18 gate. So I don't see any -- any contradiction. 13:37:18

19 Q So the term "gate" is an electrical term 13:37:22
20 and the term "word line" is a physical term. Is 13:37:27
21 that what you're saying? 13:37:31

22 A No. I'm saying that in order to help you 13:37:32

1 help the POSITA to understand the gate and word line 13:37:39
2 as shown in Figure 3 clearly they are the same okay. 13:37:45
3 But physically there's a gate layer or word line 13:37:48
4 layers that are made of conductive material, gate 13:37:53
5 layer, word line layers. And this gate layer word 13:37:57
6 line layer physically they are connected to word 13:38:00
7 line contact so that the voltage from the 13:38:08
8 voltage-generating circuit outside world can come in 13:38:13
9 through the gate -- I'm sorry, through the contact. 13:38:19
10 So I don't -- I think we -- I explained 13:38:25
11 this many times already. So it's gate is same as 13:38:28
12 word line, and gate layers is same as word line 13:38:33
13 layer. Perhaps they use that designation to, even 13:38:37
14 though they may want to convey the same thing, but 13:38:39
15 it's more of a physical, it's a layer, just like 12b 13:38:43
16 just one of 12 -- the layer -- hang on a second -- 13:38:47
17 in Figure 2 like 12a, 12b, 12c layers, okay, and 13:38:51
18 then so it's just designation. 13:38:57
19 I think I answered this question many 13:39:05
20 times already. 13:39:07
21 Q Well, I'm -- I'm trying to understand if a 13:39:08
22 gate is the same physical structure as a word line, 13:39:17

1	or if the gates are connected to the word line	13:39:21
2	layer.	13:39:27
3	MR. HSU: Objection; asked and answered.	13:39:31
4	A Again, my answer is the gate is same as	13:39:37
5	word line, gate layer same as word line layer, and	13:39:43
6	then you have gate contact that physically connects	13:39:49
7	or physically touches connect or couple to the word	13:39:53
8	line layer or the gate layer.	13:39:56
9	Q What distinguishes a word line and a word	13:39:58
10	line layer?	13:40:01
11	A As I mentioned already, it has connotation	13:40:03
12	such that the word line layer is more physical,	13:40:20
13	because going back to -- going back to the figure in	13:40:23
14	Figure 3, we mentioned that, for example, MCn, each	13:40:28
15	of the MCn has WLn as its gate, okay. But that WLn	13:40:32
16	physically or materially speaking physically is a	13:40:43
17	layer that crosses the string 308A, 300A and 300B.	13:40:48
18	So there's a gate -- there's a word line layer or	13:40:55
19	the gate layer that intersect or crosses, whatever	13:40:58
20	you want to say, or encapsulate the string, and when	13:41:04
21	they encapsulate the string, that word line layer,	13:41:08
22	physical word line layer, the material act as a gate	13:41:12

1 of that string. And also by acting as a gate of
2 string, acting as a word line of string and acting
3 as a gate of the string, okay. So and then that
4 word line layer is contacted by a word line contact.
5 It's very straightforward on Figure 2 and Figure 3.

6 Q I'm trying to understand if the term
7 "control gate" and the term "word line" mean the
8 same thing or if they are -- if they have different
9 connotations.

10 MR. HSU: Objection; asked and answered.

11 A In the context of '957, in the context of
12 what we just went through with many question on
13 Figure 3, it's clear that gate and word line are
14 used to designate the same thing, that is the
15 electrical -- that is the -- designate the same
16 thing, word line and gate are the same thing.

17 Q What about outside the '957 context, more
18 generally, does the term "control gate" mean the
19 same thing as a word line?

20 A As we see from the reference also in my
21 reply declaration, and if you have some -- some
22 other -- if you have -- if you have a specific point

13:41:19

13:41:26

13:41:30

13:41:34

13:41:37

13:41:40

13:41:44

13:41:49

13:41:54

13:41:57

13:41:59

13:42:06

13:42:10

13:42:15

13:42:19

13:42:23

13:42:25

13:42:30

13:42:33

13:42:37

13:42:40

13:42:43

1 to point to, yes, outside the context, especially in 13:42:45
2 the reference '957 cited word line and contact -- 13:42:50
3 word line and gate are also the same. 13:42:55

4 Q So would a reference say something like 13:42:58
5 you can apply a signal to a control gate that is 13:43:01
6 connected to the word line -- 13:43:04

7 (Simultaneous speaking.) 13:43:12

8 MR. HSU: Objection; form. 13:43:12

9 (Court Reporter clarification.) 13:43:14

10 Q Sure. Let me rephrase. If they are the 13:43:14
11 same thing, what does it mean to say that a control 13:43:21
12 gate is connected to a word line? 13:43:29

13 A Can you point me to the context? Can you 13:43:43
14 point me to the reference? Because I would like to 13:43:46
15 see the context. 13:43:52

16 Q Let's go back for one second to column 9, 13:44:02
17 lines 23 through 30, where it said, quote, "The 13:44:09
18 gates of the memory cells 304A and 304B," are being 13:44:15
19 applied with the voltages, quote, "through the word 13:44:27
20 line layers, e.g., 12b through 12-o" or 12 -- 13:44:30

21 A I'm not seeing where you are. I'm not 13:44:36
22 seeing where you are. Can you show me where you are 13:44:39

1	again? I'm sorry.	13:44:42
2	Q Yeah. So right now column 9, I'm reading	13:44:43
3	now from lines 27 and 28 --	13:44:47
4	A I thought you said 24, yeah. 27, okay.	13:44:52
5	Q 24 is the beginning of the sentence.	13:44:54
6	A Okay.	13:44:57
7	Q Okay. It's a long sentence. But it says,	13:44:58
8	starting from 24, "During operation of the device,	13:45:02
9	appropriate voltages can be applied to," and then	13:45:07
10	dot dot dot, "the gates of the memory cells 304A and	13:45:12
11	304B through the word line layers (e.g., 12b to	13:45:18
12	12o.)" Do you see that?	13:45:25
13	A Yes, I do.	13:45:32
14	Q And I'm trying to understand what the	13:45:35
15	distinction is between the control gates of the	13:45:40
16	memory cells 304A and 304B and the word line layers	13:45:47
17	12b and 12o.	13:45:55
18	MR. HSU: Objection; form.	13:46:08
19	A Again, this whole thing is clear in the	13:46:17
20	context that gate the same as word line and gate	13:46:22
21	layers the same as word line layers.	13:46:27
22	Q And what was the distinction between word	13:46:36

1	line and word line layer?	13:46:39
2	A As I mentioned, word line layers is	13:46:47
3	physically to show that it's a whole plane,	13:46:54
4	equipotential plane, okay, and word line itself	13:46:58
5	could just mean in the context just be the gate	13:47:01
6	based on Figure 3, and whereas word line layer is	13:47:07
7	the plane that intersect many, many strings and form	13:47:11
8	it.	13:47:15
9	Q So you're using the term -- sorry. So	13:47:15
10	you're using the term "word line" to meaning a	13:47:18
11	portion of a word line layer. Is that correct?	13:47:21
12	MR. HSU: Objection; misstates prior	13:47:25
13	testimony.	13:47:30
14	A That's not what I said. Okay. I said it	13:47:30
15	very clearly that in the context of '957 if we look	13:47:33
16	at Figure 3 and in the context of what we just read,	13:47:38
17	word line layers and gate layers --	13:47:41
18	Q Stop. You're distinguishing now word line	13:47:46
19	layers and gate layers. I'm asking about you said	13:47:49
20	-- and tell me if this is correct and you can	13:47:56
21	correct me if I'm wrong -- that the distinction --	13:47:58
22	that gates are similar to word lines and gate layers	13:48:03

1	are similar to word line layers, and that was your	13:48:07
2	explanation for this portion of paragraph 9. Am I	13:48:12
3	incorrect about that?	13:48:15
4	MR. HSU: Counsel, I would appreciate if	13:48:17
5	you let Dr. Liu finish his answer.	13:48:19
6	A Can you repeat your question again,	13:48:21
7	please.	13:48:23
8	Q Sorry. One second. So my original	13:48:25
9	question is I was trying to understand the	13:48:47
10	distinction as stated in column 9 between the gates	13:48:49
11	of the memory cells and the word line layers.	13:48:55
12	A Okay.	13:49:10
13	Q And your response is that in the context I	13:49:16
14	believe you said that gates are the same as word	13:49:24
15	lines and gate layers or control gate layers are the	13:49:28
16	same as word line layers. Is that correct?	13:49:34
17	A No. We have to -- we have to go through	13:49:40
18	the context. As I -- as I throughout my testimony,	13:49:45
19	and we start with Figure 2, there's a physical	13:49:49
20	cross-section, and you asked about 12a, 12b, those	13:49:56
21	are -- in the patent those are called word line	13:50:02
22	layers as in contrast to insulating layer. So those	13:50:06

1 are physical, that's what I'm trying to mention, 13:50:10
2 physical material. And then there's an electrical 13:50:13
3 designation, which is word line, and there's a 13:50:19
4 schematic designation because you brought out the 13:50:23
5 terminal, and I'm trying to tell you nodes, 13:50:27
6 n-o-d-e-s, different nodes. And so in the contacts 13:50:29
7 of what we went through the flow going from Figure 2 13:50:34
8 to Figure 3 in that contact I'm simply testifying 13:50:38
9 that according to Figure 2, you have a word line 13:50:43
10 layers, and that word line layers is physical, and 13:50:47
11 you have word line, which connect electrically as 13:50:54
12 the gate, the word line and gate are the same. 13:51:00

13 So, therefore, since you have physical 13:51:04
14 word line layer, you have electrical word line and 13:51:06
15 physical, according to Figure 3, show clearly that 13:51:11
16 word line and gate are synonymous, are the same. 13:51:15
17 Therefore, I mention gate layer also to denote a 13:51:20
18 physical thing same as word line layer. 13:51:25

19 So again, let me go back again, going from 13:51:28
20 the flow of Figure 2 in the context of '957 and 13:51:32
21 Figure 3, you have gate equal to word line, and you 13:51:38
22 have word line layer, which is a physical layer that 13:51:40

1 will, for lack of a better word to describe it, I 13:51:43
2 don't want to define it, but lack of a better word 13:51:45
3 that will constitute the word line of the memory 13:51:49
4 cell, and you have -- you mentioned, you introduced 13:51:52
5 the word gate terminal. I'm trying to tell you that 13:51:55
6 a POSITA will know that in the schematic case you 13:51:58
7 have terminal bit line, source line and gate 13:52:02
8 terminal. So everything is consistent. 13:52:06
9 I don't -- I don't -- I have answered 13:52:08
10 repeatedly already and I think that's -- that's the 13:52:12
11 same answer I'm going to give. 13:52:17
12 Q Okay. 13:52:17
13 A Consistent in the context of Figure 2, 13:52:20
14 because you asked me to -- you went through Figure 2 13:52:22
15 column 8 to 18 word line layers, this is referring 13:52:27
16 to Figure 2, which is a physical material, because 13:52:31
17 it's saying alternating with insulating layer and 13:52:35
18 you have physical contact, which is 22. 13:52:37
19 So we are talking about different 13:52:40
20 designations, different realm. And I think it's 13:52:43
21 very clear that suffice to say word line layers are 13:52:46
22 electric -- what will constitute electrically as the 13:52:53

1	word line and word line and gate are synonymous in	13:52:58
2	the context of Figure 3 and in the context of	13:53:02
3	specification jumping to the claim. So I believe	13:53:06
4	everything is consistent.	13:53:09
5	Q Which portion of the word line layer	13:53:12
6	corresponds to the word line which you equate with	13:53:16
7	the term "gate"?	13:53:20
8	A Repeat your question.	13:53:25
9	Q So you said that the word line layer is a	13:53:28
10	physical designation and that word line is an	13:53:33
11	electrical designation. Is that correct?	13:53:38
12	A In the context we just mentioned about	13:53:45
13	going from Figure 2 to Figure 3.	13:53:49
14	Q Okay. I'm trying to understand, going	13:53:51
15	back to Figure 2, which portion of the word line	13:53:57
16	layer corresponds to that electrical word line.	13:54:03
17	MR. HSU: Objection; form.	13:54:10
18	A Can you point specifically to something?	13:54:17
19	I'm not -- I'm having -- because I think -- I think	13:54:19
20	there may be some disconnect between maybe my	13:54:23
21	understanding and perhaps your understanding. So I	13:54:27
22	apologize, maybe I'm not --	13:54:30

1	Q	Sure. So if you go back to Figure 2,	13:54:33
2		you'll see that there's a word line layer 12b.	13:54:37
3	A	Okay.	13:54:49
4	Q	And then you'll see that there is a	13:54:50
5		channel structure 18.	13:54:56
6	A	Okay.	13:54:59
7	Q	And as we decided before, or we agreed	13:54:59
8		before, there's going to be some type of transistor,	13:55:05
9		like a memory cell formed at the intersection	13:55:10
10		between 12b and 18. Is that correct?	13:55:12
11	A	I'd say that's fair, yes.	13:55:15
12	Q	And you have said that there is a	13:55:22
13		distinction between the term "word line" layer and	13:55:24
14		word line. Is that your position?	13:55:26
15	A	I don't -- I don't think I used a	13:55:30
16		distinction, the word "distinction." I'm saying	13:55:34
17		that in the context we just read from the	13:55:37
18		description of Figure 2 and Figure 3, word line	13:55:40
19		layers are used to correspond to refer to Figure 2,	13:55:44
20		a physical layer as you just mentioned 12b, whereas	13:55:49
21		word line is used in the Figure 3, the schematic of	13:55:53
22		the memory cell as the gate of a particular memory	13:55:59

1 cell, respective memory cell. 13:56:05

2 Q So I apologize, is there a distinction 13:56:11

3 between word line layer and word line as 13:56:14

4 terminology? 13:56:17

5 A I don't know what you meant by 13:56:22

6 distinction. Again, I've testified for the past 13:56:24

7 couple hours, okay, so word line layer is, in the 13:56:28

8 context of Figure 2, is an equipotential conductive 13:56:32

9 layers, so that's, for example, 12b, along with 12a, 13:56:38

10 b, c, okay. 13:56:46

11 Q Okay. 13:56:47

12 A So that's a word line -- physical -- 13:56:48

13 that's a word line layer use that in the context of 13:56:50

14 introducing the context of Figure 2 that you 13:56:52

15 introduce also, the patent introduce and you 13:56:55

16 introduce in this deposition, so that's a physical 13:56:58

17 layer we can see from Figure 2 cross-section. 13:57:01

18 Q Okay. 13:57:03

19 A And then in Figure 3 you have this word 13:57:04

20 line and that is used to denote a gate because you 13:57:07

21 have BSG, bottom select gate, and TSG, top select 13:57:12

22 gate, and you have all these word line, WLo all the 13:57:16

1	way to M+1, greater M+1. So these are the gate or	13:57:20
2	the word line, in that context those are gate and	13:57:25
3	those are the context of Figure 3. Okay.	13:57:29
4	So now your question is in this figure --	13:57:33
5	I'll let you ask the question because I don't -- I	13:57:36
6	don't pretend to --	13:57:39
7	Q No, I'm just trying to understand does it	13:57:41
8	designate a gate or does it designate a word line	13:57:43
9	connected to the gate?	13:57:46
10	MR. HSU: Objection; form.	13:57:49
11	A Does what designate? I don't understand	13:57:52
12	the question, I'm sorry.	13:57:54
13	Q Yeah. So you said that in Figure 3 you	13:57:55
14	have a word line which is used to denote a gate, and	13:58:00
15	so I'm trying to understand the relationship between	13:58:07
16	Figures 2 and 3. Is Figure 3 saying that the word	13:58:11
17	line is a gate or is it saying that the word line is	13:58:15
18	connected to the gate?	13:58:18
19	A Figure 3 is saying that word line is the	13:58:24
20	gate. But you have to understand that we're talking	13:58:30
21	-- again, I used the word "realms" to try to be --	13:58:33
22	to try to help us understand. Word line layer, that	13:58:37

1 physical layer, that equipotential layer will get 13:58:41
2 its voltage through, as we read, through the word 13:58:46
3 line contact, and once it has the voltage, because 13:58:49
4 this word line layer surrounds the channel, this 13:58:53
5 voltage will act as the control signal acting as the 13:59:00
6 gate or acting as the word line or acting as the 13:59:06
7 gate to the memory cell. 13:59:10

8 So to the extent it's just straightforward 13:59:12
9 that you have a word line layer, which is physical, 13:59:14
10 that word line layer carry equipotential voltage 13:59:17
11 when it intersect, and when it act, it act as a gate 13:59:22
12 or word line voltage to modulate that memory cell. 13:59:26

13 So it's I think we're splitting -- 13:59:31
14 splitting hairs, we're splitting atom. Yeah, I 13:59:36
15 think it makes it very clear. So I'm sorry, go 13:59:38
16 ahead. 13:59:41

17 Q Well, you say it's very clear, but, you 13:59:41
18 know, the '957 patent distinguished the gate from 13:59:43
19 the word line layer you would agree. 13:59:49

20 A I don't know "distinguish" is the right 13:59:54
21 word. But it's the designating the physical realm 13:59:57
22 in the Figure 2 and you have electrical realm in 14:00:01

1 Figure 3.

14:00:04

2 But suffice to say, word line layer is the
3 gate layer and the word line is gate. And simply,
4 the word line layer has been imparted with the
5 voltage through the word line contact, that voltage
6 act as the gate voltage or the word line voltage to
7 modulate the memory cell.

14:00:05

14:00:10

14:00:12

14:00:16

14:00:21

14:00:25

8 Q So when you say that the word line is the
9 gate, that's the electrical realm. Is that correct?

14:00:29

14:00:35

10 A I'm using that word to help us understand,
11 yes.

14:00:40

14:00:43

12 Q And word line layer is the physical realm.
13 Is that correct?

14:00:43

14:00:46

14 A I'm using that to help explain Figure 2,
15 which are introduced and which you were the one who
16 introduce word line layer. I'm using that to try to
17 help us to facilitate understanding so we can have a
18 common basis for discussion.

14:00:47

14:00:51

14:00:54

14:00:57

14:01:02

19 Q To be clear, the '957 uses the term "word
20 line layer," you agree?

14:01:03

14:01:07

21 A '957 uses word line layer introduced in
22 Figure 2 as you pointed out, as you introduced to

14:01:08

14:01:13

1 denote that the structure -- to describe the 14:01:14
2 structure you have these word line layers sandwiched 14:01:17
3 by insulating layers. 14:01:21

4 Q And I'm trying to understand which portion 14:01:22
5 of the physical word line layer corresponds to the 14:01:24
6 gate shown in Figure 3 or the thing that you 14:01:33
7 referred to as the word line in Figure 3? 14:01:36

8 MR. HSU: Objection; asked and answered. 14:01:39

9 A Look, that designation or that distinction 14:01:45
10 you're trying to make is in a way irrelevant, 14:01:50
11 because the whole word line layer is equipotential. 14:01:53
12 So if you want to say it's at zero width as Dr. -- I 14:01:57
13 can't pronounce it, the other expert, Dr. Przybylski 14:02:01
14 -- I'm sorry. 14:02:05

15 Q Przybylski. 14:02:06

16 A Yeah, I'm messing up the name -- said zero 14:02:07
17 width. I don't think there's a distinction. The 14:02:11
18 distinction is that that place equipotential, so you 14:02:15
19 want to take it one millimeter away from where the 14:02:16
20 dielectric is or two nanometer, it doesn't matter. 14:02:19

21 The fact is that this word line layer 14:02:23
22 physical layer is equipotential and it carries the 14:02:26

1 voltage that act as the gate when it intersects the 14:02:29
2 memory cell, intersect the channel. 14:02:33

3 So to ask to point is there a distinction, 14:02:36
4 I -- there's electrical and there's a physical, 14:02:39
5 physical word line layer that carries equipotential 14:02:45
6 gate voltage to the transistor, and it receive that 14:02:49
7 voltage through the word line contact, as we 14:02:54
8 mention, via the power supply or via the voltage- 14:02:58
9 generating circuit through the X decoder, because 14:03:01
10 this is word line through the word line decoder. 14:03:04

11 So again, word line layers are -- in the 14:03:07
12 context of Figure 2 are the physical and they carry 14:03:12
13 a voltage, and that voltage is the gate voltage to 14:03:16
14 the memory cell. Therefore, you have word line 14:03:21
15 being the gate and you have word line layer. 14:03:25

16 Q Okay. So would you say that in the view 14:03:31
17 of a POSITA, a word line layer is connected to a 14:03:33
18 control gate? 14:03:40

19 MR. HSU: Objection; form. 14:03:53

20 A When you say word line layer forms a 14:03:54
21 control gate -- 14:03:56

22 Q Is connected to a control gate. 14:03:57

1 A Connected, it's -- I don't even know the 14:03:59
2 term connected to the control gate. No, it's 14:04:03
3 equipotential plane, and that equipotential plane, 14:04:08
4 if I just have a plane word line layer sitting 14:04:12
5 equipotential plane, that -- that is just a layer, 14:04:17
6 you can call it word line layer or not. But when it 14:04:19
7 intersect a channel, it forms a transistor, that 14:04:23
8 word line -- physical word line layer with this 14:04:27
9 potential is the gate of that memory cell. 14:04:32

10 So it's whether it's a -- what's the word 14:04:35
11 you said? I don't -- I don't even think that -- 14:04:39
12 that there needs to be that distinction. This word 14:04:43
13 line layer, equipotential layer is the gate -- maybe 14:04:45
14 this will be easier to understand -- is the gate 14:04:49
15 layer for the memory device for that many strings, a 14:04:53
16 gate layer. So that gate layer will be acting, will 14:04:58
17 be -- because it has a voltage on it will be acting 14:05:03
18 as the gate to each of the string that it 14:05:06
19 intersects. 14:05:09

20 Q When would a POSITA use the terms "control 14:05:11
21 gate" and "word line" differently? 14:05:17

22 A I would have to see the specific context. 14:05:23

1 I don't -- I mean, I'm analyzing with respect to 14:05:26
2 '957 and its -- its prior art reference, along with 14:05:29
3 other reference, and at least in the context of 14:05:34
4 other reference and cited by '957 the word line and 14:05:36
5 control gate are used synonymously. 14:05:40

6 And if you want to have any other context, 14:05:44
7 I will be happy -- I mean, I will look at it, but I 14:05:47
8 might not be able to opine on it because I already 14:05:50
9 render my opinion based on the '957 patent and the 14:05:54
10 reference that the '957 patent cited, which, to me, 14:05:57
11 assume that '957 -- if '957 did not distinguish in 14:06:00
12 the specification, hey, look, I used word line and 14:06:05
13 control gate different from the reference, you know 14:06:08
14 I believe Exhibit 1030 is different from the exhibit 14:06:10
15 I cited, I want to make that clear, no, '957 is 14:06:12
16 silent, therefore, '957 agrees with the reference 14:06:18
17 cited, including 1097, which clearly and also with 14:06:22
18 this Figure 2 and Figure 3, along with the 14:06:25
19 specification jumping to the claim that control gate 14:06:28
20 and word line are the same. 14:06:32

21 Q Are the two terms ever used differently? 14:06:33

22 MR. HSU: Objection; form. 14:06:38

1 A Again, you have to show me the citation or 14:06:40
2 the context. But, again, in the context of '957, in 14:06:50
3 the context of understanding of POSITA with respect 14:06:55
4 to the context of '957 and the problem it's trying 14:06:57
5 to solve, along with the prior art reference '957 14:07:00
6 refers to, along with what is known by the POSITA at 14:07:04
7 the time of invention, in totality, not in the '957 14:07:08
8 context, in this IPR context the word line and 14:07:13
9 control gate are synonymous. 14:07:16

10 Q More generally in the understanding of a 14:07:21
11 POSITA, are the terms "control gate" and "word line" 14:07:23
12 ever used differently? 14:07:30

13 MR. HSU: Objection; form. 14:07:33

14 A I cannot control how other people use 14:07:37
15 different terms okay, so. But in my knowledge as a 14:07:41
16 POSITA in the context of '957 and going through the 14:07:45
17 reference of '957 and going through the classic 14:07:49
18 textbook of Micheloni and Aritome in this, it is 14:07:53
19 my -- the opinion I rendered that to a POSITA that 14:07:59
20 word line and control gate are the same. And if 14:08:05
21 somebody out of blue out of context, out of 14:08:07
22 somewhere, and if you have that reference I'll be 14:08:10

1	happy to look at it and understand it.	14:08:13
2	But, again, I, as a POSITA sitting right	14:08:14
3	here, for this IPR given the reference -- given	14:08:18
4	understanding the word line and control gate are the	14:08:24
5	same, it's very, very -- it's not correct in this	14:08:26
6	context to say that we can -- we can go through '957	14:08:33
7	much more, there's much more detail. It's not	14:08:37
8	correct to say that there's a difference between	14:08:40
9	so-called the voltage on the gate versus word line	14:08:42
10	voltage, I think that --	14:08:46
11	Q Let's -- sorry. I'll let you finish if	14:08:50
12	there's anything more you want to say.	14:08:54
13	A Yeah, I just think that in the context	14:08:57
14	it's very clear that as a POSITA word line and gate	14:09:00
15	are the same, so.	14:09:02
16	Q Now, I just want to clarify something.	14:09:03
17	You said that there's no difference between the	14:09:05
18	voltage on the gate versus the voltage on the word	14:09:11
19	line.	14:09:16
20	MR. HSU: Objection; form.	14:09:21
21	Q Is that distinct from saying there's no	14:09:22
22	difference between a gate and a word line?	14:09:27

1	MR. HSU: Same objection.	14:09:34
2	A I don't know how to is this a different	14:09:41
3	angle. Again, the word line layer is equipotential	14:09:44
4	layer is the gate layer, and when they intersect	14:09:47
5	with the string, it imparts this voltage as the gate	14:09:52
6	voltage, it's word line voltage and word line is the	14:09:58
7	gate and the word line to the memory cell. And	14:10:01
8	because it's equipotential, when it go through	14:10:05
9	different string, it's equipotential, the word line	14:10:08
10	plane is equipotential. So there's no distinguish.	14:10:13
11	And the patent certainly doesn't --	14:10:17
12	doesn't make a point to say, hey, when I talk about	14:10:20
13	the voltage on the word line and versus my claim,	14:10:25
14	the voltage on the gate, I don't think the '957 make	14:10:29
15	a point say, hey, look, I'm -- I'm going to go off	14:10:33
16	different from my reference. I know my reference	14:10:36
17	say the gate and word line are the same, but I'm	14:10:39
18	going to be different, because my specification is	14:10:42
19	one thing and my claim is going to be another thing.	14:10:44
20	'957 never mention that and never made that	14:10:48
21	demarcation or distinction. So again, word line is	14:10:50
22	gate.	14:10:53

1	Q	What about physically rather than	14:10:54
2		electrically, is there a physical distinction	14:10:56
3		between a gate and a word line?	14:10:59
4	A	In what context?	14:11:04
5	Q	Let's say just generally are those -- is	14:11:09
6		there ever a physical distinction between a control	14:11:14
7		gate and a word line?	14:11:18
8	A	I would have to see the context. When you	14:11:22
9		say -- when you people use the word "ever" or "all"	14:11:25
10		in those kind of things are very encompassing and I	14:11:29
11		would prefer to look at the context.	14:11:34
12	Q	So let me rephrase it then. Would you say	14:11:36
13		that the phrase "control gate" always means the same	14:11:39
14		thing as the term "word line"?	14:11:42
15	A	Again, always, again, I don't control how	14:11:47
16		people use it, but I'm here testifying that in the	14:11:50
17		context of IPR for '957 what my knowledge as POSITA	14:11:53
18		and with my experience and background and looking	14:11:59
19		through all the reference cited by '957 and looking	14:12:05
20		for -- at the background reference, background prior	14:12:09
21		art, word line is same as control gate in the	14:12:12
22		context of '957.	14:12:15

1	Q	So let me -- let me say beyond the '957,	14:12:17
2		just generally, does the term "control gate" always	14:12:22
3		mean the same thing as the term "word line"?	14:12:26
4	A	Look, I'm tasked to respond in my reply	14:12:28
5		declaration to the technical analysis of '957. You	14:12:33
6		can -- again, I don't control how other people would	14:12:40
7		convolute the term.	14:12:44
8		But, again, here, sitting here testifying	14:12:46
9		for my reply declaration, under the task of render	14:12:53
10		opinion for '957 and analyzing and render opinion	14:12:58
11		'957, along with the reference '957 cited which '957	14:13:03
12		accept as the understanding at the time of the	14:13:07
13		invention, and with my knowledge as POSITA, and with	14:13:10
14		all the background textbook reference, word line and	14:13:15
15		control gate -- word line and gate are the same.	14:13:20
16	Q	Is the term --	14:13:21
17	MR. HSU:	Sorry. Is there a good stopping	14:13:21
18		point? We've gone over an hour.	14:13:24
19	MR. BALBAKY:	Yeah, we'll stop very	14:13:27
20		shortly.	14:13:29
21	MR. HSU:	Okay.	14:13:31
22	BY MR. BALBAKY:		14:13:32

1	Q	Is there -- does the term "word line	14:13:32
2		layer" mean the same thing as control gate?	14:13:36
3	MR. HSU:	Objection; form.	14:13:43
4	A	I think I testified already that you	14:13:45
5		have -- you have -- you have parallel, you have	14:13:50
6		synonym, word line and gate are the same.	14:13:54
7		Therefore, word line layer and gate layers are the	14:13:59
8		same because they are referring to I would use the	14:14:01
9		word different realms, one is a physical realm, as	14:14:05
10		introduced by Figure 2 of '957, you have word line	14:14:10
11		layer, which is gate layer, and under that context	14:14:13
12		very clear that layer will when they intersect the	14:14:16
13		actual transistor -- because if the layer is sitting	14:14:22
14		by vacuum, it's just a layer, it's just	14:14:25
15		equipotential conductor. But when it intersect the	14:14:28
16		string it will constitute the gate electrically, the	14:14:33
17		gate, because by virtue of having voltage on that	14:14:36
18		equipotential plane to become the word line voltage	14:14:39
19		or the gate voltage. So word line and gate are one	14:14:43
20		-- one group and then gate layer and word line layer	14:14:47
21		are another group. So I think -- I don't think we	14:14:50
22		should -- we should confound the two.	14:14:53

1 Q Is the term "word line" ever used to
2 describe a physical layer?

3 MR. HSU: Objection; form.

4 A Again, you mentioned ever. I will have to
5 see the context. I'm tasked to analyze in the
6 context of '957, again, with '957's citation of the
7 prior art and reference, and in my knowledge as a
8 POSITA, and in my looking at some of the background
9 references, textbook references, so that's my
10 testimony.

11 I don't -- I do not go hypothetical ever,
12 always, all. I will have to analyze each one
13 individually or at least be fair to analyze -- to be
14 able to analyze it and render opinion.

15 Q Just to be clear, your testimony is that
16 as used in the '957 the term "word line layer" is
17 physical. Is that correct?

18 A You said is. I did not say the word line
19 layer is physical. I'm saying that '957 through its
20 Figure 2 using a physical cross-section diagram to
21 introduce physically is the word line layer, they
22 are able to physically contact it by word line

1 contact. In that contact they were trying to show 14:16:14
2 us what a -- physically what a word line layer is. 14:16:16
3 And that's my testimony that in that case when it 14:16:20
4 talks about word line layer, it's always talking 14:16:23
5 about in terms of, for lack of a better word, 14:16:26
6 perhaps in terms of physical, in terms of process, 14:16:30
7 meaning as the structure is contacted to a word line 14:16:32
8 contact, it's not in the sense as a word line or the 14:16:34
9 gate. It's more trying to denote or describe the 14:16:38
10 physical aspect of the things how it's -- how it's 14:16:42
11 structurally connected, maybe I should say 14:16:47
12 structurally rather than physically, I should say 14:16:51
13 structurally connected. So that's my testimony and 14:16:54
14 that's how '957 introduce word line layer through 14:16:55
15 Figure 2. 14:17:01

16 Q And in Figure 3 when it refers to word 14:17:01
17 line, you're saying that is not the same as word 14:17:05
18 line layer? 14:17:10

19 MR. HSU: Objection; misstates prior 14:17:17
20 testimony. 14:17:20

21 A I don't know the meaning of the same. We 14:17:21
22 come to this -- I'm really sorry, I'm getting a 14:17:25

1 little bit -- a little bit I would say maybe it's my 14:17:27
2 lack of better explanation, so I apologize, and I 14:17:32
3 probably should explain better. 14:17:36

4 Again, Figure 3 is a circuit schematic and 14:17:38
5 Figure 2 is a cross-section more of a structure 14:17:43
6 schematic, okay, so they use different things. 14:17:47

7 The word line layer, the voltage that word 14:17:50
8 line layer has, this equipotential word line layer 14:17:54
9 or the gate layer, that when it intersect the string 14:17:57
10 it forms a gate of the transistor, meaning that it's 14:18:02
11 able to impart the voltage on that equipotential to 14:18:07
12 that memory cell. 14:18:11

13 Therefore, it's the gate of the memory 14:18:12
14 cell, because it can modulate the behavior of memory 14:18:15
15 cell. So this word line layer, equipotential layer, 14:18:18
16 it intersect the string and therefore at that forms 14:18:22
17 a transistor with the gate. 14:18:26

18 So physically the extent of the gate, you 14:18:29
19 know, I mentioned testimony already, it doesn't 14:18:32
20 really matter. You can for sake of understanding 14:18:36
21 you can draw a little square box saying that, okay, 14:18:38
22 this piece of the word line, word line layer I'm 14:18:42

1	going to call it electrically to be the gate. But	14:18:45
2	it doesn't really matter because the whole thing is	14:18:48
3	equipotential. So whatever voltage is on that word	14:18:50
4	line, whether you draw a box or extend that box by	14:18:54
5	another micron or by another nanometer it doesn't	14:18:58
6	matter. It's still electrically with the voltage on	14:19:02
7	it become -- forms a gate acting as a gate of that	14:19:05
8	memory -- memory transistor.	14:19:08
9	Q Would you ever say that where the word	14:19:09
10	line layer intersects the channel it forms a word	14:19:11
11	line?	14:19:18
12	MR. HSU: Objection; form.	14:19:19
13	A We testified it forms a transistor and	14:19:25
14	that word line layer will be the gate, will be the	14:19:28
15	gate electrically for that transistor. I think	14:19:33
16	we -- I think I made it very clear already, so.	14:19:37
17	Q Okay.	14:19:41
18	A And, you know, I think --	14:19:41
19	Q We'll get to a break very shortly. I just	14:19:43
20	want to finish up here, if that's okay.	14:19:46
21	A Yeah.	14:19:48
22	Q So I'm sorry, let's reset for a bit here.	14:19:52

1	So I'm trying to understand here, so you would say	14:19:57
2	that where a word line layer intersects the channel	14:19:59
3	it forms a control gate.	14:20:03
4	A No, I didn't say that. I said when the	14:20:11
5	word line intersect the channel, it forms a	14:20:14
6	transistor and that's how NAND works, and I believe	14:20:17
7	that's the description we see in paragraph and also	14:20:22
8	in -- so it forms a transistor. That word line	14:20:26
9	layer has equipotential voltage on it, that word	14:20:32
10	line layer or the gate layer has equipotential on	14:20:37
11	it, and this voltage will be the gate voltage to	14:20:41
12	control the operation of that particular memory	14:20:49
13	cell.	14:20:53
14	Q So --	14:20:56
15	A So I don't --	14:20:57
16	Q Let's take a -- sorry.	14:21:01
17	A I don't know how you demarcate the extent	14:21:03
18	of physically which part is the word line or the	14:21:06
19	gate. And my testimony is that distinguish it's not	14:21:09
20	important. All we need to know is that in the	14:21:13
21	context of '957 or the prior art reference gate,	14:21:15
22	word line the same. Gate layer, control -- gate	14:21:20

1 layer are the same. So word line layer

14:21:25

2 equipotential. So gate layer equipotential. That's

14:21:30

3 all. That's all we need to know about '957 --

14:21:32

4 Q I'm just trying to understand you say

14:21:35

5 they're the same. But are you saying that they have

14:21:39

6 the exact same meaning, like they're physically the

14:21:41

7 same, or are you saying that they have the same

14:21:44

8 voltage?

14:21:47

9 MR. HSU: Objection; compound.

14:21:48

10 A I think in the context of the waveform

14:21:52

11 operation it's critical to understand in the context

14:21:56

12 of '957 operation. So in that context the --

14:21:58

13 whatever voltage on the word line is the voltage on

14:22:03

14 the gate. So going from the specification '957

14:22:06

15 talking about word line voltage and then not with

14:22:09

16 the curve, with the figure in Figure 4 through

14:22:14

17 Figure 9 all the different waveform, different bias

14:22:19

18 condition.

14:22:23

19 So the understanding is that the word line

14:22:23

20 voltage is the same as gate voltage. The word line

14:22:25

21 layer is same as gate layer. It's the word line

14:22:29

22 layer is equipotential. And what is causing the RC

14:22:30

1 delay is coming from the X decoder. And as doctor
2 -- the other doctor mentioned, he calls it word line
3 driver, but which really include mainly X decoder
4 and to drive the voltage, and so that RC delay in
5 part will make a difference whether your
6 pre-verification time is adequate or not. And by
7 adequate it doesn't necessarily mean a specific
8 type.

9 But anyway, so if the RC delay is large,
10 you're going to get a curve waveform, and that curve
11 waveform strictly coming from the X decoder, the
12 word line layer is equipotential. And that's the
13 way that '957 is to be understood and that's the way
14 '957 is understood by a POSITA and by citing the --
15 by looking at the reference in the prior art that
16 '957 cited.

17 Q Thank you very much. I think we can take
18 a small break, if that's okay with you.

19 A Sure. I'm not sure if it's appropriate
20 for me to ask the question, because my time zone may
21 be different from yours, and I may have to -- if
22 we're going to go much longer I might have to make

1	arrangement for lunch.	14:23:49
2	Q You know, we have a bit more to go. So	14:23:52
3	I'm not sure, would you like to take a longer break	14:23:54
4	for lunch or would you like to make arrangements for	14:23:57
5	lunch?	14:24:01
6	A We can take a short break so I can try to	14:24:01
7	make arrangement for lunch, and then maybe later on	14:24:04
8	if we can take a lunch break, if we extend to that	14:24:06
9	far, yeah.	14:24:10
10	Q Yeah, I think we can do that. So let's	14:24:10
11	take say a 10-minute break and then we'll plan for	14:24:14
12	-- so that will bring us to about 2:35, and then	14:24:17
13	let's plan around 3:30, if we get there, we can take	14:24:23
14	a longer lunch break. How does that sound?	14:24:27
15	A That's fine with me, yeah.	14:24:30
16	MR. BALBAKY: Is that okay with you,	14:24:32
17	counsel?	14:24:34
18	MR. HSU: Yeah, that's fine.	14:24:34
19	THE VIDEOGRAPHER: All right. We are	14:24:36
20	going off the record and the time is 2:24 p.m.	14:24:36
21	(Recess 2:24 p.m. - 2:35 p.m.)	14:24:40
22	THE VIDEOGRAPHER: We are back on the	14:35:10

1	record and the time is 2:35 p.m.	14:35:15
2	BY MR. BALBAKY:	14:35:19
3	Q Dr. Liu, could you please turn to Figure 4	14:35:23
4	of the '957 patent.	14:35:27
5	A I'm there.	14:35:34
6	Q Is Figure 4 a claimed embodiment of the	14:35:34
7	'957 patent?	14:35:45
8	A I would have to let me go through the --	14:35:57
9	when you say claim embodiment, I -- can you -- can	14:36:00
10	you specify? I mean, can you clarify?	14:36:08
11	Q Does Figure 4 fall within the scope of any	14:36:12
12	of the claims of the '957 patent?	14:36:22
13	A Let me go to my declaration.	14:36:45
14	Q Sure, if you would like, we can turn to	14:36:52
15	your declaration. Just let me know which portions	14:36:55
16	of your declaration you are reviewing.	14:37:04
17	A Yeah, I'm trying to find it. Repeat your	14:37:06
18	question again because I want to make sure which	14:38:39
19	aspect you're talking about. Repeat your question	14:38:42
20	again, please. I'm sorry about this, yeah.	14:38:44
21	Q Yeah. My question was, is Figure 4 a	14:38:46
22	claimed embodiment of the '957 patent?	14:38:49

1	A	If I were to look at the claimed	14:38:55
2		embodiment as to, first of all, go through the	14:39:00
3		independent Claim 1, independent Claim 1 has some	14:39:01
4		limitation I don't believe that -- that Figure 4	14:39:08
5		embodies. Therefore, Figure 4 under that scenario	14:39:10
6		would not be an embodiment of -- of claim of '957.	14:39:14
7	Q	Let's turn to Figure 6.	14:39:21
8	A	I'm there.	14:39:30
9	Q	Is Figure 6 a claimed embodiment of the	14:39:31
10		'957 patent?	14:39:39
11	A	Again, you would have to -- according to	14:39:43
12		the '957 specification, I'm going to go through	14:39:56
13		column -- column 12, okay, at least just citing the	14:40:00
14		patent itself, column 12, line 28, Figure 6 is the	14:40:06
15		first schematic diagram of the verify/read operation	14:40:14
16		in the verify/read memory cell of a 3D NAND memory	14:40:17
17		device in accordance with supplementary embodiment	14:40:21
18		of the disclosure. So under that description I	14:40:24
19		would say -- answer to your question I would say	14:40:29
20		yes.	14:40:33
21	Q	I'm sorry. Can you repeat what portion of	14:40:33
22		the '957 specification are you reading from?	14:40:38

1	A	Yes. I'm reading from column 12, line 28,	14:40:41
2		and I'm simply reading the first sentence all the	14:40:48
3		way to line 31.	14:40:52
4	Q	I see. Thank you. I appreciate that.	14:40:54
5		Does Figure 6 illustrate all of the	14:40:57
6		features recited in Claim 1?	14:41:12
7	A	Can you point me to my declaration for	14:41:30
8		this aspect of your question, please? I think --	14:41:32
9		yeah.	14:41:36
10	Q	So, for example --	14:41:40
11	A	-- declaration, yeah.	14:41:43
12	Q	-- in your declaration on paragraph 44 --	14:41:44
13	A	This would be reply declaration, right?	14:41:48
14	Q	Yes, in your reply declaration.	14:41:51
15	A	Sure. Thank you, I appreciate that. That	14:41:54
16		help us to facilitate that. Thank you.	14:41:56
17	Q	That's okay. I'm just trying to	14:41:59
18		understand here. So starting in the middle of the	14:42:01
19		paragraph you state, quote, "Because the claims	14:42:03
20		cover embodiments shown in Figures 6 to 9, the	14:42:07
21		length of the pre-verify stage (and whether the gate	14:42:12
22		voltage fully develops) does not define the alleged	14:42:16

1	invention."	14:42:22
2	A Yes, I see that.	14:42:23
3	Q Okay. So my question was, is Figure 6 a	14:42:26
4	claimed embodiment of the '957 patent?	14:42:32
5	A Yeah, I just mentioned to you that in	14:42:37
6	light of the column 12, that it's an exemplary	14:42:41
7	embodiment of the disclosures, and my answer to that	14:42:49
8	would be yes, and I'll be happy to -- I'll be happy	14:42:52
9	to explain the context of paragraph 44 if you want	14:42:55
10	me to now.	14:42:59
11	Q Well, I was just trying to understand a	14:43:00
12	little bit further. So if you can turn back for a	14:43:01
13	moment to Figure 6.	14:43:05
14	A Okay.	14:43:09
15	Q My question is whether Figure 6	14:43:10
16	illustrates all of the features recited in Claim 1.	14:43:12
17	A In which aspect of the feature of Claim 1	14:43:37
18	do you have in mind?	14:43:40
19	Q Well, I'm asking if Figure 6 illustrates	14:43:44
20	all the features of Claim 1.	14:43:49
21	A Well, the column 12 I just read indicate	14:44:02
22	that this is an example the embodiment of the -- of	14:44:08

1 this patent, right. So I would assume that under
2 that qualifier, so if you have any -- any particular
3 like embodiment that you want me to discuss, I'll be
4 happy to. But I already read you the column 12
5 citation.

6 Q Well, I'm asking if it illustrates all the
7 features of Claim 1.

8 MR. HSU: Objection; asked and answered.

9 A Can you point me to my declaration, reply
10 declaration? Because I don't -- I don't -- I'm here
11 to testify for the -- for my reply declaration. I'm
12 not here to testify for my initial declaration where
13 I map out the obviousness or anticipation based
14 on -- based on the prior art. So I would prefer you
15 point me to my reply declaration where in the
16 context of your question.

17 Q You say in your declaration on paragraph
18 44, your reply declaration, that the claims cover
19 embodiments shown in Figures 6 to 9. That's
20 correct. Do you agree?

21 A I agree, yes.

22 Q Does Claim 1 cover the embodiments shown

1	in Figure 6?	14:45:50
2	A Which -- which limitation?	14:46:07
3	Q Does Claim 1 -- let me rephrase.	14:46:11
4	I asked before but I'll ask again, does	14:46:17
5	Figure 6 illustrate all of the limitations recited	14:46:20
6	in Claim 1?	14:46:25
7	A Keep in mind Figure 6 is a -- is a	14:46:42
8	waveform, right, it's, as we just read, in the	14:46:48
9	context of column 12, we just read that Figure 6 the	14:46:53
10	schematic diagram of a verify/read operation.	14:46:58
11	So in the context of the operation, in the	14:47:01
12	context of the voltage on the gate and on the word	14:47:04
13	line on the gate in this operation for verify and	14:47:11
14	read, yes, the claim Figure 6 will cover the, for	14:47:16
15	example, the applied pre-verify volt stage.	14:47:24
16	But -- but I just want to caution that	14:47:29
17	Figure 6 doesn't exist in vacuum by itself. When we	14:47:32
18	say Figure 6, the reason I'm hesitating to answer	14:47:35
19	your question is that there's a context when we say	14:47:39
20	the covered embodiment, it's referring to the	14:47:43
21	pre-verified and the operation in pre-verify and	14:47:47
22	verify in terms of the -- in terms of the word line	14:47:52

1 voltage waveform, and of course the Claim 1 has

14:48:00

2 other preambles.

14:48:04

3 So to that extent I just want to make sure

14:48:06

4 I say that Figure 6 doesn't exist in a vacuum.

14:48:12

5 Figure 6 come with Figure 1, Figure 2, Figure 3 and

14:48:17

6 all the -- you know, all the word line layer and all

14:48:20

7 the stuff including the circuitry to facilitate the

14:48:21

8 volt to waveform.

14:48:27

9 So I just want to be very careful, be very

14:48:29

10 complete in my answer that in the context that I

14:48:33

11 think column 12 is discussing, is discussing the

14:48:38

12 waveform and discussing the voltage in the

14:48:43

13 pre-verify and verify operation.

14:48:46

14 Q So does Figure -- so I'm sorry, I'm just

14:48:52

15 trying to get a straight answer. I'm not sure, but

14:49:01

16 does Figure 6 illustrate all of the features recited

14:49:04

17 in Claim 1?

14:49:07

18 MR. HSU: Objection; asked and answered.

14:49:08

19 A Let me go through it again. It's very

14:49:20

20 clear, not my word, but '957, the patent says that

14:49:25

21 in accordance with an exemplary embodiment of the

14:49:32

22 disclosure, so it's an embodiment of the disclosure.

14:49:35

1 Now, so it's a diagram, but, yeah, it doesn't exist 14:49:39
2 in vacuum. It has a context. It's a context is 14:49:43
3 that given that you have this -- this apparatus, 14:49:48
4 given that you have this, and you have this Figure 6 14:49:52
5 is schematic diagram of a verify/read operation. 14:49:56
6 The reason I'm answering this way is 14:50:01
7 Figure 6 carries the context, carries the -- I would 14:50:08
8 use like a better word, carry the genealogy or the 14:50:11
9 evolution into Figure 6. So I would assume that 14:50:15
10 implying Figure 6, you're going to have processing 14:50:18
11 circuitry and everything, otherwise you wouldn't get 14:50:22
12 these waveform in vacuum. 14:50:26
13 So I just want to make sure that all the 14:50:29
14 preamble, all the overhead stuff are actually 14:50:31
15 implied or represented in Figure 6, because the 14:50:36
16 waveform cannot come out of vacuum, right. So that 14:50:38
17 that's the point I'm trying to make. I'm not trying 14:50:42
18 to not give you a straight answer. 14:50:44
19 But in terms of the actual waveform, 14:50:47
20 column 6 -- column 12 clearly says that the Figure 6 14:50:50
21 embodies all the -- all the -- embodies the 14:50:55
22 disclosure. But then I just -- Figure 6 has in this 14:50:59

1	overhead, for example, processing circuitry and	14:51:03
2	apparatus, all that, all that --	14:51:07
3	Q Does Figure 6 --	14:51:07
4	A -- that's not shown, yeah.	14:51:11
5	Q Does Figure 6 illustrate processing	14:51:12
6	circuitry?	14:51:15
7	A It's implied because otherwise the	14:51:17
8	waveform would not show up, because waveform doesn't	14:51:20
9	show up in vacuum. That's exactly what I'm trying	14:51:24
10	to answer. I don't -- I don't want you to	14:51:26
11	misconstrue my answer.	14:51:27
12	But I want to answer with the caveat that,	14:51:29
13	look, column 12 says clearly that Figure 6 embody	14:51:33
14	the disclosure. Therefore, I take it as that Figure	14:51:38
15	6 doesn't exist in vacuum. Figure 6, the waveform	14:51:41
16	that comes out of it should have a supporting	14:51:45
17	structure to give this waveform because that's what	14:51:48
18	figure -- that's what column 12 is telling me that	14:51:51
19	it shows embodiment of the disclosure.	14:51:54
20	So to the -- to the extent that you're	14:51:57
21	asking does it -- does it include all the limitation	14:51:59
22	of Figure 1 -- of Claim 1? The -- I would say let's	14:52:02

1 take a processing circuitry, for example, okay, and 14:52:10
2 I would -- I would take into context of column 12, I 14:52:13
3 would say that although Figure 6 doesn't show the 14:52:17
4 circuitry, but the waveform doesn't -- doesn't exist 14:52:19
5 in vacuum, so... 14:52:23

6 Q So to confirm, Figure 6 does not 14:52:25
7 illustrate the processing circuitry? 14:52:28

8 A The better way to answer is that according 14:52:39
9 to column 12, again, it's very clear that Figure 6 14:52:43
10 is an embodiment of the disclosure. But as with 14:52:48
11 illustration you cannot illustrate everything, 14:52:55
12 otherwise the illustration would become too 14:52:58
13 convoluting. You can see it. 14:53:01

14 But the fact that you have waveform, I 14:53:03
15 would -- I would say that to a POSITA the fact that 14:53:06
16 you have a waveform and all the preamble, if you 14:53:09
17 want to call it preamble, all the overhead, and it's 14:53:09
18 implied there simply because a waveform cannot exist 14:53:13
19 in vacuum. 14:53:16

20 Q Does Figure 6 illustrate a first memory 14:53:18
21 cell string and a second memory cell string as 14:53:22
22 recited in Claim 1? 14:53:28

1 A Again, the fact that -- let me go back 14:53:31
2 to -- to based on column 12 and based on evolution 14:53:44
3 based in the context of column 12, although it 14:53:51
4 doesn't show as we went through this morning like 14:53:54
5 Figure 3, otherwise the figure would be too 14:53:58
6 convoluted. But the fact that you have unselected 14:54:01
7 TSG versus select TSG, it's a good indication that 14:54:05
8 there's a -- there's a selected string, unselected 14:54:09
9 string, so... 14:54:14

10 Q Does Figure 6 illustrate that the first 14:54:17
11 memory cell string includes a bottom select gate, 14:54:20
12 BSG, transistor memory cells and a top select gate, 14:54:26
13 TSG, transistor that are connected in series? 14:54:32

14 A Again, referring to column 12, that's 14:54:38
15 saying that Figure 6 is -- let me use exact word. 14:54:42
16 Figure 6 show the operation schematic diagram of a 14:54:49
17 verify/read operation to verify/read memory cell in 14:54:59
18 the 3D NAND memory device in accordance with the 14:55:04
19 exemplary embodiment of the disclosure. 14:55:08

20 So Figure 6 trying to convey the 14:55:11
21 embodiment of the invention. Although, again, the 14:55:15
22 figure will be too convoluted to show everything, 14:55:20

1 yet it does show BSG, it does show TSG, it shows
2 selected, unselected, and a POSITA would know that
3 that's how memory strings are formed. So, again,
4 it's -- it's taken in the context of column 12.

5 Q So Figure 6 standing alone does not
6 illustrate all the features recited in Claim 1, but
7 you need the additional context of the patent
8 itself.

9 MR. HSU: Objection to form.

10 Q Is that correct?

11 A I disagree with that. As I testified,
12 these waveform don't exist in vacuum. There are --
13 there has to be overhead and processing circuitry
14 and apparatus to -- to facilitate its waveform. And
15 the fact that you have selected and unselect TSG,
16 that means you have at least two strings, and the
17 fact that you have BSG and TSG, and we discussed how
18 the strings are formed with TSG on top and memory
19 cell in the middle and BSG on the bottom.

20 So I think this question is really -- to
21 me, is rhetorical question in the sense that, you
22 know, the feature don't come in vacuum and then they

14:55:24

14:55:29

14:55:32

14:55:37

14:55:45

14:55:50

14:55:54

14:55:56

14:56:00

14:56:03

14:56:03

14:56:05

14:56:08

14:56:13

14:56:19

14:56:24

14:56:27

14:56:30

14:56:34

14:56:38

14:56:42

14:56:46

1 can only illustrate that however relevant 14:56:50
2 information that a POSITA would take away to 14:56:54
3 understand the invention. But all the overhead such 14:56:58
4 as processing circuitry, such as how a NAND string 14:57:02
5 is formed, I think that is just the overhead. 14:57:04
6 I think -- I think the POSITA would know 14:57:08
7 what that string consist of, and certainly Figure 6 14:57:12
8 shows -- at least show all the component that needed 14:57:16
9 for string and needed for multiple string, and the 14:57:20
10 waveform shows that there's need for circuitry to 14:57:24
11 generate these waveforms. 14:57:26
12 So it may not have a circuit diagram, you 14:57:28
13 know, like -- like Figure 1 or something of -- 14:57:30
14 otherwise your figure would just be a big gigantic 14:57:33
15 figure, you cannot decipher anything. This figure 14:57:38
16 is meant to help us quickly understand the waveform 14:57:41
17 and understand the word line voltage, which is the 14:57:43
18 control gate voltage, and how it -- the operation in 14:57:47
19 the pre-verify and verify mode. 14:57:53
20 So I think -- I think I would say that if 14:57:56
21 not explicitly, at least a POSITA would implicitly 14:57:58
22 know that the overhead would be there. 14:58:04

1	Q	Does Figure 6 illustrate aspects of Claim	14:58:06
2	1?		14:58:14
3	A	Can you define aspects?	14:58:14
4	Q	Let's say -- let me rephrase.	14:58:17
5		Does Figure 6 illustrate certain	14:58:19
6		limitations of Claim 1?	14:58:26
7	A	By "certain" which one do you mean?	14:58:35
8		Should we go through them one by one? We can map	14:58:38
9		it, I would be happy to map it starting from apply	14:58:42
10		in the pre-verify stage we can map it.	14:58:45
11	Q	So let me -- let me ask you. So -- sorry.	14:58:47
12		You said starting with apply in the pre-verify	14:58:51
13		stage?	14:58:56
14	A	Yeah.	14:58:56
15	Q	Why did you start there? What about the	14:58:57
16		material before that?	14:58:59
17	A	Okay. Which one do you want -- let's go	14:59:01
18		through them, if you want to go through, which one,	14:59:07
19		which particular one? You mentioned the aspect, I	14:59:10
20		want to understand what you meant by aspect.	14:59:13
21	Q	So, for example, does Figure 6 illustrate	14:59:17
22		the limitation apply in a pre-verify stage a first	14:59:23

1	verify voltage on a gate terminal of a selected	14:59:28
2	memory cell of the first memory cell string?	14:59:31
3	A I believe it does.	14:59:47
4	Q Okay. Going back a little bit, does	14:59:50
5	Figure 6 illustrate processing circuitry? Or is	14:59:54
6	that part of the overhead?	15:00:01
7	A I testified to already that the fact that	15:00:03
8	you see apply in the pre-verify stage these	15:00:05
9	waveform, there has to be a means on apparatus or	15:00:11
10	circuitry to facilitate the application of these	15:00:15
11	voltage.	15:00:19
12	So to the extent that it may not show --	15:00:19
13	if it wants to show that every figure will need to	15:00:22
14	have, for example, will need to include Figure 1,	15:00:26
15	Figure 2, Figure 3, and all the way to and	15:00:28
16	including -- including Figure 11 on every -- every	15:00:34
17	figure with the waveform, and I think I just -- I	15:00:38
18	think it's fair to say that Figure 6 doesn't exist	15:00:43
19	in vacuum, and through the specification of Figure	15:00:46
20	12, I believe that it's implicit that it has to have	15:00:49
21	processing circuitry, otherwise these waveform don't	15:00:53
22	come in vacuum, right, so...	15:00:57

1 Q What about Figure 7, does Figure 7 15:01:11
2 illustrate processing circuitry? 15:01:17

3 A Again, it's the same answer, same answer 15:01:20
4 as Figure 6. So again, I want to state that the 15:01:34
5 specification in column 13, column 13 of the 15:01:42
6 specification says, "Figure 7 is a second schematic 15:01:46
7 dying of a verify/read operation to verify/read 15:01:51
8 memory cells of the 3D NAND memory device in 15:01:55
9 accordance with the exemplary embodiments of the 15:01:59
10 disclosure." 15:02:04

11 So, again, it's under the context they 15:02:05
12 show Figure 7, which means that although not shown, 15:02:08
13 definitely it's implicit in the context of the 15:02:15
14 column I just read that the processing circuitry, 15:02:17
15 everything need to be there, otherwise these 15:02:20
16 waveform will not come about. 15:02:24

17 Q And is that the same for a first memory 15:02:25
18 cell string including a bottom select gate BSG 15:02:31
19 transistor memory cells and a top select gate TSG 15:02:36
20 transistor that are connected in series? 15:02:41

21 A Well, we can look at the description. I 15:02:43
22 mean, it doesn't have to be shown in figure. The 15:02:45

1	description, I didn't want to do it to take up so	15:02:49
2	much time. But you can see in description, the	15:02:52
3	description says it clearly the schematic diagram,	15:02:56
4	and the schematic diagram it definitely will at	15:03:01
5	least refer to Figure 3. And then I think it also	15:03:05
6	shows like in the -- in the earlier statement how --	15:03:08
7	how the string are connected. So I -- so I'm not	15:03:13
8	sure how else to answer your question, right. So --	15:03:21
9	Q That's okay.	15:03:24
10	A I think -- I think when you verify	15:03:27
11	operation, and if you go all the way back to column	15:03:30
12	10, column 9, and a description going from Figure 2	15:03:33
13	to Figure 3, it's very clear, I mean, so it describe	15:03:37
14	how the strings are formed, and then in Figure 6 and	15:03:41
15	Figure 7 it shows all the components. I think to a	15:03:46
16	POSITA I think it's very straightforward that in	15:03:48
17	accordance to what I just read in column 13, column	15:03:52
18	12, I think it's these figures embodies the	15:03:55
19	disclosure, invention disclosure.	15:04:03
20	Q But they don't illustrate all of the	15:04:05
21	recited features of Claim 1.	15:04:07
22	MR. HSU: Objection; form.	15:04:12

1	A	I don't know what you meant by don't	15:04:12
2		illustrate. I think to a POSITA if I see a waveform	15:04:14
3		I need to -- I right away -- especially certain	15:04:19
4		voltage magnitude, right away I know that there is	15:04:23
5		this waveform generated off of some circuitry,	15:04:26
6		because that's how innovative circuitry works.	15:04:29
7		I wouldn't say, you know, somehow I wonder	15:04:32
8		how this waveform come about, is it just -- I don't	15:04:35
9		think -- I don't think a POSITA would read it that	15:04:39
10		way, especially not in light of all the description,	15:04:41
11		all the specification that precedes the claim	15:04:44
12		limitation description, especially what I just read	15:04:49
13		in column 12 and column 13 that these are the	15:04:52
14		embodiment.	15:04:55
15		And then -- then given that these are the	15:04:56
16		embodiment, you have these voltages and these	15:05:01
17		waveform, and they don't just show up, there has to	15:05:03
18		be -- there has to be produced and it's -- so the	15:05:09
19		processing circuitry, to me, is implied. It doesn't	15:05:15
20		have to be -- not every graph have to show	15:05:18
21		everything because it shows only representative, but	15:05:21
22		not every graph has to show everything. And I think	15:05:25

1 Figure 7 is showing embodiment, certainly embodiment 15:05:31
2 taken in its totality will have to include all the 15:05:33
3 -- for lack of a better word we just used overhead 15:05:36
4 and the processing circuitry and whatnot, so... 15:05:39

5 Q Let's go back to Figure 6 for a second. 15:05:43

6 So to confirm, it's your opinion that Figure 6 is a 15:05:47
7 claimed embodiment of the '957. Is that correct? 15:05:53

8 A Just based on the specification describing 15:06:01
9 it, unless the specification is incorrect, but the 15:06:05
10 specification says it clearly, and I'm just -- just 15:06:09
11 citing the specification. 15:06:12

12 Q Okay. And it's a claimed embodiment 15:06:14
13 specifically. Is that correct? 15:06:17

14 A Can you point me to that again? I'm -- I 15:06:18
15 think I'm a little bit lost right now, so... 15:06:31

16 Q Well, again, in your reply declaration you 15:06:34
17 opined that the claims cover embodiments shown in 15:06:37
18 Figures 6 to 9. So I'm just asking you to confirm 15:06:47
19 that you still think that Figure 6 is one of the 15:06:50
20 claimed embodiments. 15:06:54

21 MR. HSU: Objection; asked and answered. 15:06:57

22 A Yeah, as I testified repeatedly already, 15:06:59

1 the statement was made in the context that with 15:07:04
2 column specification column 12, specification 15:07:08
3 columns 13, and in light of all the components 15:07:11
4 already explicitly shown in Figure 6, as well as 15:07:15
5 Figure 7, but let's talk about Figure 6, in Figure 15:07:21
6 6, and knowing these voltage, this waveform, and in 15:07:26
7 the context of the specification they may not show 15:07:30
8 explicitly -- it just like, for example, you know, I 15:07:39
9 mean, like the -- it's taken implicit that to get to 15:07:43
10 this, you have a foundation, you have overhead that 15:07:59
11 you build upon, and therefore column 12, column 13 15:08:02
12 says it clearly. 15:08:06

13 And then so when you just look at a 15:08:06
14 figure, you know that it has all these pedigrees, 15:08:09
15 all these -- all these background already 15:08:12
16 encompassed in it. So, yeah, I mean, I think the 15:08:14
17 processing circuitry will have to be implicit to a 15:08:20
18 POSITA because otherwise how do you generate 15:08:23
19 waveform unless -- that's my testimony, yeah. 15:08:27

20 Q So to summarize, is it your testimony that 15:08:32
21 Figure 6 is one of the claimed embodiments? 15:08:37

22 MR. HSU: Objection; asked and answered. 15:08:40

1	A	Figure 6, according to the context of	15:08:51
2		specification in column 12, is an example of the	15:08:55
3		embodiment of the disclosure.	15:08:58
4	Q	But does that include claimed embodiments?	15:09:04
5		MR. HSU: Objection; asked and answered.	15:09:07
6	A	Do you want me to repeat the answer again?	15:09:13
7		Because the waveform comes with -- again, in light	15:09:18
8		of column 12, column 13, and in light of the	15:09:31
9		specification going from we went through this	15:09:35
10		morning Figure 2 all the way to Figure 3, and to a	15:09:38
11		POSITA this so-called claim limitation, a POSITA	15:09:43
12		would know that it's there because that's how	15:09:52
13		integrative circuit works, you cannot have waveform	15:09:56
14		without having circuitry to generate those	15:10:00
15		waveforms.	15:10:03
16		So I don't -- I don't -- I don't know how	15:10:03
17		else to answer except that it's implicit. Maybe the	15:10:08
18		figure does not have -- is not cut and paste Figure	15:10:13
19		2 and Figure 3 and lump everything in one figure to	15:10:17
20		confound the issue, the figure -- Figure 6 is simply	15:10:22
21		trying to illustrate a particular aspect, the saving	15:10:27
22		aspect of the invention. And so the processing	15:10:35

1 circuitry and everything has already been discussed 15:10:38
2 before, and as you can see the figure, I think it 15:10:39
3 was Figure 11 certainly show the -- all the 15:10:45
4 processing circuitry. 15:10:49

5 So I think you have to take things in 15:10:51
6 totality. I don't think it's fair to just grab a 15:10:53
7 line and say, you know, does this show this, does 15:10:56
8 this show that. I mean, it's -- it's implicit 15:10:59
9 there. And certainly Figure 7 -- or Figure 6 15:11:02
10 doesn't exist alone and Figure 6 has the -- has the 15:11:06
11 benefit of all the -- I want to say all the 15:11:10
12 supporting component to make an integrated circuit, 15:11:22
13 so. And in Figure 6 just happened to give in that 15:11:27
14 context illustrate the waveform aspect of things to 15:11:32
15 make things clear. Otherwise -- otherwise it will 15:11:35
16 be very difficult to decipher the figure. 15:11:38

17 Q But Figure 6 illustrates at least the 15:11:39
18 waveform aspects of the claims. Is that correct? 15:11:43

19 A Again, by virtue of illustrating the 15:11:52
20 waveform aspect, I think the -- all the supporting 15:11:57
21 structure, all the infrastructure needed for these 15:12:01
22 waveform wouldn't -- wouldn't necessarily be there 15:12:07

1	as well, so...	15:12:11
2	Q Okay. But Figure 6 does illustrate the	15:12:12
3	waveform aspects, would you agree?	15:12:15
4	A In the sense that Figure 6 is a waveform,	15:12:19
5	yes.	15:12:22
6	Q But it illustrates the waveform aspects of	15:12:23
7	Claim 1 specifically?	15:12:26
8	A What do you mean by waveform aspect?	15:12:28
9	Q So you would agree that Claim 1 includes	15:12:30
10	structural limitations and then descriptions of	15:12:36
11	certain waveforms being applied in pre-verify stage	15:12:39
12	and verify stage?	15:12:42
13	MR. HSU: Objection; form.	15:12:45
14	A I guess certain bias voltage, yeah,	15:12:48
15	certain bias voltage, certain limitation and bias	15:12:51
16	voltage.	15:12:55
17	Q Okay. And you would agree that Figure 6	15:12:55
18	is illustrating at least the limitations recited in	15:12:57
19	Claim 1 related to the various bias voltages?	15:13:01
20	A Well, another way of saying is that I	15:13:11
21	think Figure 6 is an example embodiment of the	15:13:15
22	claim.	15:13:19

1 Q But Figure 6 does not illustrate the 15:13:24
2 structural components, correct? 15:13:27

3 MR. HSU: Objection; asked and answered. 15:13:31

4 A To the extent that this figure don't exist 15:13:37
5 in a vacuum, you need the infrastructure to -- 15:13:41
6 infrastructure and circuitry as infrastructure, I 15:13:44
7 certainly -- certainly think that a POSITA looking 15:13:49
8 at it would understand that although not illustrated 15:13:53
9 specifically, and that there would be processing 15:13:56
10 circuitry to enable such a different voltage being 15:13:59
11 applied in the pre-verify and verify stage. 15:14:03

12 Q Okay. But Figure 6 does not illustrate 15:14:06
13 the processing circuitry and does not illustrate the 15:14:09
14 physical components recited in the preamble of Claim 15:14:14
15 1, would you agree? 15:14:19

16 MR. HSU: Objection; compound. Objection; 15:14:20
17 asked and answered. 15:14:25

18 A I would only agree it's not explicitly but 15:14:25
19 implicitly. Again, you know, looking at this, 15:14:28
20 knowing that -- having worked in the industry so 15:14:31
21 many years, again, I'm -- I'm going to let you know 15:14:34
22 that this waveform or this voltage being applied, it 15:14:38

1 don't exist in vacuum, it has to -- have to come 15:14:42

2 from somewhere, so... 15:14:44

3 Q Can you confirm that Figure 6 illustrates 15:14:47

4 the remaining claim limitations directed to applying 15:14:50

5 various bias voltages? 15:14:56

6 A Can you repeat your question again? 15:15:05

7 Q Yeah, let me clarify. Would you agree 15:15:07

8 that Figure 6 illustrates at least the limitations 15:15:09

9 of Claim 1 related to applying verified voltages and 15:15:13

10 bias voltages? 15:15:20

11 A Given that's what the column 12 specify, I 15:15:30

12 think I would agree to that, unless column 12 is 15:15:36

13 wrong. 15:15:46

14 Q Well, column 12 doesn't discuss Claim 1, 15:15:46

15 so I'm asking you to confirm, in your opinion, if 15:15:49

16 Figure 6 illustrates at least the limitations of 15:15:54

17 Claim 1 related to applying verified voltages and 15:15:59

18 bias voltages? 15:16:03

19 A Well, I mean, you see my declaration, I -- 15:16:12

20 I stand by my declaration that the claim cover 15:16:18

21 embodiment showing in Figure 6 to 9. And I think to 15:16:23

22 the extent, I mean, I think, you know, if you were 15:16:29

1 to say how do you know this adjacent and that 15:16:30
2 adjacent and all that stuff, I think a POSITA would 15:16:33
3 understand, but I want it to be my testimony -- I 15:16:37
4 want my testimony to help both side, I want my 15:16:40
5 objective testimony to help both side to understand 15:16:43
6 the issue and also help PTAB to understand the 15:16:46
7 issue. I don't want this to become a mincing of 15:16:52
8 words or wordsmith and in the sense of processing 15:16:55
9 circuitry and stuff like that. Again, my 15:16:56
10 declaration says it very clearly that and I stand by 15:17:00
11 that, yeah. 15:17:07

12 Q So to confirm, even if you will not 15:17:11
13 respond about whether Figure 6 illustrates the 15:17:15
14 limitations in Claim 1 relating to applying verified 15:17:21
15 voltages and bias voltages, your testimony is still 15:17:26
16 that the claims cover the embodiments shown in 15:17:32
17 Figures 6 through 9? 15:17:34

18 MR. HSU: Objection; misstates prior 15:17:37
19 testimony and form and asked and answered. 15:17:41

20 A What I'm saying is I don't understand when 15:17:46
21 you said the -- just like -- just like I knew you 15:17:48
22 were going to go with process circuitry and trying 15:17:52

1 to -- trying to mince on that word, I'm trying to 15:17:54
2 explain that in the context of the '957 15:17:58
3 specification these are implicit. And so if you 15:18:01
4 want to go through limitation by limitation I'll be 15:18:04
5 happy to go through with you. And I think it's 15:18:08
6 unfair to characterize that I'm not willing to do 15:18:10
7 certain things. We can go through word by word, 15:18:13
8 limitation by limitation, so that I will not have to 15:18:17
9 deal with certain things where you start saying 15:18:21
10 that, you know, does this one point to first 15:18:24
11 adjacent to next adjacent. 15:18:27

12 I think the limitation is very clear and 15:18:28
13 the graph, the Figure 6 is just to illustrate it to 15:18:31
14 the point where you trying to wordsmith or mince it 15:18:35
15 and to point out to certain things and it's best if 15:18:38
16 we go limitation by limitation, if you like, I would 15:18:42
17 be happy to go through that with you. 15:18:46

18 Q Let's -- let's move on a little bit. So 15:18:50
19 in Figure 6 at the top of the figure it divides the 15:19:05
20 waveforms into different time periods. Would you 15:19:13
21 agree? 15:19:21

22 A Well, the designation of, for example, 15:19:26

1	pre-pulse, verify/read, and post-pulse and recovery,	15:19:29
2	yes.	15:19:35
3	Q Correct. So let's use the term "time	15:19:35
4	periods" because that's what you just used. So --	15:19:43
5	A I think you used "time period." I didn't	15:19:46
6	use "time period."	15:19:48
7	Q Okay. Would you like to refer to them as	15:19:49
8	something other than "time period"?	15:19:52
9	A I just want to clarify that I'm under the	15:19:54
10	qualification that the time period was introduced by	15:19:57
11	you just in case if somehow the connotation of time	15:20:01
12	period later on deviate, I just want to reserve that	15:20:06
13	qualification that you introduced the time period.	15:20:10
14	Q I understand. Thank you. I'm not trying	15:20:13
15	to trip you up on that. I'm just trying to	15:20:15
16	understand what's being disclosed.	15:20:17
17	A Yeah.	15:20:19
18	Q So you'll agree, though, that it has what	15:20:19
19	appear to be sections of the figure denoted as	15:20:23
20	initial, pre-pulse, verify/read, post-pulse and	15:20:30
21	recovery, do you see that?	15:20:38
22	A Yes, I do see the demarcation, yeah.	15:20:42

1 Q Now, these different sections, initial, 15:20:47
2 pre-pulse, verify/read, post-pulse and recovery, 15:21:04
3 which of those, if any, or if multiple correspond to 15:21:10
4 the pre-verify stage recited in the claims? 15:21:19

5 MR. HSU: Objection; form. 15:21:27

6 A Can you point me to because I'm here to -- 15:21:30
7 to respond to my reply declaration. I think some of 15:21:33
8 this stuff should have been gone over in the initial 15:21:36
9 declaration. So I would like you to point me to my 15:21:40
10 reply declaration for the context of your question. 15:21:43
11 If you could do that, I would really pretty much 15:21:48
12 appreciate it, yeah. 15:21:52

13 Q We can get to that in a second. I'm just 15:21:53
14 trying to understand which of these periods, or 15:21:56
15 which portion of this figure corresponds to a 15:22:03
16 pre-verify stage. 15:22:08

17 MR. HSU: Objection; form. 15:22:24

18 A Okay. Please ask your question again. 15:22:50
19 But can you point me to my reply declaration where 15:23:01
20 the pre-pulse is cited? 15:23:04

21 Q Let's -- let's change tactics a little bit 15:23:08
22 then -- or, sorry, change figures a little bit then. 15:23:12

1	Let's see. Let's go to your declaration at -- well,	15:23:16
2	let me see here for a moment. Let's actually go to	15:23:26
3	your reply declaration at paragraph 11.	15:23:40
4	A Okay, I'm there.	15:23:54
5	Q Okay. And here in paragraph 11 you have	15:23:55
6	an annotated copy of Figure 7. Is that correct?	15:23:58
7	A That's correct.	15:24:02
8	Q Okay. And in this figure it divides,	15:24:03
9	similar to Figure 6 did, it has a number of labeled	15:24:06
10	sections, which is an initial section, a pre-pulse	15:24:11
11	section, a verify/read section, a post-pulse section	15:24:20
12	and a recovery section. I'm trying not to refer to	15:24:26
13	them as time periods unless you want to. But do you	15:24:27
14	see where those labels are?	15:24:30
15	A Yes, I do.	15:24:32
16	Q And I'm trying to understand, because you	15:24:38
17	have certain of those labels boxed, for example, you	15:24:40
18	have pre-pulse boxed in red, you have verify/read	15:24:44
19	boxed in red, which of those sections, initial,	15:24:49
20	pre-pulse, verify/read, post-pulse and recovery,	15:24:56
21	would correspond to the claimed pre-verify stage, if	15:25:03
22	any?	15:25:30

1 A It's one of the -- one of the -- I don't 15:25:30
2 know if I should use the word "teachings." It's one 15:25:38
3 of the aspect of the invention where pre-pulse 15:25:42
4 period is the pre-verify period. 15:25:47
5 Q Okay. And does pre-verify ever include 15:25:53
6 the initial period? 15:25:58
7 MR. HSU: Objection; form. 15:26:03
8 A I think the patent is silent on it, so I'm 15:26:10
9 not going to -- I'm not going to comment on it. But 15:26:13
10 suffice to say that the pre-pulse period is the 15:26:16
11 pre-verify period at least -- 15:26:21
12 (Simultaneous speaking.) 15:26:33
13 Q I'm trying to understand if the initial 15:26:33
14 stage is also ever considered part of the pre-verify 15:26:38
15 stage. 15:26:45
16 MR. HSU: Objection; scope. 15:26:51
17 A I think in the context of the 15:26:57
18 specification of '957, it clearly is equating or 15:27:05
19 mapping the pre-pulse period to pre-verify period 15:27:11
20 and -- 15:27:15
21 Q Okay. And does it ever map the initial 15:27:20
22 period to a pre-verify period? 15:27:22

1	MR. HSU: Objection; asked and answered.	15:27:25
2	A I don't -- I don't -- can you point me	15:27:27
3	to -- point me to my declaration where I opine on	15:27:39
4	initial period.	15:27:46
5	Q I mean, it's right here in the figure	15:27:47
6	that's in your declaration. I'm trying to ask about	15:27:49
7	the beginning and end, the delineations of when the	15:27:52
8	pre-verify stage begins and ends.	15:27:55
9	MR. HSU: Objection; asked and answered.	15:28:01
10	A I think the specification except	15:28:16
11	mentioning initial period will recall the initial	15:28:22
12	stage where there's no voltage, then introduce a	15:28:29
13	pre-pulse stage in which it is a pre-verify stage.	15:28:33
14	So, again, pre-pulse stage is pre-verify in the	15:28:37
15	context of '957.	15:28:43
16	Q Okay. And does the pre-verify stage ever	15:28:45
17	include the portion of the figure labeled as	15:28:53
18	verify/read?	15:28:58
19	A Pre-verify? Can you repeat your question	15:29:03
20	again?	15:29:06
21	Q Yeah. When does the pre-verify stage end?	15:29:06
22	A You would have to -- you just have to go	15:29:15

1 through the -- it's it could be understood derived 15:29:24

2 from the description in Figure 7, we can go to that. 15:29:29

3 Q Well, I'm just -- I'm trying to get 15:29:37

4 your -- your position on this just because you're 15:29:41

5 describing in this paragraph the durations of these 15:29:44

6 different stages. 15:29:47

7 A Right. 15:29:48

8 Q So in your opinion, what is the beginning 15:29:48

9 and the end point of the pre-verify stage? 15:29:52

10 A Well, my opinion is in accordance with 15:29:57

11 what the specification is telling me and I'm trying 15:30:00

12 to analyze it based on that boundary condition. And 15:30:03

13 clearly in column 13 it says the pre-pulse stage can 15:30:08

14 include a first portion T1 and a second portion T2. 15:30:13

15 So that's why I'm mapping it that a pre-pulse, that 15:30:16

16 pre-pulse is pre-verification. 15:30:20

17 Q Okay. And in terms of the verify stage 15:30:24

18 what is the beginning and endpoint of the verify 15:30:28

19 stage? 15:30:31

20 A Well, according to the figure, according 15:30:32

21 to the -- in the specification -- it's getting 15:30:41

22 late -- and throughout the -- throughout the context 15:30:52

1 of '957, the verify/read, the same operation, same 15:31:11
2 verify and read operation commences after the 15:31:20
3 pre-pulse. So pre-pulse is before that and then 15:31:25
4 after that is this -- it's the -- in terms of Figure 15:31:29
5 7 it's the -- it's the verify/read operation. 15:31:36
6 Q Is the post-pulse part of the verify 15:31:42
7 stage? 15:31:46
8 A Again, I think the -- 15:31:47
9 Q Bless you. 15:31:47
10 A I'm sorry, I'm really sorry. Repeat your 15:32:05
11 question again. 15:32:10
12 Q So there's a period of time labeled as 15:32:12
13 post-pulse. Is that included as part of the verify 15:32:16
14 stage? 15:32:23
15 A No, because the patent clearly says the 15:32:24
16 different stages, right, it says include initial 15:32:30
17 stage, pre-pulse stage, which is pre-verify stage, 15:32:33
18 verify/read stage and a post-pulse stage, again, so 15:32:37
19 the post-pulse stage is mentioned specifically and 15:32:43
20 also demarcated from the read -- from verify/read 15:32:47
21 stage, so -- 15:32:53
22 Q What about -- sorry. 15:32:58

1 A So the post-pulse stage is demarcated from 15:33:00
2 verify/read stage. Again, but I should qualify 15:33:05
3 that, you know, I don't think I'm -- I opine in my 15:33:10
4 reply declaration these initial and post-pulse. If 15:33:17
5 you have -- if my recollection is incorrect, I'll be 15:33:20
6 happy to have you point out to me, yeah, so... 15:33:24

7 Q Well, I'm looking at this paragraph right 15:33:27
8 here, paragraph 11, and I'm trying to just clarify 15:33:30
9 what's being illustrated. You know, you'll have to 15:33:32
10 forgive me because you did sort of annotate a 15:33:36
11 portion of a line in the post-pulse stage so I just 15:33:41
12 wanted to clarify. 15:33:43

13 Now, just to clarify a little bit further, 15:33:45
14 just to confirm, and perhaps this is implicit from 15:33:48
15 what you just said, but is the recovery stage 15:33:51
16 illustrated part of the pre-verify stage or the 15:33:55
17 verify stage? 15:34:03

18 A Again, the recovery stage, based on the 15:34:17
19 context of the specification, is demarcated, or 15:34:22
20 pointed out separately from the verify/read stage. 15:34:29

21 Q So I know we're coming up at about 15:34:37
22 3:30-ish. I forget when you said your lunch was. I 15:34:41

1 don't want to make you late for that. 15:34:46

2 A Well, I was asking that -- it really 15:34:47

3 depends, like if you were to tell me that we can 15:34:49

4 finish in an hour and then to accommodate and make 15:34:52

5 sure your time doesn't go too late on the East 15:34:57

6 Coast, I can try to just push through it if that's 15:35:00

7 what you want. But if you have a lot longer to go, 15:35:03

8 then I guess then I will apologize for keeping you 15:35:06

9 much later in your East Coast time. But I was just 15:35:11

10 trying to accommodate and make sure that, you know, 15:35:14

11 I am cognizant of the time zone difference, I want 15:35:17

12 to make sure that I'm courteous and aware of your 15:35:21

13 time zone issue, yeah, so. 15:35:25

14 Q No, I understand that. I just want to 15:35:26

15 make sure that I give you breaks and I make sure 15:35:28

16 that you're fed. I don't know quite much longer I 15:35:31

17 have. I don't think it will be more than an hour, 15:35:35

18 but, you know, we can attempt to plow ahead, if 15:35:37

19 that's okay with you then. 15:35:41

20 THE WITNESS: Johannes, what do you think? 15:35:46

21 MR. HSU: Actually, so if it's going to be 15:35:49

22 another hour, let's at least take a 10-minute break 15:35:52

1	because we are coming up over an hour anyways.	15:35:55
2	MR. BALBAKY: Okay. I think that sounds	15:35:55
3	fine.	15:36:00
4	THE WITNESS: Yeah, I'm fine with that. I	15:36:00
5	can skip lunch, we'll take a 10-minute break, and	15:36:03
6	depending on what you have, I can try my best to	15:36:06
7	accommodate and plow through because I'm aware of	15:36:08
8	East Coast time difference, so I'll be willing to	15:36:13
9	accommodate it.	15:36:17
10	MR. BALBAKY: I think that sounds good.	15:36:18
11	Then we can take a 10-minute break right now.	15:36:21
12	THE WITNESS: Thank you.	15:36:21
13	MR. BALBAKY: Thank you.	15:36:25
14	THE VIDEOGRAPHER: We are going off the	15:36:25
15	record and the time is 3:36 p.m.	15:36:26
16	(Recess 3:36 p.m. - 3:46 p.m.)	15:36:29
17	THE VIDEOGRAPHER: We are back on the	15:46:23
18	record and the time is 3:46 p.m.	15:46:24
19	BY MR. BALBAKY:	15:46:28
20	Q Dr. Liu, before we took the break, as you	15:46:39
21	may recall, we were discussing Figure 7 as you	15:46:43
22	annotated in your reply declaration on paragraph 11	15:46:48

1 of your declaration, and I was going through a 15:46:54
2 little bit about what demarcates the different 15:46:57
3 pre-verify and verify stages. 15:47:00

4 So to continue in that vein for a little 15:47:04
5 bit, I want to understand better what the purposes 15:47:13
6 of these stages and what denotes the start and 15:47:22
7 endpoints. 15:47:27

8 So is there a particular feature of the 15:47:29
9 pre-pulse period that you have annotated that 15:47:35
10 indicates that it is a pre-verify stage? 15:47:41

11 MR. HSU: Objection; form. 15:47:48

12 A Can you -- can you take me to where -- 15:47:55
13 which -- what context of my reply declaration? 15:48:01
14 Because these annotation, this so-called pre-pulse 15:48:05
15 and verify, they are the annotation for patent '957. 15:48:11
16 I'm simply, for example, highlight some very obvious 15:48:27
17 stuff. I'm highlighting pre-pulse bracket, I 15:48:31
18 bracket the verify/read and I bracket the unselected 15:48:34
19 word lines -- 15:48:39

20 Q Yeah -- I'm sorry. 15:48:40

21 A So, so -- go ahead. 15:48:42

22 Q No, I'm asking in the context of the '957, 15:48:43

1 what does it mean to have a pre-verify stage? How 15:48:48
2 do you know that this pre-pulse stage is a 15:48:52
3 pre-verify stage? 15:48:56

4 A I think -- is it any part of my reply 15:49:00
5 declaration? Because I think some of this issue 15:49:03
6 might have been addressed in the initial 15:49:05
7 declaration. So is there a particular portion you 15:49:08
8 would like to discuss? I can -- that would help 15:49:11
9 facilitate the discussion. 15:49:14

10 Q Well, I'm asking generally, and based on 15:49:17
11 the figure that you've annotated here, what makes 15:49:19
12 something a pre-verify stage? 15:49:23

13 A I didn't annotate. I simply highlighted, 15:49:27
14 right. So what aspect in my reply declaration? I 15:49:30
15 just want to make sure I can answer your question 15:49:34
16 correctly because I don't -- I don't seem to 15:49:38
17 understand your question, so... 15:49:40

18 Q In Figure 7 what distinguishes the initial 15:49:47
19 stage from the pre-pulse stage? 15:49:50

20 A What you're really trying to do is to 15:50:24
21 perform a verify/read operation, okay. In the 15:50:27
22 context of '957, to perform that, especially after a 15:50:34

1 program verify application -- after a programming
2 operation, and so the read operation is serving now
3 as a verify operation, and there may be issue with
4 ESUM due to hot carrier effect. Therefore, you have
5 introduced before the verify and read operation, you
6 have this pre-verify operation. This is in the
7 context of '957. Okay? So...

15:50:40

15:50:44

15:50:49

15:50:57

15:51:01

15:51:07

15:51:09

8 Q So to clarify -- well, you say that after
9 programming you perform a verify operation and you
10 need to do something to address issues of ESUM,
11 which I believe is E-S-U-M, and hot carrier effects.
12 Did I understand that correctly?

15:51:24

15:51:31

15:51:37

15:51:44

15:51:52

13 A I'm just sort of paraphrasing what the
14 invention '957 is trying to allegedly teaching.

15:51:56

15:52:00

15 Q What -- and I'm trying to understand what
16 are the features, as shown in Figure 6, Figure 7,
17 Figure 8, Figure 9, all the ones that you described
18 in your reply declaration as claimed embodiments,
19 you know, I'm trying to understand what features of
20 those waveforms are required for something to
21 qualify as a pre-verify stage.

15:52:07

15:52:11

15:52:16

15:52:20

15:52:25

15:52:30

15:52:38

22 A Well, the pre-verify stage -- is there a

15:53:07

1	particular -- because I believe a lot of this issue	15:53:19
2	again would have been in the initial declaration, so	15:53:23
3	I --	15:53:28
4	Q Did you opine in your initial declaration	15:53:30
5	whether Figures 6, 7, 8 and 9 of the '957 patent	15:53:33
6	itself are claimed embodiments?	15:53:38
7	A I don't recall sitting right here.	15:53:47
8	Q But you did include in your reply	15:53:50
9	declaration your opinion is that Figures 6, 7, 8 and	15:53:56
10	9 are claimed embodiments of the '957. Is that	15:54:00
11	correct?	15:54:07
12	A It's I'm simply offering my opinion based	15:54:07
13	on what the specification in '957 indicate.	15:54:13
14	Q How do you know if something is a	15:54:16
15	pre-verify stage?	15:54:19
16	MR. HSU: Objection; form.	15:54:28
17	A Let me try to go to the -- perhaps go to	15:54:35
18	the specification trying to --	15:54:52
19	Q Take your time.	15:54:56
20	A Okay. Can you repeat your question again,	15:56:47
21	please? I'm sorry.	15:56:50
22	Q Yeah. I was asking what -- what features	15:56:52

1 of an operation or of a set of applied waveforms 15:57:02

2 qualify it as a pre-verify stage? 15:57:08

3 MR. HSU: Objection; form. 15:57:15

4 A So in the context at least -- this is not 15:57:16

5 definition but a description, at least in the 15:57:19

6 context of the '957 patent, and by that referring to 15:57:21

7 column 6, right, it says in the pre-pulse scheme, 15:57:27

8 which is pre-verify, the pass voltage such as 15:57:31

9 certain voltage can be applied to word lines of the 15:57:38

10 memory cells in the selected cell string. Of 15:57:40

11 course, because by applying the word line and the 15:57:43

12 voltage, this is voltage on the gate on the word 15:57:47

13 line will also go into the unselected string, of 15:57:50

14 course. 15:57:50

15 And then and while gate -- a gate terminal 15:57:53

16 of TSG transistors can be turned on an at unselected 15:57:58

17 memory cell string, which means that you have these 15:58:04

18 word line voltage or gate voltage on the word lines 15:58:09

19 turning on and you have the unselected cell string 15:58:13

20 turning on. Keep in mind that in the read 15:58:19

21 operation, actual verify or read operation you don't 15:58:23

22 want the unselected string -- unselected gate, 15:58:25

1	unselected string, you don't want the top select	15:58:33
2	gate of the unselected string to be turned on	15:58:39
3	because that will contribute to read error because	15:58:42
4	you don't know where the read current is coming	15:58:45
5	from. They may be sharing the same bit line. Okay.	15:58:45
6	So one feature, saving feature based on	15:58:50
7	this description, obviously, is that I am actually	15:58:52
8	turning on the unselected string such that I can --	15:58:54
9	I mean, the purpose in the reference and also in the	15:58:58
10	prior art, I can perhaps stage or precondition,	15:59:02
11	channel in such a way that I can minimize hot	15:59:07
12	carrier and I can minimize ESUM errors.	15:59:12
13	So that is the description of pre-verify	15:59:17
14	operation and that comes before the verify or read	15:59:21
15	operation, obviously, because in the verify/read you	15:59:25
16	want to make sure that the unselected string does	15:59:28
17	not contribute to any current, so you have to turn	15:59:31
18	off that top select gate transistor in the	15:59:33
19	unselected string.	15:59:37
20	So as such, and I think I already	15:59:38
21	bracketed it very well, so even though the patent	15:59:41
22	doesn't teach it, bracket very well, so-called	15:59:45

1	initial, which is never mentioned, just showing	15:59:49
2	there, nothing is happening, and it just basically	15:59:50
3	can be considered no operation, everything is	15:59:53
4	grounded, just nothing.	15:59:55
5	So pre-pulse, pre-verify in that	15:59:56
6	definition I just read to be the column 6, I just	15:59:59
7	read it to you, yeah, so...	16:00:03
8	Q So I'm sorry, can you just repeat the	16:00:04
9	exact line numbers, this is column 6, which sections	16:00:07
10	you cited?	16:00:10
11	A I'm sorry, column 6 starting at -- I guess	16:00:10
12	we can go through column 6 starting with 37 and	16:00:16
13	related example, just read the whole thing out, I	16:00:21
14	mean just for completeness sake, yeah. So obviously	16:00:25
15	the intent of this pre-pulse is to pre-stage is to	16:00:28
16	condition the unselected word line -- sorry. It's	16:00:33
17	getting late -- precondition the unselected string	16:00:37
18	so the channel potential will be -- will be proper	16:00:40
19	as well as the selected string, so their potential	16:00:43
20	and everything, the gradient as well as any	16:00:48
21	electron, whatever, will be flushed out, and just	16:00:54
22	make sure when you read it, it's not going to be	16:00:57

1	susceptible to any disturb or errors, yeah.	16:01:01
2	Q So thank you. I think I'm beginning to	16:01:03
3	understand. Let's just dig in a little bit here.	16:01:06
4	So for a pre-verify stage, would it be	16:01:09
5	fair to say that you are pre-conditioning the	16:01:13
6	unselected string? Is that correct?	16:01:16
7	A You are pre-conditioning unselected	16:01:21
8	string, but you're also pre-conditioning selected	16:01:29
9	string as well.	16:01:33
10	Q So you're pre-conditioning the unselected	16:01:34
11	string and the selected string?	16:01:37
12	A I believe so, yes.	16:01:39
13	Q And forgive me, I think you said it	16:01:41
14	earlier, but I didn't quite catch it. You said that	16:01:44
15	something has to be turned on to do that, to do the	16:01:47
16	pre-conditioning. What was that?	16:01:53
17	A Oh, yeah, it's right here, it's right	16:01:56
18	here. So in the pre-pulse scheme a pass voltage can	16:01:58
19	be applied on word lines of the memory cells. So,	16:02:06
20	again, word line in this case obviously means gate,	16:02:09
21	right, in the selected memory cell string --	16:02:13
22	(Court Reporter clarification.)	16:02:13

1	A	Let me, yeah --	16:02:29
2	Q	Let's just begin from the beginning,	16:02:31
3		sorry.	16:02:33
4	A	Okay.	16:02:33
5	Q	Slowly. Slower.	16:02:34
6	A	I'm sorry. I'm really sorry, yeah, I	16:02:36
7		apologize.	16:02:38
8		So it says right here pre-pulse scheme or	16:02:40
9		stage and the verify/read scheme or stage can be	16:02:45
10		included in the verify/read operation. In the	16:02:50
11		pre-pulse scheme also known as pre-stage, I guess, a	16:02:56
12		pass voltage such as 6.8 volts can be applied on	16:03:03
13		word lines, WLS, and I added the clarification that	16:03:09
14		they're also gates, of the memory cell in a	16:03:11
15		selective memory cell string.	16:03:15
16		But keep in mind we talked about earlier	16:03:18
17		even though it's only on the selected memory cell	16:03:20
18		string, but because the nature of the word line	16:03:24
19		layer or the gate layer is going to encapsulate	16:03:27
20		other unselected string, and which is clarified	16:03:30
21		later on in the next sentence, while gate terminals	16:03:33
22		of a TSG, TSG means top select gate, transistor can	16:03:38

1 be turned on at an unselected memory cell string. 16:03:44

2 Okay. So that means you are actually connecting the 16:03:48

3 unselected string by virtue of the word line or the 16:03:51

4 gate voltage on each memory cells are all turned on, 16:03:55

5 you actually also turn on the unselected string such 16:03:58

6 that -- I like to use the word, but I will go with 16:04:02

7 patent's language -- such that you can pre-stage or 16:04:09

8 pre-verify the channel potential so that you have a 16:04:12

9 better control of the channel potential for the 16:04:16

10 subsequent read operation without -- without causing 16:04:18

11 too much a disturb. 16:04:22

12 And as you will see that in my reply 16:04:24

13 declaration, Hongtao obviously made that very clear 16:04:28

14 what the requirement of these voltages should be 16:04:34

15 because he's also trying to, just like '957, he's 16:04:37

16 also trying to precondition his memory string. 16:04:40

17 So to that extent, to answer counsel's 16:04:43

18 question, is that that's what a pre-verify or 16:04:46

19 pre-pulse scheme is trying to accomplish. 16:04:52

20 Q I see. So you're saying that -- 16:04:56

21 A I haven't finished, sorry. 16:04:59

22 Q Sorry, I interrupted you. I apologize. 16:05:02

1 A So the distinguishing feature also is that 16:05:04
2 in the subsequent read operation if you have turned 16:05:07
3 on these unselected string, you have turned on the 16:05:11
4 unselected string meaning by turning on the top 16:05:16
5 select gate of these unselected string, you need to 16:05:20
6 make sure you shut them off because you don't want 16:05:23
7 the current, any leakage current coming from the 16:05:26
8 unselected string by the virtue of being turned on 16:05:29
9 to contribute to the actual sense amplify sensing 16:05:32
10 the selected string current because that will 16:05:34
11 introduce error, introduce a read error. So you 16:05:41
12 want to make sure in the verify stage because you 16:05:41
13 were asking me to distinguish demarcate, so in the 16:05:44
14 verify stage you would prefer you would need to have 16:05:47
15 that shut off. That would be one saving distinction 16:05:50
16 between the two. 16:05:53
17 Q Okay. So to summarize, then, one 16:05:54
18 distinction is that in the pre-verify stage you are 16:05:57
19 applying a pass voltage to the word lines of the 16:06:03
20 memory cells in the string while a gate terminal of 16:06:09
21 the TSG transistor can be turned on. But then in 16:06:12
22 the verify stage you would have to turn off the TSG 16:06:18

1	transistor?	16:06:24
2	MR. HSU: Objection; misstates prior	16:06:25
3	testimony.	16:06:28
4	A In general I would say that you, depending	16:06:28
5	on the scheme operation, in general I would only say	16:06:32
6	that for sure that in the actual verify or read	16:06:36
7	operation, the unselect TSG needs to be off. And in	16:06:42
8	certain cases during the pre-verify if you want to	16:06:52
9	flush out the unselected string you may choose to	16:06:56
10	turn on the TSG of the unselected string for a	16:06:59
11	duration, for certain duration.	16:06:59
12	Q Okay. So in the pre-verify you're going	16:07:05
13	to turn on the TSG for some duration, but that	16:07:07
14	duration could be different depending on the scheme?	16:07:11
15	A I think that's fair, yeah.	16:07:15
16	Q Okay. And then how do we know the -- so	16:07:20
17	other than making sure that the TSG is turned off,	16:07:27
18	are there any other features that denote a verify	16:07:34
19	stage?	16:07:42
20	MR. HSU: Objection; form.	16:07:43
21	A I think, based on what I just read in	16:07:48
22	column 6, and of course in the -- I guess I need	16:07:51

1 to -- need you to clarify your question, because 16:07:55
2 there are two stages, obviously, there will be -- 16:07:58
3 there will be differences and I don't know if -- if 16:08:01
4 you want to be enumerated, so... 16:08:15

5 Q Okay. Let me -- let me revise a little 16:08:18
6 bit. So before we were talking about how there's 16:08:20
7 some initial stage, some verify stage -- sorry -- 16:08:24
8 some pre-pulse or pre-verify stage, a verifying 16:08:28
9 stage, and then there's also a post-pulse stage and 16:08:32
10 a recovery stage. Is there any specific features 16:08:35
11 that distinguish a post-pulse stage from the verify 16:08:42
12 stage? 16:08:48

13 A Sorry, it's getting late in the day, so 16:08:49
14 the question is a little loaded. Can I ask for 16:08:54
15 indulgence to repeat the question to me, please. 16:08:57

16 Q Yeah. So I guess just as a bit of 16:09:00
17 introduction, you may recall that in Figures 6, 7, 16:09:03
18 8, 9 of the '957 it distinguished initial period, a 16:09:08
19 pre-pulse period, a verify/read period, a post-pulse 16:09:18
20 period and a recovery period. Do you recall that? 16:09:22

21 A Yes, I do. 16:09:26

22 Q Okay. My question is whether there are 16:09:28

1	any features that would distinguish a post-pulse	16:09:35
2	period from a verify period?	16:09:41
3	MR. HSU: Objection; scope.	16:09:44
4	A If we look at the column 6 in the	16:09:59
5	description of the pre-pulse and verify/read	16:10:04
6	operation they only mention initial and post-pulse.	16:10:06
7	They don't have any -- any teaching regarding the	16:10:09
8	requirement of the post-pulse. It's not part of	16:10:12
9	the -- I would say part of teaching of this	16:10:18
10	invention. So I'm opining on pre-pulse and verify.	16:10:20
11	I'm not opining for post-pulse or initial, yeah. So	16:10:25
12	that's not part of the claim limitation and	16:10:32
13	addressing -- that's not what '957 is addressing	16:10:34
14	beside in passing these -- these stages, yeah.	16:10:39
15	Q So to clarify -- or just let me rephrase.	16:10:50
16	In your experience, what would be the purpose of a	16:10:55
17	post-pulse stage?	16:10:58
18	MR. HSU: Objection; scope.	16:11:02
19	A Well, I have not analyzed in detail the	16:11:10
20	nuances of post-pulse. I was focusing on pre-pulse	16:11:13
21	and verify/read operation. I understand, as a	16:11:17
22	POSITA understand very well, and I don't think I	16:11:21

1 would like to, for the sake of being modest, I think 16:11:25
2 I understand quite well the nuances the pre-pulse 16:11:31
3 and verify/read in terms of the scope in terms of 16:11:33
4 people involved in this case, so I'm very happy to 16:11:37
5 discuss all the nuance, all the feature, and some of 16:11:41
6 them are listed in my reply declaration, the 16:11:47
7 intricacy and the novelty -- not novelty, the 16:11:52
8 intricacy or the interesting physics of pre-pulse 16:11:54
9 and verify/read operation. And it's a subject that 16:11:58
10 I'm quite passionate about, so I'm very happy to 16:12:03
11 discuss the pre-pulse and verify/read. But I 16:12:06
12 haven't analyzed the post-pulse or recovery because 16:12:09
13 they may have different -- may have different -- 16:12:11
14 different nuances and may apply it for different 16:12:21
15 context and I have not analyzed that, so... 16:12:25
16 Q So I understand that, and I could talk 16:12:30
17 about this for hours, but I think we'll spare you 16:12:33
18 that. 16:12:36
19 Let me rephrase slightly then. Is there 16:12:37
20 anything in particular that marks the end of a 16:12:45
21 verify stage? 16:12:49
22 A Well, one -- and, again, this is -- this 16:13:17

1 is not in the scope of the reply declaration, but 16:13:23
2 it's because given that you verify, you're trying to 16:13:27
3 ascertain the state of your selected memory cell. 16:13:32
4 So I think any time your voltage, the verify voltage 16:13:36
5 or read voltage, somebody would call a sent voltage 16:13:44
6 you apply on the word line or on the gate of the 16:13:47
7 selected memory cell no longer require to be that 16:13:50
8 level and I think -- and once the sensor have enough 16:13:56
9 time to detect the state of the memory cell whether 16:14:00
10 it has current or low current giving that 16:14:05
11 verification or sensing or read voltage on the word 16:14:09
12 line of the select memory cell, and that already 16:14:13
13 determined the state. And I think, just in general, 16:14:16
14 I think the verify or read operation has 16:14:21
15 accomplished its purpose. 16:14:25
16 And so for different, you know, you may -- 16:14:26
17 you may proceed to move to next stage, whether that 16:14:30
18 involve moving to a next verification level or 16:14:33
19 shutting down certain things, you know, it's really 16:14:37
20 architecture of the design. But I think once the 16:14:42
21 verify level that you set allows you to demarcate 16:14:48
22 whether it's a conduction or no conduction in terms 16:14:53

1 of current, meaning that you determine the state of 16:14:56
2 the memory cell, and I think that's pretty much 16:14:59
3 accomplishes the purpose of verify/read operation or 16:15:01
4 sensing operation. 16:15:06

5 Q Thank you. You have been very helpful. I 16:15:14
6 think I'm -- I have some more things I could ask, 16:15:26
7 but I don't know if it would be useful. I think you 16:15:29
8 already gave some very good explanations and I 16:15:31
9 appreciate your clarification on all the Figure 2, 16:15:36
10 Figure 3, and all the different stages and such. 16:15:40

11 If you don't mind, if we could take a 16:15:44
12 short break, maybe five minutes or so, and then I 16:15:46
13 think after that I may have nothing further, but I 16:15:52
14 want to just double-check. 16:15:55

15 MR. HSU: Of course. 16:15:57

16 A Sure, that's fine with me. Thank you. 16:15:58

17 THE WITNESS: The videographer, is the 16:16:10
18 videographer aware that we're going to -- 16:16:16

19 MR. BALBAKY: I'm not sure. He may have 16:16:18
20 stepped out for a moment. 16:16:20

21 THE VIDEOGRAPHER: Oh, sorry, I guess my 16:16:28
22 volume wasn't loud enough. I read us off the 16:16:28

Transcript of David Kuan-Yu Liu, PH.D.
Conducted on May 28, 2025

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1	record.	16:16:28
2	MR. BALBAKY: Okay. Thank you very much.	16:16:28
3	THE COURT REPORTER: I didn't hear it.	16:16:28
4	THE VIDEOGRAPHER: Off the record at 4:16	16:16:29
5	p.m.	16:16:31
6	(Recess 4:16 p.m. - 4:22 p.m.)	16:16:32
7	THE VIDEOGRAPHER: We are back on the	16:22:49
8	record and the time is 4:23 p.m.	16:22:50
9	MR. BALBAKY: Back on the record. Barring	16:22:56
10	any recross, I have no further questions for	16:22:58
11	Dr. Liu.	16:23:02
12	MR. HSU: No questions from petitioner.	16:23:04
13	THE VIDEOGRAPHER: All right. This marks	16:23:10
14	the end of the deposition and we are going off the	16:23:11
15	record at 4:23 p.m.	16:23:14
16	(Time noted: 4:23 p.m.)	16:23:20
17		
18	*****	
19		
20		
21		
22		

1 CERTIFICATE OF CERTIFIED SHORTHAND REPORTER

2 NOTARY PUBLIC

3 I, MONIQUE VOUTHOURIS, Certified Court
4 Reporter and Notary Public within and for the State
5 of New Jersey, do hereby certify:

6 That DAVID KUAN-YU LIU, PH.D., the witness
7 whose deposition is hereinbefore set forth, was duly
8 sworn by me before the commencement of such
9 deposition, and that such deposition was taken
10 before me and is a true record of the testimony, to
11 the best of my ability, given by such witness.

12 I further certify that the adverse party,
13 MICRON TECHNOLOGY, INC., was represented by counsel
14 at the deposition.

15 I further certify that the deposition of
16 DAVID KUAN-YU LIU, PH.D., occurred remotely, on
17 Wednesday, May 28, 2025, commencing at 11:03 a.m.
18 EST to 4:23 p.m. EST.

19 I further certify that I am not related to
20 any of the parties to this action by blood or
21 marriage, I am not employed by or an attorney to any
22 of the parties to this action, and that I am in no

1 way interested, financially or otherwise, in the
2 outcome of this matter.

3
4 IN WITNESS WHEREOF, I have hereunto set my
5 hand this 2nd day of June 2025.

6
7
8 

9 Monique Vouthouris, CCR, RPR, CRR

10 Notary Public of the State of New Jersey

11 My commission expires: April 8, 2029
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A			
abed	accomplish	104:6, 108:16,	adequately
3:13, 5:16	170:19	108:17, 119:7	20:8, 20:17
ability	accomplished	action	adjacent
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