

Micron Technology, Inc.
Petitioner
v.
Yangtze Memory Technologies Company, Ltd.
Patent Owner

Case No. IPR2024-00792
U.S. Patent No. 11,468,957

Micron's Hearing Demonstratives

August 7, 2025

Roadmap

- I. The IPR Grounds
- II. The 957 Patent
- III. Ground 1: Hongtao in view of Yu
- IV. Ground 3: Costa in view of Seo
- V. Ground 2: Suzuki

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- I. The IPR Grounds
- II. The 957 Patent
- III. Ground 1: Hongtao in view of Yu
- IV. Ground 3: Costa in view of Seo
- V. Ground 2: Suzuki

Instituted Grounds

Ground	Prior Art	Claims
1	Hongtao + Yu	1-6 obvious
3	Costa + Seo	1-6 obvious
2	Suzuki	1-6 anticipated

Paper 1 (Petition), 8.

Roadmap

I. The IPR Grounds

II. The 957 Patent

III. Ground 1: Hongtao in view of Yu

IV. Ground 3: Costa in view of Seo

V. Ground 2: Suzuki

Overview of the 957 Patent

The present disclosure describes embodiments generally related to apparatuses and methods for verifying/reading memory cells of a 3D-NAND memory device to reduce hot carrier injection (HCI)-induced edge summation (ESUM) loss, and reduce power consumption during verifying/reading the memory cells of the 3D-NAND memory device.

*Ex. 1001 (957 Patent), 1:44-49;
see also Paper 1 (Petition), 15-17.*

Claims of the 957 Patent

1. An apparatus for reading a memory device including a first memory cell string and a second memory cell string, the first memory cell string including a bottom-select-gate (BSG) transistor, memory cells, and a top-select-gate (TSG) transistor that are connected in series, the second memory cells string including a BSG transistor, memory cells, and a TSG transistor that are connected in series, the apparatus comprising:

processing circuitry configured to:

apply, in a pre-verify stage, a first verify voltage on a gate terminal of a selected memory cell of the first memory cell string, the selected memory cell being programmed and arranged between a first adjacent memory cell and a second adjacent memory cell;

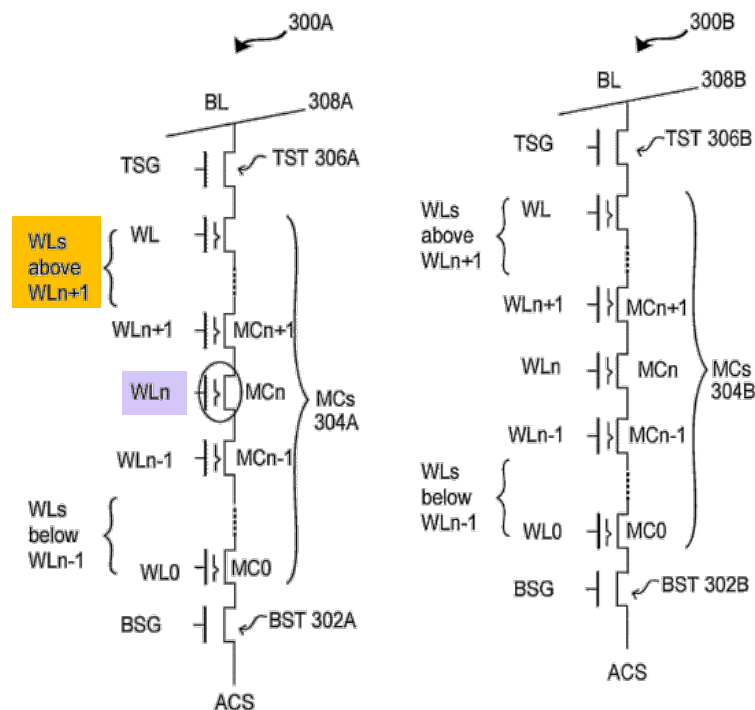
apply, in the pre-verify stage, a first bias voltage on a gate terminal of at least one memory cell of the first memory cell string that is not programmed;

apply, in a verify stage, a second verify voltage on the gate terminal of the selected memory cell of the first memory cell string; and

apply, in the verify stage, a second bias voltage on the gate terminal of the at least one memory cell of the first memory cell string that is not programmed, wherein the second bias voltage is smaller than the first bias voltage.

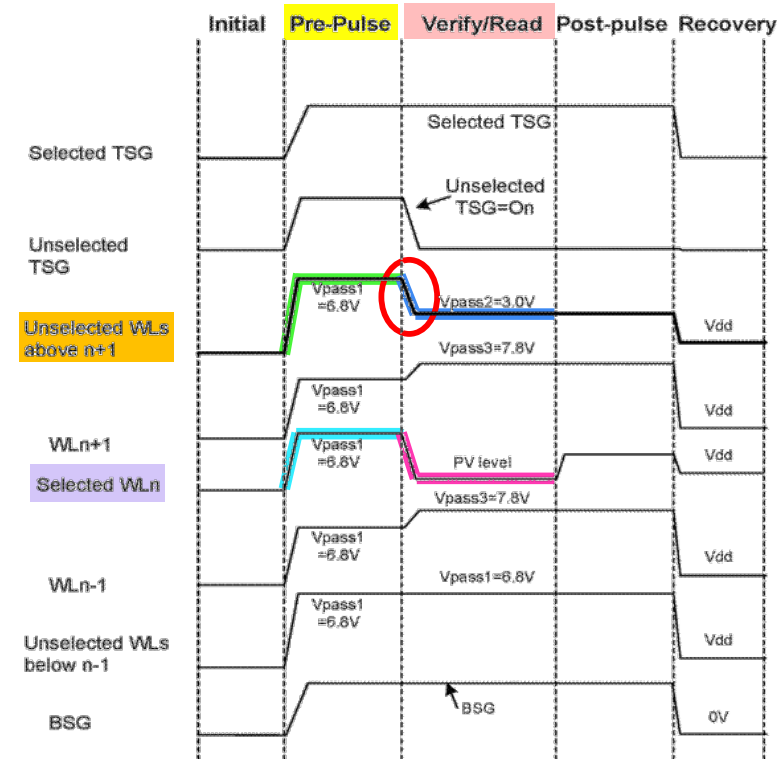
*Ex. 1001 (957 Patent), Claim 1;
see also Paper 1 (Petition), 15-17*

Claims of the 957 Patent



bias voltages on
unprogrammed cell

verify voltages on
selected cell



Ex. 1001 (957 Patent), Figs. 3, 6;
see also Paper 1 (Petition), 15-17.

Roadmap

- I. The IPR Grounds
- II. The 957 Patent
- III. Ground 1: Hongtao in view of Yu
- IV. Ground 3: Costa in view of Seo
- V. Ground 2: Suzuki

Overview of Hongtao

- Just like the 957 patent, Hongtao is directed to reducing hot carrier injection (“HCI”).

Paper 1 (Petition), 15, 21.

[0003] In the 3D NAND flash memory structure, three-dimensional arrangements are performed according to strings and rows. When the existing technology performs a read operation on a certain memory cell, it often causes read interference to other memory cells adjacent to the memory cell, causing data drift.

[0004] How to reduce read interference and improve the accuracy of read data during the reading process is an issue that needs to be solved urgently.

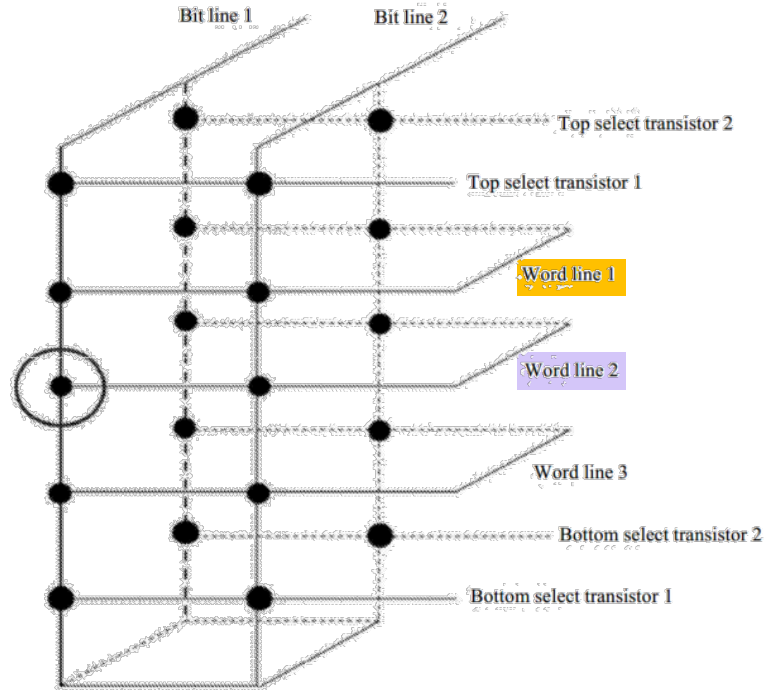
line remains at a low potential. In the specific embodiment of the present invention, the low potential is 0V. In other specific embodiments, the low potential can also be other voltage values. The channels of the unselected string and the selected string are connected to the bit line, and the channel potential will remain at the same low potential as the bit line. Therefore, the channels of the unselected string and the selected string will not generate voltage coupling due to changes in the word line voltage, thereby avoiding the problem of hot carrier injection crosstalk caused when a conduction voltage is applied to the word line of an unselected memory cell.

*Ex. 1005 (Hongtao), [0003]-[0004], [0023];
see also Paper 1 (Petition), 20-22.*

Overview of Hongtao

- Just like the 957 patent, Hongtao discloses two stages—a “pre-conduction phase” and a “read phase.”
- Notably, during the read phase, Hongtao applies on unselected word lines a conduction voltage that is lower than the pre-conduction voltage.

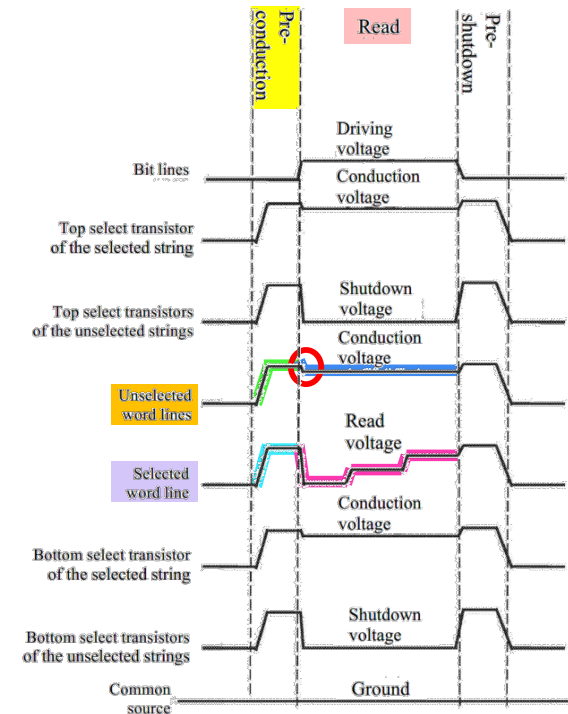
Paper 1 (Petition), 21-22.



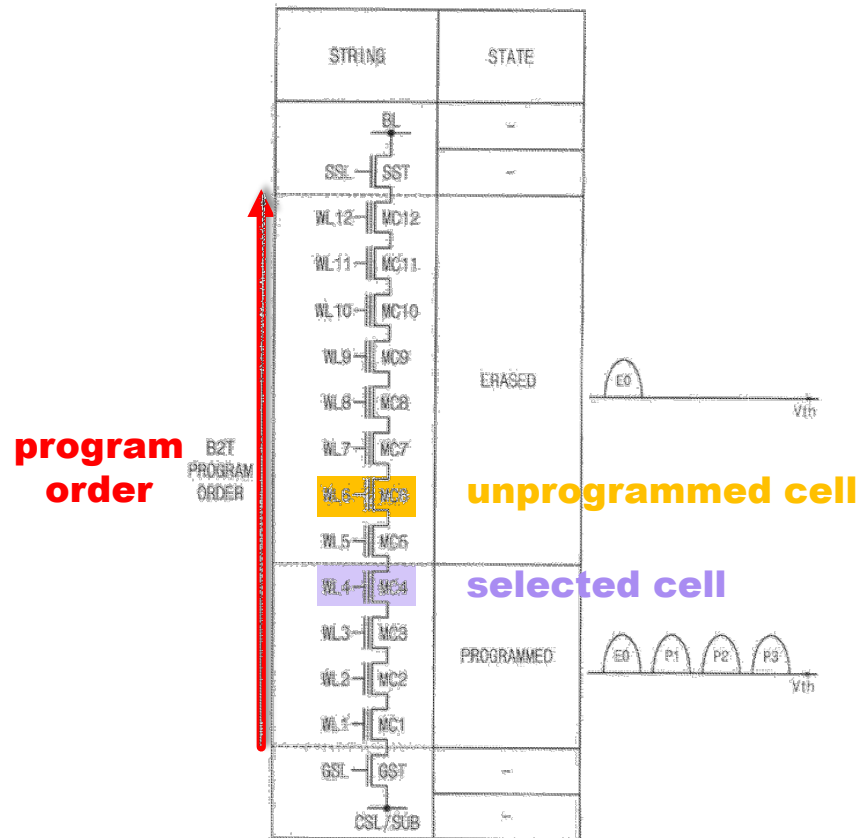
**bias voltages on
unprogrammed cell**

**verify voltages on
selected cell**

*Ex. 1005 (Hongtao), Figs. 1-2;
see also Paper 1 (Petition), 20-22.*



Overview of Yu



[0115] Referring to FIG. 11, according to a first program scenario, the program operation may be performed in an upward direction from a lowest word line. In other words, as the data stored in the memory block increase, the data may be filled in erased cells in the upward direction from bottom to top (B2T program order). The not-programmed memory cells MC5~MC12 are in an erased state E0, and each of the programmed memory cells MC1~MC4 may be in one of the erased state E0 and programmed states P1, P2 and P3. For example, at least one of the memory cells MC2~MC11 may be an intermediate switching transistor.

forming a sequence of program loops. Each program loop may include a program operation and a program verification operation. Each erase loop may include an erase operation

Ex. 1006 (Yu), Fig. 11, [0115], [0049];
see also Paper 1 (Petition), 22, 35, 72.

Summary: Patent Owner's Arguments

- For Claim 1, PO argues:
 1. Hongtao does not disclose applying voltages to gate terminals, but instead applies target voltages to word lines.
 2. Hongtao in view of Yu does not render obvious a verify operation.
 3. Hongtao in view of Yu does not render obvious a “pre-verify” stage.
- For Claims 5-6, PO argues that Hongtao does not disclose “apply[ing] a [top/bottom] bias voltage,” because the claims require the same voltage level across the pre-verify and verify stages.

Paper 17 (Response), 27, 30, 44.

Claim 1

- Claim 1 recites applying voltages on gate terminals for “reading a memory device” that includes “pre-verify” and “verify” stages.

1. An apparatus for **reading a memory device** including a first memory cell string and a second memory cell string, the first memory cell string including a bottom-select-gate (BSG) transistor, memory cells, and a top-select-gate (TSG) transistor that are connected in series, the second memory cells string including a BSG transistor, memory cells, and a TSG transistor that are connected in series, the apparatus comprising: processing circuitry configured to:

apply, in a pre-verify stage, a first verify **voltage on a gate terminal** of a selected memory cell of the first memory cell string, the selected memory cell being programmed and arranged between a first adjacent memory cell and a second adjacent memory cell;

apply, in the pre-verify stage, a first bias **voltage on a gate terminal** of at least one memory cell of the first memory cell string that is not programmed;

apply, in a verify stage, a second verify **voltage on the gate terminal** of the selected memory cell of the first memory cell string; and

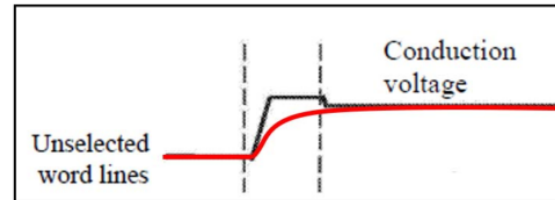
apply, in the verify stage, a second bias **voltage on the gate terminal** of the at least one memory cell of the first memory cell string that is not programmed, wherein the second bias voltage is smaller than the first bias voltage.

(1) Patent Owner's Argument that a (Target) Voltage Is Applied to a Word Line Fails

- Patent Owner argues: “as recognized by the '957, the target voltages applied to word lines via the contacts differ from the resulting voltages that develop on the gate terminals of the memory cells over time.”

Paper 17 (Response), 3; see also id., 5-6.

- Patent Owner adds its alleged “gate terminal” voltage to the Hongtao figure to distinguish Hongtao from the claims.



Id., 39-40.

- Patent Owner's argument fails:
 - A. Hongtao expressly discloses applying voltages to gate terminals.
 - B. As shown by the 957 patent and prior art, the art uses word line and gate terminal interchangeably—applying a voltage to a word lines is applying that voltage to the gate terminal.
 - C. Patent Owner's position leaves the 957 patent without any claimed embodiment and does not withstand scrutiny when considering real-world devices (or the description in the 957 patent itself).

Paper 20 (Reply), 1, 3.

(1)(A) Hongtao Expressly Discloses Applying Gate Terminal Voltages

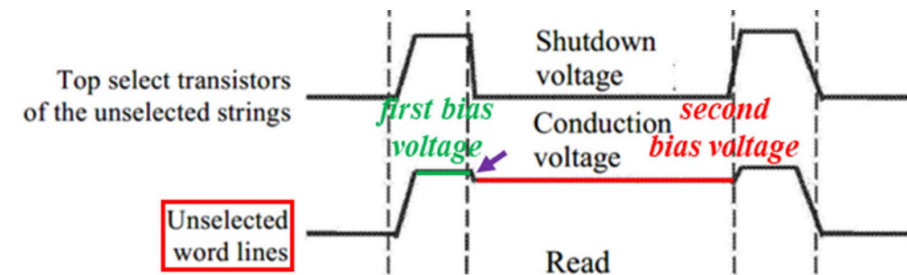
- Patent Owner's argument directly contradicts Hongtao's express disclosures.

Paper 20 (Reply), 7-8.

and the channel potential of the selected string is equal to the driving voltage on the bit line. The gates of the unselected memory cells on the selected string are applied with a conduction voltage through the unselected word lines. Therefore, the unselected memory cells on the selected string

Prelim. Resp. 24–31. Moreover, although Patent Owner argues that “Hongtao discloses voltages applied through word lines, rather than the resulting voltages applied to the gate terminals of corresponding memory cells” (*id.* at 28), we note that Hongtao states that “[t]he gates of the unselected memory cells on the selected string are applied with a conduction voltage through the unselected word lines” (Ex. 1005 ¶ 25). See also Ex. 1003 ¶ 56 (Dr. Liu testifying, with respect to claim 1 of the '957 patent's recitation of applying a voltage on a gate terminal of a memory cell, “[l]ike its reference to applying a voltage to a memory cell, the respective voltage is applied through a conductor coupled to the corresponding cell or transistor, i.e., a word line coupled to a corresponding memory cell (which in 3D memories, is actually a conductive gate layer).”).

Ex. 1005 (Hongtao), [0025]; see also Paper 1 (Petition), 39-40.



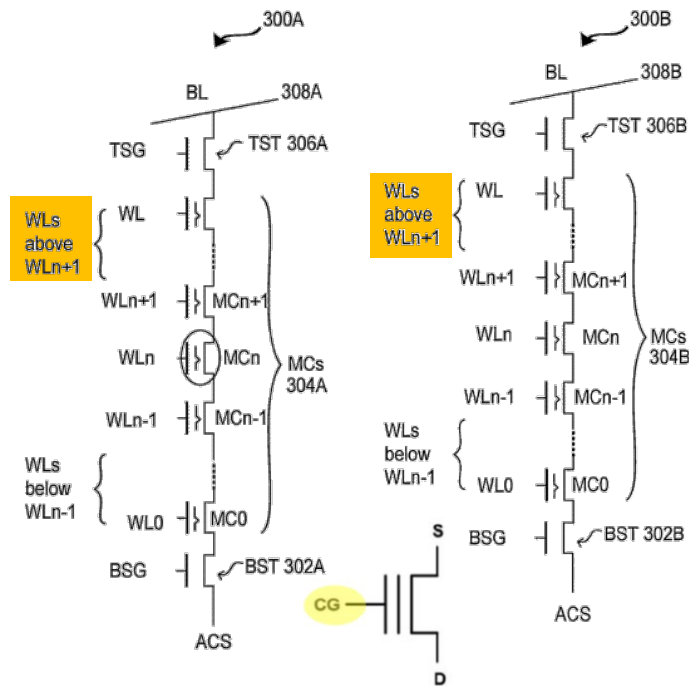
Ex. 1005 (Hongtao), Fig. 2 (partial); see also Paper 1 (Petition), 39-40.

Paper 13 (ID), 14-15.

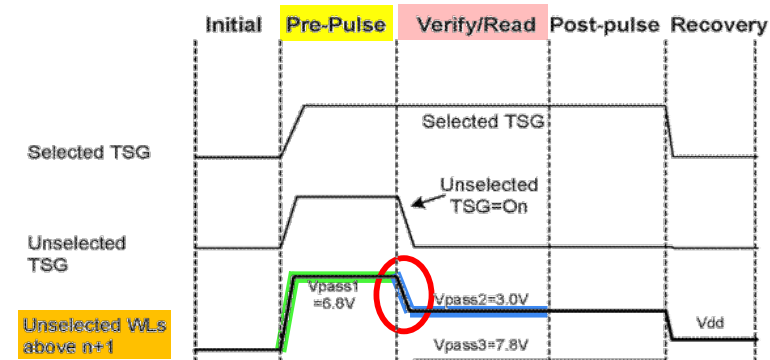
(1)(B): The 957 Patent Refers to Gate Terminals as Word Lines

- The 957 patent refers to gate terminals as word lines and describes applying bias voltages on word lines for the verify/read operation.

Paper 20 (Reply), 9-12.



*Ex. 1018 (Michelson Text), 81;
Ex. 1001 (957 Patent, Fig. 3);
see also Paper 20 (Reply), 10-11.*



pulse stage, and a recovery stage. The verify/read operation can be configured to verify whether memory cells are programmed successfully by applying appropriate bias voltages on the word line layers of the memory cells, the TSG layer of the TSG transistor, and the BSG layer of the BSG transistor. In an exemplary embodiment of FIG. 4, the

*Ex. 1001 (957 Patent), Fig. 6 (partial), 9:62-67;
see also Paper 1 (Petition), 16-17;
Paper 20 (Reply), 10-12.*

(1)(B) The Prior Art Interchangeably Refers to Word-Line Voltage and Gate-Terminal Voltage

- PO argues curved lines represent voltages applied to gate terminals.

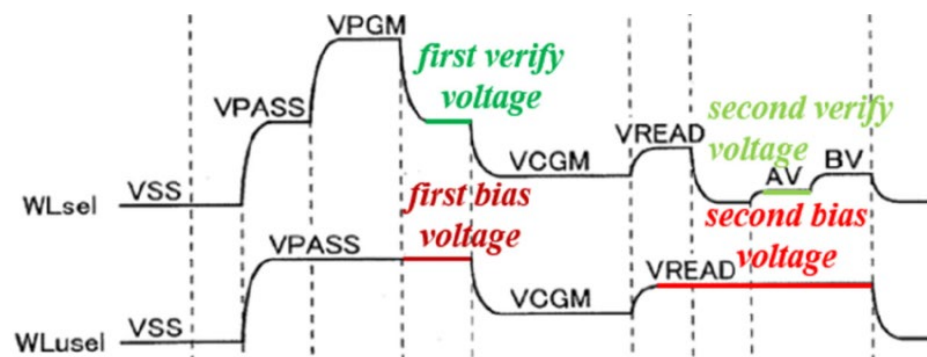
*Paper 20 (Reply), 37;
Paper 22 (Sur-Reply), 13.*

- PO agrees that Suzuki discloses applying voltages to the gate terminals.

Paper 17 (Response), 53, 57.

- Yet Suzuki describes applying voltages to word lines.

Paper 20 (Reply), 16.



[0138] At time t4, a voltage VCGM is applied to each of the word lines WLsel and WLusel. The voltage VCGM is a voltage higher than VSS and lower than VPASS and is, for example, 3 to 5V. When VCGM is applied to the word lines WLsel and WLusel, the channel voltage of the NAND string NS, which is in the floating state, drops due to the coupling between the channel and the control gate.

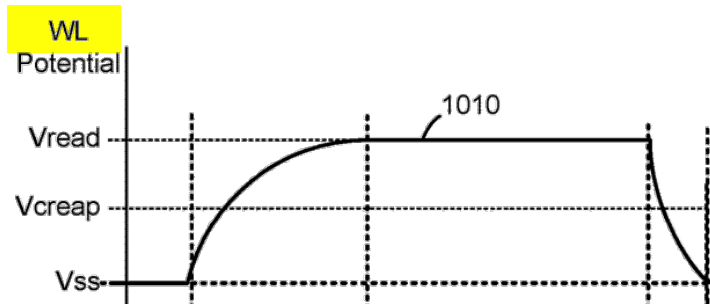
*Ex. 1007 (Suzuki), Fig. 11 (partial), [0138];
see also Paper 1 (Petition), 24;
Paper 20 (Reply), 16.*

(1)(B) The Prior Art Interchangeably Refers to Word-Line Voltage and Gate-Terminal Voltage

- **Lien** describes a gate voltage and illustrates it as a curved word line (“WL”) voltage.

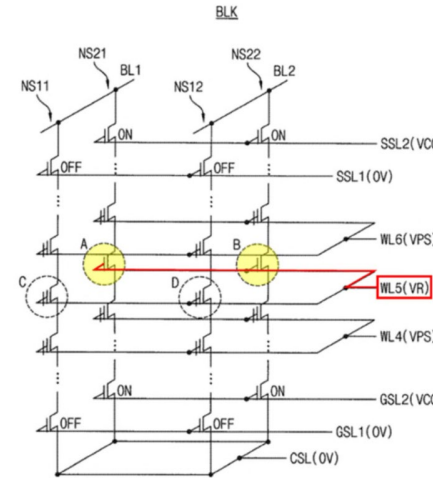
programming. A verify test can involve applying a control gate voltage of an assigned data state to the selected word line while sensing circuitry determines whether cells connected to the word line are in a conductive or non-conductive state. As in a read operation, the voltages of the

Ex. 1030 (Lien), 3:38-42; see also Paper 20 (Reply), 15.



Ex. 1030 (Lien), Fig. 10A (partial); see also Paper 20 (Reply), 19, 20.

- **Ko** illustrates a WL voltage VR and describes it as “applied to gates....”



Ex. 1021 (Ko), Fig. 13; see also Paper 20 (Reply), 15.

[0102] In this example read bias condition, the drain voltage of selected memory cells A and B is 0.5 V and the source voltage of selected memory cells A and B is 0 V. In addition, the selection read voltage VR is applied to gates of the selected memory cells A and B. Furthermore, a read

Ex. 1021 (Ko), [0102]; see also Paper 20 (Reply), 15.

(1)(C) Patent Owner's Argument Does Not Withstand Scrutiny When Considering a POSITA's Knowledge of Real-World Devices

- Patent Owner's argument means that it would be nearly impossible to figure out how long it takes for the target voltage to reach a memory cell—and that unknown time would be different for each memory cell.
- Program operations would not work because its timing would be different for each memory cell, since each memory cell would receive a different waveform.
- Tellingly, the 957 patent is silent on this fatal problem with Patent Owner's made-up distinction.

Paper 20 (Reply), 22-23.

A Yes. As we discussed at length earlier, for this particular circuit for a 3D NAND Flash, the RC delay is a complicated aggregation of distributed volt resistances and capacitances and a non-zero source resistance for the driver and a host of other factors which make it look essentially like exponential, a rising exponential.

be slightly different. And as we discussed earlier, memory cells that are closer to the word line driver will see different a time-constant than ones further away.

So there is -- in that sense, each word line layer demonstrates or a different RC delay based on where the destination is. Each memory cell is in a different physical location.

*Ex. 1031 (Przybylski Dep.) 204:22-205:8, 210:4-13;
see also Paper 20 (Reply), 22-23.*

(2) Patent Owner's Argument Against Obviousness of a Verify Operation Fails

- Patent Owner argues that “‘verifying’ and ‘reading[]’ ... are distinct operations ... using distinct voltages and biasing schemes.”

*Paper 22 (Sur-Reply), 7;
see also Paper 17 (Response) at 30.*

- Patent Owner's argument fails:
 - A. The Petition showed that it would have been obvious to use a read operation to verify programming with a reasonable expectation of success.
 - B. The two operations are not “distinct,” as demonstrated by their nearly identical operational features, the prior art, the 957 patent, and testimony of Dr. Przybylski (Patent Owner's expert).

*Paper 1 (Petition), 14-15, 72-74;
see also Paper 20 (Reply) at 23-24.*

(2)(A): The Petition Demonstrates That It Would Have Been Obvious to Employ Hongtao's Read Operation After a Program Operation—That Is, as a Verification

- The Petition demonstrates that after a program operation, a verification operation—that is, a read operation to read the data and verify the success of a program—is necessary.

As an initial matter, Yu discloses: “Each program loop may include a program operation and a program verification operation.” Yu, [0049]. This refers to the basic

Paper 1 (Petition), 72.

- The Petition shows that a way to perform this verification is with a read operation.

virtually identical. *Supra* §V.A.2 (citing Exs. 1017, 1019-1021). Indeed, “the read operation may include the verification read operation for verifying the success of the program operation or the normal read operation for determining the data stored in the memory cells.” Ex. 1021, [0103]. Further, it was well known that the program

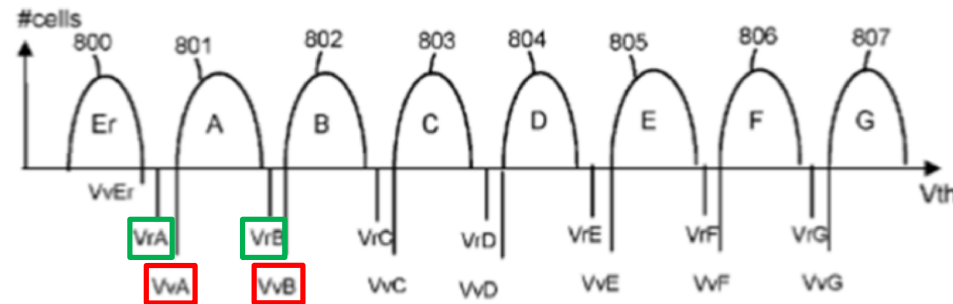
Id.

- The Petition demonstrates several advantages, including the necessity to verify the program and the benefit of using the same, fine-tuned read operation to avoid unnecessary design work. *Id.*, 73.
- The Petition shows that a POSITA would have had a high expectation of success, e.g., changing the read voltage to the verify voltage. *Id.*, 73-74.

(2)(B) A Verify Operation Is a Read Operation as Demonstrated by Their Nearly Identical Operational Features

- A read operation turns on all the non-selected word lines and applies a read voltage (two shown below).
- A verify operation turns on all the non-selected word lines and applies a verify voltage (two shown below).

Paper 20 (Reply), 23-24.



than two bits each. FIG. 8A depicts threshold voltage distributions when three bits are stored per memory cell. In this case, there are eight threshold voltage distributions 800-807, representing an erase state (Er), and states A through G. Verify voltages VvA, VvB, VvC, VvD, VvE, VvF, and VvG are depicted. Read reference voltages VrA, VrB, VrC, VrD, VrE, VrF, and VrG are depicted. Programming

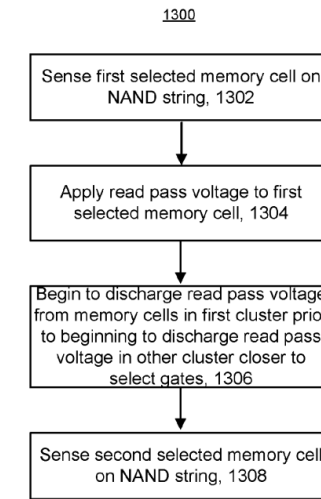
*Ex. 1017 (Dong), Fig. 8A, 15:15-21;
see also Paper 20 (Reply), 23-24.*

(2)(B) A Verify Operation Is a Read Operation as Shown in the Prior Art

- Both verify and read operations turn on all the non-selected memory cells and apply a specific voltage to the selected cell.
- This is also known as a sensing operation.

Paper 20 (Reply), 25; Ex. 1027 (Liu Reply) ¶¶ 69-74.

FIG. 13 is a flowchart of one embodiment of a process 1300 of sensing memory cells in which residual electrons are purged from a channel. The process 1300 may be used to sense one or more memory cells on a NAND string. The NAND string may be in a 3D architecture or a 2D architecture. In one embodiment, the memory cells have charge trapping layers. The sensing operation is a program verify, in one embodiment. The sensing operation is a read, in one embodiment. Process 1300 describes sensing a first selected



Ex. 1017 (Dong), 20:40-48, Fig. 13; see also Paper 20 (Reply), 25; Ex. 1027 (Liu Reply) ¶ 70.

- Put simply, a “read operation” is both for a normal read and a read after program (i.e., verification).

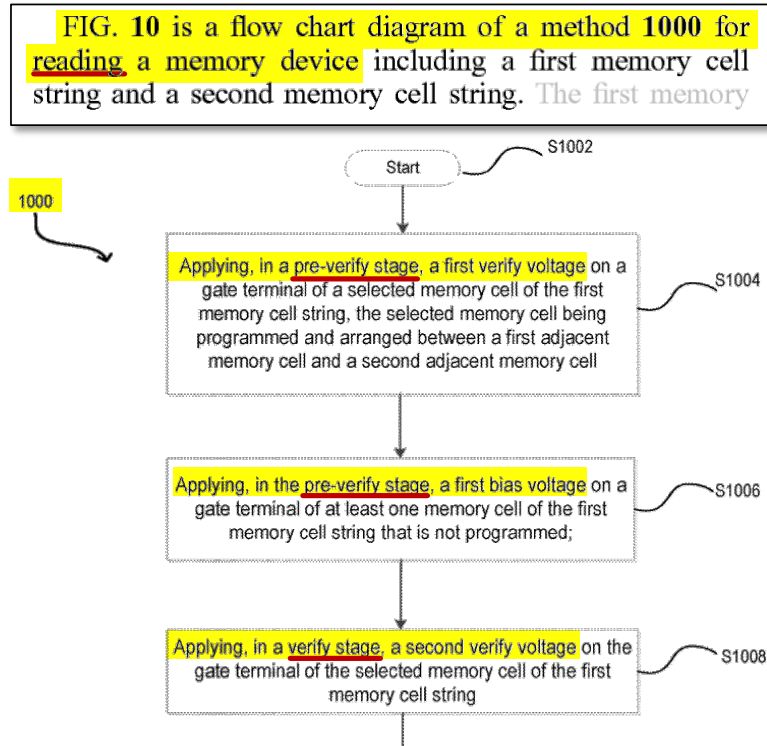
virtually identical. *Supra* §V.A.2 (citing Exs. 1017, 1019-1021). Indeed, “the read operation may include the verification read operation for verifying the success of the program operation or the normal read operation for determining the data stored in the memory cells.” Ex. 1021, [0103]. Further, it was well known that the program

Paper 1 (Petition), 72.

(2)(B) A Verify Operation Is a Read Operation as Shown by the 957 Patent Itself

- The 957 patent itself demonstrates that a verification operation is a read operation after a program.

Paper 20 (Reply), 24-25.



*Ex. 1001 (957 Patent), 15:31-33, Fig. 10 (partial);
see also Paper 20 (Reply), 24-25.*

1. An apparatus for reading a memory device including a first memory cell string and a second memory cell string, the first memory cell string including a bottom-select-gate (BSG) transistor, memory cells, and a top-select-gate (TSG) transistor that are connected in series, the second memory cells string including a BSG transistor, memory cells, and a TSG transistor that are connected in series, the apparatus comprising:

processing circuitry configured to:

apply, in a pre-verify stage, a first verify voltage on a gate terminal of a selected memory cell of the first memory cell string, the selected memory cell being programmed and arranged between a first adjacent memory cell and a second adjacent memory cell;
apply, in the pre-verify stage, a first bias voltage on a gate terminal of at least one memory cell of the first memory cell string that is not programmed;

MCs. In addition, a read (or verify) voltage can be applied on the gate terminal (or gate) of the selected memory cell MCn through a WL layer (e.g., WLn) that is coupled to the selected memory cell MCn. The read voltage can be equal to

*Ex. 1001 (957 Patent), Claim 1, 9:41-44;
see also Paper 20 (Reply), 25.*

(2)(B) A Verify Operation Is a Read Operation as Shown by the Testimony of Patent Owner's Expert

- Patent Owner's expert equated a verify operation with a read operation.

Paper 20 (Reply), 24.

Q How do read operations work?

A (Reviewing.)

Q Just to clarify, I'm asking this question just for NAND Flash memory --

A Yeah.

Q -- that existed at the time of the patent, not necessarily how the patent itself disclose or not disclose it. Is that fair?

A Okay. Because I don't think it actually discloses NAND -- let's see, it has read verify operations. In the most abstract, a read operation in a 3D NAND Flash memory device isolates one particular memory cell per string by putting all of the other transistors in the string into a conductive state, and

Ex. 1031 (Przybylski Dep.), 81:2-18; see also Paper 20 (Reply), 24.

(2)(B) A Verify Operation Is a Read Operation: an Optional Feature of Verify Is Irrelevant

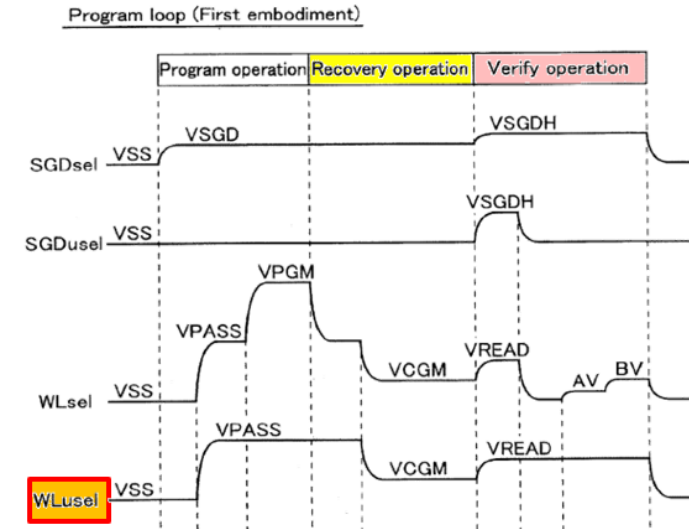
- Patent Owner's argument that read and verify operations are distinct because the programming states of the surrounding memory cells are known in verify operations (and thus Vpass on some word lines can be lowered) fails for two reasons.

Paper 17 (Response), 31.

- **First**, this is an optional feature.
- **Second**, this option is irrelevant to the claims.

① PO's argument that verify operations can use lower bias voltages on unprogrammed cell is irrelevant. POR, 31. As PO concedes, this is an optional "capab[ility]." *Id.* Suzuki's verify operation, for example, does not involve this capability. Ex. 1007, Fig. 11 (showing WL_{usel} for all unselected gates). ② Further, the claims do not require applying a voltage on the unprogrammed cells lower than that on the programmed cells during either the pre-verify or verify stage. Liu2 ¶ 73.

Paper 20 (Reply), 25.



Ex. 1007 (Suzuki), Fig. 11 (partial).

(3) Patent Owner's Argument that Hongtao Does Not Render Obvious a Pre-Verify Stage Fails

- Patent Owner argues that “Hongtao’s disclosure of ‘preparing’ for a reading operation does not equate to the ‘pre-verify’ portion of a two-stage verification.”

*Paper 22 (Sur-Reply), 10;
see also Paper 17 (Response), 31.*

- Patent Owner’s argument fails:

A. Hongtao discloses a discrete sensing stage for a verification.

B. Hongtao discloses a discrete pre-sensing stage (that is, pre-verification) before the sensing stage.
Thus, Hongtao discloses, or at least renders obvious, pre-verify and verify stages.

*Paper 1 (Petition), 31-34, 37-39;
Paper 20 (Reply), 26.*

(3)(A) Hongtao's Second Phase Is a Sensing Operation—the Verify Stage

- Hongtao's read phase senses information in the memory cell.

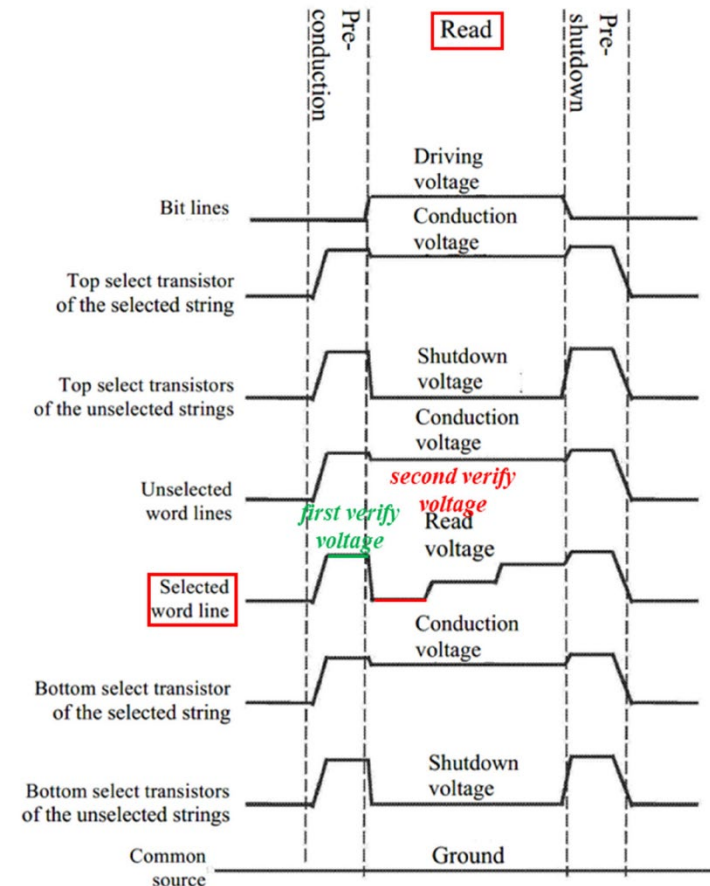
the row where it is located is used as the selected row. For example, to read the information of the selected memory cell circled in Figure 1, it is necessary to apply a driving voltage to bit line 1 and bit line 2, turn on the top select transistor 1 and the bottom select transistor 1 of the selected string where the selected memory cell is located, apply a conduction voltage to the word line 1 and word line 3 of the unselected rows other than the row where the memory cell is located, thereby turning on the channel of the selected string; in addition, turn off the top select transistor 2 and bottom select transistor 2 of the unselected string, and prevent the channels of other unselected strings from being turned on; apply a read voltage to the word line 2 of the selected row to read the information in the selected memory cell.

Ex. 1005 (Hongtao), [0019]; see also Paper 1 (Petition), 37-38.

- Hongtao's read phase performs the same sensing operation as verify.

FIG. 13 is a flowchart of one embodiment of a process 1300 of sensing memory cells in which residual electrons are purged from a channel. The process 1300 may be used to sense one or more memory cells on a NAND string. The NAND string may be in a 3D architecture or a 2D architecture. In one embodiment, the memory cells have charge trapping layers. The sensing operation is a program verify, in one embodiment. The sensing operation is a read, in one embodiment. Process 1300 describes sensing a first selected

Ex. 1017 (Dong), 20:40-48, Fig. 13; see also Ex. 1027 (Liu Reply) ¶¶ 69-74; Paper 20 (Reply), 25.



Ex. 1005 (Hongtao), Fig. 2; see also Paper 1 (Petition), 38.

29

(3)(B) Hongtao's First Phase Corresponds to the Pre-Verify

- Hongtao's pre-conduction phase pre-conditions the channel to reduce HCI for the operation.

Paper 1 (Petition), 21-22.

72. To reduce HCI, the channels of unselected strings and the selected string are kept “pre-conditioned” at 0V during the pre-conduction phase. This locking of the channel of the unselected string at 0V will remain in effect even during the sensing phase when the channel of the unselected string is disconnected from the bit line. Ex. 1005, [0022]-[0024]. As shown below, Hongtao's waveform matches

*Ex. 1003 (Liu Decl.), ¶ 72;
see also Paper 20 (Reply), 25.*

75. In summary, Hongtao attempts to reduce the HCI induced read disturb on the unselected strings by locking the channel voltage during the pre-conduction period, while also being cognizant of the “conduction voltage” on the unselected word lines not causing read disturb on the selected string due to the voltage difference of (conduction voltage – driving voltage) perpendicular to the channel.

*Ex. 1003 (Liu Decl.), ¶ 75;
see also Paper 20 (Reply), 26.*

(3)(B) Hongtao's Two Phases Correspond to the Pre-Verify and Verify Stages

- Like the 957 patent, Hongtao lowers its bias voltages from the pre-conduction phase to the read phase to reduce HCI.

Paper 1 (Petition), 21-22.

By introducing a lower bias voltage in the verify/read stage in the memory cells that are positioned above the upper adjacent memory cell MC_n+1 of the selected memory cell MC_n, the gradient of the channel potential of the selected memory cell string can be reduced. Accordingly, HCI cannot be generated from the selected memory cell to the upper adjacent memory cell of the selected memory cell in the selected memory cell string. Thus, the ESUM loss can be prevented.

Ex. 1001 (957 Patent), 12:63-13:4; see also Paper 17 (Response), 10.

line remains at a low potential. In the specific embodiment of the present invention, the low potential is 0V. In other specific embodiments, the low potential can also be other voltage values. The channels of the unselected string and the selected string are connected to the bit line, and the channel potential will remain at the same low potential as the bit line. Therefore, the channels of the unselected string and the selected string will not generate voltage coupling due to changes in the word line voltage, thereby avoiding the problem of hot carrier injection crosstalk caused when a conduction voltage is applied to the word line of an unselected memory cell.

Ex. 1005 (Hongtao), [0023]; see also id., [0003]-[0004]; Paper 1 (Petition), 20-22; Ex. 1003 (Liu Decl.), ¶ 75.

Summary: Patent Owner's Arguments

- For Claim 1, PO argues:
 1. Hongtao does not disclose applying voltages to gate terminals, but instead applies target voltages to word lines.
 2. Hongtao in view of Yu does not render obvious a verify operation.
 3. Hongtao in view of Yu does not render obvious a “pre-verify” stage.
- For Claims 5-6, PO argues that Hongtao does not disclose “apply[ing] a [top/bottom] bias voltage,” because the claims require the same voltage level across the pre-verify and verify stages.

Paper 17 (Response), 27, 30, 44.

Claim 5

- Claim 5 requires each of a bottom bias voltage and a top bias voltage, along with a positive voltage, to be applied in both the pre-verify and verify stages:

Paper 20 (Reply), 4-5.

5. The apparatus of claim 2, wherein the processing circuitry is further configured to:
- apply a bottom bias voltage on a gate terminal of the BSG transistor of the first memory cell string in the pre-verify stage and the verify stage;
 - apply a top bias voltage on a gate terminal of the TSG transistor of the first memory cell string in the pre-verify stage and the verify stage; and
 - apply a positive voltage on gate terminals of any memory cells that are positioned between the second adjacent memory cell of the selected memory cell and the BSG transistor of the first memory cell string in the pre-verify stage and the verify stage.

Ex. 1001 (957 Patent), Claim 5.

Summary: Patent Owner's Arguments

- Claims 5-6: Patent Owner argues that the “top” and “bottom” limitations “require[] a single voltage level be applied in both the pre-verify stage and the verify stage.”
- Patent Owner then argues that Hongtao fails to disclose these limitations, because the bias voltages do not have a “single voltage level.”

Paper 17 (Response), 13, 44-45.

- Patent Owner's argument fails, because it relies on a legally erroneous construction that violates multiple claim construction rules:
 1. It attempts to rewrite the claims.
 2. The specification does not limit a “bias voltage” to a single voltage level: it includes a voltage that changes over time.
 3. The “positive voltage” claim limitation with the same claim structure demonstrates that Patent Owner's construction cannot be correct.
 4. Patent Owner's “gate terminal” voltage argument undermines its claim construction.

Paper 20 (Reply), 3-7.

(1) Patent Owner Attempts to Rewrite the Claims

- Patent Owner argues that the top and bottom limitations “require[] a **single voltage level** be applied in both the pre-verify stage and the verify stage.”

Paper 17 (Response), 13.

these two stages. POR 13-17. The plain meaning of applying “a ... bias voltage ... in the pre-verify stage and the verify stage,” as recited in the claims, requires that the same voltage level be applied in both the pre-verify stage and the verify stage.

Paper 22 (Sur-reply), 1; see also Ex. 2003 (Przybylski decl.) ¶ 48.

- Patent Owner attempts to rewrite the claims *from* “apply[ing] a [top/bottom] bias voltage” *to* “apply[ing] a **single** [top/bottom] bias voltage **level**.”
- Patent Owner cites no legal basis that would support its rewrite.

Paper 20 (Reply), 3.

(2) The 957 Specification Does Not Limit a Bias Voltage to a Particular, Static Voltage Level

- The bias voltages are not a voltage level. For example, the voltage may increase.

Paper 20 (Reply), 3-4.

The bottom bias voltage applied on BSG transistor can be increased from the initial voltage to a target value (e.g., 5 volts) in the first portion of the pre-pulse stage, where the target value is equal to the bottom bias voltage of the verify/read stage. The bottom bias voltage can be maintained through the second portion of the pre-verify stage and the verify stage. Similarly, the top bias voltage applied on the selected TSG transistor can be increased from the initial voltage to a target value (e.g., 5 volts) in the first portion of the pre-pulse stage. The top bias voltage can further be

In some embodiments, the bottom bias voltage can be increased from the initial voltage to a voltage that is maintained through the second portion of the pre-verify stage and the verify stage. The top bias voltage can be increased from the initial voltage to a voltage that is maintained through the second portion of the pre-verify stage and the verify stage. The positive voltage can be increased from the initial voltage in the pre-verify stage.

*Ex. 1001 (957 Patent), 13:43-52, 2:56-63;
see also Paper 20 (Reply), 3-4.*

- All that the claims require is a “bias voltage,” even if changing, be applied on the gate terminal in both stages.

*Paper 20 (Reply), 6-7; Thorner v. Sony Comput. Ent. Am. LLC, 669 F.3d 1362, 1369 (Fed. Cir. 2012)
(reversing construction that is inconsistent with patent’s disclosure).*

(3) The “Positive Voltage” Claim Limitation with the Same Claim Structure Demonstrates that Patent Owner’s Construction Cannot Be Correct

- The “positive voltage” does not reach a flat level until the verify stage.

Paper 20 (Reply), 4-5 (Fin Control Sys. Pty, Ltd. v. OAM, Inc., 265 F.3d 1311, 1318 (Fed. Cir. 2001)).

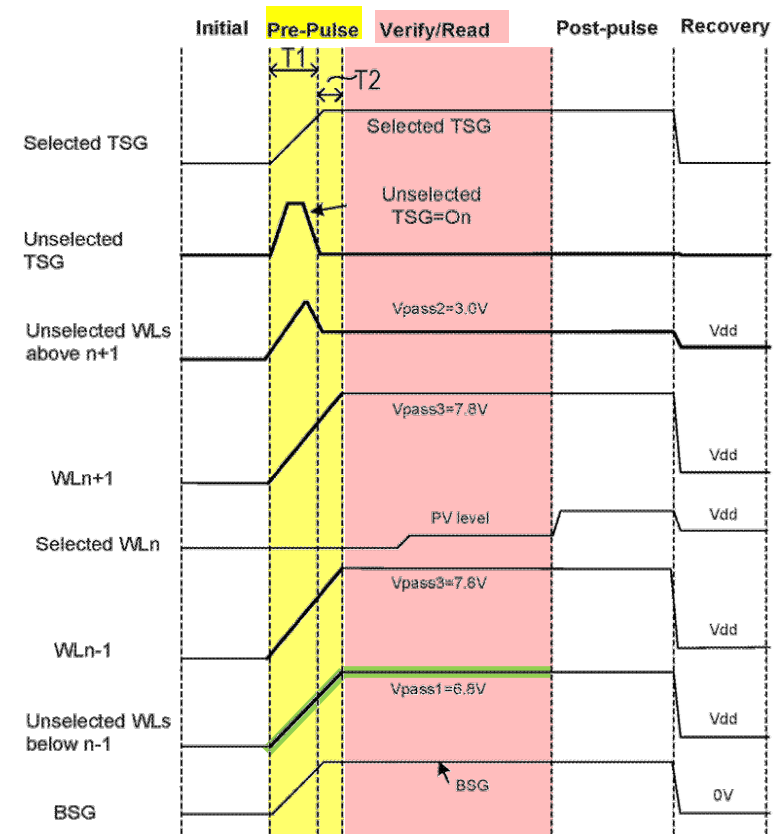
5. The apparatus of claim 2, wherein the processing circuitry is further configured to:

apply a bottom bias voltage on a gate terminal of the BSG transistor of the first memory cell string in the pre-verify stage and the verify stage;

apply a top bias voltage on a gate terminal of the TSG transistor of the first memory cell string in the pre-verify stage and the verify stage; and

apply a positive voltage on gate terminals of any memory cells that are positioned between the second adjacent memory cell of the selected memory cell and the BSG transistor of the first memory cell string in the pre-verify stage and the verify stage.

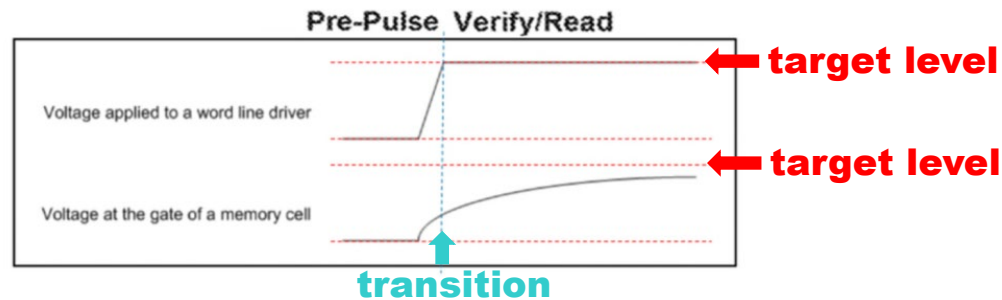
Ex. 1001 (957 patent), Claim 5, Fig. 7; see also id., Claim 6, Fig. 9; Paper 20 (Reply), 4-5.



(4) Patent Owner's "Gate Terminal" Voltage Argument Undermines Its Claim Construction Position

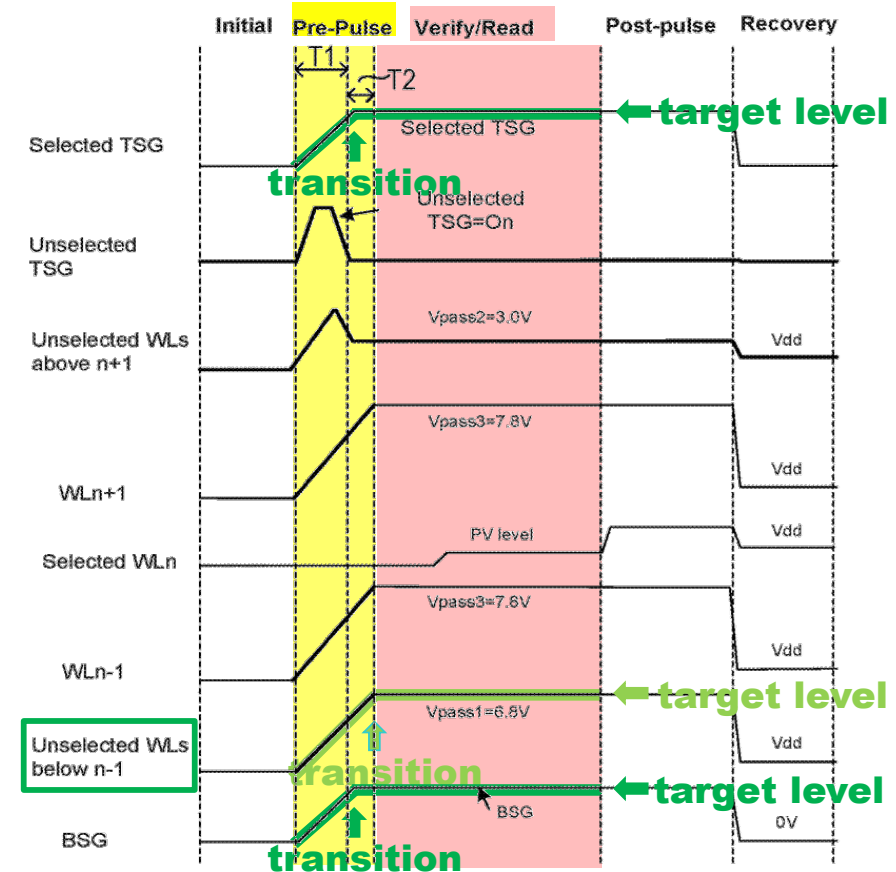
- Patent Owner argues that straight-line voltages in patent figures indicate that the voltage will be delayed before developing at the gate terminal.

Paper 20 (Reply), 5 (citing POR, 36-37).



- Thus, the positive voltage in the Figure 7 and 9 embodiments would never be at the same level in both stages to satisfy Patent Owner's construction because the transition to a horizontal level would occur later than shown in 957 figures.

Paper 20 (Reply), 6.



*Ex. 1001 (957 Patent), Fig. 7;
see Paper 20 (Reply), 5.*

Patent Owner's Case Law Does Not Support Its Position

- E.g., Patent Owner cites to *SonicWall* for the proposition that regardless of the number of bias voltages, the “claims require the same component to perform multiple functions or satisfy multiple limitations of a claim.”

Paper 17 (Response), 15 (citing Finjan LLC v SonicWall, Inc., 84 F.4th 963, 974-975 (Fed. Cir. 2023)).

- It is beyond dispute that a “bias voltage” may change, that is, it need not be at a single level.
- Thus, all that the claims require is that this same, changing “bias voltage” be applied to the respective gate terminals in both stages.

Paper 20 (Reply), 6-7.

Roadmap

- I. The IPR Grounds
- II. The 957 Patent
- III. Ground 1: Hongtao in view of Yu
- IV. Ground 3: Costa in view of Seo
- V. Ground 2: Suzuki

Overview of Costa

- Costa teaches applying a low pass voltage (among various pass voltage levels) to unprogrammed word lines during the verify (sense) operation.

Paper 1 (Petition), 111-12.

Sensing in non-volatile memory is performed using bias conditions that are dependent on the position of a selected memory cell within a group of non-volatile memory cells. During sensing, a selected memory cell receives a reference voltage while the remaining memory cells receive a read or verify pass voltage. For at least a subset of the unselected memory cells, the pass voltage that is applied is dependent upon the position of the selected memory cell in the group.

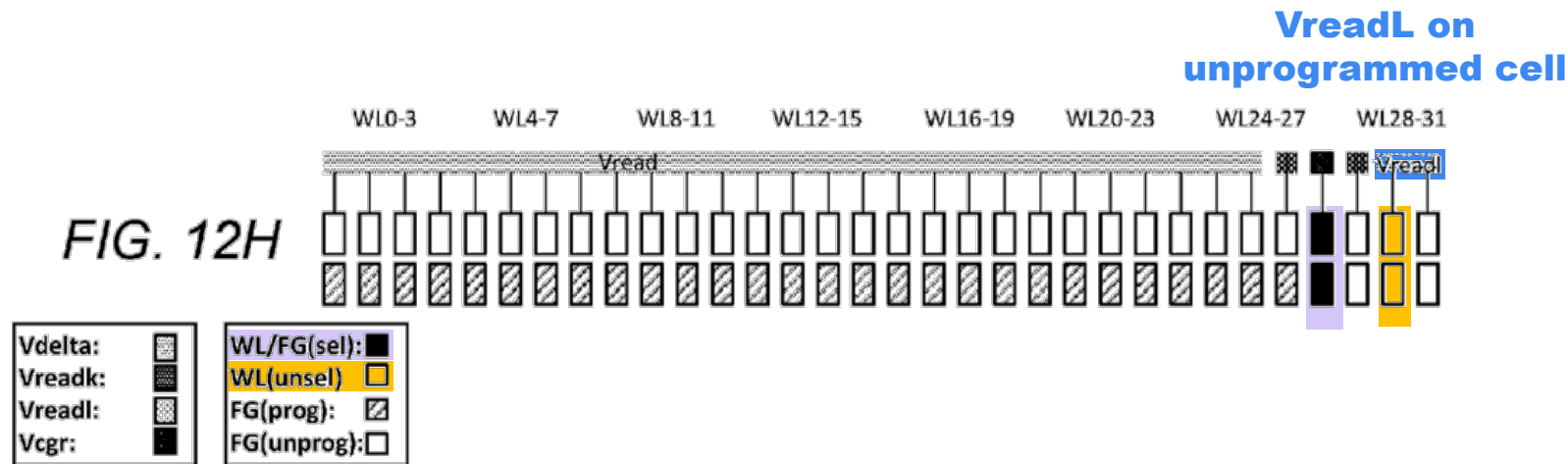
[0147] In FIG. 12H, WL28 in Zone 7 is selected for verification and receives Vcgr. The adjacent unselected word lines WL27 and WL29 receive Vreadk and unselected word lines WL30-WL31 receive the low read pass voltage Vreadl.

*Ex. 1008 (Costa), Abstract, [0147];
see also Paper 1 (Petition), 25-26, 111-12.*

Overview of Costa

- Costa teaches applying a low pass voltage (among various pass voltage levels) to unprogrammed word lines during the verify (sense) operation.

Paper 1 (Petition), 111-12.



*Ex. 1008 (Costa), Fig. 12H;
see also Paper 1 (Petition), 25-26, 111-12.*

Overview of Seo

- Seo teaches applying the standard, high Vpass voltage before sensing to reduce HCI.

Paper 1 (Petition), 108, 112.

[0008] Various embodiments are directed to a memory device capable of improving a disturb phenomenon of an unselected memory string during a read operation.

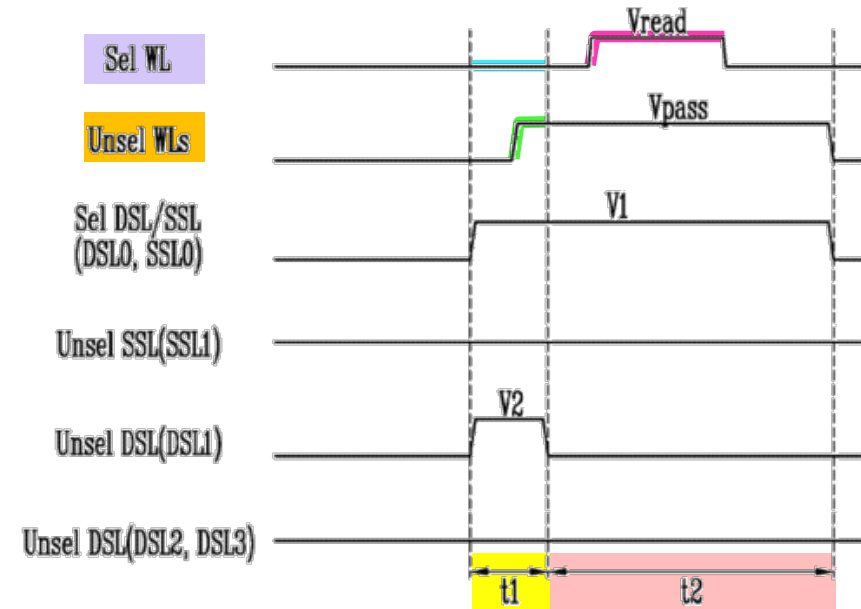
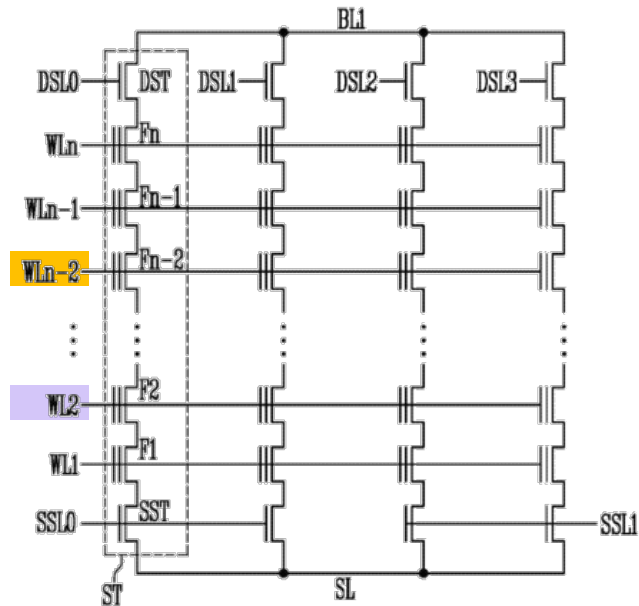
[0089] Subsequently, the pass voltage Vpass may be applied to unselected word lines Unsel WLs. Even when the pass voltage Vpass is applied to the unselected memory string which shares the first source select line SSL0 with the selected memory string, because the source select transistor SST and the drain select transistor DST are turned on, a local boosting phenomenon might not occur in a channel of the pass voltage Vpass of the unselected memory string which shares the first source select line SSL0 with the selected memory string. Accordingly, a disturb phenomenon caused by Hot Carrier Injection (HCI) may be improved.

*Ex. 1009 (Seo), [0008], [0089];
see also Paper 1 (Petition), 26-27.*

Overview of Seo

- Seo's HCI-reduction technique uses a two-phase read operation.

Paper 1 (Petition), 127-28.



*Ex. 1009 (Seo), Figs. 4, 8;
see also Paper 1 (Petition), 26-27.*

Summary: Patent Owner's Arguments

- For Claim 1, PO argues:
 1. Costa in view of Seo does not render obvious applying voltages to gate terminals, but instead applies voltages to word lines (or target voltages to word lines).
 2. Costa in view of Seo does not render obvious a “verify” operation with a “pre-verify stage.”
 3. Costa in view of Seo does not render obvious “wherein the second bias voltage is smaller than the first bias voltage”

Paper 17 (Response), 58-59.

(1) Costa in View of Seo Renders Obvious Applying Gate Terminal Voltage

- Claim 1: For all the same reasons as Ground 1, Patent Owner's argument fails.

Paper 20 (Reply), 28.

target threshold voltage ranges. For example, FIG. 10 shows a portion of a signal applied to the control gates of a plurality of memory cells connected to a common word line.

*Ex. 1008 (Costa), [0085];
see also Paper 20 (Reply), 15.*

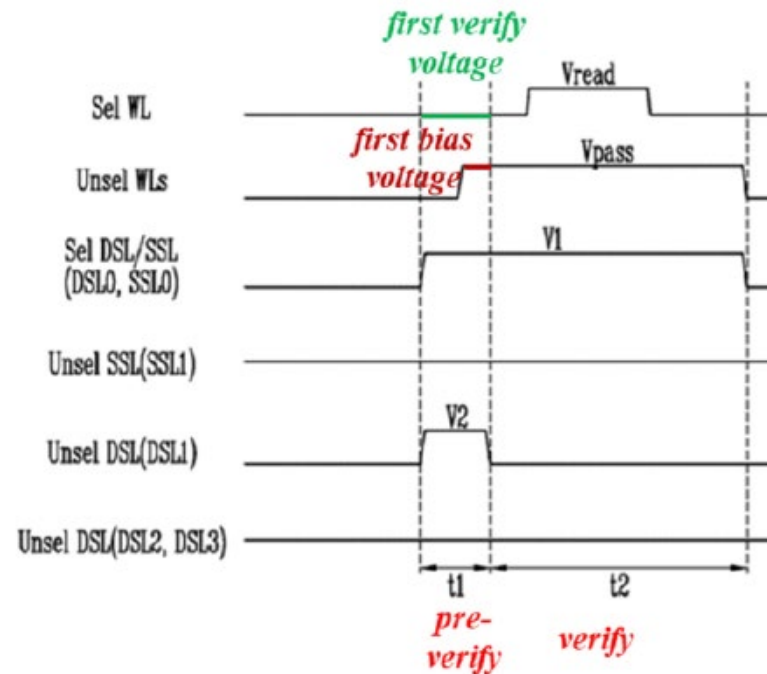
Program Verification Bias By Selected WL Zone

	Zone 0	Zone 1	Zone 2	Zone3	Zone 4	Zone 5	Zone6	Zone 7
BL	Vpre	Vpre	Vpre	Vpre	Vpre	Vpre	Vpre	Vpre
SGD	VSG	VSG	VSG	VSG	VSG	VSG	VSG	VSG
WL(Drain)	VreadL	VreadL	VreadL	VreadL	VreadL	VreadL	VreadL	VreadL
WL(n+1)	VreadK	VreadK	VreadK	VreadK	VreadK	VreadK	VreadK	VreadK
WL _n	Vcgr	Vcgr	Vcgr	Vcgr	Vcgr	Vcgr	Vcgr	Vcgr
WL(n-1)	VreadK	VreadK	VreadK	VreadK	VreadK	VreadK	VreadK	VreadK
WL(source)	Vread-700	Vread-600	Vread-500	Vread-400	Vread-300	Vread-200	Vread-100	Vread
SGS	VSG	VSG	VSG	VSG	VSG	VSG	VSG	VSG
SL	0V	0V	0V	0V	0V	0V	0V	0V

*Ex. 1008 (Costa), Fig. 10;
see also Paper 20 (Reply), 15.*

(2) Costa in View of Seo Renders Obvious a Verify Operation with a Pre-Verify Stage: Seo's Two Phases

- t2 involves applying the “Vread” voltage to sense the selected memory cell and is thus the read or verify stage.
- t1, which comes before this, is the pre-verify stage that reduces HCI.



*Paper 20 (Reply), 28-29; see also
Ex. 1027 (Liu Reply), ¶¶ 87-88.*

*Ex. 1009 (Seo), Fig. 8; see also
Paper 20 (Reply), 30.*

(2) Costa in View of Seo Renders Obvious a Verify Operation with a Pre-Verify Stage: Costa in View of Seo

- Costa expressly discloses a read operation (sensing) and its use for verification.

Paper 1 (Petition), 103, 106.

[0093] FIG. 8 is a cross-sectional view of an example of a NAND string during sensing. The NAND string in this example includes 128 data word lines per block and four dummy word lines that are not used to store user data. Sensing may be performed during reading, program verification, monitoring, detecting, probing, etc. Sensing generally refers to any determination or approximation of a condition associated with a memory cell. Sensing may refer

*Ex. 1008 (Costa), [0093]; see also
Paper 1 (Petition), 103, 106.*

- The Petition demonstrates that it would have been obvious to apply Seo's HCI-reduction technique (in the first phase) as a pre-verify stage to Costa's verify operation to improve Costa.

Paper 1 (Petition), 15, 126-28.

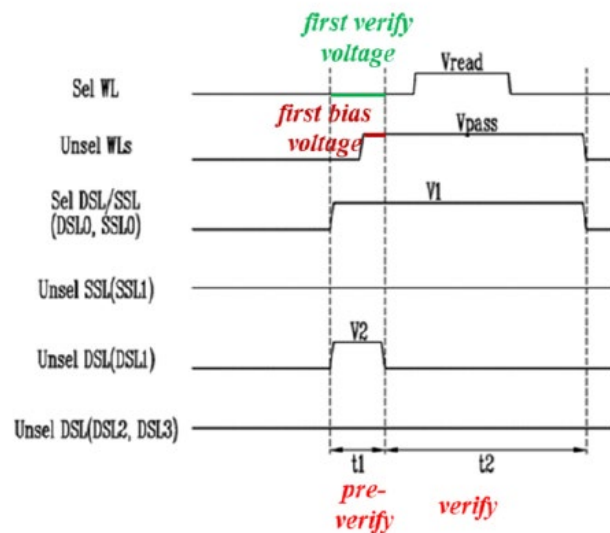
(2) Costa in View of Seo Renders Obvious a Verify Operation with a Pre-Verify Stage: Seo's Two Phases

- The Petition demonstrates that a POSITA would have been motivated to apply Seo's pre-verify HCI-reduction technique to Costa's verify operation.

Paper 1 (Petition), 126-28.

- Seo applies voltages in a time period t_1 **before** the read operation to reduce HCI.

Id., 27.



Ex. 1009 (Seo), Fig. 8; see also
Paper 20 (Reply), 30.

89. Seo reduces HCI by applying voltages in a time period t_1 before the

read operation that match the claimed '957 voltages. Ex. 1009, [0088]-[0089]. A

POSITA would recognize that, just like Hongtao and the '957 patent, Seo is locking

the channel voltage of the unselected memory string during the pre-verify period,

with the exception that the channel voltage of the memory cells above the selected

WL are pre-conditioned to the bit line voltage, while the channel voltage of the

memory cells below the selected WL are pre-conditioned to 0V, due to the fact that

the selected WL is biased at 0V.

Ex. 1003 (Liu Decl.) ¶ 89; see also *Paper 1 (Petition)*, 27.

(3) Costa in View of Seo Renders Obvious “Wherein the Second Bias Voltage Is Smaller Than the First Bias Voltage”: The Petition

- The Petition demonstrates that Costa and Seo focus on two different phenomena that impact the reliability of memory devices.
- Costa focuses on issues around channel resistance and teaches techniques to address these issues **during the verification stage**.
 - Specifically, those techniques involve using a low Vpass (“VreadL”) **during verification**.

*Paper 1 (Petition), 127-28,
Ex. 1003 (Liu Decl.) ¶¶ 306-07.*

in one example. For example, VreadL may be several millivolts less (e.g., 5.2V) than the standard read pass voltage Vread. The lower read pass voltage VreadL may be used because the word lines on the drain side have not undergone programming, and thus the corresponding memory cells should be in the erased state. Accordingly, a lower read pass voltage VreadL can be used while still ensuring that these memory cells operate as pass gates. Additionally, the lower level of VreadL may cause less read disturb whereby a memory cell is unintentionally programmed by the read pass voltage.

*Ex. 1008 (Costa), [0122]; see
also Paper 20 (Reply), 29-30;
Ex. 1027 (Liu Reply) ¶ 93.*

(3) Costa in View of Seo Renders Obvious “Wherein the Second Bias Voltage Is Smaller Than the First Bias Voltage”: The Petition

- On the other hand, Seo focuses on HCI issues and teaches techniques to address these issues during the ***pre-reading (or pre-verification) stage***.
 - Specifically, those techniques involve using the high Vpass ***during pre-reading (or pre-verification)***.

[0089] Subsequently, the pass voltage Vpass may be applied to unselected word lines Unsel WLs. Even when the pass voltage Vpass is applied to the unselected memory string which shares the first source select line SSL0 with the selected memory string, because the source select transistor SST and the drain select transistor DST are turned on, a local boosting phenomenon might not occur in a channel of the pass voltage Vpass of the unselected memory string which shares the first source select line SSL0 with the selected memory string. Accordingly, a disturb phenomenon caused by Hot Carrier Injection (HCI) may be improved.

Paper 1 (Petition), 127-28; Ex. 1003 (Liu Decl.) ¶¶ 89, 306-07.

Ex. 1009 (Seo), [0089]; see also Paper 1 (Petition), 127-28.

- Thus, applying Seo’s high Vpass voltage to Costa results in only a higher Vpass during pre-verification, because Costa teaches to reduce Vpass only during verification to serve a different function.

See also Paper 20 (Reply), 30.

(3) Patent Owner's Argument That the Combination Results in a Constant VPASSL Fails

- PO argues that “applying Costa’s teachings to Seo would—at most—result in a constant VPASSL [sic] on the unprogrammed word lines during T1 and T2.”

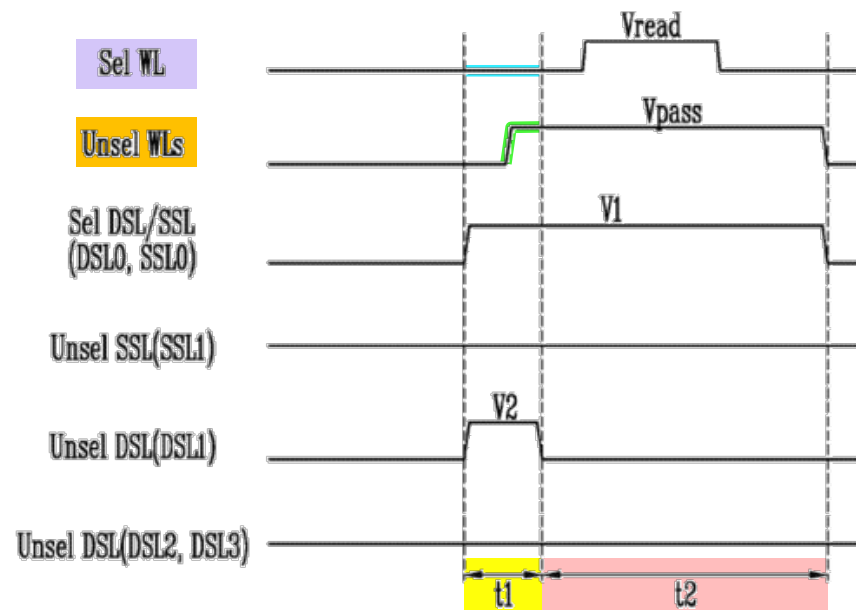
*Paper 22 (Sur-Reply), 22; see also
Paper 17 (Response), 66.*

- This arguments fails for several reasons:
 - It is inconsistent with the teachings of Seo (*supra*);
 - It would have been obvious to employ Seo's teaching of a high Vpass—there are only 2 options; and
 - Applying Costa’s VreadL to Seo’s first time period would have compromised Seo’s goal of reducing HCI (*infra*).

Paper 20 (Reply), 29-31.

Applying Costa's VreadL to Seo's First and Second Time Periods Would Have Compromised Seo's Goal to Reduce HCI

94. As I opined in my original declaration, a POSITA would have found it obvious to lower Seo's V_{pass} only during the verify stage. Ex. 1003 ¶ 308. Seo applies a low voltage to the selected memory cell during the pre-verify stage, thus turning the memory cell off. Ex. 1009, Fig. 8. Thus, there is not a conductive channel across the selected memory cell, and the source terminals of the cells above the selected cell are floating and their voltages increase. Because the threshold voltage is compared against the gate voltage relative to the source voltage, keeping the gate voltage high when the source voltage increases ensures the memory cell transistors would remain above the threshold voltage and turn on as intended, • • • verify period is short. On the other hand, lowering the gate voltage level to below V_{pass} has the risk that the gate voltage relative to the floating source terminal may not be higher than the threshold voltage needed to turn on the unselected memory cells. That would compromise Seo's goal to reduce HCI-induced read disturb on unselected memory strings.



Ex. 1027 (Liu Reply), ¶ 94; Ex. 1009 (Seo), Fig. 8; see also Paper 1 (Petition), 112; 128; Paper 20 (Reply), 30.

Roadmap

- I. The IPR Grounds
- II. The 957 Patent
- III. Ground 1: Hongtao in view of Yu
- IV. Ground 3: Costa in view of Seo
- V. Ground 2: Suzuki

Summary: Patent Owner's Arguments

- For Claim 1, Patent Owner argues that Suzuki does not disclose a “first bias voltage” that is applied in the “pre-verify stage” (or that if so, not in a way that the “second bias voltage” applied during the verify stage is “smaller than the first bias voltage”).
- For Claims 5-6, Patent Owner advances the same “apply a [top/bottom] bias voltage” argument that fails as shown in Ground 1 because it relies on a legally erroneous claim construction (*see supra*).

Paper 17 (Response), 48.

Overview of Suzuki

- Like the 957 patent, Suzuki addresses the issue of hot carrier injection.

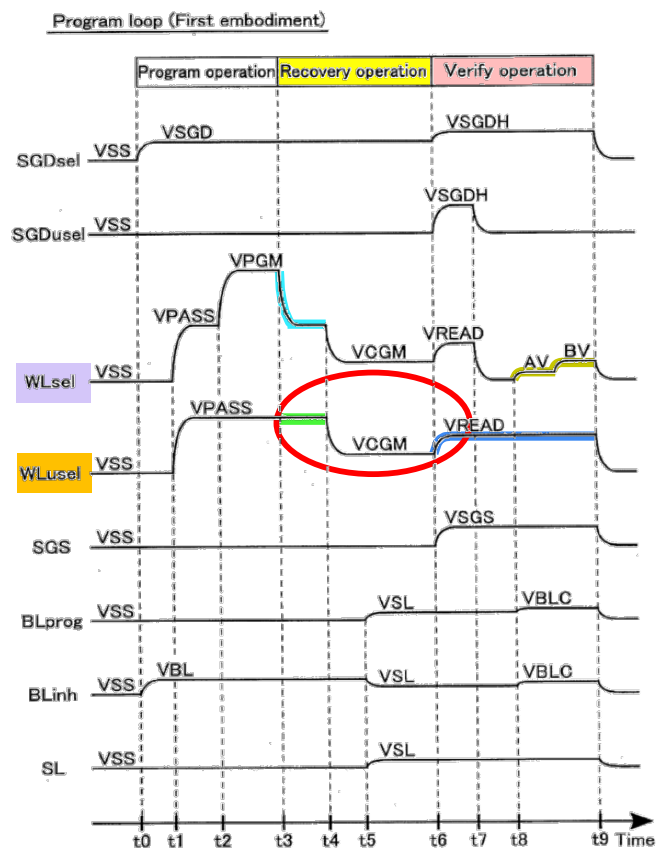
[0148] According to the semiconductor memory device 1 of the first embodiment as described above, it is possible to reduce the occurrence of error bits and enhance the reliability of data written in memory cell transistors MT. In the description below, the details of advantageous effects of the semiconductor memory device 1 according to the first embodiment will be described.

[0153] As countermeasures to the problem, pulling out electrons remaining inside the NAND string NS to the bit line BL side by bringing the select transistor ST1 to the ON state during a recovery operation is considered. On the other hand, when the select transistor ST1 is brought to the ON state during a recovery operation, concentration of electric fields is likely to occur in the select transistor ST1. In this case, the electrons remaining inside the NAND string NS may turn into hot carriers and be injected into the select transistor ST1. Injection of hot carriers to the select transistor ST1 may cause deterioration of the physical properties of the select transistor ST1.

*Ex. 1007 (Suzuki), [0148], [0153];
see also Paper 1 (Petition), 23-24.*

Overview of Suzuki

- Like the 957 patent, Suzuki addresses the issue of hot carrier injection by reducing voltage applied to unselected memory cells.



*Ex. 1007 (Suzuki), Fig. 11;
see also Paper 1 (Petition), 23-24.*

Patent Owner Misconstrues Suzuki's Recovery Operation

- PO argues that “[Suzuki’s] recovery operation includes a period from t3-t4 which is an end operation of the program operation....”, and thus the identified “first bias voltage” is not in the pre-verify stage.

Paper 17 (Response), 51; see also Paper 22 (Sur-Reply), 17.

- This argument fails for at least two reasons:
 1. t3-t6, that is, the Recovery Operation, is the pre-verify, because programming concludes right after t3.
 2. t3-t4 is part of pre-verify, because application of VPASS facilitates accurate sensing during the verify stage.

Paper 20 (Reply), 26-27.

(1) Suzuki's t3-t6 Is the Pre-Verify Stage: Programming Concludes Right After t3

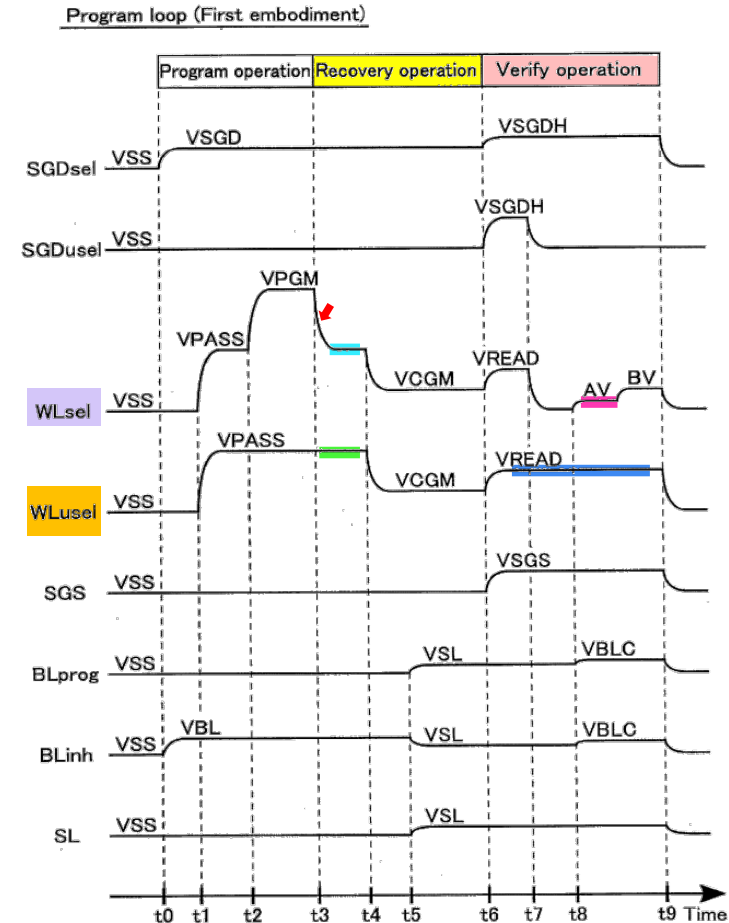
- Program operation ends when WLsel drops from VPGM to VPASS.

Paper 20 (Reply), 26-27.

[0131] As illustrated in FIG. 11, in the program loop, the sequencer 13 executes the processing of t0 to t9 in sequence. For example, a period from time t0 to time t3 corresponds to a program operation, a period from time t3 to time t6 corresponds to a recovery operation, and a period from time t6 to time t9 corresponds to a verify operation. The recovery operation is an operation in which an end operation of the program operation and the ready operation of the verify operation are combined. Hereinafter, each of the program operation, recovery operation, and verify operation will be described in the order mentioned with reference to FIG. 11.

(citing Ex. 1007 ¶ 131). Because Suzuki explains that the recovery operation combines both the end operation of the program operation and the ready operation of the verify operation, we question Patent Owner's assertion that time period t3 to t4 is not part of the ready operation of the verify operation, i.e., the recited "pre-verify stage."

Ex. 1007 (Suzuki), [0131], Fig. 11; Paper 13 (ID), 20; see also Paper 1 (Petition), 80.



(1) Suzuki's t3-t6 Is the Pre-Verify Stage: VPASS on Unselected Memory Cells During t1–t2 Helps Reduce Program Disturb

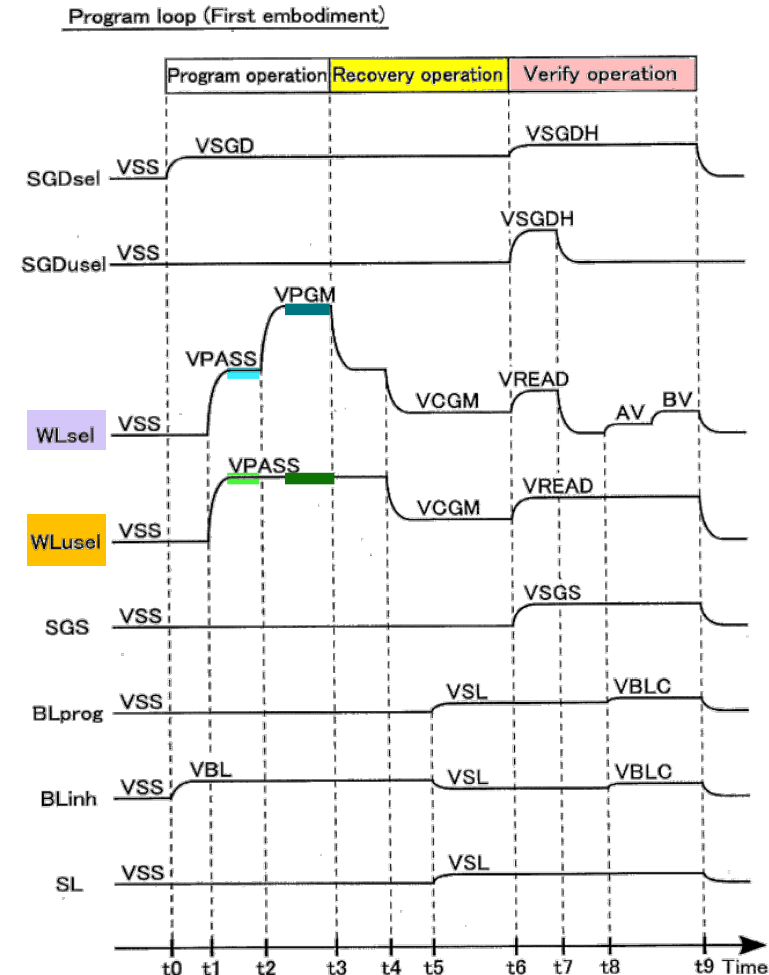
- VPASS in t1-t2 and t3-t4 prepares for the next operation, i.e., a disturb-free program operation and accurate sensing.

*Paper 20 (Reply), 26-27;
Ex. 1027 (Liu Reply), ¶ 82.*

[0134] At time t1, a voltage VPASS is applied to each of the word lines WLsel and WLusel. VPASS is a higher voltage than VSGD and is, for example, 10V. Upon application of the voltage VPASS to each of the word lines WLsel and WLusel, the channel voltage of the NAND string, which is in the floating state, increases (self-boost) due to the coupling between the channel and the control gate. On the

• • •
been injected into the charge storage layer. On the other hand, an increase in threshold voltage of the memory cell transistor MP within other NAND strings NS is suppressed because the difference in voltage between the channel and the control gate has been reduced by the self-boost.

*Ex. 1007 (Suzuki), [0134]-[0135], Fig. 11;
see also Paper 20 (Reply), 26-27.*



(1) Suzuki's t3-t6 Is the Pre-Verify Stage: VPASS on Unselected Memory Cells During t3–t4 Helps Reduce Verify Disturb

- VPASS in t1-t2 and t3-t4 prepares for the next operation, i.e., a disturb-free program operation and accurate sensing.

*Paper 20 (Reply), 26-27;
Ex. 1027 (Liu Reply), ¶ 82.*

[0140] Since the semiconductor memory device 1 according to the first embodiment executes a write operation from the source line SL side, the threshold voltage of a memory cell transistor MT between the program target memory cell transistor MT and the select transistor ST1 is included in the “Er” state. Therefore, the memory cell transistor MT between the program target memory cell transistor MT and the select transistor ST1 is placed in the ON state by having VCGM applied to it. As a result, electrons remaining inside the channel of the NAND string NS coupled to the bit line BLprog are pulled out to the bit lines BL, based on the fact that VSL has been applied to the program target bit line BLprog.

*Ex. 1007 (Suzuki), [0140], Fig. 11;
see also Paper 20 (Reply), 26-27.*

