

Patent Owner's Demonstrative Slides

Micron Technology, Inc. v. Yangtze Memory Technologies Company, Ltd.
Inter Partes Review of
U.S. Patent No. 11,468,957
August 7, 2025

IPR2024-00792
Patent Trial and Appeal Board
United States Patent and Trademark Office

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I. Introductory Section

Table of Abbreviations

Abbreviation	Description
'957	U.S. Pat. No. 11,468,957
'957FH	File History of U.S. Pat. No. 11,468,957
Challenged Claims	'957, Claims 1-6
Liu	Declaration of Dr. Liu (Ex. 1003)
Liull	Reply Declaration of Dr. Liu (Ex. 1027)
Hongtao	Chinese Pat. App. Pub. No. 109065091 (Ex. 1005)
Yu	U.S. 2019/0198117 (Ex. 1006)
Suzuki	U.S. 2021/0082505 (Ex. 1007)
Costa	U.S. 2018/0012667 (Ex. 1008)
Seo	U.S. 2021/0027848 (Ex. 1009)
Li	U.S. 2024/0295960 (Ex. 2004)
Dong	U.S. 2023/0343398 (Ex. 2005)
Liu822 Tr.	Transcript of December 17, 2024 Deposition of Dr. Liu for IPR2024-00795 in Connection with Patent U.S. 11,501,822 (Ex. 2006)
Liu957 Tr.	Transcript of May 28, 2025 Deposition of Dr. Liu for IPR2024-00792 in Connection with Patent U.S. 11,468,957 (Ex. 2011)
Yang	U.S. 10,726,920 (Ex. 2007)
Office	U.S. Patent and Trademark Office
Petition or Pet.	Petition for <i>Inter Partes</i> Review of U.S. Patent No. 11,468,957 (IPR2024-00792, Paper 1)
Parallel district court litigation	<i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc.</i> , NDCA-3-23-cv-05792 (N.D. Cal.)
Patent Owner, PO	Yangtze Memory Technologies Co. Ltd.
Petitioner	Micron Technology, Inc.
POSITA	Person of ordinary skill in the art
Przybylski	Declaration of Steven Przybylski
Reply	Petitioner's Reply Brief (IPR2024-00792, Paper 20)
POSR	Patent Owner's Sur-reply (Pap. 22)

All citations within quotations omitted herein, and emphasis added unless otherwise indicated

'957, Claim 1

- Claim 1 of the '957 recites:

[1.pre] 1. An apparatus for reading a memory device including a first memory cell string and a second memory cell string, the first memory cell string including a bottom-select-gate (BSG) transistor, memory cells, and a top-select-gate (TSG) transistor that are connected in series, the second memory cells string including a BSG transistor, memory cells, and a TSG transistor that are connected in series, the apparatus comprising: processing circuitry configured to:

[1.a] apply, in a pre-verify stage, a first verify voltage on a gate terminal of a selected memory cell of the first memory cell string, the selected memory cell being programmed and arranged between a first adjacent memory cell and a second adjacent memory cell;

[1.b] apply, in the pre-verify stage, a first bias voltage on a gate terminal of at least one memory cell of the first memory cell string that is not programmed;

[1.c] apply, in a verify stage, a second verify voltage on the gate terminal of the selected memory cell of the first memory cell string; and

[1.d] apply, in the verify stage, a second bias voltage on the gate terminal of the at least one memory cell of the first memory cell string that is not programmed, wherein the second bias voltage is smaller than the first bias voltage.

'957 Claims 2-3

- Claim 2 of the '957 recites:

2. The apparatus of claim 1, wherein the at least one memory cell of the first memory cell string that receives the first bias voltage and the second bias voltage is positioned between the first adjacent memory cell of the selected memory cell and the TSG transistor of the first memory cell string.

- Claim 3 of the '957 recites:

3. The apparatus of claim 1, wherein the at least one memory cell of the first memory cell string that receives the first bias voltage and the second bias voltage is positioned between the second adjacent memory cell of the selected memory cell and the BSG transistor of the first memory cell string.

'957 Claims 5-6

- Claim 5 of the '957 recites:

[5.pre] 5. The apparatus of claim 2, wherein the processing circuitry is further configured to:

[5.a] apply a bottom bias voltage on a gate terminal of the BSG transistor of the first memory cell string in the pre-verify stage and the verify stage;

[5.b] apply a top bias voltage on a gate terminal of the TSG transistor of the first memory cell string in the pre-verify stage and the verify stage; and

[5.c] apply a positive voltage on gate terminals of any memory cells that are positioned between the second adjacent memory cell of the selected memory cell and the BSG transistor of the first memory cell string in the pre-verify stage and the verify stage.

- Claim 6 of the '957 recites:

[6.pre] 6. The apparatus of claim 3, wherein the processing circuitry is further configured to:

[6.a] apply a bottom bias voltage on a gate terminal of the BSG transistor of the first memory cell string in the pre-verify stage and the verify stage;

[6.b] apply a top bias voltage on a gate terminal of the TSG transistor of the first memory cell string in the pre-verify stage and the verify stage; and

[6.c] apply a positive voltage on gate terminals of any memory cells that are positioned between the second adjacent memory cell of the selected memory cell and the TSG transistor of the first memory cell string in the pre-verify stage and the verify stage.

Grounds

Claims	Ground
'957, claims 1-6	Hongtao in view of Yu Obviousness
	Suzuki Anticipation
	Costa in view of Seo Obviousness

Pet. at 8.

Disputed Issues

Issue	Slides
<u>Pre-Verify Stage Limitations (all Challenged Claims)</u> • Ground 1 (Hongtao in view of Yu): Hongtao in View of Yu Fails to Render Obvious a “Pre-Verify Stage” • Ground 3 (Costa in view of Seo): Costa in View of Seo Fails to Render Obvious a “Pre-Verify Stage”	Slides 9-17
<u>First and Second Bias Voltages Limitations (all Challenged Claims)</u> • Ground 1 (Hongtao in view of Yu): Hongtao in View of Yu Fails to Render Obvious Applying “a First Bias Voltage” and “a Second Bias Voltage” on the Gate Terminal of a Not Programmed Memory Cell “Wherein the Second Bias Voltage Is Smaller than the First Bias Voltage” • Ground 2 (Suzuki): Suzuki Fails to Disclose Applying “a First Bias Voltage” and “a Second Bias Voltage” on the Gate Terminal of a Not Programmed Memory Cell “Wherein the Second Bias Voltage Is Smaller than the First Bias Voltage” • Ground 3 (Costa in view of Seo): Costa in View of Seo Fails to Render Obvious Applying “a First Bias Voltage” and “a Second Bias Voltage” on the Gate Terminal of a Not Programmed Memory Cell “Wherein the Second Bias Voltage Is Smaller than the First Bias Voltage”	Slides 18-35
<u>Top and Bottom Bias Voltages Limitations (Claims 5-6)</u> • Claim Construction • Ground 1 (Hongtao in view of Yu): Hongtao in View of Yu Fails to Render Obvious a “Top Bias Voltage” or “Bottom Bias Voltage” Applied “In the Pre-Verify Stage and the Verify Stage” • Ground 2 (Suzuki): Suzuki Fails to Disclose a “Top Bias Voltage” or “Bottom Bias Voltage” Applied “In the Pre-Verify Stage and the Verify Stage”	Slides 36-45

II. Pre-Verify Stage Limitations

Limitations [1.a]-[1.b] Require the Application of Voltages in a “Pre-Verify Stage”

[1.a] apply, in a **pre-verify stage**, a first verify voltage on a gate terminal of a selected memory cell of the first memory cell string, the selected memory cell being programmed and arranged between a first adjacent memory cell and a second adjacent memory cell;

[1.b] apply, in the **pre-verify stage**, a first bias voltage on a gate terminal of at least one memory cell of the first memory cell string that is not programmed;

Ground 1: Hongtao and Yu Fail to Disclose a Pre-Verify Stage

Petitioner argues: “[*Hongtao’s*] pre-conduction phase precedes the read/verify phase. [Hongtao], claim 1, [0022]. While not limiting, like the first verify voltage of embodiments of the ’957 patent, the pre-conduction voltage turns on the channel. Ex. 1001, 11:12-15; Hongtao, [0023]. Thus, this **“pre-conduction voltage” constitutes a first verify voltage on ... a selected memory cell, appl[ied] in a pre-verify (pre-conduction) stage**. Liu, ¶¶ 100-105.”

Pet. 32.

- But Hongtao is explicitly directed to a “reading method” for 3D NAND:

Hongtao: “*The invention relates to a **reading method** of 3D NAND flash memory.*”

Hongtao, Abstract; POR 29; Przybylski, ¶78.

- While Hongtao references a pre-conduction phase and reading phase, *Hongtao does not teach or suggest applying those teachings to create a verification operation with distinct “pre-verify” and “verify” stages*

Hongtao: “*The reading method includes a pre-conduction phase and a reading phase step in sequence, wherein, in the pre-conduction phase, a continuous precharge voltage is applied to the bit line; at the same time, the top select transistor of the selected string and the top select transistor of the unselected string are turned on, and the bottom select transistor of the selected string and the bottom select transistor of the unselected string are turned off.*”

Hongtao, [0005]-[0007]; POR 29; Przybylski, ¶78; POSR 7.

- Yu also fails to disclose a verification operation with a “pre-verify stage” and a “verify stage,” and Petitioner does not contend otherwise

POR 29-30; Pet. 30-36; Yu, [0049]-[0054]; Przybylski, ¶79; POSR 7.

Ground 1: Hongtao in View of Yu Fails to Render Obvious Pre-Verify Stage

Petitioner argues: “A POSITA would have been motivated, with a reasonable expectation of success, to employ Hongtao’s read operations in a program-verification loop in view of Yu and the knowledge of a POSITA for several reason.”

Pet. 72-74.

- But Petitioner conflates “*verifying*” and “*reading*,” which *are distinct operations*, each having their own concerns and using distinct voltages and biasing schemes
 - Verification is an iterative check within a programming cycle that follows each programming step, while reading operations check the stored state of a cell
 - In a verify operation, memory cells are known to be unprogrammed beforehand

POR 30-32; POSR 9-10; Ex. 1021, [0103]; Ex. 1020, 16:16-21; Ex. 1019, 17:10-14; Ex. 1017, 3:21-29; Przybylski, ¶¶81-82.

Ground 1: Hongtao in View of Yu Fails to Render Obvious Pre-Verify Stage

Petitioner argues: “A POSITA would have been motivated, with a reasonable expectation of success, to employ Hongtao’s read operations in a program-verification loop in view of Yu and the knowledge of a POSITA for several reason.”

Pet. 72-74.

- As another example difference between reading and verifying, verification operations use distinct bias voltages for unselected word lines on programmed and unprogrammed memory as part of a programming loop, whereas reading operations use the same voltage for all unselected word lines
 - For its programming loop (which includes verification), Yu teaches using a *different voltage for the unprogrammed memory*:

Yu: “During the program interval T3~T4, **a second pass voltage VPASS2 lower than the first pass voltage VPASS1 may be applied to** an unselected word line of the second sub block SB2. According to the first program scenario, all of the **memory cells** of the second sub block SB2 are **in the erased state E0**.”

Yu, [0121]-[0122], Figs. 11-12; POSR 7-8; see also POR 30-32; Przybylski, ¶¶79-80.

- Hongtao is concerned with reading operations, which involve applying *the same voltage to all unselected word lines*

Hongtao: “The top select transistor and the bottom select transistor of the selected string are applied with a conduction voltage, so that the channel of the selected string is connected to the bit line, and the channel potential of the selected string is equal to the driving voltage on the bit line. The gates of **the unselected memory cells on the selected string are applied with a conduction voltage through the unselected word lines**. Therefore, the unselected memory cells on the selected string will withstand read interference caused by ‘conduction voltage - driving voltage’.”

Hongtao, Fig. 2, [0025]; POSR 7-8; see also POR 19, 30-32; Przybylski, ¶¶79-80.

Ground 1: Hongtao in View of Yu Fails to Render Obvious Pre-Verify Stage

- Reading and verifying are used at different times for different purposes:

Dr. Przybylski: “Further differences between reading and verifying also arise from the fact that **verification operations are used as an iterative check within a programming cycle after every programming operation** (e.g., by repeatedly performing programming operations and verifying operations until each memory cell within the programming order is programmed correctly), while **reading operations are independent processes that are instead used to check the stored state of a cell.**”

Przybylski, ¶82; POR 30-31.

- These differences are what allow different voltages for the unprogrammed memory to be used during a verify operation (like in Yu), but not a reading operation (like in Hongtao)

Dr. Przybylski: “These differences may be particularly pronounced when using a fixed programming order, such as in Yu. See Yu [0115]. For example, when performed on memory cells that are being programmed in a fixed order, **all of the memory cells above (or below) the selected memory cell that is being verified are known to be unprogrammed. This allows a lower bias voltage to be used on the gates of the unprogrammed memory cells** while still ensuring that the memory cells are turned on.”

Przybylski, ¶82; POR 30-31; Yu, [0115]; '957, 12:28-13:4, Fig. 6; Costa [0122].

- Petitioner and Dr. Liu do not account for these distinctions between verify operations and reading operations, and have presented no arguments or evidence—beyond the conclusory statement that the functions are somehow identical

POR 30-31; Przybylski, ¶¶81-83; POSR 8-9.

Ground 1: Hongtao in View of Yu Fails to Render Obvious Pre-Verify Stage

Petitioner argues on Reply: “*PO’s argument that verify operations can use lower bias voltages on unprogrammed cell is irrelevant.* POR, 31. As PO concedes, this is an optional ‘capab[ility].’ Id. *Suzuki’s verify operation, for example, does not involve this capability.* Ex. 1007, Fig. 11 (showing WLuse1 for all unselected gates). Further, *the claims do not require applying a voltage on the unprogrammed cells* lower than that on the programmed cells during either the pre-verify or verify stage.”

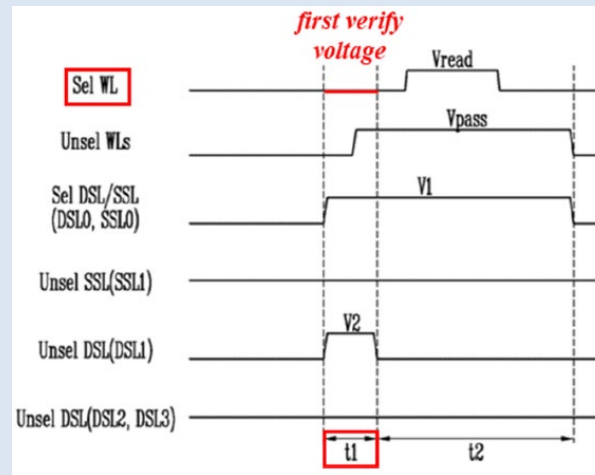
Reply 25.

- But Petitioner has failed to show that a POSITA would have been motivated to apply Hongtao’s teachings regarding *reading operations* to the *verification operations* within Yu’s programming loop
- The capability of using lower bias voltages on unprogrammed memory cells in a verify operation is merely an illustration of key differences of verify operations that Petitioner ignores (slides 12-14)
- How Suzuki operates (i.e., whether it uses lower bias voltages on unprogrammed cells) is irrelevant to these distinctions
- Whether the ’957 claims require applying a voltage on unprogrammed is irrelevant to these distinctions

POR 30-31; POSR 9-10.

Ground 3: Costa in View of Seo Fails to Render Obvious a Pre-Verify Stage

Petitioner argues: “*Seo discloses apply[ing], in a pre-verify stage (a first time period t_1 preceding a read/verify period t_2), a first verify voltage (a low voltage) on ... a selected memory cell....* In the context of the '957 patent, even applying zero volts is applying a voltage, which is bias voltage or verify voltage.”



Pet. 106-107.

- But Seo does not disclose or render obvious verification operations at all, and is instead concerned with a memory device “read” operation that is divided into a “first time period t_1 ” and a “second time period t_2 ”

POR 59-61; Przybylski, ¶148; Seo [0011].

- Costa does not disclose or render obvious a verify operation that includes a distinct “pre-verify stage” and “verify stage”

POR 59-60; Przybylski, ¶148.

Ground 3: Costa in View of Seo Fails to Render Obvious Pre-Verify Stage

- Petitioner’s proposed combination fails to show that a POSITA would have been motivated to combine Costa and Seo’s teachings to render obvious a verify operation that includes a distinct “pre-verify stage”
- Even assuming that a POSITA would have been motivated to employ Seo’s teachings when performing a verification operation, it does not follow that the time period t1 in Seo would be converted to a “pre-verify stage”

POR 60-61; Przybylski, ¶149; see also DI, 26-27 (citing Seo [0087]-[0090], Fig. 7); POR 60-61; Przybylski, ¶¶147-149; POSR 20-21.

Petitioner argues on Reply: “With the correct understanding that *read and verify operations are virtually identical*, the correspondence between Seo’s two time periods to the claimed preverify and verify stages would have been obvious.”

Reply 28-29.

- However, reading operations and verifying operations are distinct (slides 12-14)

POR 60-61; Przybylski, ¶¶147-149; POSR 20-21.

III. First and Second Bias Voltages Limitations

Limitations [1.b] and [1.d] Require the Application of a “First Bias Voltage” and a “Second Bias Voltage” Wherein the Second Bias Voltage Is Smaller Than the First Bias Voltage

[1.b] apply, in the pre-verify stage, a **first bias voltage** on a gate terminal of at least one memory cell of the first memory cell string that is not programmed;

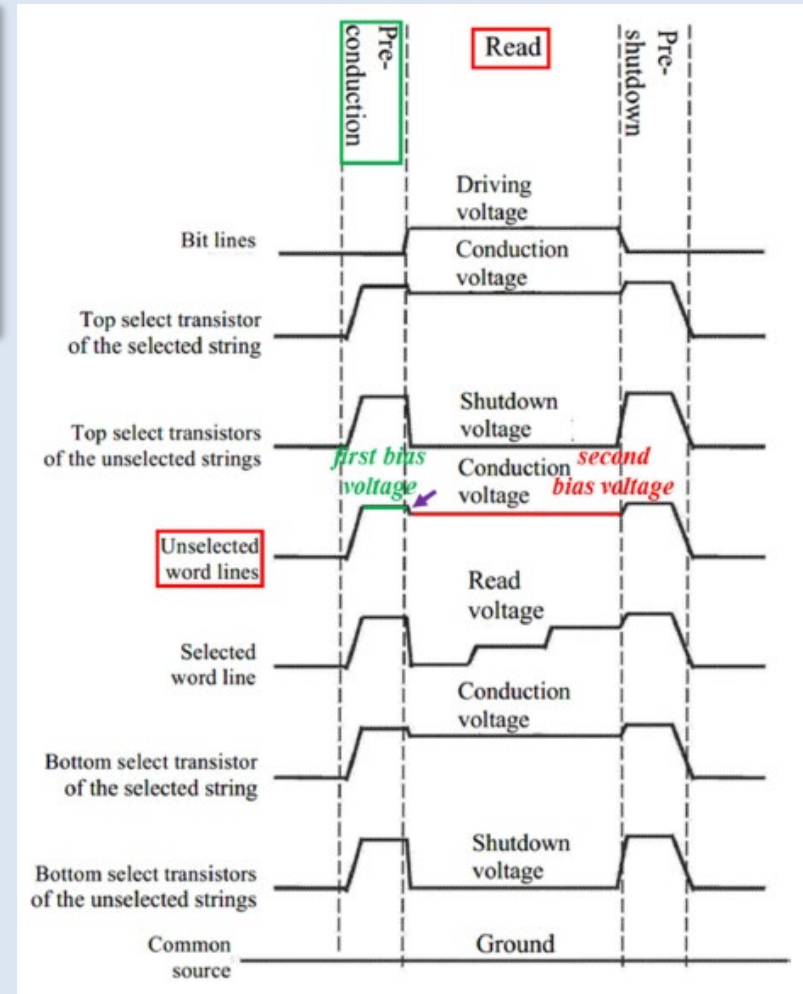
[1.d] apply, in the verify stage, a **second bias voltage** on the gate terminal of the at least one memory cell of the first memory cell string that is not programmed, wherein **the second bias voltage is smaller than the first bias voltage**.

Ground 1: Hongtao in View of Yu Fails to Render Obvious First and Second Bias Voltages Wherein the Second Bias Voltage Is Smaller Than the First Bias Voltage

Petitioner argues: “Hongtao further discloses applying a second bias voltage (a conduction voltage) on the same cell through the same unselected word lines in the verify stage (the read phase).... Hongtao, Fig. 2; see also *id.*, [0019], [0025]. **As indicated by the purple arrow, the voltage signal applied to the unselected word lines ramps down from the pre-conduction voltage to reach the conduction voltage. Thus, the second bias voltage is smaller than the first bias voltage.**”

Pet. 39-40 (citing Hongtao, Fig. 2).

- But Figure 2 of Hongtao depicts *target voltages* applied to word lines, *not the resulting voltages applied on gate terminals of the memory cells*:



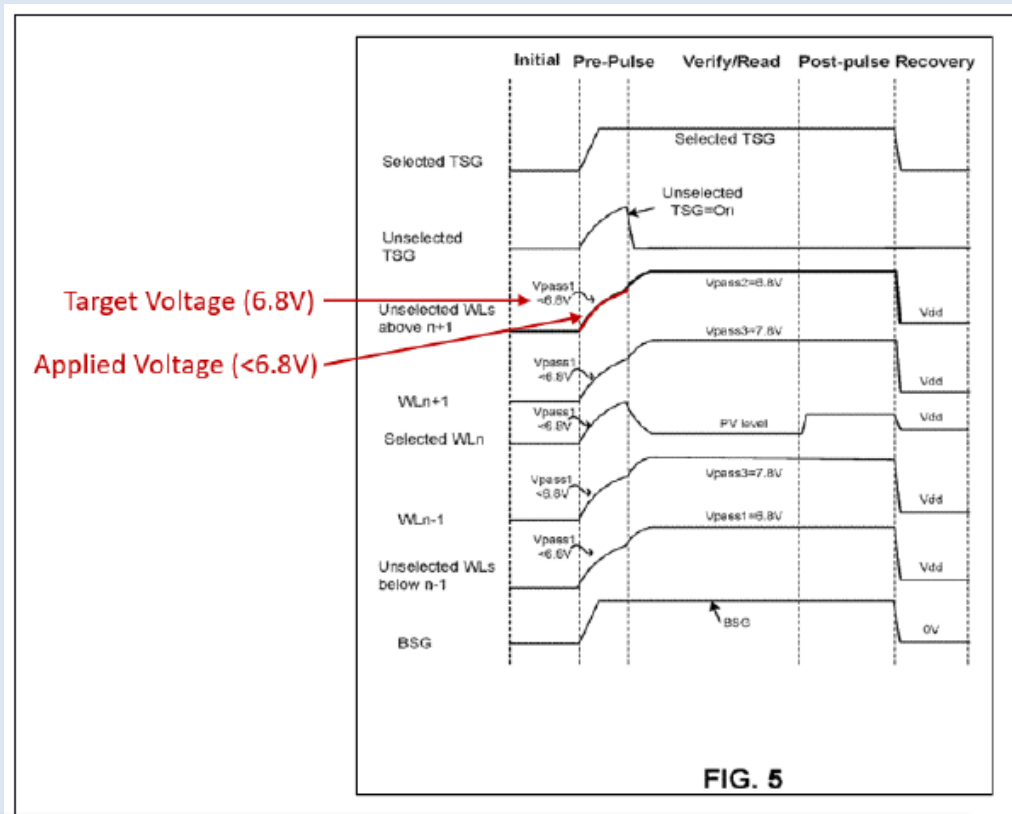
See, e.g., Hongtao, Fig. 2 (annotated by Petitioner); POR 32-44.

Ground 1: Hongtao in View of Yu Fails to Render Obvious First and Second Bias Voltages Wherein the Second Bias Voltage Is Smaller Than the First Bias Voltage

- The '957 patent distinguishes between the voltages that are applied through word line layers during a pre-pulse stage, and the bias voltages applied on the gate terminals of the memory cells that develop over time as a result

POR 33-34; '957, 11:68-12:9, 12:10-27, 12:18-19; Przybylski, ¶¶90.

- Figure 5 of the '957 patent illustrates the distinction



'957 Patent: "Compared to the verify/read operation in FIG. 5, the bias voltages applied in the pre-pulse stage can be **fully developed to (or completely reach) target** values in FIG. 7" such that "the bias voltage ... can be fully developed in the pre-pulse stage."

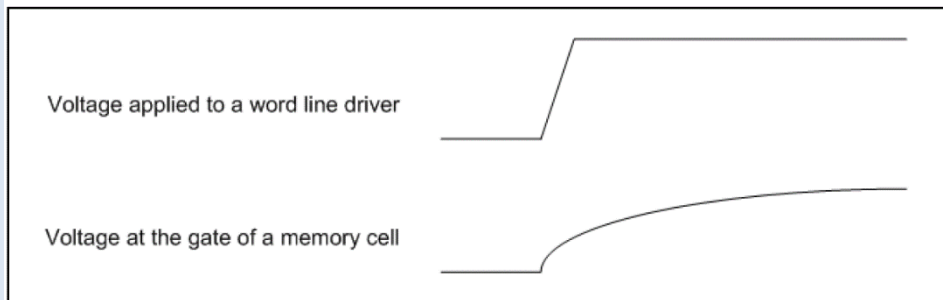
'957, 11:48-12:9, 12:15-21, 12:28-42, 13:13-17; POR 5-10, 35-38; Przybylski, ¶¶92-95; POSR 13-14.

Dr. Przybylski: "[A]s shown in Figure 5 of the '957 Patent, **when a short pre-pulse time is used the bias voltages that are applied may not have sufficient time to develop fully, resulting in the bias voltages being "less than a target value**, such as 6.8 volts" during the initial pre-pulse period."

Ground 1: Hongtao in View of Yu Fails to Render Obvious First and Second Bias Voltages Wherein the Second Bias Voltage Is Smaller Than the First Bias Voltage

- In a 3D NAND device, such as the one described by Hongtao or the '957, word lines have an RC time-constant from capacitances arising from the stacked structure, such that the actual voltages that develop on the gate terminals of the memory cells will typically appear as curved lines:

Dr. Przybylski: "Word line drivers, or analogous voltage generation circuits, operate as voltage sources that charge up the word lines and force them to reach specific target voltages over time. As a result, **the 'target' voltages being applied to the word lines may differ from the resulting voltages that are applied on the gate terminals of the memory cells**, which will appear distorted due to the RC time constants involved. For example, I prepared the figure below to help illustrate this phenomenon. ... As shown below, when a voltage is applied to a given word line, **the resulting voltages applied on the gate terminals of the memory cells will appear as curved lines that charge-up over time based on the RC time-constants associated with a given word line layer.**"



Przybylski, ¶¶94; POR 33-38; POSR 11-13.

- Dr. Liu admitted that actual voltages (as opposed to target voltages) will be distorted and curved:

Dr. Liu: "[I]n the real world **there is always going to be parasitic component...** so therefore **it's always going to be having some sort of ramping time.**

Ex. 2006, 63:22-64:22; POR 35-38; Przybylski, ¶¶92-95; POSR 13.

Ground 1: Hongtao in View of Yu Fails to Render Obvious First and Second Bias Voltages Wherein the Second Bias Voltage Is Smaller Than the First Bias Voltage

- Hongtao’s text does not describe applying a “second bias voltage” that is smaller than a “first bias voltage” to the gate terminal of an unprogrammed memory cell
- Hongtao does not contemplate that voltages need time to develop, and Figure 2 of Hongtao alone is insufficient to determine the actual voltages that develop on the gate terminals of memory cells

POR 38-39; Przybylski, ¶196.

Federal Circuit: “Our precedent has held that *drawings can be used as prior art*, without referring to the surrounding description, ***only if the prior art features are clearly disclosed by the drawing.***”

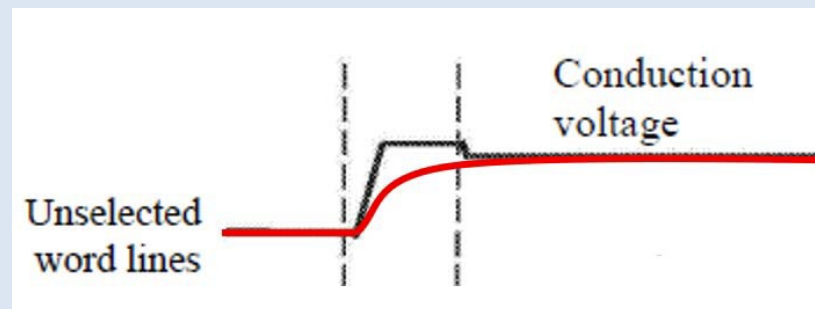
PlaSmart, Inc. v. Kappos, 482 F. App’x 568, 572 (Fed. Cir. 2012); POR 38-39.

MPEP: “[D]rawings must be evaluated for what they reasonably disclose and suggest to one of ordinary skill in the art.”

MPEP 2125; POR 38-39; Przybylski, ¶196.

Ground 1: Hongtao in View of Yu Fails to Render Obvious First and Second Bias Voltages Wherein the Second Bias Voltage Is Smaller Than the First Bias Voltage

- The waveform illustrated in Fig. 2 of Hongtao (**black lines**) is a technique to minimize the pre-conduction time by applying a *target voltage* to the word lines that is somewhat elevated at the start
- This causes voltages being *applied* to ramp up faster, but voltages of the type illustrated in Hongtao would be expected to result in bias voltages that are smoothed-out and appear as follows (**red line**):



POR 39-40; Przybylski, ¶¶97-99.

Ground 1: Hongtao in View of Yu Fails to Render Obvious First and Second Bias Voltages Wherein the Second Bias Voltage Is Smaller Than the First Bias Voltage

Petitioner argues in Reply: “Neither the '957 patent nor the prior art distinguishes word lines from gates. ... The '957 patent uses “gate” and “word line” interchangeably. ... [T]he '957 patent repeatedly describes memory-cell operations based on word-line voltages, impliedly equating word-line voltages with gate voltages. ... [T]he prior art equates the two terms.”

Reply, 9-16.

- But the deficiency in Hongtao is not that it is describing “word line voltages,” but that *Figure 2 depicts target values* (i.e., the piecewise linear function used to control a voltage generation circuit) *rather than the resulting voltage that is “appl[ied]” on the gate terminals of the memory cells* (slides 20-24)

POSR 11-13; POR 33-34; Przybylski ¶¶90; '957, 12:18-19.

Petitioner argues in Reply: “Thus, a POSITA would understand that the curves of Figure 5 illustrate this insufficient voltage development, rather than distinguishing gate voltages (curved) from word-line voltages (linear) as PO argues.”

Reply, 17-20.

- But this again misses the point, which is the distinction between idealized “*target*” voltages illustrated with straight lines and the *actual voltages that develop over time on the gate terminals as illustrated with curved lines*

'957 Patent: “Compared to the verify/read operation in FIG. 5, *the bias voltages applied in the pre-pulse stage can be full developed to (or completely reach) target values in FIG. 7*” such that “the bias voltage ... can be fully developed in the pre-pulse stage.”

'957, 11:48-12:9, 12:15-21, 12:28-42, 13:13-17; POSR 13-14; POR 5-10; POR 35-38; Przybylski, ¶¶92-95.

Ground 1: Hongtao in View of Yu Fails to Render Obvious First and Second Bias Voltages Wherein the Second Bias Voltage Is Smaller Than the First Bias Voltage

Petitioner argues in Reply: “PO argues that significant RC delays exist across a word-line layer in 3D NAND devices such that a word-line voltage and its corresponding gate voltage are different. ... **PO is mistaken about the dominant source of RC delays. ... [T]he word-line layers have negligible resistances.**”

Reply, 20-23.

- But the '957 patent distinguishes between target and actual voltages, and Dr. Liu agreed that there will always be a ramp time (slides 21-22)
- And *the Petition never addressed what the actual voltage experienced at the gate would be in Hongtao*
- Petitioner admits that the voltage might “overshoot,” “undershoot,” or “reach” the target (Reply, 22-23), and failed to show which of these happens in Hongtao

POSR 14-15.

POSR 14-15.

Ground 1: Hongtao in View of Yu Fails to Render Obvious First and Second Bias Voltages Wherein the Second Bias Voltage Is Smaller Than the First Bias Voltage

Petitioner argues in Reply: “PO’s argument that Hongtao’s paragraph [0026] does not explain why Hongtao lowers the bias voltage during the read phase also fails. POR, 41–43. **Paragraph [0026] states a general principle affecting read interference, namely, the greater the interference-inducing voltage, the greater the interference.** A POSITA would have understood that reducing conduction voltage reduces “conduction voltage - driving voltage,” the interference-inducing voltage. **Hongtao’s Figure 2 shows exactly that.**”

Reply, 8.

- But Hongtao [0026] instead describes *problems* in the embodiment of Fig. 2, which are addressed in the further embodiment of Fig. 3

Hongtao: “[I]n this specific embodiment, the read interference caused by the “**conduction voltage – driving voltage**” suffered by the unselected memory cells on the selected string is smaller than the read interference suffered by the memory cells on the unselected string. In order to improve the accuracy of memory reading, it is necessary to further reduce the read interference suffered by the memory cells on the unselected string. **In order to further reduce the read interference** suffered by the memory cells with conduction voltage on the unselected strings, **the inventors of the present invention propose another reading method of 3D NAND flash memory. Please refer to Figure 3**, which is a timing diagram of reading a 3D NAND memory cell using another reading method in another specific embodiment of the present invention.”

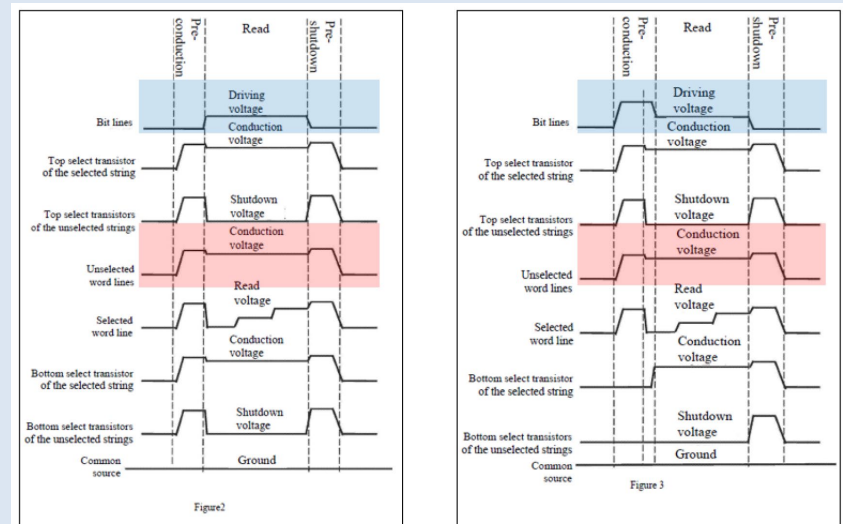
Hongtao, [0026]-[0028]; POSR 15-16; POR 39-43; Przybylski, ¶¶97-103.

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Reply, 8.

- But Hongtao [0026] instead describes *problems* in the embodiment of Fig. 2, which are addressed in the further embodiment of Fig. 3
- Both Figs. 2 and 3 depict **the exact same conduction voltage waveform depicting the same target voltage** rather than resulting voltage, and therefore both embodiments fail to disclose the claimed voltage relationship
- Instead, Hongtao addresses the problem of Fig. 2 by **applying a pre-conduction voltage to the bit lines**
- Also, reducing “conduction voltage – driving voltage” *says nothing about the relative magnitude of the voltages applied to the unselected word lines during different time periods*



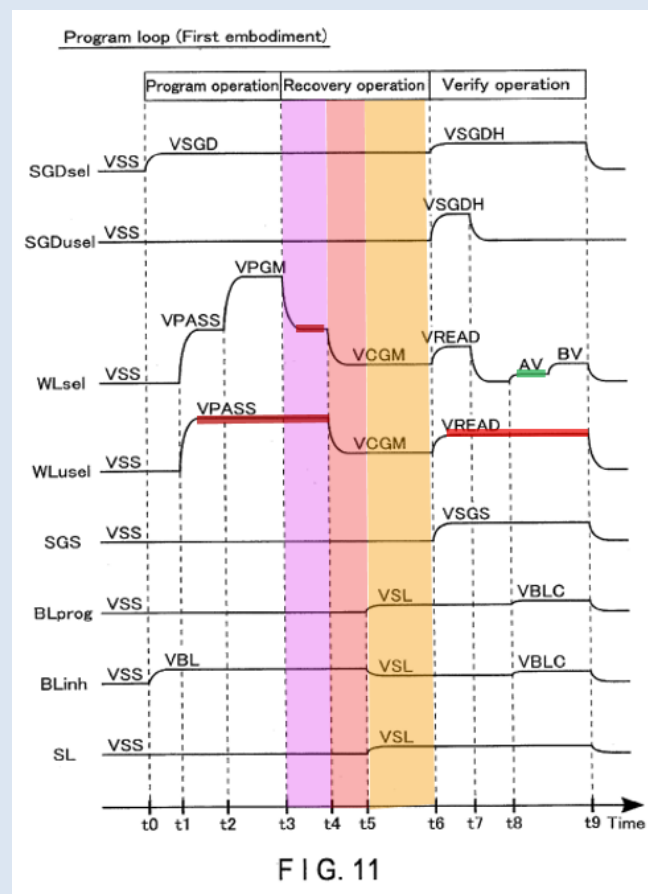
POSR 15-16; POR 39-43; Przybylski, ¶¶97-103.

Ground 2: Suzuki Fails to Disclose First and Second Bias Voltages Wherein the Second Bias Voltage Is Smaller Than the First Bias Voltage

Petitioner argues: “Suzuki discloses applying a second bias voltage (VREAD) through the same unselected word lines to the at least one memory cell in the verify stage. Suzuki, Fig. 11; see also id., [0142]. VREAD may be 8V. Id. VPASS may be 10V. Id., [0134]. **Thus, the second bias voltage (VREAD) is smaller than the first bias voltage (VPASS).** Liu, ¶ 210.”

Pet. 84 (citing Suzuki, Fig. 11).

- But VPASS is not applied during a “pre-verify stage”—instead, VPASS is applied during **t3-t4**, which is an **end operation during a final stage of the program operation**, and distinct from the period from **t5-t6** with distinct voltages that act as a **ready operation, which is part of the verify operation**, and a period from **t4-t5**, which is a **transition period** between the two



Ground 2: Suzuki Fails to Disclose First and Second Bias Voltages Wherein the Second Bias Voltage Is Smaller Than the First Bias Voltage

Petitioner argues in Reply: “PO incorrectly contends that the beginning of Suzuki’s recovery phase cannot be part of “pre-verify stage,” and hence Suzuki does not disclose the first bias voltage. POR, 50–54. To start, there can be no reasonable debate that **programming terminates after the WLsel voltage decreases below VPGM (the very beginning of t3).**”

Reply 26.

- But this ignores Suzuki’s explicit statement that the period t3-t4 is an “end operation of the program operation” in which the voltages begin to ramp down

Suzuki: “As illustrated in FIG. 11, in the program loop, the sequencer 13 executes the processing of t0 to t9 in sequence. For example, a period from time t0 to time t3 corresponds to a program operation, **a period from time t3 to time t6 corresponds to a recovery operation**, and a period from time t6 to time t9 corresponds to a verify operation. **The recovery operation is an operation in which an end operation of the program operation and the ready operation of the verify operation are combined.** Hereinafter, each of the program operation, recovery operation, and verify operation will be described in the order mentioned with reference to FIG. 11.”

Suzuki, [0131]; POR 51-55; Przybylski, ¶125-132; POSR 18-19.

Ground 2: Suzuki Fails to Disclose First and Second Bias Voltages Wherein the Second Bias Voltage Is Smaller Than the First Bias Voltage

Petitioner argues in Reply: “Next, *applying VPASS on unselected memory cells during t3–t4 self-boosts the channel voltage to prepare for a voltage transition*, 5 avoiding a disturb phenomenon, and is therefore part of the process that “pull[s] out” the electrons for more accurate sensing. Ex. 1007, [0134]–[0135], [0140]. In short, *the recovery operation in t3–t6 effectuates the removal of the electrons* for a more accurate, and thus prepares for, the verify step. Thus, recovery is “pre-verify.””

Reply 27 (citing Suzuki, [0134]–[0135], [0140]).

- While Suzuki [0134]–[0135] describes applying VPASS to “self-boost,” this boost operation is described only in the discussion of the time periods from t1–t3 (indisputably the programming stage)

Suzuki: “**At time t1**, a voltage VPASS is applied to each of the word lines WLsel and WLusel. VPASS is a higher voltage than VSGD and is, for example, 10V. Upon application of the voltage VPASS to each of the word lines WLsel and WLusel, the channel voltage of the NAND string, which is in the floating state, increases (**self-boost**) due to the coupling between the channel and the control gate.”

Suzuki: “**At time t2**, a program voltage VPGM is applied to a word line WLsel. The program voltage VPGM is, for example, 20V. ... On the other hand, an increase in threshold voltage of the memory cell transistor MP within other NAND strings NS is suppressed because the difference in voltage between the channel and the control gate has been reduced by the **self-boost**.”

Suzuki, [0134]–[0135]; POSR 19.

- If anything, this further confirms that t3–t4 is part of the programming operation, not a pre-verify operation, because VPASS is still applied
- And while Suzuki [0140] describes a process that causes electrons to be “pulled out to the bit lines,” this is during the period t5–t6, which is a ready operation but does not have a voltage that satisfies the Claims

POSR 19; Suzuki, Fig. 11.

Suzuki: “**At time t5**, a voltage VSL is applied to each of the bit lines BLprog and BLinh and the source line SL. ... As a result, **electrons remaining inside the channel of the NAND string NS coupled to the bit line BLprog are pulled out to the bit lines BL**, based on the fact that VSL has been applied to the program target bit line BLprog.”

Suzuki, [0139]–[0140], Fig. 11; POSR 19.

Ground 3: Costa in View of Seo Fails to Render Obvious First and Second Bias Voltages Wherein the Second Bias Voltage Is Smaller Than the First Bias Voltage

Petitioner argues: “A POSITA would have found it obvious that Seo’s first bias voltage is no lower than the standard read pass voltage because the same voltage level is applied to all unselected memory cells, including those already programmed, to ensure that they all conduct regardless of the program state. ... And as §XI.G further explains, **during verify, Costa seeks to reduce channel resistance issues without introducing read disturb due to an unnecessarily high read pass voltage on the unprogrammed cells**, in which case low V_{pass} voltages are optimal for unselected gates (e.g., gates of unprogrammed cells). **Thus, a POSITA would not have lowered Seo’s standard read pass voltage during pre-verify. Therefore, the second bias voltage (V_{readL}) is smaller than the first bias voltage (pass voltage V_{pass}).**” Pet. 111-112.

- Applying Costa’s teachings to Seo would—at most—result in a constant V_{PASSL} on the unprogrammed word lines during T1 and T2, and a constant V_{PASS} voltage applied to programmed word lines during T1 and T2
 - Costa’s purported teachings** (i.e., that a lower voltage value can be used to turn on unprogrammed memory because of their lower threshold voltage) **would still apply to both time periods equally**

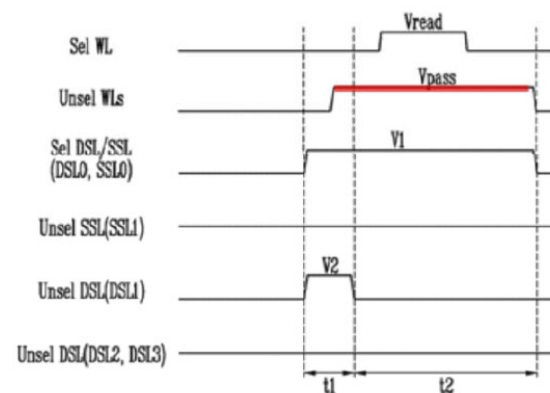
POSR 22-23; POR 66-67; Przybylski, ¶160.

- In a combined system, at no point does any of the unselected word lines receive a lower voltage during the second time period T2 relative to the voltage received in the first time period T1 (and thus the combined system fails to disclose or render obvious the claimed second bias voltage is smaller than the first bias voltage)

POSR 22-23.

Seo:

FIG. 8



POSR 21-22; POR 64-65; Przybylski, ¶¶157-158; Seo, [0087]-[0090], Fig. 8.

Ground 3: Costa in View of Seo Fails to Render Obvious First and Second Bias Voltages Wherein the Second Bias Voltage Is Smaller Than the First Bias Voltage

Petitioner argues: “A POSITA would have found it obvious that Seo’s first bias voltage is no lower than the standard read pass voltage because the same voltage level is applied to all unselected memory cells, including those already programmed, to ensure that they all conduct regardless of the program state. ... And as §XI.G further explains, **during verify, Costa seeks to reduce channel resistance issues without introducing read disturb due to an unnecessarily high read pass voltage on the unprogrammed cells**, in which case low V_{pass} voltages are optimal for unselected gates (e.g., gates of unprogrammed cells). **Thus, a POSITA would not have lowered Seo’s standard read pass voltage during pre-verify. Therefore, the second bias voltage (V_{readL}) is smaller than the first bias voltage (pass voltage V_{pass}).**” Pet. 111-112.

- Petitioner’s argument that it would have been obvious to apply Costa’s purported teachings only during period T2 is based on:
 - **Conclusory remarks from Dr. Liu** (he fails to cite any portion of Seo for his understanding of Seo’s bias scheme)
 - **Misinterpretations of the references** (Seo does not actually state that a “high V_{pass} voltage” is applied on all unselected memory cells during the first time period (or “must” be applied as argued at Pet. 128))
 - **Impermissible hindsight** (no reason but hindsight for adjusting voltages only in the second time period, or that why Costa’s teachings would be ignored during the initial time period)

POSR 22-23; POR 66-68; Przybylski, ¶¶159-164.

Ground 3: Costa in View of Seo Fails to Render Obvious First and Second Bias Voltages Wherein the Second Bias Voltage Is Smaller Than the First Bias Voltage

Petitioner argues in Reply: “*It would have been obvious to lower Seo’s Vpass only during the verify stage.* Ex. 1003 ¶ 308. Seo turns off the selected memory cell during the pre-verify stage. Ex. 1009, Fig. 8 (showing a low voltage on “Sel WL” during t1). *Without a conductive path across the selected memory cell, the source terminals of the cells above the selected cell are left floating and their voltages increase.*”

Reply 30.

- But this is an *improper new obviousness argument* not in the Petition
- Regardless, *neither the Reply nor Dr. Liu have provided any citation to Seo* for the proposition that there would be a floating voltage on the source terminals of the “cells above the selected cell” that increases over time
 - Seo does not mention such a phenomenon, nor does Seo describe using larger bias voltages on the “cells above the selected cell” to compensate for such a phenomenon
 - Even assuming such effects, *Costa’s teachings would still be applicable during both time period T1 and T2*

POSR 23.

Ground 3: Costa in View of Seo Fails to Render Obvious First and Second Bias Voltages Wherein the Second Bias Voltage Is Smaller Than the First Bias Voltage

Petitioner argues in Reply: “In any event, **only two realistic options exist** for the Vread level during the pre-verify stage: keeping it at the normal level or lowering it as in Costa’s verify stage. **A POSITA would have at least found it obvious to try both options and would have found the claims obvious.**”

Reply 31.

- But the obvious to try doctrine applies only when the options are “finite” and “*known*,” and here Costa does not even contemplate the idea of applying different bias voltages during different parts of a verify operation

Federal Circuit: “*To determine that an invention would have been obvious to try* on the basis of the record before the time of invention, this court has clarified, with respect to inventions requiring selection of a species from a disclosed genus, that ***the possible approaches and selection to solve the problem must be ‘known and finite.’*** ... Because one of ordinary skill could not use CFD simulations to detect endwall shock and ***no other evidence in the record gives a reason*** to reverse the sweep angle to intercept that shock, ***Rolls-Royce’s invention would not have presented itself as an option at all, let alone an option that would have been obvious to try.***”

Rolls-Royce, PLC v. United Techs. Corp., 603 F.3d 1325, 1339 (Fed. Cir. 2010); POSR 23-24.

- Applying Costa’s teachings in only one of the two stages violates the very purposes of Costa’s teachings—which is to reduce the voltages applied to unprogrammed memory cells
- The number of “options” does not refer to the binary choice of whether to apply a reference’s teachings (or whether to apply a reference’s teachings to certain aspects of the primary reference)—such a framing would erroneously reduce all proposed §103 combinations to one of only a handful of possibilities

POSR 23-24.

POSR 23-24.

IV. Top and Bottom Bias Voltages Limitations

Claims 5 and 6 Require the Application of a “Bottom Bias Voltage” and a “Top Bias Voltage” in the Pre-Verify Stage and the Verify Stage

- Claim 5 of the '957 recites:

[5.a] apply a **bottom bias voltage** on a gate terminal of the BSG transistor of the first memory cell string in the pre-verify stage and the verify stage;

[5.b] apply a **top bias voltage** on a gate terminal of the TSG transistor of the first memory cell string in the pre-verify stage and the verify stage; and

- Claim 6 of the '957 recites:

[6.a] apply a **bottom bias voltage** on a gate terminal of the BSG transistor of the first memory cell string in the pre-verify stage and the verify stage;

[6.b] apply a **top bias voltage** on a gate terminal of the TSG transistor of the first memory cell string in the pre-verify stage and the verify stage; and

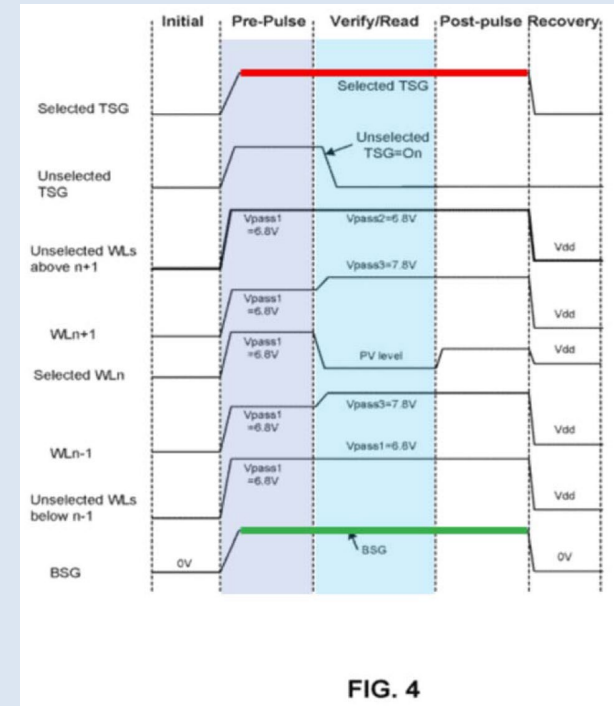
Top and Bottom Bias Voltages Limitations (Claim Construction)

The Term “Apply a [Top/Bottom] Bias Voltage on a Gate Terminal of the [TSG/BSG] Transistor of the First Memory Cell String in the Pre-Verify Stage and the Verify Stage” Requires a Single Voltage Level To Be Applied in the Pre-Verify Stage and the Verify Stage

- The plain meaning of applying “a [top/bottom] bias voltage ... in the pre-verify stage and the verify stage” requires that the same voltage level be applied in **both** the pre-verify stage and the verify stage
- The '957 depicts and describes that the same voltage is applied to the BSG/TSG during **both** the pre-verify stage and the verify stage:

'957 Patent: “When the verify/read operation is started, in the initial stage of the verify/read operation shown in FIG. 4.... Further, appropriate bias **voltages can be applied** on the selected TSG layer, the unselected TSG layer, the WLs ($>n+1$), the $WLn+1$, the WLn , the WLs ($<n-1$), and the BSG layer **in the pre-pulse stage** respectively. For example, **a bias voltage (or top bias voltage), such as 5 volts, can be applied on the selected TSG layer of the selected memory cell string.** ... In addition, **a bias voltage (or bottom bias voltage), such as 5 volts, can be applied on the BSG layer.**”

'957, 10:57-11:15; POR 13-17; Przybylski, ¶50; POSR 1-2.



'957, Fig. 4; POR 13-17; Przybylski, ¶50; POSR 1-2.

'957 Patent: “When the verify/read operation proceed to the verify/read stage, **the bias voltage (or top bias voltage) applied on the selected TSG layer of the selected memory cell string remains.** ... In addition, **the bias voltage (or bottom bias voltage) applied on the BSG layer can be maintained** to keep the channel of the selected memory cell string conductive.”

'957, 11:16-57; POR 13-17; Przybylski, ¶50; POSR 1-2.

- The other embodiments of the '957 similarly illustrate the top bias voltage and bottom bias voltage having a constant value that is applied in both a pre-verify stage and a verify stage

Top and Bottom Bias Voltages Limitations (Claim Construction)

The Term “Apply a [Top/Bottom] Bias Voltage on a Gate Terminal of the [TSG/BSG] Transistor of the First Memory Cell String in the Pre-Verify Stage and the Verify Stage” Requires a Single Voltage Level To Be Applied in the Pre-Verify Stage and the Verify Stage

Petitioner argues: “To the extent that Patent Owner argues “a bottom bias voltage” must have only one voltage level, Patent Owner is wrong. ... *[T]he bottom bias voltage may have more than one voltage level*... Like the bottom bias voltage, *a top bias voltage also need not have only one voltage level* for the same reasons.”

Pet. 61-64, 96-98; Reply 3-7.

- But Petitioner’s construction contradicts the plain language of the claim, which requires “a [top/bottom] bias voltage” in both stages, and the specification (slide 38)

Pet. 62 (citing *Elkay Mfg. Co. v. Ebco Mfg. Co.*, 192 F.3d 973, 977 (Fed. Cir. 1999)); *see also* Reply 3-4.

Petitioner argues: “‘a’ can mean more than one”

Pet. 61-64, 96-98; Reply 3-7.

- But while “*a*” in the claim language allows for multiple bias voltages (and multiple gate terminals) to be present in the claimed apparatus, it does not remove the requirement that the same *claimed* “bias voltage” must be applied “*in the pre-verify stage and the verify stage*”

Pet. 61-64, 96-98; Reply 3-7.

Federal Circuit: “[T]he indefinite article a means one or more in open-ended claims containing the transitional phrase comprising ... *But that is a separate issue from whether the claims require the same component to perform multiple functions or satisfy multiple limitations of a claim.*”

Finjan LLC v. SonicWall, Inc., 84 F.4th 963, 974-975 (Fed. Cir. 2023); POR 15-16.

Federal Circuit: “[I]t does not suffice to have multiple [claimed elements], each able to perform just one of the recited functions; *the claim language requires at least one [claimed element] capable of performing each of the recited functions.*”

Salazar v. AT&T Mobility LLC, 64 F.4th 1311, 1318 (Fed. Cir. 2023); POR 15-16.

The Term “Apply a [Top/Bottom] Bias Voltage on a Gate Terminal of the [TSG/BSG] Transistor of the First Memory Cell String in the Pre-Verify Stage and the Verify Stage” Requires a Single Voltage Level To Be Applied in the Pre-Verify Stage and the Verify Stage

Petitioner argues on Reply: “PO incorrectly construes the top/bottom-bias-voltage limitations to require ‘a single voltage level be applied in both the pre-verify stage and the verify stage.’ ... *[I]t does not restrict a “voltage” to a particular numerical value*; a “voltage” can take on multiple levels.”

Reply 3-4.

- But Patent Owner’s construction does not require a specific voltage level or value
- Rather, the issue is whether the same voltage (whatever voltage that is) must be applied in both the pre-verify and verify stages (see slide 38)
- The claims do *not* recite, for example, a first bias voltage applied in the pre-verify stage and a second bias voltage applied in the verify stage

POSR 3-4.

Top and Bottom Bias Voltages Limitations (Claim Construction)

The Term “Apply a [Top/Bottom] Bias Voltage on a Gate Terminal of the [TSG/BSG] Transistor of the First Memory Cell String in the Pre-Verify Stage and the Verify Stage” Requires a Single Voltage Level To Be Applied in the Pre-Verify Stage and the Verify Stage

Petitioner argues: “[T]he ’957 specification discloses that “the bottom bias voltage” and “the top bias voltage” can be increased from an initial level to a target level “(e.g., 5 volts)” during the pre-verify stage. ... Thus, it does not restrict a “voltage” to a particular numerical value; a “voltage” can take on multiple levels.”

Reply 3-4 (citing ’957, 13:43-53).

- But the ’957 discloses applying the same voltage in both stages:

’957 Patent: “The [top/bottom] bias voltage can be **maintained** through the second portion of the pre-verify stage and the verify stage.”

’957, 13:43-54; POSR 3-4; POR 13-17; Przybylski, ¶¶50.

’957 Patent: “[T]he [bottom/top] bias voltage ... is **maintained** through the second portion of the preverify stage and the verify stage.”

’957, 2:56-61, 4:4-9; POSR 3-4; POR 13-17; Przybylski, ¶¶50.

’957 Patent: “When the verify/read operation proceed to the verify/read stage, **the bias voltage (or top bias voltage) applied on the selected TSG layer of the selected memory cell string remains**. ... In addition, **the bias voltage (or bottom bias voltage) applied on the BSG layer can be maintained to keep the channel of the selected memory cell string conductive**.”

’957, 11:16-57; POR 13-17; Przybylski, ¶¶50; POSR 1-2.

Top and Bottom Bias Voltages Limitations (Claim Construction)

The Term “Apply a [Top/Bottom] Bias Voltage on a Gate Terminal of the [TSG/BSG] Transistor of the First Memory Cell String in the Pre-Verify Stage and the Verify Stage” Requires a Single Voltage Level To Be Applied in the Pre-Verify Stage and the Verify Stage

Petitioner argues: “[T]he positive voltage of Figure 7—PO’s chosen claim-construction embodiment—cannot rise to its target level (dotted red lines above the waveforms)—if at all—until long after the pre-verify stage. Thus, it becomes even more apparent that Figure 7 cannot satisfy PO’s claim construction. PO’s claim construction would read out PO’s chosen embodiment of the claim terms.”

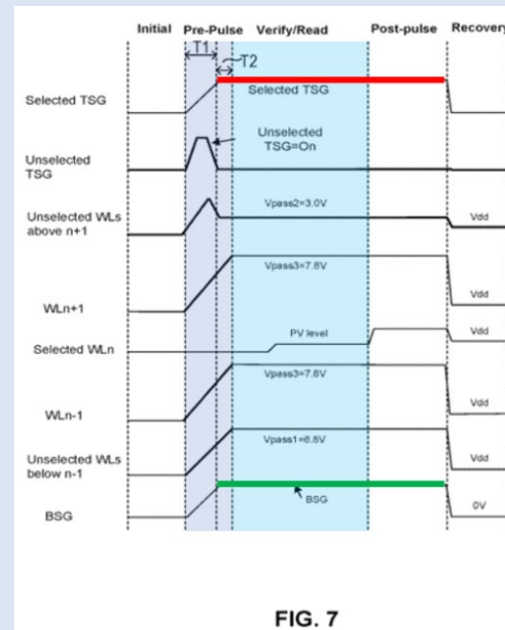
Reply 5-6.

- But it was the Petition that first pointed to Figure 7 (as somehow illustrating that the voltage of limitation [5.C] having multiple voltage levels)
 - The only reason Patent Owner cited Figure 7 was to rebut Petitioner’s argument

POSR 4-6; Pet. 7, 67; POR 16; Przybylski, ¶52.

- Contrary to Petitioner’s assertion**—the top/bottom bias voltages in Figure 7 *are maintained at a single voltage level in both the pre-verify and verify stages*

POSR 4-6; POR 16; Przybylski, ¶52.



- The '957 expressly states that the gate voltages fully develop to their target values:

'957 Patent: “Compared to the verify/read operation in FIG. 5, **the bias voltages applied in the pre-pulse stage can be full developed to (or completely reach) target values in FIG. 7.**”

'957, 13:13-21; 12:28-42; POSR 5-6; see also POR 13-17; Przybylski, ¶¶48-54.

The Term “Apply a [Top/Bottom] Bias Voltage on a Gate Terminal of the [TSG/BSG] Transistor of the First Memory Cell String in the Pre-Verify Stage and the Verify Stage” Requires a Single Voltage Level To Be Applied in the Pre-Verify Stage and the Verify Stage

Petitioner argues: “[T]he ‘positive voltage’ of claim 5, as shown in Figure 7, does not reach a single level until the verify stage. ... Thus, a single positive-voltage level does not exist in both stages, and *PO’s construction reads out the very embodiment on which it relies.*”

Reply 4-5

- But, again, Patent Owner cited Figure 7 only to rebut Petitioner (slide 42)
- Patent Owner never took a position on the construction of the term “a positive voltage” or whether Fig. 7 meets that term

POSR 4-6.

- Other '957 embodiments such as those relating to Figures 4, 6, and 8 teach the same positive voltage applied to unselected word lines in both stages

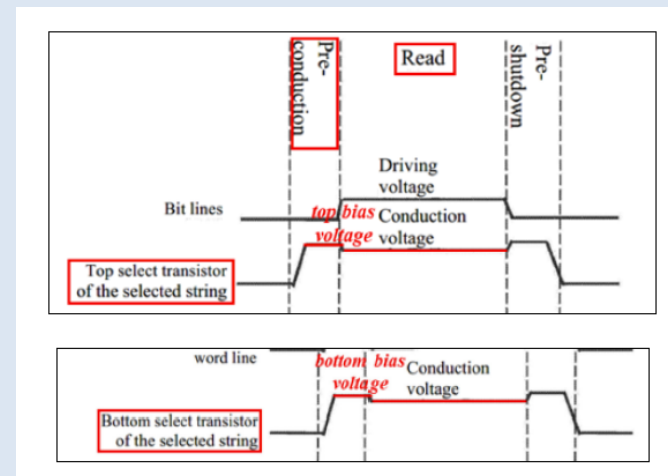
POSR 4; '957, 11:16-34, Figs. 4, 6, 8; *see also* POR 13-17; Przybylski, ¶¶48-54.

Ground 1: Hongtao in View of Yu Fails to Render Obvious a “Top Bias Voltage” or “Bottom Bias Voltage” Applied “In the Pre-Verify Stage and the Verify Stage”

Petitioner argues: “Hongtao discloses *apply[ing] a bottom bias voltage* (a pre-conduction voltage and conduction voltage) *on ... the BSG transistor of the first memory cell string* (the selected string) *in the pre-verify stage* (the pre-conduction phase) *and the verify stage* (the read phase):

Pet. 61-69.

- But Hongtao illustrates *target voltages* rather than *actual voltages applied to the gate terminals* (slides 20-24)
- Even if Hongtao depicted actual voltages (it does not), *that would mean Hongtao expressly shows different voltages being applied to the select gates during the different stages*



POR 45-46; Hongtao, Fig. 2; Przybylski, ¶¶111-112.

- Yu fails to address these deficiencies because Yu does not disclose or render obvious that bias voltages are applied to TSG and BSG transistors in the pre-verify stage and verify stage, and Petitioner does not allege that it does

POR 47; Pet. 61-69; Przybylski, ¶114.

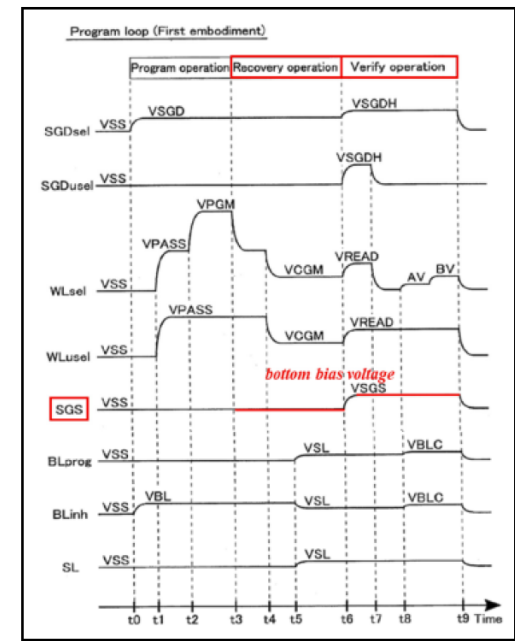
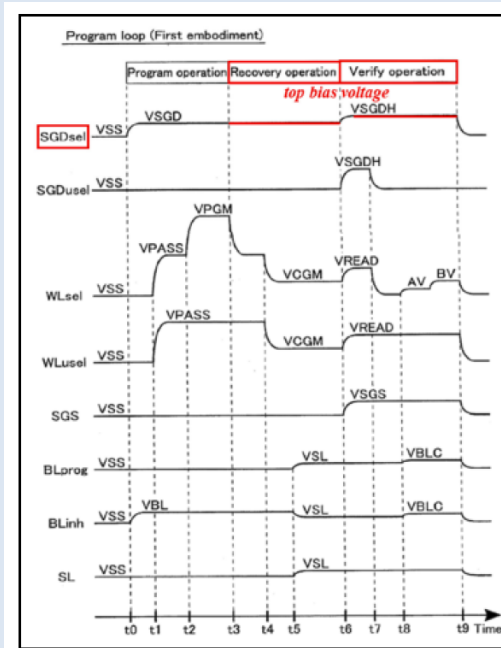
- Petitioner’s only argument on Reply is its incorrect claim construction (see slides 38-43)

Ground 2: Suzuki Fails to Disclose a “Top Bias Voltage” or “Bottom Bias Voltage” Applied “In the Pre-Verify Stage and the Verify Stage”

Petitioner argues: “Suzuki discloses *apply[ing] a bottom bias voltage* (VSS and VSGS) *on ... the BSG transistor of the first memory cell string in the pre-verify stage* (the recovery operation) *and the verify stage* (the verify operation).”

Pet. 96-97.

- But Suzuki does not disclose a single [top/bottom] bias voltage applied in the pre-verify stage and the verify stage
- The voltage applied to the purported top select gate changes from a value of “VSGD” to a value of “VSGDH” at the start of the verify stage
- The voltage applied to the purported bottom select gate changes from a value of “Vss” to a value of “VSGS” at the start of the verify stage



POR 56-58; Przybylski, ¶¶134-140; POSR 20.

- Petitioner’s only argument on Reply is its incorrect claim construction (see slides 38-43)

POSR 20; Reply 27.