

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner,

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,
Patent Owner.

IPR2024-00792
Patent 11,468,957 B2

Record of Oral Hearing
Held: August 7, 2025

Before: JO-ANNE M. KOKOSKI, KIMBERLY McGRAW, and
MICHAEL T. CYGAN, *Administrative Patent Judges*.

APPEARANCES:

ON BEHALF OF THE PETITIONER:

JEREMY JASON LANG, ESQUIRE
Orrick, Herrington, & Sutcliffe LLP
1000 Marsh Road
Menlo Park, CA 94025
jlang@orrick.com; (650) 614-7427

JOHANNES HSU, ESQUIRE
Orrick, Herrington, & Sutcliffe LLP
2050 Main Street, Suite 1100
Irvine, CA 92614
johanneshsu@orrick.com; (949) 852-7776

W. DAVID WESTERGARD, ESQUIRE
Micron Technology, Inc.
8000 S. Federal Way, MS 1-507
Boise, ID 83716
dwestergard@micron.com; (208) 841-3053

ON BEHALF OF THE PATENT OWNER:

ANDREW RADSCH, ESQUIRE
CHRISTOPHER M. BONNY, ESQUIRE
Ropes & Gray LLP
525 University Avenue, 8th Floor
Palo Alto, CA 94301
andrew.radsch@ropesgray.com; (650) 617-4763
christopher.bonny@ropesgray.com; (650) 617-4011

The above-entitled matter came on for hearing on August 7, 2025, commencing at 1:00 p.m., at the U.S. Patent and Trademark Office, 600 Dulany Street, Alexandria, Virginia.

P R O C E E D I N G S

- - - - -

JUDGE CYGAN: Good afternoon. This is Judge Cygan. Judges McGraw and Kokoski are in my video. We'll now hear argument in case number IPR2024-00792, U.S. Patent number 11,468,957, between Petitioner, Micron Technology and Patent Owner, Yangtze Memory Technologies. Counsel for the parties, starting with Petitioner, please introduce yourself.

MR. LANG: Good afternoon, Your Honors. Jason Lang, lead counsel for Micron. With me is my colleague, Johannes Hsu, and with me from Micron is senior director of licensing and litigation, Dave Westergard.

JUDGE CYGAN: Would you be presenting?

MR. LANG: I will be on a few of the grounds. One of the grounds, Mr. Hsu will be presenting. We had submitted and were granted a LEAP request for that.

MR. RADSCH: Good afternoon, Your Honors. I'm Andrew Radsch from Ropes & Gray for Patent Owner. I'm joined today by Chris Bonny. And with us on the public line today is chief IP counsel for YMTC. I will be covering Ground 1 today, and Mr. Bonny will be covering Grounds 2 and 3.

JUDGE CYGAN: Thank you. Welcome back to the Board. Per our hearing order, we provide each parties with 60 minutes of oral argument. Petitioner's LEAP request gives you an extra 15 minutes, which gives you about 75 minutes for both of you. The parties need not to use the entirety of that time. Petitioner will argue first. You may reserve time for rebuttal.

1 Patent Owner will respond to Petitioner's arguments and may reserve time
2 for sur-rebuttal. We have the demonstratives from each party. Please
3 remember to identify yourself when speaking. Also, please remember to
4 identify the slide number you're on. As you notice, we are participating by
5 video. Petitioner, how much time would you like to reserve for rebuttal?

6 MR. LANG: Twenty minutes, Your Honor.

7 JUDGE CYGAN: Thank you. Petitioner, you may begin.

8 MR. LANG: Well, Your Honors, good to see you again. I hope
9 you had a good break. Today, we'll go over the '957 Patent, and I'll turn to
10 slide 4, and just briefly highlight the grounds. The first ground is Hongtao
11 and Yu. I'll be covering Ground 3 as well, Costa and Seo, and my colleague
12 will be handling the second ground, Suzuki.

13 Turning to slide 6, just a few points on the '957 Patent, to start.
14 Here, we have the present disclosure describes embodiments generally
15 related to apparatuses and methods for verifying/reading. There's going to
16 be a lot of talk from Patent Owner today that somehow verifying and reading
17 are two discrete operations. Not, so. That's belied by the '957 Patent itself.
18 I'll go over the additional evidence to that effect as well. Second, the '957
19 Patent relates to a technique for reducing something known as hot carrier
20 injection, and we abbreviate it HCI.

21 I'll get to the claim language as the issues come up, but I want to
22 skip to slide 8 and point out a few things. So, one, we'll be talking about if
23 you see the red circle, there is a requirement that the second bias voltage,
24 which is to the right of that red circle, is smaller than the first bias voltage,
25 which is to the left of that circle.

1 I do want to note, again though, if we look at this '957 figure it
2 says, verify/read. Again, this notion that these are different operations is
3 belied by the '957 Patent itself. Indeed, the period before the verify/read is a
4 pre-pulse period rather than called pre-verified here. This is just the period
5 before the verify/read, which assists with setting up the device to reduce this
6 HCI.

7 Last, turning to slide 10, just an overview of Hongtao. Hongtao
8 relates to a process for reading. On that there you see there at the bottom,
9 avoiding the problem of hot carrier injection. That paragraph 23, in fact,
10 discloses, or describes the effect of the pre-conduction phase, which comes
11 before the pre-phase before the read.

12 Turning to slide 11, again, overview of Hongtao. Notably we see
13 here, in the red circle, from the first phase, the pre-conduction phase to the
14 read, from the first bias to the second bias, the second bias is smaller. I have
15 an enlarged picture of that I'll get to in a minute. But I do want to note in the
16 overall context, when you look at the transition from the pre-condition to the
17 read, some of those lines go up, some of them go down. In fact, some of
18 them stay flat, the bottom one, for example. Figure 3 is the same, but
19 clearly, from looking at this figure, we see that the second bias is less than
20 the first bias. We cite various case law, *In re Boyd*, (INDISCERNIBLE) on
21 that. We point to paragraph 26, which talks about the general principle of
22 wanting to lower conduction voltage, and you see it right there.

23 Turning to slide 12, a bit on Yu. What Yu stands for is a couple
24 well-known concepts. Within the last couple weeks, we've talked about
25 these vertical memory channels quite a bit. And if we imagine one of these

1 vertical memory channels, it's very common to program them from the
2 bottom to the top, and Yu describes that.

3 Secondly, Yu describes the fact that, after you program, you do a
4 re-command, it's called a verification. And why do you do that? Let's take
5 the instance of writing a 1 to a memory cell, okay. After you write a 1, you
6 read it. If I read a 1, that tells me my program was successful, I verified it.
7 So, this is getting back to the concept of a read, where verification is simply
8 a read after a program step.

9 Turning to slide 13. Now, the disputes are, one dispute,
10 effectively, Patent Owner is saying, despite what Hongtao says, despite that
11 he discloses he's applying voltages on the gate terminals, but in fact Hongtao
12 does not show that. So, they tried to draw this distinction between a voltage
13 on a word line and a voltage on the gate. That fails on multiple accounts.
14 Then they -- Arguments 2 and 3 are related. They're saying, basically,
15 Hongtao, in view of Yu, does not render obvious a verify and a pre-verify
16 stage. I'll get to claims 5 and 6 shortly.

17 So, turning to slide 14 in the claim language, the claims require
18 applying various voltages on a gate terminal. And as we talked about,
19 turning to the next slide, slide 15, two of the limitations, together, require
20 that you would have a -- in that first phase, a larger voltage than the second
21 phase. Hongtao clearly shows that as you see in that picture.

22 And so what Patent Owner has done is say, what you see is not
23 what you really see. That's their red line. They magically draw this red line
24 that just magically never gets above the black line on the right until the
25 conduction phase or the read phase. They do that to argue the claim

1 limitation is not met. As you see there, Patent Owner says the target voltage
2 applied to the word line, it's different from this gate terminal voltage. And
3 so, they say, if you actually look at the gate terminal voltage, you'd have this
4 red line.

5 Well, this argument fails for a host of reasons, one, Hongtao says
6 the opposite. Two, none of the prior art draws this distinction that Patent
7 Owner is alleging. It's inconsistent with all the records. Three, it distorts the
8 '957 Patent into that none of its figures even represent these claimed gate
9 terminals, just -- and, in fact, it creates this situation that memory wouldn't
10 work in real life that, I'll get to.

11 But I want to start with Hongtao, turning to slide 16. There's just
12 no other way to read this reference. Here is Hongtao at paragraph 25. This
13 was recited in the institution decision. The gates of the unselected memory
14 cells on the selected string are applied with a conduction voltage. You
15 cannot look at Hongtao and say that the conduction voltage is not applied to
16 the gates, it says it right there. It just -- Patent Owner is asking you to ignore
17 Hongtao's expressed disclosures, and instead, make up this red line. That is
18 just legally erroneous. It's given no basis to ignore Hongtao's express
19 disclosure. That is a gate voltage. It says the conduction voltage is applied
20 to the gate of the memory cell, right there.

21 It goes up -- it ramps up. They talk about, well, these voltages
22 need to ramp up. Guess what, it ramps up. If it was just a target voltage, it
23 would just be a plateau, there'd be no ramp-up. It ramps up. It stays at that
24 ramped-up point. It drops down. The second bias voltage is smaller than
25 the first bias voltage. It expressly says it. It shows it. If you look at all the

1 figures, some go up, some go down.

2 In paragraph 26 it says you want that conduction voltage low.

3 There's a reason it drops. There's no way around that disclosure.

4 Turning to slide 17. Now, this distinction that they're trying to
5 draw that there's some difference between a word line and a gate terminal,
6 okay? So, we've talked a lot about these memory devices. You may have a
7 staircase contact over here, the gate layers for the word lines here, and along
8 the way you have memory cells. Well, as I understand their argument,
9 they've drawn this distinction between what's on the word line here, and
10 maybe the gate of a memory cell here. Of course, you'd have another gate
11 with a memory cell here, here, here, here, here, and along the way. The
12 '957, the prior art reject that there's some difference between the two.

13 The '957 Patent itself, on slide 17, they talk about word-line
14 voltages, and where do they draw the word lines on the left? They put the
15 word line right at the control gate terminal of the memory cell. There's no
16 time constant between there. There's no -- they don't show some type of
17 delay. It's rejected by the '957 Patent itself.

18 Turning to slide 18, Patent Owner said, oh, well, if it's curved, it
19 means gate, not word line. And Suzuki's curved, so apparently Suzuki is
20 showing gate. But then why does Suzuki say, the voltage is applied to the
21 word line? That's because there is no difference between the word line and
22 the gate. The art uses them interchangeably.

23 Indeed, turning to slide 19, we see Lien. We've cited various
24 references in the paper to further establish this. On the left --

25 JUDGE CYGAN: (CROSSTALK).

1 MR. LANG: Sorry, Your Honor.

2 JUDGE CYGAN: Let me interject for a second. Should the
3 public line be on or off for this proceeding? Is there any need for the public
4 line to be off? I am understanding it's supposed to be open.

5 MR. LANG: It can be open.

6 MR. RADSCH: Open, I believe, Your Honor.

7 JUDGE CYGAN: Okay. Thank you.

8 MR. LANG: So, Your Honor, on slide 19, in the papers, we had
9 pointed out various prior art references where this false distinction has just
10 proven to be false. If you look at Lien on the left, it describes a gate voltage
11 and it says that it's applying it to the selected word line, but yet it shows a
12 curved waveform.

13 And according to Patent Owner's argument, curve mean it's a gate
14 voltage not a word line voltage. If you look on the right, in Ko, and it's
15 saying applying -- a word line voltage applied to the gate, but yet it just calls
16 it a word line voltage and shows it on the word line. That is because there is
17 no distinction between this word line and gate, the art uses them
18 interchangeably. Because, after all, we're talking about an operation on the
19 memory cell. They're showing the voltage on the memory cell. But that is
20 only in addition because we can't lose sight of the fact that Hongtao says the
21 voltages are applied on the gates.

22 Turning to slide 20, I do want to make this point. And I have a
23 slide later coming up, but if you applied PO's interpretation to the '957
24 Patent itself, I guess you would have to take all of the straight line figures,
25 which are in all of the figures except the figure that doesn't embody the

1 claim, and you would have to add some type of curve to it. And then you
2 ask yourself, does the voltage really go from bigger to smaller because I
3 guess there's some curve. And so, the '957 Patent, all of a sudden, not even
4 showing gate voltages yet it claims it.

5 Then there's another real-world complication that's telling.
6 According to their expert, this delay, apparently from the word line to the
7 control gate is some complicated aggregation of factors, and it's going to be
8 different for every memory cell. Well, if you think about it, you got your
9 staircase contact, and I've got, I guess, to them, some type of delay here,
10 another delay here, another delay here. Maybe I'm programming this one,
11 but the signal hasn't even got over here yet. None of the references talk
12 about this time delay between the different memory cells as
13 (INDISCERNIBLE).

14 Now, I'm going to turn to slide 21 and the second argument.
15 Patent Owner argues verifying and reading are distinct operations, and
16 therefore it would not be obvious to use Hongtao's read operation for
17 verifying, okay? These are not distinct operations. There is not a better case
18 for a predictable use of a known prior art feature. Verification is simply a
19 read after a program. Let me walk you through the evidence. And in fact,
20 the '957 Patent itself tells you that.

21 I want to start with slide 22. So, to start with, Yu stands for the
22 fact that after you program, you're going to do this verification, okay? And
23 I'll show you, that's just a read after the program. This is the petition here,
24 citing Exhibit 1021. Exhibit 1020 and 1017 will say the same. Indeed, the
25 read operation may include the verification operation for verifying the

1 success of the program operation. That's what I was talking about, you read
2 after you program to verify that you programmed correctly. It continues, the
3 read operation may include the verification or the normal read operation for
4 determining data stored.

5 This read is both for the normal read and for verification. The
6 petition demonstrates several advantages of just using that same read
7 operation on -- well namely, number one, you really need to verify after you
8 program to make sure you program correctly. That hasn't been disputed, nor
9 has it been disputed that you have this advantage of, once you create a read
10 operation, why do you want to start from scratch to reinvent the wheel and
11 create a whole new read operation to do the same function after a program.
12 It makes no sense.

13 Now, I want to jump first to slide 24, and this basically says the
14 same as Exhibit 1021. All any read is, some people call it a sensing
15 operation, if you turn on all the other transistors, except the one you're
16 reading, and then you sense what's in that selected memory cell.

17 And here's Exhibit 1017, in a flowchart of one embodiment of the
18 process of sensing memory cells. Continuing, the sensing operation is a
19 program verify, in another embodiment, the sensing operation is a read in
20 one embodiment, okay? So, again, you can call it a read, you can call it a
21 sense, but it's for two things: for a program verify or for a normal read.

22 In turning back to slide 23, Patent Owner would say, oh, these are
23 distinct, these are unique, bias (INDISCERNIBLE) scheme I think they're
24 saying. There's two -- there's just two -- there's one difference and then one
25 optional capability that I'll get to.

1 As 1017, 1020, and 1021 describe, it's been known for many
2 decades, the real difference is, as I said, you open up all -- and turn on all the
3 other transistors except the one you're sensing, and then you apply a voltage
4 to that selected memory cell. If it's a read, you apply a read voltage.

5 And let me just back up a step and say, what this is showing, this
6 figure is showing, that A, B, C, D, E, those are data states. Those data states
7 are represented by threshold values. And so, when you do a read, you see
8 that first green box, you're checking between data state, okay? If it turns on,
9 I know I at least got an A there. If it's a verify, that's the first red box, you
10 just move it over a little bit, because you want to verify that you got enough
11 electrons in there that you're in the A state. Okay, that is a difference on the
12 read. All it is, is a slight tweak of the read voltage/verify voltage.

13 I do want to turn now to the '957 Patent, which is very telling,
14 okay? The '957 Patent, okay, that apparently the PO would tell you is all
15 about verification, it's so different that read. Well, what does the '957 Patent
16 say? On the left there, Figure 10 is a flowchart diagram of a method for
17 reading a memory device. And then it goes on, and it talks about verifying.
18 Because this is just the flavor where it's being done after a program, and the
19 verify voltage instead of the read voltage is going to be applied, yet they still
20 call it a reading operation.

21 Indeed, claim 1, on the right, a apparatus for reading a memory
22 device. It cannot be said with a straight face that reading and verifying are
23 so different and distinct when the '957 Patent itself is claiming a device for
24 reading.

25 The last portion at the bottom there is very telling as well. It states

1 in addition, a read (or verify) voltage can be applied on the gate terminal (or
2 gate) of the selected memory cell. Two points: they just correlated gate
3 terminal (or gate). So, this idea that somehow the word line is different than
4 the gate terminal. But the bigger point here, a read (or verified) voltage can
5 be applied on the gate terminal of the selected memory cell. That is exactly
6 what I just showed, going back to slide 23, which was known for many
7 decades. It is described in 1017, 1020, and 2021. All you're doing that is
8 different is applying either a read voltage or a verify voltage.

9 And going back to slide 25, the '957 Patent itself recognizes, in this
10 read operation, that that's all you do, either apply a read or verify. You
11 apply a read voltage, it's a read op. If you apply verify, it's a verify. So,
12 everything is consistent in the prior art of the '957, that a verification is a
13 read after a program. This is Hongtao's read, the most predictable use,
14 established use, assumed use, is that it's used as a read after a program,
15 which is a verification.

16 Turning to slide 26. Indeed, their own expert, we asked him about
17 read operations, he just started talking about read verify operations. And it
18 just shows how folks think about them.

19 Turning to slide 27, Patent Owner hangs their hat on that there's
20 this optional capability with the verify. With the verify, because you just did
21 the programming -- you're doing the programming, if you're programming
22 bottom-to-top, you do know that, for example, what's below you is
23 programmed. What's above you is not programmed.

24 Accordingly, there's this optional capability to drop the pass
25 voltage a little bit on top. It's an optional capability that does not negate and

1 make disappear all the evidence I just showed you that people consider a
2 verification, simply a read after a program. It's an optional capability that
3 they admit it was optional. Suzuki does not do it. Costa, at paragraph 96,
4 which we cite in our papers says you can do it or not do it. More
5 importantly, it has no effect on the claims. There's no claim requirement
6 that unprogrammed verse programmed voltages. In fact, they have not
7 argued, nor could they, that if you applied this optional capability, it would
8 take the combination outside of the claim scope, it would not. This is
9 irrelevant to the issues at hand.

10 Finally, with respect to -- they further make their argument, well,
11 now there's no (CROSSTALK) --

12 JUDGE CYGAN: Counselor --

13 MR. LANG: Yeah.

14 JUDGE CYGAN: Before you move to that one, I have one
15 question about how you frame the combination in your petition. In the
16 section where you're discussing using read to verify, around petition 72, 73,
17 you state a POSITA would have been motivated to employ Hongtao's read
18 operation, which reduces these problems for verification. And before that,
19 you had talked about how they're nearly identical.

20 So, is your argument that the combination is taking Hongtao's
21 specific read operations, the specific voltages, the specific timings, and then
22 applying that for the purpose of verification? Were there any tweaks that
23 were going to be undertaken when it's being moved from read to
24 verification?

25 MR. LANG: Yeah, the only tweak that we talked about that is

1 necessary -- and we talked about it in the reasonable expectation of success,
2 is that you move the -- like I said, instead of a read voltage that's applied on
3 the selected word line, it's a verify voltage. That was the slide -- let me just
4 briefly go back. That was slide 23. So, we discussed this in our papers that
5 that's the difference, and a POSITA would have a reasonable expectation of
6 success because this change was well known, Exhibit 1017, 20, 21, all
7 describe this.

8 JUDGE CYGAN: Thank you.

9 MR. LANG: With respect to the arguments against read pre-
10 verification, and look, there can't be a dispute now that this read -- I'm
11 looking at slide 29, my apologies, that this read is for a read/verify.
12 Certainly, it would be obvious to do this after a program. Okay. So now,
13 we're at the verification step, okay?

14 So, what comes before that? You know, the '957 Patent just calls it
15 the pre-pulse. What Hongtao is describing -- let me move to slide 30. What
16 Hongtao is describing is this pre-phase, this pre-conduction phase, pre-
17 conditioning the channels to avoid HCI.

18 And let me skip to slide 31. It's right here in paragraph 23.
19 Paragraph 23 is all about pre-conditioning these channels to avoid hot carrier
20 injection (HCI). It's precisely what the '957 Patent is talking about in its
21 pre-pulse period. It occurs before the sensing, before their verification,
22 therefore it's a pre-verification step, Your Honors.

23 Your Honors, I want to turn to slide 32 in the arguments against 5
24 and 6. And turning to -- now, let me turn to the claim language, slide 33.
25 The claims require, for the bottom bias and the top bias voltage, to apply a

1 bottom bias voltage -- skip some -- let's go back, and then in the pre-verify
2 and the verify stage, okay? We can go over our arguments with the bottom
3 bias voltage the same.

4 I have to point out -- I want to point out, importantly, that indeed,
5 there's another limitation that PO doesn't want to grapple with that says
6 apply a positive voltage in the pre-verify and verify stage. It has the same
7 structure. We cited the case law that these limitations with the same
8 structure need to be construed consistently. Patent Owner hasn't provided a
9 reason why they should not be (INDISCERNIBLE).

10 I want to turn to their argument, slide 34, and point out something
11 important. It feels like to me, they're changing their argument in sur-reply,
12 and I looked at their slides, and I think they're changing their argument.
13 Their argument in their Patent Owner response was -- and here it is at the top
14 bullet. The top and bottom limitations, quote, "Require a single voltage
15 level be applied in both the pre-verify stage and the verify stage." That was
16 their argument, a single voltage level.

17 It seems like to me that they might get up and say, no, no, all that's
18 required is the same voltage at some point in the first stage and the same
19 voltage at some point in the second stage. I will handle that in rebuttal, but
20 if they argue that, the prior art clearly discloses that, okay? But what their
21 PO argument is, is that you have to have the single level, so I'll address that
22 now.

23 This fails on multiple legal counts. It attempts to rewrite the
24 claims. It's inconsistent with how bias voltage is used in a specification, and
25 the positive voltage limitation, that has that same structure, absolutely means

1 its construction is incorrect. And, finally, it undermines their own -- that
2 first argument, they made the gate terminal argument.

3 So, again, that's what they're saying it means at the top -- that top
4 requires single voltage level. Single is found nowhere in the claim language,
5 level is found nowhere in the claim language. So, they're attempting to
6 rewrite it as follows: applying a top/bottom bias voltage to applying a single
7 -- just insert single bias voltage -- insert level. They cite no disclaimer, no
8 definitional language. Instruction fails on that ground alone.

9 Turning to slide 36, when we look at the specification it says the
10 bottom bias voltage can be increased from the initial stage to a target. It can
11 be increased. So, this voltage need not be at a level, it can be a changing
12 voltage. The bias voltage cannot be construed to be required to be a level
13 because it's described as changing. So, all that the claims require is a bias
14 voltage that's applied in both stages, and that voltage can be changing.

15 Turning to slide 37, this is critical. You see there, highlighted in
16 green on the left, apply a positive voltage. It, too says, in the pre-verify and
17 the verify stage. You see in the figure, it's highlighted green as well, the pre-
18 verify stage in yellow, and that voltage increases all the way through the pre-
19 pulse stage. It's never a level. So, to say that this claim structure somehow
20 requires a level is not found definitionally, not disclaimed, but moreover
21 would directly conflict with this embodiment for the positive voltage
22 limitation.

23 Turning to slide 38, just a quick point I want to make here, Your
24 Honors, is that if we were to take Patent Owner's argument about the gate
25 terminal versus the word line, well, I guess we'd have to take this figure

1 from the '957 and add all these curves to it. And then, if you looked at the
2 positive voltage limitation, it would never have even reached that level. And
3 so, this further shows -- and we couldn't even understand what this picture is
4 showing, because you've got to somehow make all these curves that aren't
5 disclosed or described in the '957 Patent, and it just undermines that
6 argument as well.

7 And I want to jump forward to the Costa in view of Seo ground.

8 JUDGE CYGAN: Counselor, one question on the language in
9 claim 5. What would be the difficulty with a claim construction, which is
10 more limiting, I guess, in the entire scope of the Patent, where the claim
11 scope is directed to just a single voltage? I'm trying to get a sense of the
12 difference between applying a voltage to the string in stage A and stage B,
13 and another possible way of writing that claim would be apply a voltage in
14 stage A and then applying a voltage in stage B. The second way of writing
15 that, clearly, you can have two different voltages. As I understand their
16 argument, it's a single voltage. What would be the problem with that as a
17 more limiting way of writing the claim?

18 MR. LANG: Well, I think the claim language, when you looked at
19 claim 1, for example, it discloses a first verify and a second verify voltage,
20 and it has no relative requirement between them. When they wanted to put a
21 relative requirement in there, they did. For the first bias voltage and the
22 second bias voltage, they said the second bias voltage has to be less than the
23 first. So, when they wanted to add some type of explicit relative
24 requirement, the claim language did.

25 And I would add, Your Honor, if you're asking again to this point

1 that I have their slides, that that contends a new argument, does the voltage
2 just need to be the same at some point? The prior art discloses that, and I
3 can handle that on rebuttal. Prior art discloses, it goes up and it goes down,
4 and then it stays flat over here. So, as it's going up, it is at the same level, or
5 same point. There's a point in time when this voltage in the pre is at the
6 same as this voltage in the sensing phase. So, if the construction you're
7 asking about is just does it need to be the same at some point, I would say
8 the specification doesn't support that, but the prior art certainly discloses
9 that.

10 JUDGE CYGAN: I'm not sure I understand your comparison to
11 claim 1 for support, because in claim 1 they're using literally first and second
12 voltages, whereas in claim 5, they're just supplying a voltage. I'm not sure
13 how, looking at claim 1, which has two separate specified voltages, lets us
14 assume that claim 5 with a single voltage should actually be read as two
15 separate voltages.

16 MR. LANG: Yeah, I think my point is, is that, if they wanted to
17 draw some type of requirement, relative requirement between the two
18 phases, they would write it into the claim language like they did with respect
19 to claim 1 for one limitation, where they said the second bias is less than the
20 first. So, I would think, actually, if they wanted to put that requirement in,
21 they would have put it into two, a first and second bias voltage, and would
22 have wrote wherein, the first and second are the same, something like that.
23 Because, clearly, the bias voltage, as the specification demonstrates, can be
24 increasing and can be changing.

25 JUDGE CYGAN: Thank you.

1 MR. LANG: Briefly, on Costa in Seo, I want to jump forward to
2 48. So, the ground starts with Costa, and we see here again, sensing may be
3 performed during reading, program verification, monitoring, et cetera. This
4 is all showing that a sense, a read can be a normal read, can be a
5 programming verification. The starting point we start with is Costa's
6 programming verification. That is a read after a program.

7 Turning to slide 50, what Costa teaches, importantly, is during the
8 read, during the sensing through the verification, that you have this ability,
9 and you can take the pass voltage for some of the unselected word lines, and
10 use VreadL, which is several millivolts in the standard read pass voltage,
11 less than standard read pass voltage. So, we're starting with that as the
12 second bias voltage.

13 Now, we're using Costa in view of Seo, so let me turn to Seo slide
14 47. And Seo discloses two phases. You have a first phase, T2, as the papers
15 explained, that's either a read, a verify -- you see the read voltage right there.
16 And then, so you ask yourself, what comes before that in T1? That is the
17 same pre-pulse, get ready period, as you see in the pre-pulse '957 Patent. I

18 In fact, turning to slide 49, Seo describes it at paragraphs 88 and
19 89, and what it is, is a technique that reduces HCI by applying voltages in
20 this T1 period. Seo specifically describes it at 88 and 89. And so,
21 effectively, what it's doing is, is it's locking these channel voltages before
22 you start to sensing in order to reduce HCI.

23 Now, turning to slide 51 -- sorry. Oh, just briefly, again, you see it
24 here on paragraph 89 of Seo itself, it's talking about this T1 period, and it
25 talks about reducing this disturb effect, again, HCI, which we had talked

1 about today. But how does Seo do that. It applies the pass voltage Vpass. It
2 doesn't talk about lowering Vpass. This is the Vpass that turns on all of the
3 transistors.

4 And so, where that brings us, turning to slide 52, is Patent Owners
5 argued that, well, Seo doesn't it itself, show this bias voltage, the first and
6 second going from high-to-low. They say, Costa, by itself, doesn't show it
7 going from high-to-low, okay. But obvious analysis has to look at the
8 collective teachings -- they have a collective teaching. And when we look at
9 the collective teaching, Costa is saying, during the sensing phase only --- it
10 doesn't describe a prefix. During the sensing phase only, I'm going to lower,
11 not use the standard VP (Vpass), I'm going to lower. So, now when we go
12 to Seo, he's saying, I'm applying the standard VP.

13 Now, Patent Owners argued, well, let's look at them collectively.
14 Why wouldn't you just still lower it like Costa? And you wouldn't for two
15 reasons. One, Seo is concerned with the different effect -- let's start with
16 HCI. Costa's concerned with its channel resistance. But more importantly,
17 Seo wouldn't work if you lowered it. Seo wouldn't work if you lowered it.
18 And let me explain why.

19 Patent Owner actually argues that this is an untimely argument in
20 their slides. It's not. I think they know that they have a problem with it, but
21 it's not a new argument. If you look at his original declaration at Exhibit
22 1003, paragraph 308, he describes the same thing. It's unrebutted. And it's
23 unrebutted because this is just how transistors have worked for 100 years.
24 What Seo described is, if you look at the top, that selected word line is off
25 -- this is during T1, he turns that off. He turns on all of the other transistors,

1 okay? He describes turning all the other transistors on with the Vpass
2 voltage.

3 All right. What is the issue, the problem with turning the selected
4 word line off? The issue that you have is -- remember, this is what Dr. Liu
5 describes, you remember this vertical memory channel structure? So, if I'm
6 turned off in the middle, I've got all these transistors above it. And for 90
7 years a transistor turned on, by the gate voltage minus the source voltage,
8 that's how it turns on. That has to be greater than a threshold. Dr. Liu
9 explained, as Seo 88 through 89 explains, that word line is off, and therefore
10 this is floating, and you have voltages building up on your source. You have
11 to apply this Vpass -- standard Vpass voltage because of the source voltage
12 building up to ensure that they turn on. So, you're not going to accomplish
13 Seo's point of reducing this HCI if you're not applying the higher Vpass
14 voltage.

15 At a bare, bare minimum, it would be obvious to try it for two
16 reasons. Seo says, apply the standard Vpass voltage and any POSITA would
17 look at this and say, with that selected word line off, I've got a problem.
18 These are floating, the source voltages are going to build, I'm going to need
19 to overcome that to turn it on. That testimony is unrebutted, okay? And it's
20 not new. You can look back. Their expert accurately addressed it initially,
21 in response to paragraph 308, and all he said was, well, Seo doesn't
22 expressly say that. He did not refute that -- and I disagree it doesn't say it,
23 because it shows the word line off. It doesn't go into the detail, the source
24 building up, sure. But he did not refute the explanation that because that
25 word line was off, you had this effect of voltages building up on the source.

1 So, if Your Honors have no other questions with those two
2 grounds, I'll turn it over to my colleague.

3 MR. HSU: Your Honors, good afternoon. My name is Johannes
4 Hsu. I'll be covering Ground 2, Suzuki, this afternoon, and this is slide 54.
5 Skipping to slide 56, an overview of Suzuki. Suzuki discloses a program
6 and verified loop. And like the '957 Patent, Suzuki's technique addresses the
7 issue of hot carrier injection by mitigating its effect. Suzuki's technique also
8 improves the error that might occur in a re-verifying operation. And as the
9 first sentence in paragraph 153 indicates, the way Suzuki does that is by
10 performing a recovery operation between program and verifying. And this
11 recovery operation pulls electron out of the channel, which if they were
12 allowed to remain in the channel, would cause a data retention issue that
13 would later cause verify or read errors.

14 Moving to slide 57. And like we just described, Suzuki's technique
15 uses this recovery operation that's highlighted in yellow to remove electrons
16 out of the channel. And this improves the accuracy of a subsequent
17 verifying operation. And this is accomplished, using the waveform that's
18 shown here in Figure 11, including applying a Vpass voltage on the
19 unselected word lines. Vpass voltage being highlighted in green.

20 And then, this Vpass voltage corresponds to the first bias voltage
21 of the '957 Patent. And then, a Vread voltage is applied during that
22 verifying operation. And this Vread voltage corresponds to the second bias
23 voltage at the '957 Patent. In essence, Suzuki shows Vread is less than
24 Vpass, and therefore satisfying the '957 claim requirement that the second
25 bias voltage is smaller than the first.

1 JUDGE KOKOSKI: Counsel.

2 MR. HSU: Yes.

3 JUDGE KOKOSKI: Excuse me. This is Judge Kokoski. Staying
4 on that slide 57. Now, doesn't Suzuki describe the different periods of the
5 recovery operation so that T3 to T4 is the end of the program operation? So,
6 how do we know where the pre-verify stage starts within T3?

7 MR. HSU: Yes, Your Honor --

8 JUDGE KOKOSKI: (CROSSTALK), yes.

9 MR. HSU: I'm glad you bring it up, Your Honor. So, what Suzuki
10 says -- in fact, let me turn to -- it's here on slide 59, paragraph 131. And in
11 highlight there, the recovery operation is an operation in which an end
12 operation of the program operation and the ready operation of the verifying
13 operation are combined. So, Suzuki is characterizing the entire recovery
14 operation. It doesn't divide up, for example, T3 to T4 as the end of operation
15 of the program operation as the Patent Owner will have you believe.
16 Instead, it characterizes the entire recovery operation.

17 But what happens is, in fact, the -- let me go to slide -- sorry,
18 actually, I'll stay on this slide. What happens is, the program operation
19 actually ends shortly after T3, because the program operation ends when the
20 voltage on the selected word line falls below VPGM. And Suzuki actually
21 discloses that in paragraph 137 of Suzuki, which is cited by the petition, but
22 not on this slide. In paragraph 137 Suzuki states, and I quote, "The program
23 operation increased the amount of the threshold voltage of the program
24 target memory cell, MT, is based on the voltage value of VPGM, and the
25 time during which VPGM is applied to the word line, WLsel," end quote.

1 Now, this quote shows that VPGM controls the program operation. And
2 therefore, when the voltage on the selected word line falls below VPGM,
3 programming ends, and that's undisputed.

4 And so, again, it is not correct to say, T3, T4 is the end operation
5 -- program operation because Suzuki doesn't say that. In fact, Suzuki says
6 the opposite through its characterization of the program operation.

7 Now, I will go through the other aspect of it, which Your Honors
8 have noted in your institution decision, which is the role of this Vpass
9 voltage.

10 Now, moving on to slide 60.

11 JUDGE CYGAN: Counsellor, before you move on, I just have
12 one question.

13 MR. HSU: Sure.

14 JUDGE CYGAN: It is important that the program operation ends
15 before the pre-verify stage begins?

16 MR. HSU: Well, so, in the case that a pre-verify stage is present,
17 we will understand, yes, there's a delineation when the programming ends
18 and then a pre-verify begins. Now, Patent Owner did not seek to construe
19 the term pre-verify. But we would understand that under its plain meaning,
20 pre-verify -- so, it comes before verify, and presumably what it does in that
21 period, has something to do with the verifying operation. And this, in fact,
22 is what we will be showing you next, which is: the Vpass voltage; that is,
23 prepare the channel -- the memory device for more accurate sensing, and
24 Vpass voltage is integral to that operation.

25 JUDGE CYGAN: Is there anything functionally about the pre-

1 verify stage that we should be concerned with?

2 MR. HSU: Could you elaborate on what you mean by
3 functionally?

4 JUDGE CYGAN: Well, I'm just trying to understand your
5 argument --

6 MR. HSU: Mm-hmm.

7 JUDGE CYGAN: -- and how you're distinguishing Suzuki's
8 Figure 11. Judge Kokoski had asked, is it part of the program operation?
9 You replied, no, it's not part of the program operation, you can see that from
10 the graph.

11 MR. HSU: Mm-hmm.

12 JUDGE CYGAN: The program voltage ends before the pre-
13 verifying starts.

14 MR. HSU: Mm-hmm.

15 JUDGE CYGAN: So, I'm just trying to understand if there is an
16 importance, the program operation ends before the pre-verifying starts. And
17 you had mentioned some functional properties about how it prepares it for
18 the verifying stage.

19 MR. HSU: Mm-hmm.

20 JUDGE CYGAN: Is that important for us to look at when we're
21 understanding how to read the art in the claims?

22 MR. HSU: I would say that, yes, pre-verify should be completed
23 with programming, right? Again -- and I want to be precise, we're not
24 saying, there's nothing related through programming within T3 to T4. We're
25 saying, programming ends right when the voltage on the selected word line

1 falls below VPGM, and that happens -- that does happen within T3 to T4,
2 but it happens very shortly after T3. And beyond that point, programming is
3 finished, it's done. And now you're looking at an operation to prepare the
4 channel for a more accurate verifying operation. And that whole process is
5 pre-verifying, or it corresponds to the pre-verifying of the '957 Patent. Now
6 --

7 JUDGE CYGAN: And you're almost into your rebuttal.

8 MR. HSU: Yes.

9 JUDGE CYGAN: You just started it.

10 MR. HSU: I will brief. So, as shown in slide 60 here, basically, a
11 Vpass is applied during both T1 and T2, and T3 and T4, and that Vpass is an
12 intermediate voltage to basically prepare the device for the voltage that's
13 coming up in the next period. And it's telling that Suzuki includes the Vpass
14 voltage in T3, T4 period of where it labels it as recovery operation. If, as
15 Patent Owner would have you believe, that this entire period of T3 to T4 is
16 the end of the programming operation, then it would have made more sense
17 for Suzuki to include T3, T4 under the program operation umbrella instead
18 of here, clearly labeled under the recovery operation. And with that, I'll
19 pause, unless there's more questions.

20 JUDGE KOKOSKI: Counsel, this is Judge Kokoski again. I do
21 have one more question. So, what are we supposed to think about the
22 VCGM voltage that's lower than both Vpass and Vread? How does that
23 factor into this period?

24 MR. HSU: Sure. So, VCGM is the voltage that actually performs
25 the removal of the electrons out of the channel as we previously discussed,

1 and that is the core operation that ensures -- that removes the electrons and
2 results in a more accurate verifying operation. But as Dr. Liu explains in his
3 reply declaration in paragraph 82, Vpass conditions the channel whereas a
4 disturb-free, what I'll call channel flush; meaning, removing the electrons
5 out of the channel, and that Vpass is integral to the recovery operation, so
6 the two cannot be separate. Now, if you're talking about -- so, the two
7 -- both functions two together improve the verify accuracy, and so, in that
8 sense, Vpass is also a bias voltage.

9 Now, the petition, on page 18, I believe, explained that a bias
10 voltage -- when the claim says apply a voltage between a certain stage, it
11 does not require the voltage to be applied during the entire stage. That's
12 been rebutted. And so, Vpass, in that sense, constitute a first bias voltage.

13 And with that, I'll (CROSSTALK) --

14 JUDGE KOKOSKI: Okay, thank you.

15 MR. HSU: Thank you.

16 JUDGE CYGAN: Petitioner, I have you at 17 minutes left for
17 your rebuttal time. How much time would you like to reserve for your sur-
18 rebuttal?

19 MR. RADSCH: Thank you, Your Honor. Can we please reserve
20 15 minutes?

21 JUDGE CYGAN: You may begin.

22 MR. RADSCH: Thank you, Your Honors, and good afternoon.

23 May it please the Board. As I mentioned earlier, I will be addressing
24 Ground 1, and my colleague, Mr. Bonny, will be addressing Grounds 2 and
25 3. I'd like to start with respect to Ground 1, the issue about the first and

1 second bias voltage limitations.

2 So, I'm turning now to Patent Owner's demonstrative slide number
3 19. And I guess just to set the table here, I think the issue here is actually
4 very simple straightforward about what the problem with their mapping is in
5 their ground. I think it's been complicated by the briefing, unnecessarily so.
6 So, I'm going to try to unpack it, set the stage, and then dive in and explain
7 what the issue is.

8 So, starting here on slide 19 with the claim language, what the
9 claim requires is the application of a first bias voltage on a gate terminal
10 with at least one memory cell of the first memory cell string, then the
11 application of the second bias voltage to that same gate terminal of the
12 memory cell, where that second bias voltage is smaller than the first bias
13 voltage. So, that's what the claim requires.

14 Now, what is the ground that Petitioner has proposed here? I'm
15 turning now to the petition -- this is at petition page number 39. So, their
16 position is that, Hongtao discloses this limitation. There's no obviousness
17 argument for this limitation, it's simply that Hongtao discloses it. What is
18 the evidence on which they rely for Hongtao disclosing this limitation?
19 They rely entirely on the waveform of Hongtao's Figure 2, shown here again
20 on petition's page 39, circled in red, the unselected word lines, and shown
21 (INDISCERNIBLE) to this minor change in that waveform of Hongtao's
22 Figure 2.

23 Turning back to the slides, I'm on Patent Owner's slide 20. Again,
24 this is the entirety of their argument. It's what is shown in the waveform of
25 Hongtao's Figure 2. The problem with their argument is that Figure 2

1 represents the target waveforms, they're administered to the word-line
2 layers. It does not show the actual bias voltages that are applied, at any
3 given time, to a particular gate terminal on a particular selected memory
4 string.

5 Now, there's no dispute that the waveforms depicted in Figure 2
6 are target waveforms, they are not the actual resulting waveforms. And the
7 evidence on that, as I said, it's undisputed and it's ample. So, to start with, as
8 Dr. Przybylski, Patent Owner's expert, explains -- this is in his declaration,
9 Exhibit 2003 at paragraph 96, the waveforms, illustrated in Figure 2, depict
10 steep slew rates -- those are the change rates of voltage through time,
11 straight lines and sudden changes, which signify target voltages, all of which
12 indicate that Hongtao is illustrating target voltages rather than the resulting
13 voltages that develop over time on the gate terminals of the memory cells.
14 So, that's his testimony.

15 And I'll just pause. What Petitioner's argument has focused on,
16 both in the briefing and today, is whether a curved or straight line represents
17 a voltage applied at a gate versus on a word line. But that, I would submit to
18 you, is not the central issue. The issue is, is Figure 2 the actual voltages
19 applied at the gate terminal or is it the target voltages applied to the word
20 line with a target -- what the goal is? And there's no dispute that these
21 waveforms are target waveforms.

22 Their own expert, Dr. Liu, in his reply declaration, Exhibit 1027,
23 paragraph 19, acknowledges that these are target levels -- that the
24 waveforms represent targets. Dr. Liu, their same expert again, was deposed
25 in another related proceeding, this is in Exhibit 2007, he testified that there

1 will always be ramping time in the voltage application. Hence, those curves
2 in an actual voltage application will always be curved. So again, we know
3 that this figure represents target values. And Dr. Liu, their expert, agrees
4 there will always be RC delay in the application of voltage to the gate
5 terminal.

6 Now, he disagrees about the major source of that delay, and I'll get
7 into that, but that's not relevant to this particular issue, which is, he agrees,
8 there's always RC delay, which results in there being different waveforms
9 that is curved and non-straight wave forms to represent the actual application
10 of voltage.

11 So, what it boils down to is that their entire case is built around this
12 figure, but this figure does not represent the actual voltages applied at the
13 gate terminals of particular memory strings. These are the target values that
14 are applied onto the word lines.

15 I'm turning now to slide 21. Now, the '957 Patent itself
16 acknowledges and frankly addresses this very problem. The '957 Patent
17 distinguishes between the voltages that are applied through the word-line
18 layers during a pre-pulse stage, and the bias voltages that result and are
19 applied to the gate terminals that develop and result over time.

20 So, you may have a target voltage of 6.8 volts in the pre-pulse
21 stage, but your applied voltage is only less than that, and that's because you
22 do not apply that voltage for a sufficient amount of time. There's not enough
23 time for it to develop. That's what the '957 Patent says, for example, at
24 column (sic) 1148, column 12, line 9. It says, compared to the verify/read
25 operations in Figure 5, which is depicted here on slide 21, the bias voltage is

1 applied in the pre-pulse stage can be fully developed to completely reach
2 target values in Figure 7. And so, that's one of the very purposes of the '957,
3 is to provide a sufficiently long pre-pulse period to allow the actual voltages
4 to reach their target values. The problem with Hongtao is it's silent on how
5 long its pre-conduction phase is.

6 I'm turning back now to slide 20. There's no discussion about how
7 long that pre-conduction phase is at all. And it doesn't discuss anywhere in
8 the text relative voltages during the read cycle versus the pre-conduction
9 cycle. So, they staked their case entirely on what is shown in the figure, not
10 as what is described in the accompanying text, because it's silent on that
11 issue. It's not concerned about those relative values of the unselected word
12 lines.

13 Now, I'm turning now on to slide 24. As Dr. Przybylski, Patent
14 Owner's expert explained, the actual waveform that would result from this
15 target value, represented in the Hongtao reference, would look something
16 like what's annotated in red on slide 24. Now, Petitioner has criticized this
17 annotation and said, well, it's just made-up.

18 And I turn now to slide 26, focusing on the bottom bullet. What
19 they've argued in the reply is, well, that annotation, it may actually
20 overshoot or undershoot the target depending on a myriad of different
21 factors.

22 So, we go back to that, and that really is the heart of the problem.
23 They have presented no evidence, anywhere in their petition, about what the
24 actual waveform would look like. And they acknowledged that this
25 representation with the actual waveform looks like it may overshoot the

1 target, may undershoot the target. We just don't know, they say. But it's
2 their burden to have put forth that case in their petition. But they stake the
3 entirety of their case on these waveforms that represent the targets, not what
4 it actually develops on the gate terminal of the identified claimed memory
5 string.

6 Now, the Federal Circuit has told us, right, it is legal error to rely
7 solely on a figure unless the features are clearly disclosed by their drawing.
8 That's what the Court said in the case here on slide 23.

9 Now, the problem here is, it's probably even more drastic than
10 developed in these cases is that, again, they're relying upon a figure that
11 represents an idealized target value as evidence of what the actual value is,
12 without performing any analysis of what that actual resulting waveform
13 would look like, and it is the waveform, over time, that's critical to the claim.

14 JUDGE CYGAN: Counsel, can I ask you a question?

15 MR. RADSCH: Yes.

16 JUDGE CYGAN: Let's take a look at slide 20.

17 MR. RADSCH: I'm there, Your Honor.

18 JUDGE CYGAN: In the read operation on this slide, what is being
19 read?

20 MR. RADSCH: In the -- what is circled in red?

21 JUDGE CYGAN: No, I'm sorry. It's "what voltage is being
22 read?" Is it reading the memory cell voltage?

23 MR. RADSCH: So, for the selected word line below what's
24 circled in red, that is what is being read, the value of that selected word line.
25 And what it's showing here is the application of some voltage -- induction

1 voltage, simply to open up the cell on the unselected word lines. So, what's
2 being read is the selected word line.

3 Now, the Petitioner has argued that Hongtao, in its -- I'm now on
4 Patent Owner's slide 27, that Hongtao, in its paragraph 26, references the
5 desirability of reducing the conduction voltage. And although that may be
6 true as a general matter, Hongtao says nothing about reducing the
7 conduction voltage in time period two versus time period one. And that's
8 what the claim is all about, is a relative amount of voltage being applied at
9 the gate terminal of a particular string at time one versus time two. Hongtao
10 is silent about that issue. Now, they've claimed that Hongtao is addressing
11 the same hot carrier injection issue as the '957 Patent. That's simply
12 incorrect.

13 I'm turning now to Petitioner's slide 31. It's true, both references
14 mention hot carrier injection, but the problems are completely different, as
15 are the solutions. As you can see from the top box, which is referring to the
16 '957 Patent, in column 12, the issue here, is it states by introducing a lower
17 bias voltage in the verify/read stage, as opposed to the earlier pre-verify
18 stage, the gradient of the channel potential of the selected memory cells can
19 be reduced. Accordingly, HCI cannot be generated from the selected
20 memory cell to the upper adjacent memory cell of the selected memory cell
21 in the selected memory cell string. It's a mouthful of words, but they're
22 dealing with HCI issues within a given memory cell string in the area above
23 where the selected memory cell is. In contrast, Hongtao is dealing, as it says
24 here on the bottom, with a problem of potential crosstalk between different
25 memory cell strings.

1 So, these are -- they both may be concerned with it's a hot carrier
2 injection issue, but in completely different manners. The '957 is dealing it
3 within a given cell string, and then, Hongtao is dealing with it and concerned
4 with it across different memory cell strings, so that does not help them
5 either.

6 Let me turn back to -- so, many slides, where they address this
7 issue of whether memory -- or a gate terminal is the same as a word line. It's
8 frankly irrelevant to deciding this issue, because again, the figure they rely
9 upon is simply a target value. But there is no dispute that a word line, which
10 are the lines that are these horizontal lines through the stack, right? That
11 those are a different structure than a gate terminal of a memory cell on a
12 particular memory string, which is what the claim requires where we look at
13 the given voltage.

14 JUDGE CYGAN: Counsel, I guess that's still my question on
15 Hongtao's Figure 2, which you have in your previous slide. In the sense that
16 it's reading, it's reading the memory cell, right? The purpose of the
17 operation is to read that memory cell, correct? It's not just reading the word
18 line, in general, it's reading a particular memory cell which has a gate on it.
19 So, to the extent that it needs time to develop on it, the point of the read
20 operation is to reach these levels so it can read the cell, and so that the other
21 word lines are developed separately so they can read it properly. Why isn't
22 it proper to read that figure as developing those on the cell, as opposed to
23 just some part of the memory of the word line that is not being read?

24 MR. RADSCH: I think there's a couple of responses, Your Honor.
25 Firstly, the only memory cell being read in this figure is on the selected word

1 line. The voltage is being applied to the unselected word lines to open them
2 up -- to be opened up, to facilitate the reading process on the selected word
3 line.

4 But even if one were to interpret this as reading those unselected
5 word lines, it still says nothing. No one cannot determine anything from this
6 figure about target values to what the resulting actual voltage waveform
7 looks like, because we know this is not an actual waveform. And again, I go
8 back, this is exactly, as you said on slide 21, the problem that the '957 Patent
9 is addressing in the context of Figure 5, it shows that. It takes time for the
10 voltage develop. If you do not have a sufficiently long pre-pulse period, you
11 will not reach your target value.

12 And so, going back to slide 20 in Figure 3 of Hongtao, again it's
13 silent about the length of that pre-conduction period and whether that period
14 is of sufficient duration to reach those idealized target values. So, you can't
15 simply extrapolate from target value to real value. And we know that
16 because of the existence of RC delay. There's no dispute that RC delay is a
17 real thing. Their expert simply claims that it's not too big of a problem. Just
18 let me address that. I'm on slide 26.

19 JUDGE CYGAN: Before we go there, isn't there some time
20 concept, if we're taking a look at Figure 2, if we take a look at the read
21 voltage -- the read operation on the selected word line, there's certainly
22 going to be some delay in the circuit for these voltages to reach their targets.
23 But at some point if you had too short of a delay, you wouldn't be doing any
24 read operation at all. So, doesn't the target tell you something about what
25 has to be done in practice?

1 MR. RADSCH: It does not, because this is precisely, if I turn to
2 slide 21, what the patent talks about, right? So, if you turn to, actually,
3 column 12 of the '957 Patent, lines 18 to 21, where it's discussing this figure,
4 it says, for example, as shown in Figure 5, again, I'm on slide 21, the bias
5 voltages are less than a target value such as 6.8 volts. The bias voltages can
6 still be developed to the target value such as 6.8 volts in the verified read
7 stage. So, they may be eventually developed to the target, but here it's not
8 happening until the read stage. So, we know what matters, the waveform
9 over time, because that's really what the claim is directed to. Because it has
10 to have a lower voltage in Time 2 relative to the voltage in Time 1.

11 If we go back to slide 20, in the figure, nothing in Hongtao says
12 that there's any importance, or any desirability of reaching a pre-conduction
13 voltage for those unselected word lines that's higher than the conduction
14 voltage during the read period. There's no -- that's not addressed anywhere
15 in Hongtao. There's no statement that that's a benefit, that's a purpose,
16 there's some reason to do that. Again, they're relying solely on this minor
17 change in slope in this idealized waveform as the totality of their evidence.

18 JUDGE CYGAN: So, I understand that you're focusing on that
19 specific delay in the unselected word lines, which is really, I think, the main
20 issue. You're not really contesting that -- and I don't think your expert is
21 contesting either, that the other voltages that are being obtained are going to
22 be -- they're going to approach the target voltage, which is listed on there.
23 So, it's not that Figure 2 is unrelated to the outcomes that are required on the
24 specific cells?

25 MR. RADSCH: I don't think that there's any evidence at all that

1 they reached their target values. And so, there's no particular values
2 identified in Hongtao, this is just a waveform. What those values are, they're
3 just -- exemplary values are stated in the '957 Patent, but they're not stated
4 here. Again, whether the actual waveforms reach their target, and whether
5 they reach it in the time period required for the claim is the critical issue.
6 Because, remember, for the claim mapping to work, the value in a -- the
7 target value of the pre-conduction stage would have to be reached during
8 that stage for the claim limitation to be met.

9 JUDGE CYGAN: But just going more generally to that figure. If
10 we were to look at Figure 2, I think, taking your expert's testimony to an
11 extreme, let's say, and we were to say, well, looking at Figure 2, the bit lines
12 at the top of Figure 2 may never reach their driving voltage, and the top
13 select transistor of the selected string may never reach its conductive
14 voltage. At some point, we have to say, well, Hongtao really wouldn't work
15 if these voltages weren't reached, right?

16 MR. RADSCH: I don't think that's his testimony, and I don't think
17 that's taking his testimony to the extreme. I don't think that's an accurate
18 characterization. And I turn to slide 24 to address that, right? What he's
19 showing here, right, in slide 24, is what the likely actual voltage line looks
20 like. And the reason, as he's explained -- Dr. Przybylski's explained, the
21 reason why there's that steep ramp in the pre-conduction phase of Hongtao,
22 is to more quickly reach that target value during the read stage so you can
23 minimize the time needed for that pre-conduction phase.

24 The '957 is directed to a different issue. The reason it has a higher
25 voltage in the pre-verified stage, and then lowers it for the verified stage, is

1 to address that hot carrier injection issue within a given memory cell string.
2 That's not an issue that Hongtao addresses or acknowledges.

3 JUDGE CYGAN: So, just to go back to your expert's testimony,
4 your expert's testimony is really supporting the point that Hongtao isn't
5 specific on it, and the petition isn't specific on it, in the absence of that
6 specificity it's possible that they may not develop fully; is that correct?

7 MR. RADSCH: I would simplify it as follows. In testimony, it's
8 un rebutted that the waveform of Hongtao is not an actual waveform, it
9 represents a target value. And what actually results, the waveform will look
10 different. And he's now annotated in the figure with how he understands
11 that waveform to look. The problem is, it is Petitioner's burden to prove that
12 the actual waveform would meet the requirements of claim 1, and it has to
13 do that in the time period set forth in claim 1. That is, it must reach the
14 higher level during time period 1 before receding to a lower period in time
15 period 2. And they don't have that analysis anywhere. All they do is rely
16 upon what is conceivably a target value. And we know the target values are
17 often not reached, what matters is here the time when it is reached.

18 And I think, again -- I think, come back to the notion to -- the fact
19 is, there's no dispute that there's RC delay in these devices. Their own
20 expert admits it. Now, he, again, he argues about the significant cause of
21 that RC delay. But I'll just point out, that the only textbook -- in Exhibit
22 1014, here on the screen, the only textbook that Petitioner relies upon is
23 Exhibit 1014, NAND flash memory technologies, part 2 of that exhibit
24 -- this is at page 350. There's an entire section of that textbook devoted to
25 word line RC delay. So, far from a negligible concern, there's an entire

1 section devoted to it. And it says that in stacked word line structure in 3D
2 NAND cells, a word line capacitance is greatly increased from 2D cells.

3 So, far from an insignificant concern, this is a significant concern.
4 Petitioner's argument seems to be, well, device physics are complicated so
5 we should ignore device physics in interpreting Hongtao's Figure 2, but that
6 obviously cannot be done. Just because device physics are complicated, you
7 can't just ignore those physics interpreting Hongtao's Figure 2. And the
8 problem is, again, that they stake their entire case on a target waveform, not
9 an actual waveform. That is the heart of the issue that they haven't
10 addressed anywhere in their proof, let alone in their arguments.

11 And I'll just -- on this point, let me just turn to slide -- this is Patent
12 Owner's slide 26, where their expert -- and they have argued that word-line
13 layers have negligible resistances. If you look at their expert's declaration
14 on this, Dr. Liu's declaration, it's Exhibit 1027 at page 41, there's absolutely
15 no citation for that statement, and it's contradicted by the textbook we just
16 saw, that they rely upon, that has an entire section devoted to the word line
17 RC delay.

18 So, unless there are further questions on that issue, I'd like to turn
19 to the next issue with respect to claim 1 and Ground 1. So, I'm turning now
20 to Patent Owner's slide 10, and this is the limitation requiring there be a pre-
21 verify stage in the claims.

22 Now, turning to Patent Owner's slide 11, there's a lot of talk, I
23 think today, about similarities between a read operation and a verify
24 operation, and there's no dispute albeit any -- we're not concerned with that
25 there are similarities. But they're not the same, they're not synonymous.

1 Their own evidence shows that they're not the same thing, they're not
2 synonymous. In their own prior art they cite, right, it treats it differently. It
3 talks about similarities, but it treats them differently, so we know that they're
4 different things, right? And it's clear that Hongtao does not disclose a pre-
5 verify, let alone a verify stage that is directed to a reading process. These
6 things are not just synonymous. But let me focus what the issue is with their
7 combination. These are distinct operations, verifying and reading.

8 And one of the key differences, and I say, they never ever address
9 or focus on the differences, they focus only on the similarities, but their
10 proposed combination motivation ignores the differences, and I'd say, that's
11 error. One of the differences is, is that verification is an iterative check
12 within a programming cycle that follows each programming step while
13 reading operations check the stored state of the cell.

14 Well, what do they want to do? They want to take the two-stage
15 process from the reading operation of Hongtao and add it to the verification
16 process of Yu. And so, you're adding, for every verification process now of
17 Yu, every verification operation, you're now adding an additional stage.
18 They don't, anywhere, address those shortcomings, that is the added delay
19 that might pause the program. And the reasons one would not choose to do
20 that, because you're now adding an entirely new stage to every single
21 verification operation.

22 They talk a lot about -- in their remarks about the general
23 motivation to apply reading teachings to a verification process. That is not
24 the right analysis. The analysis is, would a person of ordinary skill in the art
25 be motivated to apply the teachings that they rely upon from Hongtao to the

1 Yu reference?

2 I think it's important to go to what their argument is with respect to
3 the motivation to combine. So, I'm turning to the petition at page 72, and
4 what they argue is that, a POSITA would have been motivated to employ
5 Hongtao's read operations in a program verification loop in view of Yu.

6 Now, first of all, again as mentioned, they don't account for the
7 differences; that is, there's a single-stage verification, and they're proposing
8 adding a whole other stage, and they don't address the resulting delays that
9 would result from that.

10 Second, nowhere in their motivation to combine section do they
11 address the motivation to apply Hongtao's specific waveforms that they rely
12 upon to Yu. They just say, it would be obvious to apply read operations,
13 generally, to Yu's verification process. But they are relying on the specific
14 waveforms, all of them, as it says here, from Hongtao to apply to Yu.
15 Nowhere did they explain why a POSITA would have been motivated to
16 apply those particular waveforms to Yu.

17 Lastly, they have different biasing schemes. This is critical, and
18 they try to ignore this by saying they're not claimed. The point is, the
19 biasing scheme in Hongtao is different than the biasing scheme in Yu, and
20 this is a very important difference. Yu explains that it applies different
21 voltages to the memory cells, below the cell being read -- let me turn to
22 Patent Owner's slide on this.

23 So, we're now on slide 13. What you described is a different
24 voltage for unprogrammed memory and for programmed memory as
25 explained in Yu's Figure 7, but there are these two sub blocks. There's a sub

1 block of memory cells within a given string, sub block 1, that's below, where
2 it includes the cell that's being read, and a second block above, because the
3 blocks above hit a lower voltage than the box below. So, within a given
4 string, the unprogrammed memory has a different voltage applied during
5 verification than those that are below the selected memory cell. That is
6 entirely different from Hongtao.

7 Hongtao applies the same conductive voltage to all unselected
8 word lines. And we saw that from Figure 2, right, Figure 2 of Hongtao, I'm
9 going back to slide 20, right? All unselected word lines we see in the exact
10 same conductive voltage. There's two entirely different biasing schemes
11 here. Hongtao applies the same conduction voltage to all of the unselected
12 word lines, whereas, again, as addressed on slide number 13, Yu has
13 different voltages applied based upon whether they are programmed or
14 unprogrammed. But what their combination would do is, take all of the
15 teachings, with respect to the waveforms, from Hongtao and apply those to
16 Yu. And they never explain why one would dispense with this beneficial
17 biasing scheme that Yu uses in combining these references.

18 This has nothing to do with whether those differences are claimed
19 in the '957 Patent, this has to do with the art they're looking to combine
20 operates differently in meaningful ways and they never address it. In fact,
21 they don't say, you keep using biasing scheme or do you apply Hongtao's?
22 We actually don't know. It seems, based upon their combination, you apply
23 all of Hongtao, because that's what their petition says, to Yu. Because you
24 could clearly alter that scheme, nowhere is that addressed. So, we think that
25 the motivation clearly is not there to apply the particular teachings of

1 Hongtao to Yu.

2 Let me now turn to the last issue with respect to Ground 1, which
3 is the dependent claims 5 and 6. These require a bottom bias voltage and a
4 top bias voltage, and that these be applied to gate terminals of the BSG and
5 TSG in the pre-verify and the verify stage. I'm on slide 37 now, which has a
6 (INDISCERNIBLE).

7 Patent Owner's slide 38, the plain meaning of this requires the
8 same voltage be applied during the pre-verify and verify stage. This has
9 always been our position. I think the word level helps to understand that
10 we're talking about a particular value. And what the value is, is not
11 important, but that value must be maintained between the pre-pulse period
12 and the verifying period. That's precisely what's described in the '957
13 Patent, as showing here on 38, describes that the voltage can be applied,
14 such that it reaches high volts in the pre-pulse period and this can be
15 supplied sufficiently long that that target value is actually reached.

16 And then, '957 goes on to say, in that second box on slide 38, when
17 the verify/read operation proceeds to the verify/read stage, the bias voltage
18 remains. All right. So, we're talking about obtaining the target voltage
19 through a long enough pre-pulse period and then maintaining that voltage
20 into the verify stage. That's precisely what claims 5 and 6 are about. What
21 they would have the Board do is basically weed out the limitation altogether.
22 They say that it could be any changing number of voltages. It can go to
23 anything.

24 And as they say on the petition, page 107, quote, "In the context of
25 the '957 Patent, even applying zero volts is applying a voltage." All right, so

1 under their theory of this changing voltage that could be applied to meet the
2 claim language, it could be zero volts, followed by some volts, back to no
3 volts again, and that would somehow meet the claim language. It
4 completely reads out and gives no meaning whatsoever to this claim
5 limitation.

6 Now, it's clear that “a”, it can mean more than one, and I think that
7 they've now abandoned this argument that there can be multiple different
8 voltages, but maybe not, but the Federal Circuit has been clear that even
9 though “a” means more than one in the context of these types of claims,
10 there must still be at least one voltage that is applied in both stages. And
11 that's what the prior art doesn't have.

12 And I think, Your Honor, Judge Cygan, your question is, how does
13 claim 1 relate to this construction of claim 1? Well, when you're talking
14 about different voltages it applied, it says that expressly, a higher versus
15 lower voltage. Here, it just recites a voltage, and we don't have that. The
16 distinction that you have in claim 1, in the claim language of claims 5 and 6,
17 it is a voltage applied in the pre-verify and the verify stage.

18 So, slide 40 notes that the claims do not recite, for example, a first
19 bias voltage applied in the pre-verify stage, a second bias voltage applied in
20 the verify stage. Now, I want to be clear, because Petitioner's counsel has
21 sort of threatened to get up on rebuttal and introduce a brand-new
22 obviousness theory never before disclosed. But our position, the way it's
23 always been, that while the same voltage level has to be applied in both the
24 pre-verify and verify stage, it need not be maintained for the entirety of that
25 stage as illustrated in these figures. That's always been our position, and

1 that's in our briefing, expressly. So, I'm curious to hear their new
2 obviousness theory never therefore disclosed, and I'm happy to address that
3 on sur-rebuttal.

4 Again, slide 41, there's ample description in the specification of
5 maintaining the voltage between the verify and pre-verify stages, and that's
6 directly what this is getting at. (INDISCERNIBLE) to address this issue
7 with respect to Figure 7. Figure 7 is not a figure Patent Owner relied upon
8 as its claim construction embodiment. As Petitioner argued, we simply
9 responded that, in this case, what's shown for the TSG layer and the BSG
10 layer, that's what would satisfy this claim language. But as to the unselected
11 word lines below N-1 they point to, that would not meet the claim language,
12 and we never said it would.

13 So, turning now to slide 44, this is Ground 1. What they rely upon
14 are different voltage levels. Here is their annotation from their briefing.
15 And what they argue -- well, first of all, again, Hongtao illustrates target
16 voltages, so we don't know what voltages they actually apply to the gate
17 terminals. We don't have that resulting waveform. They have not explained
18 what the resulting waveform is. But even if we were to assume that
19 somehow that figure illustrates the actual waveform, and there's no dispute it
20 doesn't, what they rely upon are two different voltages applied during the
21 pre-conduction period and the read period in Hongtao. So, that cannot
22 plausibly meet the claims as properly construed.

23 Unless there are further questions, I will turn the remaining time to
24 Mr. Bonny to address the remaining grounds.

25 MR. BONNY: Thank you, Your Honor, Christopher Bonny for

1 Patent Owner. And since we're short on time, I'll do my best to just hit the
2 key points here. I'll be addressing Grounds 2 and 3. So, I'll start with
3 Ground 2, which was the Suzuki anticipation ground, there's no obviousness
4 issues to consider there.

5 And to begin with, I'll start with, on slide 29, the issue of Suzuki's
6 failure to disclose first and second bias voltages, wherein the second bias
7 voltage is smaller than the first. I think you already know from Petitioner's
8 presentation what the dispute is here, and so I'll focus observing, and just on
9 why it is the case that the time period from T3 to T4 is part of the
10 programming operation and is not part of the pre-verify -- alleged pre-verify
11 period.

12 The main issue here is that the disclosure in Suzuki, paragraph
13 131, states that the recovery operation is an operation in which an end
14 operation of the program operation, and the ready operation of the verify
15 operation are combined. And so, Dr. Przybylski has explained in detail, in
16 paragraphs 125 through 132 of his declaration, how that indicates that the
17 voltages are being applied in two distinct time periods and how the time
18 period from T3 to T4 is what corresponds to what's described there as the
19 end operation of the program operation.

20 Looking back at the figure in Suzuki on slide 29, you can see in
21 that figure that the Vpass voltage on one of the lines continues into that
22 period, and then for the selected word line, you can see that the voltage
23 returns to the same Vpass voltage that was on the selected word line at the
24 beginning of the program operation.

25 Counsel for Petitioner argues that the VPGM voltage is what

1 controls whether you're in a program operation. But you can see from the
2 figure that that's simply not the case. Vpass exists on the selected word line.
3 During the program operation, it raises up to VPGM and then it returns to
4 that Vpass voltage. And then it -- there's a separate voltage, after that, that
5 VPGM voltage, that is used to prepare the selected word line for the verify
6 operation.

7 And I won't read all of Dr. Przybylski's testimony because of time
8 here, but I strongly invite the Board to read through the paragraphs 125
9 through 132, where he further elaborates on how the teachings of Suzuki
10 indicate that that period from T2 to T3 -- T3 to T4, rather, is part of the
11 program operation.

12 The second issue for Ground 3 is on slide -- is at the end here,
13 actually, on slide 45. And this issue relates to the same claim construction
14 argument that Mr. Radsch already went over, and so I won't repeat what he
15 already covered. But the point I'll just make here is that, with respect to
16 claims 5 and 6, there's no dispute that under the proper construction of this
17 term that Mr. Radsch covered, the Suzuki reference fails to disclose these
18 claims.

19 And with the remaining time, I'd like to briefly address the final
20 ground, which is Ground 3. Starting with --

21 JUDGE CYGAN: Counselor?

22 MR. BONNY: Go ahead.

23 JUDGE CYGAN: Do you agree with your counterpart that the
24 pre-verify stage has to be after the program voltage stage?

25 MR. BONNY: That the -- I'm sorry, could you repeat the question

1 one more time?

2 JUDGE CYGAN: Your counterpart on the other side seemed to
3 agree that the pre-verify operation had to occur before the verify operation,
4 but after the program operation. Is that sort of, like, a requirement in your
5 view?

6 MR. BONNY: I don't know if we've taken an expressed position
7 on that, but even assuming that what Petitioner says is true, that actually, I
8 believe, further supports our position with regards to the Suzuki reference
9 going back to the prior issue. Because if there is this defined cutoff between
10 the periods, then you need to look at what is actually going on in those
11 periods. And as their counsel acknowledged, it's the VCGM voltage, that's
12 what -- I think in their words what they said was, removing the electrons,
13 and it's the core operation of the pre-verify stage. And so, if you're looking
14 at what is going on in those stages, and looking for that defined cutoff, that's
15 where it would be. It would be between the Vpass voltage and the VCGM
16 voltage.

17 JUDGE CYGAN: But do you agree that it has to have some
18 specific functioning to it, the pre-verify stage?

19 MR. BONNY: Yes. Yes, Your Honor. That stage is preparing the
20 selected word line for the verify stage.

21 JUDGE CYGAN: And that, sort of, functional characteristic helps
22 to define when it begins and ends, I guess? So, it can't begin at a time when
23 it's not performing that function?

24 MR. BONNY: That's correct, Your Honor, yes.

25 JUDGE CYGAN: Thank you.

1 MR. BONNY: The final ground, Ground 3, addressing that just
2 briefly. First, similar to the Ground 1 with Hongtao, Costa in view of Seo
3 fails to render obvious the pre-verify stage limitation. The main issue here,
4 neither reference, individually, teaches this, of course, and they're relying on
5 a combination. Seo -- Costa, rather, does not have distinct time periods, and
6 Petitioner does not dispute this. And so, their argument is that Seo discloses
7 a time period, T1 is a pre-verified stage, and that the voltage applied in this
8 period is the claimed first verify voltage. And the main issue here is that
9 Seo is about a read operation rather than a verify operation, and that's the
10 same issue and the same distinction that Mr. Radsch elaborated on earlier.

11 And so, I'll just briefly then turn to the final issue, which is, again,
12 with Ground 3, on slide 32. Costa in view of Seo also fails to render
13 obvious the first and second bias voltages, wherein the second bias voltage is
14 smaller than the first bias voltage. I'll just hit the key issue here, and that is
15 -- the main problem here is, that what Costa purports to teach, which is that a
16 lower-voltage value can be used to turn on unprogrammed memory because
17 of their lower threshold with voltages, that teaching would apply equally to
18 both time periods, both the T1 period and Time 2 period. They're selectively
19 applying that teaching, but they're doing it without any basis to do so. And
20 their main argument is that, Costa, in that first time period -- or rather, Seo,
21 in that first time period has a high Vpass voltage that must be applied on all
22 selected memory cells during the first time period. The issue there is, Costa
23 never says that, and -- or Seo never says that, rather. And you heard
24 Counsel admit that Seo doesn't say that. Counsel explained and
25 acknowledged that there's nothing in the reference about source voltage

1 build-up.

2 And so, this entire argument, and this entire theory that is the basis
3 for maintaining the voltage in that first time period, and ignoring the
4 teaching of Costa for that first time period so that it's selectively applied, that
5 entire concept is not found anywhere in the references, and is based entirely
6 on the conclusory remarks from Dr. Liu. And Patent Owner submits that
7 that is based entirely on nothing more than impermissible hindsight, looking
8 for a way to selectively apply that in a way that's not taught by the
9 references.

10 And if there's no further questions, we'll save the rest of our time
11 for rebuttal.

12 JUDGE CYGAN: Thank you, Counsel. You have 12 minutes left
13 for your rebuttal. Petitioner, you have 17 minutes left. You can begin when
14 you're ready.

15 MR. LANG: All right, thank you, Your Honors. So, Patent
16 Owner would have you ignore what Hongtao says. They're saying there's no
17 dispute that Hongtao is showing target voltages and implying by that, that
18 there's no dispute that these voltages are not on the gates. They're implying,
19 if not saying, that Petitioner agrees that this is not showing the voltages on
20 the gates as claimed. That is just false. Our entire reply says that these are
21 the voltages on the gate. Dr. Liu, in paragraph 19, specifically says the
22 same. They had made some type of argument, in their Patent Owner
23 response, that this is actually referring to the voltages on the edge of the
24 word lines, and it takes this a long time to get to the gate, and we said, that's
25 not the case.

1 And I will remind Your Honors again, Hongtao says, the gates of
2 the unselected memory cells on a selected string are applied with the
3 conduction voltage, and then it shows the conduction voltage. That is the
4 voltage on the gates.

5 How many times does Hongtao say target? According to Patent
6 Owner, you'd think it'd be a lot, right? Hongtao says target zero times, zero
7 times. Hongtao is not talking about some target voltage. Who knows if it
8 ever gets there? Let's just magically draw some type of curve underneath
9 that. Hongtao expressly says, the conduction voltage on the gate. There's no
10 other way to read that, and in fact, one of Your Honors asked a question that
11 is consistent with Dr. Liu's testimony. It does show a ramp-up time. So, if
12 it's showing that ramp-up time, what's this additional ramp-up time they're
13 talking about? It's like, it shows a ramp-up time, and it shows, as Dr. Liu
14 explains, a holding in that state steady for quite a while, and then it goes
15 down.

16 Now, the other thing that Patent Owner made much to do about
17 -- and I -- made much to do about is, that Patent Owner -- or the Petitioners
18 only rely on Figure 2. That is just not true. The Petitioner -- in fact, they
19 have a whole slide, and they recognize Hongtao -- paragraph 26, where
20 Hongtao -- and they recognize that Hongtao says generally, it's good to have
21 a conduction voltage, if you can lower it, to lower it, so. In that same
22 paragraph, after he says that, you see the conduction voltage lowered, then
23 you further see a further improvement that Hongtao addresses.

24 But the idea that somehow our position has been that this isn't
25 showing the voltage is on the gates, our whole reply, makes the opposite

1 argument. Number two, as Dr. Liu explains in paragraph 19 of his reply
2 declaration, this shows -- you can call it a target, that's fine, but it shows the
3 voltage on the gates. It clearly ramps up, it stays there for a significant
4 amount of time, and it goes back down. And as I'll say it again, Hongtao,
5 the gates of the unselected memory cells are applied with the conduction
6 voltage. Okay, so.

7 JUDGE CYGAN: Counselor?

8 MR. LANG: Yeah.

9 JUDGE CYGAN: Can I ask you one question about their
10 argument? When your counterparts were talking about their own patent, and
11 they were describing what happens in Figure 4, Figure 4, kind of like
12 Hongtao, is describing what happens when you apply voltage to the word
13 lines itself. And then, they were bringing in the fact, in the disclosure of the
14 patent, that there's this additional time delay in order for it to reach the gates.
15 There's certainly nothing in the claims that talk about a time delay, but there
16 is the requirement in the claims that the voltages be developed on the gates.

17 When you're looking at the disclosure of Hongtao, and you have
18 the description in Figure 2, and Figure 2 refers to the voltage, which is put
19 on the word lines, and you also have some discussion about that the voltage
20 is applied to the transistors, how are you stringing that together to really
21 show that what they're talking about is not just voltages that are applied to
22 the word lines, but these voltages are really actually explicitly representing
23 what happens on the --

24 MR. LANG: Because Hongtao uses the language interchangeably.
25 Right there, it doesn't say word line, it says, a conduction voltage -- the gates

1 of the unselected memory itself.

2 JUDGE CYGAN: I'm sorry, Counselor, can you pause a second?

3 We have a connection issue.

4 JUDGE KOKOSKI: I'm back, thank you.

5 JUDGE CYGAN: Counsel, could you restart with your answer to
6 that? can you summarize the question and then restart your reply?

7 MR. LANG: I think your question was, there is some disclosures
8 in Hongtao about applying the voltages on word lines, and how do we know
9 that those are developed on the gates? Hongtao uses gates and word lines
10 interchangeably. We see it right here, Hongtao says, the gates of the
11 unselected memory cell, not word lines, the gates are applied with the
12 conduction voltage, okay? That is what the claims say, the gates of the
13 memory cell. Hongtao is expressly saying, he's applying it on the gates.
14 The reply further explains that any delay between the word line and the gate
15 where the memory cell is, is minimal. And you see the delay, Your Honor,
16 there in the signal building up. They show it building up, and then it holds
17 flat for long periods of time. And guess what that is just like, Your Honors?
18 The '957 Patent, if you look at Figures 6 through 7, they too have straight
19 lines.

20 And lastly, we're not just relying on the figure. As we said, Figure
21 25 says it's applied to the gates directly. Figure 26 recognizes this general
22 principle of a conduction voltage being less, which is good. It supports it
23 being less. And, in fact, importantly, from the figure alone, if you look at
24 Figures 2 and 3, some go up, some go down, some stay flat. Clearly, this is
25 a signal that goes down.

1 JUDGE CYGAN: Counsel, just to probe this one more time, just
2 so I really understand your argument and to contrast it with Patent Owner's
3 argument. If we would read this section of Hongtao as stating how the gates
4 are being supplied with voltage as opposed to the magnitude of voltage that
5 they're being supplied with -- this is a quote from paragraph 25, it's talking
6 about the read operation, and not specifically about the pre-verification step
7 that we're looking at. But how do we know from phrases like this that the
8 voltage that's being applied to the gates is actually what's matching what's in
9 the Figure 2?

10 MR. LANG: Because you see a ramp-up time, right? And as Dr.
11 Liu explained, we all agree that there's going to be some type of ramp-up
12 time. But all of the references that we've shown, they show that this idea of
13 a difference between a word line and a gate voltage -- or a gate, is used
14 interchangeable. And it simply shows it develop to the top. It calls it a
15 conduction voltage. It says that's applied to the gate. I just don't see how
16 you could read it and say that it never gets there. Hongtao says no such
17 thing. All these references that we pointed to, it shows the signals develop
18 and then they plateau.

19 This is just like Figures 6 through 9 of the '957 Patent that
20 allegedly are fully developed, they show just the same type of straight-line
21 development and then plateaus. So, it's just like the '957, Figures 6 through
22 9.

23 JUDGE CYGAN: So, your reading of Figure 2 is, that it
24 represents both the voltage being applied to the word lines and then, at the
25 same time, the voltage applying (CROSSTALK) --

1 MR. LANG: Yes. None of these references -- and that's why we
2 cited all those different references it used, word line and gate
3 interchangeably. None of them are drawing this as distinction. The idea is
4 that we're talking about a memory operation. We're showing the voltage at
5 the memory cells because that's what effectuates a memory operation.

6 These graphs would mean very little if we didn't know what
7 voltages were at the memory cell. In the Patent Owner's world, we're
8 looking at graphs, and we don't even know what the voltages at the memory
9 cells are. I mean, it doesn't -- it wouldn't convey what it's intended to
10 convey.

11 I do want to turn briefly to this whole discussion they had with
12 you, and they just misrepresented the petition. Well, I'll read you, Your
13 Honors, what the petition says at page 72. It says a POSITA would have
14 been motivated with a reasonable expectation of success to employ
15 Hongtao's read operations in a program verified loop in view of Yu and the
16 knowledge of a POSITA for several reasons.

17 And so, what is described is, that you're applying it into a program
18 loop. It's not saying, bodily incorporate Yu. This whole notion of -- that
19 you're taking Yu exact programming techniques and adding it to Hongtao's
20 exact read verification, the petition doesn't say that. That would be bodily
21 incorporation. The idea is, that we've been programming flash memories for
22 40 years. The point is, is that you have program verifications. After you
23 program, you verify.

24 So, this whole argument they have about Yu had some type of
25 specific programming thing, that isn't bodily incorporation. The point is, if

1 we think of the Hongtao device, right, it discloses reading. Presumably, that
2 device discloses a programming operation too. If you have a memory, you
3 program it, you read it. The point that the Petitioner is saying is, that it
4 would obvious to simply read after a program. We're not bodily
5 incorporating Yu.

6 Now, on their slide 13, talking about Yu's programming operation
7 again. That assumes bodily incorporation, number one. Number two, it's
8 irrelevant because how you read, it's different than a program. You've got a
9 program operation, if you read after that, you did a read verification.

10 Now, claims 5 through 6, I want to briefly touch on this. I do need
11 to get this slide up (CROSSTALK) --

12 JUDGE CYGAN: I'm going to pause your time while you get the
13 slide up.

14 MR. LANG: Yeah, for some reason I can't get the PDF to open
15 here. Can you do full screen?

16 MR. LANG: Well, somebody smarter than me did that.

17 MR. LANG: All right, Your Honors. Okay, thank you. So,
18 they've changed their argument here on claims 5 through 6. We had quoted
19 them, they talked about this level, and they kept talking about the same
20 voltage level. But what do we have here that they're pointing at? Now
21 they're just saying, apparently, they just have to be at the same voltage at
22 some point in the pre-verify and the read stage.

23 If we look at the voltage that is highlighted there, let's say the
24 conduction voltage in the read phase is 5.0 volt, and let's say it's 5.3 in the
25 pre-conduction phase. Well, it goes from zero up to 5.3, and then it goes

1 down to 5. So, as it goes on its way up, it hits 5. And it exactly is, at some
2 point, that first bias voltage, or the top bias voltage, and the bottom bias
3 voltage, absolutely is at the same value in both the pre-verify and the verify.
4 That is why they were making this argument in the POR about you have to
5 have a single level. Hongtao, in the other reference clearly discloses -- and
6 I'll go to the next page. Just like this on the next page, when it goes to the
7 program verification, it hits that, and then it goes up. But it's at the same
8 point -- that value's at the same point in a program -- in the pre-verify and
9 the verify.

10 So, if their argument has shifted from I'm not asking you to adopt a
11 single level in both, and just adopt that it has to be the same value at some
12 point in both, the prior art clearly discloses that, and we'd argue it's a proper
13 new argument, it's irrelevant because the prior art discloses it. This, in fact,
14 looks exactly like the positive value limitation.

15 I'll just say, very briefly, on Costa and Seo, they never said that Dr.
16 Liu is wrong. Their whole defense is, Seo doesn't expressly say that there's
17 this source building up. They never say that Dr. Liu is wrong. They admit
18 that. So, Dr. Liu's testimony is unrebutted, uncontested here that, in fact,
19 you have to, in Seo, use a regular Vpass voltage or you don't get Seo's effect
20 of HCI reduction.

21 JUDGE CYGAN: On to Mr. Hsu?

22 MR. HSU: Yes, Your Honor, I'll be brief. Going back to the
23 Suzuki ground, I want to just make one point. Just as T1 -- the Vpass in T1
24 to T2 is conditioning the channel for the program operation, and therefore is
25 part of the program operation, the Vpass in T3 to T4 is conditioning channel

1 for the removal of their electron and therefore is part of the recovery
2 operation.

3 JUDGE CYGAN: Okay. You have 12 minutes for sur-rebuttal.

4 MR. RADSCH: Thank you, Your Honor. I'm on Petitioner's slide
5 16 where they talk about paragraph 25 (INDISCERNIBLE). Hongtao does
6 not say that the voltage is applied -- simply applied to the gates of the
7 unselected memory cells. But they continually to admit is what it says next,
8 the voltage is applied, not on the gates directly, but through the unselected
9 word lines. The voltage goes from the driver, it's applied onto the word line,
10 and that's how it reaches, eventually, the memory cells. And again, the
11 claims require voltages be applied at a particular memory cell; that is, of the
12 selected memory string. To continually leave out these words, that it's
13 applied through the unselected word lines, and that's exactly what Hongtao
14 says.

15 Again, and that doesn't even begin to address though the fact that
16 what Hongtao's Figure 2 is, represents a target value. That type of slope
17 -- that waveform is not the actual waveform, either on the word line itself,
18 let alone on the particular gate of the selected memory string. That is simply
19 a representation of the target voltage waveform of the driver. And their own
20 expert acknowledges that, even as between the driver and the word line,
21 there's going to be RC delay so you're going to have a curved waveform
22 when you have a real waveform. This is not a real waveform. Again, it does
23 not say you apply the voltage to the gate. It's applied to the gate through the
24 word line.

25 And as Dr. Przybylski explained, there is RC delay on the word

1 line itself. They keep trying to minimize that word line delay. But, again,
2 going back to the reference they relied upon, I'm on Exhibit 1014. This is
3 the Table of Contents, chapter 8, challenges of 3-D NAND flash memory.
4 There's an entire section devoted to word line RC delay. That's what I just
5 explained earlier when it says, as compare to 2-D NAND, it's at page, I
6 believe 350 of this reference, 1014, the RC delay on the word line of 3-D
7 NAND is greatly increased. This is a real problem, and this is why you
8 cannot just assume that the waveform depicted on slide 16 here, on top
9 Figure 2, actually results in what is applied to the gate of a particular
10 memory cell on a particular selected line, or string rather.

11 And they talk about Figures 6 and 7 of the '957 Patent, that also
12 have these straight lines. That's true, but irrelevant. Those are also figures
13 that depict the target values. The difference between the '957 Patent and
14 Hongtao, is '957 Patent explains how to reach those target values, and
15 explains in prose that the second voltage, that is the voltage during the verify
16 period, is less than the voltage realized during the pre-verified period. It
17 would have the Board look at the figures in isolation, ignoring all of the
18 accompanying text and that, of course, is improper.

19 In turning to Patent Owner's slide number 21, they also say that,
20 well, Hongtao shows in its Figure 2, a ramp-up. Slide 21. Well, just
21 because -- I'm actually now on slide 20. They say, well, Hongtao shows a
22 ramp-up here, so that's addressing the ramp-up that would occur in a real
23 -- in a real waveform. But that doesn't suffice either.

24 I mean -- I'm now on slide 21. Figure 5 of the '957 Patent also
25 shows a ramp-up during the pre-pulse period. And what's critical there is,

1 that because there's insufficient time for that voltage to develop, it never
2 reaches its target.

3 So, simply because there is a ramp-up period doesn't ever mean
4 that the voltage target is realized at the gate terminal of a particular memory
5 cell string. And that is, again, the exact problem with Hongtao, it's silent as
6 to that pre-conduction period how long or how short it is. Again, it's silent
7 to having -- there's no explained reason for having any pre-conduction
8 voltage be higher during the pre-conduction phase than during the read
9 phase.

10 And I'll point the Board to paragraph 23 of Hongtao, where it
11 explains that the pre-conduction phase -- that the purpose of that is simply to
12 turn on channels of those word lines to simply apply a conduction voltage.
13 That conduction voltage is simply maintained at the read stage. As Dr.
14 Przybylski explained, the reason for that steep ramp is so that you achieve
15 that conduction voltage -- you turn it on more quickly. There's no reason for
16 the actual waveform to go up and then get it down again.

17 So, this notion again, that just because the Hongtao applies
18 voltages at the gates is insufficient to show that -- either that the waveform
19 in Figure 2 is the actual waveform, or that you can ignore that it's supplied
20 through the word line as Hongtao expressly says, they never explain the
21 relationship between the idealized target value and what actually results in
22 Hongtao's Figure 2.

23 Now, let me turn to the next issue, which is the difference -- this is
24 the second issue with respect to Ground 1, which is the motivation to
25 combine. Now, they're arguing that we have -- are somehow arguing against

1 bodily incorporation, but that simply is not the case. The purpose of the
2 explanation on slide 13 is that the verify operations and the read operations
3 of Hongtao and Yu are different. That's just -- that also supports the general
4 notion that those are different processes and they take different biasing
5 schemes, and so you don't simply take one and apply it to other because
6 they're different schemes. They don't explain, again, how you account for
7 those differences, they just point to the fact that there are some similarities,
8 and that is the reason that you would combine them. But they are taking the
9 particular waveforms from Hongtao and applying them into Yu's teachings.
10 That is a proposed combination. They never explained why one would take
11 those particular waveforms and use those particular waveforms in a
12 verification operation.

13 Now, going to their last argument, they've now introduced -- I'm
14 now on slide number 37. It's just a new theory now, apparently for claim 5,
15 arguing is their basis that we have somehow changed our proposed
16 construction. Our proposed construction is and always has been the same.
17 We cannot now introduce some new theory. There needs to be the
18 maintenance of the same voltage and the pre-pulse and verify stage, or the
19 pre-verify and verify stage. We've never said that it has to be during that
20 entirety of that period.

21 We now say that there's some rising portion during Hongtao that
22 would -- and I'm now on slide 44 of Patent Owner's demonstratives that
23 somehow meet that limitation. Again, that's a brand-new theory, but
24 moreover, they're not showing how that would meet the claim language of
25 applying a particular bias voltage on a particular gate. That's simply their

1 ramp-up. They never -- they have no expert testimony, no explanation
2 anywhere in the papers, let alone in their rebuttal arguments, how that would
3 satisfy applying a particular bias voltage, let alone a processing circuitry
4 configured to apply that voltage, and that's simply passing through the ramp-
5 up stage.

6 And again, the arguments do not address the fact that, undisputed,
7 once again, that the type of waveform shown in Figure 2 is representative of
8 a target waveform, not the waveform it actually develops on a word line, let
9 alone the waveform that actually develops at the gate of a particular selected
10 memory string.

11 With the remaining minutes, let me pass the podium to Mr. Bonny
12 to address issues with respect to the remaining ground.

13 MR. BONNY: So, I'll just address a couple of the points that were
14 raised with respect to Grounds 2 and 3. So, for Ground 2, which was -- or
15 Ground 3, rather, which was Costa in view of Seo, the main assertion that
16 was raised just now, is that, we, Petitioner, or sorry, Patent Owner and Dr.
17 Przybylski never say that Dr. Liu is wrong about the effects that are
18 described with respect to the -- why you would keep the voltage high on the
19 first time period in Seo. But, in fact, Dr. Przybylski explained in paragraph
20 160 of his declaration, why he disagreed with the opinions of Dr. Liu.

21 And to add to that though, even if you accepted at face value with
22 no support in any of the references, even if you were to accept the assertions
23 of Dr. Liu, that still doesn't explain why you would selectively apply a
24 teaching to lower voltage to just the second time period and not the first time
25 period. Because the goal of what Costa describes, what it teaches, that a

1 lower voltage value can be used to turn on unprogrammed memory because
2 of their lower threshold voltage, that would still apply equally to both time
3 periods.

4 The other issue that I just wanted to briefly touch on was the
5 obviousness to try argument, and this is on slide 35. As we explained in our
6 briefing, there's two issues with this argument. First, this requires, not just
7 showing that there are a finite number of options, but those options must be
8 known and they haven't shown that. And second, as we explained in our
9 briefing, it's more than just a binary choice, there's actually numerous
10 options -- an infinite number of options and time periods.

11 And I see that we're out of time, so I'll end it there.

12 JUDGE CYGAN: I'd like to thank counsel for both parties today
13 for their presentation, especially for your excellent command on the record.
14 It's very helpful for us in coming to our determination. Also, again, I'd like
15 to compliment your colleagues, who did a great job on the demonstrative
16 exhibits. I'd like to also compliment our hearing staff for reconnecting and
17 working through problems, in general, doing an excellent job. A final
18 decision will be issued in due course. The hearing is concluded, but please
19 stay to answer any questions the court reporter may have.

20 (Whereupon, the above-entitled matter went off the record at 3:26
21 p.m.)

IPR2024-00792
Patent 11,468,957 B2

PETITIONER:

Jeremy Jason Lang
K. Patrick Herman
Travis Jensen
Johannes Hsu
ORRICK, HERRINGTON & SUTCLIFFE LLP
ptabdocketjl2@orrick.com
p52ptabdocket@orrick.com
t61ptabdocket@orrick.com
ptabdocketj1h1@orrick.com

PATENT OWNER:

James L. Davis, Jr.
Andrew Radsch
Christopher M. Bonny
Abed R. Balbaky
ROPES & GRAY LLP
james.l.davis@ropesgray.com
andrew.radsch@ropesgray.com
christopher.bonny@ropesgray.com
abed.balbaky@ropesgray.com